Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **N1512-01** Date: January 8, 2016
Product Affected: 8725AM-21LF(T)

Date Effective: April 8, 2016

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ■ Product Mark Change in ordering part#
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: TSD Clock Team
E-mail: clocks@idt.com

Attachment: ■ Yes ☐ No
Samples: Samples are available now.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ■ Other - Die Revision Change

This notice is to advise our customers that the IDT Part 8725BM-21LF(T) is an updated version of the 8725AM-21LF(T) to improve the VCO stability for an overall better performance.

There is a minor change to the top metal. The is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 3.

We are requesting a last time buy of the previous version by April 8, 2016.

RELIABILITY/QUALIFICATION SUMMARY:

There is no change in die technology/process.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT 1 - PCN #: N1512-01

PCN Type: Die Revision Change / Datasheet

Data Sheet Change: Yes

Detail of Change: This notice is to advise our customers that the IDT Part 8725BM-21LF(T) is an updated version of the 8725AM-21LF(T) to improve the VCO stability for an overall better performance.

There is a minor change to the top metal. The is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 3.

We are requesting a last time buy of the previous version by April 8, 2016.

Table 1

Old Ordering Part Number	New Ordering Part Number
8725AM-21LF	8725BM-21LF
8725AM-21LFT	8725BM-21LFT

Qualification Test Plan and Result:

Qual Vehicle: 8725BM-21LF

Test Description	Test Method (Latest specs in effect)	Test Results (SS / Rej)
ESD: Human Body Model @ 2000V	Each IO Pin Individually to I/O	3/0
ESD: Charged Device Model @ 1500V	JESD22-C101	3/0
Latch-up	JESD78	6/0

Datasheet Comparizon

FROM **rev A**

8725-21 / COMMERICAL temperature range

Table 6. AC Characteristics, VDD = VDDA = 3.3V ± 5%, VDDO = 1.8V ± 0.2V, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				630	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ≤ 700MHz	3.2		4.5	ns
t sk(Ø)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-95	30	155	ps
t sk(o)	Output Skew; NOTE 3, 5	PLL_SEL = 0V			50	ps
t jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				35	ps
t jit(θ)	Phase Jitter; NOTE 4, 5, 6				±50	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - 85	t_{PERIOD}/2	t_{PERIOD}/2 + 85	ps

All parameters measured at fMAX unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Characterized at VCO frequency of 622MHz.

TO **rev B**

8725BI-21 / INDUTRIAL Temperature Range

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				630	MHz
t_{PD}	Propagation Delay[3]	PLL_SEL = 0V, f ≤ 630MHz	3.2		4.5	ns
t sk(Ø)	Static Phase Offset[4, 5]	PLL_SEL = 3.3V	-125	37.5	200	ps
t sk(o)	Output Skew[5, 6]	PLL_SEL = 0V			50	ps
t jit(cc)	Cycle-to-Cycle Jitter[5, 7]				50	ps
t jit(θ)	Phase Jitter[5, 7, 8]				±50	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
t_{PW}	Output Pulse Width		t_{PERIOD}/2 - 90	t_{PERIOD}/2	t_{PERIOD}/2 + 90	ps

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. All parameters measured at fMAX unless noted otherwise

NOTE 3. Measured from the differential input crossing point to the differential output crossing point.

NOTE 4. Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 5. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 7. Characterized at VCO frequency of 622MHz.

NOTE 8. Phase jitter is dependent on the input source used.