

Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN) ADDENDUM

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PCN #:L9910-03R1DATE:May 22, 2000Product Affected:Selected 3.3V Double Density Logic FCT Devices (See Below For Detail Part Nos.)Manufacturing Location Affected:N/ADate Effective:June 22, 2000		 MEANS OF DISTINGUISHING CHANGED DEVICES: Product Mark Back Mark Date Code Prefix from "N" or "L" to "X" Other 		
Contact: Bimla Paul				
Title: Product Assurance Ma	anager	Attachment::	Yes	No No
Phone #: 408-654-6419				
Fax #: 408-492-8362		Samples:	Available upon request	
E-mail: bimla.paul@idt.com			and appening upon	
DESCRIPTION AND PURPOSE	OF CHANGE:			
Die Technology				
■ Wafer Fabrication Process	For selected 3.3V Double De		-	-
Assembly Process Equipment	die revision for process conse change. This PCN Addendum		-	ons or package
 Equipment Material 	change. This PCN Addendum	n replaces PCIN # L	JJ10-0J.	
□ Testing	Additional affected part num	bers are: 74FCT16	3373, 163374, 163543	163601 & 163952
□ Manufacturing Site	Please see attachment for the			
Data Sheet			-	
□ Other				
Qualification and reliability data will CUSTOMER ACKNOWLEDGM IDT records indicate that you requine to grant approval or request addition it will be assumed that this change in IDT reserves the right to ship either on the earlier version has been depl	ENT OF RECEIPT: re written notification of this c nal information. If IDT does n is acceptable.	ot receive acknowle	edgement within 30 days	s of this notice
Customer:	D	Approval fo	or shipments prior to) effective date.
Name/Date:	E-1	Mail Address:		
Title:	Ph	one#/Fax#:		
CUSTOMER COMMENTS:				
IDT ACKNOWLEDGMENT OF	RECEIPT·			
RECD. BY:		DATE:		_
IDT FRC-1509-01 REV. 05 03/28/0	00 Page 1	of 1	ŀ	REFER TO QCC-1795

ATTACHMENT



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PCN Summary PCN Type

ren Type:	Design Change Change to Fab Process	
Commodity	Logic	
Forecast or Execute	Execute	
Planned or Unplanned	Unplanned	
Data Sheet Change	No Change	

Detail of Change

For selected 3.3V Double Density Logic FCT products, IDT will be migrating to a new die revision for process consolidation. There is no data sheet specification or package change.

The affected part numbers are: 54/74FCT163344, 163501, 163827, 163646, 163244, 163245, 74FCT163373, 163374, 163543, 163601 and 163952

Process / Design Changes

	Current Die		Replacment Die
	54/74FCT163344 54/74FCT163501 54/74FCT163827 74FCT163543 74FCT163601 74FCT163952	54/74FCT163646 54/74FCT163244 54/74FCT163245 74FCT163373 74FCT163374	
Wafer Fab Technology Feature Size Minimum Gate Oxide Wafer Size Die Dimension (sq mils) Fab Facility Datecode Prefix Designator	CMOS 7 0.8µm 140 Å 6" 11.4 Fab 2 N	CMOS 7 0.8µm 140 Å 6" 6.28 Fab 2 L	СМОЅ 8 0.6µm 140 Å 6" 7.76 Fab 2 X

Conversion schedule (Estimated)

PCN # L9910-03R1

Sample Availability

Production Shipments

54/74FCT163344 54/74FCT163501 Available Available

February 1, 2000 February 1, 2000



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54/74FCT163646	Available	February 1, 2000
54/74FCT163827	Available	February 1, 2000
54/74FCT163244	Available	February 1, 2000
54/74FCT163245	Available	February 1, 2000
74FCT163373	Available	June 22, 2000
74FCT163374	Available	June 22, 2000
74FCT163543	Available	June 22, 2000
74FCT163601	Available	June 22, 2000
74FCT163952	Available	June 22, 2000

Qualification Data

Test Vehicle: 65501X/65373X/65244X/65646X

	Lot #1	Lot #2	Lot #3
Operating Life Test (Dynamic)	116/0	116/0	116/0
(1000 Hrs @125°C, Vcc = $3.3V$) Temperature cycling (-65°C to +150°C, 500cyc)	45/0	45/0	45/0
Bake and Ball Shear Test	20/0	20/0	20/0
Die Shear Test	3/0	3/0	3/0
ESD: HMB Category II (>2kV) Mil-Std 883, Method 3015	3/0	3/0	3/0
ESD: CDM	3/0	3/0	3/0
Latch-up JEDEC Std 17	10/0	N/A	N/A
Electrical characterization	10/0	N/A	N/A
I/O capacitance	5/0	N/A	N/A

Characterization Data:

Characterization Data is available upon request.