

Technical Brief

July 10, 2003

TB410.1

General Description



The EL4511 demo board is designed for demonstrating the operation of Elantec's super sync separator. The

user can evaluate the demo board with or without the software interface. For a detailed description, please refer to the data sheet.

On the board, the power pins V_{CCD}, V_{CCA1}, and V_{CCA2} are connected together as V_{CC}. C₁ and C₂ are 0.1µF ceramic small signal bypass capacitors for those pins. C₆ is a 4.7µF Tantalum power bypass capacitor.

 $H_{IN},$ SYNCIN, and V_{IN} are the three line sync signal inputs. For YUV or RGB applications, Y or G should be connected to SYNCIN input. For applications with separate horizontal and vertical sync inputs, these should be connected to the H_{IN} and V_{IN} pins. Composite video input signals should be connected to SYNCIN pin. R_8 is 75 Ω termination resistor and C_3 is 0.1 μ F AC coupling capacitor. R_{11} is 10k Ω pull up resistor to enable the chip when the switch is close.

The LEVEL pin indicates 2X the amplitude of the sync tip vs back porch. Logic high at the SYNCLOCK pin indicates the sync has locked to the line rate. SYNCOUT, BACKPORCH, V_{OUT}, H_{OUT}, ODD/EVEN, and VBLANK are the logic outputs for the sync separator.

X1 is a 32.768kHz crystal. The XTAL and XTALN pins are the crystal input and output pins. By default setting, the crystal oscillator is disabled (Reg9, bit6 is 0). The Mode control bits in Reg1 and the sample cut-off mode in Reg2 are overridden by the values on XTAL pin and XTALN pin. See Table 1 for operation details. Switches S₂, S₃ can be used to change the states at those two pins.

SDENB, SCL, and SDA are the three line serial interface pins.

Driver Section

The SN74ACT1284 chip is used to increase the logic signals from the parallel port and the EL4511 chip. R₁, R₂, an R₃ are the pull-up resistors. R₅, R₆, and R₇ are 1k Ω resistors to protect the inputs of EL4511's serial interface pins. R₄ is 499 Ω from the PC ground to the demo board ground.

Software Control

The EL4511 demo board uses the supplied Visual Basic executable file and the parallel port to write and read the data stream for serial interface. Please refer to the data sheet for a detailed description of the logic table and the timing diagram. From the EL4511 Driver disk, copy the EL4511.exe to your window desktop. If your operating system is Win98, copy the files "ntport.dll" and "zntport.sys" to C:\windows\system. If your operating system is Win2000, Windows XP, or Windows NT, just copy the files "ntport.dll" and "zntport.sys" to C:\winnt|system32. To open the program, just double-click the EL4511.exe icon. A control panel appears (see Figure 1.) From the panel, the user can write data to register 1, 2, 3, 4, 5, 6, 9, and 10 and read data from register 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 13, 14, 15, and 16 individually.

Evaluation Instructions

Evaluate with the crystal oscillator is disabled.

- 1. Apply 5V to V_{CC}, PC_V_{CC}.
- 2. Set the states for XTAL and XTALN pins, which depends on the test signals. See Table 1.
- Apply the test video signal to the inputs: SYNCIN for composite video signal; for separate horizontal and vertical sync inputs, these should be connected to H_{IN} and V_{IN} respectively.
- 4. Check that SYNCLOCK pin is held high continuously.
- 5. Measure the DC level at the LEVEL. It should be ~2X the sync tip amplitude (~560mV for NTSC/PAL).
- 6. Confirm operations of all sync separator outputs.
- 7. Load the EL4511.exe program and connect the parallel port from your computer to the demo board. Write data to or read data from the registers.

Evaluate with the crystal oscillator is enabled.

- 1. Apply 5V to V_{CC} , PC_V_{CC} .
- Apply the test video signal to the inputs: SYNCIN for composite video signal; for separate horizontal and vertical sync inputs, these should be connected to H_{IN} and V_{IN} respectively.
- 3. Load the EL4511.exe program and connect the parallel port from your computer to the demo board. Set bit6 in Reg9 to high to enable the crystal oscillator. Program the registers.
- 4. Check that SYNCLOCK pin is held high continuously.
- 5. Measure the DC level at the LEVEL. It should be ~2X the sync tip amplitude (~560mV for NTSC/PAL).
- 6. Confirm operations of all sync separator outputs.

ENXTAL REG9 (BIT 6)	XTAL PIN 1	XTALN PIN 24	MODE CONTROL REG1 (BIT 5:3)	SAMPLE CUT-OFF REG2 (BIT 0)	DESCRIPTION (CRYSTAL OSCILLATOR)	
1	х	Х	Reg1 (5:3)	Reg2 (0)	Enabled, normal operation	
0	0	0	000	0	Disabled, all signal types allowed	
0	0	1	011	0	Disabled, tri-level only	
0	1	0	101	1	Disabled, bi-level only	
0	1	1	111	1	Disabled, H _{IN} only	

EL4511 Demo Board



É EL4511C		_ 🗆 🗙
Parallel Port		
I DIST Speed	Quit	
Registors MS Address LS Data Bit LS HexWrit	e MS DataRead LS	HexRead
MS Address Data Bit LS	MS DataRead LS	
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Reg18 Image: Constraint of the second s	MS DataRead LS	

FIGURE 1. WINDOWS CONTROL PANEL

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