ISL70062SEH

PSpice Simulation Results

Abstract

The ISL70062SEH Pspice model is a nominal model of the ISL70062SEH load switch IC. It simulates the load switch functionality and the typical performance across temperature of the datasheet specification parameters. Basic ON/ OFF Control, Undervoltage Lockout (UVLO), Reverse Current Protection (RCP), selectable discharge MOSFET feature, and slow turn-on controlled rise time functions are modeled. The model simulations closely match the typical performance curves in the datasheet.

The first section of this document provides a brief explanation of using the model to generate a general functional test simulation.The simulation shows the functionality of ON/OFF control, UVLO, slow turn-on rise time, and the selectable discharge MOSFET feature.

The second section shows Pspice simulation results of the load switch compared to characterization test results using the ISL70062SEHEV1Z evaluation board. Parameters for r_{ON} vs V_{SWI} vs temperature, r_{ON} vs I_{SW} vs temperature, turn-on and turn-off waveforms, and I_{RCP} enter vs V_{SWO} vs temperature response are compared.

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Related Literature

For a full list of related documents, visit our website:

- ISL70062SEH and ISL73062SEH device pages

1. PSpice General Functional Test Simulation

The simulation shown in Figure 4 shows how the ISL70062SEH PSpice model replicates the load switch functionality for basic on/off control, Undervoltage Lockout (UVLO), the selectable discharge MOSFET feature, and slow turn-on controlled rise time.

1.1 ISL70062SEH.LIB and ISL70062SEH.OLB PSpice Files

The PSpice ISL70062SEH.LIB and ISL70062SEH.OLB files can be downloaded from the Renesas website at the ISL70062SEH and ISL73062SEH device pages under the **Download** tab. The file path to the ISL70062SEH.OLB sub-circuit Figure 1 must be added to the Cadence parts placement tool. It can then be used in simulation schematics. The ISL70062SEH.LIB file path must be added to the Cadence simulation profile as shown in Figure 2. Renesas uses Cadence Allegro Design Entry CIS 16.6-S071 (v16-6-112FZ).

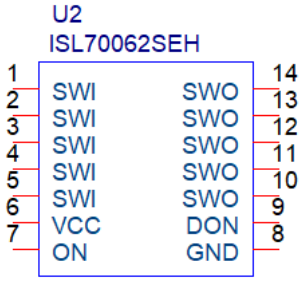

Figure 1. ISL70062SEH Sub-Circuit (ISL70062SEH.OLB)

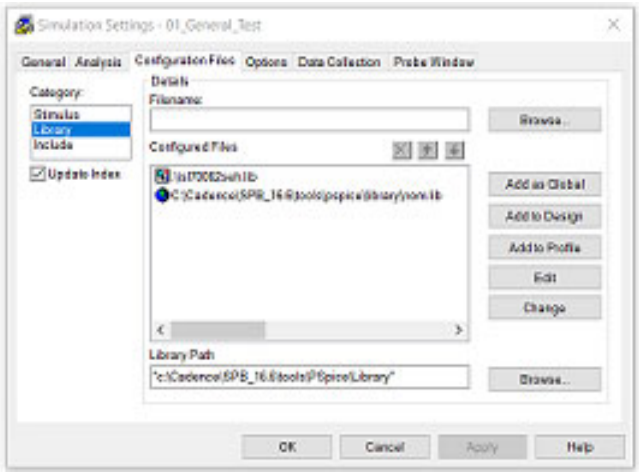

Figure 2. ISL700062SEH.LIB

1.2 Functional Simulation Schematic

Figure 3 shows the PSpice simulation schematic used for the functional simulation test.

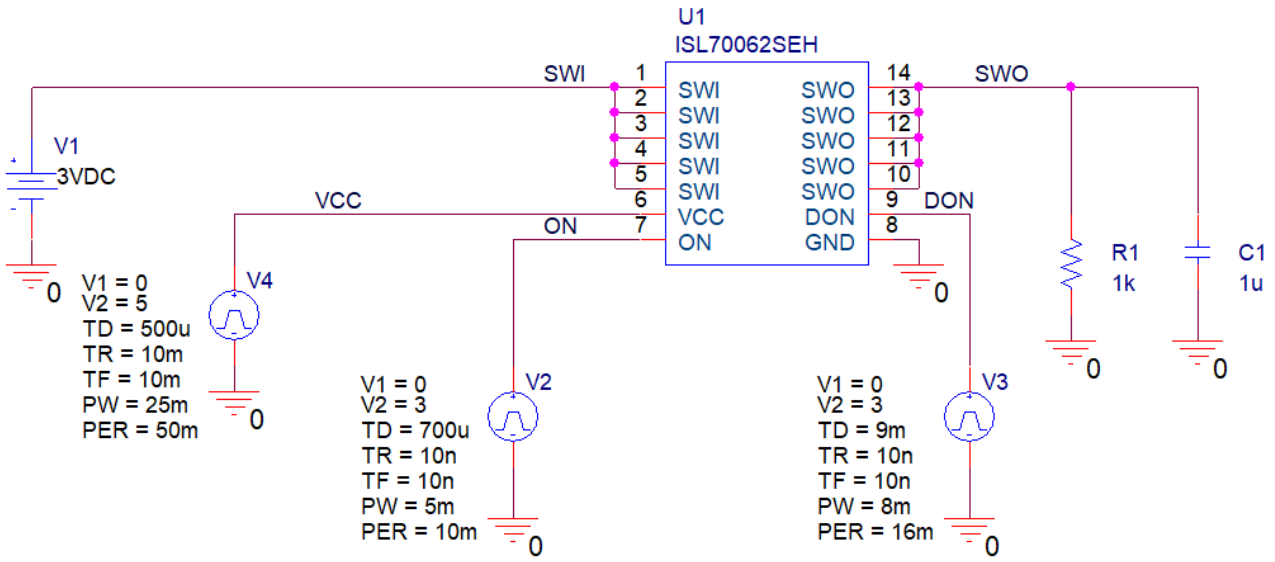

Figure 3. ISL70062SEH PSpice General Functional Test Schematic

1.3 Functional Simulation Results

Figure 4 shows the time-domain transient simulation results for the functional test. VCC (blue trace), DON (red trace), ON (green trace), and SWO (black trace) vs Time are the plots shown. The functional states of the load switch are indicated by the numbers 1-6 on the SWO plot. The functional states relate to the numbers 1-6 as follows:

1. The part is in the UVLO off state. Because the VCC voltage is below the UVLO falling threshold of 2.2V the switch is OFF even though ON = High.
2. When the VCC voltage reaches the UVLO rising threshold voltage of 2.3V, the part is no longer in the UVLO state and because ON = High, the switch turns ON.
3. ON = Low and the switch turns OFF. The output slowly decays to ground. The 1kΩ load resistor with the 1µF load capacitance connected at the output slowly decays the output to ground.
   Note: DON = Low (discharge MOSFET circuitry is disabled).
4. ON = High and the switch turns ON with a controlled rise time of ≈ 2.2ms.
5. DON = High (discharge MOSFET circuitry is enabled), ON = Low: The switch turns OFF. The internal 100Ω discharge resistor quickly discharges the output to ground.
6. The part enters the UVLO off state. Because the VCC voltage is below the UVLO falling threshold voltage of 2.2V, the switch is OFF even though ON = High.

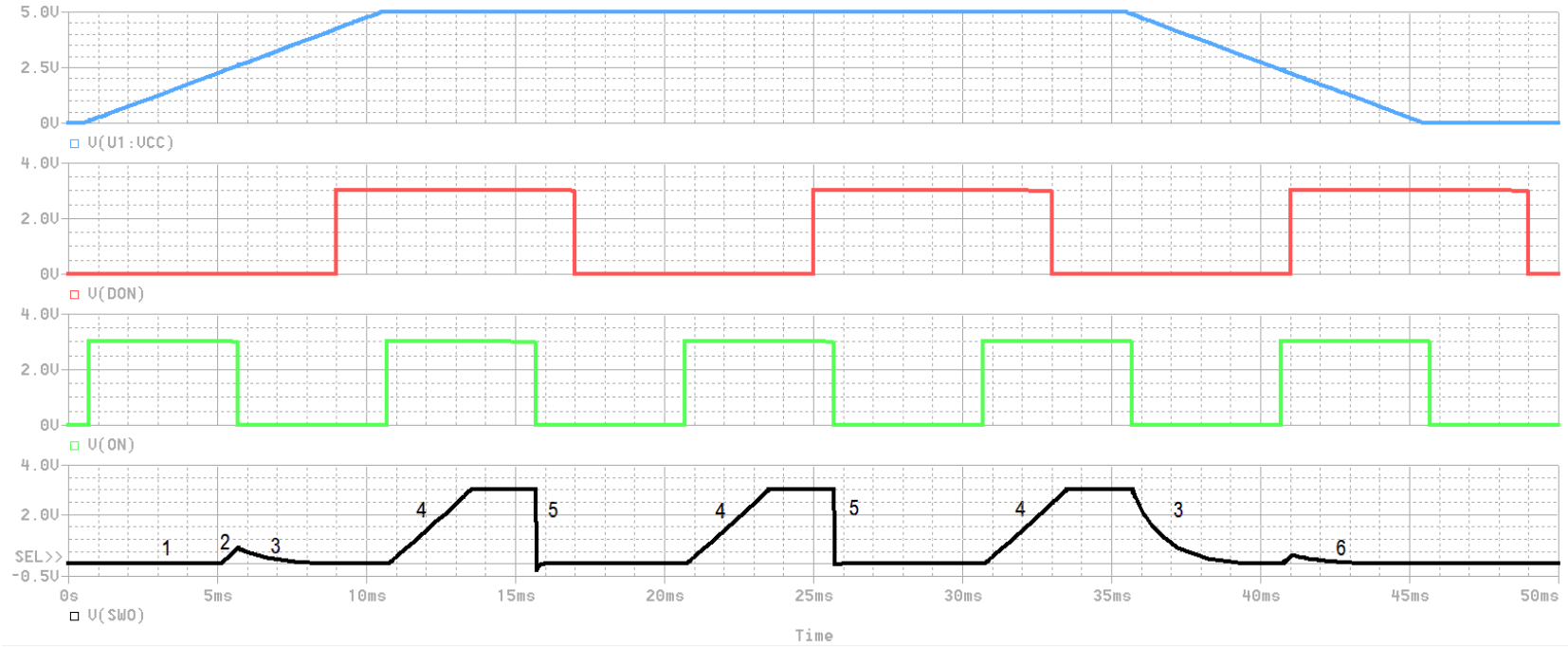

Figure 4. ISL70062SEH Pspice General Functional Simulation Results

2. PSpice Simulation Results Verses Characterization Test Results

The ISL70062SEH PSpice model was designed to meet the typical values across temperature of the specification parameters in the ISL70062SEH data sheet. Pspice simulations closely match the typical performance curves in the data sheet. This section, for a few parameters, provides a comparison between the PSpice simulation results and actual part characterization test results.

Figure 5 - Figure 22 shows the Pspice simulation results vs the load switch characterization test results for r_{ON} vs V_{SWI}, r_{ON} vs I_{SW}, turn-on and turn-off timing, and the RCP enter response.

For a particular parameter, the graph on the left is the PSpice sims result and the graph on the right is the characterization result. For example: Figure 5 is the PSpice result and Figure 6 is the characterization result for r_{ON} vs V_{SWI} vs temperature with V_{CC} = 5.5V. You can quickly compare the graphs to see how the PSpice simulation result correlates with the characterization test result.

2.1 r_{ON} vs V_{SWI} vs Temperature

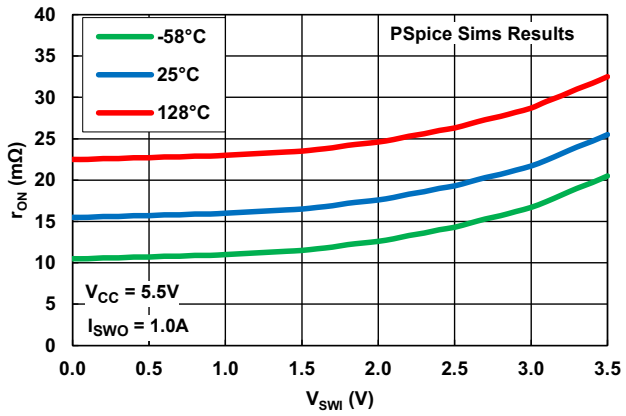

Figure 5. r_{ON} vs V_{SWI} vs Temperature, V_{CC} = 5.5V (PSpice Results)

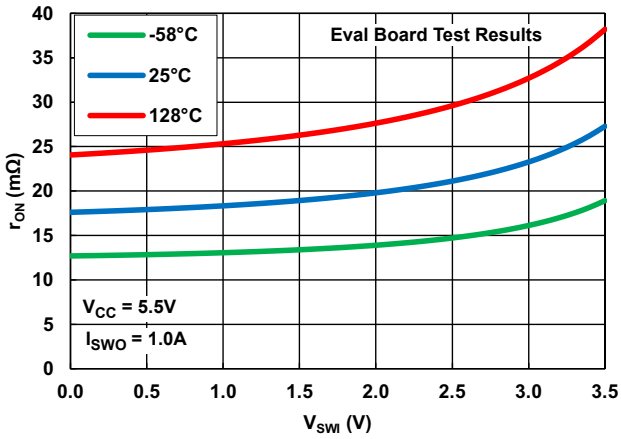

Figure 6. r_{ON} vs V_{SWI} vs Temperature, V_{CC} = 5.5V (Characterization Results)

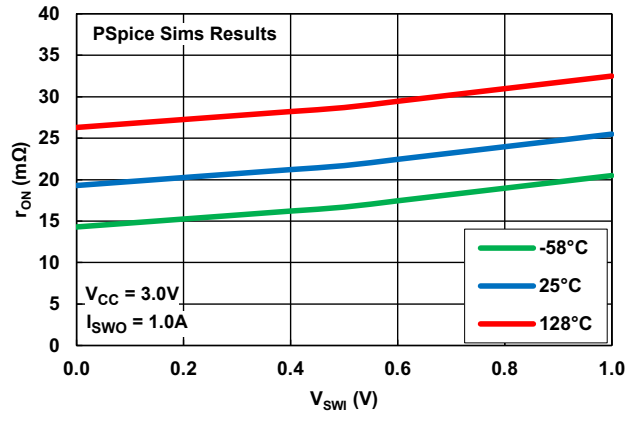

Figure 7. r_{ON} vs V_{SWI} vs Temperature, V_{CC} = 3.0V (PSpice Results)

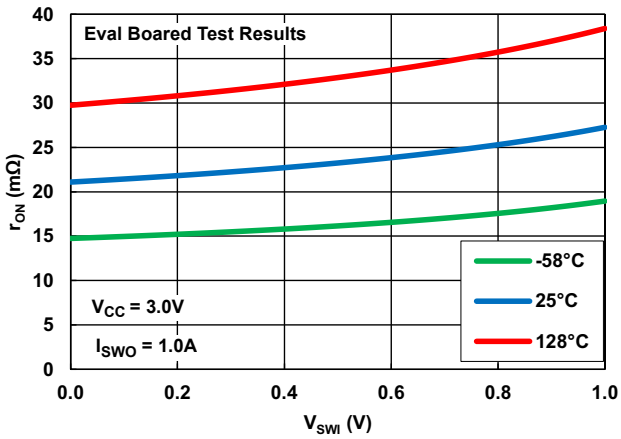

Figure 8. r_{ON} vs V_{SWI} vs Temperature, V_{CC} = 3.0V (Characterization Results)

2.2 r_{ON} vs I_{SWO} vs Temperature

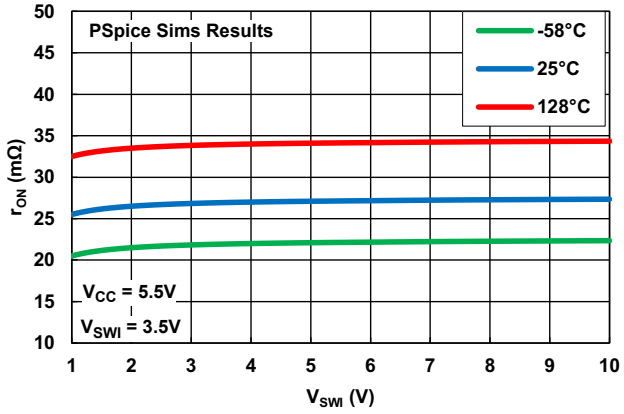

Figure 9. r_{ON} vs I_{SW} vs Temperature, V_{CC} = 5.5V (PSpice Results)

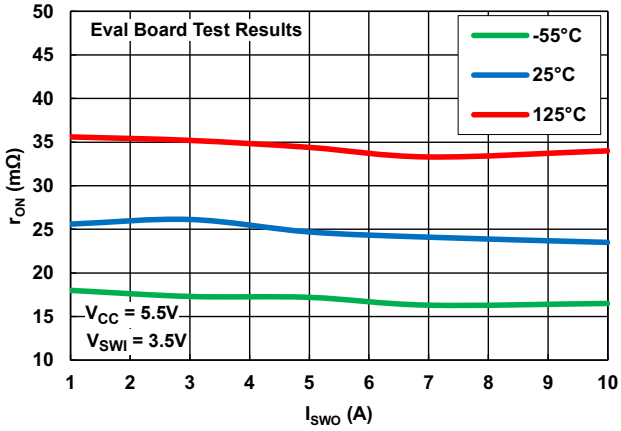

Figure 10. r_{ON} vs I_{SW} vs Temperature, V_{CC} = 5.5V (Characterization Results)

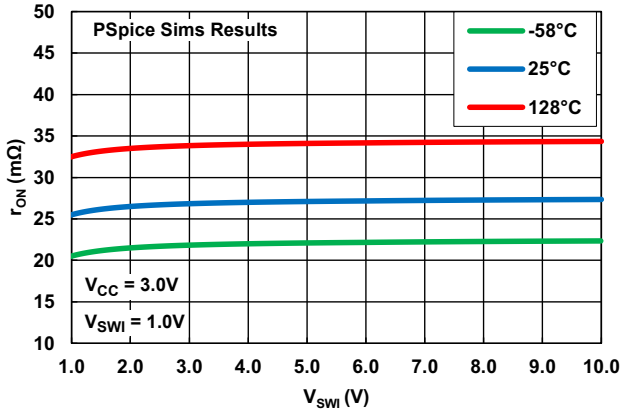

Figure 11. r_{ON} vs I_{SW} vs Temperature, V_{CC} = 3.0V (PSpice Results)

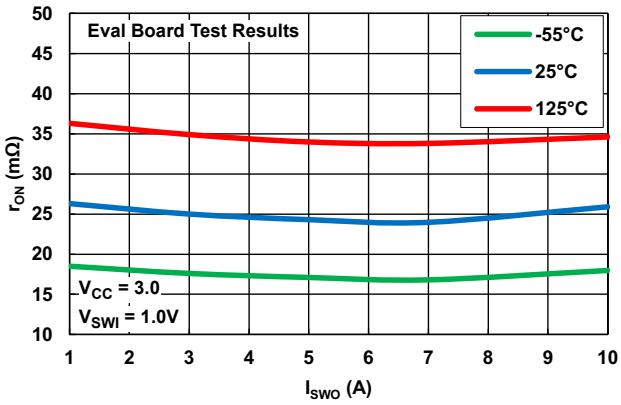

Figure 12. r_{ON} vs I_{SW} vs Temperature, V_{CC} = 3.0V (Characterization Results)

2.3 Turn-ON and Turn-OFF Waveforms

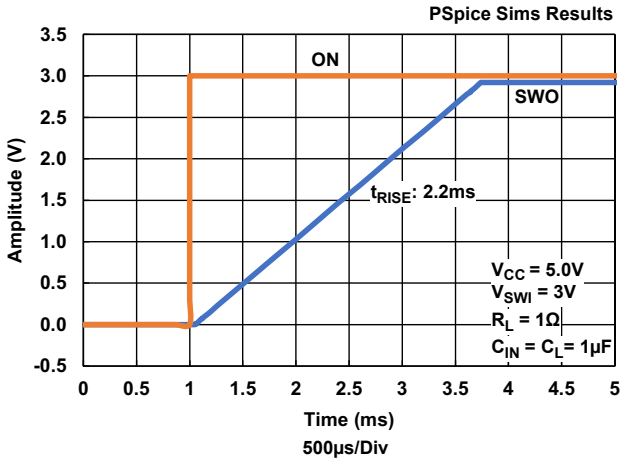

Figure 13. Turn-On Waveform, V_{SWI} = 3V, C_L = 1µF (PSpice Results)

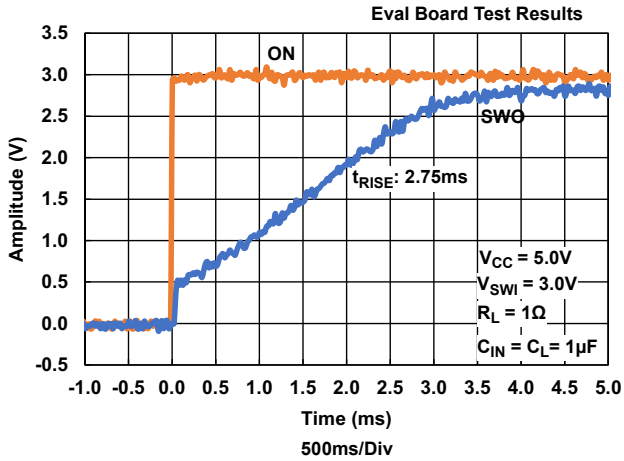

Figure 14. Turn-On Waveform, V_{SWI} = 3V, C_L = 1µF (Characterization Results)

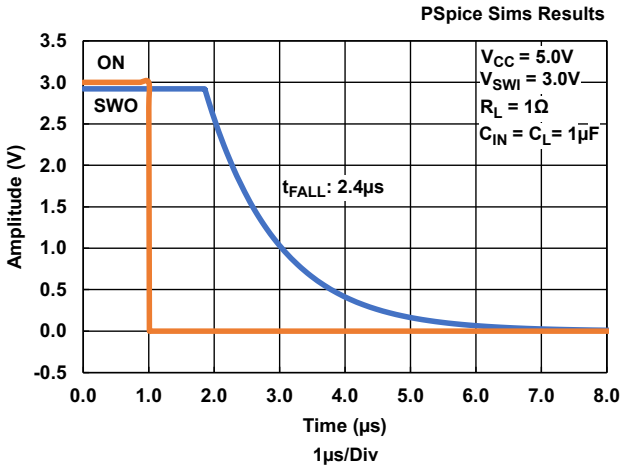

Figure 15. Turn-Off Waveform, V_{SWI} = 3V, C_L = 1µF (PSpice Results)

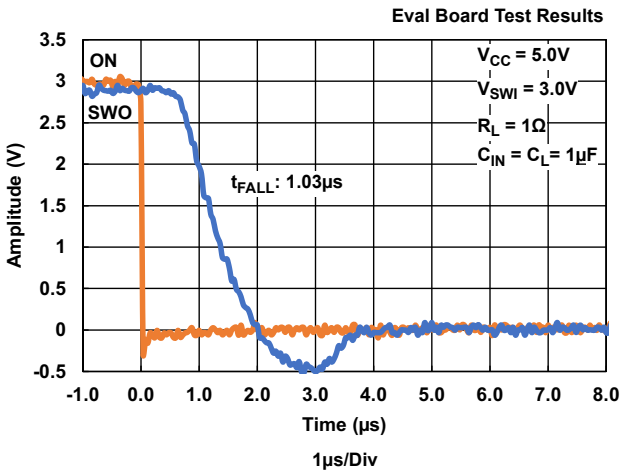

Figure 16. Turn-Off Waveform, V_{SWI} = 3V, C_L = 1µF (Characterization Results)

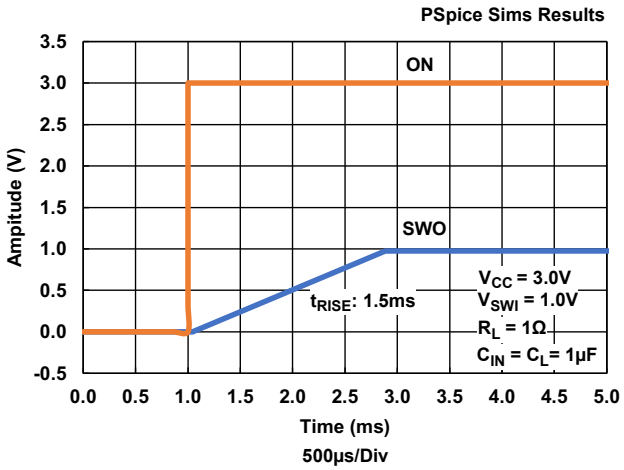

Figure 17. Turn-On Waveform, V_{SWI} = 1V, C_L = 1µF (PSpice Results)

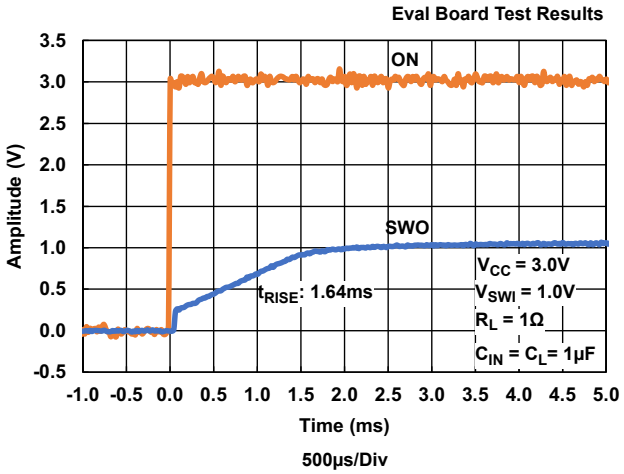

Figure 18. Turn-On Waveform, V_{SWI} = 1V, C_L = 1µF (Characterization Results)

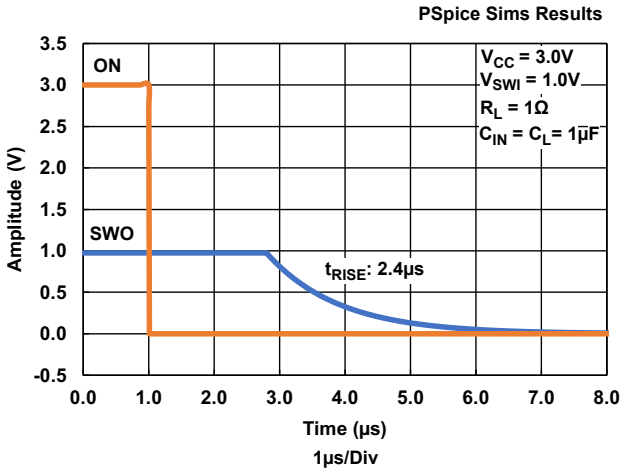

Figure 19. Turn-Off Waveform, V_{SWI} = 1V, C_L = 1µF (PSpice Results)

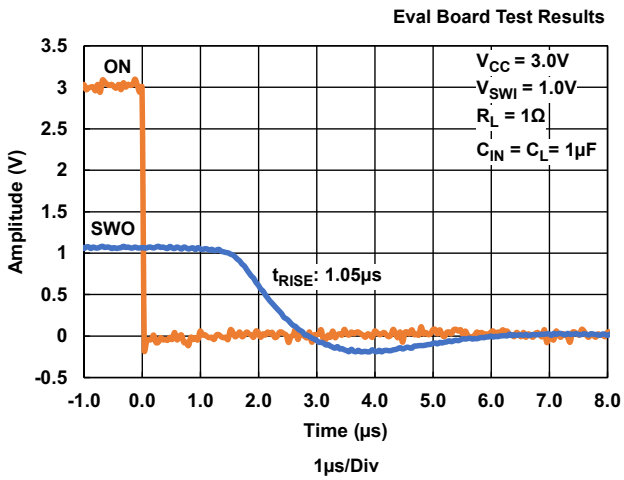

Figure 20. Turn-Off Waveform, V_{SWI} = 1V, C_L = 1µF (Characterization Results)

2.4 Reverse Current Protection (RCP) Waveforms

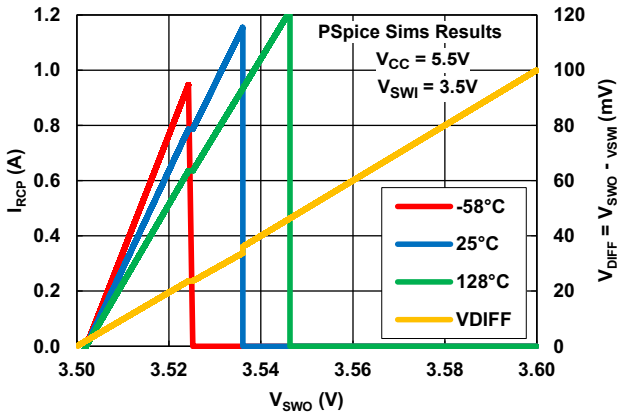

Figure 21. I_{RCP} Enter vs V_{SWO} vs Temperature, (PSpice Results)

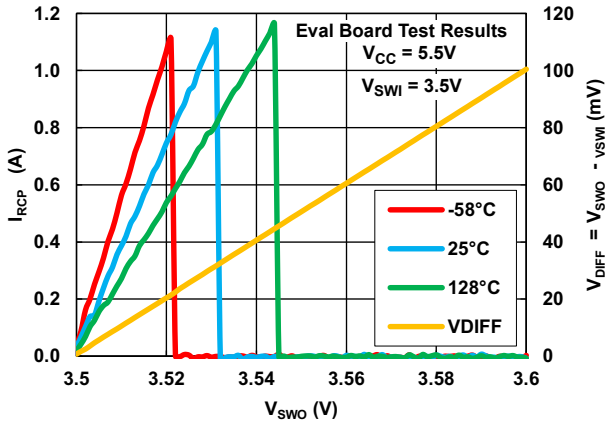

Figure 22. $_{RCP}$ Enter vs V_{SWO} vs Temperature, (Characterization Results)

2.5 Conclusion

The ISL70062SEH PSpice model replicates the functionality of the ISL70062SEH load switch. It closely matches the characterization curves in the ISL70062SEH datasheet and meets the typical values across temperature of the parameters in the datasheet specification table.

3. Revision History

Rev.	Date	Description
1.00	Mar.6.20	Initial release

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