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April 1st, 2010
Renesas Electronics Corporation

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Low-Voltage CMOS Logic HD74LV_A/LVC Series

Definition

1. Loading Circuit

For the AC loading circuit used in characterizing and specifying propagation delays of all HD74LV-A/LVC/LVC-A series devices, please refer to individual data sheets. The loading capacitance of 50 pF allows more leeway in stray capacitance and also serves as a load to the device during rising and falling output transitions. This more closely resembles the loading to be expected in average applications and thus gives the designer more useful delay estimations. In HD74LVC/LVC-A series devices the 500 Ω of resistor to ground can be a passive prove for an oscilloscope. In another word, the 500 Ω resistor to ground can be a series of a 450 Ω resistor and a sampling oscilloscope with 50 Ω internal termination through a 50 Ω coaxial cable. And, the device input pin is connected with the other input to the sampling oscilloscope through a cable of the same impedance. It equivalents to terminating output of pulse generator signal with 50 Ω. And HD74LV-A series devices, load resistor of 1 kΩ is connected between Output and GND, and measurement pins are connected to oscilloscope through probes (impedance is more than 1 MΩ).

In HD74LV-A/LVC/LVC-A series AC loading circuit, another resistor (500Ω: HD74LVC/LVC-A series, 1 kΩ: HD74LV-A series) is used between the output of a tested device and a switch. During the measurement of propagation delay, this switch is open, and to measure enable and disable time of three-state output it is connected to GND (high to off, off to high) or 6 V supply (low to off, off to low).

Output pins voltage will be quiescent low level when this switch is connected to GND, and connection with 6 V supply divided the 6 V voltage by two resistors (500 Ω: HD74LVC/LVC-A series, 1 kΩ: HD74LV-A series) to make output pins quiescent high level.

Please refer to figures from 1 to 5 for definitions of AC test waveforms.

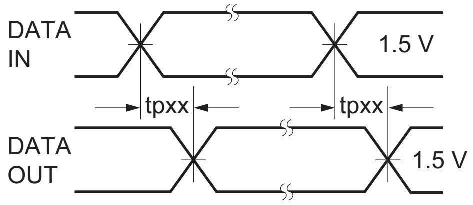

Figure 1 Propagation Delay Time

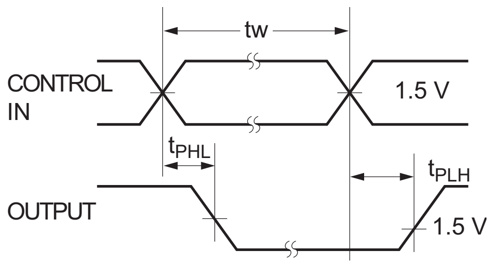

Figure 2 Propagation Delay Time and Pulse Width

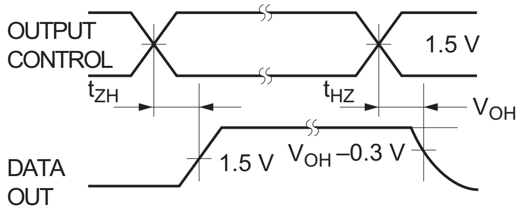

Figure 3 Three-State Output : t_{ZH}, t_{HZ}

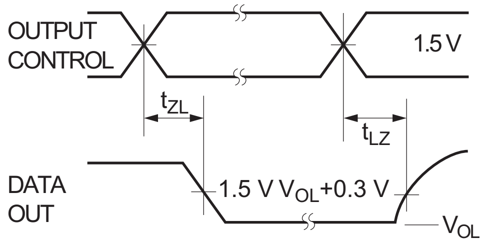

Figure 4 Three-State Output : t_{ZL}, t_{LZ}

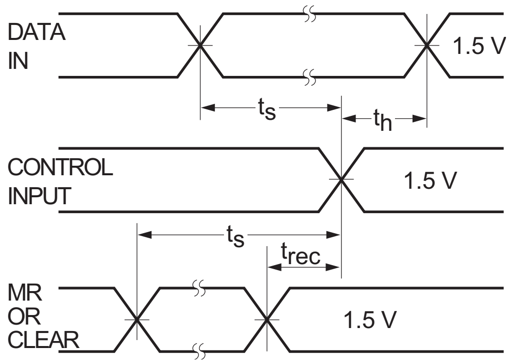

Figure 5 Set Up Time and Hold Time

2. Test Conditions

The AC test conditions take 0V as low level and 2.7V for high level. And input rising and falling time is defined to be 2.5 ns, and 1 ns at maximum clock frequency and pulse-width measurements. DC characteristics tests use V_{IH} and V_{IL} defined in specifications for input voltages. On test, adequate decoupling of power supplies is required to eliminate the influence of noise. Special attention must be paid when an IC tester or a handler is used. To improve the noise margin for testers' inherent noise which does not occur in the actual system, DC input levels may need to be adjusted. Noise immunity testing is performed by raising V_{IN} to the supply voltage, V_{CC} then dropping it to a level corresponding to V_{IH}, and then raising it again to the VCC level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL}, then returning it to 0 V. Confirm that no changes appear at outputs when input levels reach V_{IH} or V_{IL}. On fabricating test jigs and tools, high frequency characteristics should be sufficiently considered for wirings. Leads on the load capacitor should be as short as possible to evaluate ripples and undershoot on output waveforms. Generous ground metal or preferably a plane ground should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

3. Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Devices with two or more outputs will delay by about 400 PS (HD74LVC/LVC-A Series) or 200 PS (HD74LV-A Series) than the specification in datasheet for each increase of simultaneously switching outputs. This effect is not significant on an octal devices unless more than four outputs are switching simultaneously. This derating is applied for the entire temperature range from –40 to 85°C and V_{CC} range of 2.7 V and 3.3±0.3 V.

4. ΔI_{CC} Characteristics

The ΔI_{CC} specification denotes the increase in normal I_{CC}. For each input at applied V_{CC}–0.6 V, the ΔI_{CC} value should be added to the quiescent current to get the circuit's worst-case static I_{CC} value. In fact, low voltage CMOS logic outputs can drive HD74LV-A/LVC/LVC-A series inputs down to nearly equal to 0 V and up to nearly equal to V_{CC}. Consequently, voltage can be applied to input pins under relaxed conditions than the DI_{CC} test conditions. Moreover, typical values of ΔI_{CC} on each input pin will be much less than the specification. Figure 6 to 7 shows the change of ΔI_{CC} for input voltages. On designing with HD74LV-A/LVC/LVC-A series, understand the meaning of ΔI_{CC} spec. and consider that the actual values will be fairly small compared with the specs. in the datasheet.

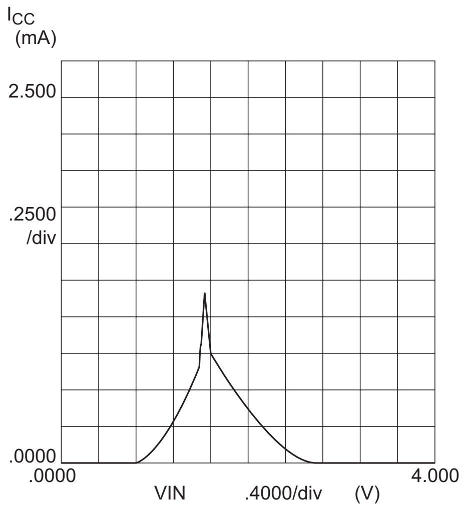

Figure 6 Input Voltage vs. I_{CC} Characteristics in HD74LV-A Series

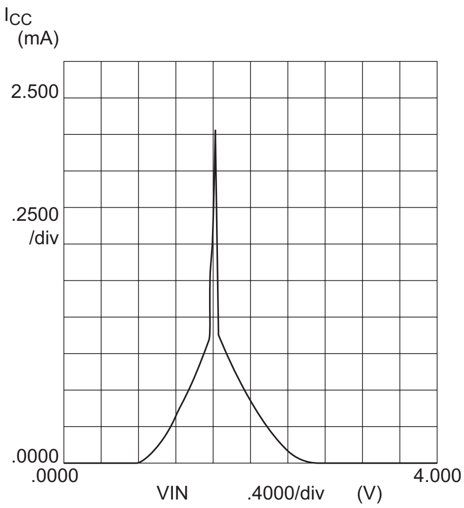

Figure 7 Input Voltage vs. I_{CC} Characteristics in HD74LVC/LVC-A Series

5. Calculating the Power Dissipation

The power dissipation PT of low-voltage CMOS logic can be calculated by (1). From this equation, the power dissipation depends on the load capacitance, frequency and supply voltage.

$$P_T = (C_{pd} + C_L) \times f \times V_{CC}^2 \qquad (1)$$

then,

C_L: Load capacitance, Cpd: Power dissipation capacitance,
f: Operating frequency, V_{CC}: Supply voltage

6. Power Dissipation Capacitance

Power dissipation capacitance (Cpd) can be calculated by the following equations,

$$P_T = (C_{pd} + C_L) \times f \times V_{CC}^2 = I_{CC} \times V_{CC} \qquad (2)$$

therefore,

$$C_{PD} = \frac{I_{CC}}{f \times V_{CC}} - C_L \qquad (3)$$

then,

I_{CC}: Supply current
(Test conditions)
Ta = 25°C, V_{CC}= 3.3 V, f = 10 MHz
duty = 50%, $t_r = t_f$ = 2.5 ns, C_L = 50 pF

(1) HD74LVC/LVC-A Series power dissipation capacitance (Cpd)
V_{CC} = 3.3 V, Ta = 25°C, C_L = 50 pF, Other Input = V_{CC} or GND
P1: f = 10 MHz, duty = 50%, P2: f = 5 MHz, duty = 50%

Product part No.	Test Condition		enable	disable	Unit
	INPUT	OUTPUT	Typ	Typ	
HD74LVC00	1A:P1	1Y	17.0	—	pF
HD74LVC02	1A:P1	1Y	17.0	—	
HD74LVC04	1A:P1	1Y	13.0	—	
HD74LVC08	1A:P1	1Y	16.0	—	
HD74LVC14	1A:P1	1Y	14.0	—	
HD74LVC32	1A:P1	1Y	17.0	—	
HD74LVC74	1CK:P1, 1D:P2	1Q	16.0	—	
HD74LVC125A	1A:P1	1Y	16.0	2.0	
HD74LVC138	A:P1	Y0	38.0	—	
HD74LVC139	1A:P1	1Y0	32.0	—	
HD74LVC240A	1A1:P1	1Y1	15.0	1.0	
HD74LVC244A	1A1:P1	1Y1	14.0	2.0	
HD74LVC245A	A0:P1	B0	17.0	2.0	
HD74LVC373A	1D:P1	1Q	18.0	3.0	
HD74LVC374A	1CK:P1, 1D:P2	1Q	17.0	9.5	
HD74LVC533	1D:P1	1Q	16.0	3.0	
HD74LVC534	1CK:P1, 1D:P2	1Q	16.0	9.5	
HD74LVC540A	A1:P1	Y1	14.0	1.0	
HD74LVC541A	A1:P1	Y1	15.0	2.0	
HD74LVC573A	1D:P1	1Q	17.0	3.0	
HD74LVC574A	1CK:P1, 1D:P2	1Q	17.0	10.0	
HD74LVC16240A	1A1:P1	1Y1	15.0	1.0	
HD74LVC16244A	1A1:P1	1Y1	16.0	2.0	
HD74LVC16245A	1A1:P1	1B1	18.0	2.0	
HD74LVC16373A	1D1:P1	1Q1	16.0	3.0	
HD74LVC16374A	1CK:P1	1Q1	17.0	10.0	

(2) HD74LVCZ Series power dissipation capacitance (Cpd)
V_{CC} = 3.3 V, Ta = 25°C, C_L = 50 pF, Other Input = V_{CC} or GND
P1: f = 10 MHz, duty = 50%, P2: f = 5 MHz, duty = 50%

Product part No.	Test Condition		enable	disable	Unit
	INPUT	OUTPUT	Typ	Typ	
HD74LVCZ240A	1A1:P1	1Y1	27.0	5.5	pF
HD74LVCZ244A	1A1:P1	1Y1	26.0	5.0	
HD74LVCZ245A	A0:P1	B0	31.0	5.0	
HD74LVCZ16240A	1A1:P1	1Y1	30.0	7.0	
HD74LVCZ16244A	1A1:P1	1Y1	30.0	5.0	
HD74LVCZ16245A	1A1:P1	1B1	34.0	5.5	
HD74LVC2244A	1A1:P1	1Y1	26.0	3.5	
HD74LVCR2245A	A0:P1	B0	31.0	3.5	

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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