To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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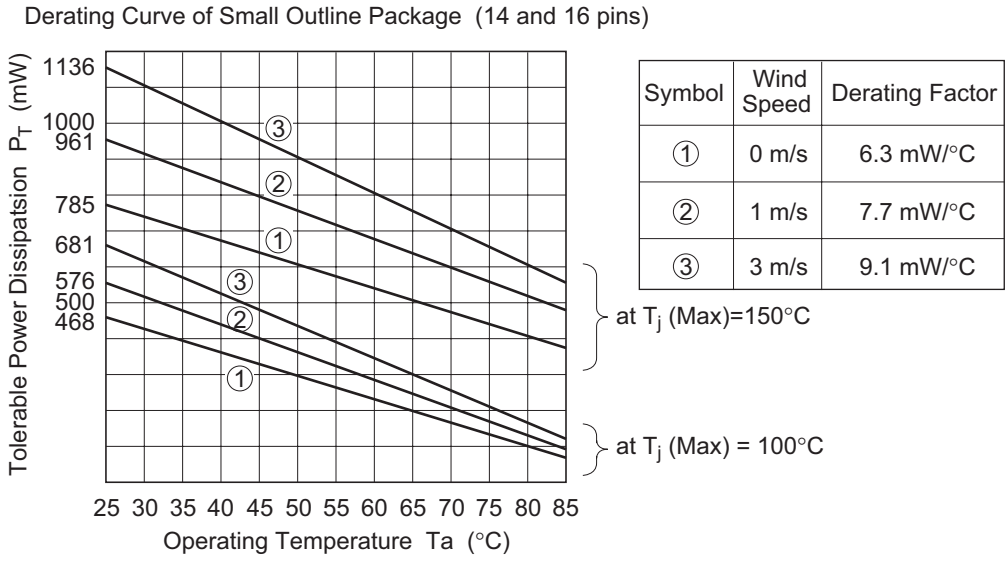
Low-Voltage CMOS Logic HD74LV_A/LVC Series

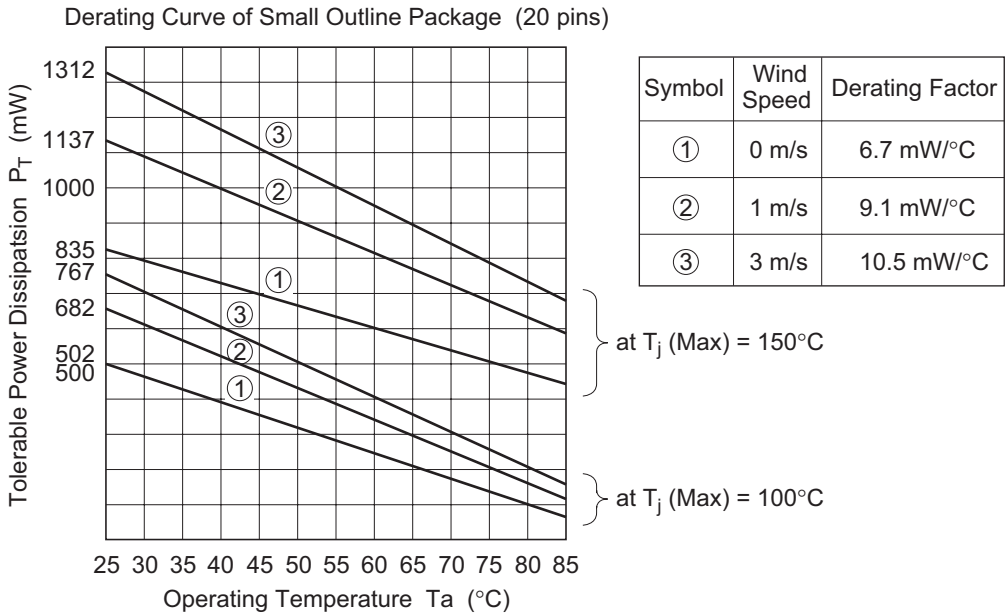
Package Thermal Resistance

1. Thermal Resistance of SOP

Figure 1 shows the derating curve of SOP with HD74LV-A/LVC/LVC-A devices and table 1 shows the thermal resistance (θj-a).



Symbol	Wind Speed	Derating Factor
①	0 m/s	6.3 mW/°C
②	1 m/s	7.7 mW/°C
③	3 m/s	9.1 mW/°C



Symbol	Wind Speed	Derating Factor
①	0 m/s	6.7 mW/°C
②	1 m/s	9.1 mW/°C
③	3 m/s	10.5 mW/°C

Note: For the ambient temperature less than 25°C, the power dissipation at 25°C is applied. The data above are measured by ΔV_{BE} method mounting on glass epoxy board (40 × 40 × 1.6 mm) with 10% of wiring density. In the actual application, using conditions, ambient temperature and forced air-cooling conditions should be sufficiently examined.

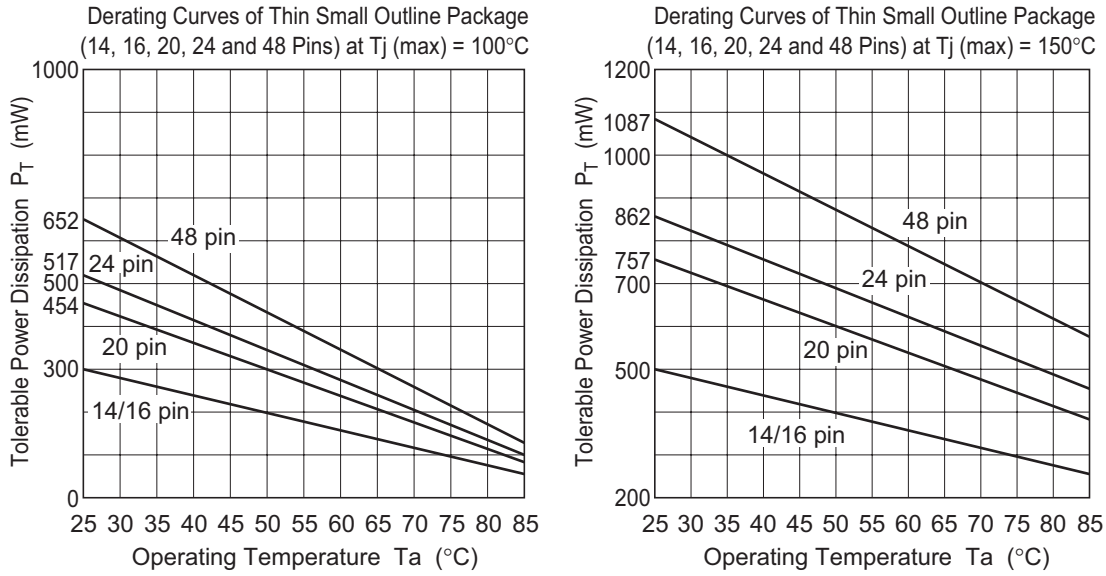
Figure 1 Dreating Curve of SOP

Table 1 Thermal Resistance of SOP Package

Pin Count	Wind Speed	Derating Factor	Thermal Resistance	Tolerable Power Dissipation	
				at Tj (max) = 150°C	at Tj (max) = 100°C
14, 16	0 m/s	6.3 mW/°C	160°C/W	785 mW	468 mW
	1 m/s	7.7 mW/°C	130°C/W	961 mW	576 mW
	3 m/s	9.1 mW/°C	110°C/W	1136 mW	681 mW
20	0 m/s	6.7 mW/°C	150°C/W	835 mW	502 mW
	1 m/s	9.1 mW/°C	110°C/W	1137 mW	682 mW
	3 m/s	10.5 mW/°C	95°C/W	1312 mW	787 mW

2. Thermal Resistance of TSSOP

Figure 2 shows the derating curve of TSSOP with HD74LV-A/LVC/LVC-A devices, table 2 shows the thermal resistance (θj-a) and figure 3 shows the mounting method.

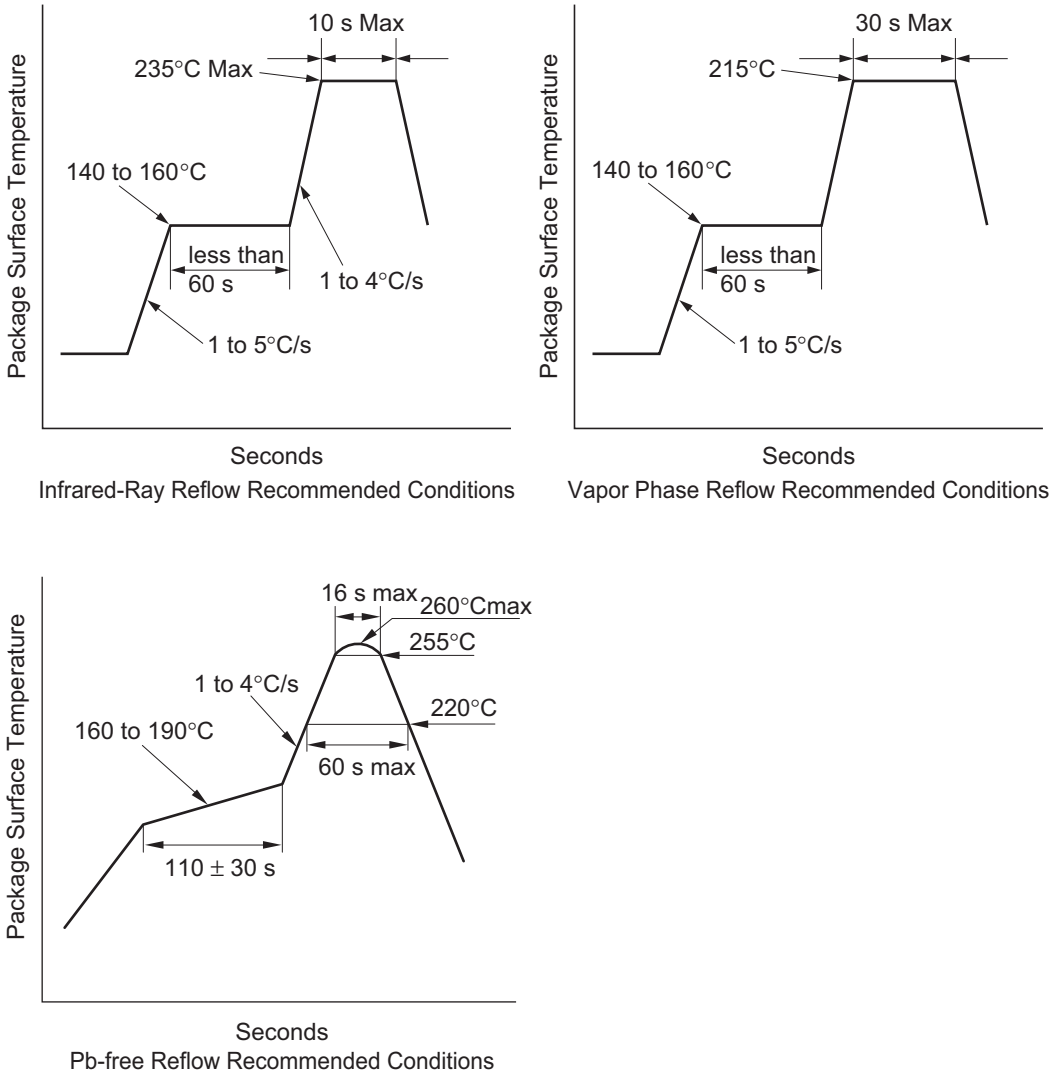


Note: For the ambient temperature less than 25°C, the power dissipation at 25°C is applied. The data above are measured by ΔV_{BE} method mounting on glass epoxy board (40 × 40 × 1.6 mm) with 10% of wiring density. In the actual application, using conditions, ambient temperature and forced air-cooling conditions should be sufficiently examined.

Figure 2 Derating Curve of TSSOP

Table 2 Thermal Resistance of TSSOP Package

Pin Count	Wind Speed	Derating Factor	Thermal Resistance	Tolerable Power Dissipation	
				at Tj (max) = 150°C	at Tj (max) = 100°C
14, 16	0 m/s	4.0 mW/°C	250°C/W	500 mW	300 mW
20	0 m/s	6.1 mW/°C	165°C/W	757 mW	454 mW
24	0 m/s	6.9 mW/°C	145°C/W	862 mW	517 mW
48	0 m/s	8.7 mW/°C	115°C/W	1087 mW	652 mW

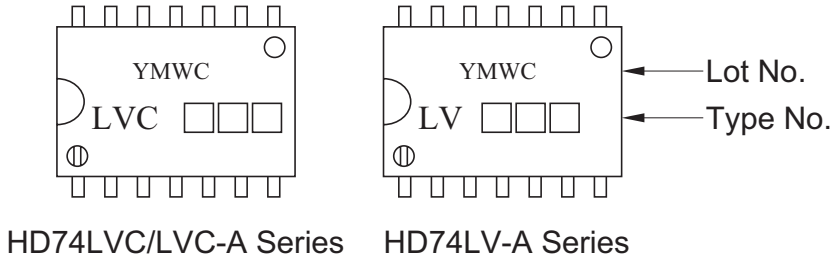


Note: As mounting methods for TSSOP (14, 16, 20, 24 and 48 pins), Renesas recommends the infrared-ray reflow and vapor phase reflow. (Solder-dip is not recommended.)

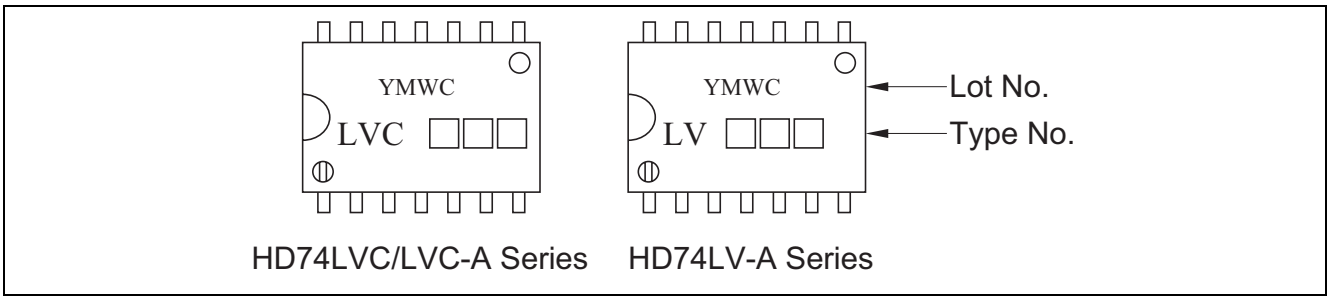
Figure 3 Mounting Method of TSSOP

3. Marking on Package

(1) Small outline Package (JEITA) 14, 16, 20 pins

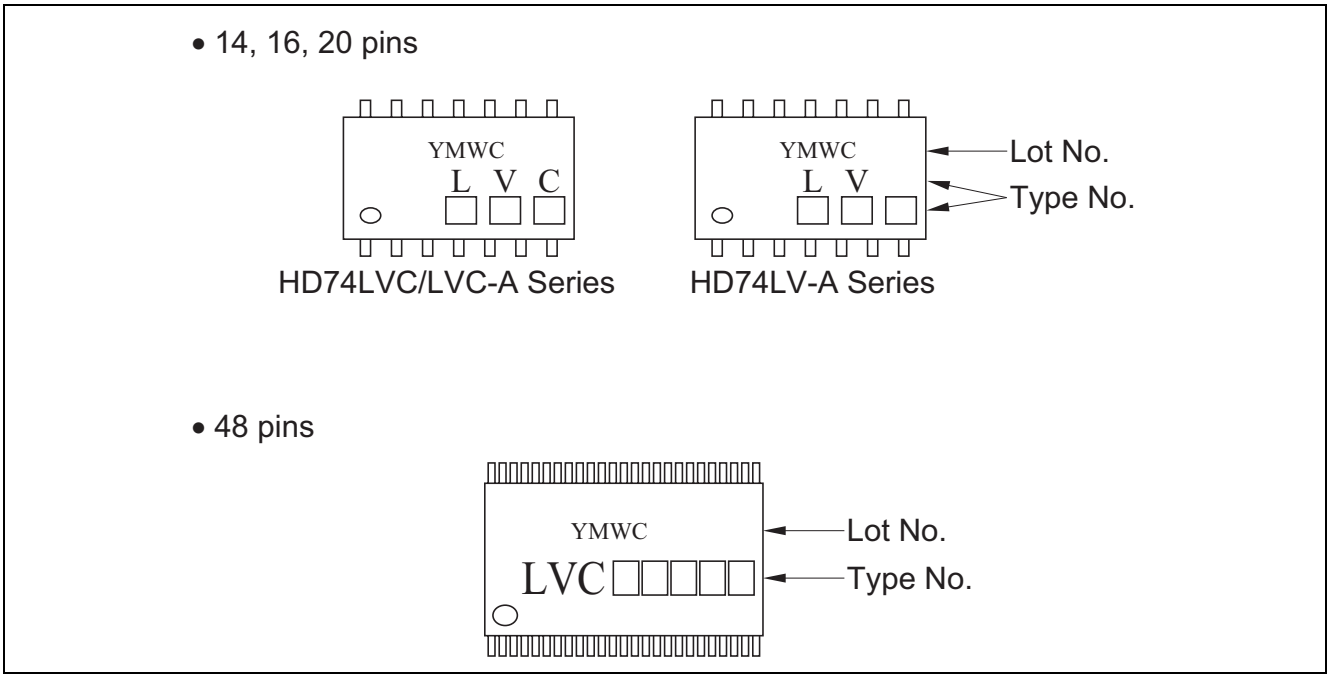


(2) Small outline Package (JEDEC) 14, 16, 20 pins



Note: Meaning of marking on package example device name: HD74LVC245AT
Y: Year code (the last digit of year)
M: Month code
W: Week code
C: Control code
Type No.: delete HD74 and package code (T) from device name

(3) Thin Shrink Small outline Package 14, 16, 20, 48 pins



Note: Meaning of marking on package example device name: HD74LVC245AT
Y: Year code (the last digit of year)
M: Month code
W: Week code
C: Control code
Type No.: delete HD74 and package code (T) from device name

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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