

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Development Tools (1/5)

Remark For details about development tools, see the site for development tools at NEC Electronics Website. NEC Electronics Website: http://www.nec.com

Table with 2 columns: Host Machine, Software Tools. Lists software packages like SP78K0, SP78K0, SP78K0, etc.

(2) Hardware Tools (1/3)
<1> On-chip debug emulator OB-78K0MINI (MINICUBE®)

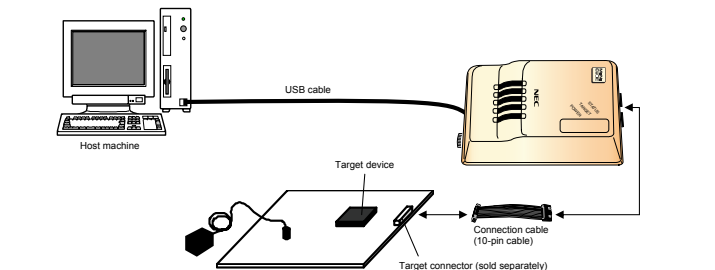


Table with 2 columns: Connector pin layout (10-pin), Description. Lists pins like RESET, RELOAD, VDD, etc.

Notes 1. Signal names in MINICUBE. 2. As seen from MINICUBE.

Development Tools (5/5)

(3) Flash Memory Write Tools (3/3)
<2> Flash memory programmer PG-FP5, FL-PRS, PG-FPA, FL-PR4, PG-FPL3, FL-PLT3 (1/2)

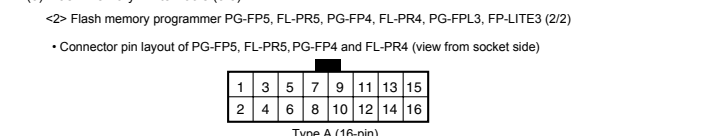


Table with 2 columns: Connector pin layout of PG-FP5, FL-PRS, PG-FPA and FL-PR4 (view from socket side).

Table with 2 columns: Connector pin configuration of PG-FP5, FL-PRS, PG-FPA and FL-PR4.

Table with 2 columns: Signal name of PG-FP4, Target Connector Type A (Signal 16-Pin).

Note Signals in parentheses and the corresponding pins are not used with 78K0KD2.

Operation List (1/6)

Operand identifiers and specification methods

Table with 3 columns: Identifier, Specification Method, Operands. Lists identifiers like R, W, SP, etc.

Note Addresses from FFD0H to FFD5H cannot be accessed with these operations.

Operation List (5/6)

Table with 3 columns: Instruction Group, Mnemonic, Operands, Bytes, Cycles, Operation, Flag. Lists instructions like BCD adjustment, bit manipulate, etc.

Notes 1. When the internal high-speed RAM area is accessed... 2. When an area except the internal high-speed RAM area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

Special Function Register (SFR) List (3/4)

Table with 3 columns: Address, Special Function Register (SFR) Name, Symbol, RW, Manipulatable Bit Unit, After Reset. Lists registers like FFF3H, FFF4H, etc.

Notes 1. The reset value of WDETE is determined by setting of option byte. 2. The value of this register is set immediately after a reset release...

Development Tools (2/5)

(2) Hardware Tools (2/3)
<2> In-Circuit Emulator OB-78K0K2 (ICEUBE®)

Table with 2 columns: In-Circuit Emulator, Package, Check Point, Emulation, Exchange Adapter, Space Adapter, VQ Connector, Mount Adapter, Target Connector.

Remark The OB-78K0K2 is supplied with ID78K0-OB, a USB cable, a power supply unit, OB-MINICE, connection cables (10-pin cable and 16-pin cable) and the 78K0-OCDD board.

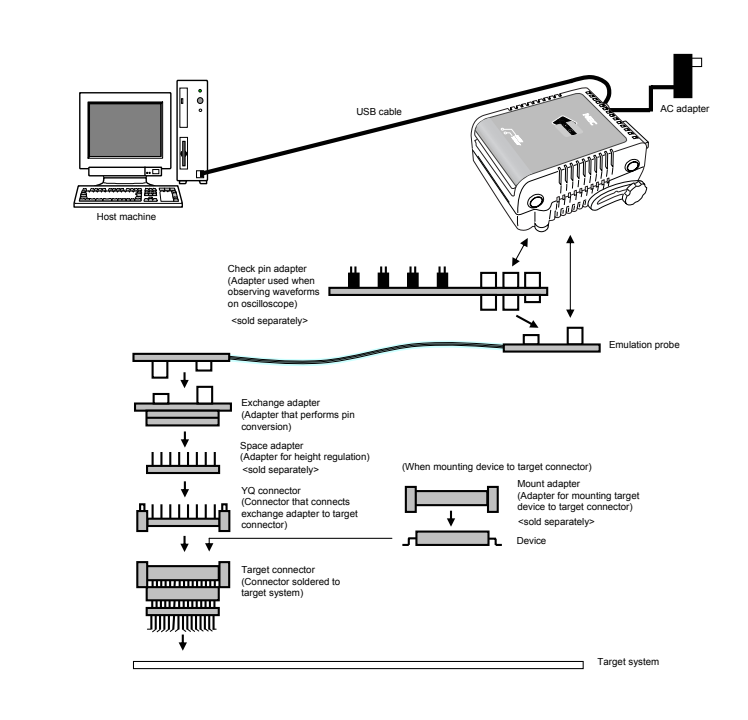


Table with 2 columns: Connector pin configuration (10-pin), Description. Lists pins like RESET, RELOAD, VDD, etc.

Notes 1. Signal names in MINICUBE. 2. As seen from MINICUBE.

Operation List (2/6)

Description of operation column. A: Register, X: Register, B: Register, C: Register, D: Register, E: Register, H: Register, L: Register, AX: Register, etc.

Table with 3 columns: Instruction Group, Mnemonic, Operands, Bytes, Cycles, Operation, Flag. Lists instructions like MOV, ADDC, SUB, etc.

Notes 1. When the internal high-speed RAM area is accessed... 2. When an area except the internal high-speed RAM area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

Operation List (6/6)

Table with 3 columns: Instruction Group, Mnemonic, Operands, Bytes, Cycles, Operation, Flag. Lists instructions like RET, PUSH, POP, etc.

Notes 1. When the internal high-speed RAM area is accessed... 2. When an area except the internal high-speed RAM area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

Special Function Register (SFR) List (4/4)

Table with 3 columns: Address, Special Function Register (SFR) Name, Symbol, RW, Manipulatable Bit Unit, After Reset. Lists registers like FFE0H, FFE1H, etc.

Notes 1. Regardless of the internal memory capacity, the initial values of the internal memory size switching register (MCS) and internal expansion RAM size switching register (IXS) of all products in the 78K0KD2 are fixed (MCS = CH1, IXS = OCH1).

Development Tools (3/5)

(2) Hardware Tools (3/3)
<2> On-chip debug emulator with programming function OB-MIN2 (MINICUBE®) for on-chip debugging

Table with 2 columns: OB-MIN2, Target Connector Specifications. Lists connector types and pin counts.

(3) Flash Memory Write Tools (1/3)
<1> On-chip debug emulator with programming function OB-MIN2 (MINICUBE®) for flash programming

Table with 2 columns: OB-MIN2, Target Connector Specifications. Lists connector types and pin counts.

Remarks 1. The OB-MIN2 is supplied with a USB cable, connection cables (10-pin cable and 16-pin cable) and the 78K0-OCDD board.

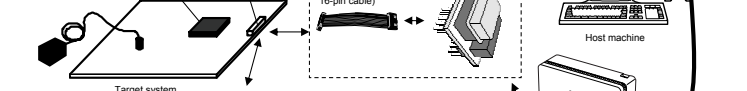


Table with 2 columns: Connector pin layout (16-pin), Description. Lists pins like GND, RESET, etc.

Table with 2 columns: Connector pin configuration (16-pin), Description. Lists pins like GND, RESET, etc.

Notes 1. Signal names in MINICUBE. 2. As seen from MINICUBE.

Remark The 10-pin target connector is the same as that of MINICUBE.

Operation List (3/6)

Table with 3 columns: Instruction Group, Mnemonic, Operands, Bytes, Cycles, Operation, Flag. Lists instructions like MOV, ADDC, SUB, etc.

Notes 1. When the internal high-speed RAM area is accessed... 2. When an area except the internal high-speed RAM area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

Special Function Register (SFR) List (1/4)

Table with 3 columns: Address, Special Function Register (SFR) Name, Symbol, RW, Manipulatable Bit Unit, After Reset. Lists registers like FFD0H, FFD1H, etc.

Note Available only in the PD78F0524A, 78F0525A, 78F0526A, 78F0527A, and 78F0527DA.

Development Tools (4/5)

(3) Flash Memory Write Tools (2/3)
<2> Flash memory programmer PG-FP5, FL-PRS, PG-FPA, FL-PR4, PG-FPL3, FL-PLT3 (1/2)

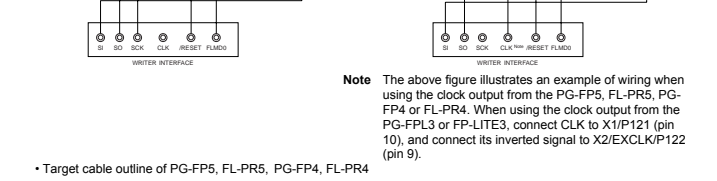
Table with 2 columns: Flash Memory Programmer, Flash Memory Write Adapter. Lists models like PG-FP5, FL-PRS, etc.

Remark 1. FL-PRS, FL-PR4, FL-PLT3, FA-52GB-BET-A, FA-78F0527GB-UET-MK are products of Naito Densei Mochida Mfg. Co., Ltd.



Table with 2 columns: Connector pin layout of PG-FP5, FL-PRS, PG-FPA and FL-PR4 (view from socket side).

Table with 2 columns: Connector pin configuration of PG-FP5, FL-PRS, PG-FPA and FL-PR4.



Note The above figure illustrates an example of wiring when using the clock output from the PG-FP5, FL-PRS, PG-FPA or FL-PR4.

Table with 2 columns: Target cable outline of PG-FP5, FL-PRS, PG-FPA, FL-PR4.

Notes 1. The target cable of PG-FP5 and FL-PRS is not equipped with Type B. 2. Type B is not used to connect with 78K0KD2 because 78K0KD2 incorporates the single-power-supply flash memory.

Operation List (4/6)

Table with 3 columns: Instruction Group, Mnemonic, Operands, Bytes, Cycles, Operation, Flag. Lists instructions like OR, XOR, AND, etc.

Notes 1. When the internal high-speed RAM area is accessed... 2. When an area except the internal high-speed RAM area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

Special Function Register (SFR) List (2/4)

Table with 3 columns: Address, Special Function Register (SFR) Name, Symbol, RW, Manipulatable Bit Unit, After Reset. Lists registers like FFF3H, FFF4H, etc.

Note Available only in the PD78F0524A, 78F0525A, 78F0526A, 78F0527A, and 78F0527DA.

This document is a reference.

The information in this document is current as of July, 2007. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc.

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