Tsi106/Tsi107 Device Differences

80C2000_AN007_02

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Tsi106/Tsi107 Device Differences

This document primarily summarizes the register differences between the Tsi106 and Tsi107. For more information on the feature differences between these devices, see the *Tsi106 User Manual* and the *Tsi107 User Manual*.

The following topics are discussed:

- "Functional Differences" on page 4
- "Register Differences" on page 6
- "Graphic Register Changes" on page 10
- "Signal/Pinout Differences" on page 31
- "Physical Differences" on page 31

Revision History

80C2000_AN007_01, Formal, November 2009

This version of the document was rebranded as IDT.

80C2000_AN007_01, Formal, March 2006

This is the first release of the *Tsi106 and Tsi107 Device Differences*.

1. Functional Differences

The functional differences between the Tsi106 and Tsi107 are summarized in the following table.

Table 1: Functional Differences

Function/Feature	Tsi106	Tsi107
Processor Interface		
Dual processor support	✓	✓
Quad processor support	✓	
Various operating frequencies and divider ratios	✓	✓
Processor power management		✓
32-bit address bus / 64-bit data bus	✓	✓
32-bit data bus		✓
Full memory coherency	✓	✓
Optional 60x local bus slave	✓	✓
L2 cache Support	✓	
Memory Controller		
FPM DRAM, EDO, SDRAM support	✓	✓
ECC support for SDRAM	External	✓
ECC support for EDO, FPM		✓
1-8 banks of 4,16,64,128M	✓	✓
256 MB Support		✓
1 GB RAM Space	✓	✓
ROM	16 MB	144 MB
Port X (up to 64 GPIOs)		✓
SDRAM frequencies	66 MHz/ 83 MHz	100 MHz

Table 1: Functional Differences *(Continued)*

Function/Feature	Tsi106	Tsi107
PCI Interface		
PCI revision	2.1	2.2
32-bit address	✓	✓
Frequency	33 Mhz	33 Mhz
5 V tolerant	✓	✓
Both big endian and little endian support	✓	✓
PCI arbiter with 5 request and grant pairs		✓
PCI agent mode		✓
Support for PCI locked accesses to memory	✓	✓
Store gathering for PCI writes to memory	✓	✓
Selectable memory pre-fetching for reads	✓	✓
Address translation unit		✓
Internal Configuration registers accessible from PCI		✓
Embedded and other features		
Two channel DMA		✓
I^2C		✓
I_2O		✓
EPIC		✓
Programmable Watch point trigger		✓
Error Injection/Capture on Data Path		✓
IEEE 1149.1 JTAG/Test Interface	✓	✓

2. Register Differences

This section discusses the register differences between the Tsi106 and Tsi107 devices.

2.1 Register Changes

In the migration from the Tsi106 to the Tsi107, registers have been added, modified, and removed. The following sections detail the register changes.

2.1.1 Added Registers

The following registers have been added to the Tsi107 programming model, but do not exist in the Tsi106. The code type column in the table indicates the typical sections of code that access the register.

Table 2: Added Tsi107 Registers

Register	Description	Code Type	
PCI Interface		**Initialization**	**Application**
Local Memory Base Address Register Bit Definitions (Offset 0x10)	Local memory base address register (LMBAR)	✓	
PCSR Base Address Register Bit Definitions (Offset 0x14)	Peripheral control and status registers base address register (PCSRBAR)	✓	
Expansion ROM base address (Offset 0x30)	This register is read-only. The default value has 0b0 in bit 0, defining the expansion ROM base address register as disabled in the Tsi107.	✓	
PCI Arbiter Control Register Bit Definitions (Offset 0x46)	This register controls the on-chip arbitration for external PCI masters. As many as five external devices are supported.	✓	
Output/Clock Driver and Miscellaneous I/O Control Registers		**Initialization**	**Application**
Clock Driver Control Register (ODCR) (Offset 0x74)	The clock driver control register (CDCR) controls the output enable/disable capability available for the clock signals.	✓	
Miscellaneous I/O Control Register (Offset 0x76)	The Miscellaneous I/O Control Register (MIOCR) that controls the type of output for the MCP_, SRESET_ and QACK_ signals.	✓	

Table 2: Added Tsi107 *(Continued)* Registers

Register	Description	Code Type	
Embedded Utilities Memory Block		**Initialization**	**Application**
Embedded Utilities Memory Block Base Address Register (Offset 0x78)	The embedded utilities memory block base address register (EUMBBAR) controls the placement of the embedded utilities memory block (EUMB).	✓	
Address Map B Options Register (AMBOR) (Offset 0xE0)	The address map B options register (AMBOR) controls various configuration settings that can be used to alias some addresses and to control accesses to holes in the address map.		

2.1.2 Modified Registers

The following registers exist in both devices but have modified fields or bits between the Tsi106 and Tsi107. The code type column in the table indicates the typical sections of code that access the register.

Table 3: Modified Registers

Register	Description	Code Type	
PCI Interface		**initialization**	**Application**
Device ID (Offset 0x02)	Identifies the particular device.	✓	
PCI Command register (Offset 0x04)	Provides coarse control over a device's ability to generate and respond to PCI bus cycles.	✓	
PCI Status Register (Offset 0x06)	Records status information for PCI bus-related events.	✓	
PCI Configuration Register - Bus Number (Offset 0x40)	Identifies the assigned bus number.	✓	
Power Management		**Initialization**	**Application**
Power Management Configuration Register 1 and 2 (Offset 0x70, 0x72)	The power management configuration registers (PMCRs) control the power management functions.		✓
Output Driver Control Register (ODCR) (Offset 0x73)	Controls driver strength for various interfaces.	✓	

Table 3: Modified Registers

Register	Description	Code Type	
Processor Interface		**Initialization**	**Application**
Processor Interface Configuration Register 1 (PICR1) and 2 (PICR2) (Offset 0xA8, 0xAC)	The processor interface configuration registers (PICRs) control the programmable parameters of the 60x bus interface and the L2 cache interface.	✓	
Error Handling		**Initialization**	**Application**
Error Enabling Register 1 (ErrEnR1) and 2 (ErrEnR2) (Offset 0xC0, 0xC4)	Error enabling registers control whether the device recognizes and reports specific error conditions.		✓
Error Detection Register 2 (ErrDR2) (Offset 0xC5)	Error Detection Register 2 (ErrDR2) contains error flags that report when the device detects a specific error condition.		✓
Memory		**Initialization**	**Application**
Memory Control Configuration Register 1 (MCCR1) (Offset 0xF0)	The 32-bit memory control configuration registers (MCCRs) set all RAM and ROM parameters.	✓	
Memory Control Configuration Register 2 (MCCR2) (Offset 0xF4)	The 32-bit memory control configuration registers (MCCRs) set all RAM and ROM parameters.	✓	
Memory Control Configuration Register 3 (MCCR3) (Offset 0xFC)	The 32-bit memory control configuration registers (MCCRs) set all RAM and ROM parameters.	✓	

2.1.3 Removed Registers

The following registers were part of the Tsi106 programming model, but are not supported in the Tsi107. The code type column in the table indicates the typical sections of code that access the register.

Table 4: Removed Tsi106 Registers

Register	Description	Code Type	
PCI Interface		**initialization**	**Application**
Disconnect counter (Offset 0x42)	Specifies the timer for target-disconnect timeout (0x00 = the timer is disabled)		✓

Table 4: Removed Tsi106 Registers

Register	Description	Code Type	
Performance Monitoring		**Initialization**	**Application**
Performance Monitor Command Register (CMDR) (Offset 0x48)	The performance monitor command register (CMDR) is used to select the counter and the events to be counted.		✓
Performance Monitor Mode Control Register (MMCR) (Offset 0x4C)	The performance monitor mode control register (MMCR) is used to control performance monitor operation.		✓
Performance Monitor Counters (PMC0, PMC1, PMC2, PMC3) (Offset 0x50, 0x54, 0x58, 0x5C)	There are four performance monitor counter registers (PMC0, PMC1, PMC2, and PMC3) that can be used to count events selected by the CMDR.		✓
Operating System		**Initialization**	**Application**
Alternate OS-Visible Parameters Register 1 and 2 (Offset 0xBA, 0xBB)	The alternate OS-visible parameters registers 1 and 2 provide operating systems an alternate means to access some of the bits in the Processor Interface Configuration Register 1 (PICR1).	✓	
Emulation Support		**Initialization**	**Application**
Emulation Support Configuration Register 1 and 2 (Offset 0xE0, 0xE8)	The 32-bit Emulation support Configuration Registers (ESCRs) control the behavior of the device when operating in emulation mode.	✓	
Modified Memory Status Register (Offset 0xE4, 0xEC)	When the device is operating in emulation mode, the modified memory status register tracks the state of system memory that has been modified by PCI masters.		✓
External Configuration		**initialization**	**Application**
External Configuration Register 1, 2, and 3 (Offset 0x092, 0x81C, 0x850)	When using address map A, certain configuration bits can be accessed by reading or writing to the ports at addresses 0x8000_0092 (referred to as port 0x092), 0x8000_081C (referred to as port 0x81C), or 0x8000_0850 (referred to as port 0x850). These external configuration registers should only be accessed as a 1-byte quantity, even though the other bytes in the double word are reserved.		✓

2.2 Graphic Register Changes

The following sections graphically display the registers that have been added, modified, or removed between the Tsi106 design and the Tsi107.

Not all registers contained in the devices are shown.

2.2.1 Added Registers

Local Memory Base Address Register Bit Definitions (Offset 0x10)

Table 5: Local Memory Base Address Register Bit Definitions (Offset 0x10)

Bits	Name	Reset Value	R/W	Description
31:12	Inbound memory base address	0x0000_0	R/W	Indicates the base address where the inbound memory window resides. The inbound memory window should be aligned based on the granularity specified by the inbound window size specified in the ITWR. Note that the EUMB area must be selected first, then the ITWR programmed, and then the bits set. Refer to Chapter 3, “Address Maps,” for more information on the EUMB and the ATU.
11:4	Reserved	All 0s	R	Reserved; the Tsi107 only allows a minimum of a 4-Kbyte window.
3	Prefetchable	1	R	Indicates that the space is prefetchable.
2:1	Type	00	R	The inbound memory window may be located anywhere within the 32-bit PCI address space.
0	Memory space indicator	0	R	Indicates PCI memory space

PCSR Base Address Register Bit Definitions (Offset 0x14)

Table 6: PCSR Base Address Register Bit Definitions (0x14)

Bits	Reset Value	R/W	Description
31:12	0x0000_0	R/W	Indicates the PCI base address that is mapped to the runtime registers (for example, DMA, I_2O).
11:0	0x000	R	Reserved

Expansion ROM base address (Offset 0x30)

Graphic not shown.

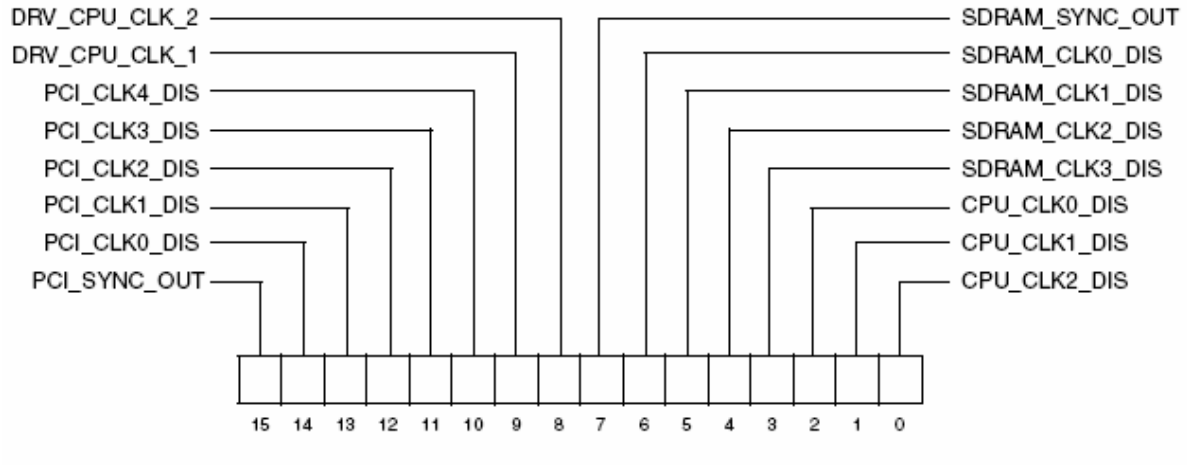
PCI Arbiter Control Register Bit Definitions (Offset 0x46)

Table 7: PCI Arbiter Control Register Bit Definitions (0x46)

Bits	Reset Value	R/W	Description
msb 15	x	R/W	Enable on-chip PCI arbitration 0 If cleared, the on-chip arbiter for external PCI masters is disabled, and the Tsi107 presents its request on GNT0 to the external arbiter and receives its grant on REQ0. 1If set, indicates the on-chip arbiter is enabled.
14:13	00	R/W	Parking mode controls which device receives the bus grant when there are no outstanding bus requests and the bus is idle. 00The bus is parked with the last device to use the bus. 01The bus is parked with the device using REQ0 and GNT0. 10The bus is parked with Tsi107. 11Reserved; do not use.
12	0	R/W	PCI broken master disable. This bit controls whether the PCI arbiter negates the bus grant to a requesting master that does not assert FRAME within 16 PCI clock cycles from the time the bus is idle. 0 PCI arbiter negates the PCI GNT*x* signal to a requesting master that does not begin using the bus (by asserting FRAME) within 16 PCI clock cycles from the time the PCI clock is idle. 1 A PCI master that has been granted the bus never loses its grant until (and unless) it begins a transaction or negates the REQ*x* signal. It is recommended that this bit stay cleared.
11	0	R	Reserved
10	0	R/W	Retry PCI Configuration Cycle 1PCI target logic retries all external PCI configuration transactions. 0PCI target logic responds to external PCI configuration transactions.
9:8	00	R	Reserved
7	0	R/W	Tsi107 priority level, 1 = high, 0 = low
6:5	00	R	Reserved
4:0	0_0000	R/W	External device priority levels, 1 = high, 0 = low. Bit 0 corresponds to the device using REQ0 and GNT0, bit 1 to REQ1 and GNT1, etc.

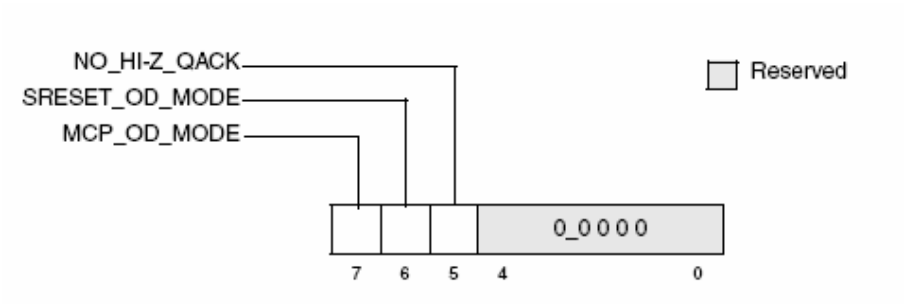
Clock Driver Control Register (ODCR) (Offset 0x74)

Figure 1: Tsi107



Miscellaneous I/O Control Register (Offset 0x76)

Figure 2: Tsi107



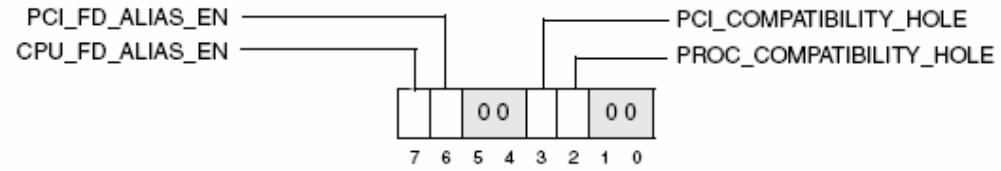
Embedded Utilities Memory Block Base Address Register (Offset 0x78)

Table 8: Tsi107

Bits	Name	Reset Value	Description
msb 31–20	Base Address	0x000	Base address of the embedded memory utilities block. The block size is 1 Mbyte, and its base address is aligned naturally to a 1 Mbyte address boundary (so the base address is 0xXXX0_0000). This block is used by processor-initiated transactions and should be located within PCI memory space. Registers within the EUMB are located from 0x8000_0000 to 0xFDFF_FFFF. Thus, valid values are 0x800–0xFDF. Otherwise, the EUMB is effectively disabled.
19–0	—	0x0_0000	Reserved

Address Map B Options Register (AMBOR) (Offset 0xE0)

Figure 3: Tsi107



2.2.2 Modified Registers

Device ID (0x02)

Graphic not shown.

PCI Command Register (0x04)

Figure 4: Tsi106

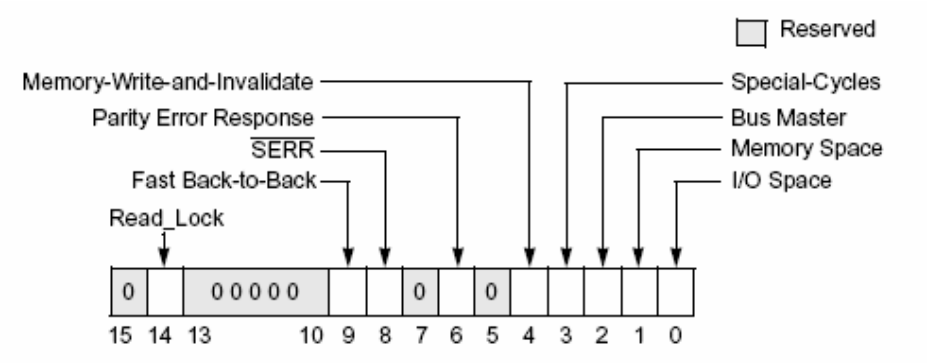
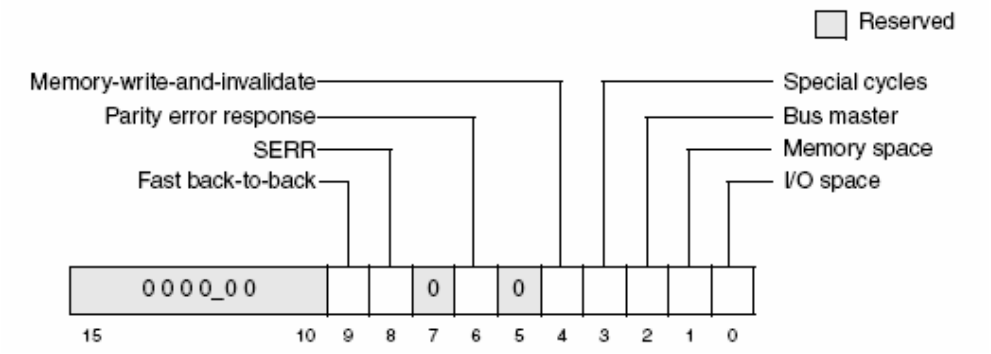


Figure 5: Tsi107



PCI Status Register (0x06)

Figure 6: Tsi106

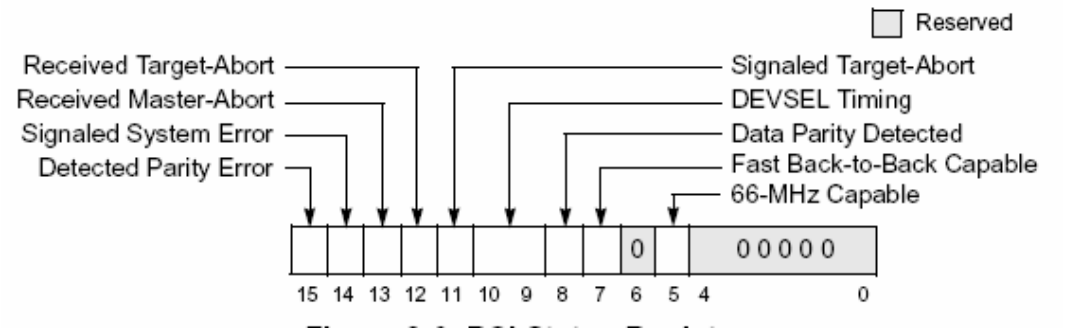
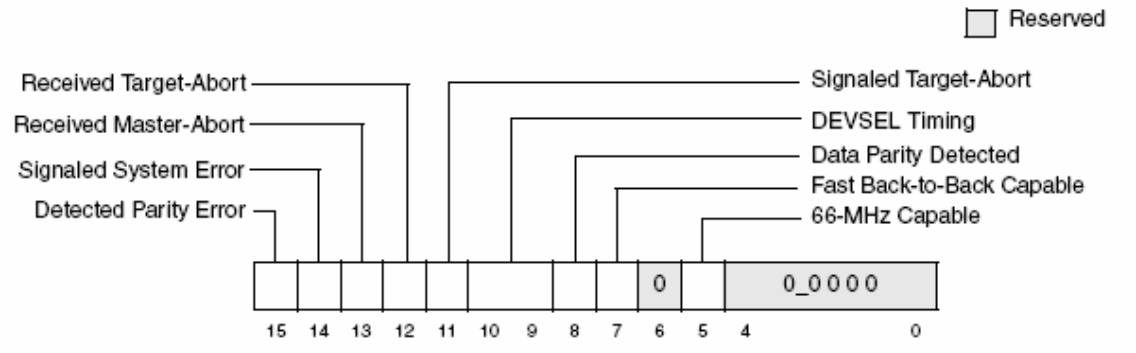


Figure 7: Tsi107



PCI Configuration Register - Bus Number (Offset 0x40)

Graphic not shown.

Power Management Configuration Register 1 (Offset 0x70)

Figure 8: Tsi106

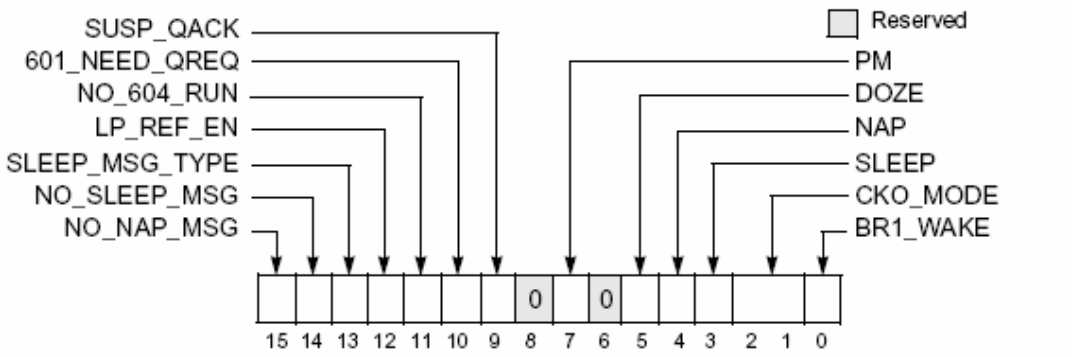
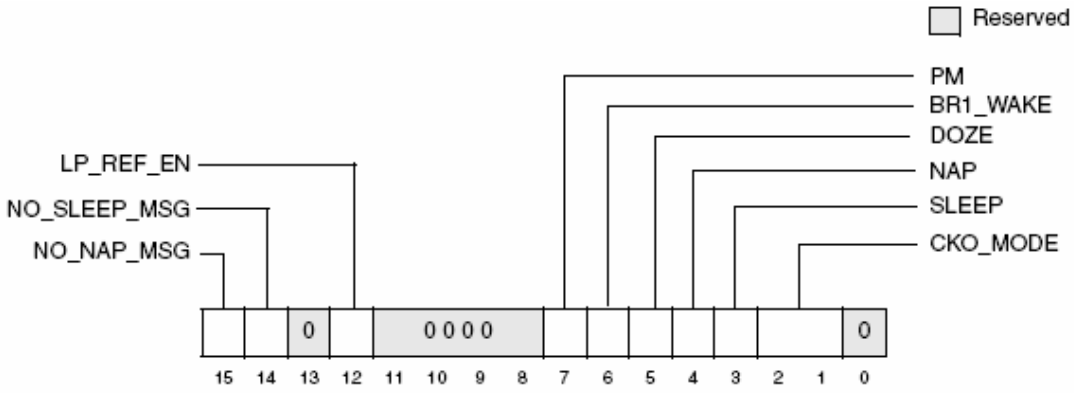


Figure 9: Tsi107



Power Management Configuration Register 2 (Offset 0x072)

Figure 10: Tsi106

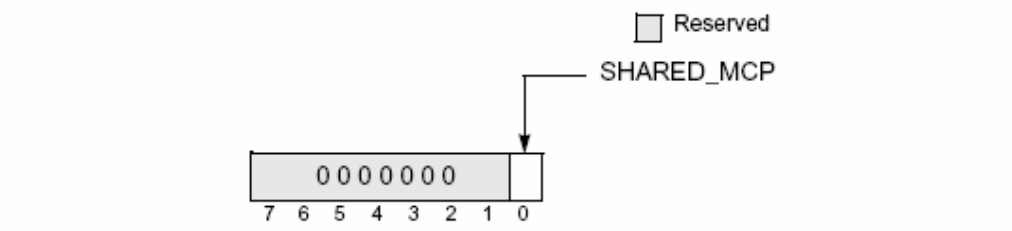
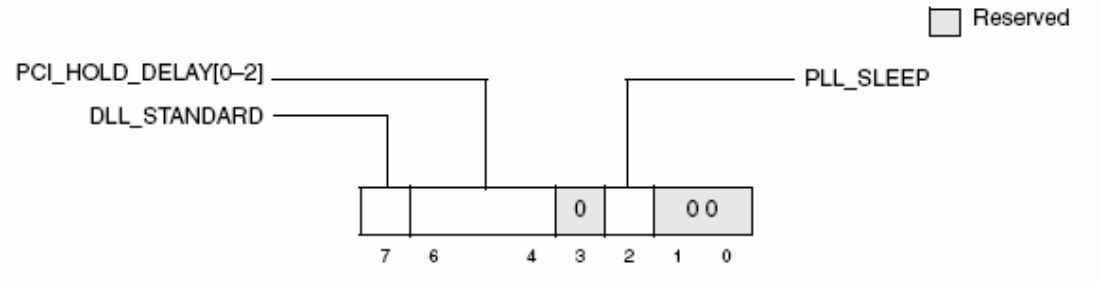


Figure 11: Tsi107



Output Driver Control Register (ODCR) (Offset 0x73)

Figure 12: Tsi106

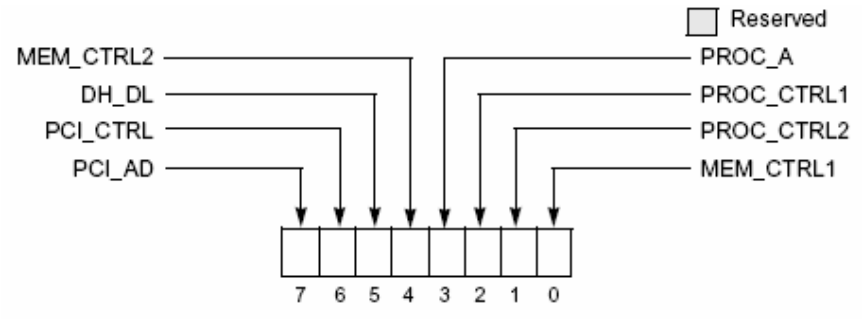
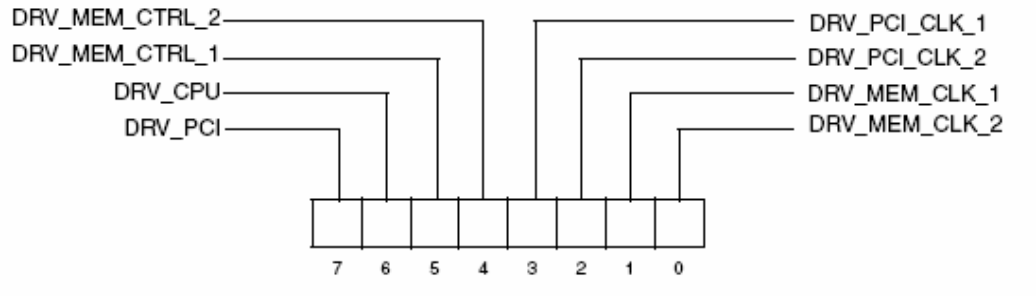


Figure 13: Tsi107



Processor Interface Configuration Register 1 (PICR1) (Offset 0xA8)

Figure 14: Tsi106

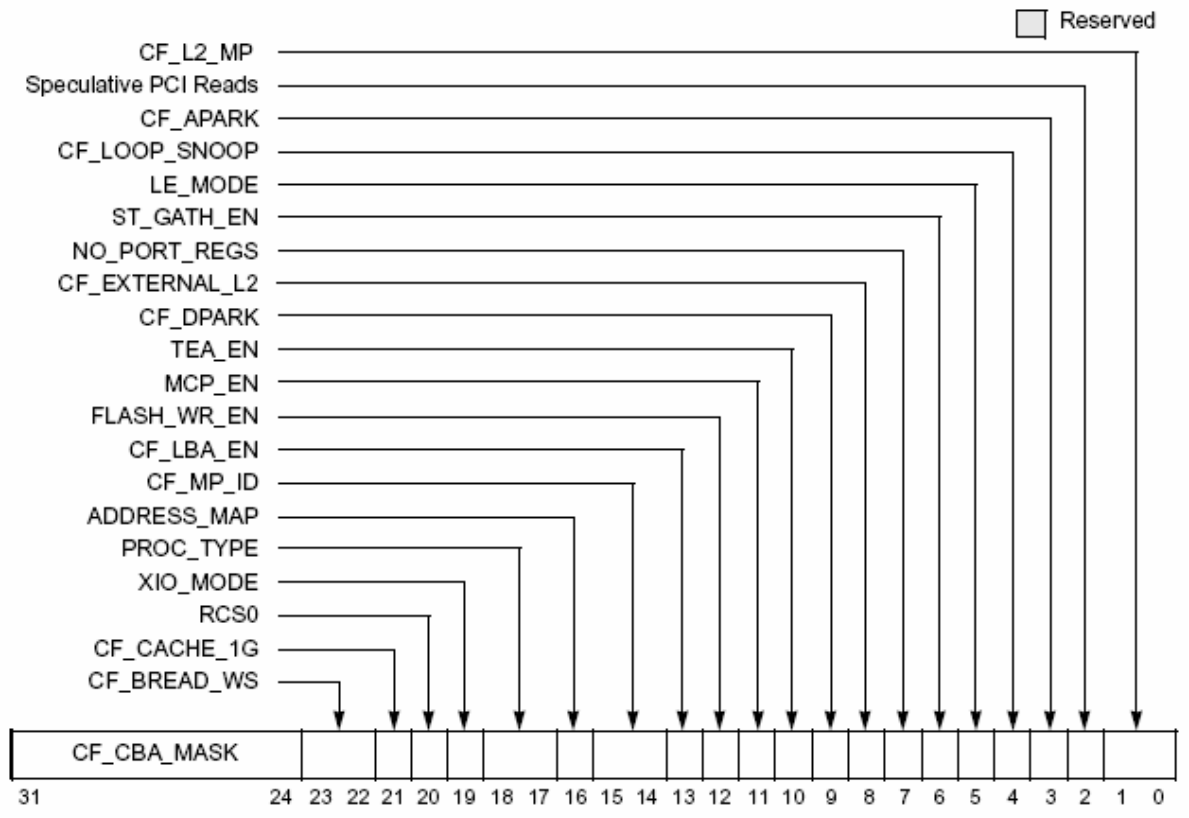
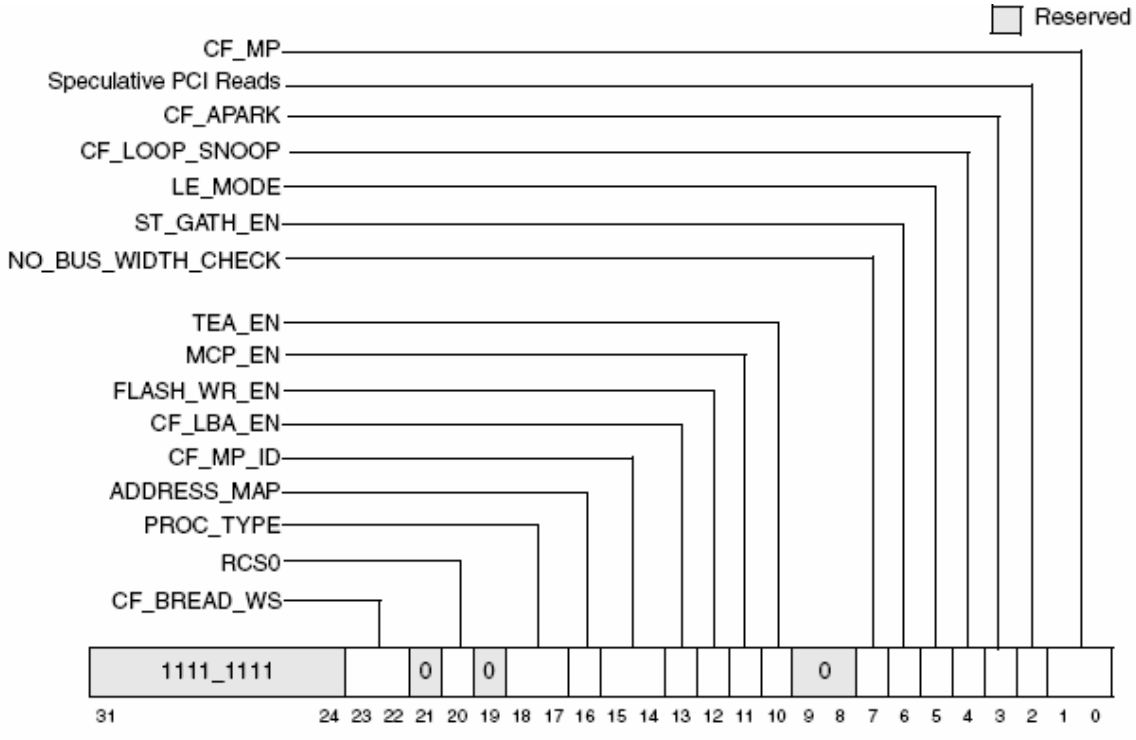


Figure 15: Tsi107



Processor Interface Configuration Register 2 (PICR2) (Offset 0xAC)

Figure 16: Tsi106

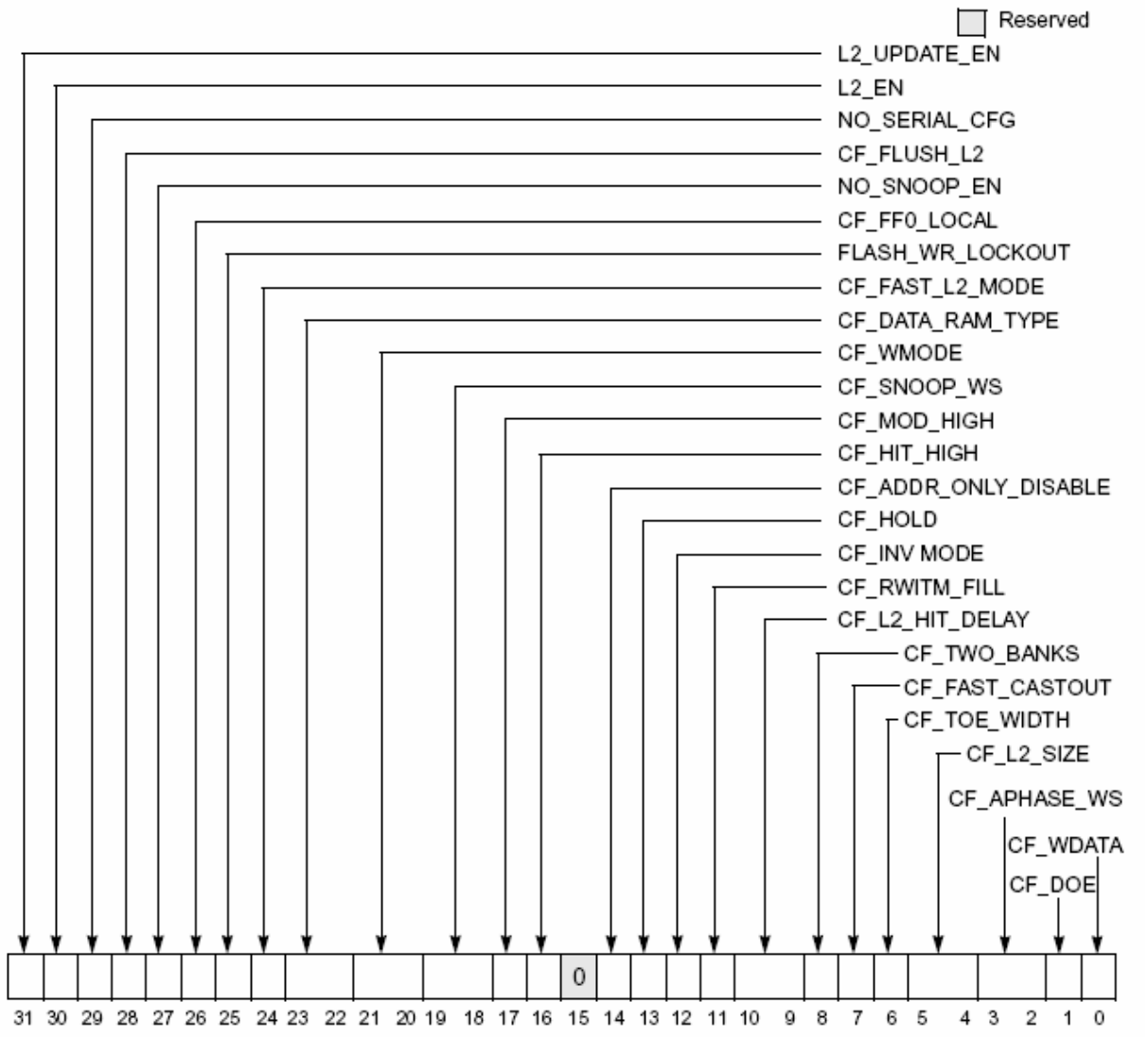
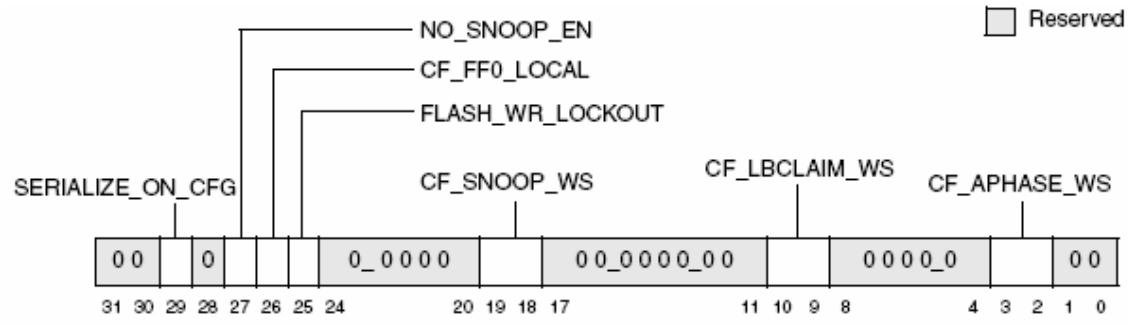


Figure 17: Tsi107



Error Enabling Register 1 (ErrEnR1) (Offset 0xC0)

Figure 18: Tsi106

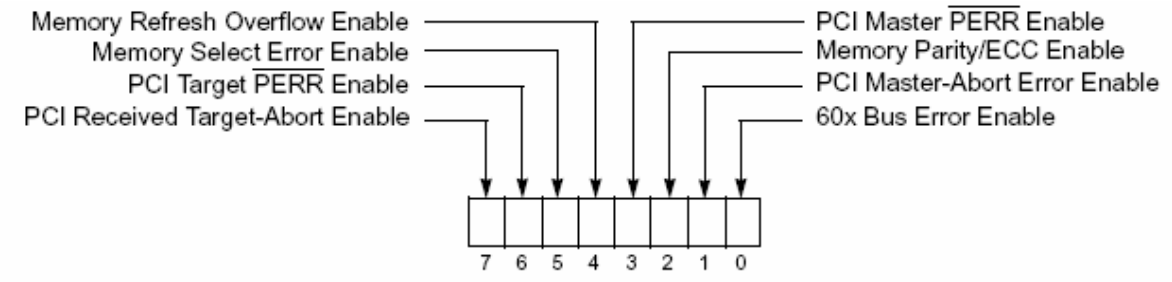
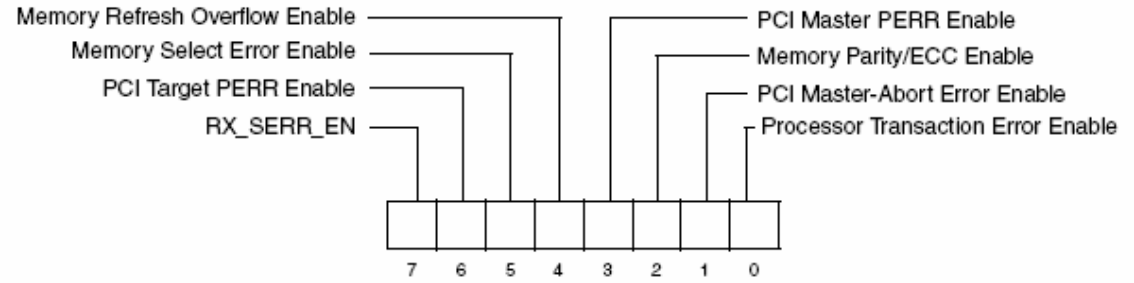


Figure 19: Tsi107



Error Enabling Register 2 (ErrEnR2) (Offset 0xC4)

Figure 20: Tsi106

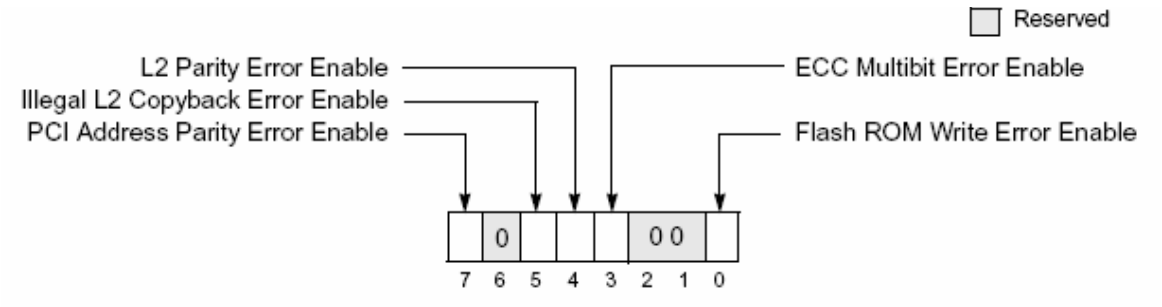
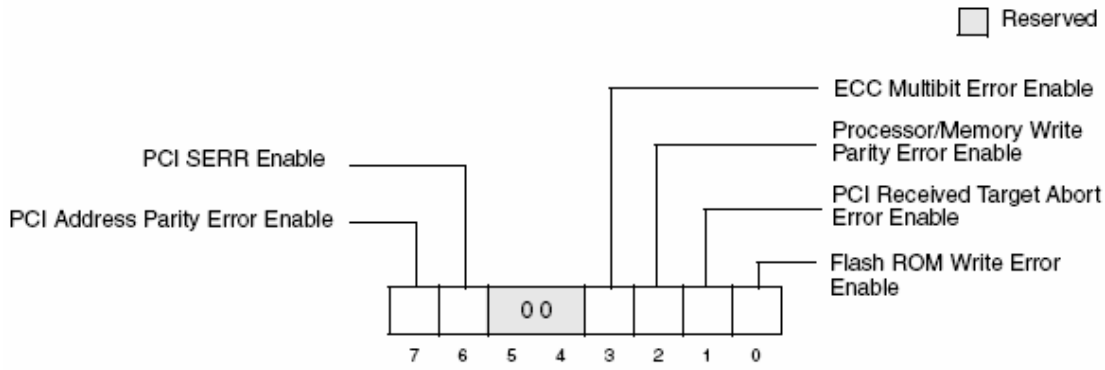


Figure 21: Tsi107



Error Detection Register 2 (ErrDR2) (Offset 0xC5)

Figure 22: Tsi106

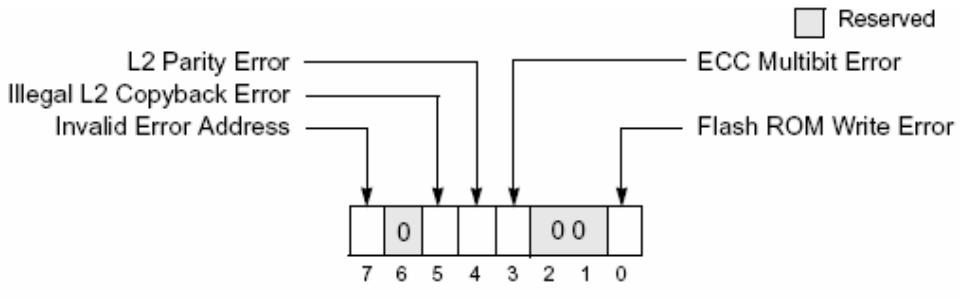
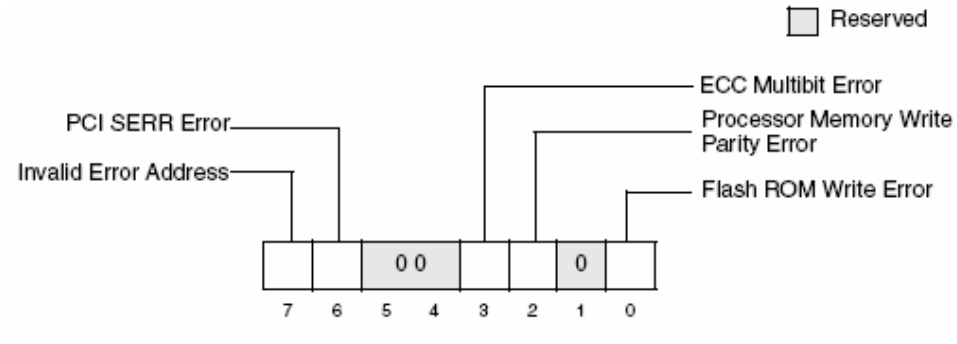


Figure 23: Tsi107



Memory Control Configuration Register 1 (MCCR1) (Offset 0xF0)

Figure 24: Tsi106

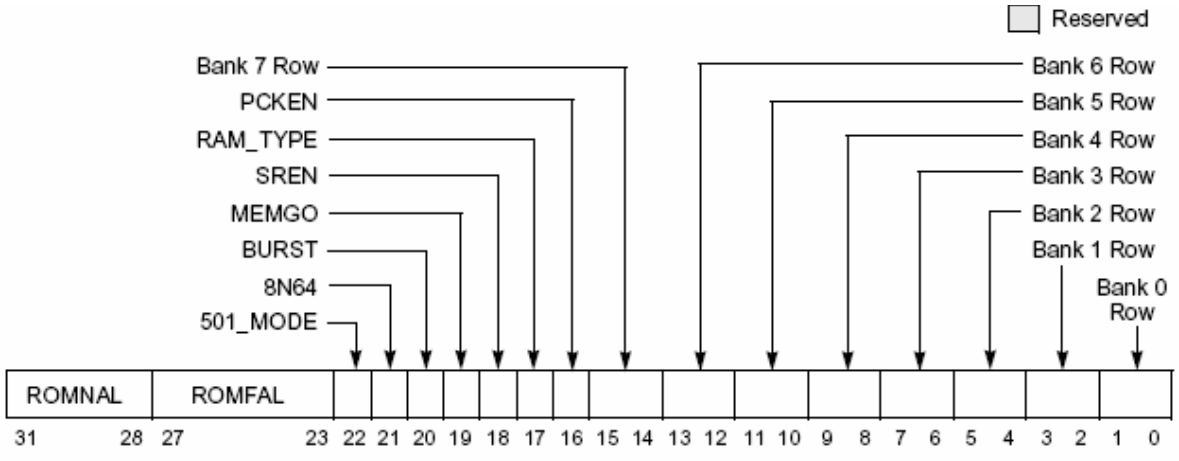
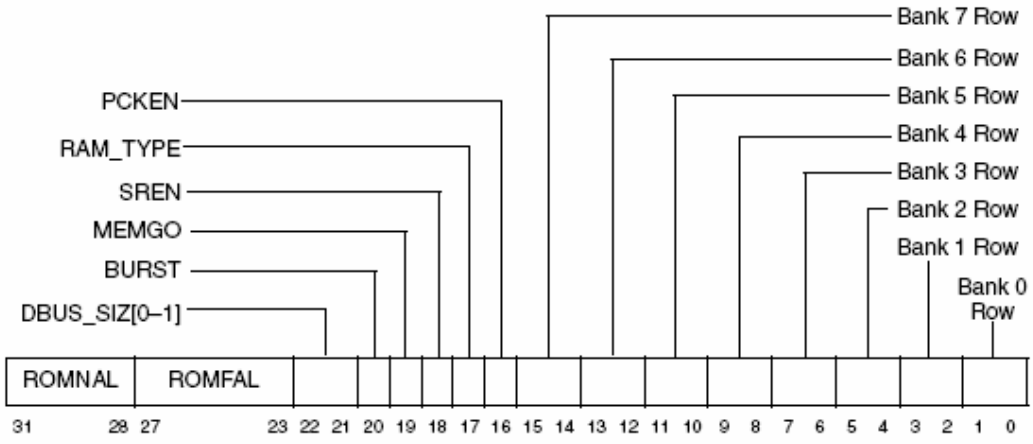


Figure 25: Tsi107



Memory Control Configuration Register 2 (MCCR2) (Offset 0xF4)

Figure 26: Tsi106

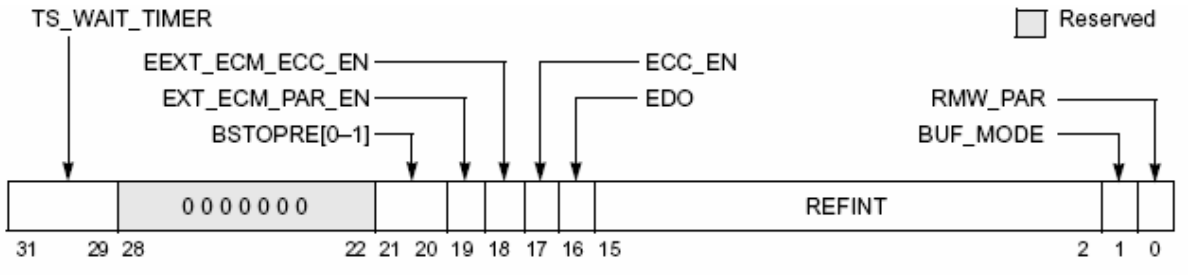
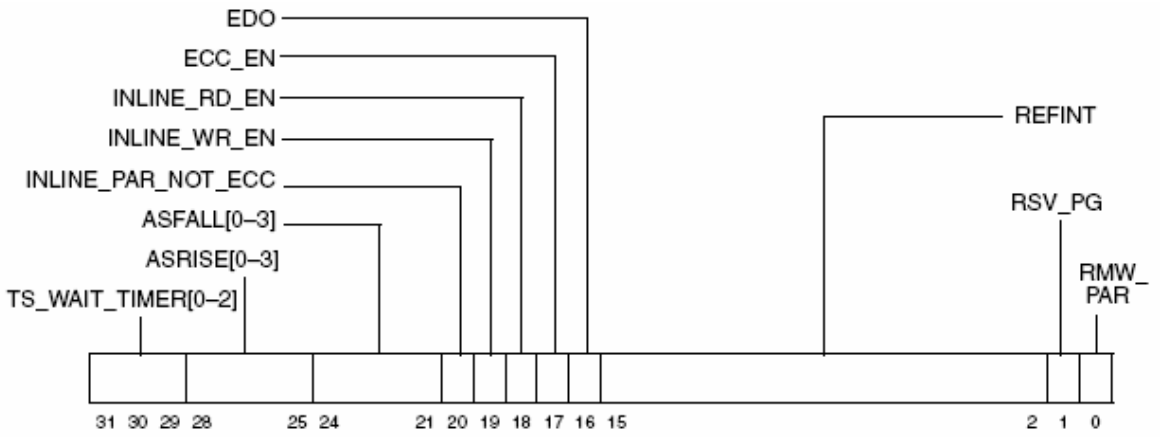


Figure 27: Tsi107



Memory Control Configuration Register 4 (MCCR4) (Offset 0xFC)

Figure 28: Tsi106

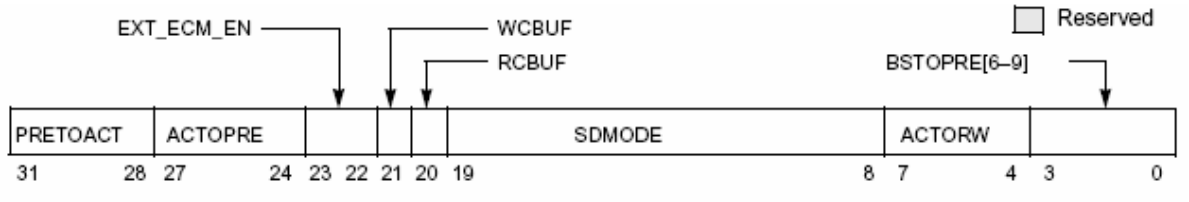
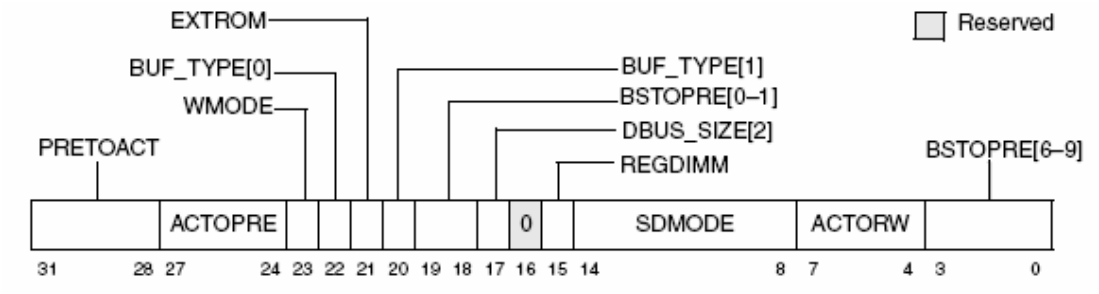


Figure 29: Tsi107



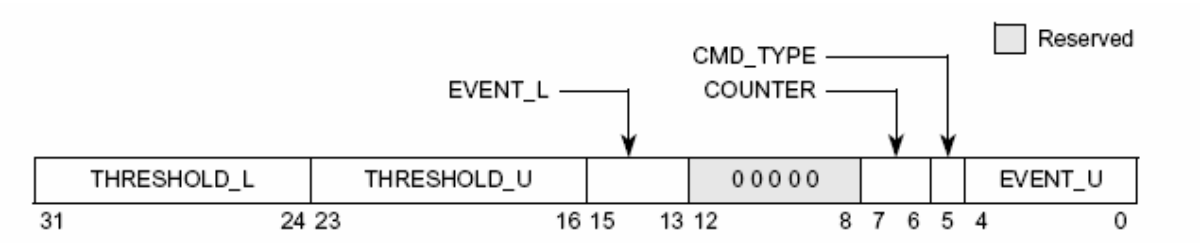
2.2.3 Removed Registers

Disconnect counter (Offset 0x42)

Graphic not shown.

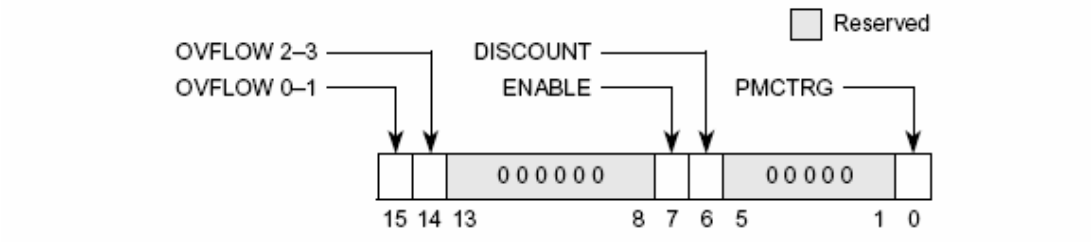
Performance Monitor Command Register (CMDR) (Offset 0x48)

Figure 30: Tsi106



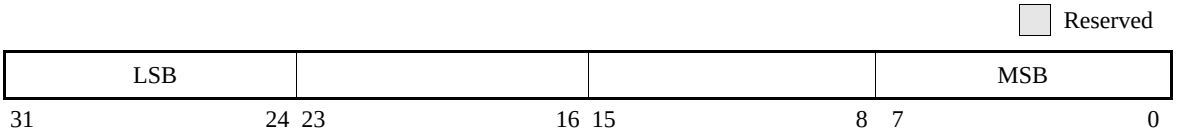
Performance Monitor Mode Control Register (MMCR) (Offset 0x4C)

Figure 31: Tsi106



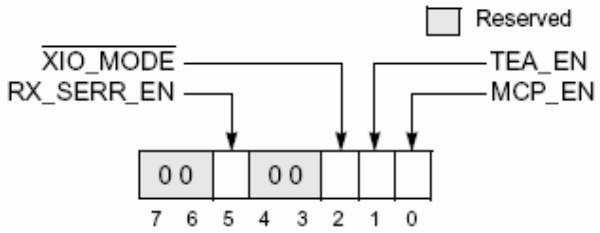
Performance Monitor Counters (PMC0, PMC1, PMC2, PMC3) (Offset 0x50, 0x54, 0x58, 0x5C)

Figure 32: Tsi106



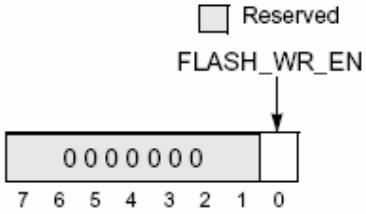
Alternate OS-Visible Parameters Register 1 (Offset 0xBA)

Figure 33: Tsi106



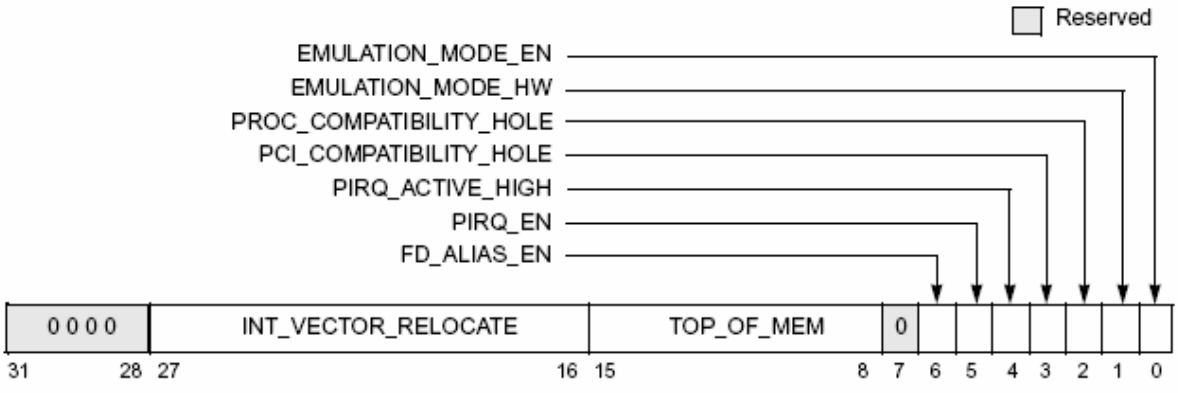
Alternate OS-Visible Parameters Register 2 (Offset 0xBB)

Figure 34: Tsi106



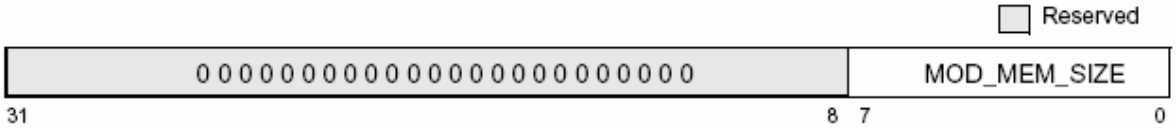
Emulation Support Configuration Register 1 (Offset 0xE0)

Figure 35: Tsi106



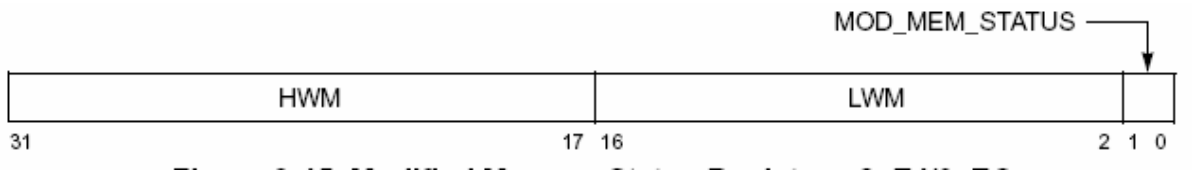
Emulation Support Configuration Register 2 (Offset 0xE8)

Figure 36: Tsi106



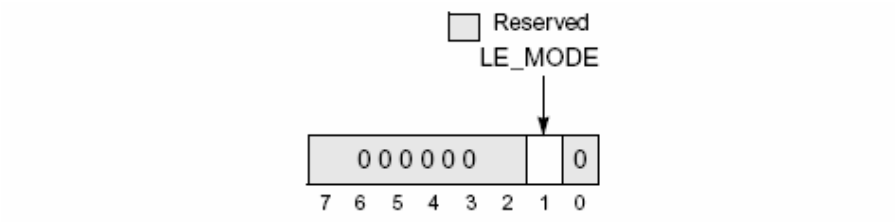
Modified Memory Status Register (Offset 0xE4, 0xEC)

Figure 37: Tsi106



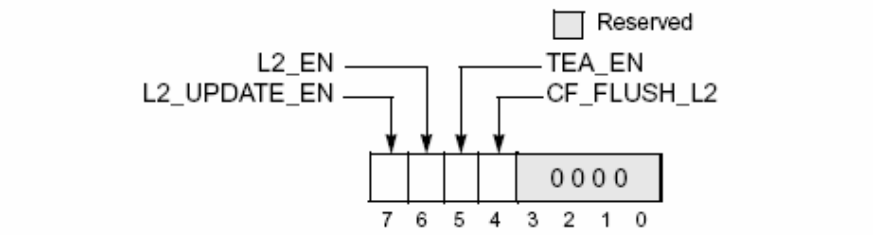
External Configuration Register 1 (Offset 0x092)

Figure 38: Tsi106



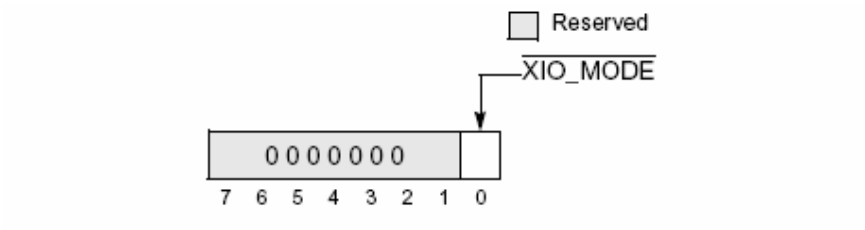
External Configuration Register 2 (0x81C)

Figure 39: Tsi106



External Configuration Register 3 (0x850)

Figure 40: Tsi106



3. Electrical Differences

The two devices have different electrical specifications. Please refer to individual user manuals for more information on device differences.

4. Signal/Pinout Differences

The two devices have different signal descriptions and pinouts. Please refer to individual user manuals for more information on device differences.

5. Physical Differences

The Tsi106 and Tsi107 have different package designs. The Tsi106 package type is a 21 mm x 25 mm, 304-lead C4 ceramic ball grid array (CBGA), while the Tsi107 uses a 33 mm × 33 mm, 503-pin flip chip plastic ball grid array (FC-PBGA) package.