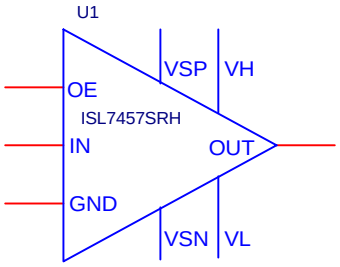
ISL7457SRH

Description

The ISL7457SRH model is written for PSPICE 15.X and higher. It uses a macro modeling technique for speed and ease of modification instead of transistor level model. There are 2 parts to the model. The OLB symbol shown below and the ISL7457.LIB file which contains the PSPICE netlist which the OLB calls out and controls.



Instead of modeling the complete IC only ¼ of the IC is modeled so it's easier to wire the symbol in the circuit schematic as opposed to having one complete part. This allows the user to vary some of the parameters in individual driver blocks to show mis-match effects.

Modifying the Model

The model has parameters which control the various aspects of the model. For example VIH controls the logic 1 threshold voltage for the INPUT signal. These parameters are listed in the table below with explanations. By default the model has been set up for VSP=VH=15, VSN=VL=0. Load capacitance is 1nF. Parameter values can be changed as required.

Param	Description	Min	Typ	Max	Unit
VIH	Logic "1" Input Voltage		1.63		V
VIL	Logic "0" Input Voltage		1.4		V
CIN	Input Capacitance		5.7p		F
RIN	Input Resistance. This will also affect input leakage current.		3G		Ω
TDP	Turn on delay from 0 to 5V on IN with CL=1nF. The sets the ideal internal prop delay. The measurement is done at 50% of input signal to 10% of OUT signal. Therefore there will be an extra 10% of prop delay due to 10% of the rise time. Therefore from the datasheet 11.5ns – 0.1 x 11ns = 10.4ns		10.4n		sec
TDN	Turn off delay from 5V to 0 on IN with CL=1nF. The sets the ideal internal prop delay. The measurement is done at 50% of input signal to 90% of OUT signal. Therefore there will be an extra 10% of prop delay due to 10% of the fall time. Therefore from the datasheet 13ns – 0.1 x 12ns = 10.4ns		11.8n		sec
ROH	High side on resistance		3.5		Ω
ROL	Low side on resistance		3.0		Ω
RLEAKP	High side drive leakage resistance. This is used to		3G		Ω

	emulate ILEAK+				
RLEAKN	Low side drive leakage resistance. This is used to emulate ILEAK-		3G		Ω
ISRSC	Peak source current. This effectively determines the rise time for the output. This is calculated by Vout / Trise = ISRC / Load Cap. Here its (15V x 0.8) / 11ns = ISRC / 1nF. Where 0.8 is 10% to 90% measurement. This works out to 1.09A. However, there is the effect of ROH x Load Cap which will increase the rise time. Therefore this number needs to be adjusted by hand to improve the accuracy.		1.27		A
ISINK	Peak sink current. This effectively determines the fall time for the output. This is calculated by Vout / Tfall = ISINK / Load Cap. Here its (15V x 0.8) / 12ns = ISINK / 1nF. Where 0.8 is 10% to 90% measurement. This works out to 1.0A. However, there is the effect of ROL x Load Cap which will increase the fall time. Therefore this number needs to be adjusted by hand to improve the accuracy.		1.07		A
VEH	Logic “1” Enable Voltage		1.63		V
VEL	Logic “0” Enable Voltage		1.4		V
CEN	Enable Input Capacitance		5.7p		F
REN	Enable Input Resistance. This will also affect input leakage current.		3G		Ω
TEN	Turn on delay from 0 to 5V on OE with RL=1KΩ		12n		sec
TDIS	Turn off delay from 5V to 0 on OE with RL=1KΩ		27n		sec
IQ0	Quiescent current per driver with input low		0.43m		A
IQ1	Quiescent current per driver with input high		0.19m		A
UVLO	Minimum power supply voltage VS which the IC will start to operate		4.5		V
CINT	Capacitance per driver for internal switching current as per eq 1 of page of the datasheet		80p		F
RESD	Parallel resistance of ESD diodes. This emulates the leakage current from the diodes. This will effect the leakage currents.		3G		Ω

To change any of these parameters, left click on the OLB symbol and then right click. You can either edit properties or edit part. If you chose edit properties, the parameters will be listed in the columns. Click on the column and edit the value. If you chose edit part, scroll through the list and edit the parameter.

For either method you choose, recommend also turning on both name and value for the display. For edit properties, you will need to right click on the column to get the display option. This is helpful to show the changes made to the model such as time delay mis-match.

Recommend setting ITL1,ITL2 and ITL4 to 1000 in the PSPICE Options to minimize convergence issues.