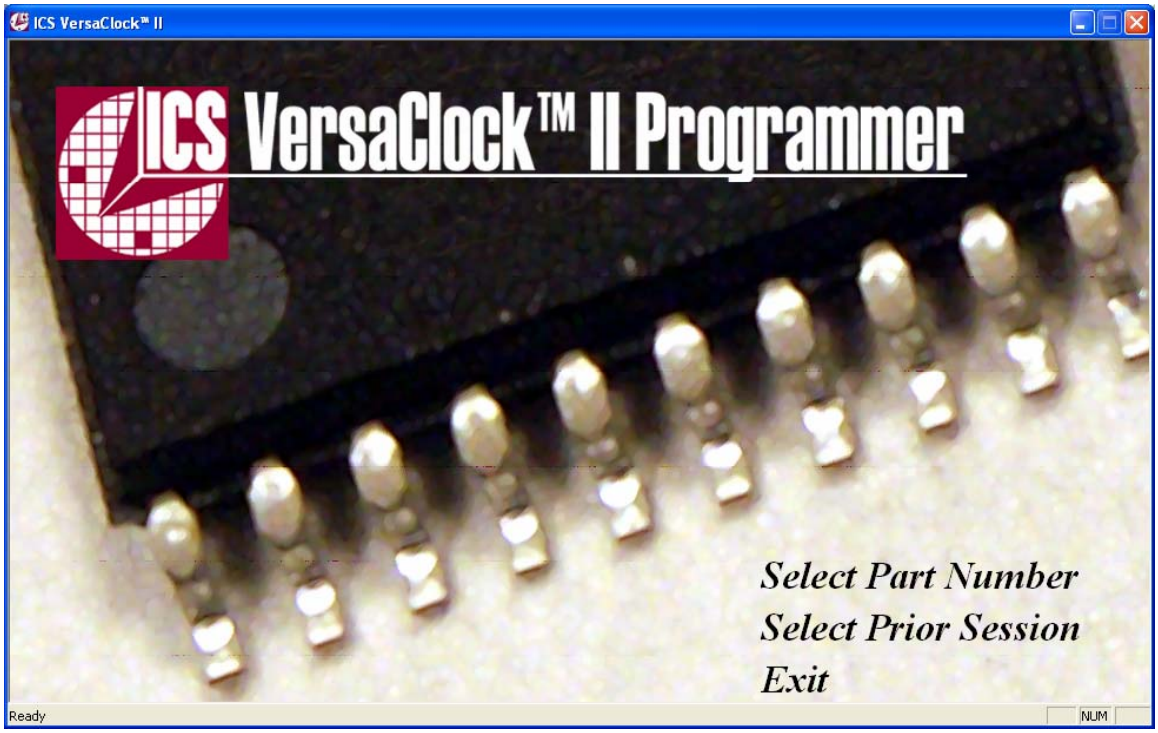
# ICS VersaClock™ II User Guide



ICS VersaClock™ II User Guide for Microsoft Windows©



## Table of Contents

## New Features for VersaClock™ II

1) All register/single register configuration option
2) Pin locking capability
3) Manual pin assignment
4) Pin diagram labels
5) Backward/forward compatibility between previous versions of VersaClock™

## 1) Programmable Clocks – Introduction

The ICS programming software is targeted at enabling novice through experienced PLL designers to easily select and optimize performance from the ICS programmable clock product line. These products include devices that are EPROM (OTP) programmable, as well as serially programmable.

The software evaluates the desired input and output frequencies and sets the corresponding PLL parameters to optimize the clock output jitter and device power consumption. For the given input frequency, a pin allocation map is generated.

The ICS programmable clock portfolio contains products with the capability to incorporate Spread Spectrum functionality on selected clock outputs. Spread Spectrum creates a regular frequency "dithering" of the output frequency to reduce the electro-magnetic interference (EMI) radiation associated with a fundamental clock signal propagating around a system or across cabled interfaces.

The Spread Spectrum capability can be enabled with either "Center Spread" or "Down Spread" functionality at a variety of selectable percentage increments and modulation frequencies.

## 2) Installing ICS VersaClock™ II Software

a) Software is available for free download from:

***http://search.icst.com/software***

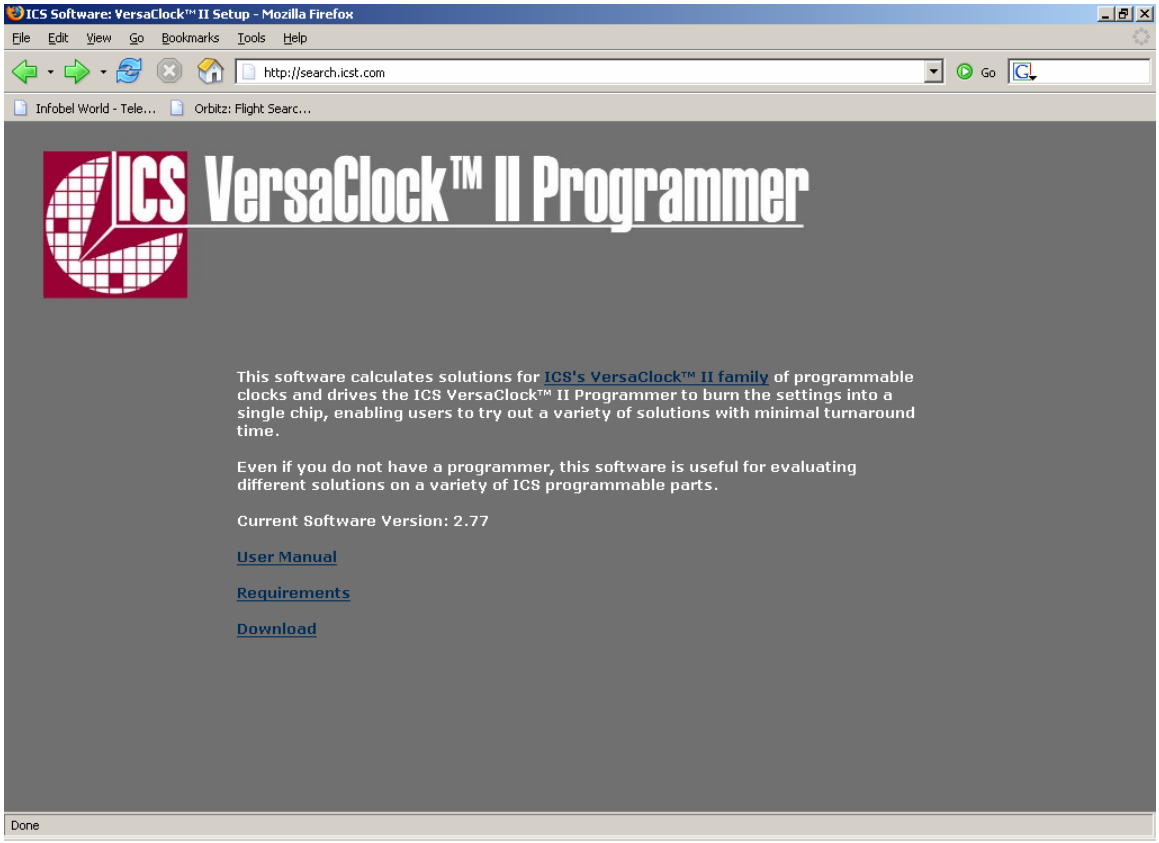
b) You must install this application onto your computer's hard disk; you cannot run this program from the Internet.

c) Supported Computer Configurations: Windows 95/98/2000/ME/XP with a minimum of 32 MB of RAM and 10 MB of available hard disk space.

d) There are two versions of the VersaClock™ II software: "Web Based" and "Desktop".

- VersaClock™ II web based version software downloads the latest part information every time the software is used. VersaClock™ II Web Based requires that the computer be connected to the Internet to operate.
- VersaClock™ II desktop version software allows non-Internet connected operation. Part information and software updates are provided only when downloaded and installed from the download site above.

Both versions of the software may be installed simultaneously on the same computer without conflict.

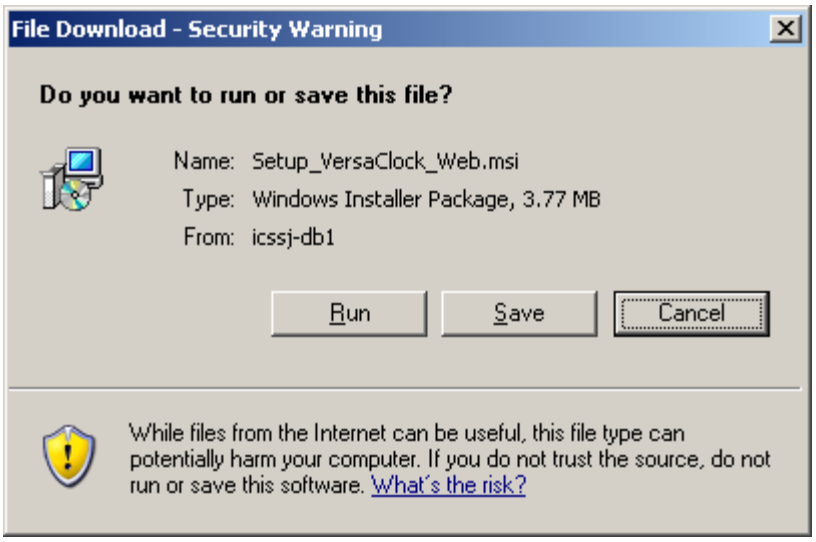



** Note: VersaClock™ II software utilizes Microsoft™ Windows Installer software. Some versions of Windows may not have this utility installed. Free download is available at:

For Windows 95/98/ME: Microsoft Windows Installer Software

For Windows NT 4.0/2000: Microsoft Windows Installer Software

By selecting the download of either VersaClock™ II software option, the following screen will appear:




Select Run to automatically initiate the installation process and install over older versions of the software if defaults settings are used.

You do not need to restart your computer once the software is installed. You are now ready to use the ICS VersaClock™ II software.

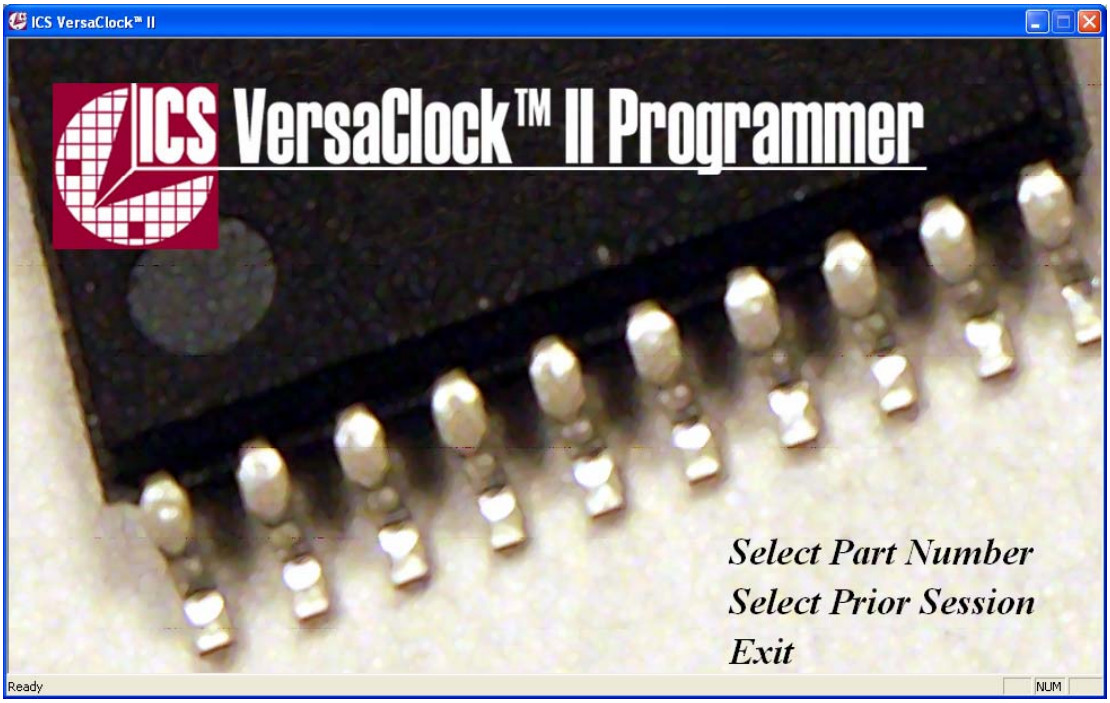
[Note: Periodically, the VersaClock™ II software will be updated and products added. When connecting to the product database, you will be alerted when new software is available. Desktop versions of the software must be manually checked and downloaded.]

## 3) Programming Software Operation

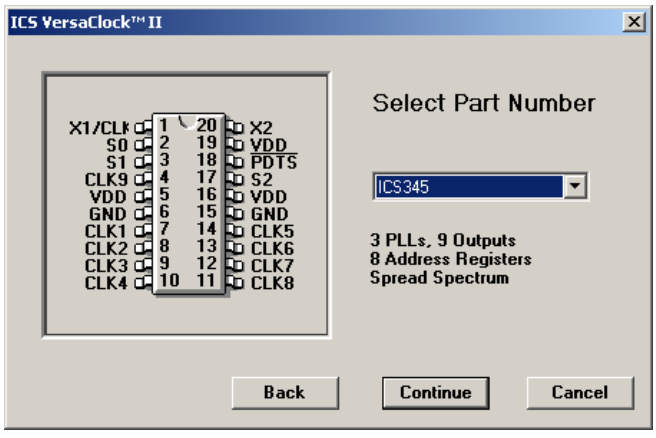
### *Getting started*

From your desktop, you will have icons for either “VersaClock™ II” (for web based version), “VersaClock™ II Desktop” or both. Double click on icon to start. You may also start from Start > Programs > VersaClock™.

The VersaClock™ II software can be initiated by selecting the desired part number or by returning to a prior saved session. Selecting by part number provides a brief description of each part’s functionality.




### *Selecting a Part*




Each part is provided with a brief description of features that are available.

## 4) Configuring Devices - Two Information Views

All Registers View -

Ability to manipulate all registers simultaneously. All configuration inputs are entered in a matrix format to ensure that address selections conform to the anticipated changes.

To facilitate configurations, each pin can be labeled to remind the user how the output will be used. Tabs labeled with Req. ppm, Spread, Drive, etc. use the same matrix to apply the functionality to the target outputs during the single computation.

Selection of this mode is provided by selecting View > All Registers option.

Single Register View - Allows user to work on one register at a time.

Ability to configure outputs for a single register in a single screen.

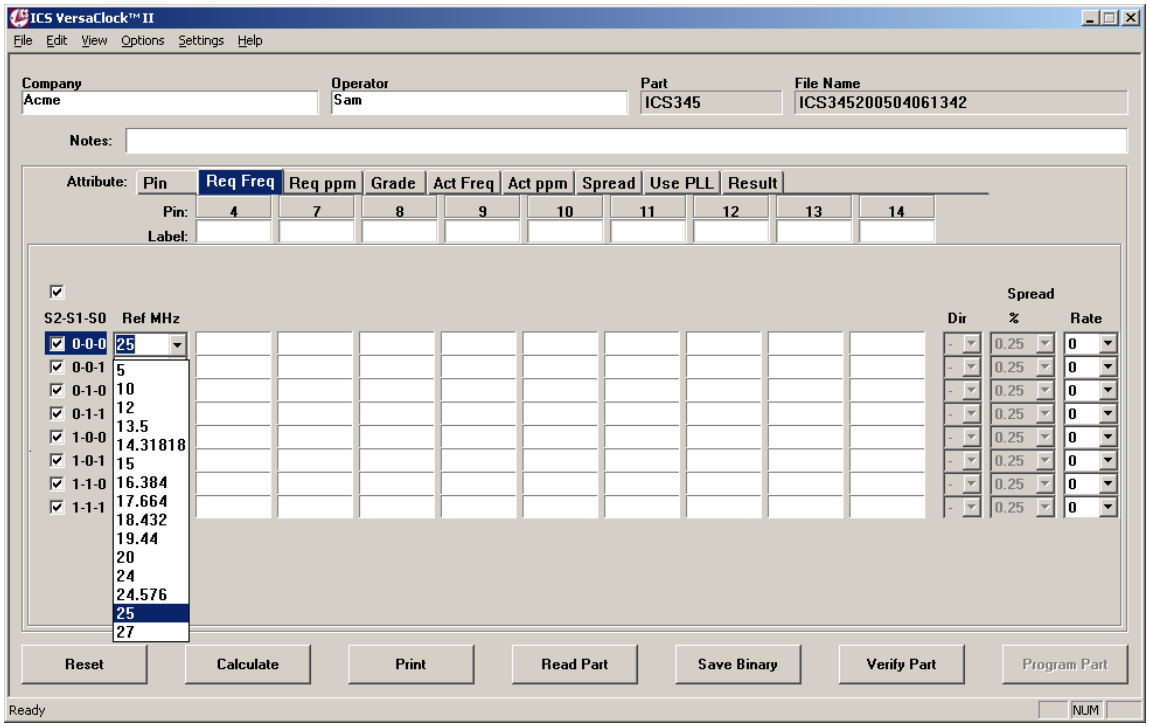
Register Tabs across the top of the screen allow the user to select the register and copy/modify configurations on a register-by-register basis. There is the ability to copy contents of one register into another for configuration.

Selection of this mode is provided by selecting View > Single Register option.

*[Hint: It is often useful to toggle between the two views to establish a complete configuration. For example, use All Register View to establish register address frequency logic table and fix clock output pin assignments. Once outputs are established, go to Single Register View to set accuracy tolerance, spread spectrum amounts or clock output drive. Finally, return to All Register View to calculate all register simultaneously, to assure register-pin relationships.]*

## ***All Register View***

Inserting Data




Fields that are accessible to the user are in white. The user can include text information in the Company, Operator and Notes fields for reference. While the program is operating, the Company and Operator fields will default to the last session's values.

### Input Frequency Selection

The user must select the starting frequency from which the operation of the PLL will be derived. Input frequency selection may impact the output clock accuracy, jitter or power consumption. Best performance is generated when the input frequency is an integer multiple of the desired output.

Users may select standard crystal frequencies from the pull down menu, or type in a value in the space provided.

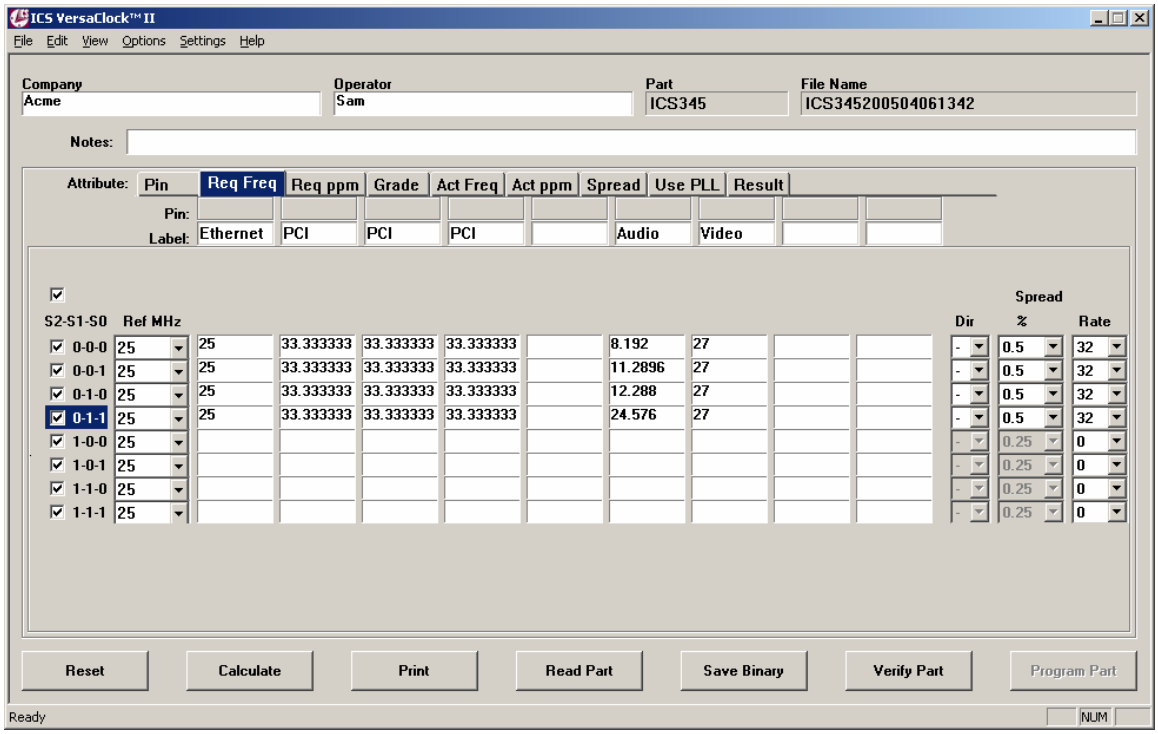
Strategies for selecting the input frequency may include:

a) Use the target output frequency that is most sensitive in the system. It would ensure at 0 ppm solution and lower phase noise performance.

b) Use of a common divider frequency to several outputs. This may minimize the number of PLLs that will be needed, thereby reducing power consumption.

A pull down menu of common input frequencies is provided. Other frequencies may be typed into the Reference Frequency window at any time. *If typing in a frequency, place as many frequency decimal places as necessary, to insure best accuracy solution.*

(NOTE: A single Input Frequency is the default condition for a programmable device session. All successive registers will automatically fill with the last frequency selected. Each register configuration is calculated independently, so a single device may be used in multiple applications that require different clock references. A warning will appear if a second reference is selected for a register within a single session. Once a second reference is selected, it is recommended to verify the selected reference for all registers.)




The Register that is being modified and the Attribute that is active will be highlighted. This allows you to focus on the proper information to be entered. Make sure that the entries for each Attribute aligns in the matrix with the target frequency.

**Attributes Tabs**

a) Pin – Unassigned prior to the calculation unless the Manual Pin Assignment Option is applied in the Options pull down menu

b) Req. Freq – Target frequency to be synthesized

c) Req. ppm – Accuracy tolerance window permissible for target frequency

For each target output frequency, the user has the ability to specify the maximum tolerable output clock synthesis error in ppm (parts per million). This is the frequency error additive to the error of the reference input. If no value is included, the default is zero. This is particularly helpful in cases where the input reference frequency does not allow, or gives poor solutions for 0 ppm accuracy.

The software will provide the best performance solution within the given accuracy tolerance window. To achieve improved jitter performance, the window must be widened.

Entering *positive* numbers – the accuracy window is the absolute value (+ and – ppm error values will be considered)

Entering *negative* numbers – only frequencies lower than target frequency are considered

The ppm accuracy has an upper bound of 9999, but the user should not exceed the deviations allowable by the user's system. While higher accuracy solutions may be achievable, a less accurate solution (within designated bounds) may be selected by the software, due to performance criteria.

d) Grade – Solution rating from 1 red bar to 5 green bars for each target output

e) (See Solution Interpretation section below)

f) Act. Freq – Solution actual output frequency calculated

g) Act. ppm – Solution actual ppm accuracy of actual frequency from target

h) Spread – Check box to turn on Spread Spectrum capability for target output

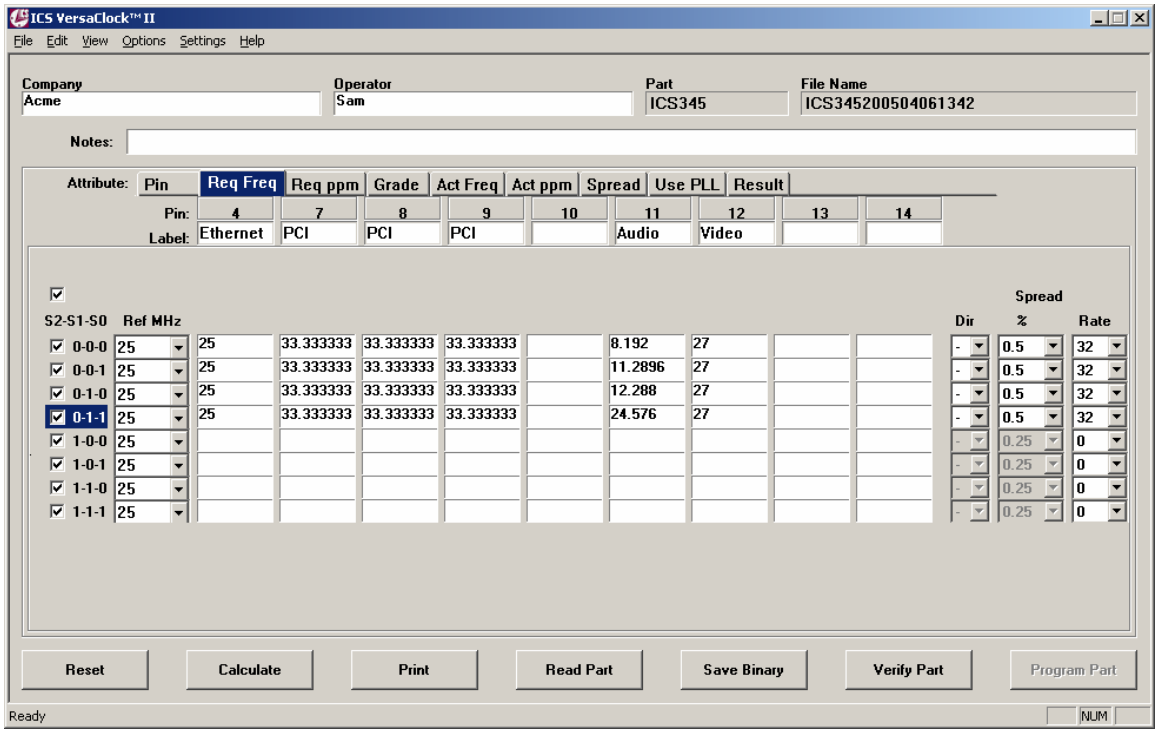
i) Use PLL – Check box forces an output to be synthesized, rather than using a buffered, reference output. For outputs that must be synthesized, checking this box will not affect the output.

j) Result – Hexidecimal configuration string for each register, along with estimated current consumption (Idd) and Spread Spectrum modulation rate (where applicable)

## Manual Pin Assignment

a) Manual pin assignment is accessible from the Options menu. Selecting Manual Pin Assignment will reset any present solution. Manual Pin Assignment is a toggled feature and may be turned on/off as desired.

b) With this feature turned on, target outputs be inserted in the field aligned to the pin number column.




## Spread Spectrum

Spread Spectrum is a technique whereby the output frequency is modulated to minimize the system noise energy associated with the clocking of data around the system. This noise energy may generate radio frequency interference with other electronic devices and is a key component of U.S. FCC certification.

a) Center Spread

The frequency spread is distributed evenly, in both the positive and negative directions from the target output clock frequency. The average frequency, in this type of spread spectrum operation, is the same as the target frequency. Selection of the center spread percentage is defined as the deviation in both the positive and negative directions. The total spread excursion is 2x the selected value.

b) Down Spread

Some systems cannot tolerate clock frequencies that exceed the target frequency. For example, some processor ICs are rated at a maximum operation frequency. Down spread reduces the target frequency such that with spread spectrum enabled, the maximum frequency generated (at the maximum, positive excursion from the new center frequency) is at or below the specified output clock frequency. Down spread reduces the average system clock frequency from the target frequency. The total spread excursion is equal to the selected spread percentage value.

c) Spread Modulation Rate

When selecting spread spectrum, the user has the option of selecting either 32 kHz or 120 kHz modulation rate. The PCI specification specifies that spread spectrum modulation must be between 31 and 33 kHz. For other applications, either modulation rate may be chosen.

A consideration for selecting the 32 kHz modulation rate is whether there is a “down stream” PLL or Zero Delay Buffer (ZDB) that the clock is driving. The PLL bandwidth being driven must be at least 20 times the modulation frequency. Faster modulation rates are more difficult for PLLs to track.

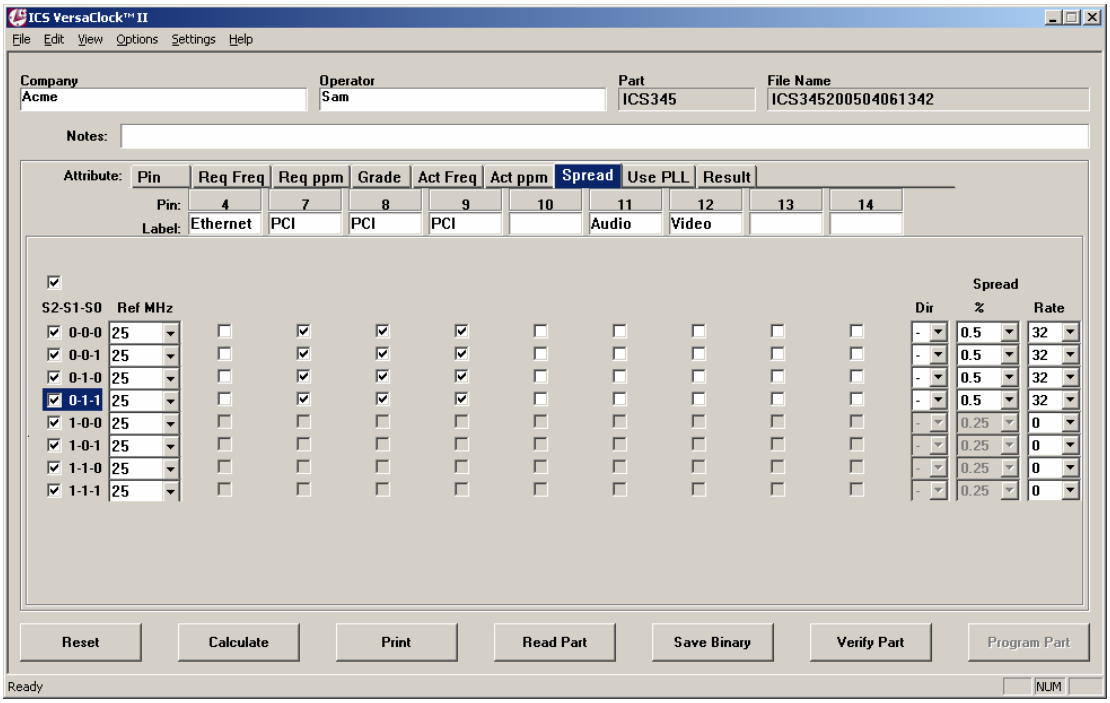
120 kHz modulation has been measured to provide approximately 25% additional EMI attenuation compared to 32 kHz, but is not always permissible in the system.

d) Selecting Spread Spectrum Outputs

Once the Spread Spectrum direction, modulation rate, and percentage deviation are selected, the outputs that will be modulated must be selected.

By going to the Spread tab, a matrix of check boxes corresponding to the target outputs is available. Only outputs with target frequencies will have enabled check boxes. Checked outputs will have modulation applied.

Note: Spread Spectrum is not available on all PLL outputs. To modulate multiple frequencies, there must be a common PLL VCO frequency that can be easily divided into the target frequencies. The Spread Spectrum magnitude percentage and direction will be the same for all outputs.

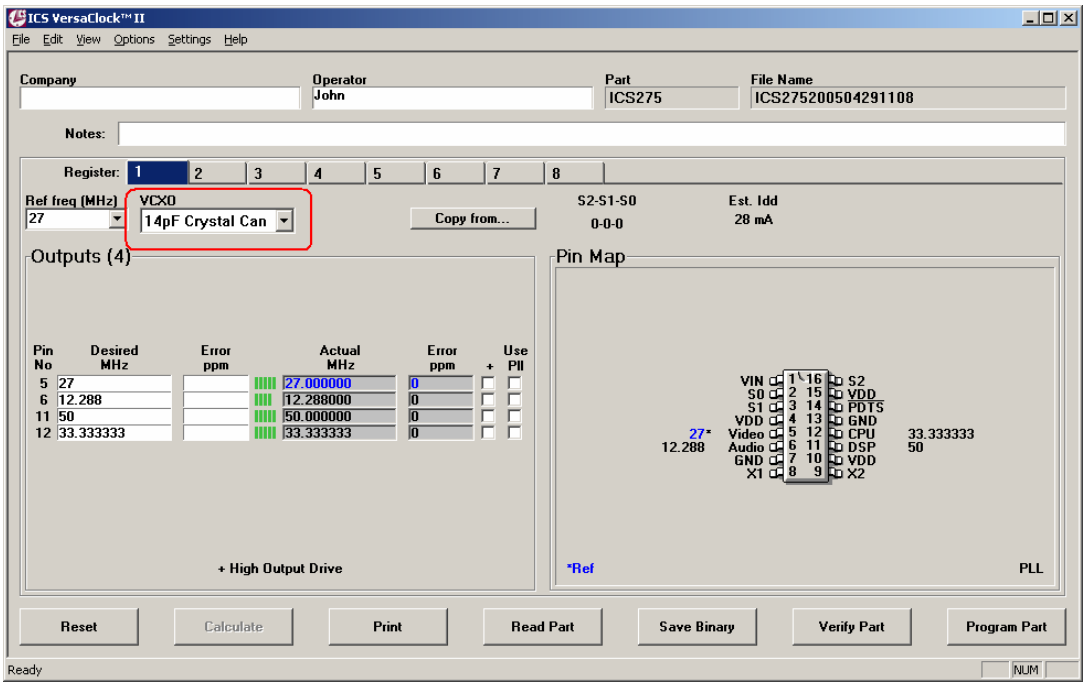


## VCXO

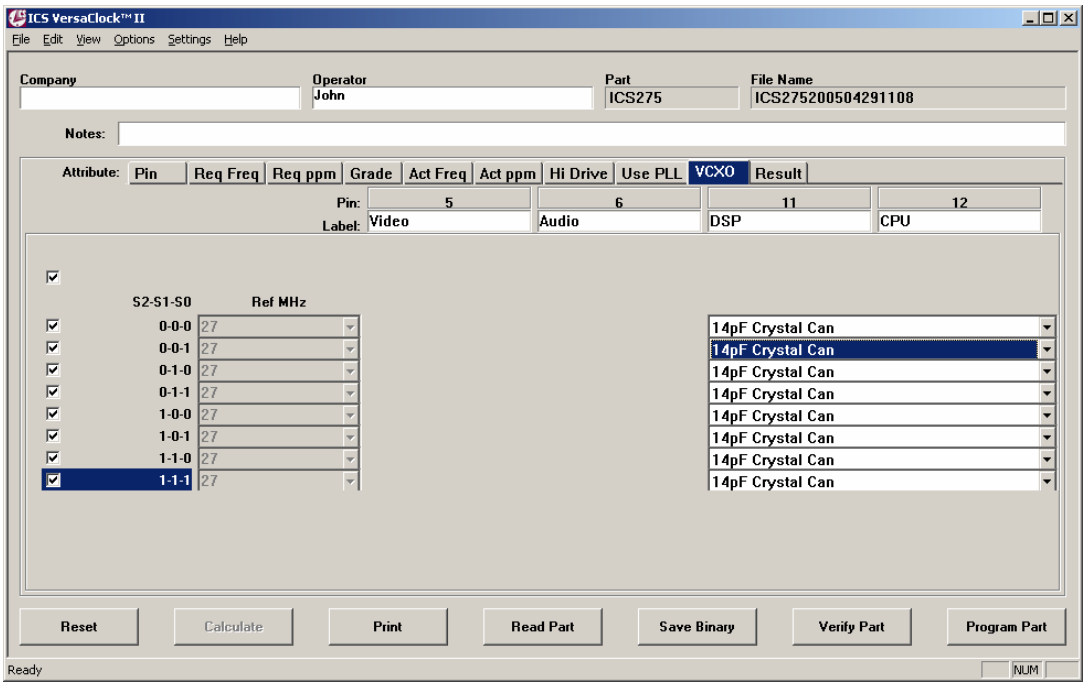
For devices that have programmable VCXO capability, a pullable crystal must be selected. Information on selecting an appropriate crystal for his application is available from the ICS website in Application Note MAN05.

For each device, a pull down menu will appear with supported crystal load capacitance values. The VersaClock software will adjust the device VCXO offset and gain to match the crystal load and provide the optimum configuration.

Single Register View




All Register View



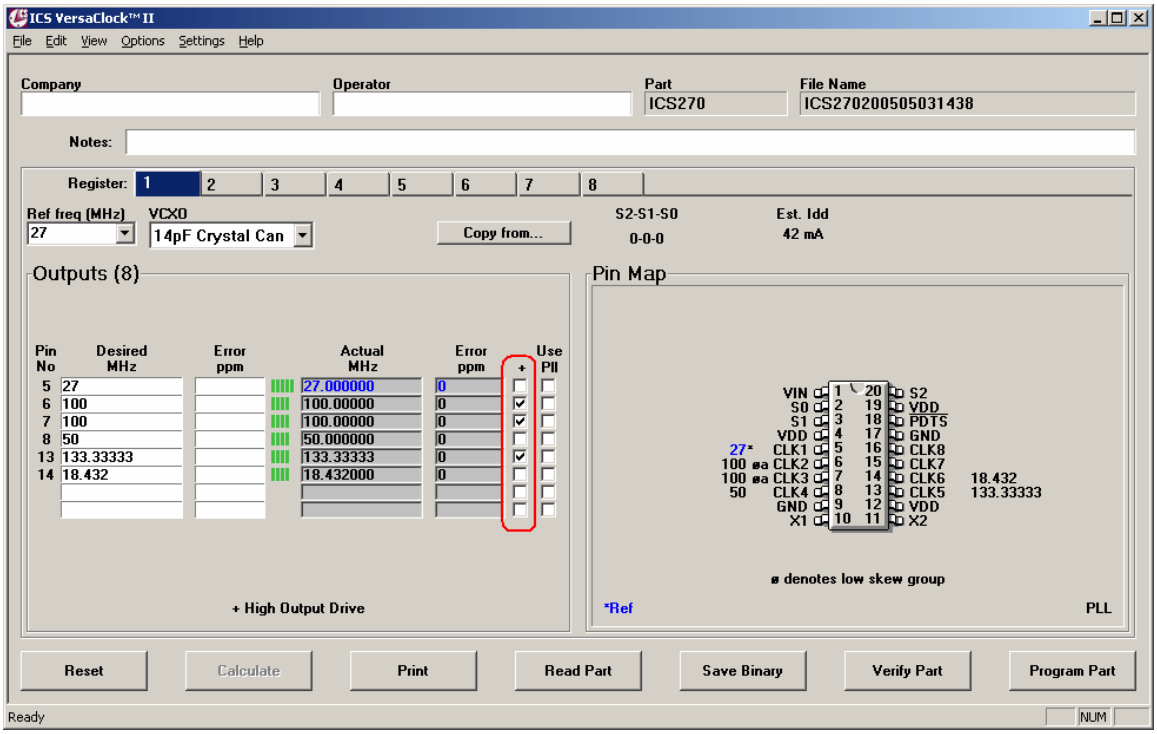
### Adjustable Output Drive

Some devices have adjustable output drive capability. For those devices, a check box is provided for low drive (unchecked) and high drive (checked) control for each output, individually.

High drive should be set for outputs above 100MHz, as well as VDDO capable parts, where VDDO is 2.5V or less.

In Single Register View, there exists a column denoted by a "+". Check all outputs that required high drive.

For All Register View, check boxes in the output matrix.



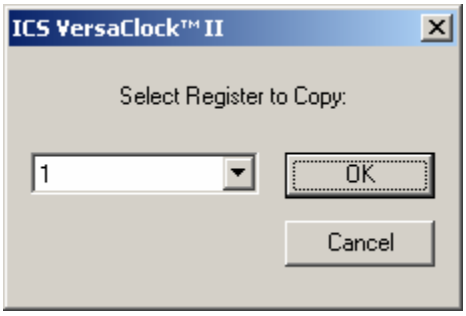

Single Register View

### Copy Register

Calculated or un-calculated register configurations may be copied to other registers to facilitate the population of the target matrix.

To do so, you must first go to the address you wish to copy to. Clicking on the address or one of the target fields in that register, you will switch the focus to the register. In the example above, the address 0-1-1 is highlighted in blue.

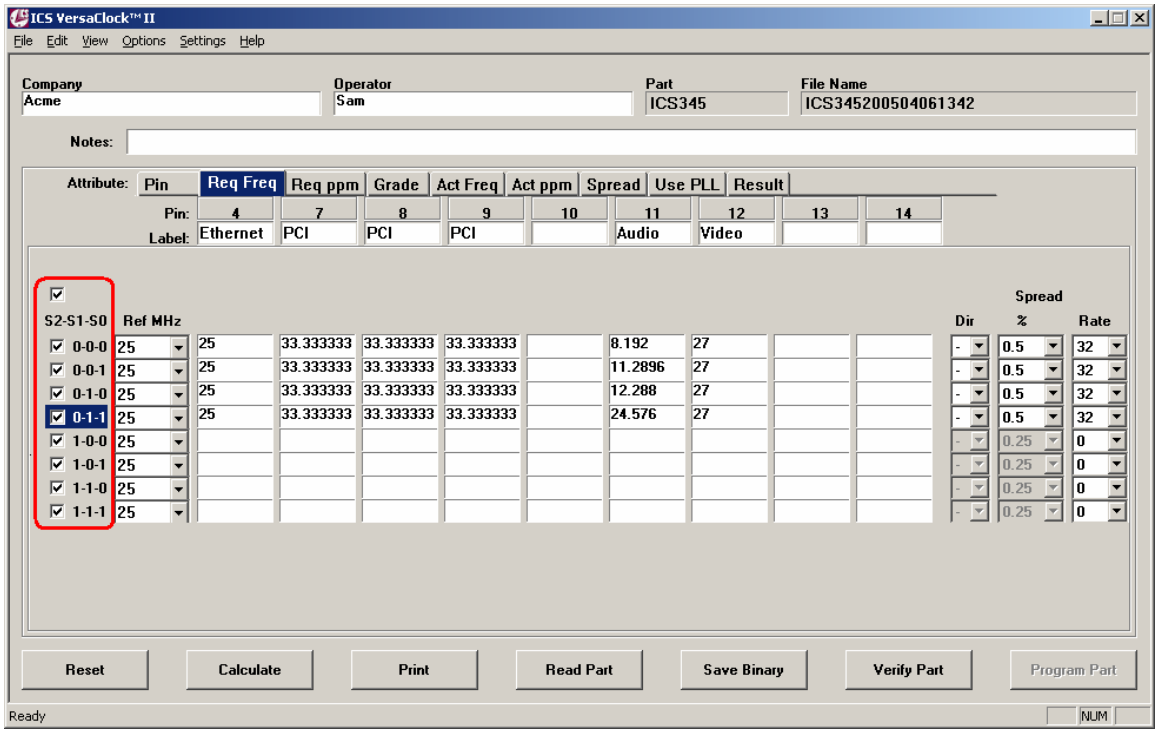
Selecting Options > Copy Register (or ALT-C) displays a window that allows you to select the source register from which to copy.




The pull down menu allows the copying of any register to the target register. You do not need to go in any specific order.

Once copied, any field may be edited prior to configuration calculation.

### Calculation Reset




One or multiple registers can be Reset and Recalculated.

Registers with the box next to the address checked (seen above, circled in red) will be reset when the Reset button on the bottom left is selected. A master select (above the individual address select boxes) will select/reselect all register selects simultaneously.

### Calculate Solution

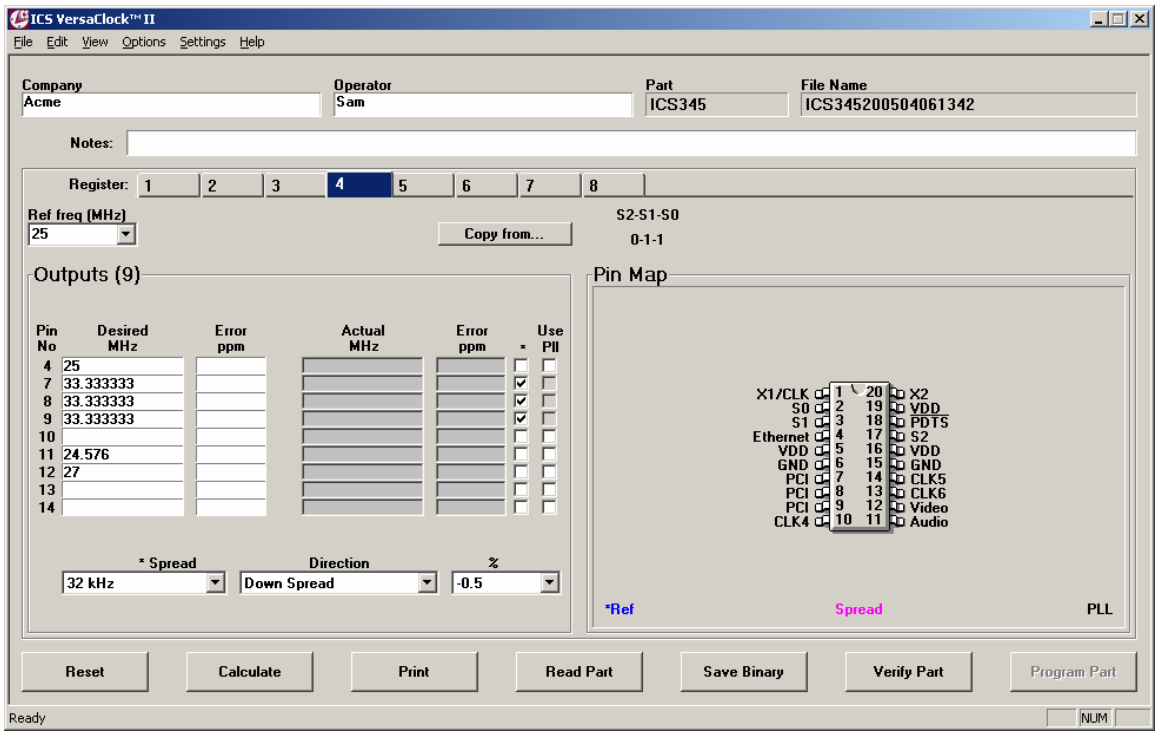
Pressing the Calculate button in the lower left corner will calculate all selected registers together, to insure proper pin alignment between registers. Whether using Manual Pin Assignment or not, the outputs in a given column will appear on the same output pin for the specified register address.

## *Single Register View*

As indicated above, it is possible to toggle between All Register View and Single Register View by selecting the appropriate option from the View menu. It does not matter whether registers have been calculated or uncalculated to switch views.

When switching to Single Register View, the highlighted or active register (address in blue above) will be the register that will be opened.

It is possible to go from any Attribute Tab into Single Register View.




Some things to note about Single Register View:

- Pin Labels set in All Register View are placed on the component pin diagram. Labels cannot be edited in this view mode.
- Manual Pin Select feature works in this view mode. Pin numbers are to the left of the input fields.
- Target outputs that require Spread Spectrum modulated outputs need to be checked beneath the (*****) field. The amount and direction of Spread Spectrum is configured for each address as a group.
- Register Tabs - Individual registers may be inspected and edited by selecting the Register Tabs across the top of the input field.
- Data is entered under the same principles as described above in the All Register View. The only difference is that all attributes for a given output are visible in the same row.
- Reset and Calculate buttons in the bottom left corner will clear and calculate only the register in view. Registers are calculated independently. Go to All Register View to configure an entire part.

For each register address, a solution must be calculated individually. Only the address register currently viewed will be calculated. (Note: If you change the Reference Frequency in one register, you must recalculate all registers for the new frequency input setting.)

### Copying Registers

The contents of a register may be copied to another register to maintain pin assignments between registers.

First, go to the target register into which you wish to copy.

Second, from the Options menu, select “Copy Register”. A window will open requesting that you select the register address from which menu you wish to copy. Select “OK” to enact the copy. (You can also use Options Copy or ALT-C to enact this function).

*[Tip: The addition of Spread Spectrum for a register automatically forces the entire solution to be recalculated. If the target device has registers with Spread Spectrum turned on and similar outputs with Spread Spectrum off, you MUST calculate a Spread Spectrum ON register first, to establish the initial pin assignment. You may start calculation on any register. It is not necessary to start with Register 1.]*

## 6) Solution Interpretation

### *Actual Frequency Output*

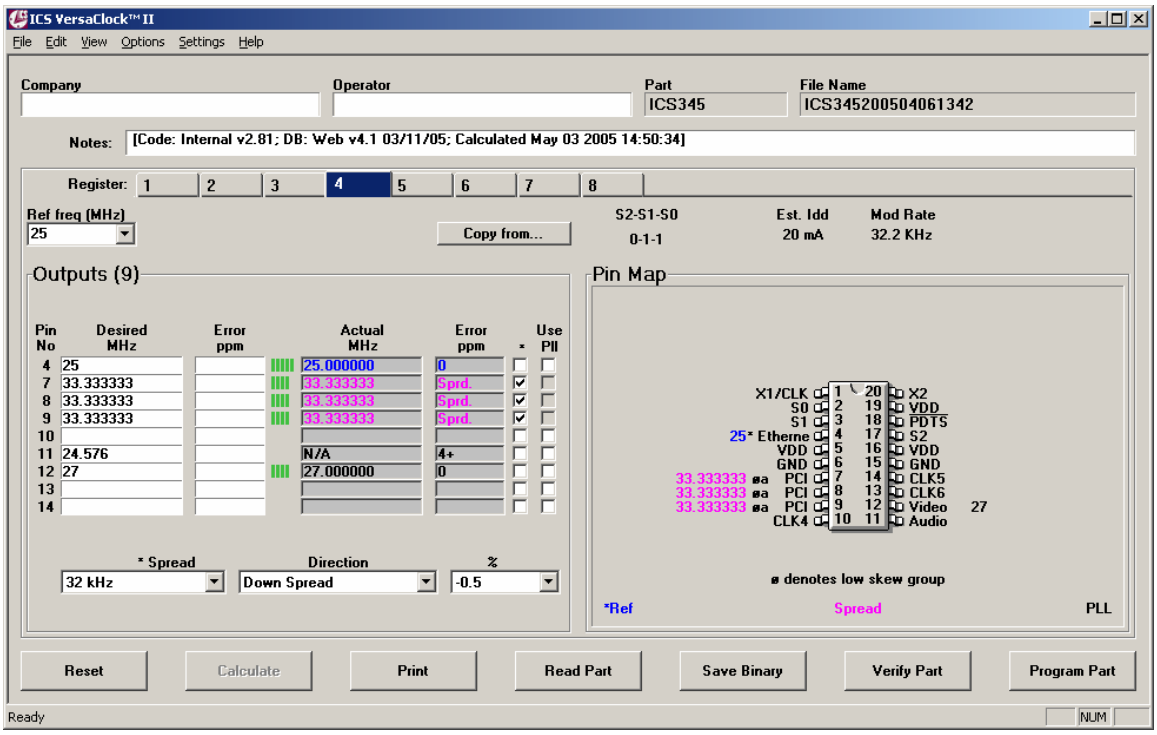
For both the Single Register and All Register Views, each target output, if a solution exists, will be displayed in a grayed box with the associated accuracy error. If Spread Spectrum is applied to an output, the accuracy will be noted as “Spread”. (Note: The minimum Spread value - 0.5% - is equivalent to 5000 ppm. The target center frequency of a Spread output will be within the stated desired accuracy.)

Solutions may not be available for a variety of reasons. Examples are: 1) no solution with equal or better accuracy to specified target frequency; 2) inadequate chip resources to support target frequency.

**[Tip: If no solution is found for a target output, try widening the allowable accuracy error until a solution is provided. If this does not provide a solution, check to see if the number of discrete output frequencies (excluding direct reference frequency outputs) is greater than the number of PLLs provided on the selected part.]**

(Note: For Output Clocks that are a buffer Reference Frequency output, the frequency on the Pin Map will be written in Blue and have an asterisk. For Output Clocks that have Spread Spectrum applied, the frequency will be written in Magenta. All non-spread, synthesized clock outputs will be written in black.)

Below is a typical calculated result for a Spread Spectrum capable part (ICS345) in Single Register View.

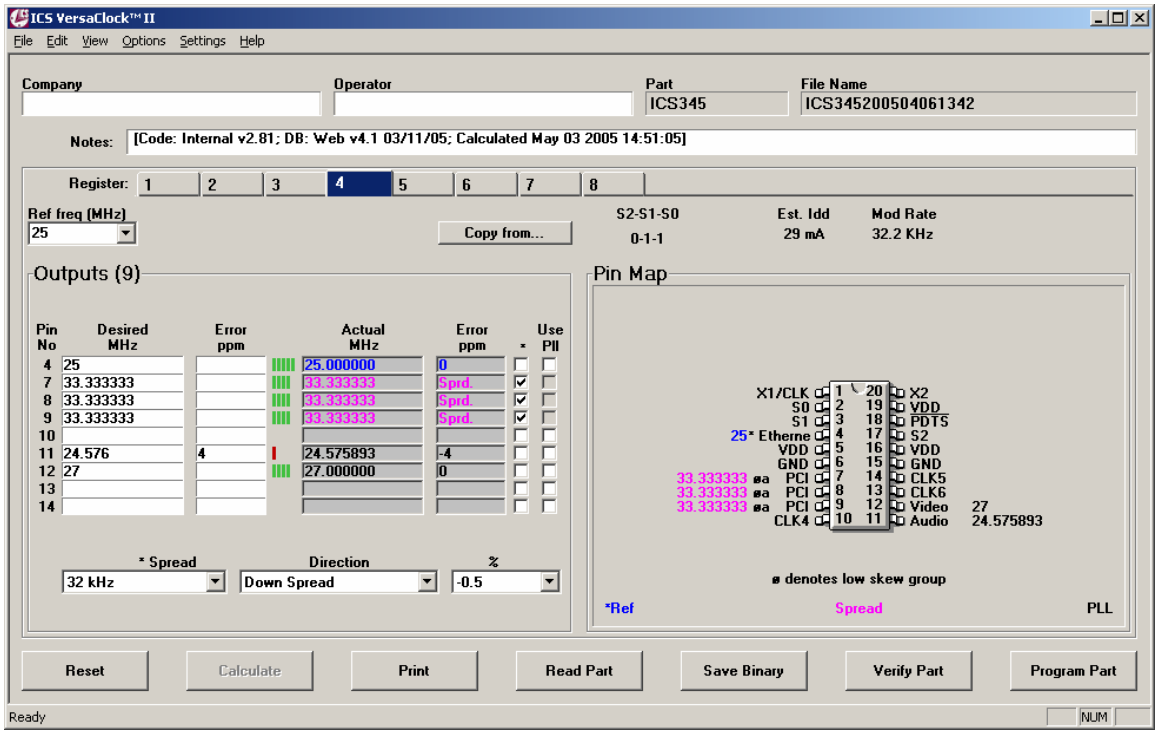



The calculator optimizes the target frequency outputs for a given input. Occasionally, the calculator is unable to find a solution within the specified tolerance. This may be due to:

- Greater ppm error than specified for target frequency. Error PPM will specify minimum accuracy needed to obtain a solution (i.e. 5+ indicates that the Target Error PPM must be >= 5). Change the Error PPM value and recalculate.
- No Available Resources. When more non-related output frequencies are specified than the individual part may support at the same time, the Error PPM will provide a N/A (not

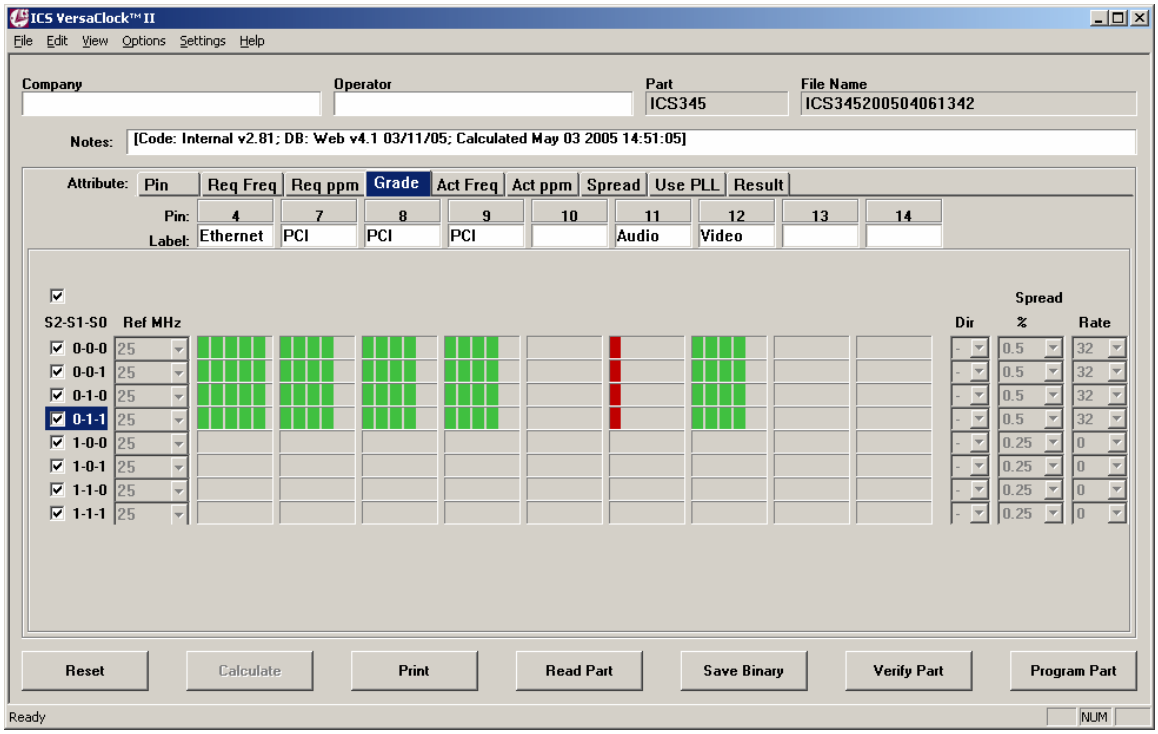
available) notation. This occurs when, for example, 5 unrelated frequencies are targeted for a 3 PLL device. The user must then prioritize which frequencies are most important and omit the remainders, or increase the target Error PPM or change the target frequency, in the hope of being able to create an integer divisor of one of the existing PLL frequencies.

In the example above, notice that the target output of 24.576 MHz did not have a 0 ppm synthesis solution. The nearest solution is 4 ppm away. A minimum of 4 ppm Error target must be inserted for the output to find a solution. Only outputs that previously had no solution will be calculated.




Recalculation, provided a solution with -4 ppm synthesis offset.

In All Register View Mode, the final calculated screen appears as:




### *Grade*

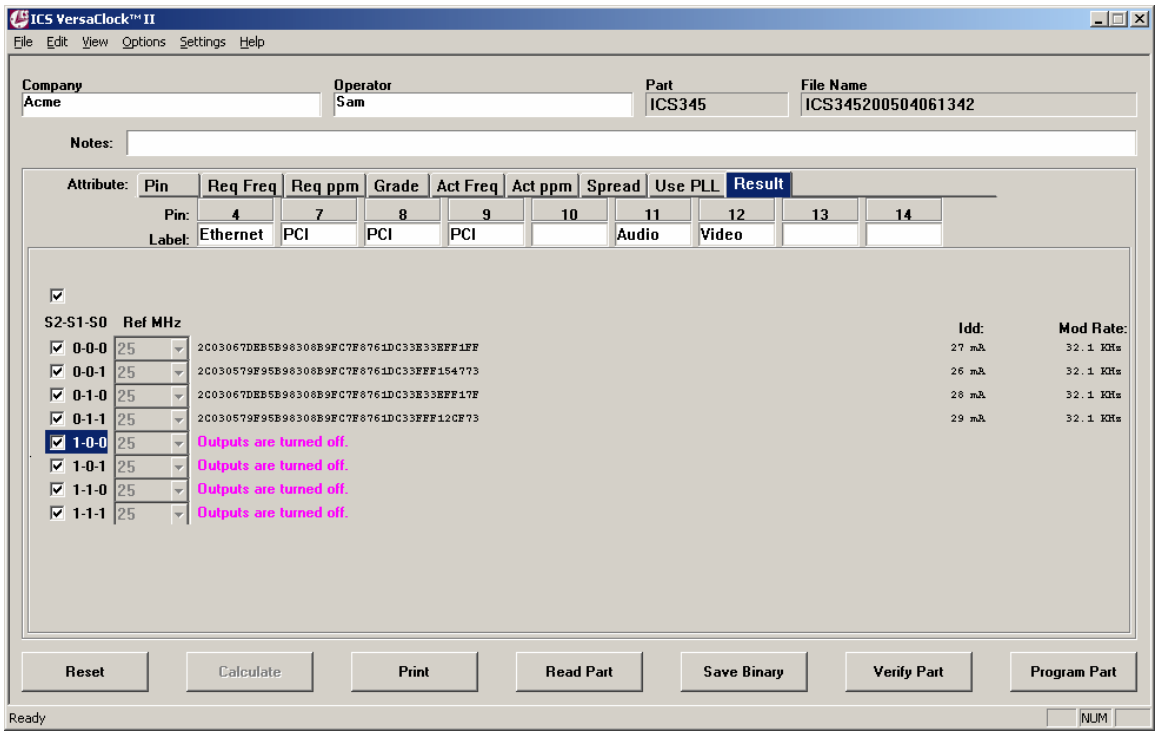
After calculating in All Register View Mode, the display automatically switches to the Grade attributes tab to show whether a solution was available.

Each frequency solution will be given a 1- to 5-bar "grade" of how well the output frequency jitter performance can be anticipated for the configuration. The bar grade provided is not an absolute value, rather a relative strength within the PLL's operating parameters.

- 1-Bar – indicates that the PLL will operate at minimum performance criteria
- 3-Bars – indicates the PLL operates within the mid-range of operating criteria. Clock output performance will be suitable for most applications
- 5-Bars – indicates that the PLL is maximized for all parameters. This is the best solution.

Tip: To increase the performance grade for a given clock output, increase the allowable Error PPM. By widening the accuracy requirement, more solutions will become available. Within each accuracy requirement, the best jitter performance will be selected for each individual clock output.

### *Results Tab*




a) Hexadecimal Output – Register configuration sequence Programming Word Display

The 160 bit programming word may be displayed as a 20-character hexadecimal character string.

b) Estimated Idd

For the individual register configuration – including reference input value and all outputs – the estimated Idd has been characterized to be within 20% of the actual value.

c) Spread Spectrum Modulation Rate

For outputs with Spread Spectrum selected, the modulation frequency will be displayed. Typically, the modulation rate will be in the 31-33 kHz range, but may be substantially higher (above 40 kHz) for output frequencies above 125 MHz.

Outputs Turned Off – For registers with no target outputs, calculating in All Register View mode will automatically turn off unused registers. Address assertions to these registers will have all PLLs and outputs turned off.

For Register View mode, each unused register must be individually calculated to turn off outputs and set PLLs off. If this is not done, then these registers will remain in an non-programmed state.

## *Single Register View Only*

### Solution Pin Map

Upon completion of solution calculation, a description of each device pin is provided. The pin map displays the actual frequencies corresponding to that register address.

Frequencies that are the buffered reference frequency will be displayed in **Blue**.

Frequencies that have Spread Spectrum applied are displayed on the pin map in **Magenta**.

### Low Skew Groups

Multiple copies of a frequency output may be generated using the same PLL and output divide circuitry. When this happens, the outputs are "low skew" and are in-phase to within the limits specified in the datasheet. Up to 4 low skew groups can exist simultaneously. Each group will have a letter designation, in conjunction with the symbol "phi" (ø) on the resulting pin map.

### Programming Word Display

The 160-bit programming word may be displayed as a 20-character hexadecimal character string. To display, select Options > Show Programming Word (ALT-W). The programming word will appear beneath the pin diagram. By selecting the option a second time, it will toggle the word display off.

## *Other VersaClock Features (available in both view modes)*

### Save Binary

This button allows conversion of the VersaClock™ II session file into an Intel compatible hexidecimal format for production programming. The default extension for this file is *.hex. This format is used by third party programmers.

### Verify Part

When connected to a VersaClock II programmer, selecting this button will read back the configuration of all registers of a programmed part and compare them to the hexadecimal value of the loaded file.

### Read Part

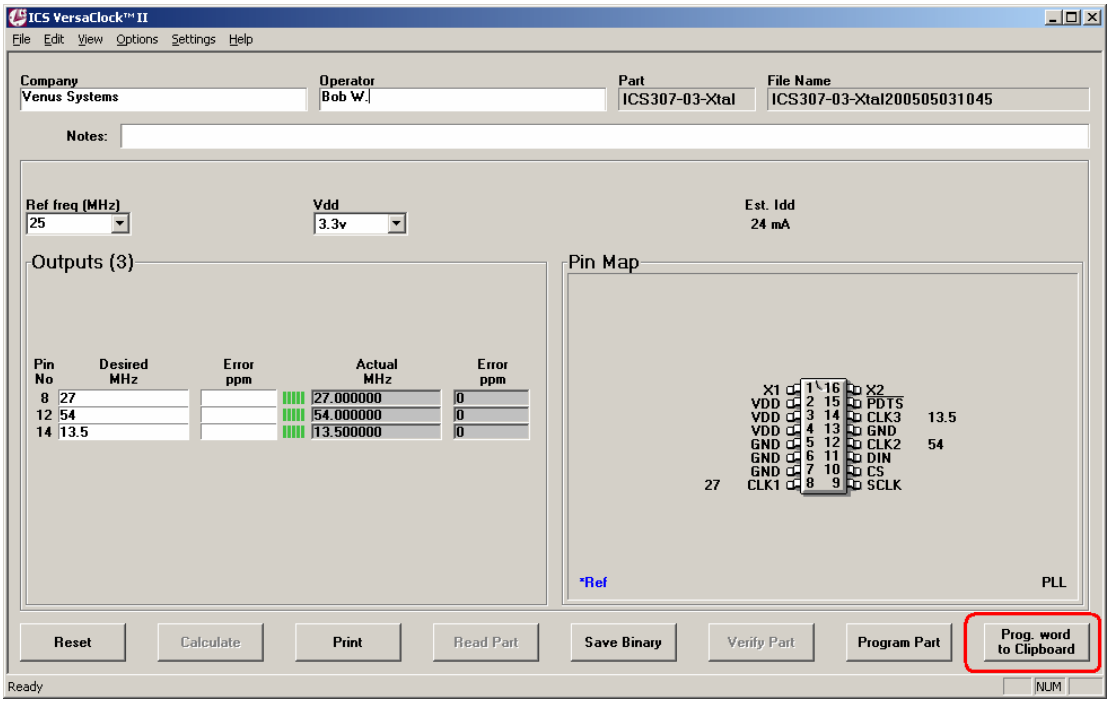
When connected to a VersaClock II programmer, selecting this button will allow the software to upload the contents of a known programmed part. This will allow the configuration of additional parts with the same code. Because there is no input reference frequency, the VersaClock software will not be able to provide information on the configuration of the part. You will need to contact ICS Marketing to get information about how the part was configured.

(Note: You must first select the proper new part from the parts selection menu - File > New.)

**Program Word to Clipboard** (Serial Programmable Devices Only)

To facilitate the implementation of serial programmable systems, users have an additional user feature on the bottom right corner of the window: “Program word to Clipboard”

By selecting this button, the configuration program word is made available for pasting into other documents or embedded development code.




**Program Part**

When connected directly to an ICS VersaClock II programmer – either by serial port or USB port connection – selecting this button will directly program the identified part. No exporting configuration files to another software applications is required.

If no programmer is available, or programmer socket is empty, selecting this button will return a message telling you that you need to take appropriate action before attempting to program a device.

## 7) Saving Solution

Multi-session programming (for direct use with ICS VersaClock™ II programmer)

Device configuration may be saved into a uniquely named file for multi-session development. With use, along with the ICS VersaClock programmer, the “Program Chip” button will directly program the configuration into the chip.

File Default Naming, File Default Annotation

All files default to a unique file name - the device number (I.e. ICS345) and the date code in the format YYYYMMDDHHMM. An example is ICS345200504061342 for a configuration first developed on 6 April 2005 at 1:42pm.

Annotations may be included in file, such as Company Name, Operator and other notes. Company Name and Operator used in a session will be the default of following session, as long as software is in use.

Returning to a saved solution

From Startup screen (see Image 1 on Page 4), select the Prior Session button to open a saved solution from a previous session. The saved solution will let the software know what part type was in use.

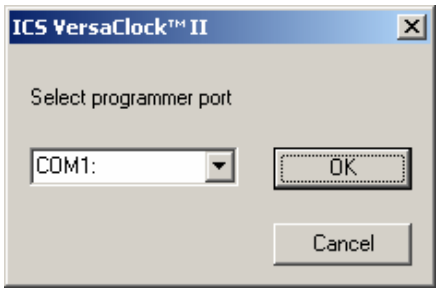
You may also return to a saved solution by selecting any part type from the Startup > Open screen, and selecting the desired file from the File Menu in the calculator workspace.

## 5) Programming a Device

### *First Time Setup*

If you have ICS VersaClock™ II hardware, you will need to set up the serial connection to directly program the clock circuit from the software. Determine which COM port you are using to connect the hardware. From any device work screen, select Settings > Select Port.

A pop-up window will appear for you to select the appropriate COM port from the pull down menu.




**Server**

The database server is set to default to ***search.icst.com***. No user information is shared with the server.

**Connecting the Programmer**

Connect the serial cable between the programmer and the selected serial port on your computer. When the power supply is attached to the programmer, a green LED will light in the upper right corner.

- The Serial Port (COM1) should be configured as follows:

| | |
|---|---|
| Bits per second: | 9600 |
| Data bits: | 8 |
| Parity: | None |
| Stop bits: | 1 |
| Flow control: | Xon/Xoff |

Insert the appropriate device daughter card (8-pin SOIC, 16-pin TSSOP, 20-pin TSSOP or 20-pin SSOP) into the programmer socket with the words “Pin 1” oriented in the Upper Left hand corner.

Insert an unprogrammed device with Pin 1 indentation aligned in the upper left.

**Programming the Device**

When the device configuration is completed and calculated for the desired registers, select the Program Chip button in the bottom right corner. A message will be displayed when the transmission is successfully completed.

(Note: The software will notify the user when the programmer is not connected to the port and when the power to the programmer is not on.)

**Device Program Verification**

Once the device has been programmed, verify that it has been programmed correctly. With the device in the socket, select the “Verify Chip” button in the lower right side of the VersaClock window. If the device is exactly the same code as exists in all available registers, then a positive confirmation will be returned. If any single bit is incorrect, in any of the registers, then a negative response will be displayed.

## 6) Help

A full copy of this user manual is available from Help menu. By selecting the User Manual, the user can toggle between the active VersaClock view (either Single Register or All Register View) and the user manual.

## 7) FAQ

**Does it matter which order the outputs are entered?**

No. The outputs are allocated independently of the order in which they are listed. Multiple copies of a desired output frequency do not have to be next to each other. If there are outputs that are unused, you may chose to insert additional copies of any of the output frequencies provided for that register address.

Spread Spectrum outputs are always allocated first, because only one of the PLLs has that capability. Always start calculation with a register that requires Spread Spectrum (if appropriate). It is then easier to maintain pin compatibility with other registers by modifying the spread percentage or turning off the feature.

**How many outputs can have Spread Spectrum?**

Spread Spectrum may be applied to some or all of the output frequencies. For example, if there are 9 copies of 14.31818MHz output requested, up to 9 copies of that output frequency can be selected.

Multiple frequencies derived from the same Spread Spectrum VCO frequency may also have Spread Spectrum modulation applied. Select the check buttons associated with the target Spread Spectrum frequencies. Multiple frequencies with simultaneous Spread Spectrum modulation will each have the same percentage and frequency modulation.

**Can I specify negative accuracy error only?**

Yes. By placing a negative ppm accuracy value in Error ppm column, only negative accuracy error solutions will be considered. If a positive ppm accuracy value is provided, both positive and negative accuracy solutions will be considered.

**What frequency does the Spread Spectrum modulate the output clock?**

The software targets either 32kHz or 120kHz modulation of the selected output clock(s). 32kHz was set in compliance with PCI standard Spread Spectrum modulation requirements. This frequency may increase slightly, especially when the output clock is greater than 125MHz. This is caused by the necessity of using a VCO frequency higher than 250MHz.

**Why do I sometimes get no available resources (N/A) instead of a solution for desired output frequencies?**

Each programmable device has a limited number of PLLs and output dividers to generate output target frequencies. In some cases, individual resources may be required by multiple target outputs, but only one may be serviced. The other output will have an N/A notation. An example of this would be 2 or more sub-1MHz outputs. In order to provide these frequencies, very large output dividers are required. Once the resource has been used, it cannot be simultaneously for another frequency.

Occasionally, you may be able to obtain a better solution by bringing the non-supported frequency to the top of the list. Although this does not guarantee a solution, it sometimes forces frequencies that take up limited resources in one solution to select a different configuration.

**What file formats do the VersaClock™ II software recognize?**

The VersaClock™ II software defaults a .TXT file format. When you save a file, no file extension is required, but a .TXT extension is recommended to allow you to open the file in a text editor to manually read the file. Using no file extension or .TXT works equally well with the software.

**Can I turn off all outputs on a register to make sure that I am in the lowest power mode possible?**

If you run calculate with no target outputs, you will receive a message “No target frequencies have been specified. Register will be programmed to “Off”. Proceed?” By selecting OK, a banner will be placed at the bottom of the device pin map that indicates all outputs are turned off.

**Can I change the background colors of VersaClock?**

The VersaClock II software determines it’s color scheme from the Windows Display Properties. It can be changed by moving the cursor over the Windows background, right-click and selecting the Appearances tab.