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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

SuperH™ Family E10A Emulator

Additional Document for User's Manual

SH7729R E10A HS7729RKCM02HE Renesas Microcomputer Development Environment System SuperH™ Family / SH7700 Series Specific Guide for the SH7729R E10A Emulator

Renesas Electronics
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Rev.1.0 2003.12

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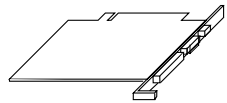
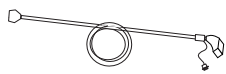
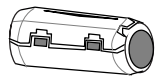
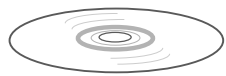
Contents

Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The SH7729R E10A emulator supports the SH7729R and SH7709S. Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator (HS7729RKCM01H, HS7729RKCM02H, HS7729RKCI01H, or HS7729RKCI02H)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Card emulator	 (PCMCIA) or  (PCI)	1	HS7729RKCM01H (PCMCIA: 14-pin type): Depth: 85.6 mm, Width: 54.0 mm, Height: 5.0 mm, Mass: 27.0 g HS7729RKCM02H (PCMCIA: 36-pin type): Depth: 85.6 mm, Width: 54.0 mm, Height: 5.0 mm, Mass: 28.0 g HS7729RKCI01H (PCI: 14-pin type): Depth: 144.0 mm, Width: 105.0 mm, Mass: 93.0 g HS7729RKCI02H (PCI: 36-pin type): Depth: 122.0 mm, Width: 96.0 mm, Mass: 90.0 g
	User system interface cable		1	HS7729RKCM01H (PCMCIA: 14-pin type): Length: 80 cm, Mass: 33.0 g HS7729RKCM02H (PCMCIA: 36-pin type): Length: 30 cm, Mass: 55.0 g HS7729RKCI01H (PCI: 14-pin type): Length: 150 cm, Mass: 86.0 g HS7729RKCI02H (PCI: 36-pin type): Length: 80 cm, Mass: 69.0 g
	Ferrite core (connected with the user interface cable)		1	Countermeasure for EMI* (only for HS7729RKCM02H and HS7729RKCI02H)
Soft-ware	SH7729R E10A emulator setup program, SuperH™ Family E10A Emulator User's Manual, and Specific Guide for the SH7729R E10A Emulator		1	HS7729RKCM01SR, HS0005KCM01HJ, HS0005KCM01HE, HS7729RKCM02HJ, and HS7729RKCM02HE (provided on a CD-R)

Note: The EMI is an abbreviation of the Electrical Magnetic Interference.

For EMI countermeasure, use the ferrite core by connecting the user interface cable.
When the user interface cable is connected with the emulator or user system, connect the ferrite core in the user system as shown in figure 1.1.

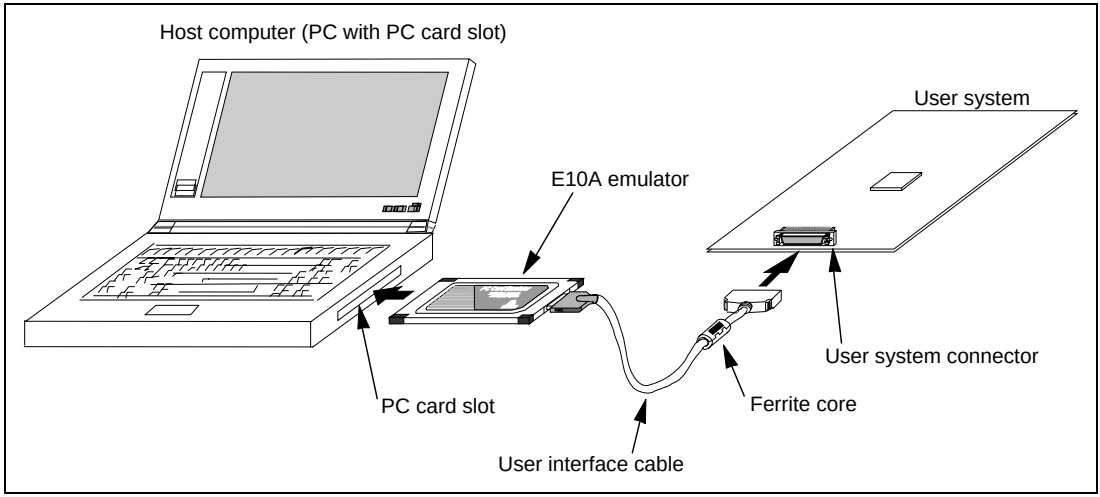


Figure 1.1 Connecting Ferrite Core

1.2 Connecting the E10A Emulator with the User System

To connect the E10A emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MCU. In addition, read the E10A emulator user's manual and hardware manual for the related device.

Table 1.2 shows the type number of the E10A emulator, the corresponding connector type, and the use of AUD function.

Table 1.2 Type Number, AUD Function, and Connector Type

Type Number	Connector	AUD Function
HS7729RKCM02H, HS7729RKCI02H	36-pin connector	Available
HS7729RKCM01H, HS7729RKCI01H	14-pin connector	Not available

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use them according to the purpose of the usage.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. For tracing, only the internal trace function is supported. Since the 14-pin type connector is smaller than the 36-pin type (1/2.5), the area where the connector is installed on the user system can be reduced.

1.3 Installing the H-UDI Port Connector on the User System

Table 1.3 shows the recommended H-UDI port connectors for the emulator.

Table 1.3 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type
14-pin connector	2514-6002	Minnesota Mining & Manufacturing Ltd.	14-pin straight type

Note: When the 36-pin connector is used, do not connect any components under the H-UDI connector. When the 14-pin connector is used, do not install any components within 3 mm of the H-UDI port connector.

1.4 Pin Assignments of the H-UDI Port Connector

Figures 1.2 and 1.3 show the pin assignments of the 36-pin and 14-pin H-UDI port connectors, respectively.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following pages differ from those of the connector manufacturer.

Pin No.	Signal	Input/ Output*1	SH7729R, SH7709S Pin No. FP-208	BP-240	Note	Pin No.	Signal	Input/ Output*1	SH7729R, SH7709S Pin No. FP-208	BP-240	Note
1	NC	——				19	TMS	Input	137	H16	
2	GND	——				20	GND	——			
3	AUDATA0	I/O	135	J18		21*2	/TRST	Input	136	J19	
4	GND	——				22	GND	——			
5	AUDATA1	I/O	133	K19		23	TDI	Input	138	H17	
6	GND	——				24	GND	——			
7	AUDATA2	I/O	131	K18		25	TDO	Output	120	N18	
8	GND	——				26	GND	——			
9	AUDATA3	I/O	130	L17		27*2	/ASEBRKAK	Output	128	L18	
10	GND	——				28	GND	——			
11*2	/AUDSYNC	Output	94	V14		29	NC	——			
12	GND	——				30	GND	——			
13	NC	——				31*2	/RESETP	Output	193	C7	
14	GND	——				32	GND	——			
15	NC	——				33*3	GND	Output			
16	GND	——				34	GND	——			
17	TCK	Input	139	H18		35	AUDCK	Input	151	D16	
18	GND	——				36	GND	——			

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.

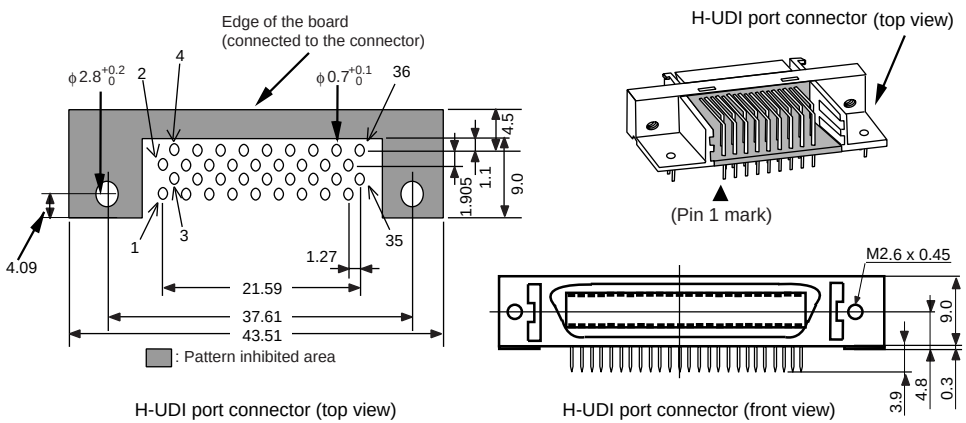


Figure 1.2 Pin Assignments of the H-UDI Port Connector (36 Pins)

Pin No.	Signal	Input/ Output*1	SH7729R, SH7709S Pin No. FP-208	BP-240	Note
1	TCK	Input	139	H18	
2*2	/TRST	Input	136	J19	
3	TDO	Output	120	N18	
4*2	/ASEBRKAK	Output	128	L18	
5	TMS	Input	137	H16	
6	TDI	Input	138	H17	
7*2	/RESETP	Output	193	C7	
11	Not connected	—	—	—	—
8 to 10 12 to 13	GND	—	—	—	—
14*3	GND	Output	—	—	—

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.

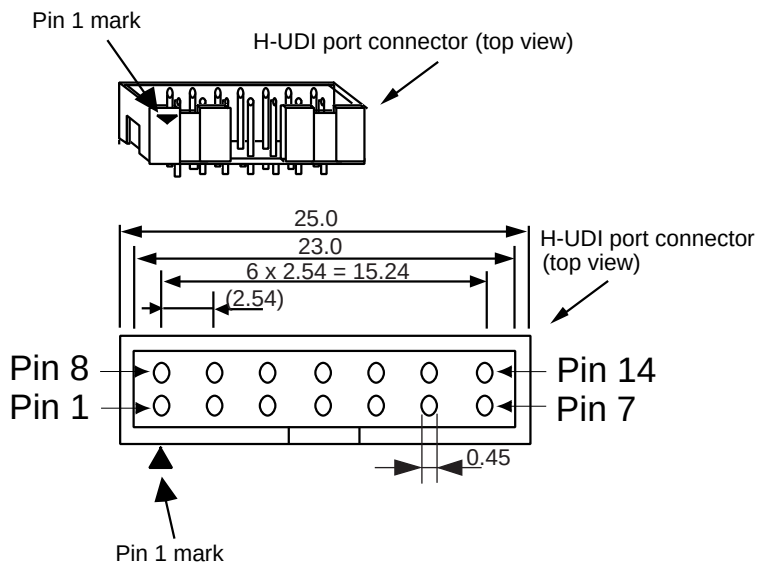


Figure 1.3 Pin Assignments of the H-UDI Port Connector (14 Pins)

1.5 Recommended Circuit between the H-UDI Port Connector and the MPU

1.5.1 Recommended Circuit (36-Pin Type)

Figure 1.4 shows a recommended circuit for connection between the H-UDI port connector (36 pins) and the MPU.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.

2. Note that the processing of the /ASEMD0 pin differs depending on whether the emulator is used or not. In addition, the /ASEMD0 pin must be switched on the board because it is not controlled by the emulator.
   (1) When the emulator is used: /ASEMD0 = low (ASE mode)
   (2) When the emulator is not used: /ASEMD0 = high (normal mode)
3. The reset signal in the user system is input to the /RESETP pin of the MCU. Connect this signal to the H-UDI port connector as the output from the user system.
4. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
5. The pattern between the H-UDI connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
6. The resistance values shown in figure 1.4 are recommended.
7. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related device.

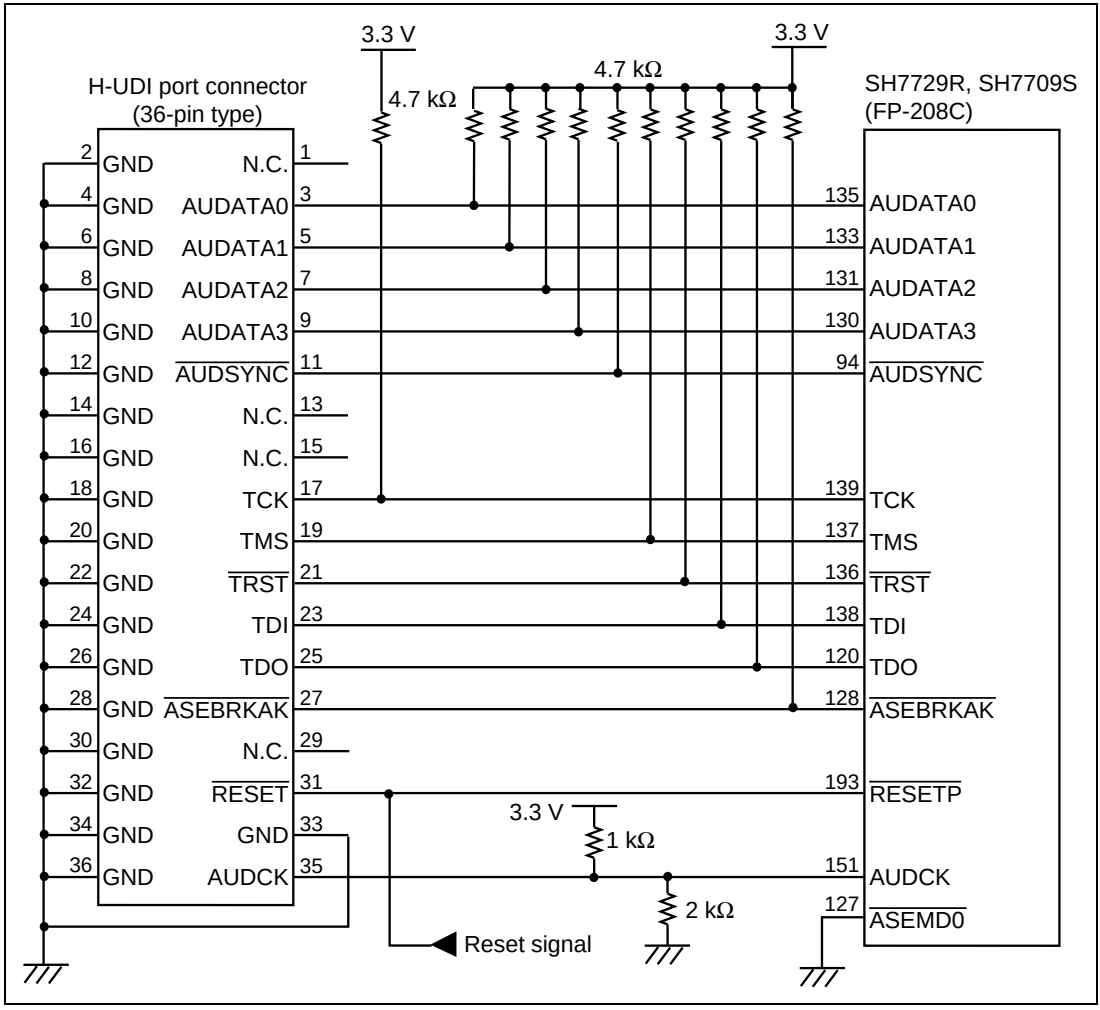


Figure 1.4 Recommended Circuit for Connection between the H-UDI Port Connector and MPU (36-Pin Type)

1.5.2 Recommended Circuit (14-Pin Type)

Figure 1.5 shows a recommended circuit for connection between the H-UDI port connector (14 pins) and the MPU.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.

2. Note that the processing of the /ASEMD0 pin differs depending on whether the emulator is used or not. In addition, the /ASEMD0 pin must be switched on the board because it is not controlled by the emulator.
   (1) When the emulator is used: /ASEMD0 = low (ASE mode)
   (2) When the emulator is not used: /ASEMD0 = high (normal mode)
3. The reset signal in the user system is input to the /RESETP pin of the MCU. Connect this signal to the H-UDI port connector as the output from the user system.
4. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
5. The pattern between the H-UDI connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
6. The resistance values shown in figure 1.5 are recommended.
7. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related device.

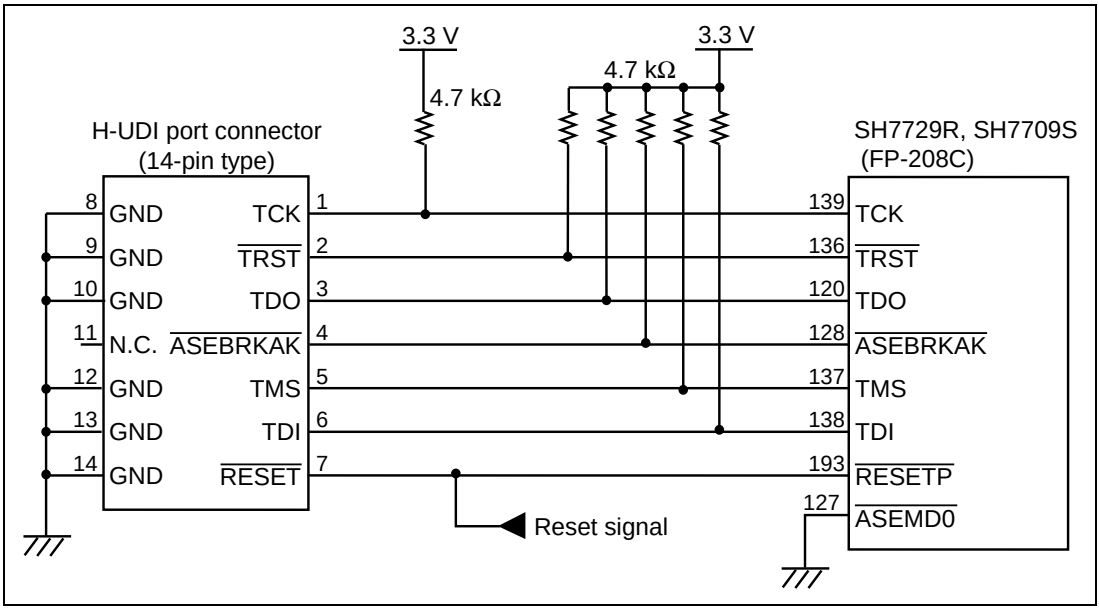


Figure 1.5 Recommended Circuit for Connection between the H-UDI Port Connector and MPU (14-Pin Type)

Section 2 Specifications of the SH7729R E10A Emulator's Software

2.1 Differences between the SH7729R, SH7709S, and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the actual SH7729R and SH7709S registers are undefined.

Table 2.1 Register Initial Values at Emulator Power-On

Register	Emulator at Power-on
R0 to R14	H'00000000
R15 (SP)	H'A0000000
R0_BANK to R7_BANK	H'00000000
PC	H'A0000000
SR	H'700000F0
GBR	H'00000000
VBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
SPC	H'00000000
SSR	H'000000F0
RS*	H'00000000
RE*	H'00000000
MOD*	H'00000000
A0G, A1G*	H'00
A0, A1*	H'00000000
X0, X1*	H'00000000
Y0, Y1*	H'00000000
M0, M1*	H'00000000
DSR*	H'00

Note: These registers are not displayed when the SH7709S is selected.

2. The emulator uses the H-UDI; do not access the H-UDI.

3. Low-Power States (Sleep, Software Standby, and Module Standby)

   For low-power consumption, the SH7729R and SH7709S have sleep, software standby, and module standby states.

   The sleep, software standby, and module standby states are switched using the SLEEP instruction. When the emulator is used, only the sleep state can be cleared with either the normal clearing function or with the [STOP] button, and a break will occur. Note that if a command has been entered in standby mode or module standby mode, no commands can be used from the emulator. The states cannot be canceled by the [STOP] button.

Notes: 1. The memory must not be accessed or modified in sleep mode.

2. When the [STOP] button is clicked in sleep mode, a break does not occur immediately after executing the SLEEP instruction. The number of instructions to be proceeded differs according to the emulator environment or operating frequency of the chip. It is about 500 instructions when the Pentium® III 800-MHz PC is used and the operating frequency is 25 MHz.
3. When the UBC is set to be used, do not set the UBC to the standby mode.
4. When the SLEEP instruction is executed by STEP-type commands to switch the mode to sleep, the emulator does not enter sleep mode, and execution skips to the next instruction. Do not execute the SLEEP instruction to switch the mode to standby because a TIMEOUT error will occur.

4. Reset Signals (/RESETP and /RESETM)

   The SH7729R and SH7709S reset signals (/RESETP and /RESETM) are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the SH7729R or SH7709S.

Note: Do not break the user program when the /RESETP, /RESETM, /BREQ, and /WAIT signals are being low. A TIMEOUT error will occur. If the /BREQ or /WAIT signal is fixed to low during break, a TIMEOUT error will occur at memory access.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   When a memory is accessed from the memory window, etc. during user program execution, the user program is resumed after it has stopped in the E10A emulator to access the memory. Therefore, realtime emulation cannot be performed.

   The stopping time of the user program is as follows:

   Environment:

   Host computer: 800 MHz (Pentium® III)
   Operating system: Windows® 2000
   SH7729R: 50 MHz (CPU clock)
   JTAG clock: 15 MHz

When a one-byte memory is read from the command-line window, the stopping time will be about 35 ms.

7. Memory Access during User Program Break

   The emulator can download the program for the flash memory area (refer to section 6.22, Download Function to the Flash Memory Area, in the Debugger Part of the SuperH™ Family E10A Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area. When the memory area can be written by the MMU, do not perform memory write, BREAKPOINT, or downloading.

8. Cache Operation during User Program Break

   When cache is enabled, the emulator accesses the memory by the following methods:

   - At memory write: Writes through the cache, then writes to the memory.
   - At memory read: Does not change the cache write mode that has been set.

   Therefore, when memory read or write is performed during user program break, the cache state will be changed.

9. Ports E, F, G, and H

   The AUD and H-UDI pins are multiplexed as shown in table 2.2.

Table 2.2 Multiplexed Functions

Port	Function 1	Function 2
E	PTE0 input/output (port)	TDO (H-UDI)
E	PTE7 input/output (port)*	/AUDSYNC output
F	PTF7 input (port) / PINT15 input (INTC)	/TRST (AUD and H-UDI)
F	PTF6 input (port) / PINT14 input (INTC)	TMS (H-UDI)
F	PTF5 input (port) / PINT13 input (INTC)	TDI (H-UDI)
F	PTF4 input (port) / PINT12 input (INTC)	TCK (H-UDI)
G	PTG6 input (port)	/ASEMD0 (AUD and H-UDI)
G	PTG5 input (port)	/ASEBRKAK (H-UDI)
G	PTG3 input (port)*	AUDATA3 (AUD)
G	PTG2 input (port)*	AUDATA2 (AUD)
G	PTG1 input (port)*	AUDATA1 (AUD)
G	PTG0 input (port)*	AUDATA0 (AUD)
H	PTH6 input (port)*	AUDCK (AUD)

Note: Note that function 1 cannot be used when the emulator is used. Function 1 can be used when the AUD pins are not connected to the emulator.

10. UBC

    When [User] is specified in the [UBC mode] list box in the [Configuration] dialog box, the UBC can be used in the user program.
    Do not use the UBC in the user program as it is used by the E10A emulator when [EML] is specified in the [UBC mode] list box in the [Configuration] dialog box.

11. MFI Boot Mode

    When the MFI boot mode is used, be sure to allocate the boot program from the top of MFRAM.

12. Memory Access during Break

    In the enabled MMU, when a memory is accessed and a TLB error occurs during break, it can be selected whether the TLB exception is controlled or the program jumps to the user exception handler in [TLB Mode] in the [Configuration] dialog box. When [TLB miss exception is enable] is selected, a Communication Timeout error will occur if the TLB exception handler does not operate correctly. When [TLB miss exception is disable] is selected, the program does not jump to the TLB exception handler even if a TLB exception occurs. Therefore, if the TLB exception handler does not operate correctly, a Communication Timeout error will not occur but the memory contents may not be correctly displayed.

13. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be as follows:

    - When HS7729RKCI01H or HS7729RKCI02H is used: TCK = 4.125 MHz
    - When HS7729RKCM01H or HS7729RKCM02H is used: TCK = 3.75 MHz

14. [IO] window

    - Display and modification

      Do not change values of the User Break Controller because it is used by the emulator.

      For each watchdog timer register, there are two registers to be separately used for write and read operations.

Table 2.3 Watchdog Timer Register

Register Name	Usage	Register
WTCSR(W)	Write	Watchdog timer control/status register
WTCNT(W)	Write	Watchdog timer counter
WTCSR(R)	Read	Watchdog timer control/status register
WTCNT(R)	Read	Watchdog timer counter

- The watchdog timer operates only when the user program is executed. Do not change the value of the frequency change register in the [IO] window or [Memory] window.

- The internal I/O registers can be accessed from the [IO] window. However, note the following when accessing the SDMR register of the bus-state controller. Before accessing the SDMR register, specify addresses to be accessed in the I/O-register definition file (SH7729R.IO) and then activate the HEW. After the I/O-register definition file is created, the MPU's specification may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register definition file can be customized depending on its format. Note that, however, the E10A emulator does not support the bit-field function.
- Verify

  In the [IO] window, the verify function of the input value is disabled.

15. Illegal Instructions

    If illegal instructions are executed by STEP-type commands, the emulator cannot go to the next program counter.

16. Interrupt

    When the BLMSK bit in the ICR1 register is 1, the NMI interrupt is accepted during break and the program is executed from the NMI interrupt vector. If the program cannot return normally from the NMI interrupt routine or the value in the general-purpose register is not guaranteed, a communication timeout error will occur.

2.2 Specific Functions for the SH7729R E10A Emulator

The SH7729R E10A emulator does not support the following function:

- Profiler function

2.2.1 Emulator Driver Selection

Table 2.4 shows drivers which are selected in the [E10A Driver Details] dialog box.

Table 2.4 Type Number and Driver

Type Number	Driver
HS7729RKCM01H	E10A PC Card Driver 3
HS7729RKCM02H	E10A PC Card Driver 2
HS7729RKCI01H	E10A PCI Card Driver 3
HS7729RKCI02H	E10A PCI Card Driver 2

2.2.2 Break Condition Functions

In addition to BREAKPOINT functions, the emulator has Break Condition functions. Three types of conditions can be set under Break Condition 1, 2, 3. Table 2.5 lists these conditions of Break Condition.

Table 2.5 Types of Break Conditions

Break Condition Type	Description
Address bus condition (Address)	Breaks when the SH7729R or SH7709S address bus value or the program counter value matches the specified value.
Data bus condition (Data)	Breaks when the SH7729R or SH7709S data bus value matches the specified value. Byte, word, longword, X bus, or Y bus can be specified as the access data size.
X-bus or Y-bus condition (Address and data)	Breaks when the X-bus or Y-bus address bus or data bus matches the specified value.
ASID condition (ASID)	Breaks when the SH7729R or SH7709S ASID value matches the specified condition.*
Bus state condition (Bus State)	There are two bus state condition settings: Read/Write condition: Breaks when the SH7729R or SH7709S RD or RDWR signal level matches the specified condition. Bus state condition: Breaks when the operating state in an SH7729R or SH7709S bus cycle matches the specified condition.
Internal I/O break condition	Breaks when the SH7729R accesses the internal I/O.
LDTLB instruction break condition	Breaks when the SH7729R executes the LDTLB instruction.
Count	Breaks when the conditions set are satisfied the specified number of times.

Note: When the SH7709S is selected, the data size for the X-bus or Y-bus access and X-bus or Y-bus condition (address and data) cannot be specified.

Table 2.6 lists the combinations of conditions that can be set under Break Condition 1, 2, 3.

Table 2.6 Dialog Boxes for Setting Break Conditions

	Type						
Dialog Box	**Address Bus Condition (Address)**	**Data Bus Condition (Data)**	**ASID Condition (ASID)**	**Bus State Condition (Bus Status)**	**Count Condition (Count)**	**Internal I/O Break**	**LDTLB Instruction Break**
[Break Condition 1] dialog box	O	O	O	O	O	X	X
[Break Condition 2] dialog box	O	X	O	O	X	X	X
[Break Condition 3] dialog box	X	X	X	X	X	O	O

Note: O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2.2.3 Trace Functions

Table 2.7 shows the trace functions.

Table 2.7 Trace Functions

Function		Description
Internal trace		Branch instruction trace functions which are built into the chip. This function displays the branch source and branch destination addresses and enables a realtime trace.
AUD trace*	Realtime trace	This function is operational when the AUD pin is connected to the emulator. This function displays the branch source and branch destination addresses, and instruction words at the branch destination. When the next branch occurs while the trace information is being output, the information is stopped and the next trace information is output. The user program can be executed in realtime, but some trace information will not be output. • Trace continue mode: When the trace buffer becomes full, this function always overwrites the oldest trace information to acquire the latest trace information. • Trace stop mode: After the trace buffer becomes full, the trace information is not acquired. (The user program is continuously executed.)
	Non realtime trace	This function is operational when the AUD pin is connected to the emulator. This function displays the branch source and branch destination addresses, and instruction words at the branch destination. When the next branch occurs while the trace information is being output, the CPU stops operations until the information is output. The user program is not executed in realtime. • Trace continue mode: When the trace buffer becomes full, this function always overwrites the oldest trace information to acquire the latest trace information. • Trace stop mode: After the trace buffer becomes full, the trace information is not acquired. (The user program is continuously executed.)

Note: When HS7729RKCM01H and HS7729RKCI01H are used, the AUD function cannot be used.

Table 2.8 Type Name and AUD Function

Type Name	AUD Function
HS7729RKCM01H	Not available
HS7729RKCM02H	Available
HS7729RKCI01H	Not available
HS7729RKCI02H	Available

Notes: 1. In the internal trace of the SH7729R and SH7709S, trace acquisition of the eight latest branch instructions is enabled. In addition, when the user program execution starts, the following one-branch trace is displayed:

Branch source address: Previous user program execution end address

Branch destination address: User program execution start address

2. In the internal trace of the SH7729R and SH7709S, the upper 4-bit address values are not acquired by trace. When the MMU is used, do not use the internal trace. Since the internal trace acquires only lower 28 bits, a TLB error may occur when the instruction code is displayed. When the emulator supports the AUD trace function, it is recommended to use the AUD trace.
3. The AUD trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previous branch source address is the same as the upper 16 bits, the lower 17 bits are output. If it matches the upper 24 bits, the lower 9 bits are output. If it matches the upper 28 bits, the lower 5 bits are output.
   The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.
4. In realtime trace, when the cache is on, the CPU clock is 33 MHz, and the AUD clock is 30 MHz, trace information will be lost under the following condition:
   Continuous nine NOP instructions and the non-limited loop of the BRA instruction at the 10th instruction
5. When the AUD trace function is used, the AUD clock (AUDCK) in the PCMCIA and PCI cards does not operate correctly at 50 MHz or higher.
6. In the SH7729R E10A emulator, the maximum number of trace display pointers is as follows:
   When HS7729RKCM02H is used: 13106 (6553 branches)
   When HS7729RKCI02H is used: 52428 (26214 branches)

2.2.4 Notes on Using the JTAG Clock (TCK) and AUD Clock (AUDCK)

1. When JTAG clock (TCK) is used, set the JTAG clock (TCK) frequency to lower than the frequency of half of the CPU clock.
2. Set the AUD clock (AUDCK) frequency to 50 MHz or below for PCMCIA and PCI cards. The upper limit of the AUD clock must be lower than the CPU clock and the lower limit must be the quarter of the CPU clock.

2.2.5 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. Accordingly, it can be set only to the internal RAM area. However, a BREAKPOINT cannot be set to the following addresses:
   - An area other than CS0 to CS6 and the internal RAM
   - An instruction in which Break Condition 2 is satisfied
   - A slot instruction of a delayed branch instruction
   - An area that can be only read by MMU
3. During step execution, a BREAKPOINT is disabled.
4. Conditions set at Break Condition 2 are disabled when an instruction to which a BREAKPOINT has been set is executed. Do not set a BREAKPOINT to an instruction in which Break Condition 2 is satisfied.
5. When execution resumes from the address where a BREAKPOINT is specified, single-step execution is performed at the address before execution resumes. Therefore, realtime operation cannot be performed.
6. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
7. When a BREAKPOINT is set to the cacheable area, the cache block containing the BREAKPOINT address is filled immediately before and after user program execution.
8. Note on DSP repeat loop:
   A BREAKPOINT is equal to a branch instruction. In some DSP repeat loops, branch instructions cannot be set. For these cases, do not set BREAKPOINTs. Refer to the hardware manual for details.
9. When the [Normal] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address or a virtual address according to the SH7729R or SH7709S MMU status during command input when the VPMAP_SET command setting is disabled. The ASID value of the SH7729R or SH7709S PTEH register during command input is used. When VPMAP_SET command setting is enabled, a BREAKPOINT is set to a physical address into which address translation is made

according to the VP_MAP table. However, for addresses out of the range of the VP_MAP table, the address to which a BREAKPOINT is set depends on the SH7729R or SH7709S MMU status during command input. Even when the VP_MAP table is modified after BREAKPOINT setting, the address translated when the BREAKPOINT is set valid.

10. When the [Physical] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address. A BREAKPOINT is set after disabling the SH7729R or SH7709S MMU upon program execution. After setting, the MMU is returned to the original state. When a break occurs at the corresponding virtual address, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
11. When the [Virtual] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a virtual address. A BREAKPOINT is set after enabling the SH7729R or SH7709S MMU upon program execution. After setting, the MMU is returned to the original state. When an ASID value is specified, the BREAKPOINT is set to the virtual address corresponding to the ASID value. The emulator sets the BREAKPOINT after rewriting the ASID value to the specified value, and returns the ASID value to its original value after setting. When no ASID value is specified, the BREAKPOINT is set to a virtual address corresponding to the ASID value at command input.
12. An address (physical address) to which a BREAKPOINT is set is determined when the BREAKPOINT is set. Accordingly, even if the VP_MAP table is modified after BREAKPOINT setting, the BREAKPOINT address remains unchanged. When a BREAKPOINT is satisfied with the modified address in the VP_MAP table, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
13. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Editor] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the break condition, the mark ● disappears.

2.2.6 Notes on Setting the [Break Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Break Condition 2 are disabled.
2. Break Condition 2 is disabled when an instruction to which a BREAKPOINT has been set is executed. Accordingly, do not set a BREAKPOINT to an instruction which satisfies Break Condition 2.
3. When a Break Condition is satisfied, emulation may stop after two or more instructions have been executed.

4. If a PC break address condition is set to the slot instruction after a delayed branch instruction, user program execution cannot be terminated before the slot instruction execution; execution stops before the branch destination instruction.
5. A break will not occur with the execution counts specified on the execution of the multi-step instruction.

2.2.7 Note on Setting the UBC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [UBC mode] list box has been set, the STEP-type commands that use Break Condition 2 for implementation cannot be used.

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