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Renesas Electronics Corporation

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User's Manual

SH-4A, SH4AL-DSP E200F Emulator

Additional Document for User's Manual Supplementary Information on Using the SH7354

Renesas Microcomputer Development Environment System

SuperH™ Family / SH7354 Series

E200F for SH7354 R0E873540EMU00E

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Contents

Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The E200F emulator supports the SH7354. Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

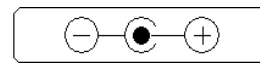
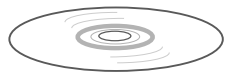
Classification	Component	Appearance	Quantity	Remarks
Hardware	Emulator main unit		1	R0E0200F0EMU00: Depth: 185.0 mm, Width: 130.0 mm, Height: 45.0 mm, Mass: 321.0 g
	AC adapter (serial numbers: 0081 or before)		1	Input: 100 to 240 V Output: 12 V 4.0 A Depth: 120.0 mm, Width: 72.0 mm, Height: 27.0 mm, Mass: 400.0 g 
	AC adapter (serial numbers: 0082 or after)		1	Input: 100 to 240 V Output: 12 V 3.0 A Depth: 99.0 mm, Width: 62.0 mm, Height: 26.0 mm, Mass: 270.0 g 
	AC cable		1	Length: 200 mm
	USB cable		1	Length: 1500 mm, Mass: 50.6 g

Table 1.1 Components of the Emulator (cont)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware (cont)	External probe (serial numbers: 0081 or before)		1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
	External probe (serial numbers: 0082 or after)		1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
Soft-ware	E200F emulator setup program,		1	R0E0200F0EMU00S,
	SH-4A, SH4AL-DSP E200F Emulator User's Manual,			R0E0200F0EMU00J, R0E0200F0EMU00E,
	Supplementary Information on Using the SH7354*			R0E873540EMU00J, R0E873540EMU00E (provided on a CD-R)

Note: Additional document for the MPUs supported by the emulator is included. Check the target MPU and refer to its additional document.

1.2 Connecting the Emulator with the User System

To connect the E200F emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MPU.

It is impossible to connect the emulator to the 14-pin type connector that is recommended for the E10A-USB emulator. The 36-pin type connector is the same as that of the E10A-USB emulator. When designing the user system, read the E200F emulator user's manual and hardware manual for the related device.

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use them according to the purpose of the usage.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. This connector type is not available for the E200F emulator; the E10A-USB emulator is available.

1.3 Installing the H-UDI Port Connector on the User System

Table 1.2 shows the recommended H-UDI port connectors for the emulator.

Table 1.2 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type

Note: When designing the 36-pin connector layout on the user board, do not place any other signals under the H-UDI connector to reduce cross-talk noises, etc.

1.4 Pin Assignments of the H-UDI Port Connector

Figure 1.1 shows the pin assignments of the 36-pin H-UDI port connector.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following page differs from those of the connector manufacturer.

Pin No.	Signal	Input/ Output *1	SH7354 Pin No.	Note	Pin No.	Signal	Input/ Output *1	SH7354 Pin No.	Note
1	AUDCK	Output	W5		19	TMS	Input	U4	
2	GND	——			20	GND	——		
3	AUDATA0	Output	W4		21	/TRST *2	Input	T5	
4	GND	——			22	(GND) *4	——		
5	AUDATA1	Output	V5		23	TDI	Input	W3	
6	GND	——			24	GND	——		
7	AUDATA2	Output	U5		25	TDO	Output	V4	
8	GND	——			26	GND	——		
9	AUDATA3	Output	U6		27	/ASEBRK / *2 BRKACK	Input/ output	W6	
10	GND	——			28	GND	——		
11	/AUDSYNC *2	Output	V6		29	UVCC	Output		
12	GND	——			30	GND	——		
13	N.C.	——			31	/RESETP *2 /RESETA	Output Output	T3 P4	User reset *5
14	GND	——			32	GND	——		
15	N.C.	——			33	GND *3	Output		
16	GND	——			34	GND	——		
17	TCK	Input	V3		35	N.C.	——		
18	GND	——			36	GND	——		

Notes: 1. Input to or output from the user system.
2. The symbol (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. When the user system interface cable is connected to this pin and the MPMD pin is set to 0, do not connect to GND but to the MPMD pin directly.
5. Connect /RESETP and /RESETA to the user system if required, as shown in figure 1.2.

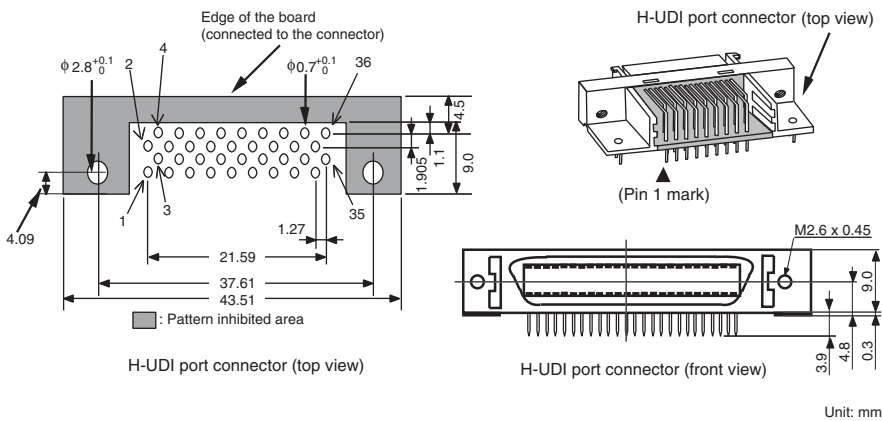


Figure 1.1 Pin Assignments of the H-UDI Port Connector (36 Pins)

1.5 Recommended Circuit between the H-UDI Port Connector and the MPU

1.5.1 Recommended Circuit (36-Pin Type)

Figure 1.2 shows a recommended circuit for connection between the H-UDI and AUD port connectors (36 pins) and the MPU when the emulator is in use.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.

2. The MPMD pin must be 0 when the emulator is connected and 1 when the emulator is not connected, respectively.
   (1) When the emulator is used: MPMD = 0
   (2) When the emulator is not used: MPMD = 1
   Figure 1.2 shows an examples of circuits that allow the MPMD pin to be GND (0) whenever the emulator is connected by using the user system interface cable.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The /TRST pin must be at the low level for a certain period when the power is supplied whether the H-UDI is used or not. Reduce the power supplied to the /TRST pin by pulling the pin down by a resistance of 1 kilo-ohm and setting PUL10 = 0 in the PULCR register after a reset.
5. The pattern between the H-UDI port connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
6. Since the H-UDI and the AUD of the MPU operate with the VccQ, supply only the VccQ to the UVCC pin.
7. The resistance values shown in figure 1.2 are for reference.
8. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MPU.
9. For the AUDCK pin, guard the pattern between the H-UDI port connector and the MPU at GND level.

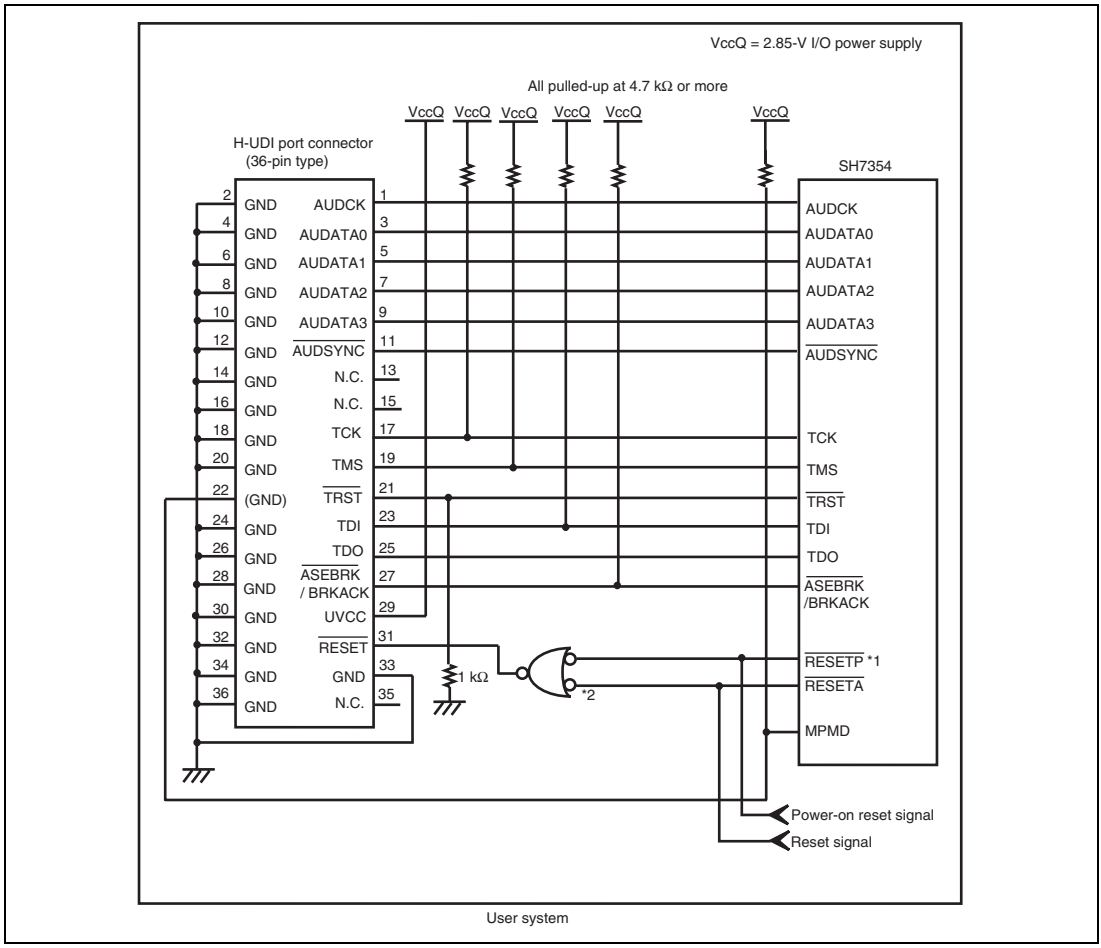


Figure 1.2 Recommended Circuit for Connection between the H-UDI Port Connector and MPU when the Emulator is in Use (36-Pin Type)

Notes: 1. Do not use /RESETP in the emulator after the user system has been activated. When reset signals are used for debugging, use /RESETA.

2. Fix /RESETA as high level when it is not used.

Section 2 Software Specifications when Using the SH7354

2.1 Differences between the SH7354 and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the actual SH7354 registers are undefined. When the emulator is initiated from the workspace, a value to be entered is saved in a session.

Table 2.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	H'A0000000
R0_BANK to R7_BANK	H'00000000
PC	H'A0000000
SR	H'700000F0
GBR	H'00000000
VBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
SPC	H'00000000
SSR	H'000000F0
RS	H'00000000
RE	H'00000000
MOD	H'00000000
A0G, A1G	H'00000000
A0, A1	H'00000000
X0, X1	H'00000000
Y0, Y1	H'00000000
M0, M1	H'00000000
DSR	H'00000000

2. The emulator uses the H-UDI; do not access the H-UDI.

3. Low-Power States (Sleep, Software Standby, Module Standby, U Standby, and R Standby)

   For low-power consumption, the SH7354 has sleep, software standby, module standby, U standby, and R standby states.

   The sleep and software standby states are switched using the SLEEP instruction. When the emulator is used, the sleep state can be cleared with either the normal clearing function or with the [STOP] button, and a break will occur.

   The power for some areas is turned off in U standby or R standby state and turned on in using the emulator.

Note: The memory must not be accessed or modified in sleep state.

4. Reset Signals (/RESETA)

   The SH7354 reset signal is only valid during emulation started with clicking the GO or STEP-type button. If the reset signal is input during execution of the user program, the program may generate a break; the break source will be displayed as 'PIN BREAK'.

   If the reset signal is enabled on the user system in command input wait state, it is not sent to the SH7354.

Note: Do not break the user program when the /RESETA signal is being low and the wait control signal is being active. A TIMEOUT error will occur. If the wait control signal becomes active during break, a TIMEOUT error will occur at memory access.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   When a memory is accessed from the memory window, etc. during user program execution, the user program is resumed after it has stopped in the emulator to access the memory. Therefore, realtime emulation cannot be performed.

   The stopping time of the user program is as follows:

   Environment:

   Host computer: 800 MHz (Pentium® III)
   JTAG clock: 30 MHz

   When a one-byte memory is read from the command-line window, the stopping time will be about 45 ms.

7. Memory Access during User Program Break

   The emulator can download the program for the flash memory area (for details, refer to section 6.22, Download Function to the Flash Memory Area, in the SH-4A, SH4AL-DSP E200F Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area.

8. Cache Operation during User Program Break

   When cache is enabled, the emulator accesses the memory by the following methods:

   - At memory write: Writes through the cache, then issues a single write to outside. The LRU is not updated.
   - At memory read: Reads memory from the cache. The LRU is not updated.

   Therefore, when memory read or write is performed during user program break, the cache state does not change.

   - At breakpoint set: Disables the instruction cache.

9. Port G

   The AUD pin is multiplexed as shown in table 2.2.

Table 2.2 Multiplexed Functions

Port	Function 1	Function 2
G	PTG4 input/output (port)*	/AUDSYNC (AUD)
G	PTG3 input/output (port)*	AUDATA3 (AUD)
G	PTG2 input/output (port)*	AUDATA2 (AUD)
G	PTG1 input/output (port)*	AUDATA1 (AUD)
G	PTG0 input/output (port)*	AUDATA0 (AUD)

Note: Function 1 can be used when the AUD pins of the device are not connected to the emulator. When the AUD trace function is enabled, the emulator changes settings so that function 2 is forcibly used.

10. UBC

    When [User] is specified in the [UBC mode] list box in the [Configuration] dialog box, the UBC can be used in the user program.
    Do not use the UBC in the user program as it is used by the emulator when [EML] is specified in the [UBC mode] list box in the [Configuration] dialog box.

11. MFI

    When the MFI boot mode is used, be sure to activate the emulator by setting the MFIINT signal as a trigger for the MFI transfer from the base-band side.
    In the active-through mode, the emulator does not operate during break.

12. Memory Access during Break

    In the enabled MMU, when a memory is accessed and a TLB error occurs during break, it can be selected whether the TLB exception is controlled or the program jumps to the user exception handler in [TLB Mode] in the [Configuration] dialog box. When [TLB miss exception is enable] is selected, a “Communication Timeout error” will occur if the TLB exception handler does not operate correctly. When [TLB miss exception is disable] is selected, the program does not jump to the TLB exception handler even if a TLB exception occurs. Therefore, if the TLB exception handler does not operate correctly, a “Communication Timeout error” will not occur but the memory contents may not be correctly displayed.

13. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be 1.25 MHz.

14. [IO] Window

    - Display and modification

      Do not change values of the User Break Controller because it is used by the emulator.

      For each RWDT register, there are two registers to be separately used for write and read operations.

Table 2.3 RWDT Register

Register Name	Usage	Register
RWTCSR(W)	Write	RWDT control/status register
RWTCNT(W)	Write	RWDT counter
RWTCSR(R)	Read	RWDT control/status register
RWTCNT(R)	Read	RWDT counter

The RWDT operates only when the user program is executed. Do not change the value of the frequency change register in the [IO] window or [Memory] window.

The internal I/O registers can be accessed from the [IO] window. However, note the following when accessing the SDMR register of the bus-state controller. Before accessing the SDMR register, specify addresses to be accessed in the I/O-register definition file (SH7354.IO) and then activate the High-performance Embedded Workshop. After the I/O-register definition file is created, the MPU’s specifications may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register definition file can be customized depending on its format. Note that, however, the E200F emulator does not support the bit-field function.

- Verify

  In the [IO] window, the verify function of the input value is disabled.

15. Illegal Instructions

    If illegal instructions are executed by STEP-type commands, the emulator cannot go to the next program counter.

16. [Reset CPU] and [Reset Go] in the [Debug] Menu

    When [Reset Mode] of the [Configuration] dialog box is set as [Auto], an H-UDI reset is issued by executing [Reset CPU] or [Reset Go]. For the H-UDI reset, the clock pulse generator and RCLK watchdog timer are not initialized.
    When [User] is selected and [Reset CPU] or [Reset Go] is executed, a reset signal input from the user system is waited; do not input /RESETP.

2.2 Specific Functions for the Emulator when Using the SH7354

In the SH7354, the emulator does not support the I/O analyzer function.

2.2.1 Notes on Using the Trace Functions

The emulator supports the trace functions listed in table 2.4.

Table 2.4 Trace Functions

Function	Internal Trace	AUD Trace	Memory Output Trace
Branch trace	Supported (eight branches)	Supported	Supported
Range memory access trace	Supported (eight events)	Supported	Supported
Software trace	Supported (eight events)	Supported	Supported

Internal Trace Function: This function is activated by selecting the [Internal trace] radio button in the [Trace type] group box of the [Trace mode] page. Set the trace condition to be used.

Notes: 1. If an interrupt is generated at the program execution start or end, including a step operation, the emulator address may be acquired. In such a case, the following message will be displayed. Ignore this address because it is not a user program address.
*** EML ***

2. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
3. Trace information cannot be acquired for the following branch instructions:
   - The BF and BT instructions whose displacement value is 0
   - Branch to H'A0000000 by reset

AUD Trace Function: This function is operational when the AUD pin of the device is connected to the emulator. It is activated by selecting the [AUD trace] radio button in the [Trace type] group box of the [Trace mode] page.

Notes: 1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.

2. The AUD branch trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previously output address is the same as the upper 16 bits, the lower

16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.

3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. In the emulator, when multiple loops are performed to reduce the number of AUD trace displays, only the IP counts up.
5. In the emulator, the maximum number of trace displays is 524288 lines. However, the maximum number of trace displays differs according to the AUD trace information to be output. Therefore, the above pointers cannot be always acquired.
6. The AUD trace acquisition is not available when [User] is selected in the [UBC mode] list box of the [Configuration] dialog box. In this case, close the [Trace] window.
7. Do not use the AUD full-trace mode for the VIO function.
8. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.

Memory Output Trace Functions: This function is activated by selecting the [Use Memory trace] radio button in the [Trace type] group box of the [Trace mode] page.
In this function, write the trace data in the specified user memory range.
Specify the start address to output a trace for the [Start] edit box in the [User memory area] group box, and the end address for the [End Address] edit box.

Notes: 1. The memory range for which trace is output is the address on the system bus and not supported for the MMU or cache.
2. In the memory range for output, do not specify the ranges that the user program has been downloaded or the user program accesses.
3. The range for trace output must be 1 MB or less.

2.2.2 Notes on Using the JTAG (H-UDI) Clock (TCK) and AUD Clock (AUDCK)

1. Set the JTAG clock (TCK) frequency to lower than the frequency of the SH7354 peripheral module clock (CKP).
2. Set the AUD clock (AUDCK) frequency to 108 MHz or lower. If the frequency is higher than 108 MHz, the emulator will not operate normally.
3. The set value of the JTAG clock (TCK) is initialized by executing [Reset CPU] or [Reset Go]. Thus the TCK value will be 1.25 MHz.

2.2.3 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. Accordingly, it can be set only to the RAM areas in CS0 to CS6 and the internal RAM areas. A BREAKPOINT cannot be set to the following addresses:
   - ROM areas in CS0 to CS6
   - Areas other than CS0 to CS6 except for the internal RAM
   - A slot instruction of a delayed branch instruction
   - An area that can be only read by MMU
3. During step operation, BREAKPOINTs are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified, single-step operation is performed at the address and execution is continued from the next PC value. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
6. Note on DSP repeat loop:
   A BREAKPOINT is equal to a branch instruction. In some DSP repeat loops, branch instructions cannot be set. For these cases, do not set BREAKPOINTs. Refer to the hardware manual for details.
7. When the [Normal] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address or a virtual address according to the SH7354 MMU status during command input when the VPMAP_SET command setting is disabled. The ASID value of the SH7354 PTEH register during command input is used. When VPMAP_SET command setting is enabled, a BREAKPOINT is set to a physical address into which address translation is made according to the VP_MAP table. However, for addresses out of the range of the VP_MAP table, the address to which a BREAKPOINT is set depends on the SH7354 MMU status during command input. Even

when the VP_MAP table is modified after BREAKPOINT setting, the address translated when the BREAKPOINT is set valid.

8. When the [Physical] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address. A BREAKPOINT is set after disabling the SH7354 MMU upon program execution. After setting, the MMU is returned to the original state. When a break occurs at the corresponding virtual address, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
9. When the [Virtual] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a virtual address. A BREAKPOINT is set after enabling the SH7354 MMU upon program execution. After setting, the MMU is returned to the original state. When an ASID value is specified, the BREAKPOINT is set to the virtual address corresponding to the ASID value. The emulator sets the BREAKPOINT after rewriting the ASID value to the specified value, and returns the ASID value to its original value after setting. When no ASID value is specified, the BREAKPOINT is set to a virtual address corresponding to the ASID value at command input.
10. An address (physical address) to which a BREAKPOINT is set is determined when the BREAKPOINT is set. Accordingly, even if the VP_MAP table is modified after BREAKPOINT setting, the BREAKPOINT address remains unchanged. When a BREAKPOINT is satisfied with the modified address in the VP_MAP table, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
11. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the event condition, the mark ● disappears.

2.2.4 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.
3. If a PC break address condition is set to the slot instruction after a delayed branch instruction, user program execution cannot be terminated before the slot instruction execution; execution stops before the branch destination instruction.

2.2.5 Note on Setting the UBC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [UBC mode] list box has been set, Ch10 (IA_OA_R) and Ch11 (OA_OA_CT_R) of Event Condition cannot be used.

2.2.6 Note on Setting the PPC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [PPC mode] list box has been set, Ch1 and Ch2 of the performance analysis function and options 1 and 2 of the profile function cannot be used.

Section 3 Preparing to Connect the Trace Unit

3.1 Connecting the E200F Trace Unit with the User System

To use the external bus trace function in the emulator, the emulator and the user system must be connected via the external bus trace unit (R0E0200F0ETU00). Install the trace unit connector on the user system for connection of the trace unit, referring to section 3.2, Installing the Trace Unit Connector, in this manual. When designing the user system, read the SH-4A, SH4AL-DSP E200F Emulator User's Manual and hardware manual for the related MPU.

3.2 Installing the Trace Unit Connector

3.2.1 Trace Unit Connector Installed on the User System

Table 3.1 shows the recommended trace unit connector.

Table 3.1 Recommended Connector

Type Number	Manufacturer	Specification
QTH-090-04-L-D-A	Samtec, Inc.	QTH series, 0.5-mm pitch, 180 pins

Note: To connect the connector on the trace unit, do not place any components within 6 mm of the trace unit connector.

3.2.2 Pin Assignments of the User System Connector

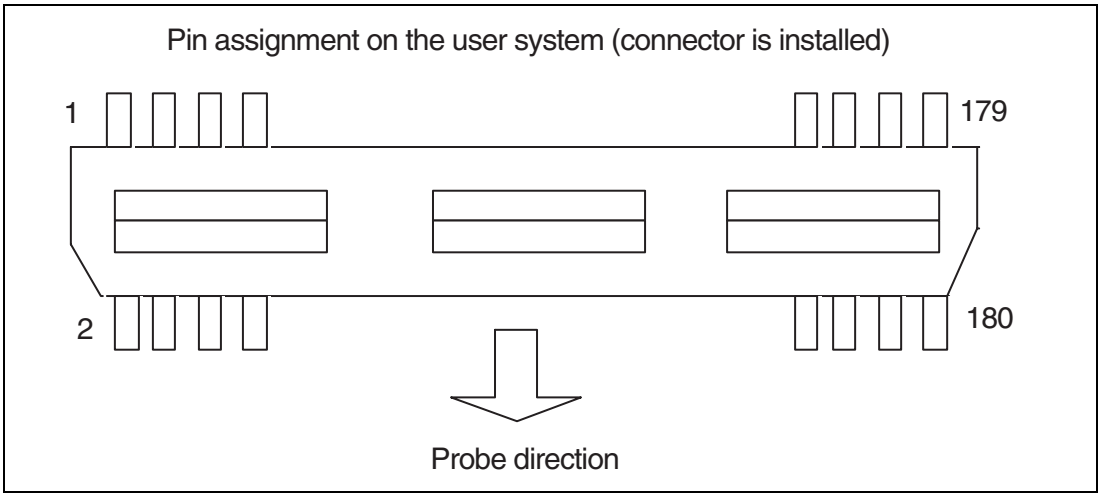


Figure 3.1 Pin Assignments of the User System Connector

3.2.3 Recommended Pad Pattern

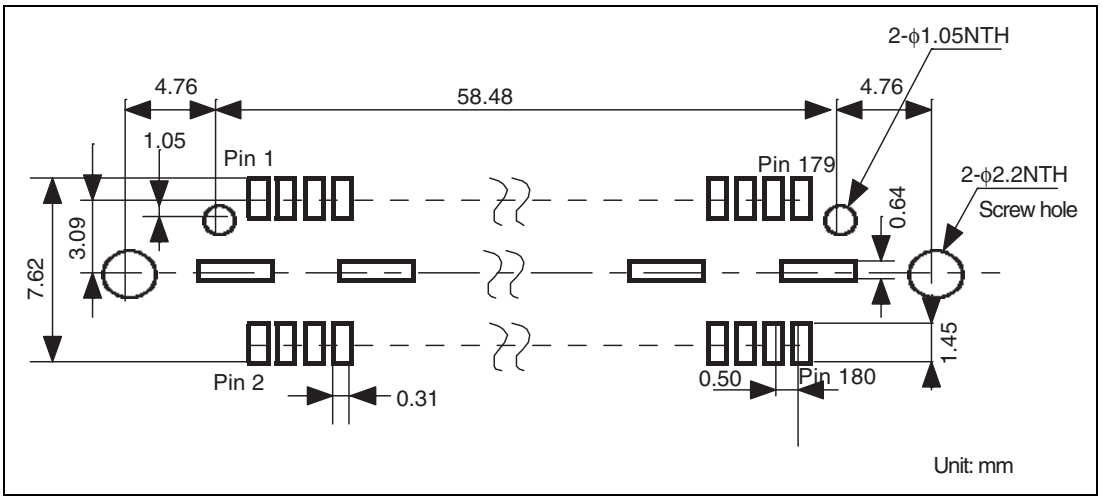


Figure 3.2 Recommended Pad Pattern (on which the Connector is Installed)

3.2.4 Restrictions on Component Installation

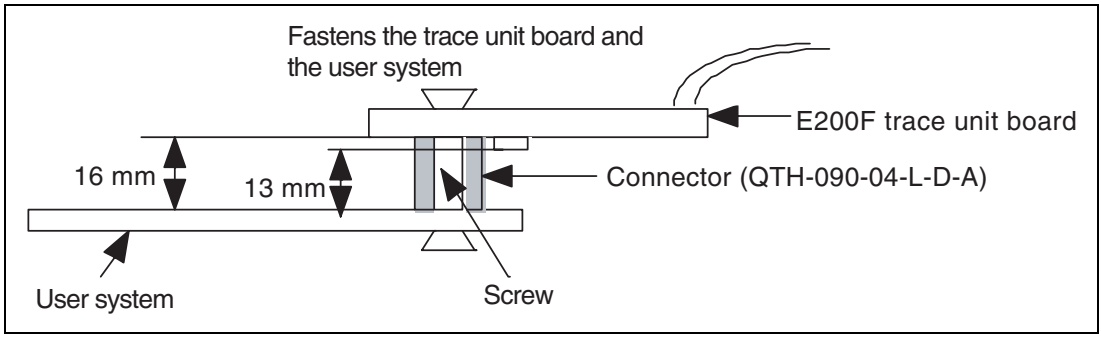


Figure 3.3 Restrictions on Component Installation

3.2.5 Pin Assignments of the Trace Unit Connector

Table 3.2 shows the pin assignments of the trace unit connector.

Table 3.2 Pin Assignments of the Trace Unit Connector

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
1	I	UA-P0	PTU0/A0/ LCDD18	Port/address bus/ LCD data bus	Connect the address signal of the MPU. Fix A0 to low level when A0 is not used.
2	I	UA-P1	PTU1/A1/ LCDD19	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
3	I	UA-P2	PTU2/A2/ LCDD20	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
4	I	UA-P3	PTU3/A3/ LCDD21	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
5	I	UA-P4	PTU4/A4/ LCDD22	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
6	I	UA-P5	PTU5/A5/ LCDD23	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
7	I	UA-P6	PTH0/A6/ LCDD16	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
8	I	UA-P7	PTH1/A7/ LCDD17	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
9		GND	GND		
10		GND	GND		
11	I	UA-P8	PTL0/A8/ LCDD8	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
12	I	UA-P9	PTL1/A9/ LCDD9	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
13	I	UA-P10	PTL2/A10/ LCDD10	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
14	I	UA-P11	PTL3/A11/ LCDD11	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
15	I	UA-P12	PTL4/A12/ LCDD12	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
16	I	UA-P13	PTL5/A13/ LCDD13	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
17	I	UA-P14	PTL6/A14/ LCDD14	Port/address bus/ LCD data bus	Connect the address signal of the MPU.
18	I	UA-P15	PTL7/A15/ LCDD15	Port/address bus/ LCD data bus	Connect the address signal of the MPU.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
19		GND	GND		
20		GND	GND		
21	I	UA-P16	PTH5/A16/ LCDHSYN/ LCDCS	Port/ address bus/ LCD horizontal-synchronous signal/ LCD chip select	Connect the address signal of the MPU.
22	I	UA-P17	PTH6/A17/ LCDVSYN	Port/ address bus/ LCD vertical-synchronous signal	Connect the address signal of the MPU.
23	I	UA-P18	PTM0/A18/ LCDD0	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
24	I	UA-P19	PTM1/A19/ LCDD1	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
25	I	UA-P20	PTM2/A20/ LCDD2	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
26	I	UA-P21	PTM3/A21/ LCDD3	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
27	I	UA-P22	PTM4/A22/ LCDD4	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
28	I	UA-P23	PTM5/A23/ LCDD5	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
29		GND	GND		
30		GND	GND		
31	I	UA-P24	PTM6/A24/ LCDD6	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
32	I	UA-P25	PTM7/A25/ LCDD7	Port/ address bus/ LCD data bus	Connect the address signal of the MPU.
33	I	UA-P26	GND		
34	I	UA-P27	GND		
35	I	UA-P28	GND		
36	I	UA-P29	GND		
37	I	UA-P30	GND		
38	I	UA-P31	GND		
39		GND	GND		
40		GND	GND		
41	IO	UD-P0	PTA0/D0/ VIO_D0/ THPRTA0	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
42	IO	UD-P1	PTA1/D1/ VIO_D1/ THPRTA1	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
43	IO	UD-P2	PTA2/D2/ VIO_D2/ THPRTA2	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
44	IO	UD-P3	PTA3/D3/ VIO_D3/ THPRTA3	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
45	IO	UD-P4	PTA4/D4/ VIO_D4/ THPRTA4	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
46	IO	UD-P5	PTA5/D5/ VIO_D5/ THPRTA5	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
47	IO	UD-P6	PTA6/D6/ VIO_D6/ THPRTA6	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.
48	IO	UD-P7	PTA7/D7/ VIO_D7/ THPRTA7	Port/data bus/ VIO data input/ through port	Connect the data signal of the MPU.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
49		GND	GND	GND	
50		GND	GND	GND	
51	IO	UD-P8	PTS0/D8/ VIO_CLK/ THPRTB0	Port/data bus/ VIO clock input/ through port	Connect the data signal of the MPU.
52	IO	UD-P9	PTS1/D9/ VIO_VD/ THPRTB1	Port/data bus/ VIO vertical signal/ through port	Connect the data signal of the MPU.
53	IO	UD-P10	PTS2/D10/ VIO_HD/ THPRTB2	Port/data bus/ VIO horizontal signal/ through port	Connect the data signal of the MPU.
54	IO	UD-P11	PTS3/D11/ VIO_FLD/ THPRTB3	Port/data bus/ VIO field select signal/ through port	Connect the data signal of the MPU.
55	IO	UD-P12	PTH2/D12/ LCDDON/ LCDDON2	Port/data bus/ LCD start signal 1/ LCD start signal 2	Connect the data signal of the MPU.
56	IO	UD-P13	PTH3/D13/ LCDDISP/LC DRS	Port/data bus/ LCD enable signal/ LCD register select signal	Connect the data signal of the MPU.
57	IO	UD-P14	PTH4/D14/ LCDVSYN2	Port/data bus/ LCD vertical-synchronous signal	Connect the data signal of the MPU.
58	IO	UD-P15	PTR2/D15/ LCDLCLK	Port/data bus/ LCD clock source input	Connect the data signal of the MPU.
59		GND	GND		
60		GND	GND		
61	IO	UD-P16	N.C.[*1]	N.C.	
62	IO	UD-P17	N.C.[*1]	N.C.	

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
63	IO	UD-P18	N.C.*1	N.C.	
64	IO	UD-P19	N.C.*1	N.C.	
65	IO	UD-P20	N.C.*1	N.C.	
66	IO	UD-P21	N.C.*1	N.C.	
67	IO	UD-P22	N.C.*1	N.C.	
68	IO	UD-P23	N.C.*1	N.C.	
69		GND	GND		
70		GND	GND		
71	IO	UD-P24	N.C.*1	N.C.	
72	IO	UD-P25	N.C.*1	N.C.	
73	IO	UD-P26	N.C.*1	N.C.	
74	IO	UD-P27	N.C.*1	N.C.	
75	IO	UD-P28	N.C.*1	N.C.	
76	IO	UD-P29	N.C.*1	N.C.	
77	IO	UD-P30	N.C.*1	N.C.	
78	IO	UD-P31	N.C.*1	N.C.	
79		GND	GND		
80		GND	GND		
81	IO	UD-P32	N.C.*1		
82	IO	UD-P33	N.C.*1	N.C.	
83	IO	UD-P34	N.C.*1	N.C.	
84	IO	UD-P35	N.C.*1	N.C.	
85	IO	UD-P36	N.C.*1	N.C.	
86	IO	UD-P37	N.C.*1	N.C.	
87	IO	UD-P38	N.C.*1	N.C.	
88	IO	UD-P39	N.C.*1	N.C.	
89		GND	GND		
90		GND	GND		
91	IO	UD-P40	N.C.*1	N.C.	
92	IO	UD-P41	N.C.*1	N.C.	

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
93	IO	UD-P42	N.C.*1	N.C.	
94	IO	UD-P43	N.C.*1	N.C.	
95	IO	UD-P44	N.C.*1	N.C.	
96	IO	UD-P45	N.C.*1	N.C.	
97	IO	UD-P46	N.C.*1	N.C.	
98	IO	UD-P47	N.C.*1	N.C.	
99		GND	GND		
100		GND	GND		
101	IO	UD-P48	N.C.*1	N.C.	
102	IO	UD-P49	N.C.*1	N.C.	
103	IO	UD-P50	N.C.*1	N.C.	
104	IO	UD-P51	N.C.*1	N.C.	
105	IO	UD-P52	N.C.*1	N.C.	
106	IO	UD-P53	N.C.*1	N.C.	
107	IO	UD-P54	N.C.*1	N.C.	
108	IO	UD-P55	N.C.*1	N.C.	
109		GND	GND		
110		GND	GND		
111	IO	UD-P56	N.C.*1	N.C.	
112	IO	UD-P57	N.C.*1	N.C.	
113	IO	UD-P58	N.C.*1	N.C.	
114	IO	UD-P59	N.C.*1	N.C.	
115	IO	UD-P60	N.C.*1	N.C.	
116	IO	UD-P61	N.C.*1	N.C.	
117	IO	UD-P62	N.C.*1	N.C.	
118	IO	UD-P63	GND		
119		GND	GND		
120		GND	GND		

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
121	I	UCONT-P0	PTR0/WE0/ LCDVEPWC/ LCDVEPWC2	Port/lower byte write signal/liquid-crystal-module power control (VEE) 1/ liquid-crystal-module power control (VEE) 2	Connect the WE0 signal of the MPU.
122	I	UCONT-P1	PTR1/WE1/ LCDVCPWC/ LCDVCPWC2	Port/upper byte write signal/liquid-crystal-module power control (VCC) 1/ liquid-crystal-module power control (VCC) 2	Connect the WE1 signal of the MPU.
123	I	UCONT-P2	N.C.*1	N.C.	
124	I	UCONT-P3	N.C.*1	N.C.	
125	I	UCONT-P4	N.C.*1	N.C.	
126	I	UCONT-P5	N.C.*1	N.C.	
127	I	UCONT-P6	N.C.*1	N.C.	
128	I	UCONT-P7	N.C.*1	N.C.	
129	I	UCONT-P8	N.C.*1	N.C.	
130	I	UCONT-P9	N.C.*1	N.C.	
131	I	UCONT-P10	PTH7/RDWR/ LCDDCK/ LCDWR	Port/read/write signal/LCD dot clock/LCD write strobe	Connect the RDWR signal of the MPU.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
132	I	UCONT-P11	PTR4/RD/ LCDRD	Port/read signal/ LCD read strobe	Connect the RD signal of the MPU.
133	I	UCONT-P12	RESETP	Power-on reset	Connect the RESETP signal of the MPU.
134	I	UCONT-P13	N.C.[*1]	N.C.	
135	I	UCONT-P14	N.C.[*1]	N.C.	
136	I	UCONT-P15	N.C.[*1]	N.C.	
137	I	UCONT-P16	WAIT	External wait input	Connect the wait signal of the MPU. When WAIT is not used, this is N.C.
138	I	UCONT-P17	PTJ7/ STATUS0	Port/status output	Connect the STATUS0 signal of the MPU.
139	I	UCONT-P18	PTJ6/ STATUS2	Port/status output	Connect the STATUS2 signal of the MPU.
140	I	UCONT-P19	PTJ5/ PDSTATUS	Port/status output	Connect the PDSTATUS signal of the MPU.
141	I	UCONT-P20	NMI	NMI	Connect the NMI signal of the MPU.
142	I	UCONT-P21	PTJ0/IRQ0/ THPRTB5	Port/ interrupt request/ through port	Connect the interrupt request signal. When interrupt is not used, this is N.C.
143	I	UCONT-P22	PTJ1/IRQ1/ THPRTB6	Port/ interrupt request/ through port	Connect the interrupt request signal. When interrupt is not used, this is N.C.
144	I	UCONT-P23	PTD6/ SDHIWP/ IRQ2	Port/SD write protect/interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
145	I	UCONT-P24	PTK6/SIUILR/ IRQ3	Port/SIU sound input L/R clock/ interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
146	I	UCONT-P25	PTK5/SIUIBT/ IRQ4	Port/SIU sound input bit clock/ interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
147	I	UCONT-P26	N.C.*1	N.C.	Connect the interrupt request signal. When interrupt is not used, this is N.C.
148	I	UCONT-P27	N.C.*1	N.C.	Connect the interrupt request signal. When interrupt is not used, this is N.C.
149	I	UCONT-P28	N.C.*1	N.C.	Connect the interrupt request signal. When interrupt is not used, this is N.C.
150	I	UCONT-P29	N.C.*1		
151	I	UCONT-P30	N.C.*1		
152	I	UCONT-P31	N.C.*1		
153	I	GND	GND		
154	I	GND	GND		
155	I	MPUCLK	CKO	CKO clock	Be sure to connect the CKO clock of the MPU.
156	I	GND	GND		
157	I	GND	GND		
158	I	DDRCLK	N.C.*1		
159	I	GND	GND		
160	I	DDRCLK-N	N.C.*1		
161	I	GND	GND		
162	I	GND	GND		
163	I	CS0IN-N	PTS6/CS0/ MFIDREQ1	Port/chip select 0/ MFIDREQ1 output	Connect CS (chip select). Fix the unused CS pin to high level.
164	I	CS1IN-N	N.C.*1		
165	I	CS2IN-N	N.C.*1		
166	I	CS3IN-N	PTS5/CS4/ MFIDREQ0	Port/chip select 4/ MFIDREQ0 output	Connect CS (chip select). Fix the unused CS pin to high level.
167	I	CS4IN-N	N.C.*1		

Table 3.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7354 Signal Name	Meaning of Signal	Note
168	I	CS5IN-N	N.C.*1		
169	I	CS6IN-N	PTR3/CS6A/ LCDCS2	Port/chip select 6A/LCD chip select 2	Connect CS (chip select). Fix the unused CS pin to high level.
170	I	CS7IN-N	N.C.*1		
171	I	CS8IN-N	N.C.*1		
172	I	CS9IN-N	N.C.*1		
173	O	EM0OUT-N	EM0OUT-N	Emulation-memory select output	Connect this signal instead of CS of the MPU when an emulation memory is used.*2
174	O	EM1OUT-N	N.C.*1		
175	O	EM2OUT-N	N.C.*1		
176	O	EMEN-P	N.C.*1		
177	I	UVCC1	VccQ1	Power supply for SRAM interface I/O (1.8 V/2.85 V)	
178	I	UVCC2	VccQ3	Power supply for SDRAM I/O (1.8 V)	
179	I	UVCC3	Power supply for user system: 2.85 V	Power supply 2.85 V	
180	I	UCNN-N	Connect to user connector	GND	Fix this signal to low level.

Notes: 1. Do not connect anything to this pin.
2. Refer to section 3.2.8, Description of Emulation Memory Control Signal.

3.2.6 Layout of the Trace Unit Connector

When designing the user system, there are restrictions on the position to install the trace unit connector. Figure 3.4 shows the external dimensions of the trace unit.

The size of the printed-circuit board of the E200F trace unit is 90 mm × 125 mm. The size of components around the user system connector must not exceed the limit on component installation (the height must be 10 mm or less).

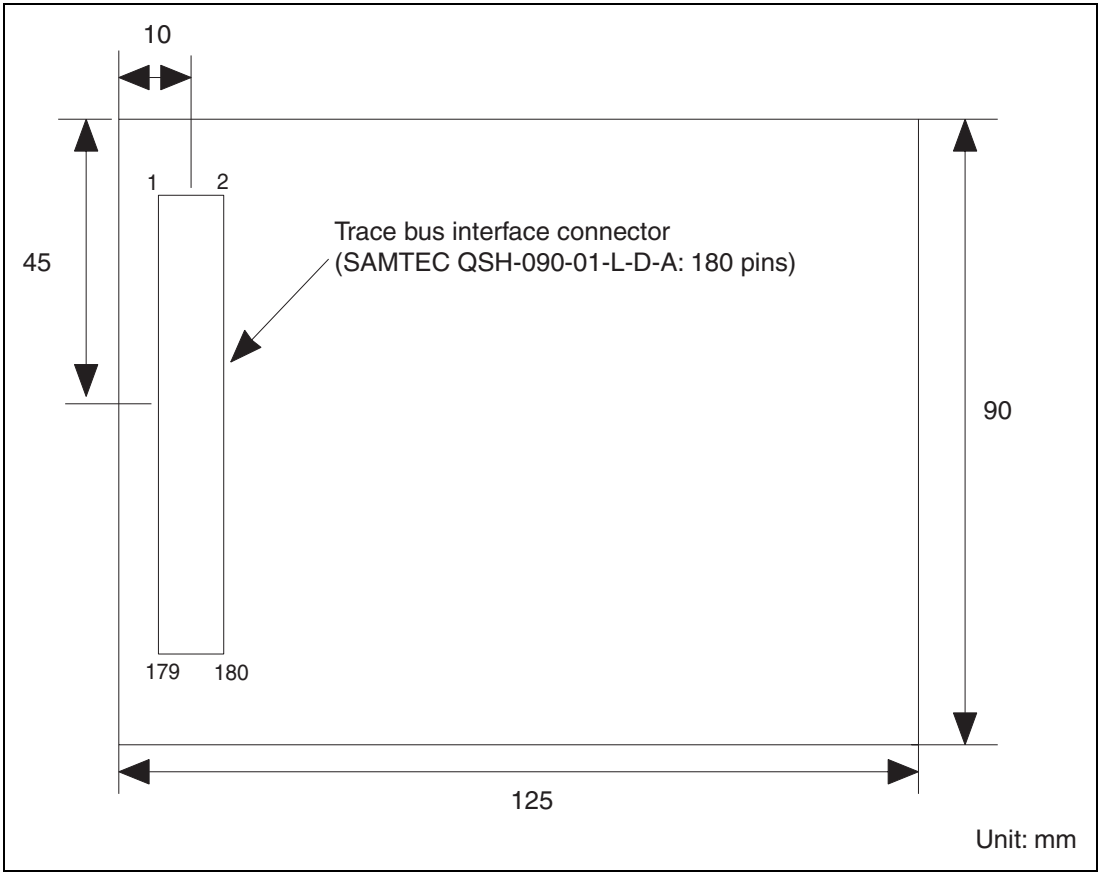


Figure 3.4 External Dimensions of the Trace Unit (on which the Connector is Installed)

Notes: 1. The external bus trace interface connector installed on the user system must be as close to the MPU as possible.

2. Wiring pattern of clock lines (CKO)
   The followings are notes on wiring of clock lines for the E200F trace interface signals. Take them into consideration when designing the user system to embed suitable clock lines.
   (a) Clock lines must be as short as possible.
   (b) Clock lines must be surrounded by the GND pattern for protection so that the signals will be of low-impedance.
   (c) Other layers next to the layer with clock line wiring should have solid patterns of GND/VCC so that the signals will be of low-impedance.
   (d) To prevent affect by the crosstalk noise, other signal patterns must not be embedded along with the clock lines.

3.2.7 Restrictions on Using the Trace Unit

(1) This trace unit supports the external bus memory interfaces of SH7354; SRAM interface and byte-selection SRAM interface (except for SRAM page mode). For burst ROM and SDRAM interfaces, bus trace acquisition and bus event detection are not supported.

(2) When the sequential trace stop condition or delay-count trace stop condition is specified, trace acquisition will stop after several cycles have been passed from the stop condition match cycle.

(3) During break mode, a timestamp value of the external bus trace information that has been acquired by a trace is not counted up.

(4) When an emulation memory is used, it is not possible to access the memory on the user system which is in the same area as an area where the emulation memory has been set.

(5) When an emulation memory is accessed, at least six wait cycles are required. Set the number of wait cycles by using bits WR3 to WR0 in the CS0 area wait control register (CS0WCR).

(6) The emulator occupies the CS0 area where the emulation memory has been set. Accordingly, it is not possible to access the memory in the user system side of that area.

(7) This trace unit is available for the external 8- or 16-bit data bus width. When the data bus width is 8 bits, unused data bus pins D15 to D8 of the trace unit connector must be fixed to high or low level. In addition, when area 0 is used with the emulation memory, the bus width of the emulation memory needs to be set. For details, refer to section 5.1.8, Changing the Memory Map Setting, in the SH-4A, SH4AL-DSP E200F Emulator User's Manual.

3.2.8 Description of Emulation Memory Control Signal

When the CS signal of the MPU is connected directly to the memory or used to generate the CS signal of the memory, connect the EM0OUT-N signal (pin 173) of the external bus connector instead of the CS signal of the MPU.

Even if the emulator is not used, prepare the jumper pins as shown in figure 3.5 so that connection of the CS signal can be easily changed.

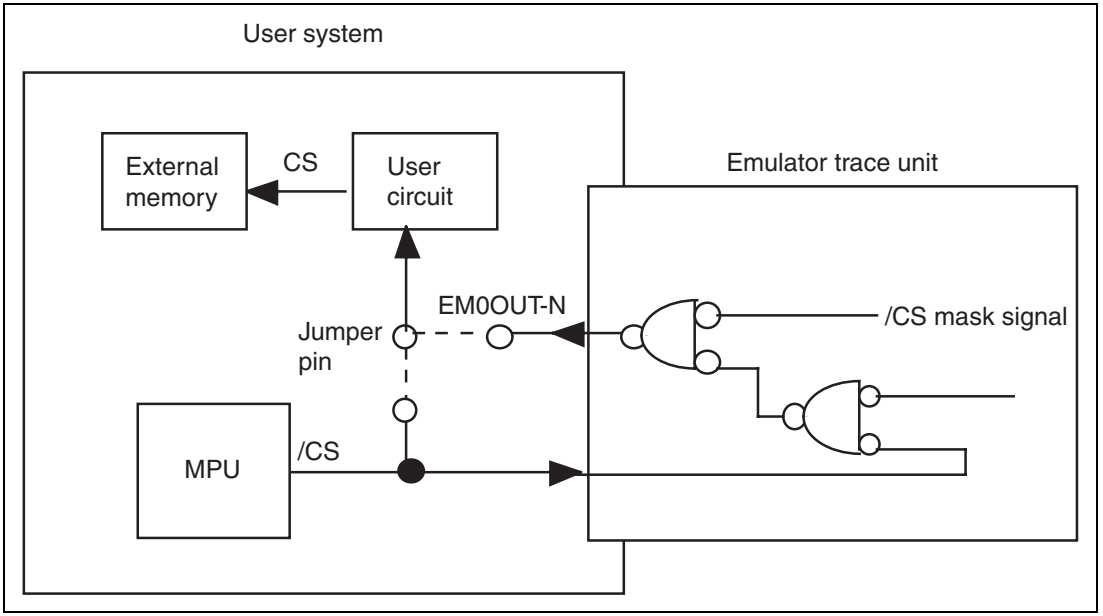


Figure 3.5 EM0OUT-N Signal (Pin 173)

SH-4A, SH4AL-DSP E200F Emulator
Additional Document for User's Manual
Supplementary Information on Using the SH7354

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