User's Manual

32

RX671 Group

Renesas Starter Kit+ for RX671
User's Manual

RENESAS 32-Bit MCU
RX Family / RX600 Series

Renesas Electronics
www.renesas.com

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit+ (RSK+), the user accepts the following terms:

The RSK+ is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK+ is assumed by the User. The RSK+ is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK+. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK+, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK+ product:

This Renesas Starter Kit+ is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RX671 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	Renesas Starter Kit+ for RX671 User's Manual	R20UT4879EG
Tutorial Manual	Provides a guide to setting up RSK+ environment, running sample code and debugging programs.	Renesas Starter Kit+ for RX671 Tutorial Manual	CS+: R20UT4880EG e^2 studio: R20UT4883EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample.	Renesas Starter Kit+ for RX671 Quick Start Guide	CS+: R20UT4881EG e^2 studio: R20UT4884EG
Smart Configurator Tutorial	Provides a guide to code generation and importing into the e^2 studio/CS+ IDE.	Renesas Starter Kit+ for RX671 Smart Configurator Tutorial Manual	CS+: R20UT4882EG e^2 studio: R20UT4885EG
Schematics	Full detail circuit schematics of the CPU Board.	Renesas Starter Kit+ for RX671 Schematics	R20UT4878EG
Hardware Manual	Provides technical details of the RX671 microcontroller.	RX671 Group Hardware Manual	R01UH0899EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DNF	Do Not Fit
E1 / E2 Lite	Renesas On-chip Debugging Emulator
EEPROM	Electronically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GLCDC	Graphic LCD Controller
I2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
RTC	Real Time Clock
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer

Table of Contents

1. Overview

1.1 Purpose

This CPU Board is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the CPU Board hardware.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample applications
- Sample peripheral device initialisation code

The RSK+ board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microcontroller	Part No : R5F5671EHDFB *3
	Package : 144-pin PLQP0144KA-B
	On-Chip Memory : ROM 2MB, RAM 384KB
On-Board Memory	SDRAM: 128Mbit (Data width 16bit)
	I²C EEPROM: 2Kbit
	SPI Serial Flash: 32Mbit x 2
Input Clock	RX671 Main : 24MHz
	RX671 Sub : 32.768kHz
	RL78/G1C Main: 12MHz
Power Supply	DC Power Jack : 5 V Input
	Power Supply IC : 5V Input, 3.3V Output
	Power Supply IC : 3.3V Input, 3.3V Output(For SDHI)
	Power Supply IC : 5V Input, 5V Output(For USB Host)
Debug Interface	E2 Lite 14-pin box header
DIP Switch	MCU Mode Configuration & Pin Function Selection : 4-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer(for ADC)	Single-turn, 10kΩ
LED	5V Power indicator: green x 1
	3.3V Power Indicator : green x 1
	User : green x 1, orange x 1, red x 2
SDHI *1	SD Card Slot (4-bit) x 1
CAN	Connector : 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
USB	USB0-Function : USB-MiniB
	USB0-Host : USB-TypeA
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod™	PMOD1 : Angle type, 12-pin Connector
	PMOD2 : Angle type, 12-pin Connector
Touch Interface	Slider x 1, Key x 2
SSIE & Audio Interface	Audio codec
	Terminal Block for passive speaker (4-pin)
	Headphone Jack
	Microphone x 2
Battery backup	Coin Cell Holder *4
Application Board Interface *2	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: The RX671 Group incorporate an SD Host Interface (SDHI) which is compliant with the SD Specifications. When developing host devices that are compliant with the SD Specifications, the user must enter into the SD Host/Ancillary Product License Agreement (SD HALA).

*2: The connector is not included in the product.

*3: R5F5671EHDFB has a built-in security function.

*4: Not fitted.

2. Power Supply

2.1 Requirements

This board has an optional centre positive supply connector using a 2.0mm barrel power jack (PWR). The main power supply connected to PWR should supply a minimum of 10W to ensure full functionality. When the board is connected to another system then that system should supply power to the board.

This CPU board supports one external voltage input. Details of the external power supply connection are shown in **Table 2-1 and Table 2-2** below. The default power configuration is shown in **bold, blue text.**

Table 2-1: PWR connector Requirements

Connector	Supply voltage
PWR	Input 5VDC

There are RSK+ products which supports the 12V voltage input. Since this board is supporting the 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally.
Moreover, the main power supply connected to PWR should supply a minimum of 10W to ensure full functionality.

Table 2-2: Main Power Supply Requirements

J25[*1] Setting	Supply Source	Board_5V	UC_VCC
Open	**PWR connector**/JA1-5V/Unregulated_VCC	**5V**	**3.3V**
Shorted	VBUS0	5V	3.3V

[*1]: The connector is not included to a product.

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the ‘Release’ build of the example tutorial software pre-programmed into the Renesas microcontroller. Please consult the ‘Renesas Starter Kit+ Smart Configurator Tutorial Manual’ for further information of this example.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

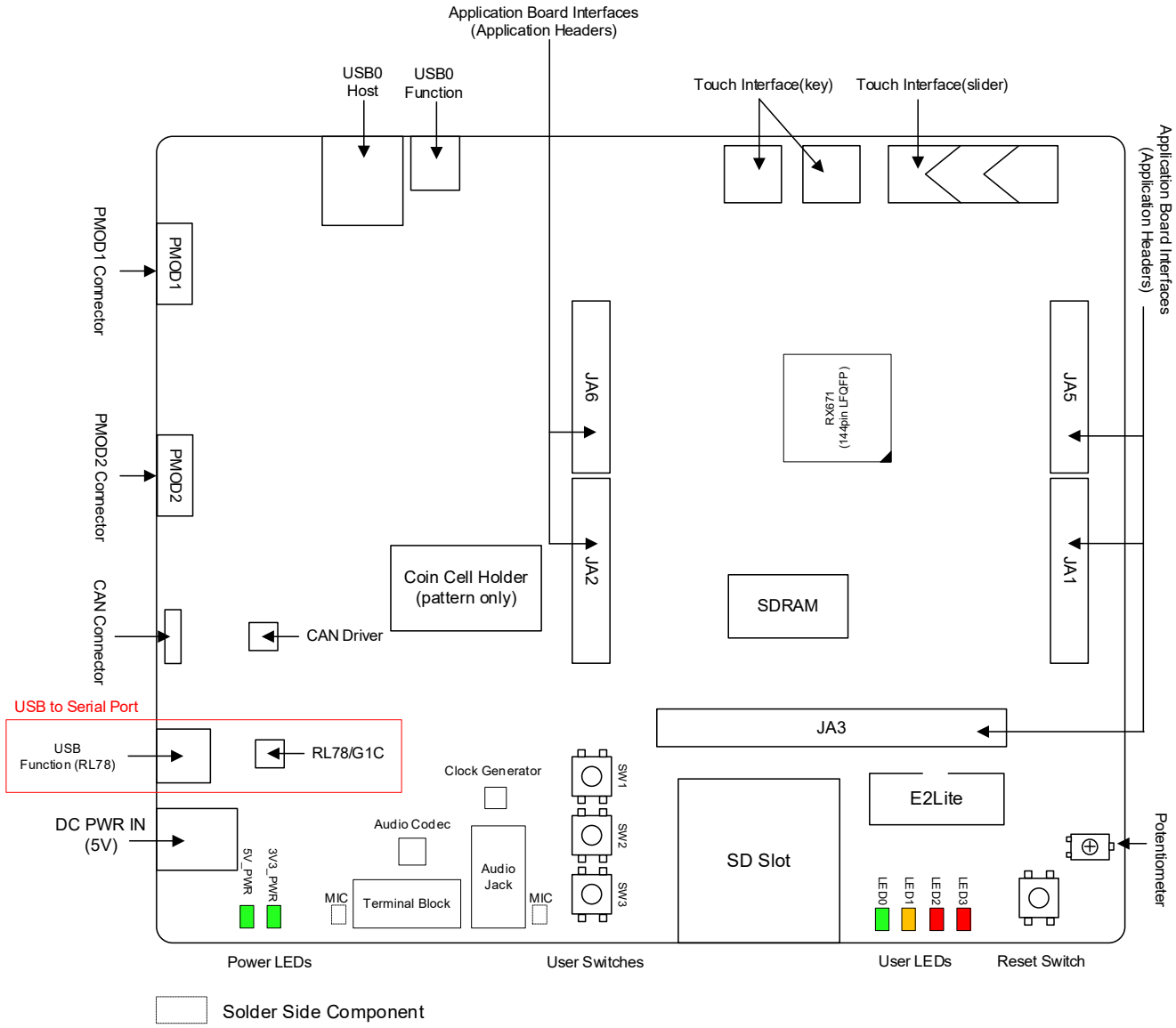

Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

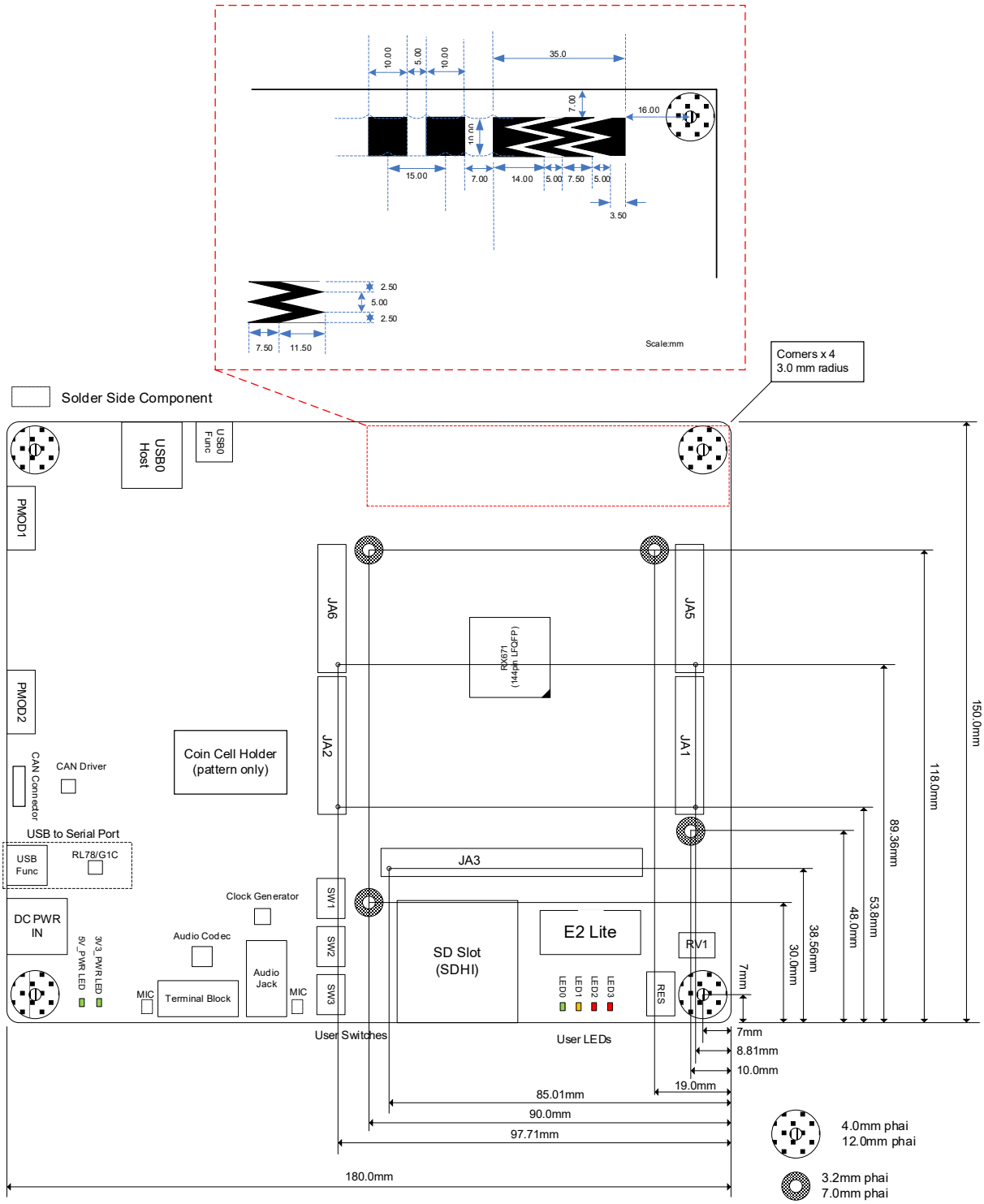

Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in **Figure 3-4**. Component types and values are shown on the board schematics.

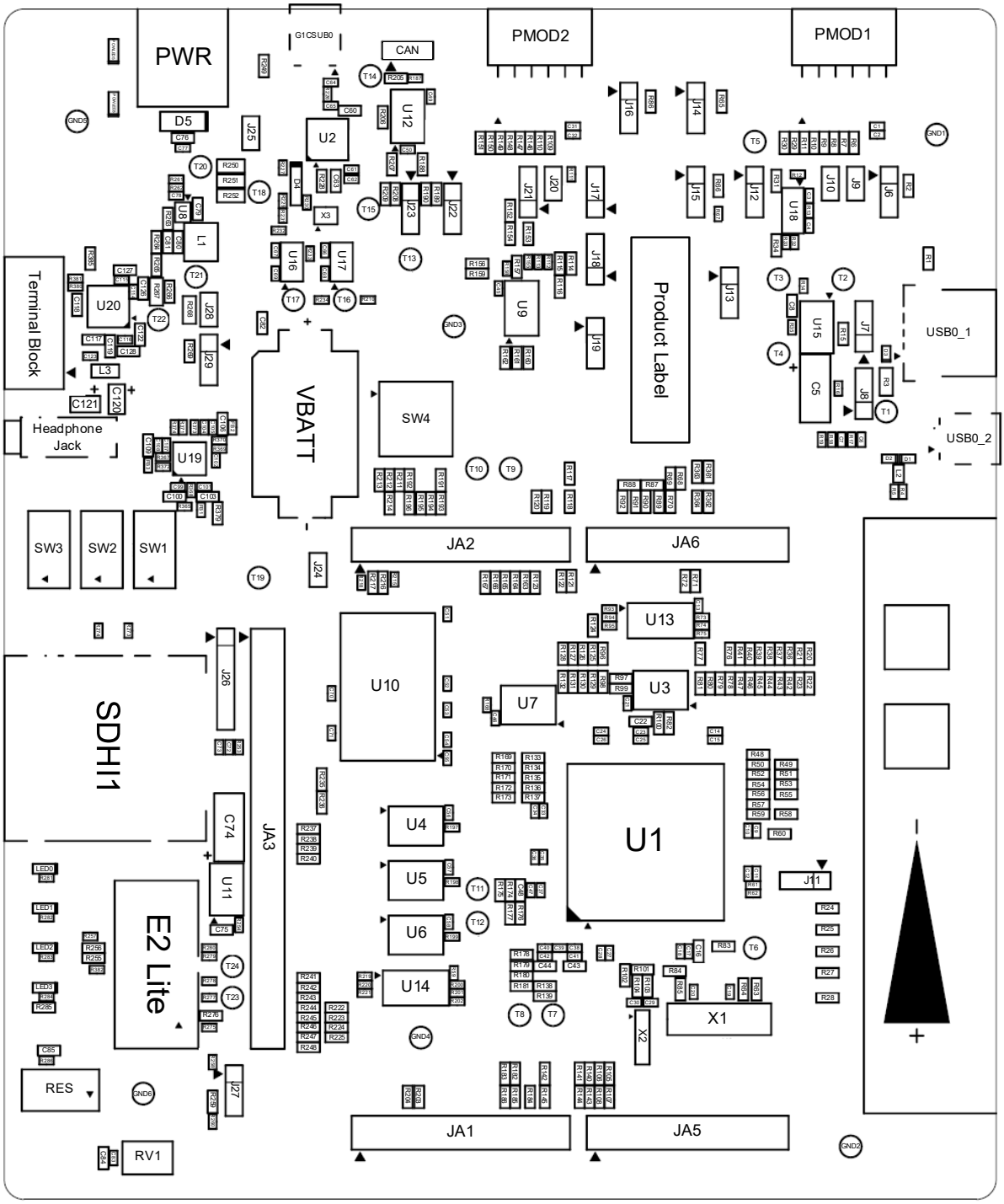

Figure 3-3: Top-Side Component Placement

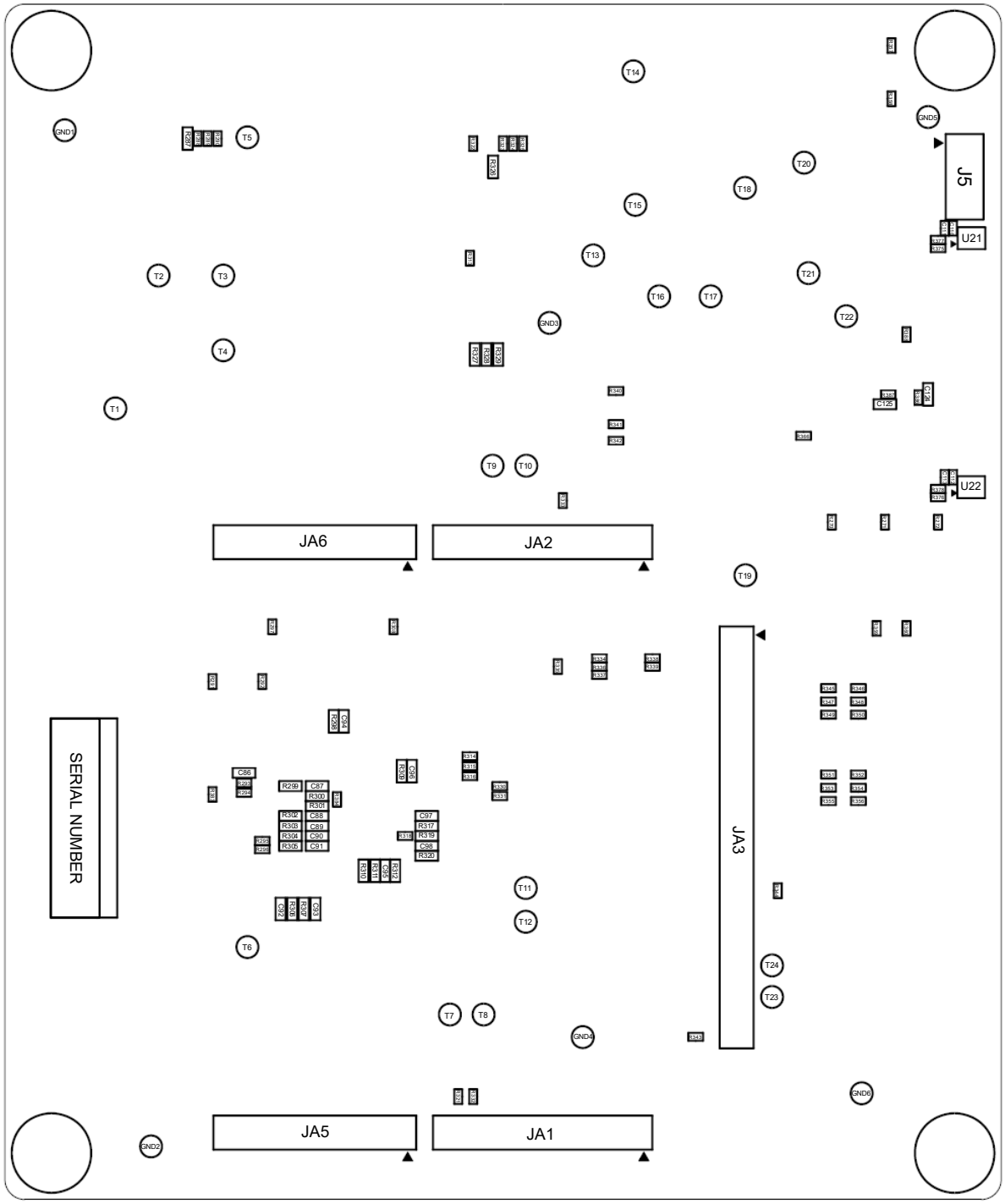

Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MCU.

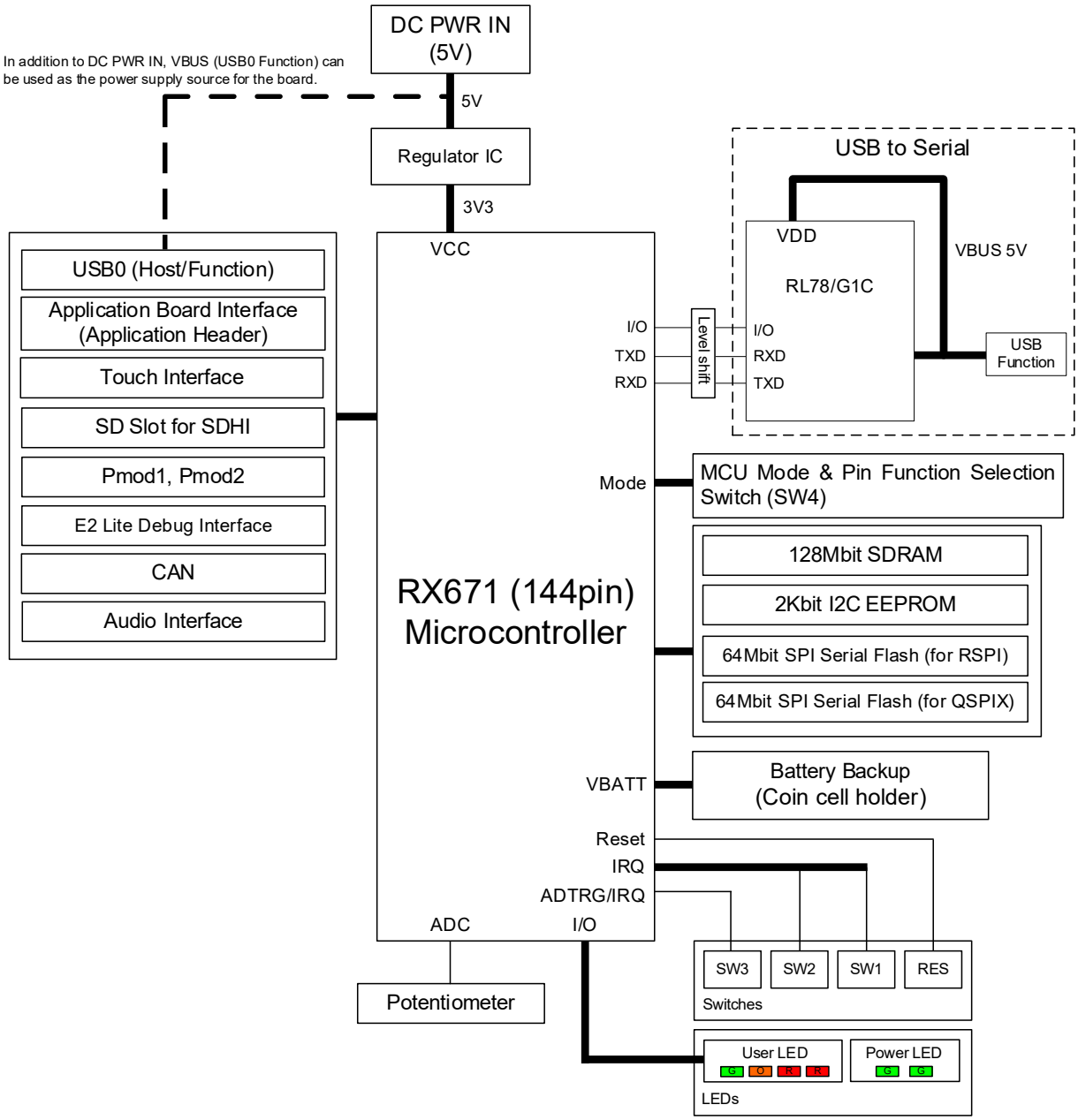

Figure 4-1: Internal Board Block Diagram

4.2 Debugger Connections

Figure 4-2 below shows the connections between the CPU board, E2 Lite debugger and the host PC.

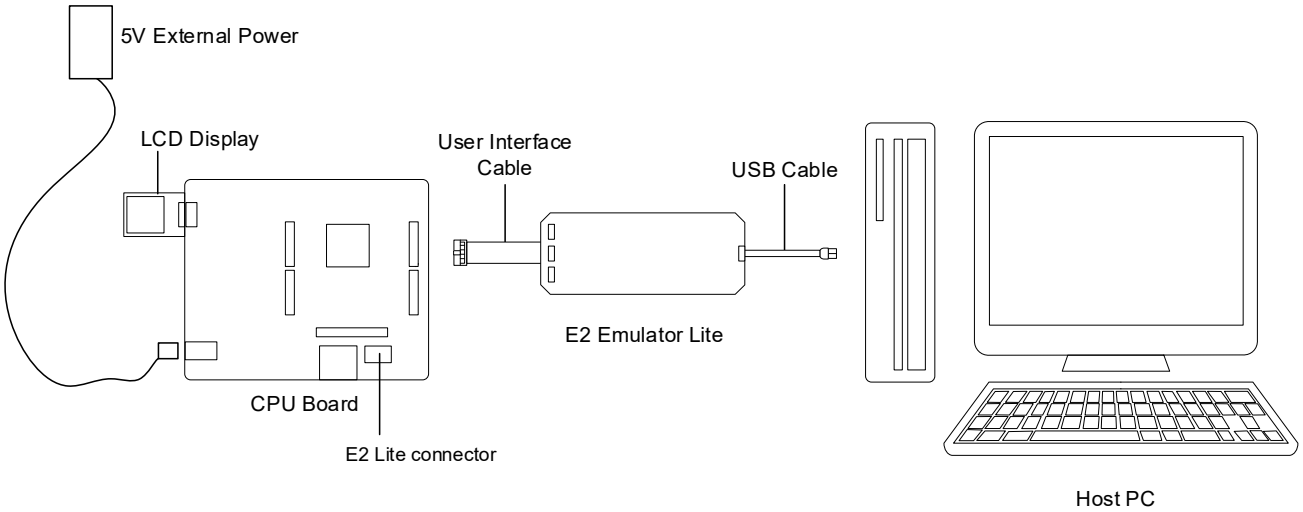

Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal, and is triggered from the RES switch. Refer to the RX671 Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX671 Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators and clock generator fitted to the board are listed in **Table 5-1** and **Table 5-2** below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX671	Fitted	24MHz	Encapsulated, SMT
X2	Real time Clock for RX671	Fitted	32.768kHz	Encapsulated, SMT
X3	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT

Table 5-2: Clock Generator

Clock Generator	Function	Default Placement	Frequency
U19	Audio clock for RX671 and audio codec	Fitted	24.576MHz

5.3 Switches

There are four switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-3 and Table 5-4**. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-3: Push Switch Connections

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	19
SW1	Connects to an IRQ9 input for user controls.	P91	129
SW2	Connects to an IRQ10 input for user controls.	P92	128
SW3	Connects to an IRQ15 input for user controls. Connects to an ADTRG0 input for ADC controls.	P07	144

Table 5-4: DIP Switch Connections

Switch		Function	MCU	
			Signal (Port)	Pin
SW4	Pin 1	Refer to section 6.2 for the setting contents.	MD/FINED	16
SW4	Pin 2	Refer to section 6.2 for the setting contents.	PC7	60
SW4	Pin 3	Refer to section 6.3 for the setting contents.	NC	NC
SW4	Pin 4	Refer to section 6.3 for the setting contents.	NC	NC

5.4 LEDs

There are 6 LEDs on the RSK+ board. The function of each LED, its colour, and its connections are shown in **Table 5-5**.

Table 5-5: LED Connections

LED	Colour	Function	MCU	
			Port	Pin
3V3_PWR	Green	Indicates the status of the Board_3V3 power rail.	NC	NC
5V_PWR	Green	Indicates the status of the Board_5V power rail.	NC	NC
LED0	Green	User operated LED.	P17	38
LED1	Orange	User operated LED.	PF5	9
LED2	Red	User operated LED.	P03	4
LED3	Red	User operated LED.	P05	2

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin 141. The potentiometer can be used to create a voltage between Board_3V3 and AVSS0.
Refer to the maker site for specification of the potentiometer (VISHAY with part number TS53 series).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX671 Group User's Manual: Hardware for further details.

5.6 Pmod™

The RSK+ board is equipped with connectors for Digilent Pmod™ interface. Please connect the provided LCD module to the PMOD1 connector.

> Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible headers use an SPI interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-6 and Table 5-7** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

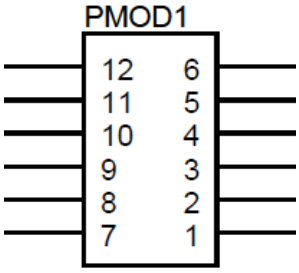

Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-6: Pmod™1 Header Connections

Pin	Pmod™ Interface			MCU	
	Type 2A (SPI)	Type 3A (UART)	Type 6A (I2C)	Port	Pin No.
1	CS	CTS/GPIO	INT	PJ3/CTS6#/IRQ11	13
2	MOSI	TXD	RESET	P00/TXD6/SMOSI6	8
				P02*2	6
3	MISO	RXD	SCL	P01/RXD6/SMISO6/SSCL6	7
4	SCK	RTS/GPIO	SDA	P02/SCK6	6
				P00/SSDA6*2	8
5	GND	GND	GND	-	-
6	3V3*1	3V3*1	3V3/5V*1	-	-
7	GPIO/INT	GPIO/INT	GPIO	P56/IRQ6	50
8	GPIO/RESET	GPIO/RESET	GPIO	P74	72
9	GPIO/CS2	GPIO	GPIO	P71	86
10	GPIO/CS3	GPIO	GPIO	P72	85
11	GND	GND	GND	-	-
12	3V3*1	3V3*1	3V3/5V*1	-	-

*1: This board allows you to choose between 3V3 and 5V, and the default RSK+ configuration is 3V3. Also, 5V can be used only when used as I2C, but signals other than I2C signals must be separated from RX671.

*2: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

Table 5-7: Pmod™2 Header Connections

Pin	Pmod™ Interface			MCU	
	Type 2A (SPI)	Type 3A (UART)	Type 6A (I2C)	Port	Pin No.
1	CS	CTS/GPIO	INT	PJ5/CTS2#/IRQ13	11
2	MOSI	TXD	RESET	P13/TXD2/SMOSI2*2	44
				P51*2	55
3	MISO	RXD	SCL	P12/RXD2/SMISO2/SSCL2*2	45
4	SCK	RTS/GPIO	SDA	P51/SCK2*2	55
				P13/SSDA2*2	44
5	GND	GND	GND	-	-
6	3V3*1	3V3*1	3V3/5V*1	-	-
7	GPIO/INT	GPIO/INT	GPIO	P82/IRQ2	63
8	GPIO/RESET	GPIO/RESET	GPIO	P90	131
9	GPIO/CS2	GPIO	GPIO	P32/TXD0*2 *3	27
10	GPIO/CS3	GPIO	GPIO	P33/RXD0*2 *3	26
11	GND	GND	GND	-	-
12	3V3*1	3V3*1	3V3/5V*1	-	-

*1: This board allows you to choose between 3V3 and 5V, and the default RSK+ configuration is 3V3. Also, 5V can be used only when used as I2C, but signals other than I2C signals must be separated from RX671.

*2: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

*3: TXD0 and RXD0 are special assignments for connecting with Renesas Silex WiFi Pmod.

5.7 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RX671 Serial Communications Interface (SCI) module. Multiple options are provided to allow the selection of the connected SCI6 port. Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-8** below.

Table 5-8: Serial Port Connections

Signal Name	Function	MCU	
		Port	Pin
SERIAL-TXD	SCI1 Transmit Signal. *1	P26	31
	SCI10 Transmit Signal.	P87	39
	External RS232 Transmit Signal. *1	-	-
SERIAL-RXD	SCI1 Receive Signal. *1	P30	29
	SCI10 Receive Signal.	P86	41
	External RS232 Receive Signal. *1	-	-
SERIAL-CTS *2	Clear To Send.	P15	42
SERIAL-RTS *2	Request To Send.	P55	51

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

*2: Flow control is a signal provided for expansion and is not currently supported. There is no schedule of function expansion at present.

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing a driver and then report that a driver has been installed successfully, as shown in **Figure 5-2**. The exact messages may vary depending upon operating system.

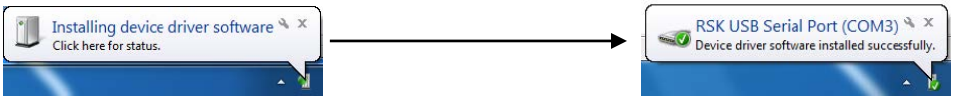

Figure 5-2: USB-Serial Windows™ Installation message

If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/document/rsk-usb-serial-driver?language=en

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the RSK+ board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX671 Group User's Manual: Hardware. The connections for the CAN microcontroller signals are listed in **Table 5-9** below.

Table 5-9: CAN Connections

CAN Signal	Function	MCU	
		Port	Pin
CAN-TX JA5-CAN1TX *1	CAN Data Transmission.	P32	27
CAN-RX JA5-CAN1RX *1	CAN Data Reception.	P33	26

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.9 Universal Serial Bus (USB)

This CPU board is fitted with a USB Host socket (type A) and a Function socket (type Mini B). USB module USB0 is connected to the Host and Function socket, and can operate as either a Host or Function device. The connection for the USB0 module is shown in **Table 5-10** below.

Table 5-10: USB0 Module Connections

USB Signal	Function	MCU	
		Port	Pin
USB0-DP	D+ I/O pin of the USB on-chip transceiver	PH1	48
USB0-DM	D– I/O pin of the USB on-chip transceiver	PH2	47
USB0-VBUS	USB cable connection monitor pin	P16	40
USB0-VBUSEN *1	VBUS (5V) supply enable signal for external power supply chip		
USB0-OVRCURA	External overcurrent detection signals A	P14	43

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.10 External Bus

The RX671 features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-11** below. Further details of the devices connected to the external bus can be found in the board schematics.

Table 5-11: External Bus Address Space

Chip Select	Device Name	Device Description	Address Space
CS0	JA3	Application Header	FF000000h – FFFFFFFFh (16Mbyte)
SDCS(SDRAM-SDCSn)	U10	128Mbit SDRAM	08000000h – 0FFFFFFFh (128Mbyte)
SDCS(JA3-CSb)	JA3	Application Header	08000000h – 0FFFFFFFh (128Mbyte)
CS1 – CS2	-	Unused	06000000h – 07FFFFFFh (2 x 16Mbyte)
CS3(JA3-CSc)	JA3	Application Header	05000000h – 05FFFFFFh (16Mbyte)
CS4 – CS7	-	Unused	01000000h – 04FFFFFFh (4 x 16Mbyte)

5.11 SDRAM

The RX671 features an SDRAM controller. It is connected to SDRAM on the CPU board with a 16-bit width. **Table 5-12** gives an Overview of the onboard SDRAM.

Table 5-12: Overview of the onboard SDRAM

Specification	Contents
Type name	MT48LC8M16A2P-6A
Constitution	2Meg x 16 x 4 bank
Capacity	128Mbit
Row address	12bit
Column address	9bit
Number of banks	4
Auto refresh period (tRFC)	Min. 60ns
Initialization auto refresh count	2
Precharge command period (tRP)	Min. 18ns
Auto refresh request interval	15.625us (64ms/4096)
CAS latency (CL)	2 or 3
Write recovery period (tWR)	Min. 12ns
ACTIVE-to-PRECHARGE command period (tRAS)	Min. 42ns
ACTIVE-to-READ or WRITE delay (tRCD)	Min. 18ns

When accessing SDRAM on the CPU board, make the following settings regardless of the operating frequency of the SDRAM clock. **Table 5-13** shows the On-board SDRAM settings.

Table 5-13: On-board SDRAM settings

Register name	Setting values	Setting details
Drive Capacity Control Register (PORTA.DSCR)	0b00000000	Normal drive output
Drive Capacity Control Register (PORTB.DSCR)		
Drive Capacity Control Register (PORTD.DSCR)		
Drive Capacity Control Register (PORTE.DSCR)		

5.12 RSPI

The RX671 features Serial Peripheral Interface (RSPId and RSPIA). RSPI0/RSPIA is connected to a 64Mbit Serial Flash. **Table 5-14** below details the connected devices, and their connections to the MCU.

Table 5-14: RSPI Connections

RSPI Signal	Function	MCU	
		Port	Pin
RSPI-CS*1	Chip Select	PA4	92
RSPI-CLK*1	Clock	PA5	90
RSPI-MOSI*1	Master out slave in data	PA6	89
RSPI-MISO*1	Master in slave out data	PA7	88

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.13 QSPIX

The RX671 features one Quad Serial Peripheral Interface (QSPIX). **Table 5-15** below details the connected device, and its connection to the MCU.

Table 5-15: QSPI Connections

QSPI signal	Function	MCU	
		Port	Pin
QSPI-CS*1	Chip Select	PD4	122
QSPI-CLK*1	Clock	PD5	121
QSPI-IO0*1	I/O Data0	PD6	120
QSPI-IO1*1	I/O Data1	PD7	119
QSPI-IO2*1	I/O Data2	PD2	124
QSPI-IO3*1	I/O Data3	PD3	123

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.14 Inter-IC Bus (I²C Bus)

The RX671 features I²C (Inter-IC Bus) interface (RIICa) and High-Speed I²C (Inter-IC Bus) Interface (RIICHS). RIIC0/RIICHS is connected to a 2Kbit EEPROM. When using RIICHS high speed mode, add 2KΩ pull-up resistors to each of the SCL and SDA lines. **Table 5-16** below details the connected device, and their connection to the MCU.

Table 5-16: I²C Bus Connections

I²C Bus signal	Function	MCU	
		Port	Pin
E2P-SDA	Data	P13	44
E2P-SCL	Clock	P12	45

5.15 SD Host Interface (SDHI)

A SD Card Slot is fitted to the CPU board, and connected to the SD Host Interface (SDHI) MCU peripheral. For further details regarding the SDHI operation, please refer to the RX671 Group User's Manual: Hardware. The connections for the SDHI signals are listed in **Table 5-17 and Table 5-18** below.

Table 5-17: SDHI Connections (1)

SD Card Slot (SDHI)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SDHI-D3*1	PD3	123	2	SDHI-CMD*1	PD4	122
3	GROUND	-	-	4	SDHI-VCC	-	-
5	SDHI-CLK*1	PD5	121	6	GROUND	-	-
7	SDHI-D0*1	PD6	120	8	SDHI-D1*1	PD7	119
9	SDHI-D2*1	PD2	124	10	SDHI-CD*1	PE6	102
11	GROUND	-	-	12	SDHI-WP*1	PE7	101

*1: This connection is a not available in the default RSK+ configuration - refer to §6 for the required modifications.

Table 5-18: SDHI Connections (2)

SDHI signal	Function	MCU	
		Port	Pin
SDHI-PE	SDHI-VCC enable control	P73	77
SDHI-POWFLT	Fault monitor of SDHI-VCC	P60	117

5.16 Serial Sound Interface (SSIE) & Audio Interface

The RX671 features an Serial Sound Interface (SSIE) module. The SSIE is connected to an audio interface. The connections for the SSIE signals are listed in **Table 5-19**, **Table 5-20** and **Table 5-21** below.

Table 5-19: SSIE Connections (Clock Generator)

SSIE Signal	Function	MCU	
		Port	Port
SSI-AUDIOCLK	Audio Clock	P22	35

Table 5-20: SSIE Connection (Audio Codec)

SSIE Signal and Miscellaneous	Function	MCU	
		Port	Port
SSI-LRCK	LR Clock	PC6	61
SSI-SCK	Bit Clock	PC5	62
SSI-TXD	Data Output	PC7	60
AUDIO-SCL	Control Interface Clock	P76	69
AUDIO-SDA	Control Interface Data	P77	68

Table 5-21: SSIE Connection (Microphone)

SSIE Signal	Function	MCU	
		Port	Port
SSI-LRCK	LR Clock	PC6	61
SSI-SCK	Bit Clock	PC5	62
SSI-RXD	Data Input	P20	37

5.17 Touch Interface

The RSK+ Board is fitted with a Touch Interface (slider x 1, key x2). The connections for the Touch Interface signals are listed in **Table 5-22** below.

Table 5-22: Touch Interface Connections

Touch Interface signal	Function	MCU	
		Port	Pin
TS6	Electrostatic capacitive measurement pin (touch slider)	P23	34
TS5	Electrostatic capacitive measurement pin (touch slider)	P24	33
TS4	Electrostatic capacitive measurement pin (touch slider)	P25	32
TS9	Electrostatic capacitive measurement pin (touch key)	P20	37
TS8	Electrostatic capacitive measurement pin (touch key)	P21	36
TSCAP	LPF (Low-pass filter) connection pin	PC4	66

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX671 Group User's Manual: Hardware and CPU board schematics for further information.

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU Operating Modes.

Table 6-1: MCU Operating Modes Switch Settings

SW4 Pin1	SW4 Pin2	J24 *1	Explanation	Related Ref.
OFF	**OFF(don't care)**	**OFF(don't care)**	**Single Chip Mode**	R256, R255
OFF	**OFF(don't care)**	**OFF(don't care)**	**FINE Boot Mode** *2	R256, R255
ON	OFF	OFF(don't care)	SCI Boot Mode	R256, R255
ON	ON	Open	USB Boot Mode (Bus-powered)	R256, R255
		Shorted	USB Boot Mode (Self-powered)	R256, R255

*1: Jumper J24 are not mounted on the board at the time of product shipment.
*2: To use the FINE interface, mode control by the E2 Lite debugger is required.

6.3 BUS Switch Configuration

Table 6-2 below details the option links associated with configuring the BUS Switch Configuration.

Table 6-2: BUS Switch Configuration

SW4 Pin3	SW4 Pin4	Available Feature
OFF	**OFF**	**SDRAM**
OFF	OFF	RSPI, QSPI
OFF	ON	N/A (Do not select)
ON	ON	RSPI, SDHI

6.4 E2 Lite Debugger Configuration

Table 6-3 below details the function of the option links associated with E2 Lite Debugger Configuration.

Table 6-3: E2 Lite Debugger Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PC7	60	PC7	**UB**	**R256**	-	**SW4.2**	-	-
						E2Lite.10	-	-
			SSI-TXD	**R255**	-	**J31.12**	-	-
TRSTn	25	P34	**TRSTn**	-	-	**E2Lite.3**	-	-
P31	28	P31	**TMS**	**R191**	**R193**	**E2Lite.9**	-	-
			JA2-CTSaRTSa	R193	R191	JA2.12	-	-
P30	29	P30	**TDI_RXD**	**R211**	**R192, R196**	**E2Lite.11**	-	-
			SERIAL-RXD	R192	R211, **R196**	U16.3	-	R88, **R91**
			JA2-RXDa	R196	R211, **R192**	JA2.8	-	-
P27	30	P27	**TCK**	**R195**	**R194**	**E2Lite.1**	**R276**	-
			JA2-SCKa	R194	R195	JA2.10	-	-
P26	31	P26	**TDO_TXD**	**R213**	**R212, R214**	**E2Lite.5**	-	-
			SERIAL-TXD	R212	R213, **R214**	U17.3	-	R87, **R90**
			JA2-TXDa	R214	R213, **R212**	JA2.6	-	-
RES#	19	-	**RESn**	-	-	**E2Lite.13**	-	-
						RES(Switch)	-	-
						JA2.1	-	-
EMLE	10	-	**EMLE**	-	-	**E2Lite.4**	-	-
						J27.2	-	-
MD_FINED	16	-	**MD_FINED**	-	-	**E2Lite.7**	-	-
						SW4.1	-	-

Table 6-4 below details the function of the jumpers associated with the E2 Lite Debugger.

Table 6-4: E2 Lite Debugger Configuration Jumper Settings

Reference	Jumper Position	Explanation	Related Ref.
J27(DNF) *1	Shorted Pin1-2	Enable E2 Lite debugging with Hot plug-in function.	-
	Shorted Pin2-3	**Enable E2 Lite normal debugging and MCU single operation (without E2 Lite).**	**R259**
	All open	DO NOT SET.	-

*1: Jumper J27 is not fitted on the default CPU board. Same as Jumper Position “shorted pin2-3” setting by resistor R259.

6.5 Power Supply Configuration

Table 6-5 below details the function of the option links associated with Power Supply Configuration.

Table 6-5: Power Supply Configuration Option Links

Reference	Explanation	Fit	DNF	Related Ref.
VBUS0	Connect 5V Power rail to VBUS0.	J25.Short, **J8.Pin1-2**	-	U8.1, U8.2
Unregulated_VCC	**Connect 5V power rail to Unregulated_VCC.**	**R251**	-	U8.1, U8.2
JA1-5V	**Connect 5V power rail to JA1-5V.**	**R250**	-	U8.1, U8.2
USB_5V	**Connect 5V power rail to USB_5V.**	**R252**	-	U15.2, U15.3
Board_5V	**Connect 5V power rail to Board_5V.**	-	-	J14, J16, R156
SD_3V3	**Connect 3.3V power rail to SD_3V3.**	**R267**	-	U11.2, U11.3
JA1-3V3	**Connect 3.3V power rail to JA1-3V3.**	**R266**	-	JA1.3
Board_3V3	**Connect 3.3V power rail to Board_3V3.**	-	-	J14, J16, R159
UC_VCC	**Connect 3.3V power rail to UC_VCC.**	J28.Short or **R268**	-	U1, R83, R176, R180, R269, J29
	Enable current probe for measurement MCU current consumption.	-	**J28.Open**, R268	U1, R83, R176, R180, R269, J29
VBATT	**Connect UC_VCC power rail to VBATT.**	**R269** or J29.Pin1-2	-	U1
	J30 connected to VBATT of MCU	J29.Pin2-3	R269	U1

Table 6-6 below details the function of the jumpers associated with the Power Supply Configuration.

Table 6-6: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Explanation	Related Ref.
J28(DNF) *1	**Shorted**	**Connect 3.3V power rail to UC_VCC.**	R268
	All open	Enable current probe for measurement MCU current consumption.	
J25(DNF) *2	Shorted	Enable VBUS0.	J8
	All open	**Disable VBUS0**	J8

*1: Jumper J28 is not fitted on the default CPU board. Fitting resistor R268 has the same effect as "shorting" jumper J28.

*2: Jumper J25 is not fitted on the default CPU board.

6.6 Clock Configuration

Table 6-7 below details the function of the option links associated with Clock Configuration.

Table 6-7: Clock Configuration Option Links

Reference	Explanation	Fit	DNF	Related Ref.
XTAL, EXTAL	**Connect 24MHz crystal (X1) to RX671.**	**R64, R85**	**R63**	U1.20, U1.22
	Connect JA2-EXTAL to RX671.	R63	R64, R85	U1.22
XCIN, XCOUT	**Connect 32.768kHz crystal (X2) to RX671.**	**R103, R104**	**R102**	U1.17, U1.18
	Disconnect X2 from RX671.	R102	R103, R104	-

6.7 Analog Power & ADC Configuration

Table 6-8 below details the function of the option links associated with Analog Power & ADC Configuration.

Table 6-8: Analog Power & ADC Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07	144	P07	**SW3**	**R142**	**R145, R184**	**SW3**	-	-
			JA1-ADTRG	R184	R142, **R145**	JA1.8	-	-
			JA1-IRQd	R145	R142, **R184**	JA1.23	-	-
P47	133	P47	**JA5-ADC7**	**R107**	**R105**	**JA5.4**	-	-
			JA1-IO3	R105	R107	JA1.18	-	-
P46	134	P46	**JA5-ADC6**	**R108**	**R106**	**JA5.3**	-	-
			JA1-IO2	R106	R108	JA1.17	-	-
P45	135	P45	**JA5-ADC5**	**R143**	**R140**	**JA5.2**	-	-
			JA1-IO1	R140	R143	JA1.16	-	-
P44	136	P44	**JA5-ADC4**	**R144**	**R141**	**JA5.1**	-	-
			JA1-IO0	R141	R144	JA1.15	-	-
P43	137	P43	**JA1-ADC3**	-	-	**JA1.12**	-	-
P42	138	P42	**JA1-ADC2**	-	-	**JA1.11**	-	-
P41	139	P41	**JA1-ADC1**	-	-	**JA1.10**	-	-
P40	141	P40	**RV1-ADC**	**R204**	**R203**	**RV1**	-	-
			JA1-ADC0	R203	R204	JA1.9	-	-
VREFH0	142	-	**UC_VCC**	**R176**	**R177**	-	-	-
			JA1-VREFH	R177	R176	JA1.7	-	-
VREFL0	140	-	**GROUND**	**R174**	**R175**	-	-	-
			JA1-AVSS	R175	R174	JA1.6	-	-
AVCC0-1	143, 3	-	**UC_VCC**	**R180**	**R179, R181**	-	-	-
			JA1-AVCC	R181	R180, **R179**	JA1.5	-	-
			Board_3V3	**R178**, R179	R180, **R181**	-	-	-
AVSS0-1	1, 5	-	**GROUND**	**R138**	**R139**	-	-	-
			JA1-AVSS	R139	R138	JA1.6	-	-

6.8 BUS & SDRAM Configuration

Table 6-9, Table 6-10, Table 6-11 and Table 6-12 below details the function of the option links associated with BUS & SDRAM Configuration.

Table 6-9: BUS & SDRAM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P54	52	P54	**JA2-M1WP**	**R166**	**R123, R167**	**JA2.17**	-	-
			JA2-TIMIN0	R123	R166, **R167**	JA2.21	-	-
			JA3-ALE	R167	R166, **R123**	JA3.46	R245	**R223**
JA3-BCLK	53	P53	**JA3-BCLK**	-	-	JA3.44	R242	**R241**
JA3-RDn	54	P52	**JA3-RDn**	-	-	**JA3.25**	-	-
P51	55	P51	PMOD2-IO3_SCK_RTS	J19.Pin1-2	R225, **R222**	PMOD2.4	-	**J20.Open**
			PMOD2-RESET0	J19.Pin2-3	R225, **R222**	PMOD2.2	**R326**	-
			JA3-WRHn	**R225**	**J19, R222**	**JA3.47**	**R247**	**R248**
			JA3-WAIT	R222	R225, **J19**	JA3.45	R244	**R243**
P50	56	P50	**JA3-WRn**	**R239**	**R240**	**JA3.26**	**R238**	**R237**
			JA3-WRLn	R240	R239	JA3.48	R246	**R224**
P67	98	P67	**SDRAM-DQMH**	**R126**	**R130**	**U10.39**	-	-
			JA3-DQMH	R130	R126	JA3.47	R248	R247
P66	99	P66	**SDRAM-DQML**	**R127**	**R131**	**U10.15**	-	-
			JA3-DQML	R131	R127	JA3.48	R224	**R246**
P65	100	P65	**SDRAM-CKE**	**R128**	**R132**	**U10.37**	-	-
			JA3-CKE	R132	R128	JA3.46	R223	**R245**
P64	112	P64	**SDRAM-WEn**	**R169**	**R133**	**U10.16**	-	-
			JA3-WEn	R133	R169	JA3.26	R237	R238
P63	113	P63	**SDRAM-CASn**	**R170**	**R134**	**U10.17**	-	-
			JA3-CAS	R134	R170	JA3.49	-	-
P62	114	P62	**SDRAM-RASn**	**R171**	**R135**	**U10.18**	-	-
			JA3-RAS	R135	R171	JA3.50	-	-
P61	115	P61	**SDRAM-SDCSn**	**R136**	**R172**	**U10.19**	-	-
			JA3-CSb	R172	R136	JA3.28	-	-
P60	117	P60	**SDHI-POWFLT**	**R137**	**R173**	**U11.5**	-	-
			JA3-CSa	R173	R137	JA3.27	-	-
P73	77	P73	**SDHI-PE**	**R36**	**R42**	**U11.4**	-	-
			JA3-CSc	R42	R36	JA3.45	R243	**R244**
P70	104	P70	**SDRAM-SDCLK**	**R235**	**R236**	**U10.38**	-	-
			JA3-SDCLK	R236	R235	JA3.44	R241	**R242**
PA7	88	PA7	**SDRAM-A7_JA3-A7**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.31**	-	-
						JA3.8	-	-
			RSPI-MISO	SW4.3.ON	-	U13.2	-	-
PA6	89	PA6	**SDRAM-A6_JA3-A6**	**SW4.3.OFF, SW4.4.OFF, R82**	**R298**	**U10.30**	-	-
						JA3.7	-	-
			RSPI-MOSI	SW4.3.ON, **R82**	**R298**	U13.5	-	-
			JA6-M1VIN	R298	R82	JA6.15	-	-
PA5	90	PA5	**SDRAM-A5_JA3-A5**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.29**	-	-
						JA3.6	-	-
			RSPI-CLK	SW4.3.ON	-	U13.6	-	-
PA4	92	PA4	**SDRAM-A4_JA3-A4**	**SW4.3.OFF, SW4.4.OFF, R99**	**R97**	**U10.26**	-	-
						JA3.5	-	-
			RSPI-CS	SW4.3.ON, **R99**	**R97**	U13.1	-	-
			JA6-M1UIN	R97	R99	JA6.14	-	-

Table 6-10: BUS & SDRAM Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SDRAM-A3_JA3-A3	94	PA3	**SDRAM-A3_JA3-A3**	-	-	**U10.25**	-	-
						JA3.4	-	-
SDRAM-A2_JA3-A2	95	PA2	**SDRAM-A2_JA3-A2**	-	-	**U10.24**	-	-
						JA3.3	-	-
PA1	96	PA1	**SDRAM-A1_JA3-A1**	**R98**	**R96**	**U10.23**	-	-
						JA3.2	-	-
			JA2-IRQb_M1HSIN1	R96	R98	JA2.9	-	-
PA0	97	PA0	**JA3-A0**	**R129**	**R125, R124**	**JA3.1**	-	-
			JA2-M1VP	R125	R129, **R124**	JA2.15	-	-
			JA2-TIMOUT0	R124	R129, **R125**	JA2.19	-	-
PB7	78	PB7	JA2-M1UP	R43	R37	JA2.13	-	-
			JA3-A15	**R37**	**R43**	**JA3.16**	-	-
PB6	79	PB6	**SDRAM-A14_JA3-A14**	**R44**	**R38**	**U10.21**	-	-
						JA3.15	-	-
			JA2-M1UN	R38	R44	JA2.14	-	-
PB5	80	PB5	**SDRAM-A13_JA3-A13**	**R45**	**R39**	**U10.20**	-	-
						JA3.14	-	-
			JA2-M1ENC	R39	R45	JA2.23	R119	**R120**
PB4	81	PB4	**SDRAM-A12_JA3-A12**	**R46**	**R40**	**U10.35**	-	-
						JA3.13	-	-
			JA6-DE011	R40	R46	JA6.21	-	-
PB3	82	PB3	**SDRAM-A11_JA3-A11**	**R41**	**R47**	**U10.22**	-	-
						JA3.12	-	-
			JA2-IRQa_M1HSIN0	R47	R41	JA2.7	-	-
SDRAM-A10_JA3-A10	83	PB2	**SDRAM-A10_JA3-A10**	-	-	**U10.34**	-	-
						JA3.11	-	-
PB1	84	PB1	**SDRAM-A9_JA3-A9**	**R78**	**R76**	**U10.33**	-	-
						JA3.10	-	-
			JA2-IRQc_M1HSIN2	R76	R78	JA2.23	R120	**R119**
PB0	87	PB0	**SDRAM-A8_JA3-A8**	**R81**	**R77**	**U10.32**	-	-
						JA3.9	-	-
			JA6-M1WIN	R77	R81	JA6.16	-	-
PC6	61	PC6	**SSI-LRCK**	**R58**	**R59**	**J31.11**	-	-
			JA3-A22	R59	R58	JA3.43	-	-
PC5	62	PC5	**SSI-SCK**	**R300**	**R301**	**J31.9**	-	-
			JA3-A21	R301	R300	JA3.42	-	-
PC4	66	PC4	**TSCAP**	**R52**	**R51**	**C86**	-	-
			JA3-A20	R51	R52	JA3.41	-	-
JA3-A19	67	PC3	**JA3-A19**	-	-	**JA3.40**	-	-
PC2	70	PC2	**JA6-TXDB011**	**R49**	**R50**	**JA6.17**	-	-
			JA3-A18	R50	R49	JA3.39	-	-
PC1	73	PC1	**JA6-TXDA011**	**R20**	**R22**	**JA6.19**	-	-
			JA3-A17	R22	R20	JA3.38	-	-
PC0	75	PC0	**JA2-M1UD**	**R21**	**R23**	**JA2.11**	-	-
			JA3-A16	R23	R21	JA3.37	-	-

Table 6-11: BUS & SDRAM Configuration Option Links (3)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PD7	119	PD7	**SDRAM-D7_JA3-D7**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.13**	-	-
						JA3.24	-	-
			QSPI-IO1	SW4.3.ON, **SW4.4.OFF**	-	U14.2	-	-
			SDHI-D1	SW4.3.ON, SW4.4.ON	-	SDHI.8	-	-
PD6	120	PD6	**SDRAM-D6_JA3-D6**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.11**	-	-
						JA3.23	-	-
			QSPI-IO0	SW4.3.ON, **SW4.4.OFF**	-	U14.5	-	-
			SDHI-D0	SW4.3.ON, SW4.4.ON	-	SDHI.7	-	-
PD5	121	PD5	**SDRAM-D5_JA3-D5**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.10**	-	-
						JA3.22	-	-
			QSPI-CLK	SW4.3.ON, **SW4.4.OFF**	-	U14.6	-	-
			SDHI-CLK	SW4.3.ON, SW4.4.ON	-	SDHI.5	-	-
PD4	122	PD4	**SDRAM-D4_JA3-D4**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.8**	-	-
						JA3.21	-	-
			QSPI-CS	SW4.3.ON, **SW4.4.OFF**	-	U14.1	-	-
			SDHI-CMD	SW4.3.ON, SW4.4.ON	-	SDHI.2	-	-
PD3	123	PD3	**SDRAM-D3_JA3-D3**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.7**	-	-
						JA3.20	-	-
			QSPI-IO3	SW4.3.ON, **SW4.4.OFF**	-	U14.7	-	-
			SDHI-D3	SW4.3.ON, SW4.4.ON	-	SDHI.1	-	-
PD2	124	PD2	**SDRAM-D2_JA3-D2**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.5**	-	-
						JA3.19	-	-
			QSPI-IO2	SW4.3.ON, **SW4.4.OFF**	-	U14.3	-	-
			SDHI-D2	SW4.3.ON, SW4.4.ON	-	SDHI.9	-	-
SDRAM-D1_JA3-D1	125	PD1	**SDRAM-D1_JA3-D1**	-	-	**U10.4**	-	-
						JA3.18	-	-
SDRAM-D0_JA3-D0	126	PD0	**SDRAM-D0_JA3-D0**	-	-	**U10.2**	-	-
						JA3.17	-	-

Table 6-12: BUS & SDRAM Configuration Option Links (4)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PE7	101	PE7	**SDRAM-D15_JA3-D15**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.53**	-	-
						JA3.36	-	-
			SDHI-WP	SW4.3.ON, SW4.4.ON	-	SDHI.12	-	-
PE6	102	PE6	**SDRAM-D14_JA3-D14**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.51**	-	-
						JA3.35	-	-
			SDHI-CD	SW4.3.ON, SW4.4.ON	-	SDHI.10	-	-
SDRAM-D13_JA3-D13	106	PE5	**SDRAM-D13_JA3-D13**	-	-	**U10.50**	-	-
						JA3.34	-	-
SDRAM-D12_JA3-D12	107	PE4	**SDRAM-D12_JA3-D12**	-	-	**U10.48**	-	-
						JA3.33	-	-
SDRAM-D11_JA3-D11	108	PE3	**SDRAM-D11_JA3-D11**	-	-	**U10.47**	-	-
						JA3.32	-	-
SDRAM-D10_JA3-D10	109	PE2	**SDRAM-D10_JA3-D10**	-	-	**U10.45**	-	-
						JA3.31	-	-
SDRAM-D9_JA3-D9	110	PE1	**SDRAM-D9_JA3-D9**	-	-	**U10.44**	-	-
						JA3.30	-	-
SDRAM-D8_JA3-D8	111	PE0	**SDRAM-D8_JA3-D8**	-	-	**U10.42**	-	-
						JA3.29	-	-

6.9 CAN Configuration

Table 6-13 below details the function of the option links associated with CAN Configuration.

Table 6-13: CAN Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P33	26	P33	**CAN-RX**	**R189** or J22.Pin1-2, **R188**	**R190**	**U12.4**	-	-
			JA5-CAN1RX	**R189** or J22.Pin1-2, R190	R188	JA5.6	-	-
			PMOD2-IO7_CS2_WIFIRXD	J22.Pin2-3	R189	PMOD2.10	-	-
P32	27	P32	**CAN-TX**	**R208** or J23.Pin1-2, **R207**	**R209**	**U12.3**	-	-
			JA5-CAN1TX	**R208** or J23.Pin1-2, R209	R207	JA5.5	-	-
			PMOD2-IO6_CS1_WIFITXD	J23.Pin2-3	R208	PMOD2.9	-	-

6.10 General IO & LED Configuration

Table 6-14 below details the function of the option links associated with General IO & LED Configuration.

Table 6-14: General IO & LED Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P05	2	P05	**LED3**	**R182**	**R185**	**LED3.K**	**R285**	-
			JA1-IO7	R185	R182	JA1.22	-	-
P03	4	P03	**LED2**	**R183**	**R186**	**LED2.K**	**R285**	-
			JA1-IO6	R186	R183	JA1.21	-	-
P17	38	P17	**LED0**	**R72**	-	**LED0.K**	**R285**	-
			JA6-M1TOGGLE	**R71**	-	**JA6.13**	-	-
P47	133	P47	**JA5-ADC7**	**R107**	**R105**	**JA5.4**	-	-
			JA1-IO3	R105	R107	JA1.18	-	-
P46	134	P46	**JA5-ADC6**	**R108**	**R106**	**JA5.3**	-	-
			JA1-IO2	R106	R108	JA1.17	-	-
P45	135	P45	**JA5-ADC5**	**R143**	**R140**	**JA5.2**	-	-
			JA1-IO1	R140	R143	JA1.16	-	-
P44	136	P44	**JA5-ADC4**	**R144**	**R141**	**JA5.1**	-	-
			JA1-IO0	R141	R144	JA1.15	-	-
P81	64	P81	**JA6-DACK**	**R56**	**R55**	**JA6.2**	-	-
			JA1-IO5	R55	R56	JA1.20	-	-
P80	65	P80	**JA6-DREQ**	**R54**	**R53**	**JA6.1**	-	-
			JA1-IO4	R53	R54	JA1.19	-	-
LED1	9	PF5	**LED1**	-	-	**LED1.K**	**R285**	-

6.11 I2C & EEPROM Configuration

Table 6-15 and Table 6-16 below detail the function of the option links associated with I2C & EEPROM Configuration.

Table 6-15: I2C & EEPROM Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P12	45	P12	**E2P-SCL**	**R152** or J21.Pin1-2, **R153**	-	**U9.6**	-	-
			JA1-SCL	**R152** or J21.Pin1-2, **R154**	-	**JA1.26**	-	-
			PMOD2-IO2_MISO_RXD_SCL	J21.Pin2-3	R152	PMOD2.3	-	-
P13	44	P13	**E2P-SDA**	**R114** or J18.Pin1-2, **R115**	-	**U9.5**	-	-
			JA1-SDA	**R114** or J18.Pin1-2, **R116**	-	**JA1.25**	-	-
			PMOD2-IO1_MOSI_TXD	J18.Pin2-3, J17.Pin1-2	R114	PMOD2.2	**R326,** J19.Pin1-2	R225, **R222**
			PMOD2-SDA	J18.Pin2-3, J17.Pin2-3	R114	PMOD2.4	J20.Short, J19.Pin2-3	R225, **R222**

Table 6-16: I2C & EEPROM Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
E2P-SDA, E2P-SCL	**Connect pull-up resistor to Board_3V3.**	**R159**	**R156**	U9
	Connect pull-up resistor to Board_5V.	R156	R159	U9
WP	EEPROM Write protect.	R157	-	U9
A0, A1, A2	**Device address (0xA6).**	**R329, R328, R160**	**R162, R161, R327**	U9
	Device address (0xA4).	R162, **R328, R160**	R329, **R161, R327**	U9

6.12 IRQ & Switch Configuration

Table 6-17 below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-17: IRQ & Switch Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P07	144	P07	**SW3**	**R142**	**R145, R184**	**SW3**	-	-
			JA1-ADTRG	R184	R142, **R145**	JA1.8	-	-
			JA1-IRQd	R145	R142, **R184**	JA1.23	-	-
P35	24	P35	**JP-UPSEL**	**R217**	-	**J24.2**	-	-
			JA2-NMIn	**R216**	-	**JA2.3**	-	-
SW2	128	P92	**SW2**	**-**	-	**SW2**	-	-
SW1	129	P91	**SW1**	**-**	-	**SW1**	-	-
PA1	96	PA1	**SDRAM-A1_JA3-A1**	**R98**	**R96**	**U10.23**	-	-
						JA3.2	-	-
			JA2-IRQb_M1HSIN1	R96	R98	JA2.9	-	-
PB3	82	PB3	**SDRAM-A11_JA3-A11**	**R41**	**R47**	**U10.22**	-	-
						JA3.12	-	-
			JA2-IRQa_M1HSIN0	R47	R41	JA2.7	-	-
PB1	84	PB1	**SDRAM-A9_JA3-A9**	**R78**	**R76**	**U10.33**	-	-
						JA3.10	-	-
			JA2-IRQc_M1HSIN2	R76	R78	JA2.23	R120	**R119**
RES#	19	-	**RESn**	-	-	**E2Lite.13**	-	-
						RES(Switch)	-	-
						JA2.1	-	-

6.13 MTU & POE Configuration

Table 6-18 and Table 6-19 below details the function of the option links associated with MTU & POE Configuration.

Table 6-18: MTU & POE Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P17	38	P17	**LED0**	**R72**	-	**LED0.K**	**R285**	-
			JA6-M1TOGGLE	**R71**	**-**	**JA6.13**	-	-
P15	42	P15	**JA2-M1TRDCLK**	**R118**	**R117**	**JA2.26**	-	-
			SERIAL-CTS	R117	R118	U16.2	-	-
P14	43	P14	**USB0-OVRCURA**	**R121**	**R122**	**U15.5**	-	-
			JA2-M1TRCCLK	R122	R121	JA2.25	-	-
P55	51	P55	**JA2-M1WN**	**R164**	**R163, R165**	**JA2.18**	-	-
			JA2-TIMIN1	R163	R164, **R165**	JA2.22	-	-
			SERIAL-RTS	R165	R164, **R163**	U17.2	-	-
P54	52	P54	**JA2-M1WP**	**R166**	**R123, R167**	**JA2.17**	-	-
			JA2-TIMIN0	R123	R166, **R167**	JA2.21	-	-
			JA3-ALE	R167	R166, **R123**	JA3.46	R245	**R223**
P83	58	P83	**JA2-M1VN**	**R68**	**R69, R70**	**JA2.16**	-	-
			JA2-TIMOUT1	R69	**R68**, R70	JA2.20	-	-
			JA6-SCKb	R70	**R68**, R69	JA6.10	-	-
JA2-M1POE	127	P93	**JA2-M1POE**	-	-	**JA2.24**	-	-

Table 6-19: MTU & POE Configuration Option Links (2)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PA6	89	PA6	**SDRAM-A6_JA3-A6**	**SW4.3.OFF, SW4.4.OFF, R82**	**R298**	**U10.30**	-	-
						JA3.7	-	-
			RSPI-MOSI	SW4.3.ON, **R82**	**R298**	U13.5	-	-
			JA6-M1VIN	R298	R82	JA6.15	-	-
PA4	92	PA4	**SDRAM-A4_JA3-A4**	**SW4.3.OFF, SW4.4.OFF, R99**	**R97**	**U10.26**	-	-
						JA3.5	-	-
			RSPI-CS	SW4.3.ON, **R99**	**R97**	U13.1	-	-
			JA6-M1UIN	R97	R99	JA6.14	-	-
PA1	96	PA1	**SDRAM-A1_JA3-A1**	**R98**	**R96**	**U10.23**	-	-
						JA3.2	-	-
			JA2-IRQb_M1HSIN1	R96	R98	JA2.9	-	-
PA0	97	PA0	**JA3-A0**	**R129**	**R125, R124**	**JA3.1**	-	-
			JA2-M1VP	R125	R129, **R124**	JA2.15	-	-
			JA2-TIMOUT0	R124	R129, **R125**	JA2.19	-	-
PB7	78	PB7	JA2-M1UP	R43	R37	JA2.13	-	-
			JA3-A15	**R37**	**R43**	**JA3.16**	-	-
PB6	79	PB6	**SDRAM-A14_JA3-A14**	**R44**	**R38**	**U10.21**	-	-
						JA3.15	-	-
			JA2-M1UN	R38	R44	JA2.14	-	-
PB5	80	PB5	**SDRAM-A13_JA3-A13**	**R45**	**R39**	**U10.20**	-	-
						JA3.14	-	-
			JA2-M1ENC	R39	R45	JA2.23	R119	**R120**
PB3	82	PB3	**SDRAM-A11_JA3-A11**	**R41**	**R47**	**U10.22**	-	-
						JA3.12	-	-
			JA2-IRQa_M1HSIN0	R47	R41	JA2.7	-	-
PB1	84	PB1	**SDRAM-A9_JA3-A9**	**R78**	**R76**	**U10.33**	-	-
						JA3.10	-	-
			JA2-IRQc_M1HSIN2	R76	R78	JA2.23	R120	**R119**
PB0	87	PB0	**SDRAM-A8_JA3-A8**	**R81**	**R77**	**U10.32**	-	-
						JA3.9	-	-
			JA6-M1WIN	R77	R81	JA6.16	-	-
PC0	75	PC0	**JA2-M1UD**	**R21**	**R23**	**JA2.11**	-	-
			JA3-A16	R23	R21	JA3.37	-	-

6.14 PMOD1 Configuration

Table 6-20 and Table 6-21 below details the function of the option links associated with PMOD1 Configuration.

Table 6-20: PMOD1 Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P02	6	P02	**PMOD1-IO3_SCK_RTS**	**R2** or J6.Pin1-2	-	**PMOD1.4**	-	**J9.Open**
			PMOD1-RESET0	J6.Pin2-3	R2	PMOD1.2	**R287**	-
P01	7	P01	**PMOD1-IO2_MISO_RXD**	**R66** or J15.Pin1-2	-	**PMOD1.3**	-	**J10.Open**
			PMOD1-SCL	J15.Pin2-3	R66	PMOD1.3	J10.Short	-
P00	8	P00	**PMOD1-IO1_MOSI_TXD**	**R31** or J12.Pin1-2	-	**PMOD1.2**	**R287, R2** or J6.Pin1-2	-
			PMOD1-SDA	J12.Pin2-3	R31	PMOD1.4	J9.Short, J6.Pin2-3	R2
PMOD1-IO4_INT1	50	P56	**PMOD1-IO4_INT1**	-	-	**PMOD1.7**	-	-
PMOD1-IO5_RESET1	72	P74	**PMOD1-IO5_RESET1**	-	-	**PMOD1.8**	-	-
PMOD1-IO7_CS2	85	P72	**PMOD1-IO7_CS2**	-	-	**PMOD1.10**	-	-
PMOD1-IO6_CS1	86	P71	**PMOD1-IO6_CS1**	-	-	**PMOD1.9**	-	-
PMOD1-IO0_CS0_INT0	13	PJ3	**PMOD1-IO6_CS1**	-	-	**PMOD1.1**	-	-

Table 6-21: PMOD1 Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
Pmod1_VCC	**Connect to Board_3V3.**	**R65** or J14.Pin1-2	-	PMOD1
	Connect to Board_5V.	J14.Pin2-3	R65	PMOD1

6.15 PMOD2 Configuration

Table 6-22 and Table 6-23 below details the function of the option links associated with PMOD2 Configuration.

Table 6-22: PMOD2 Configuration Option Links (1)

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P13	44	P13	**E2P-SDA**	**R114** or J18.Pin1-2, **R115**	-	**U9.5**	-	-
			JA1-SDA	**R114** or J18.Pin1-2, **R116**	-	**JA1.25**	-	-
			PMOD2-IO1_MOSI_TXD	J18.Pin2-3, J17.Pin1-2	R114	PMOD2.2	**R326,** J19.Pin1-2	R225, **R222**
			PMOD2-SDA	J18.Pin2-3, J17.Pin2-3	R114	PMOD2.4	J20.Short, J19.Pin2-3	R225, **R222**
P12	45	P12	**E2P-SCL**	**R152** or J21.Pin1-2, **R153**	-	**U9.6**	-	-
			JA1-SCL	**R152** or J21.Pin1-2, **R154**	-	**JA1.26**	-	-
			PMOD2-IO2_MISO_RXD_SCL	J21.Pin2-3	R152	PMOD2.3	-	-
P33	26	P33	**CAN-RX**	**R189** or J22.Pin1-2, **R188**	**R190**	**U12.4**	-	-
			JA5-CAN1RX	**R189** or J22.Pin1-2, R190	R188	JA5.6	-	-
			PMOD2-IO7_CS2_WIFIRXD	J22.Pin2-3	R189	PMOD2.10	-	-
P32	27	P32	**CAN-TX**	**R208** or J23.Pin1-2, **R207**	**R209**	**U12.3**	-	-
			JA5-CAN1TX	**R208** or J23.Pin1-2, R209	R207	JA5.5	-	-
			PMOD2-IO6_CS1_WIFITXD	J23.Pin2-3	R208	PMOD2.9	-	-
P51	55	P51	PMOD2-IO3_SCK_RTS	J19.Pin1-2	R225, **R222**	PMOD2.4	-	**J20.Open**
			PMOD2-RESET0	J19.Pin2-3	R225, **R222**	PMOD2.2	**R326**	-
			JA3-WRHn	**R225**	**J19, R222**	**JA3.47**	**R247**	**R248**
			JA3-WAIT	R222	R225, **J19**	JA3.45	R244	**R243**
PMOD2-IO4_INT1_WIFIWKUP	63	P82	**PMOD2-IO4_INT1_WIFIWKUP**	-	-	**PMOD2.7**	-	-
PMOD2-IO5_RESET1_WIFIMDRES	131	P90	**PMOD2-IO5_RESET1_WIFIMDRES**	-	-	**PMOD2.8**	-	-
PMOD2-IO0_CS0_INT0	11	PJ5	**PMOD2-IO0_CS0_INT0**	-	-	**PMOD2.1**	-	-

Table 6-23: PMOD2 Configuration Option Links (2)

Reference	Explanation	Fit	DNF	Related Ref.
Pmod2_VCC	**Connect to Board_3V3.**	**R86** or J16.Pin1-2	-	PMOD2
	Connect to Board_5V.	J16.Pin2-3	R86	PMOD2

6.16 QSPIX Configuration

Table 6-24 below details the function of the option links associated with QSPIX Configuration.

Table 6-24: QSPIX Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PD7	119	PD7	**SDRAM-D7_JA3-D7**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.13**	-	-
						JA3.24	-	-
			QSPI-IO1	SW4.3.ON, **SW4.4.OFF**	-	U14.2	-	-
			SDHI-D1	SW4.3.ON, SW4.4.ON	-	SDHI.8	-	-
PD6	120	PD6	**SDRAM-D6_JA3-D6**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.11**	-	-
						JA3.23	-	-
			QSPI-IO0	SW4.3.ON, **SW4.4.OFF**	-	U14.5	-	-
			SDHI-D0	SW4.3.ON, SW4.4.ON	-	SDHI.7	-	-
PD5	121	PD5	**SDRAM-D5_JA3-D5**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.10**	-	-
						JA3.22	-	-
			QSPI-CLK	SW4.3.ON, **SW4.4.OFF**	-	U14.6	-	-
			SDHI-CLK	SW4.3.ON, SW4.4.ON	-	SDHI.5	-	-
PD4	122	PD4	**SDRAM-D4_JA3-D4**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.8**	-	-
						JA3.21	-	-
			QSPI-CS	SW4.3.ON, **SW4.4.OFF**	-	U14.1	-	-
			SDHI-CMD	SW4.3.ON, SW4.4.ON	-	SDHI.2	-	-
PD3	123	PD3	**SDRAM-D3_JA3-D3**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.7**	-	-
						JA3.20	-	-
			QSPI-IO3	SW4.3.ON, **SW4.4.OFF**	-	U14.7	-	-
			SDHI-D3	SW4.3.ON, SW4.4.ON	-	SDHI.1	-	-
PD2	124	PD2	**SDRAM-D2_JA3-D2**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.5**	-	-
						JA3.19	-	-
			QSPI-IO2	SW4.3.ON, **SW4.4.OFF**	-	U14.3	-	-
			SDHI-D2	SW4.3.ON, SW4.4.ON	-	SDHI.9	-	-

6.17 RSPI Configuration

Table 6-25 below details the function of the option links associated with RSPI Configuration.

Table 6-25: RSPI Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PA7	88	PA7	**SDRAM-A7_JA3-A7**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.31**	-	-
						JA3.8	-	-
			RSPI-MISO	SW4.3.ON	-	U13.2	-	-
PA6	89	PA6	**SDRAM-A6_JA3-A6**	**SW4.3.OFF, SW4.4.OFF, R82**	**R298**	**U10.30**	-	-
						JA3.7	-	-
			RSPI-MOSI	SW4.3.ON, **R82**	**R298**	U13.5	-	-
			JA6-M1VIN	R298	R82	JA6.15	-	-
PA5	90	PA5	**SDRAM-A5_JA3-A5**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.29**	-	-
						JA3.6	-	-
			RSPI-CLK	SW4.3.ON	-	U13.6	-	-
PA4	92	PA4	**SDRAM-A4_JA3-A4**	**SW4.3.OFF, SW4.4.OFF, R99**	**R97**	**U10.26**	-	-
						JA3.5	-	-
			RSPI-CS	SW4.3.ON, **R99**	**R97**	U13.1	-	-
			JA6-M1UIN	R97	R99	JA6.14	-	-

6.18 SDHI Configuration

Table 6-26 below details the function of the option links associated with SDHI Configuration.

Table 6-26: SDHI Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P60	117	P60	**SDHI-POWFLT**	**R137**	**R173**	**U11.5**	-	-
			JA3-CSa	R173	R137	JA3.27	-	-
P73	77	P73	**SDHI-PE**	**R36**	**R42**	**U11.4**	-	-
			JA3-CSc	R42	R36	JA3.45	R243	**R244**
PD7	119	PD7	**SDRAM-D7_JA3-D7**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.13**	-	-
						JA3.24	-	-
			QSPI-IO1	SW4.3.ON, **SW4.4.OFF**	-	U14.2	-	-
			SDHI-D1	SW4.3.ON, SW4.4.ON	-	SDHI.8	-	-
PD6	120	PD6	**SDRAM-D6_JA3-D6**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.11**	-	-
						JA3.23	-	-
			QSPI-IO0	SW4.3.ON, **SW4.4.OFF**	-	U14.5	-	-
			SDHI-D0	SW4.3.ON, SW4.4.ON	-	SDHI.7	-	-
PD5	121	PD5	**SDRAM-D5_JA3-D5**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.10**	-	-
						JA3.22	-	-
			QSPI-CLK	SW4.3.ON, **SW4.4.OFF**	-	U14.6	-	-
			SDHI-CLK	SW4.3.ON, SW4.4.ON	-	SDHI.5	-	-
PD4	122	PD4	**SDRAM-D4_JA3-D4**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.8**	-	-
						JA3.21	-	-
			QSPI-CS	SW4.3.ON, **SW4.4.OFF**	-	U14.1	-	-
			SDHI-CMD	SW4.3.ON, SW4.4.ON	-	SDHI.2	-	-
PD3	123	PD3	**SDRAM-D3_JA3-D3**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.7**	-	-
						JA3.20	-	-
			QSPI-IO3	SW4.3.ON, **SW4.4.OFF**	-	U14.7	-	-
			SDHI-D3	SW4.3.ON, SW4.4.ON	-	SDHI.1	-	-
PD2	124	PD2	**SDRAM-D2_JA3-D2**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.5**	-	-
						JA3.19	-	-
			QSPI-IO2	SW4.3.ON, **SW4.4.OFF**	-	U14.3	-	-
			SDHI-D2	SW4.3.ON, SW4.4.ON	-	SDHI.9	-	-
PE7	101	PE7	**SDRAM-D15_JA3-D15**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.53**	-	-
						JA3.36	-	-
			SDHI-WP	SW4.3.ON, SW4.4.ON	-	SDHI.12	-	-
PE6	102	PE6	**SDRAM-D14_JA3-D14**	**SW4.3.OFF, SW4.4.OFF**	-	**U10.51**	-	-
						JA3.35	-	-
			SDHI-CD	SW4.3.ON, SW4.4.ON	-	SDHI.10	-	-

6.19 Serial & USB to Serial Configuration

Table 6-27 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-27: Serial & USB to Serial Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P15	42	P15	**JA2-M1TRDCLK**	**R118**	**R117**	**JA2.26**	-	-
			SERIAL-CTS	R117	R118	U16.2	-	-
P27	30	P27	**TCK**	**R195**	**R194**	**E2Lite.1**	**R276**	-
			JA2-SCKa	R194	R195	JA2.10	-	-
P26	31	P26	**TDO_TXD**	**R213**	**R212, R214**	**E2Lite.5**	-	-
			SERIAL-TXD	R212	R213, **R214**	U17.3	-	R87, **R90**
			JA2-TXDa	R214	R213, **R212**	JA2.6	-	-
P31	28	P31	**TMS**	**R191**	**R193**	**E2Lite.9**	-	-
			JA2-CTSaRTSa	R193	R191	JA2.12	-	-
P30	29	P30	**TDI_RXD**	**R211**	**R192, R196**	**E2Lite.11**	-	-
			SERIAL-RXD	R192	R211, **R196**	U16.3	-	R88, **R91**
			JA2-RXDa	R196	R211, **R192**	JA2.8	-	-
P55	51	P55	**JA2-M1WN**	**R164**	**R163, R165**	**JA2.18**	-	-
			JA2-TIMIN1	R163	R164, **R165**	JA2.22	-	-
			SERIAL-RTS	R165	R164, **R163**	U17.2	-	-
P77	68	P77	**AUDIO-SDA**	**R361**	**R362**	**U20.18**	-	-
			JA6-TXDc	R362	R361	JA6.9	-	-
P76	69	P76	**AUDIO-SCL**	**R363**	**R364**	**U20.17**	-	-
			JA6-RXDc	R364	R363	JA6.12	-	-
JA6-SCKc	71	P75	**JA6-SCKc**	-	-	**JA6.11**	-	-
P87	39	P87	**SERIAL-TXD**	**R87**	**R89**	**U17.3**	-	**R90, R212**
			JA6-TXDb	R89	R87	JA6.8	-	-
P86	41	P86	**SERIAL-RXD**	**R88**	**R92**	**U16.3**	-	**R91, R192**
			JA6-RXDb	R92	R88	JA6.7	-	-
P83	58	P83	**JA2-M1VN**	**R68**	**R69, R70**	**JA2.16**	-	-
			JA2-TIMOUT1	R69	**R68**, R70	JA2.20	-	-
			JA6-SCKb	R70	**R68**, R69	JA6.10	-	-
PB4	81	PB4	**SDRAM-A12_JA3-A12**	**R46**	**R40**	**U10.35**	-	-
						JA3.13	-	-
			JA6-DE011	R40	R46	JA6.21	-	-
PC2	70	PC2	**JA6-TXDB011**	**R49**	**R50**	**JA6.17**	-	-
			JA3-A18	R50	R49	JA3.39	-	-
PC1	73	PC1	**JA6-TXDA011**	**R20**	**R22**	**JA6.19**	-	-
			JA3-A17	R22	R20	JA3.38	-	-
-	-	-	JA6-RS232RX	R91	**-**	U16.3	-	R88, **R192**
-	-	-	JA6-RS232TX	R90	**-**	U17.3	-	R87, **R212**

6.20 SSIE & Audio Interface Configuration

Table 6-28 below details the function of the option links associated with SSIE & Audio Interface Configuration.

Table 6-28: SSIE & Audio Interface Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SSI-AUDIOCLK	35	P22	**SSI-AUDIOCLK**	-	-	**J31.5**	-	-
P20	37	P20	**TS9**	**J11.Pin1-2**	**-**	**KEY1**	-	-
			SSI-RXD	J11.Pin2-3	-	J31.10	-	-
P77	68	P77	**AUDIO-SDA**	**R361**	**R362**	**U20.18**	-	-
			JA6-TXDc	R362	R361	JA6.9	-	-
P76	69	P76	**AUDIO-SCL**	**R363**	**R364**	**U20.17**	-	-
			JA6-RXDc	R364	R363	JA6.12	-	-
PC7	60	PC7	**UB**	**R256**	-	**SW4.2**	-	-
						E2Lite.10	-	-
			SSI-TXD	**R255**	-	**J31.12**	-	-
PC6	61	PC6	**SSI-LRCK**	**R58**	**R59**	**J31.11**	-	-
			JA3-A22	R59	R58	JA3.43	-	-
PC5	62	PC5	**SSI-SCK**	**R300**	**R301**	**J31.9**	-	-
			JA3-A21	R301	R300	JA3.42	-	-

6.21 Touch Interface Configuration

Table 6-29 below details the function of the option links associated with Touch Interface Configuration.

Table 6-29: Touch Interface Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TS4	32	P25	**TS4**	-	-	**SLIDER1.S3**	-	-
TS5	33	P24	**TS5**	-	-	**SLIDER1.S2**	-	-
TS6	34	P23	**TS6**	-	-	**SLIDER1.S3**	-	-
TS8	36	P21	**TS8**	-	-	**KEY2**	-	-
P20	37	P20	**TS9**	**J11.Pin1-2**	**-**	**KEY1**	-	-
			SSI-RXD	J11.Pin2-3	-	J31.10	-	-
PC4	66	PC4	**TSCAP**	**R52**	**R51**	**C86**	-	-
			JA3-A20	R51	R52	JA3.41	-	-

6.22 USB Configuration

Table 6-30 below details the function of the option links associated with the USB Configuration.

Table 6-30: USB Configuration Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P16	40	P16	**USB0-VBUS**	**J13.Pin1-2**	-	**USB0_2.1 (Self-powered)**	**J8.Pin1-2, R15** or J7.Pin1-2, **J25.Open**	-
						Board_3V3 (Bus-powered)	**J8.Pin1-2,** J7.Pin2-3, J25.Short	R15
			USB0-VBUSEN	J13.Pin2-3	-	U15.4	-	-
P14	43	P14	**USB0-OVRCURA**	**R121**	**R122**	**U15.5**	-	-
			JA2-M1TRCCLK	R122	R121	JA2.25	-	-
P35	24	P35	**JP-UPSEL**	**R217**	-	**J24.2**	-	-
			JA2-NMIn	**R216**	-	**JA2.3**	-	-
USB0-DP	48	PH1	**USB0-DP**	-	-	**USB0_1.3**	-	-
						USB0_2.3	-	-
USB0-DN	47	PH2	**USB0-DN**	-	-	**USB0_1.2**	-	-
						USB0_2.2	-	-

Table 6-31 below details the function of the jumpers associated with the USB Configuration.

Table 6-31: USB Configuration Jumper Option Links

Reference	Jumper Position	Explanation	Related Ref.
J7(DNF)	Shorted Pin1-2	Self-powered	J8, J25, R15
	Shorted Pin2-3	Bus-powered	J8, J25, R15
	All open	**Self-powered by R15**	J8, J25, R15
J8	**Shorted Pin1-2**	**USB0 Function mode**	J7
	Shorted Pin2-3	USB0 Host mode	-
	All open	DO NOT SET.	-
J25	**Open**	**Disconnect VBUS0 from 5V Power rail.**	J7, R15
	Shorted Pin	Connect 5V Power rail to VBUS0.	J7, R15

6.23 Other Function Configurations

Table 6-32 below details the function of the option links associated with the Other Function Configurations.

Table 6-32: Other Function Configurations Option Links

Signal name	MCU		MCU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P81	64	P81	**JA6-DACK**	**R56**	**R55**	**JA6.2**	-	-
			JA1-IO5	R55	R56	JA1.20	-	-
P80	65	P80	**JA6-DREQ**	**R54**	**R53**	**JA6.1**	-	-
			JA1-IO4	R53	R54	JA1.19	-	-

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Table 7-1: Application Header JA1 Connections

Application Header JA1					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	5V JA1-5V	-	2	0V GROUND	-
3	3V3 JA1-3V3	-	4	0V GROUND	-
5	AVCC JA1-AVCC	3, 143	6	AVSS JA1-AVSS	1, 5, 140
7	AVREF JA1-VREFH	142	8	ADTRG JA1-ADTRG	144
9	ADC0 JA1-ADC0	141	10	ADC1 JA1-ADC1	139
11	ADC2 JA1-ADC2	138	12	ADC3 JA1-ADC3	137
13	DAC0 NC	NC	14	DAC1 NC	NC
15	IO_0 JA1-IO0	136	16	IO_1 JA1-IO1	135
17	IO_2 JA1-IO2	134	18	IO_3 JA1-IO3	133
19	IO_4 JA1-IO4	65	20	IO_5 JA1-IO5	64
21	IO_6 JA1-IO6	4	22	IO_7 JA1-IO7	2
23	IRQd / IRQAEC / M2_HSIN0 JA1-IRQd	144 / NC / 144	24	IIC_EX NC	NC
25	IIC_SDA JA1-SDA	44	26	IIC_SCL JA1-SCL	45

Table 7-2 below lists the connections of the application header, JA2.

Table 7-2: Application Header JA2 Connections

Application Header JA2					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	RESET RESn	19	2	EXTAL JA2-EXTAL	22
3	NMI JA2-NMIn	24	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX JA2-TXDa	31
7	IRQa / WKUP / M1_HSIN0 JA2-IRQa_M1HSIN0	82 / NC / 82	8	SCIaRX JA2-RXDa	29
9	IRQb / M1_HSIN1 JA2-IRQb_M1HSIN1	96 / 96	10	SCIaCK JA2-SCKa	30
11	M1_UD JA2-M1UD	75	12	CTSaRTSa JA2-CTSaRTSa	28
13	M1_UP JA2-M1UP	78	14	M1_UN JA2-M1UN	79
15	M1_VP JA2-M1VP	97	16	M1_VN JA2-M1VN	58
17	M1_WP JA2-M1WP	52	18	M1_WN JA2-M1WN	51
19	TimerOut0 JA2-TIMOUT0	97	20	TimerOut1 JA2-TIMOUT1	58
21	TimerIn0 JA2-TIMIN0	52	22	TimerIn1 JA2-TIMIN1	51
23	IRQc / M1_EncZ / M1_HSIN2 JA2-23PIN	84 / 80 / 84	24	M1_POE JA2-M1POE	127
25	M1_TRCCLK JA2-M1TRCCLK	43	26	M1_TRDCLK JA2-M1TRDCLK	42

Table 7-3 below lists the connections of the BUS application header, JA3.

Table 7-3: Application Header JA3 Connections

Application Header JA3 (Bus)					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	A0 JA3-A0	97	2	A1 SDRAM-A1_JA3-A1	96
3	A2 SDRAM-A2_JA3-A2	95	4	A3 SDRAM-A3_JA3-A3	94
5	A4 SDRAM-A4_JA3-A4	92	6	A5 SDRAM-A5_JA3-A5	90
7	A6 SDRAM-A6_JA3-A6	89	8	A7 SDRAM-A7_JA3-A7	88
9	A8 SDRAM-A8_JA3-A8	87	10	A9 SDRAM-A9_JA3-A9	84
11	A10 SDRAM-A10_JA3-A10	83	12	A11 SDRAM-A11_JA3-A11	82
13	A12 SDRAM-A12_JA3-A12	81	14	A13 SDRAM-A13_JA3-A13	80
15	A14 SDRAM-A14_JA3-A14	79	16	A15 JA3-A15	78
17	D0 SDRAM-D0_JA3-D0	126	18	D1 SDRAM-D1_JA3-D1	125
19	D2 SDRAM-D2_JA3-D2	124	20	D3 SDRAM-D3_JA3-D3	123
21	D4 SDRAM-D4_JA3-D4	122	22	D5 SDRAM-D5_JA3-D5	121
23	D6 SDRAM-D6_JA3-D6	120	24	D7 SDRAM-D7_JA3-D7	119
25	RDn JA3-RDn	54	26	WR / SDWE JA3-26PIN	56 / 112
27	CSa JA3-CSa	117	28	CSb [*1] JA3-CSb	115
29	D8 SDRAM-D8_JA3-D8	111	30	D9 SDRAM-D9_JA3-D9	110
31	D10 SDRAM-D10_JA3-D10	109	32	D11 SDRAM-D11_JA3-D11	108
33	D12 SDRAM-D12_JA3-D12	107	34	D13 SDRAM-D13_JA3-D13	106
35	D14 SDRAM-D14_JA3-D14	102	36	D15 SDRAM-D15_JA3-D15	101
37	A16 JA3-A16	75	38	A17 JA3-A17	73
39	A18 JA3-A18	70	40	A19 JA3-A19	67
41	A20 JA3-A20	66	42	A21 JA3-A21	62
43	A22 JA3-A22	61	44	SDCLK [*2] JA3-44PIN	53 / 104
45	CSc / Wait JA3-45PIN	77 / 55	46	ALE / SDCKE JA3-46PIN	52 / 100
47	HWRn / DQMH JA3-47PIN	55 / 98	48	LWRn / DQML JA3-48PIN	56 / 99
49	CAS JA3-CAS	113	50	RAS JA3-RAS	114

[*1]: The chip select signal assigned on this board can also be used as a SDRAM chip select.
[*2]: This board can also output BCLK signal to JA3 header.

Table 7-4 below lists the connections of the application header, JA5.

Table 7-4: Application Header JA5 Connections

Application Header JA5					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	ADC4 JA5-ADC4	136	2	ADC5 JA5-ADC5	135
3	ADC6 JA5-ADC6	134	4	ADC7 JA5-ADC7	133
5	CAN1TX JA5-CAN1TX	27	6	CAN1RX JA5-CAN1RX	26
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 NC	NC / NC / NC	10	IRQf / M2_HSIN2 NC	NC / NC
11	M2_UD NC	NC	12	M2_Uin NC	NC
13	M2_Vin NC	NC	14	M2_Win NC	NC
15	M2_Toggle NC	NC	16	M2_POE NC	NC
17	M2_TRCCLK NC	NC	18	M2_TRDCLK NC	NC
19	M2_UP NC	NC	20	M2_Un NC	NC
21	M2_VP NC	NC	22	M2_Vn NC	NC
23	M2_WP NC	NC	24	M2_Wn NC	NC

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MCU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MCU Pin**
1	DREQ JA6-DREQ	65	2	DACK JA6-DACK	64
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX JA6-RS232TX	NC	6	RS232RX JA6-RS232RX	NC
7	SCIbRX JA6-RXDb	41	8	SCIbTX JA6-TXDb	39
9	SCIcTX JA6-TXDc	68	10	SCIbCK JA6-SCKb	58
11	SCIcCK JA6-SCKc	71	12	SCIcRX JA6-RXDc	69
13	M1_Toggle JA6-M1TOGGLE	38	14	M1_Uin JA6-M1UIN	92
15	M1_Vin JA6-M1VIN	89	16	M1_Win JA6-M1WIN	87
17	Features for RX671 only JA6-TXDB011	70	18	Reserved NC	NC
19	Features for RX671 only JA6-TXDA011	73	20	Reserved NC	NC
21	Features for RX671 only JA6-DE011	81	22	Reserved NC	NC
23	Unregulated_VCC Unregulated_VCC	-	24	Vss GROUND	-

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via an E2 Lite debugger. An E2 Lite debugger is supplied with this RSK+ product.

For further information regarding the debugging capabilities of the E2 Lite debuggers, refer to E1/E20 Emulator, E2 Emulator Lite Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK+ is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot Modes (SCI and USB and FINE), which are configured on the RSK+ board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU’s registers, which are listed in the RX671 Group User’s Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK+ is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E2 Emulator Lite (as supplied with this RSK+) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer E2 Emulator Lite User’s Manual (R20UT3240EJ).

8.5 Address Space

For the MCU address space details, refer to the ’Address Space’ section of RX671 Group User’s Manual: Hardware.

8.6 Note of Flash Access Window Setting Register

This register is used to set the write protection flag and start-up area select flag for setting the flash access window start address, flash access window end address, and access window.

Once 0 is written to this bit, the bit can never be restored to 1.
Therefore, the access window and the BTFLG bit will never be set again. If set the TM function will never be disabled, once enabled. Exercise extra caution when handling the FSPR bit.

For details, refer to Section 7.2.9 in the RX671 Group User’s Manual: Hardware.

9. Additional Information

Technical Support

For information about the RX671 Group microcontrollers refer to the ‘RX671 Group Manual: Hardware’.

For information about the RX assembly language, refer to the ‘RX Family User’s Manual: Software’.

Technical Contact Details

Please refer to the contact details listed in section 8 of the “*Quick Start Guide*”

General information on Renesas microcontrollers can be found on the Renesas website at:
https://www.renesas.com/

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