User's Manual

R-IN32M4-CL2

User's Manual Gigabit Ethernet PHY Edition

R9J03G019GBG

Document number: R18UZ0043EJ0100
Issue date: Mar 4, 2016

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The following usage notes are applicable to CMOS devices from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

How to Use This Manual

1. Purpose and Target Readers

This manual is intended for users who wish to understand the functions of industrial Ethernet communications ASSP (Application Specific Standard Product) “R-IN32M4-CL2” (R9J03G019GBG) and design application systems using it.
Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.

When designing an application system that includes this MCU, take all points to note into account. Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual. The mark “<R>” in the text indicates the major revisions to this version. You can easily find these revisions by copying “<R>” and entering it in the search-string box for the PDF file.

Literature — Literature may be preliminary versions. Note, however, that the following descriptions do not indicate "Preliminary". Some documents on cores were created when they were planned or still under development. So, they may be directed to specific customers. Last four digits of document number (described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

Documents related to R-IN32M4-CL2

Document Name	Document Number
R-IN32M4-CL2 User’s Manual	R18UZ0033EJ****
R-IN32M4-CL2 User’s Manual: Peripheral Modules	R18UZ0035EJ****
R-IN32M4-CL2 User’s Manual: Gigabit Ethernet PHY Edition (This manual)	R18UZ0043EJ****
R-IN32M4-CL2 User’s Manual: Board Design	R18UZ0046EJ****
R-IN32M4-CL2 Programming Manual: Driver	R18UZ0038EJ****
R-IN32M4-CL2 Programming Manual: OS	R18UZ0040EJ****

2. Numbers and Symbols

Data significance: Higher digits on the left and lower digits on the right

Active low representation:

xxxZ (capital letter Z after pin or signal name)

or xxx_N (capital letter _N after pin or signal name)

or xxnx (pin or signal name contains small letter n)

Note:

Footnote for item marked with Note in the text

Caution:

Information requiring particular attention

Remark:

Supplementary information

Numeric representation:

Binary … xxxx , xxxxB or n'bxxxx (n bits)

Decimal … xxxx

Hexadecimal … xxxxH or n'hxxxx (n bits)

Prefix indicating power of 2 (address space, memory capacity):

K (kilo) … $2^{10} = 1024$

M (mega) … $2^{20} = 1024^2$

G (giga) … $2^{30} = 1024^3$

Data Type:

Word … 32 bits

Halfword … 16 bits

Byte … 8 bits

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FIGURES

TABLES

1. Product Overview

The GbE-PHY is a dual-port Gigabit Ethernet PHY.

The GbE-PHY is designed for space-constrained 10/100/1000BASE-T applications. It features integrated, line-side termination to conserve board space, lower EMI, and improved system performance.

1.1 Key Features

This section lists the main features and benefits of the GbE-PHY.

1.1.1 Superior PHY and Interface Technology

- Two integrated 10/100/1000BASE-T Ethernet copper transceiver (IEEE 802.3ab)
- HP Auto-MDIX and manual MDI/MDIX support
- Jumbo frame support up to 12 kilobytes

1.1.2 Best in Class Power Consumption

- EcoEthernet™ v2.0 green energy efficiency with ActiPHY™
- Fully optimized power consumption for all link speeds

1.1.3 Key Specifications

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, and 1000BASE-T) Specifications
- Devices support operating temperatures of –40 °C ambient to 125 °C junction

1.2 Caution in This Manual<R>

Registers and bits used in this manual are expressed in accordance with the IEEE Standard. For details, see Section 3.1, Register and Bit Conventions.

2. Functional Descriptions

This section describes the functional aspects of the GbE-PHY, including available operational features, and testing functionality.

2.1 Twisted Pair Media Interface

The twisted pair interface is compliant with IEEE 802.3-2008.

2.1.1 Voltage Mode Line Driver

The GbE-PHY uses a voltage mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's media interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

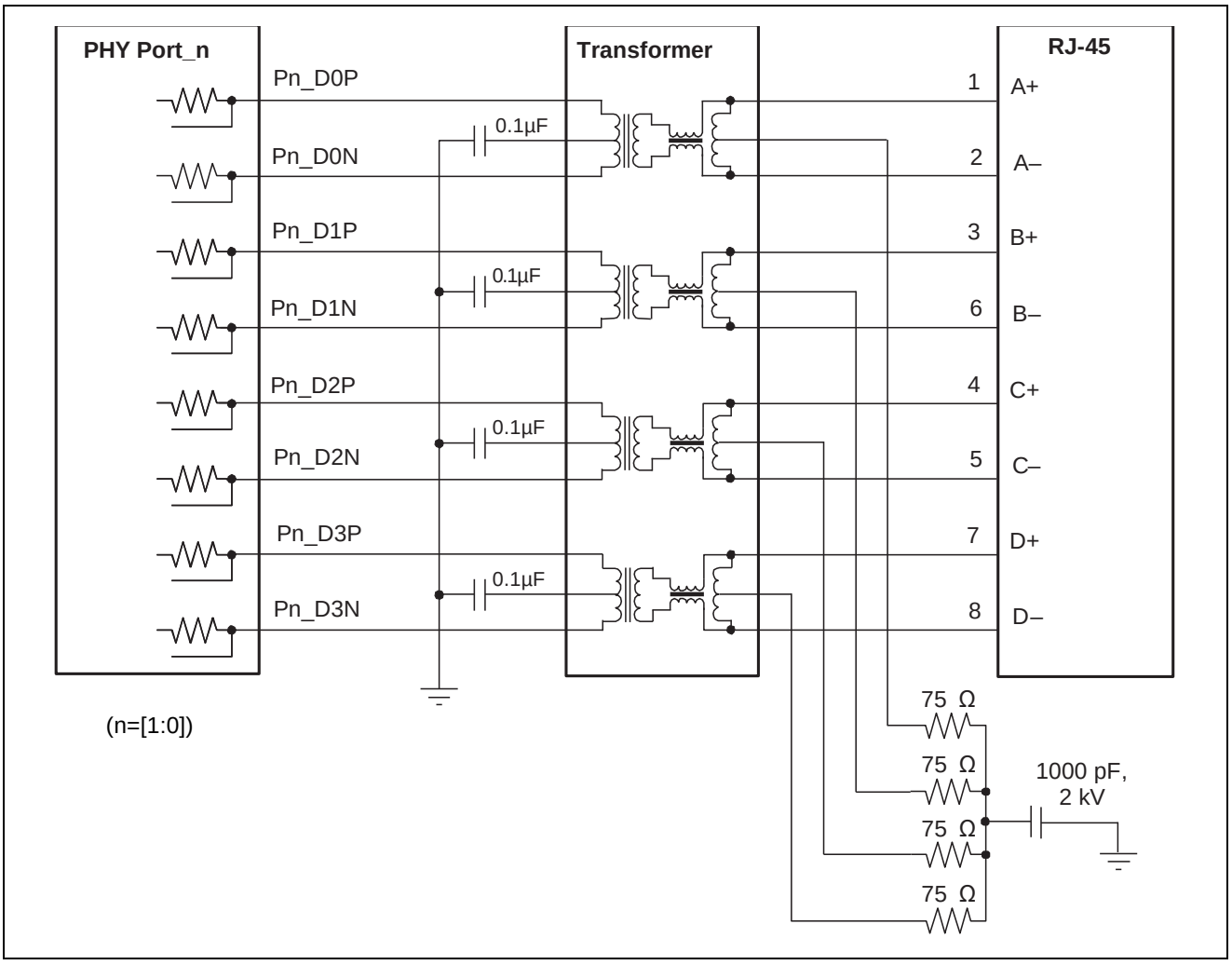

Figure 2.1 Media Interface

2.1.2 Autonegotiation and Parallel Detection

The GbE-PHY supports twisted pair autonegotiation, as defined by IEEE 802.3-2008 Clause 28. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-T.

If the link partner does not support autonegotiation, the GbE-PHY automatically uses parallel detection to select the appropriate link speed.

Autonegotiation is disabled by clearing register 0, bit 12. When autonegotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

Caution: While 10BASE-T and 100BASE-TX do not require autonegotiation, IEEE 802.3-2008 Clause 40 has defined 1000BASE-T to require autonegotiation.

2.1.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the GbE-PHY includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-TX, and 1000BASE T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs — a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Caution: The GbE-PHY can be configured to perform HP Auto-MDIX, even when autonegotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.
The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A (of four twisted pairs A, B, C, and D) is connected to the RJ45 connector 1,2 in normal MDI mode.

Table 2.1 Supported MDI Pair Combinations

RJ45 Connections				
1, 2	3, 6	4, 5	7, 8	Mode
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

2.1.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

2.1.5 Link Speed Downshift

For operation in cabling environments that are incompatible with 1000BASE-T, the GbE-PHY provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:2. For more information, see Table 3.33 ActiPHY Control, Address 20E1 (0x14).

2.2 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the GbE-PHY also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of fast link pulse over copper media.

The ActiPHY power management mode is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

- Low power state
- Link partner wake-up state
- Normal operating state (link-up state)

The GbE-PHY switches between the low power state and link partner wake- up state at a programmable rate until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY state machine operates as described.

When autonegotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and link partner wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. When autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

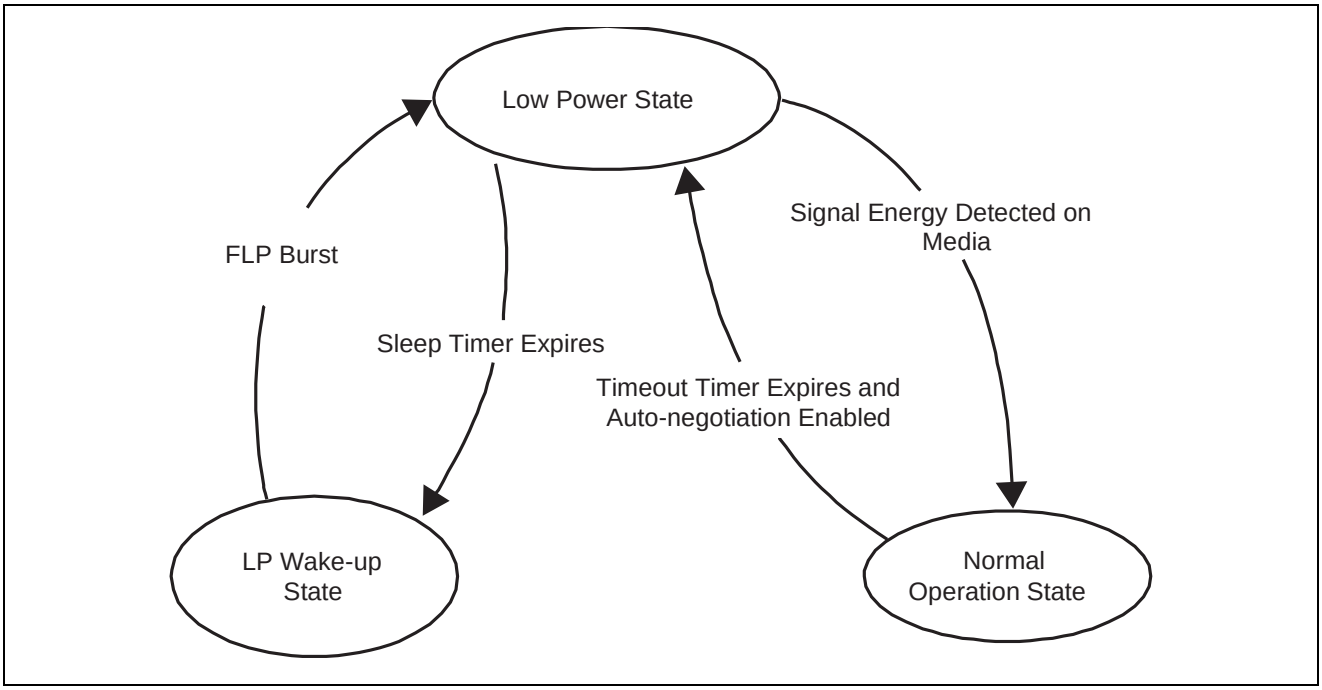

Figure 2.2 ActiPHY State Diagram

2.2.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Autonegotiation-capable link partner
- Another PHY in enhanced ActiPHY link partner wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to link partner wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

2.2.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete fast link pulse bursts are sent on alternating pairs A and B of the media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

After sending signal energy on the relevant media, the PHY returns to the low power state.

2.2.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

2.3 LED Interface

The polarity of the LED outputs is programmable and can be changed using register 17E2, bits 13:10. The default polarity is active low.

It provides four LED signals per port, LED0 through LED3. The mode and function of each LED signal can be configured independently.

Caution: LED number is listed using the convention, LED<LED#>_<Port#>.

2.3.1 LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The default LED state is active low and can be changed by modifying the value in register 17E2, bits 13:10. The blink/pulse stretch is dependent on the LED behavior setting in register 30.

The following table provides a summary of the LED modes and functions. The modes listed are equivalent to the setting used in register 29 to configure each LED pin.

Table 2.2 LED Mode and Function Summary

(1/2)

Mode	Function Name	LED State and Description
0	Link/Activity	1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1: No link in 1000BASE-T. 0: Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.
2	Link100/Activity	1: No link in 100BASE-TX. 0: Valid 100BASE-TX. Blink or pulse-stretch = Valid 100BASE-TX link with activity present.
3	Link10/Activity	1: No link in 10BASE-T. 0: Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1: No link in 100BASE-TX or 1000BASE-T. 0: Valid 100BASE-TX or 1000BASE-T link. Blink or pulse- stretch = Valid 100BASE-TX or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1: No link in 10BASE-T or 1000BASE-T. 0: Valid 10BASE-T or 1000BASE-T link. Blink or pulse-stretch = Valid 10BASE-T or 1000BASE-T link with activity present.
6	Link10/100/Activity	1: No link in 10BASE-T or 100BASE-TX. 0: Valid 10BASE-T or 100BASE-TX link. Blink or pulse-stretch = Valid 10BASE-T or 100BASE-TX link with activity present.
7	Reserved	Reserved.
8	Duplex/Collision	1: Link established in half-duplex mode, or no link established. 0: Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1: No collision detected. Blink or pulse-stretch = Collision detected.

Table 2.2 LED Mode and Function Summary

(2/2)

Mode	Function Name	LED State and Description
10	Activity	1: No activity present. Blink or pulse-stretch = Activity present.
11	Reserved	Reserved.
12	Autonegotiation Fault	1: No autonegotiation fault present. 0: Autonegotiation fault occurred.
13	Reserved	Reserved.
14	Force LED Off	1: De-asserts the LED Note.
15	Force LED On	0: Asserts the LED Note.

Note: Setting this mode suppresses LED blinking after reset.

2.3.2 LED Port Swapping

For additional hardware configurations, the GbE-PHY can have its LED port order swapped. This is a useful feature to help simplify PCB layout design. Register 25G bit 0 controls the LED port swapping mode. LED port swapping only applies to the general mode LEDs.

2.3.3 LED Behavior

LED behaviors can be programmed into the GbE-PHY. Use the settings in register 30 to program LED behavior, which includes the following:

LED Combine Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display when the combine feature is disabled.

LED Blink or Pulse-Stretch This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

Rate of LED Blink or Pulse-Stretch This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms,
100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

LED Pulsing Enable To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz.

2.4 Fast Link Failure Indication

The GbE-PHY exceeds IEEE 802.3 standards by indicating the onset of a link failure in less than 1 ms (worst case <3 ms). (IEEE 802.3 standard establishes a delay of up to 750 ms before indicating that a 1000BASE-T link is no longer present.) A fast link failure indication is critical to support ports used in a synchronization timing link application. The fast link failure indication works for all copper media speeds.

Caution: For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that analyzes the integrity of the link, and asserts at the indication of failure.

2.5 Testing Features

The GbE-PHY includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

2.5.1 Ethernet Packet Generator

The Ethernet packet generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for copper media to isolate problems between the MAC and the GbE-PHY, or between a locally connected PHY and its remote link partner. Enabling the EPG feature disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Caution: The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the GbE-PHY is connected to a live network.

To enable the EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output data to the MAC are still active when the EPG is enabled. When it is necessary to disable the MAC receive data as well, set the register bit 0.10 to 1.

When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

- Source and destination addresses for each packet
- Packet size
- Interpacket gap
- FCS state
- Transmit duration
- Payload pattern

When register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

2.5.2 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface into the MAC interface of the PHY where it is retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

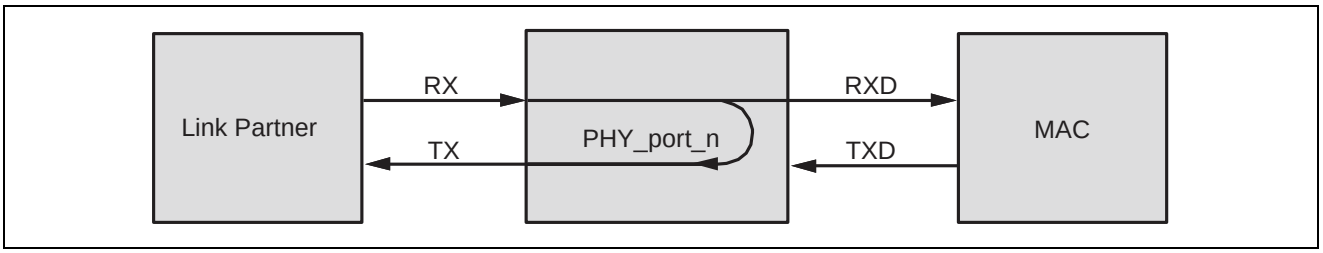

Figure 2.3 Far-End Loopback Diagram

2.5.3 Near-End Loopback

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

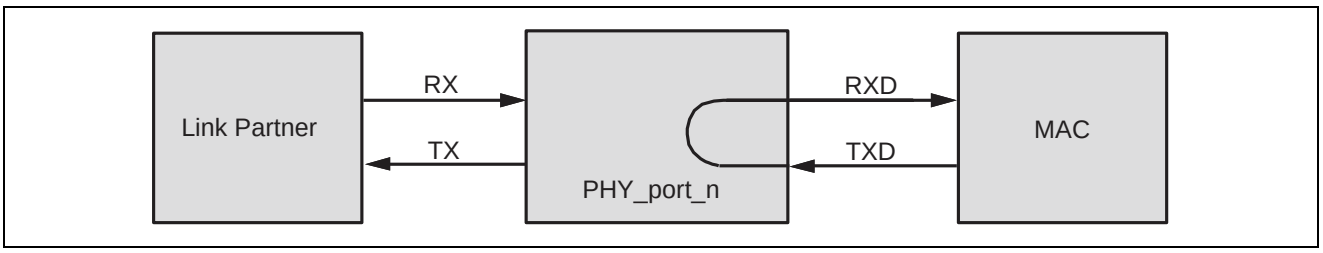

Figure 2.4 Near-End Loopback Diagram

2.5.4 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Connect pair A and pair B, and pair C and pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

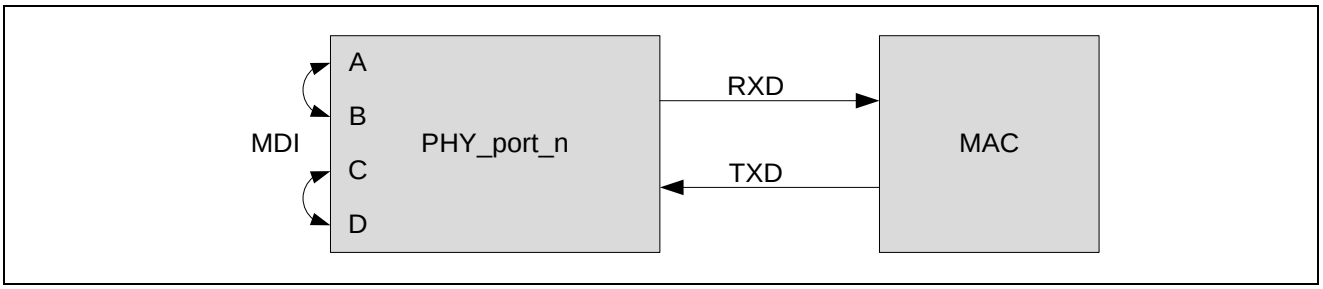

Figure 2.5 Connector Loopback Diagram

When using the connector loopback testing feature, the device autonegotiation, speed, and duplex configuration is set using device registers 0, 4, and 9.

For 1000BASE-T connector loopback, additional writes are required in the following order:

1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.
2. Disable pair swap correction. Set register bit 18.5 to 1.

3. Registers

This section provides information about how to configure the GbE-PHY using its internal memory registers and the management interface. The registers marked reserved should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; however, in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

- RO: Read Only
- R/W: Read and Write
  The GbE-PHY uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Two pages of extended registers with addresses from 16E1–30E1 and 16E2–30E2
- General-purpose registers with addresses from 0G to 30G

The following illustration shows the relationship between the device registers and their address spaces.

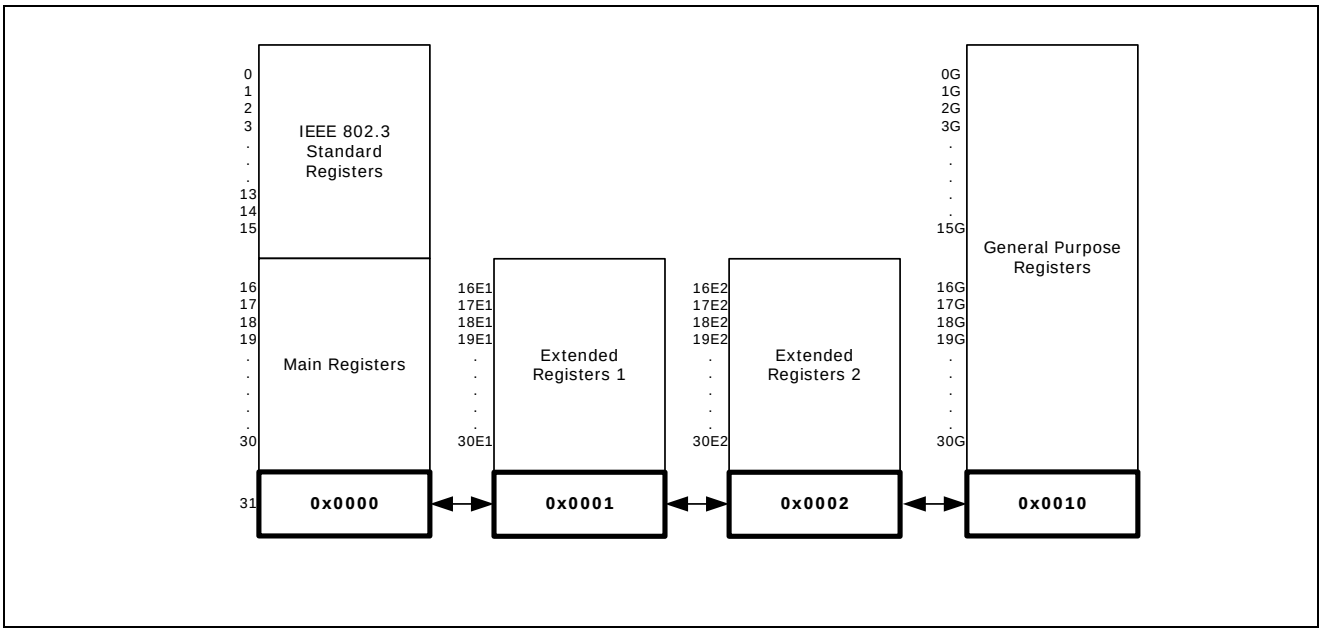

Figure 3.1 Register Space Diagram

Reserved Registers For main registers 16–31, extended registers 16E1–30E1, 16E2–30E2 and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.

Reserved Bits In writing to registers with reserved bits, use a read-modify-then- write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and heir read state cannot be considered static or unchanging.

3.1 Register and Bit Conventions

This document refers to registers by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (example 27E1) means it is a register contained within extended register page number 1. A register with a G attached (example 13G) means it is a General Purpose page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

3.2 IEEE 802.3 and Main Registers

In the GbE-PHY, the page space of the standard registers consists of the IEEE 802.3 standard registers and the GbE-PHY standard registers. The following table lists the names of the registers associated with the addresses as specified by IEEE 802.3.

Table 3.1 IEEE 802.3 Registers

Address	Name
0	Mode Control
1	Mode Status
2	PHY Identifier 1
3	PHY Identifier 2
4	Autonegotiation Advertisement
5	Autonegotiation Link Partner Ability
6	Autonegotiation Expansion
7	Autonegotiation Next-Page Transmit
8	Autonegotiation Link Partner Next-Page Receive
9	1000BASE-T Control
10	1000BASE-T Status
11-14	Reserved
15	1000BASE-T Status Extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 3.2 Main Registers

Address	Name
16	100BASE-TX status extension
17	1000BASE-T status extension 2
18	Extended PHY control 0
19	Error Counter 1
20	Error Counter 2
21	Error Counter 3
22	Extended Control and Status
23	Extended PHY control 1
24	Extended PHY control 2
25	Interrupt mask
26	Interrupt status
27	Reserved
28	Auxiliary control and status
29	LED mode select
30	LED behavior
31	Extended/General purpose Register page access

3.2.1 Mode Control

The device register at memory address 0 controls several aspects of the GbE-PHY functionality. The following table shows the available bit settings in this register and what they control.

Table 3.3 Mode Control, Address 0 (0x00)

Bit	Name	Access	Description	Default
15	Software reset	R/W	Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits. 1: Reset asserted. 0: Reset de-asserted. Wait 1us after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1: Loopback enabled. 0: Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register).	0
13	Forced speed selection LSB[Note]	R/W	Bit6 / Bit1 / Communication speed 0 / 0 / 10 Mbps. 0 / 1 / 100 Mbps. 1 / 0 / 1000 Mbps. (Initial Value) 1 / 1 / Setting prohibited	0
12	Autonegotiation enable	R/W	1: Autonegotiation enabled. 0: Autonegotiation disabled.	1
11	Power-down	R/W	1: Power-down enabled.	0
10	Isolate	R/W	1: Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart autonegotiation	R/W	Self-clearing bit. 1: Restart autonegotiation on media interface.	0
8	Duplex	R/W	1: Full-duplex. 0: Half-duplex.	0
7	Collision test enable	R/W	1: Collision test enabled.	0
6	Forced speed selection MSB[Note]	R/W	Bit6 / Bit13 / Communication speed 0 / 0 / 10 Mbps. 0 / 1 / 100 Mbps. 1 / 0 / 1000 Mbps. (Initial Value) 1 / 1 / Setting prohibited	1
5:0	Reserved	RO	Reserved.	0x00

Note: Before selecting the 1000 Mbps forced speed mode, manually configure the PHY as master or slave by setting bit 11 in register 9 (1000BASE-T Control). Each time the link drops, the PHY needs to be powered down(0.11) manually to enable it to link up again using the master/slave setting specified in register 9.11.

3.2.2 Mode Status

The register at address 1 in the device main registers space enables reading the currently enabled mode setting. The following table shows possible readouts of this register.

Table 3.4 Mode Status, Address 1 (0x01)

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1: 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1: 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1: 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1: 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1: 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1: 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1: 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1: Extended status information present in register 15.	1
7	Reserved	RO	Reserved.	1
6	Preamble suppression capability	RO	1: MF preamble can be suppressed. 0: MF preamble required. (MF: Management Frame)	1
5	Autonegotiation complete	RO	1: Autonegotiation complete.	0
4	Remote fault	RO	Latches high. 1: Far-end fault detected.	0
3	Autonegotiation capability	RO	1: Autonegotiation capable.	1
2	Link status	RO	Latches low. 1: Link is up.	0
1	Jabber detect	RO	Latches high. 1: Jabber condition detected.	0
0	Extended capability	RO	1: Extended register capable.	1

3.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the GbE-PHY are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

Table 3.5 PHY Identifier 1, Address 2 (0x02)

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0×0007

Table 3.6 PHY Identifier 2, Address 3 (0x03)

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	000001
9:4	Model number	RO	Model number	100011
3:0	Device revision number	RO	Revision A	0001

3.2.4 Autonegotiation Advertisement

The bits in address 4 in the main registers space control the ability to notify other devices of the status of its autonegotiation feature. The following table shows the available settings and readouts.

Table 3.7 Autonegotiation Advertisement, Address 4 (0x04)

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1: Request enabled	0
14	Reserved	RO	Reserved	0
13	Transmit remote fault	R/W	1: Enabled	0
12	Reserved	RO	Reserved	0
11	Advertise asymmetric pause	R/W	1: Advertises asymmetric pause	0
10	Advertise symmetric pause	R/W	1: Advertises symmetric pause	0
9	Advertise100BASE-T4	R/W	1: Advertises 100BASE-T4	0
8	Advertise100BASE-TX FDX	R/W	1: Advertise 100BASE-TX FDX	1
7	Advertise100BASE-TX HDX	R/W	1: Advertises 100BASE-TX HDX	1
6	Advertise10BASE-T FDX	R/W	1: Advertises 10BASE-T FDX	1
5	Advertise10BASE-T HDX	R/W	1: Advertises 10BASE-T HDX	1
4:0	Advertise selector	R/W	Advertise selector	00001

3.2.5 Link Partner Autonegotiation Capability

The bits in main register 5 can be used to determine if the link partner (LP) used with the GbE-PHY is compatible with the autonegotiation functionality.

Table 3.8 Autonegotiation Link Partner Ability, Address 5 (0x05)

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1: Requested	0
14	LP acknowledge	RO	1: Acknowledge	0
13	LP remote fault	RO	1: Remote fault	0
12	Reserved	RO	Reserved	0
11	LP advertise asymmetric pause	RO	1: Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1: Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1: Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1: Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1: Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1: Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1: Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO	LP Advertise selector	00000

3.2.6 Autonegotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP autonegotiation functioning. The following table shows the available settings and readouts.

Table 3.9 Autonegotiation Expansion, Address 6 (0x06)

Bit	Name	Access	Description	Default
15:5	Reserved	RO	Reserved.	0x000
4	Parallel detection fault	RO	This bit latches high. 1: Parallel detection fault.	0
3	LP next page capable	RO	1: LP is next page capable.	0
2	Local PHY next page capable	RO	1: Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1: New page is received.	0
0	LP is autonegotiation capable	RO	1: LP is capable of autonegotiation.	0

3.2.7 Transmit Autonegotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an autonegotiation sequence. The following table shows the settings available.

Table 3.10 Autonegotiation Next Page Transmit, Address 7 (0x07)

Bit	Name	Access	Description	Default
15	Next page	R/W	1: More pages follow	0
14	Reserved	RO	Reserved	0
13	Message page	R/W	1: Message page 0: Unformatted page	1
12	Acknowledge 2	R/W	1: Complies with request 0: Cannot comply with request	0
11	Toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	Message/unformatted code	R/W	Message/unformatted code	0x001

3.2.8 Autonegotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP autonegotiation. The following table shows the possible readouts.

Table 3.11 Autonegotiation LP Next Page Receive, Address 8 (0x08)

Bit	Name	Access	Description	Default
15	LP next page	RO	1: More pages follow	0
14	Acknowledge	RO	1: LP acknowledge	0
13	LP message page	RO	1: Message page 0: Unformatted page	0
12	LP acknowledge 2	RO	1: LP complies with request	0
11	LP toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	LP message/unformatted code	RO	LP Message/unformatted code	0x000

3.2.9 1000BASE-T Control

The 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 3.12 1000BASE-T Control, Address 9 (0x09)

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000: Normal 001: Mode 1: Transmit waveform test 010: Mode 2: Transmit jitter test as master 011: Mode 3: Transmit jitter test as slave 100: Mode 4: Transmitter distortion test 101–111: Reserved	000
12	Master/slave manual configuration	R/W	1: Master/slave manual configuration enabled	0
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1: Configure PHY as master during negotiation 0: Configure PHY as slave during negotiation	0
10	Port type	R/W	1: Multi-port device 0: Single-port device	1
9	1000BASE-T FDX capability	R/W	1: 1000BASE-T FDX capable	1
8	1000BASE-T HDX capability	R/W	1: 1000BASE-T HDX capable	1
7:0	Reserved	RO	Reserved	0x00

Caution: Transmitter test mode (bits 15:13) operates in the manner described in IEEE 802.3 section 40.6.1.1.2.

3.2.10 1000BASE-T Status

The bits in register 10 of the main register space can be read to obtain the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 3.13 1000BASE-T Status, Address 10 (0x0A)

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1: Master/slave configuration fault detected 0: No master/slave configuration fault detected	0
14	Master/slave configuration resolution	RO	1: Local PHY configuration resolved to master 0: Local PHY configuration resolved to slave	1
13	Local receiver status	RO	1: Local receiver is operating normally	0
12	Remote receiver status	RO	1: Remote receiver OK	0
11	LP 1000BASE-T FDX capability	RO	1: LP 1000BASE-T FDX capable	0
10	LP 1000BASE-T HDX capability	RO	1: LP 1000BASE-T HDX capable	0
9:8	Reserved	RO	Reserved	00
7:0	Idle error count	RO	Self-clearing register	0x00

3.2.11 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 3.14 1000BASE-T Status Extension 1, Address 15 (0x0F)

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	00
13	1000BASE-T FDX capability	RO	1: PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1: PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO	Reserved	0x000

3.2.12 100BASE-TX Status Extension

Register 16 in the main registers page space provides additional information about the status of the 100BASE-TX operation.

Table 3.15 100BASE-TX Status Extension, Address 16 (0x10)

Bit	Name	Access	Description	Default
15	100BASE-TX Descrambler	RO	1: Descrambler locked	0
14	100BASE-TX lock error	RO	Self-clearing bit. 1: Lock error detected	0
13	100BASE-TX disconnect state	RO	Self-clearing bit. 1: PHY 100BASE-TX link disconnect detected	0
12	100BASE-TX current link status	RO	1: PHY 100BASE-TX link active	0
11	100BASE-TX receive error	RO	Self-clearing bit. 1: Receive error detected	0
10	100BASE-TX transmit error	RO	Self-clearing bit. 1: Transmit error detected	0
9	100BASE-TX SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected	0
8	100BASE-TX ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected	0
7:0	Reserved	RO	Reserved	0x00

3.2.13 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 16.

Table 3.16 1000BASE-T Status Extension 2, Address 17 (0x11)

(1/2)

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1: Descrambler locked.	0
14	1000BASE-T lock error	RO	Self-clearing bit. 1: Lock error detected	0
13	1000BASE-T disconnect state	RO	Self-clearing bit. 1: PHY 1000BASE-T link disconnect detected	0
12	1000BASE-T current link status	RO	1: PHY 1000BASE-T link active	0
11	1000BASE-T receive error	RO	Self-clearing bit. 1: Receive error detected	0
10	1000BASE-T transmit error	RO	Self-clearing bit. 1: Transmit error detected	0
9	1000BASE-T SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected	0
8	1000BASE-T ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected	0
7	1000BASE-T carrier extension error	RO	Self-clearing bit. 1: Carrier extension error detected	0

Table 3.16 1000BASE-T Status Extension 2, Address 17 (0x11)

(2/2)

Bit	Name	Access	Description	Default
6	Reserved	RO	Reserved	0
5	MDI crossover error	RO	1: MDI crossover error was detected	0
4:0	Reserved	RO	Reserved	00000

3.2.14 Extended PHY Control 0

The following table shows the settings available.

Table 3.17 Extended PHY Control 0, Address 18 (0x12)

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved	0x00
7	HP Auto-MDIX at forced 10/100	R/W	Sticky bit. 1: Disable HP Auto-MDIX at forced 10/100 speeds	1
6	Reserved	RO	Reserved	0
5	Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled)	R/W	Sticky bit. 1: Disable the automatic pair swap correction	0
4	Disable polarity correction	R/W	Sticky bit. 1: Disable polarity inversion correction on each subchannel	0
3:0	Reserved	RO	Reserved	1000

3.2.15 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 3.18 Error Counter 1, Address 19 (0x13)

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	0x00
7:0	100/1000 receive error counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

3.2.16 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 3.19 Error Counter 2, Address 20 (0x14)

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	0x00
7:0	100/1000 false carrier counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

3.2.17 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 3.20 Error Counter 3, Address 21 (0x15)

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	0x00
7:0	Copper media link disconnect counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

3.2.18 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 3.21 Extended Control and Status, Address 22 (0x16)

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	Sticky bit. 1: Bypass link integrity test 0: Enable link integrity test	0
14	Reserved	RO	Reserved	0
13	Disable 10BASE-T echo	R/W	Sticky bit. 1: Disable 10BASE-T echo	1
12:10	Reserved	RO	Reserved	100
9	Sticky reset enable	R/W	Super-sticky bit. 0: Enabled	1
8:1	Reserved	RO	Reserved	0x00
0	SMI broadcast write	R/W	Sticky bit. 1: Enabled	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if
  bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

3.2.19 Extended PHY Control 1

The following table shows the settings available.

Table 3.22 Extended PHY Control 1, Address 23 (0x17)

Bit	Name	Access	Description	Default
15:4	Reserved	RO	Reserved.	0x200
3	Far-end loopback mode	R/W	1: Enabled.	0
2:0	Reserved	RO	Reserved.	000

3.2.20 Extended PHY Control 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 3.23 Extended PHY Control 2, Address 24 (0x18)

Bit	Name	Access	Description	Default
15:6	Reserved	RO	Reserved	0x000
5:4	Jumbo packet mode	R/W	Sticky bit. 00: Normal IEEE 1.5 kB packet length 01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock) 10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock) 11: Reserved	00
3:1	Reserved	RO	Reserved	000
0	1000BASE-T connector loopback	R/W	1: Enabled	0

Caution: When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

3.2.21 Interrupt Mask

These bits control the device interrupt mask. The following table shows the settings available.

Table 3.24 Interrupt Mask, Address 25 (0x19)

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	Sticky bit. 1: Unmask.	0
14	Speed state change mask	R/W	Sticky bit. 1: Unmask.	0
13	Link state change mask	R/W	Sticky bit. 1: Unmask.	0
12	FDX state change mask	R/W	Sticky bit. 1: Unmask.	0
11	Autonegotiation error mask	R/W	Sticky bit. 1: Unmask.	0
10	Autonegotiation complete mask	R/W	Sticky bit. 1: Unmask.	0
9	Reserved	R/W	Reserved	0
8	Symbol error interrupt mask	R/W	Sticky bit. 1: Unmask.	0
7	Fast link failure interrupt mask	R/W	Sticky bit. 1: Unmask.	0
6	Reserved	R/W	Reserved	0
5	Reserved	R/W	Reserved	0
4	Reserved	R/W	Reserved	0
3	False carrier interrupt mask	R/W	Sticky bit. 1: Unmask.	0
2	Link speed downshift detect mask	R/W	Sticky bit. 1: Unmask.	0
1	Master/Slave resolution error mask	R/W	Sticky bit. 1: Unmask.	0
0	RX_ER interrupt mask	R/W	Sticky bit. 1: Unmask.	0

Caution: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 25.15 to be set.

3.2.22 Interrupt Status

The status of interrupts already written to the device is available for reading from register 26 in the main registers space. The following table shows the expected readouts.

Table 3.25 Interrupt Status, Address 26 (0x1A)

Bit	Name	Access	Description	Default
15	MDINT interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
14	Speed state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
13	Link state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
12	FDX state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
11	Autonegotiation error status	RO	Self-clearing bit. 1: Interrupt pending.	0
10	Autonegotiation complete status	RO	Self-clearing bit. 1: Interrupt pending.	0
9	Reserved	RO	Reserved	0
8	Symbol error status	RO	Self-clearing bit. 1: Interrupt pending.	0
7	Fast link failure detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
6	Reserved	RO	Reserved	0
5	Reserved	RO	Reserved	0
4	Reserved	RO	Reserved	0
3	False carrier interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	Link speed downshift detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
1	Master/Slave resolution error status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	RX_ER interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link partner's data transmission.

3.2.23 Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

Table 3.26 Auxiliary Control and Status, Address 28 (0x1C)

Bit	Name	Access	Description	Default
15	Autonegotiation complete	RO	Duplicate of bit 1.5 when autonegotiation is enabled, otherwise this is the current link status	0
14	Autonegotiation disabled	RO	Inverted duplicate of bit 0.12	0
13	HP Auto-MDIX crossover indication	RO	1: HP Auto-MDIX crossover performed internally	0
12	CD pair swap	RO	1: CD pairs are swapped	0
11	A polarity inversion	RO	1: Polarity swap on pair A	0
10	B polarity inversion	RO	1: Polarity swap on pair B	0
9	C polarity inversion	RO	1: Polarity swap on pair C	0
8	D polarity inversion	RO	1: Polarity swap on pair D	0
7	ActiPHY link status time- out control [1]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB.	0
6	ActiPHY mode enable	R/W	Sticky bit. 1: Enabled	0
5	FDX status	RO	1: Full-duplex 0: Half-duplex	0
4:3	Speed status	RO	00: Speed is 10BASE-T 01: Speed is 100BASE-TX 10: Speed is 1000BASE-T 11: Reserved	00
2	ActiPHY link status time- out control [0]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB.	1
1:0	Media mode status	RO	00: No media selected 01: Copper media selected 10: Reserved 11: Reserved	00

Bit 7 / Bit 2 / Time-out time:

Bit7	Bit2	Time-out time
0	0	2 second
0	1	4 seconds (Initial Value)
1	0	6 seconds
1	1	8 seconds

3.2.24 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs. For more information about LED modes, see Table 2.

Table 3.27 LED Mode Select, Address 29 (0x1D)

Bit	Name	Access	Description	Default
15:12	LED3 mode select	R/W	Sticky bit. Select from LED modes 0–15.	1000
11:8	LED2 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0000
7:4	LED1 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0010
3:0	LED0 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0001

3.2.25 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 3.28 LED Behavior, Address 30 (0x1E)

(1/2)

Bit	Name	Access	Description	Default
15:13	Reserved	RO	Reserved	000
12	LED pulsing enable	R/W	Sticky bit 0: Normal operation 1: LEDs pulse with a 5 kHz, programmable duty cycle when active	0
11:10	LED blink/pulse- stretch rate	R/W	Sticky bit 00: 2.5 Hz blink rate/400 ms pulse-stretch 01: 5 Hz blink rate/200 ms pulse-stretch 10: 10 Hz blink rate/100 ms pulse-stretch 11: 20 Hz blink rate/50 ms pulse-stretch The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports	01
9	Reserved	RO	Reserved	0
8	LED3 pulse-stretch/ blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
7	LED2 pulse-stretch/ blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
6	LED1 pulse-stretch/ blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
5	LED0 pulse-stretch/ blink select	R/W	Sticky bit 1: Pulse-stretch 0: Blink	0
4:2	Reserved	RO	Reserved	000

Table 3.28 LED Behavior, Address 30 (0x1E)

(2/2)

Bit	Name	Access	Description	Default
1	LED1 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0
0	LED0 combine feature disable	R/W	Sticky bit 0: Combine enabled (link/activity, duplex/collision) 1: Disable combination (link only, duplex only)	0

Caution: Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

3.2.26 Extended Page Access

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, an extended set of registers provide an additional 15 register spaces.

The register at address 31 controls access to the extended registers. Accessing the General Purpose page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 3.29 Extended/General Purpose Register Page Access, Address 31 (0x1F)

Bit	Name	Access	Description	Default
15:0	Extended/General Purpose page register access	R/W	0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access. 0x0001: Registers 16–30 access extended register space 1 0x0002: Registers 16–30 access extended register space 2 0x0010: Registers 0–30 access General Purpose register space	0x0000

3.3 Extended Page 1 Registers

To access the extended page 1 registers (16E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E1–30E1 instead of those same registers in the IEEE- specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Table 3.30 Extended Registers Page 1 Space

Address	Name
16E1–17E1	Reserved
18E1	Cu Media CRC good counter
19E1	Extended mode control
20E1	ActiPHY control
21E1–28E1	Reserved
29E1	EPG Control Register 1
30E1	EPG Control Register 2

3.3.1 Cu Media CRC Good Counter

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 3.31 Cu Media CRC Good Counter, Address 18E1 (0x12)

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0
14	Reserved	RO	Reserved.	0
13:0	Cu Media CRC good counter contents	RO	Self-clearing bit. Counter containing the number of packets with valid CRCs modulo 10,000; this counter does not saturate and will roll over to zero on the next good packet received after 9,999.	0x0000

3.3.2 Extended Mode Control

Register 19E1 controls the extended modes. The following table shows the settings available.

Table 3.32 Extended Mode Control, Address 19E1 (0x13)

Bit	Name	Access	Description	Default
15:5	Reserved	RO	Reserved	0x000
4	Fast link failure	R/W	Enable fast link failure. This must be done from PHY0 only. 1: Enabled 0: Disabled	0
3:2	Force MDI crossover	R/W	00: Normal HP Auto-MDIX operation 01: Reserved 10: Copper media forced to MDI 11: Copper media forced to MDI-X	00
1:0	Reserved	RO	Reserved	00

3.3.3 ActiPHY Control

Register 20E1 controls the device ActiPHY sleep timer, its wake-up timer, and its link speed downshifting feature. The following table shows the settings available.

Table 3.33 ActiPHY Control, Address 20E1 (0x14)

(1/2)

Bit	Name	Access	Description	Default
15	Disable carrier extension	R/W	1: Disable carrier extension in 1000BASE-T copper links	1
14:13	ActiPHY sleep timer	R/W	Sticky bit. 00: 1 second 01: 2 seconds 10: 3 seconds 11: 4 seconds	01
12:11	ActiPHY wake-up timer	R/W	Sticky bit. 00: 160 ms 01: 400 ms 10: 800 ms 11: 2 seconds	00
10	Reserved	RO	Reserved	0
9	PHY address reversal	R/W	Reverse PHY address Enabling causes physical PHY 0 to have address of 1, and PHY 1 address of 0. Changing this bit to 1 should initially be done from PHY 0 and changing to 0 from PHY1 1: Enabled 0: Disabled Valid only on PHY0	0
8	Reserved	RO	Reserved	0

Table 3.33 ActiPHY Control, Address 20E1 (0x14)

(2/2)

Bit	Name	Access	Description	Default
7:6	Media mode status	RO	00: No media selected 01: Copper media selected 10: Reserved 11: Reserved	00
5	Enable 10BASE-T no preamble mode	R/W	Sticky bit. 1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it	0
4	Enable link speed autodownshift feature	R/W	Sticky bit. 1: Enable auto link speed downshift from 1000BASE-T	0
3:2	Link speed auto downshift control	R/W	Sticky bit. 00: Downshift after 2 failed 1000BASE-T autonegotiation attempts 01: Downshift after 3 failed 1000BASE-T autonegotiation attempts 10: Downshift after 4 failed 1000BASE-T autonegotiation attempts 11: Downshift after 5 failed 1000BASE-T autonegotiation attempts	01
1:0	Reserved	RO	Reserved	00

3.3.4 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

Table 3.34 EPG Control Register 1, Address 29E1 (0x1D)

Bit	Name	Access	Description	Default
15	EPG enable	R/W	1: Enable EPG	0
14	EPG run or stop	R/W	1: Run EPG	0
13	Transmission duration	R/W	1: Continuous (sends in 10,000-packet increments) 0: Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00: 125 bytes 01: 64 bytes 10: 1518 bytes 11: 10,000 bytes (jumbo packet)	00
10	Interpacket gap	R/W	1: 8,192 ns 0: 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte source address	0000
1	Payload type	R/W	1: Randomly generated payload pattern 0: Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1: Generate packets with bad FCS 0: Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the GbE-PHY is connected to a live network.
- bit 29E1.13 (continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

3.3.5 Ethernet Packet Generator Control 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

Table 3.35 EPG Control Register 2, Address 30E1 (0x1E)

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x0000

Caution: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

3.4 Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see Table 31.

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE- specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

Table 3.36 Extended Registers Page 2 Space

Address	Name
16E2	Reserved
17E2	LED Control
18E2–30E2	Reserved

3.4.1 LED Control

The register at address 17E2 consists of the bits that provide additional LED control.

Table 3.37 LED Control, Address 17E2 (0x11)

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	00
13:10	Invert LED polarity	R/W	1: Invert polarity of LED[3:0]_PHY[1:0] signals. Default is to drive an active low signal on the LED pins.	0000
9:6	Reserved	RO	Reserved.	0000
5	Enable 1000BASE-T force mode	R/W	1: Enable 1000BASE-T force mode to allow PHY to link-up in 1000BASE-T mode without forcing master/slave when register 0, bits 6 and 13 are set to 2'b10.	0
4:0	Reserved	RO	Reserved	0x00

3.5 General Purpose Registers

Accessing the general purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31. All general purpose register bits are super-sticky

3.5.1 Reserved General Purpose Address Space

The bits in registers 0G to 18G, 20G to 24G, 26G to 28G and 30G of the general purpose register space are reserved.

3.5.2 Reserved

This register is reserved.

Table 3.38 Reserved, Address 14G (0x0E)

Bit	Name	Access	Description	Default
15:0	Reserved	RO	Reserved.	0x2200

3.5.3 Fast Link Failure Control

Register 19G in the general purpose register space controls the selection of the source PHY for the fast link failure indication. The following table shows the settings available for the FASTLINK_FAIL pin.

Table 3.39 Fast Link Failure Control, Address 19G (0x13)

Bit	Name	Access	Description	Default
15:4	Reserved	RO	Reserved	0x000
3:0	Fast link failure port setting	R/W	Select fast link failure PHY source 0000: Port0 0001: Port1 0010–1111: Output disabled	1111

3.5.4 Enhanced LED Control

The following table contains the bits to control advanced functionality of LED signals.

Table 3.40 Enhanced LED Control, Address 25G (0x19)

Bit	Name	Access	Description	Default
15:8	LED pulsing duty cycle control	R/W	Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments	0x00
7:1	Reserved	RO	Reserved	0x00
0	LED port swapping	R/W	0: LED port swapping disabled 1: LED port swapping enabled	0

3.5.5 Global Interrupt Status

The following table contains the interrupt status from the various sources to indicate which one caused that last interrupt on the pin.

Table 3.41 Global Interrupt Status, Address 29G (0x1D)

Bit	Name	Access	Description	Default
15:2	Reserved	RO	Reserved	0x0400
1	PHY1 interrupt source	RO	PHY1 interrupt source indication 0: PHY1 caused the interrupt 1: PHY1 did not cause the interrupt	1
0	PHY0 interrupt source	RO	PHY0 interrupt source indication 0: PHY0 caused the interrupt 1: PHY0 did not cause the interrupt	1

4. Design Considerations

This section provides information about design considerations for the GbE-PHY device.

(1) 1000BASE-T distortion

Silicon from some process corners at voltage and temperature extremes may not pass IEEE802.3 1000BASE-T distortion specification requirement of <10 mV across 60% of UI.

This marginality does not have any real-world link performance impact, and no BER or interoperability issues have been seen as a result.

(2) 10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) if 2.5V is supplied with the low voltage. Additionally, associated templates may be marginal or have failures.

This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

(3) 10BASE-T transmitter return loss

10BASE-T transmitter return loss can be 15dB below the incident from the range of 5MHz to 10MHz for each of the resistances: 100Ω, 85Ω, and 111Ω when using a random data pattern.

This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

REVISION HISTORY	R-IN32M4-CL2 User's Manual Gigabit Ethernet PHY Edition

Rev.	Date	Description	
		Page	Summary
0.01	Jan 15, 2016	-	First edition issued
1.00	Mar 4, 2016	-	Changed to the document format conforming the R-IN Series User's Manual.
		1	added to Section 1.2, Caution in This Manual.

[Memo]

R-IN32M4-CL2

User’s Manual Gigabit Ethernet PHY Edition

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