User's Manual

R-IN32M3 Series

User's Manual: Board design edition

- R-IN32M3-EC
- R-IN32M3-CL

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Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution.
When there is a mention unlike the text of this manual, a mention of the text takes first priority.

1.Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
  In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

How to use this manual

1. Purpose and Target Readers

This manual is intended for users who wish to understand the functions of Industrial Ethernet network LSI "R-IN32M3-EC/CL" for designing application of it. It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.
The mark "<R>" means the updated point in this revision. The mark "<R>" let users search for the updated point in this document.

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Please be understanding of this beforehand. In addition, because we make document at development, planning of each core, the related document may be the document for individual customers. Last four digits of document number (described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M3 Series

Document Name	Document Number
R-IN32M3 Series Datasheet	R18DS0008EJ****
R-IN32M3 Series User's Manual R-IN32M3-EC	R18UZ0003EJ****
R-IN32M3 Series User's Manual R-IN32M3-CL	R18UZ0005EJ****
R-IN32M3 Series User's Manual: Peripheral Modules	R18UZ0007EJ****
R-IN32M3 Series Programming Manual: Driver	R18UZ0009EJ****
R-IN32M3 Series Programming Manual: OS	R18UZ0011EJ****
R-IN32M3 Series User's Manual Peripheral: Board design edition	This manual

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary: xxxx , xxxxB or n'bxxxx (n bits)

Decimal: xxxx

Hexadecimal: xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1024$

M (mega): $2^{20} = 1024^2$

G (giga): $2^{30} = 1024^3$

Data Type:

Word: 32 bits

Halfword: 16 bits

Byte: 8 bits

Contents

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1. Outline

This manual is intended for being used by engineers that work on a circuit and PCB design that is equipped with an Ethernet communication LSI from the R-IN32M3 series made by Renesas Electronics. Target devices are the R-IN32M3-EC and R-IN32M3-CL devices.

It is recommended to study this manual carefully and to follow the recommendations during the circuit and board design.

1.1 Definition of Pin Handling and Symbols in This Manual

Pin handling and symbols are defined as follows in this manual.

Table 1.1 Definition of Pin Handling

	Description
Low level	This pin is connected to GND.
High level	This pin supplies VDD33 (3.3 V).

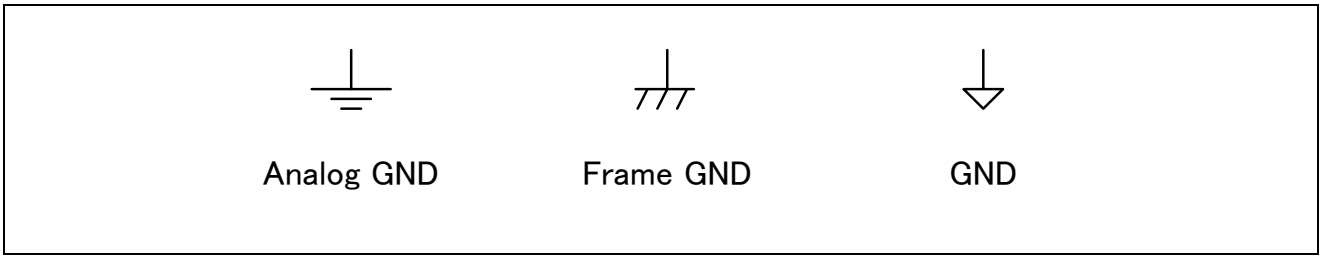


Figure 1.1 Definition of GND Symbols

2. Power/Reset Pins

2.1 Power-On/Off Sequence

Power structure of the R-IN32M3 series is internal power (VDD10: 1.0V) and I/O power (VDD33: 3.3V) and PHY power supply (VDD15: 1.5V). (PHY power is subject only R-IN32M3-EC.)

Power is recommended to put the I/O power after switching on the internal power supply. In addition, power-off is recommend internal power-off after cut-off of I/O power (see section 2.1, Power-On/Off Sequence).

In the case of supplying internal power after I/O power, note that I/O value becomes indefinite due to uncertain mode while I/O is powered on but internal power isn't, whether it is in input mode or output mode. Also, 3.3 V must be applied to the I/O pins only after applying the power supply voltages.

Power on/off time difference, that regardless of the power-on sequence, it does not matter which power supply is applied to (or removed from) the device first, but it is recommended to ensure 100ms or less time difference between the application or removal of each power supply. The 100ms or less time measurement is based on the period from 10% to 90% of each voltage range.

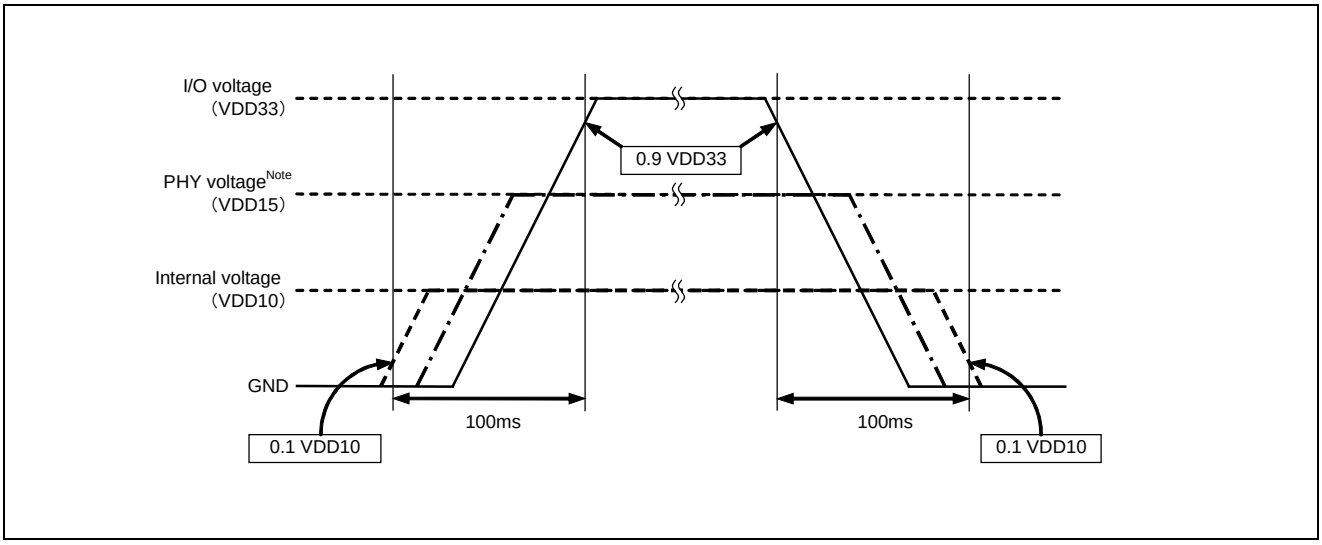


Figure 2.1 Recommended Sequence of Power-On/Off

Note. The timing for PHY power supply voltage VDD15 only needs to be observed, when the internal regulator in the R-IN32M3-EC device is not used.

2.2 Power Supply Pins

This is a list of power supply pins of the R-IN32M3.

Connect these pins according to the description given in the "Connection Example" column.

Terminal Name	Feature	Connection Example
PLL_VDD	PLL voltage (VDD) (1.0 V)	See section 4, PLL Power Pins.
PLL_GND	PLL GND potential (GND)	See section 4, PLL Power Pins.
VDD33	I/O voltage (3.3 V)	Supply a power supply from the power unit such as a regulator or DC-DC converter.
VDD10	Internal voltage (1.0 V)	Supply a power supply from the power unit such as a regulator or DC-DC converter.
GND	GND potential (GND)	Connect GND of system board.
VDDQ_MII[Note2]	Ethernet I/O voltage (3.3 V)	Supply a power supply from the power unit such as a regulator or DC-DC converter.
LX[Note1]	Built-in regulator 1.5 V output	See section 5.1, Built-in Regulator Used.
AVDD_REG[Note1]	Analog power supply for built-in regulator (3.3 V)	
AGND_REG[Note1]	Analog GND potential for built-in regulator (GND)	
BVDD[Note1]	Power supply for built-in regulator (3.3 V)	
BGND[Note1]	GND potential for built-in regulator (GND)	
FB[Note1]	Feedback input for built-in regulator	
EXTRES[Note1]	Reference resistance joining pin for Ethernet PHY	Connect to AGND through 12.4kΩ±1%.
P0VDDARXTX[Note1]	Analog power supply for Rx/Tx pin (1.5 V) - Port 0	See section 7.1, Ethernet PHY Power Supply Pins.
P1VDDARXTX[Note1]	Analog power supply for Rx/Tx pin (1.5 V) - Port 1	
VDDACB[Note1]	Analog power supply for Ethernet PHY (3.3 V)	
AGND[Note1]	Analog GND potential for PHY (3.3 V)	
VDD15[Note1]	Core voltage for Ethernet PHY (1.5 V)	
VDDAPLL[Note1]	Analog power supply for Ethernet PHY (1.5 V)	
VSSAPLLCB[Note1]	Analog GND potential for Ethernet PHY (GND)	
VDD33ESD[Note1]	Analog test power supply for Ethernet PHY (3.3 V)	
VDDQ_PECL_B0[Note1]	PECL buffer power supply (3.3 V)	
VDDQ_PECL_B1[Note1]	PECL buffer power supply (3.3 V)	

Notes 1. R-IN32M3-EC only
2. R-IN32M3-CL only

2.3 Reset Pins

This is a list of reset pins of R-IN32M3.

As a width at low level of at least 100 ms is required for the reset input signals, secure this by applying the low level of the reset signal over the oscillation stabilization time of the external oscillator (25 MHz).

In addition, de-assert the RESETZ and HOTRESETZ signals after de-asserting the PONRZ signal.

Pin Name	Feature	Connection Example
RESETZ	Reset input	-
HOTRESETZ Note	Hot reset input	-
PONRZ	Power-on reset input for built in RAM	-
TRSTZ	JTAG reset signal	See section 16, CAN Pins.
RSTOUTZ	External reset output	-

Note. R-IN32M3-CL only

3. Clock Input Pins

3.1 Features of Pins

The following table shows the pin functions for clock supply to the device.

Pin Name	I/O	Features
XT1	IN	・External resonator connection pin. ・When external clock input mode is used (OSCTH = 1), set XT1 to the low level.
XT2	IN/OUT	・External resonator connection pins. ・When "OSCTH = 0", this pin is the output. ・When external clock input mode is used (OSCTH = 1), input the clock from an external oscillator to XT2.
OSCTH	IN	・Selects the clock oscillation source to be connected to the clock pin. Low level: XT1 and XT2 are to be connected to a resonator. High level: XT2 is to be connected to an oscillator.

3.2 Notes on Configuring the Oscillation Circuit

As the R-IN32M3 series includes an oscillation block, oscillation circuits are easily configurable by externally connecting a resonator and components for external constants. Though configuring an oscillation circuit is easy, the configured circuit is analog and operates at a high frequency, so notes that differ for logic become applicable.

To achieve stable operation of the oscillation circuit, set components for external constants to the optimum values (capacitors on the input and output sides, and limiting resistors) and observe the following points required for an analog circuit.

- Place the oscillation circuit near the R-IN32M3.
- Place the oscillation circuit as far as possible from high-frequency input pins such as clock pins.
- Place the resonators and components for external constants immediately close to the input and output pins of oscillation circuit, and keep the connections as short as possible.
- Make the ground connections of the capacitors to the GND pins of R-IN32M3 as short and thick as possible.
- Make the lead wires between the resonator and capacitors as short as possible.
- Surround the components for external constant parts by as much GND wiring as is possible.

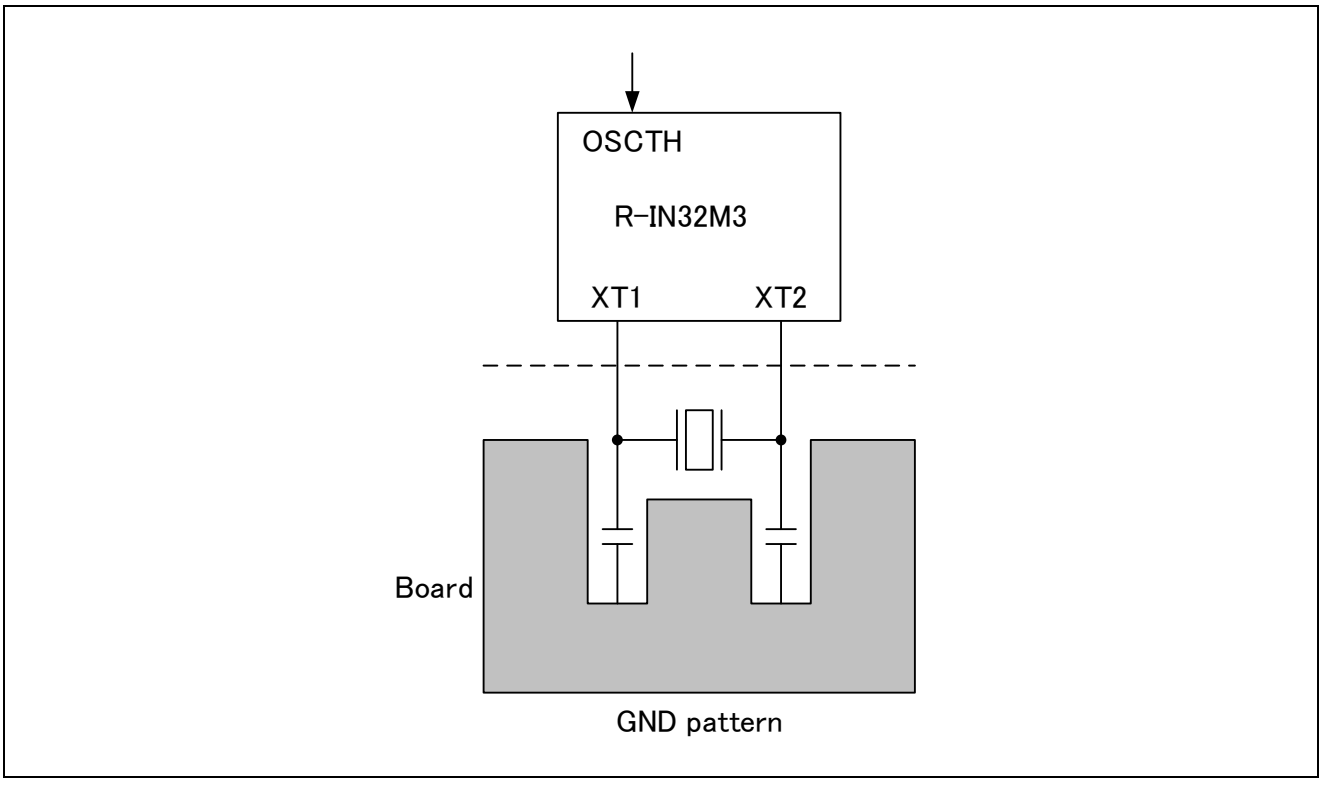


Figure 3.1 Example of GND Pattern for the Components for External Constants

In addition, the following points to note should be observed in evaluating and determining the external constants.

- The range of oscillating operation may vary due to the dielectric constant of the board's material, so use the actual printed circuit board that will be used in the finished design.
- Check use of the board with the developed R-IN32M3 and the actual resonator to be mounted on it.

3.3 Oscillation Circuit Configuration Example

The following figure shows typical examples of oscillation circuits.

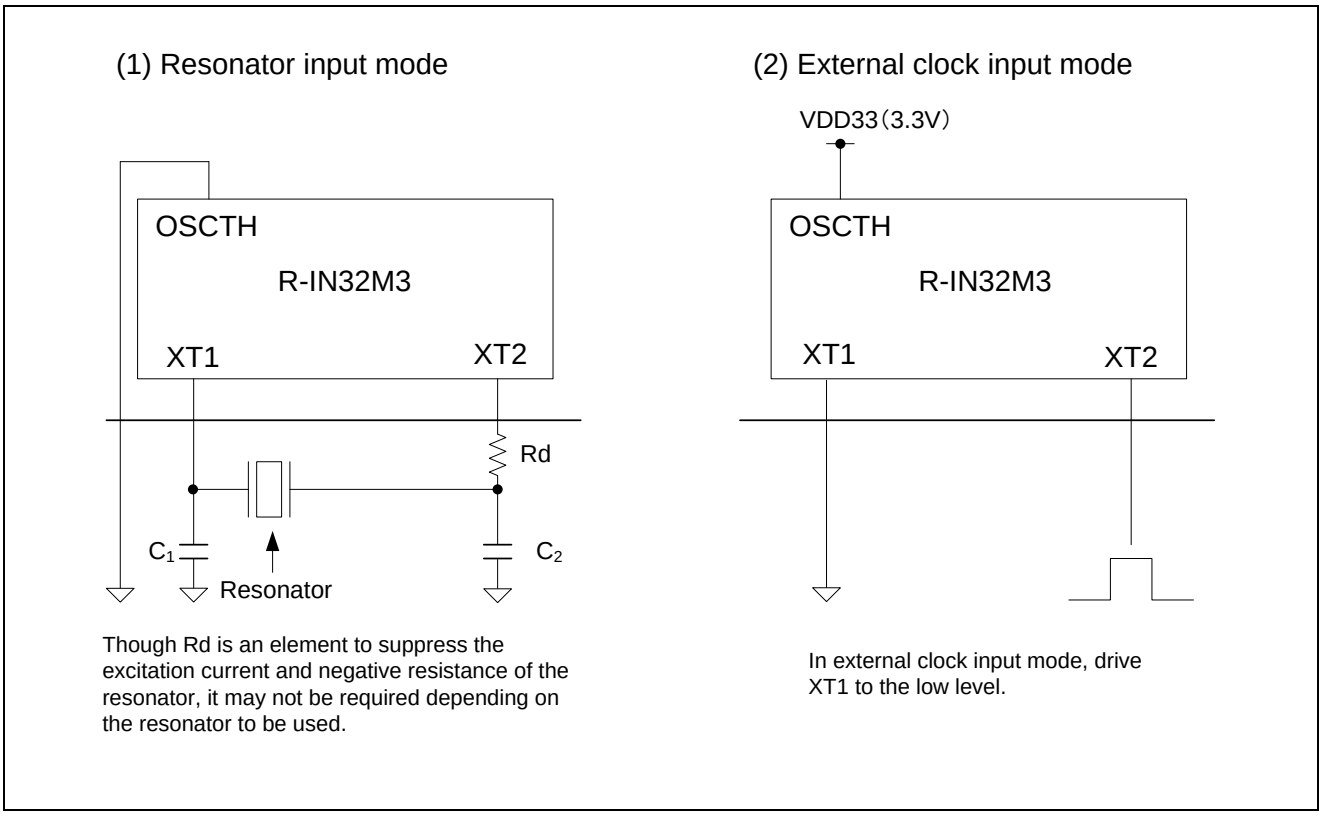


Figure 3.2 Configuration Example of the Oscillation Circuit

Caution. The input of the R-IN32M3 is fixed to 25 MHz.
When a resonator is to be used, contact the resonator manufacturer and ask for a corresponding part number and external constants.
Renesas recommends the following oscillator and resonator manufacturers.

- **Nihon Dempa Kogyo Co., Ltd. (NDK)**
  URL: http://www.ndk.com/en/index.html
- **KYOCERA Crystal Device Corporation**
  URL: http://1 www.kyocera-crystal.jp/

4. PLL Power Pins

The PLL circuit is susceptible to noise. To reduce the influence of noise, it is recommended to place filters in the power supply pin of the PLL. Also if user avoid the interference noise of the PLL board and power supply, the usage of user ferrite beads (FB).

4.1 Recommended Configuration of Filter

Figure 4.1 shows the recommended configuration of the filter for the PLL power supply pins.

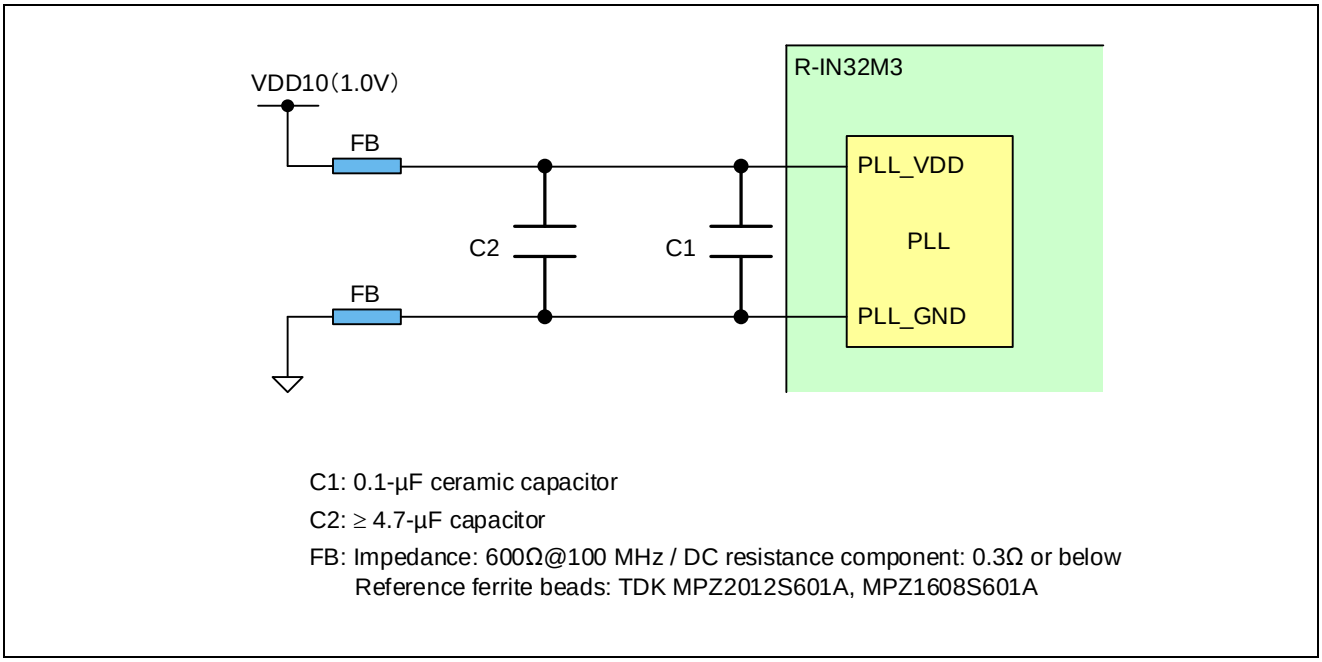


Figure 4.1 Recommended Configuration of Filter

Caution. Put C1 as close as possible to the PLL_VDD and PLL_GND pins.
C2 placement is less critical and there is no problem even if it can't be arranged as close to the R-IN32M3 as C1.

4.2 Notes on Placement of Peripheral Components

The 0.1-µF ceramic capacitor (C1) should be placed immediately close to R-IN32M3 (in the immediate vicinity of the pin).

Figure 4.2 is a schematic view from below the board.

In addition, the wiring patterns for the electrolytic capacitor (C2) and ferrite beads running parallel to other signal lines should be avoided.

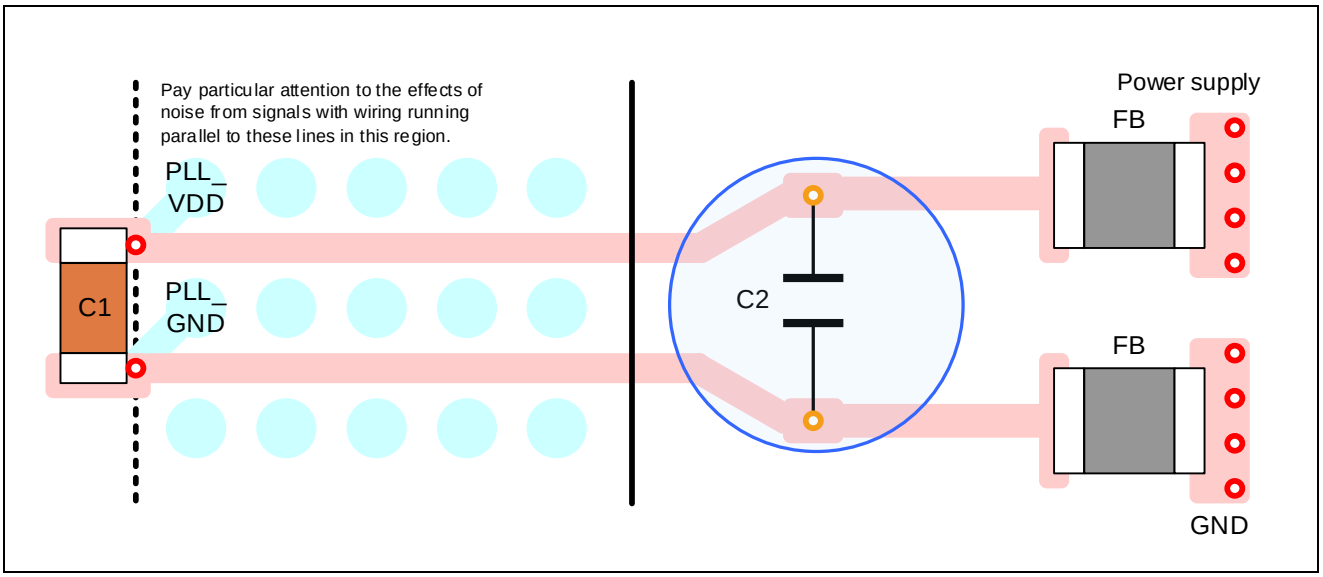


Figure 4.2 Schematic View from Below the Board

Caution. PLL_VDD and PLL_GND lines should be as short and thick as possible in PCB wiring. Longer wiring leads to stronger crosstalk because the LC components of the wiring increase, more readily leading to effects.

5. Built-in Regulator Pin (R-IN32M3-EC only)

In the R-IN32M3-EC, supplying 1.5 V to the VDD15, VDDAPLL, and PxVDDARXTX (x = 0, 1) pins is required as an internal power supply for Ethernet PHY.

Since the R-IN32M3-EC is equipped with a regulator, there is no need to generate power externally. When not using a built-in regulator, see section 6.2, Built-in Regulator Unused and design.

5.1 Built-in Regulator Used

Make wiring and layout as follows at the time of the built-in regulator in use.

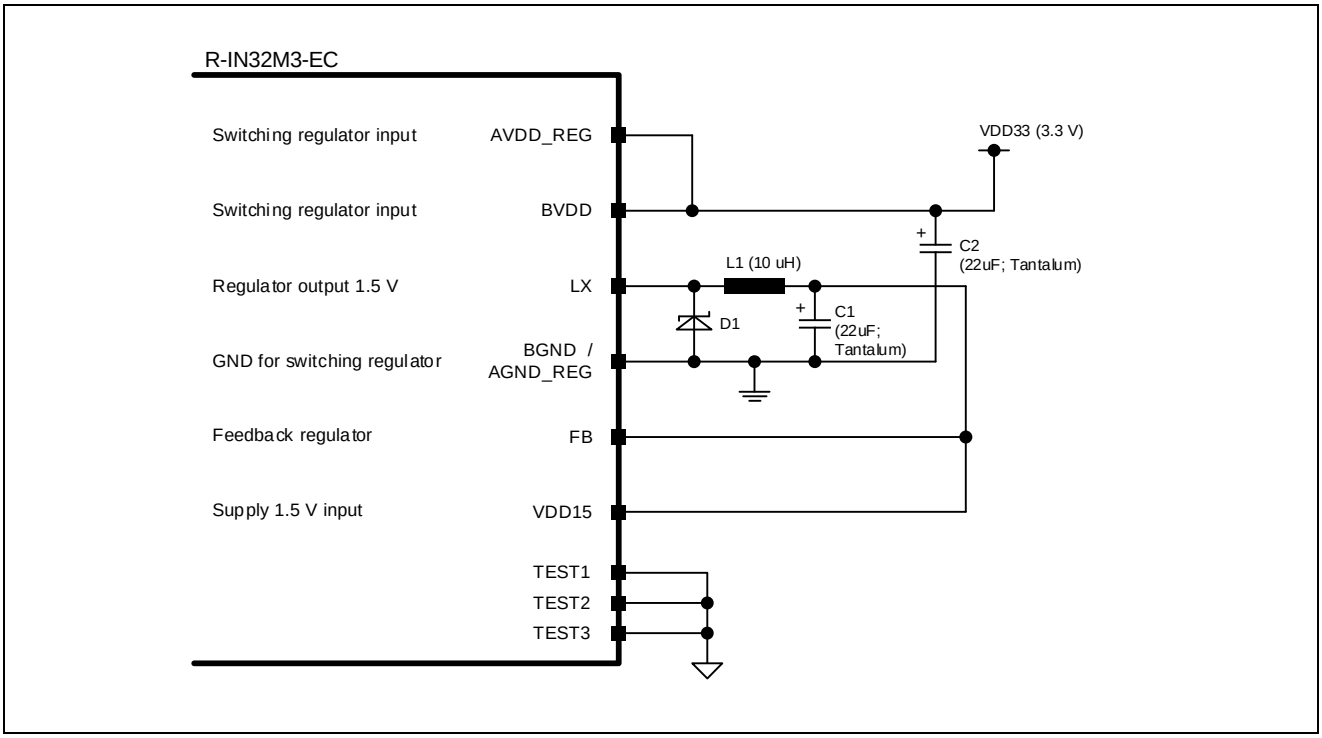
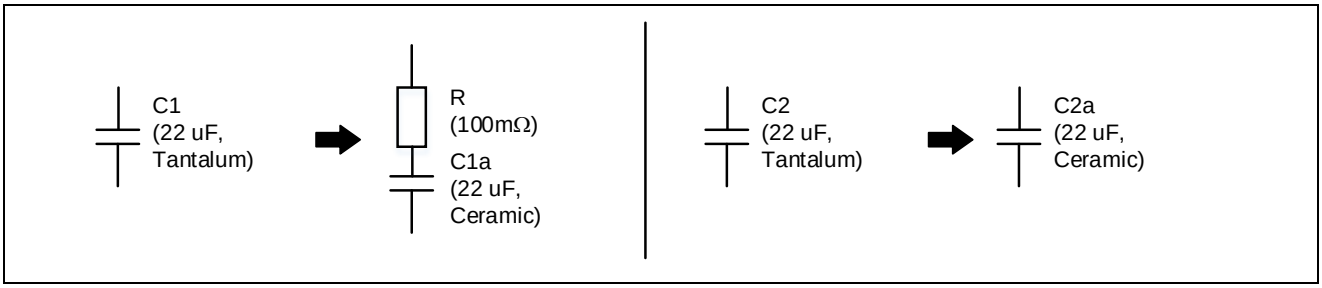


Figure 5.1 Wiring Example of the Regulator Unit (Built-in Regulator Used)

If tantalum capacitors are not available, it is possible to use a resistor and a ceramic capacitor for C1, and a ceramic capacitor for C2.



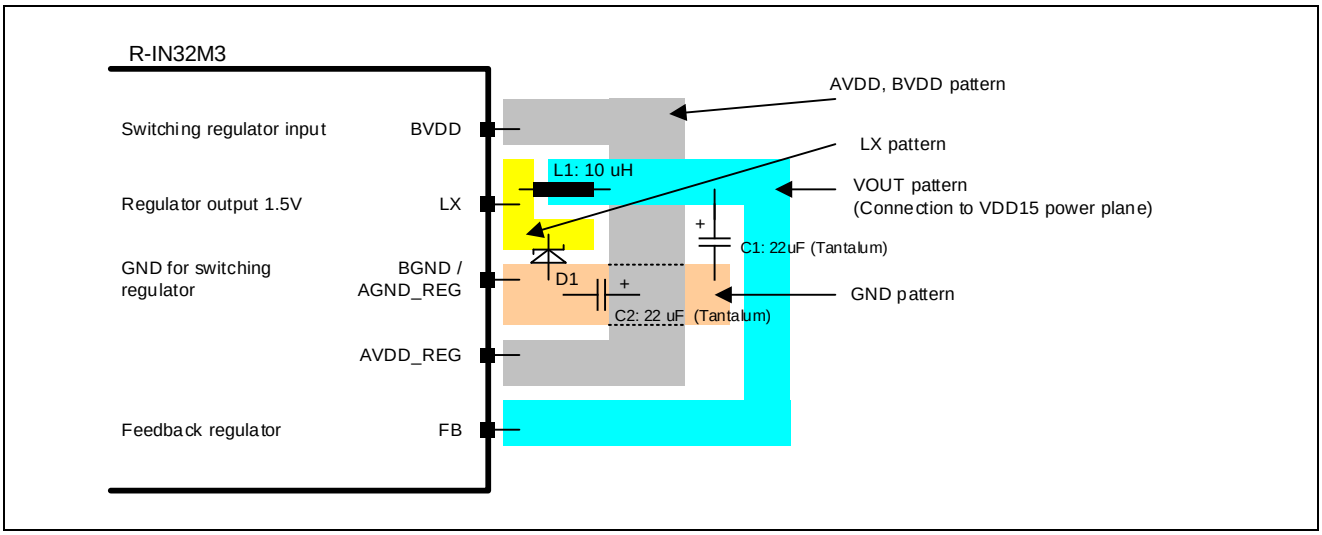


Figure 5.2 Layout Example of the Regulator Section

Table 5.1 List of Recommended Parts for Use

Parts	Type	Characteristics	Recommend Ports
D1	Schottky diode	30 V, 1 A	STPS1L30UPBF (ST)
L1	Inductor	10 uH	VLC5028T (TDK)
C1, C2	Tantalum capacitor	22 uF±20% ESR: 75 to 300 mΩ	PSLB21A226M (NEC TOKIN)
C1a, C2a	Ceramic capacitor	22 uF±10%	GRM32ER71A226KE20L (Murata)
R	Resistor	100 mΩ±1%	MCR18EZHFLR100 (ROHM)

5.2 Built-in Regulator Unused

When the built-in regulator is not in use, make wiring and layout as follows.

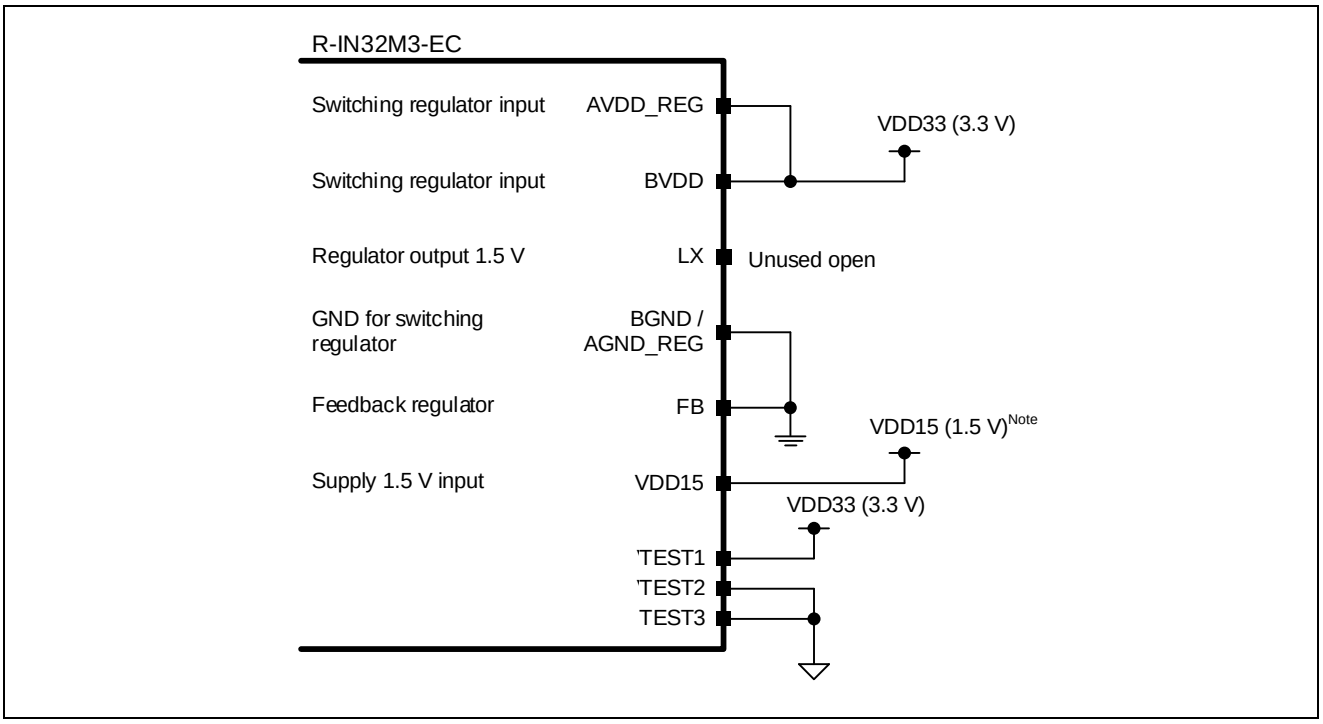


Figure 5.3 Wiring Example of the Regulator Unit (Internal Regulator is Not Used)

Note. Supply stable power supply.

6. GPIO Port Pins

GPIO is a general-purpose I/O port. As for the internal configuration, see the section in the following document.

R-IN32M3-EC: User’s Manual R-IN32M3-EC "2.3.6 Port Signals"

R-IN32M3-CL: User’s Manual R-IN32M3-CL "2.5.6 Port Signals"

7. Ethernet PHY Pins (R-IN32M3-EC Only)

7.1 Ethernet PHY Power Supply Pins

As for analog power supply pins for the built-in Ethernet PHY of the R-IN32M3-EC, power separation by ferrite beads (FB) and the configuration of filters as follows are recommended.

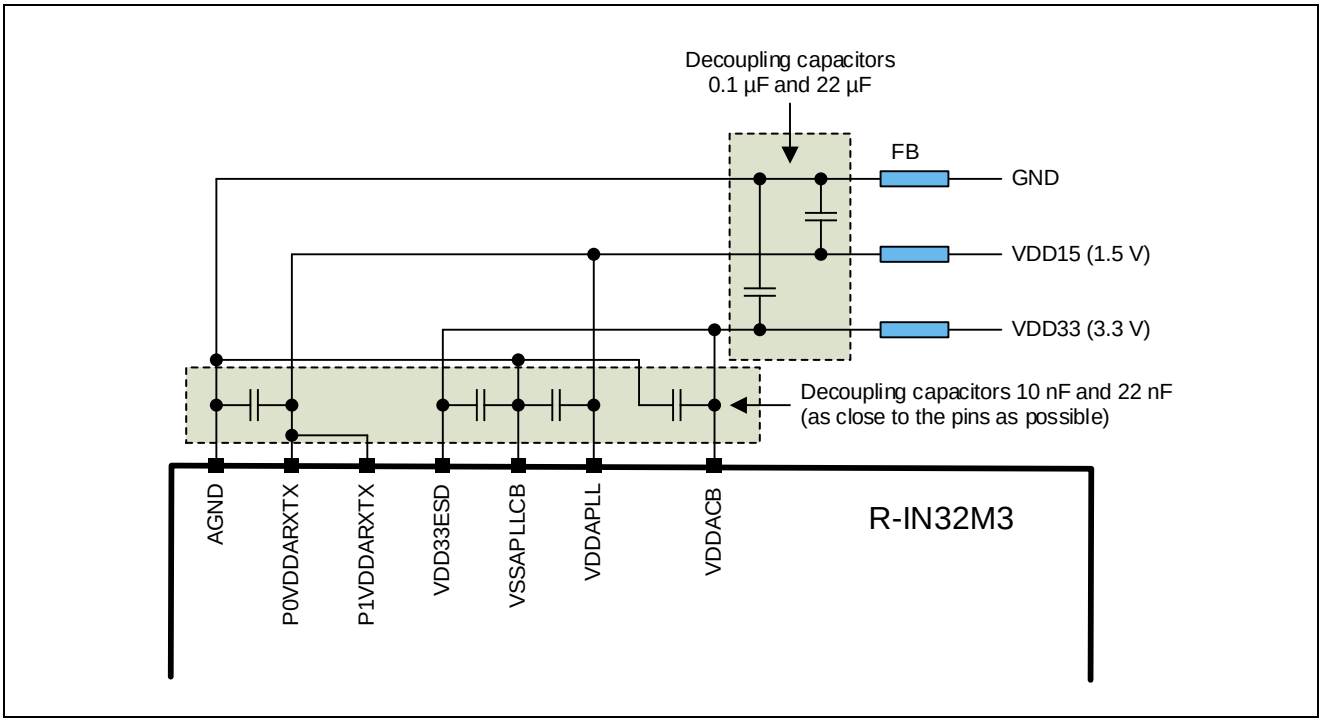


Figure 7.1 Decoupling Capacitors for Power Supply

7.2 100Base-TX Pins

This is an example of connection using the pulse transformer.

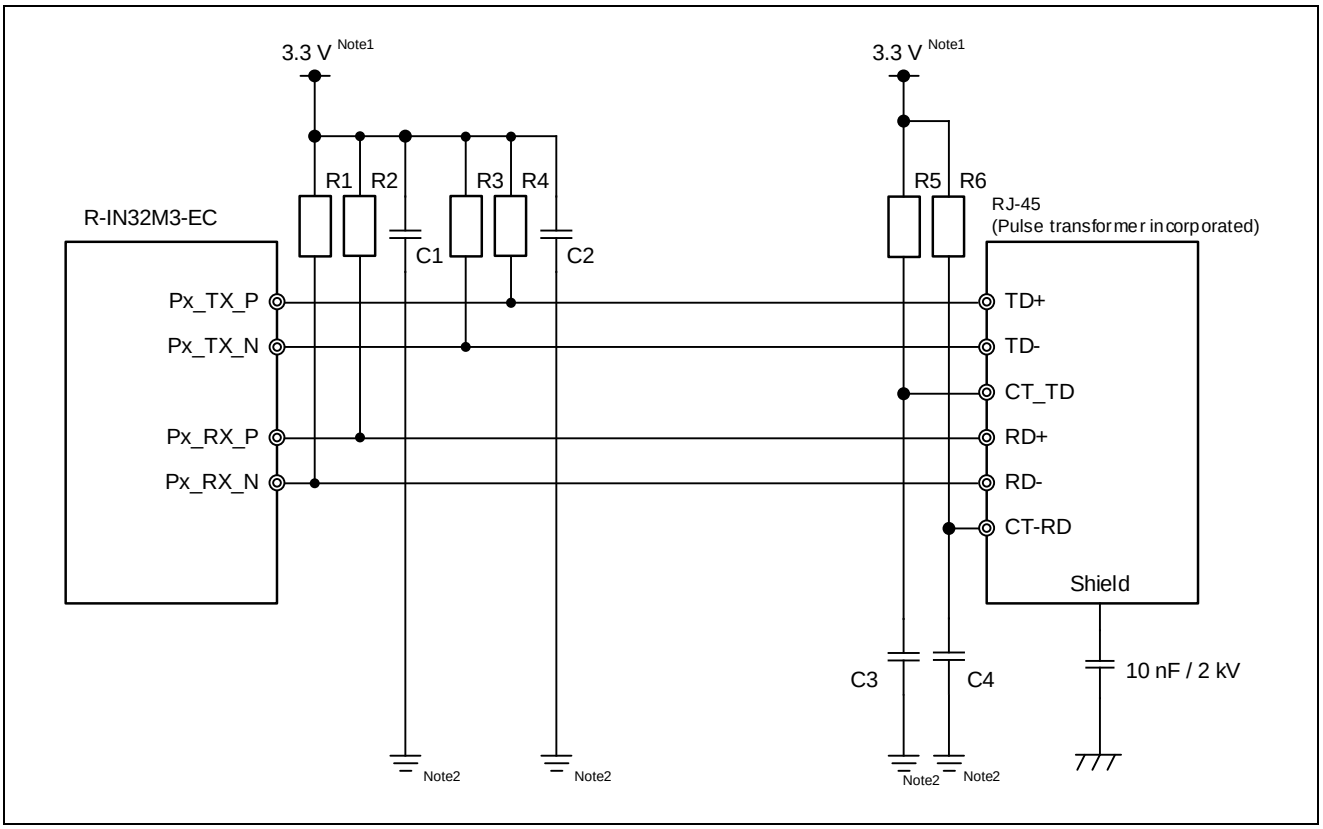


Figure 7.2 Connection Example of R-IN32M3-EC and RJ-45 Connector (Pulse Transformer Incorporated)

Remark. x = 0 or 1

Notes 1. Same potential with VDDACB and VDD33ESD
2. Same potential with AGND

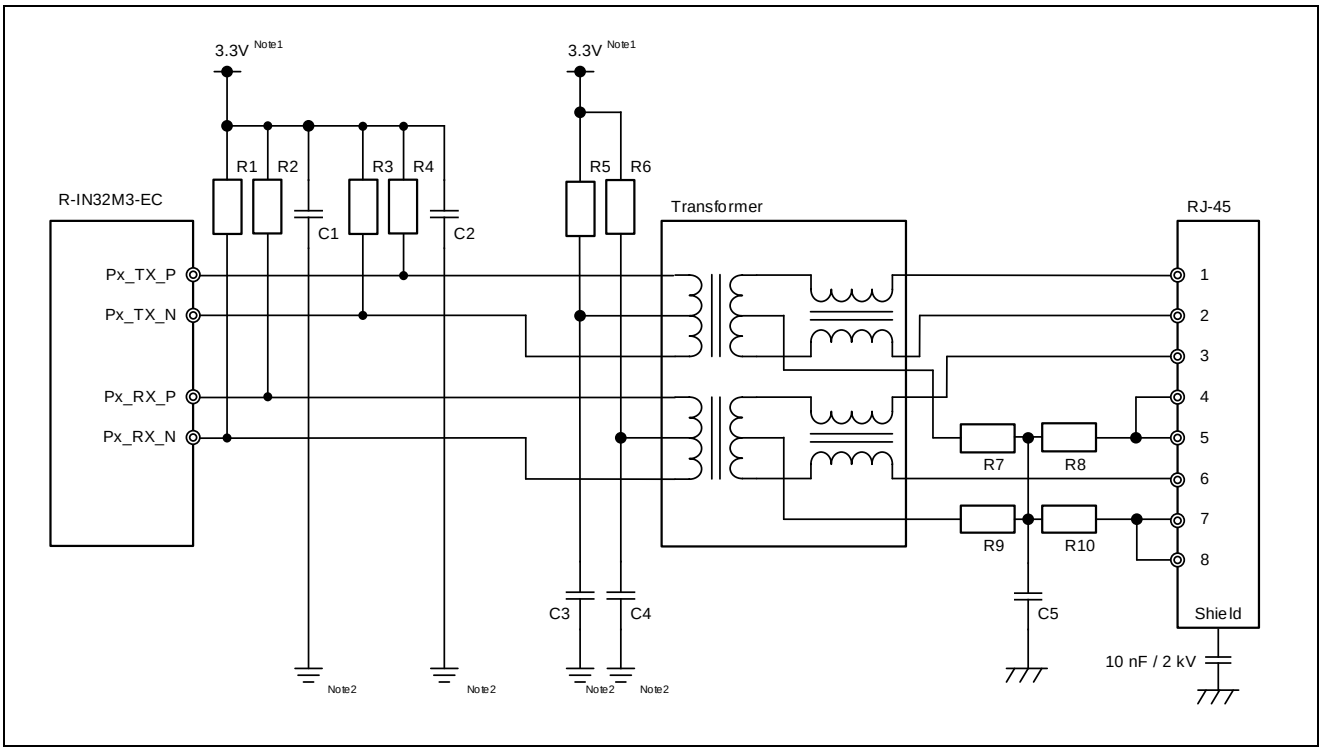


Figure 7.3 Connection Example of R-IN32M3-EC, Pulse Transformer, and RJ-45 Connector

Remark. x = 0 or 1

Notes 1. Same potential with VDDACB and VDD33ESD
2. Same potential with AGND

Table 7.1 Parts List (100Base-TX interface)

Part	Type	Characteristics	Recommended Components
R1, R2, R3, R4	Resistor	49.9Ω±1% 1/16W Note	-
R5, R6	Resistor	10Ω±1% 1/16W Note	-
R7, R8, R9, R10	Resistor	75Ω±1% 1/16W	-
C1	Capacitor	10 nF to 100 nF	-
C2	Capacitor	10 nF to 100 nF	-
C3	Capacitor	10 nF to 22 nF	-
C4	Capacitor	10 nF to 22 nF	-
C5	Capacitor	4.7 nF±10%	-
Pulse transformer		One channel	Pulse Electronics H1012NL, H1102NL
		Two channels	Pulse Electronics H1270N+, HX1294
RJ-45 connector (Pulse transformer incorporated)		Two channels	Pulse Electronics JG0-0031NL

Note. We recommend 1/8W when using in harsh environments, such as at high temperature.

The wiring on the board, note the following.

- Long wires should be avoided. R-IN32M3 and, the transformer, and the connector should be placed together as close as possible.
- Crossing of differential traces with other lines and among each other should be avoided. The components should be placed that way that crossing of differential pairs of TxP/N and RxP/N is not necessary.
- Differential lines should be routed straight and as short as possible.
- Lines should bend with 135 degree angle or more. (Figure 7.4)
- Traces between R-IN32M3-EC, transformer and RJ-45 connector should be designed with a differential impedance of 100Ω±10% and with an impedance of 50Ω related to GND.
- The traces of a differential pair should match in length. 0.5mm is the maximum deviation. Adjustments of the length should be done at the connector, device or transformer.
- Additional to the length the single traces should be designed symmetrical. They should be parallel and routed in the same layer with continuous width and a preferable fixed spacing. Components, vias and connections should also be symmetrical.
- Stubs should be avoided.
- Preferable is a large edge gap at differential pairs. An empty space of five times of the trace width between differential pair and other signals, planes or components is recommended.
- Differential lines should not cross edges of the GND/supply plane, other planes or voids in the layer below. For continuous impedance a GND plane in the layer below is preferable.
- Beneath the magnetics no lines or planes should be routed.
- Preferable differential pairs should be routed via as little vias as possible. If vias are necessary, note the following:
  (a) Vias of the related plane (e.g. AGND) should be placed near the signal vias. The distance between signal via and GND via should be equal to the distance between the layers to avoid a discontinuity of the impedance. (See Figure 7.6)
  (b) Void and no planes between and around the signal vias. Metal of planes close to the differential vias could influence the impedance.
  (c) The diameter of the vias should be almost equal to the trace width. (See Figure 7.6)

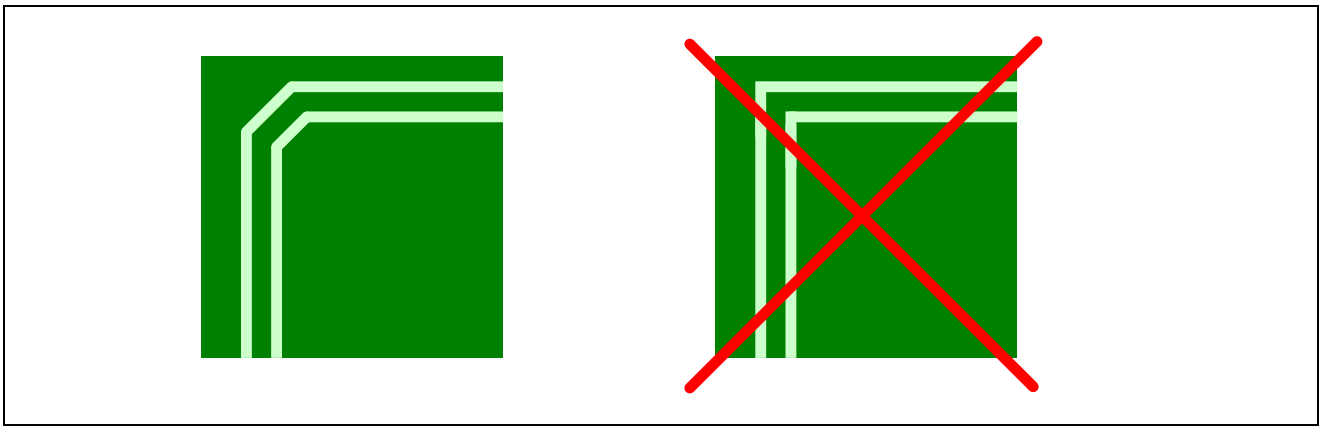


Figure 7.4 Wiring Example of the Differential Signal Transmission Line (1)

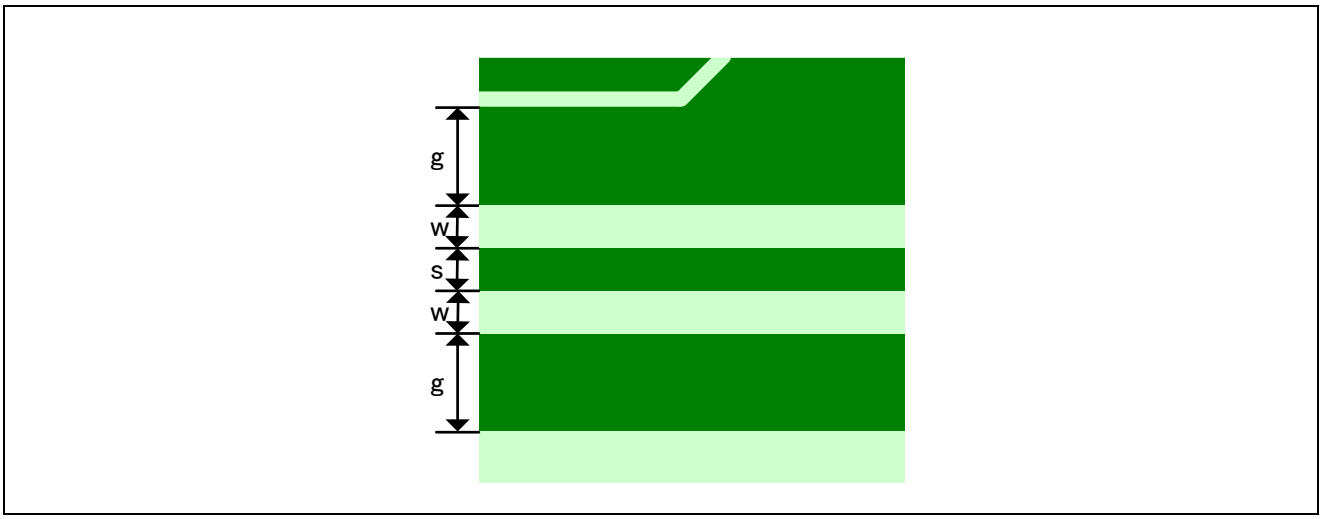


Figure 7.5 Wiring Example of the Differential Signal Transmission Line (2)

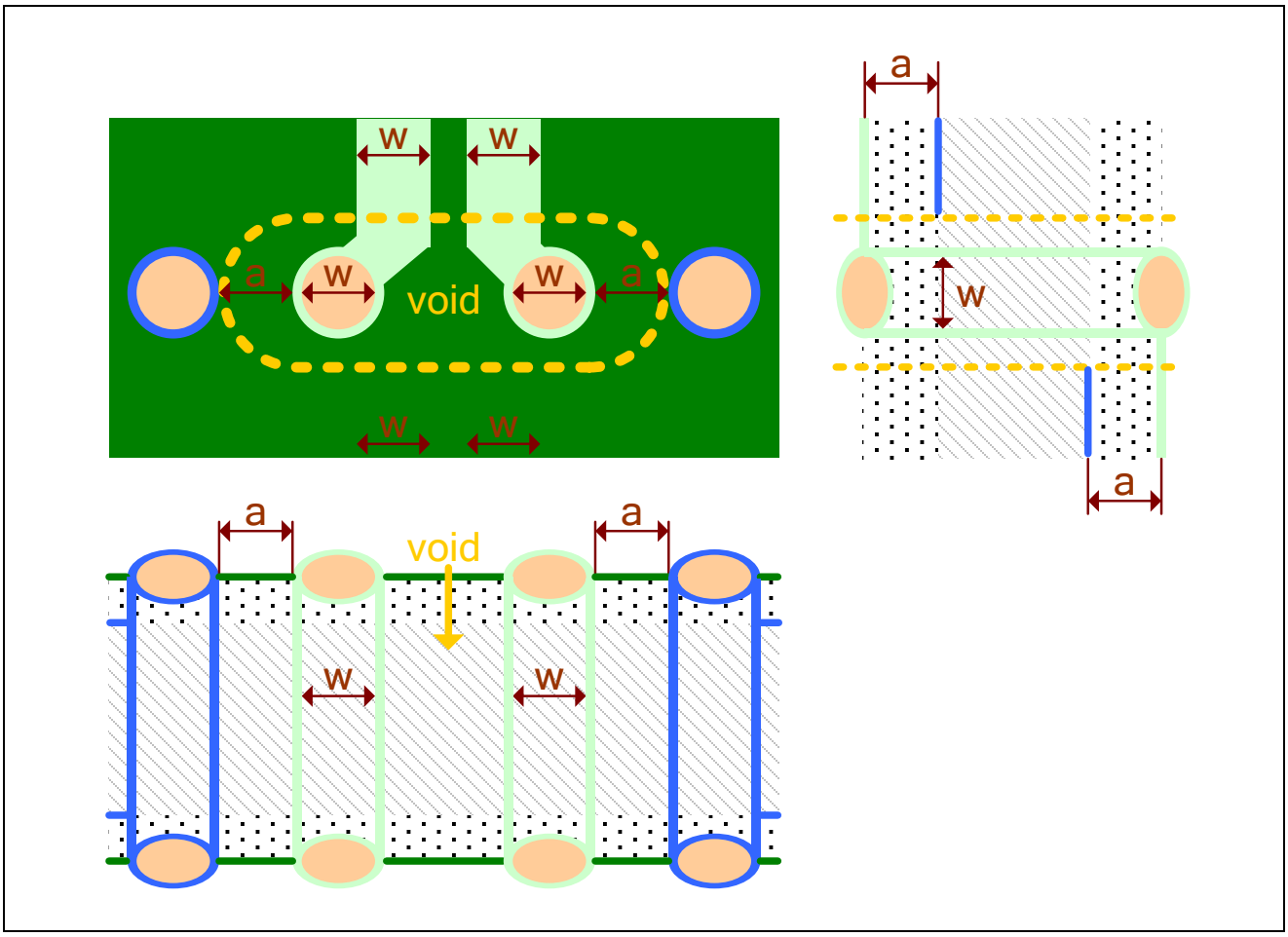


Figure 7.6 Wiring Example of the Differential Signal Transmission Line (3)

7.3 100Base-FX Pins (Optical Fiber)

An example of a connection with an optical fiber module is indicated below. As for the notes of the differential signal transmission line, refer to "7.2 100Base-TX Pins".

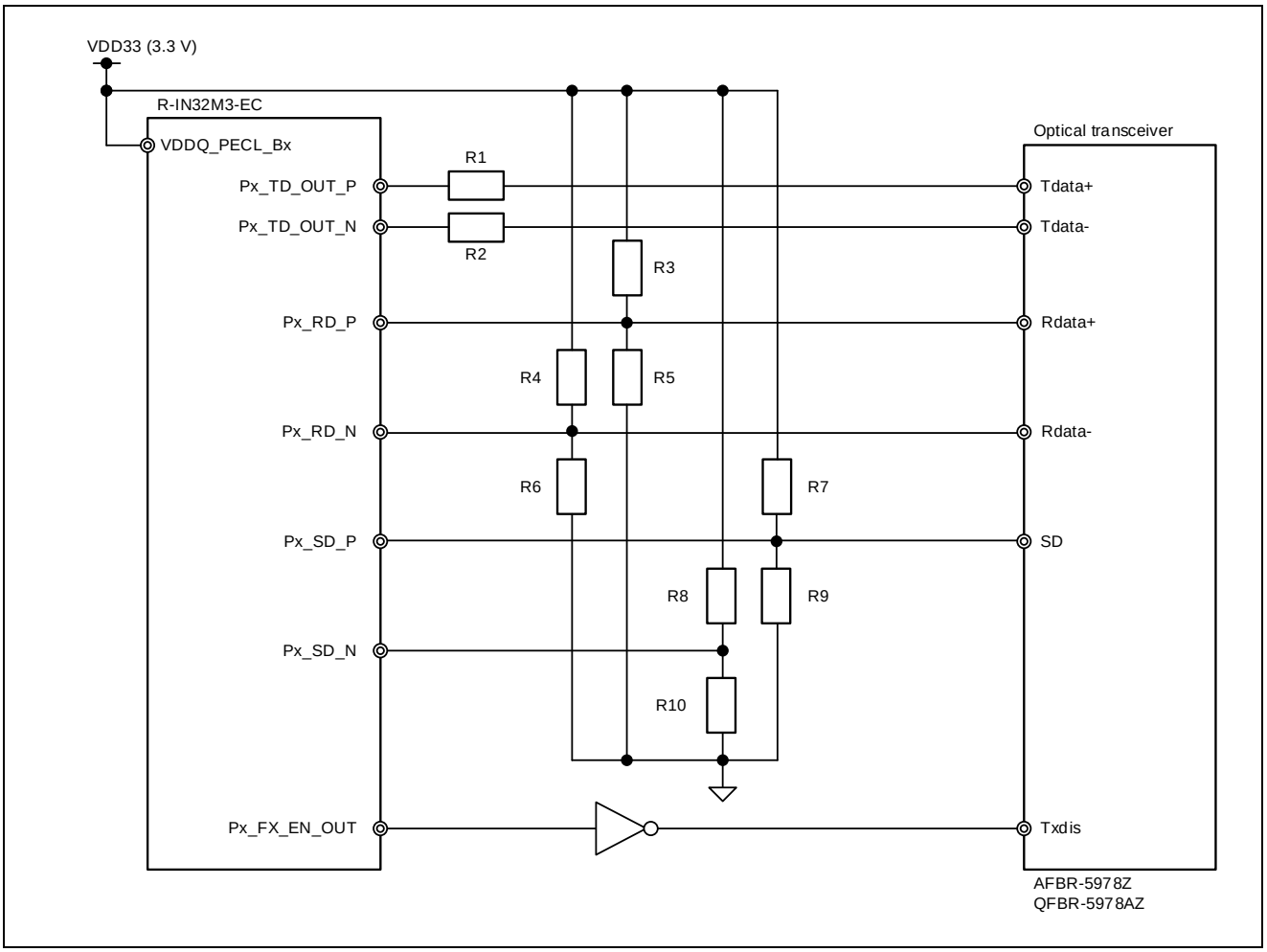


Figure 7.7 Interface Circuit with Optical Transceiver

Remark. x = 0 or 1

Table 7.2 Part List (100Base-FX Interface)

Part	Type	Characteristics	Recommended components
R1, R2	Resistor	150Ω±1%	-
R3, R4, R7	Resistor	130Ω±1%	-
R5, R6, R9	Resistor	82Ω±1%	-
R8	Resistor	86.6Ω±1%	-
R10	Resistor	127Ω±1%	-
Optical transceiver		One channel	AvagoTechnologies AFBR-5978Z, QFBR-5978AZ

8. GMII Pins (R-IN32M3-CL Only)

Figure 8.1 shows a connection image of R-IN32M3-CL and Gigabit Ethernet PHY.

The value of damping resistors should be 33Ω within a tolerance of 5%, and the damping resistors should be put in the nearest point of the R-IN32M3-CL. In addition, wires of target pins (which is GTXC, TXDx, TXEN and TXER) are recommended to be short and equal-length.

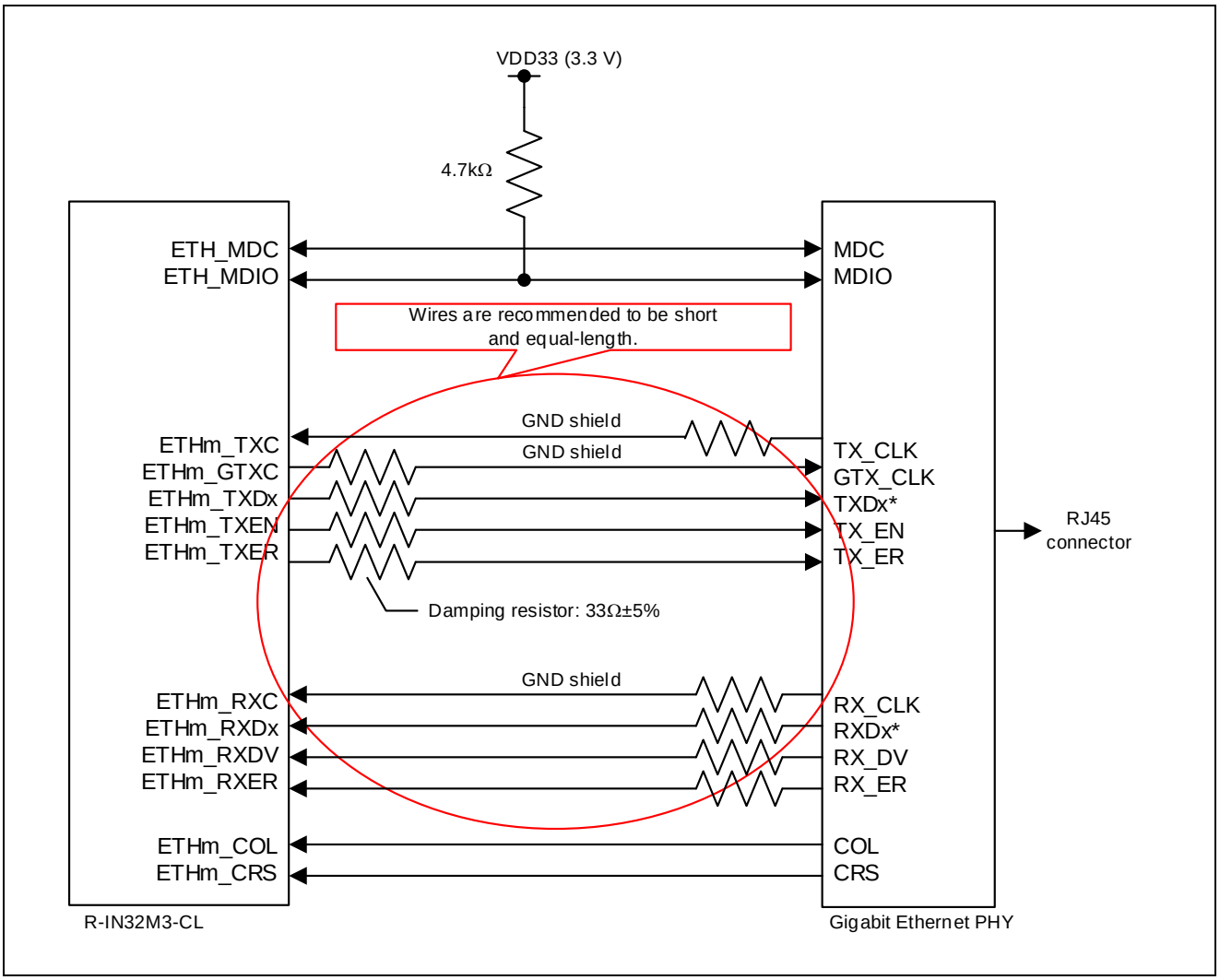


Figure 8.1 Connection Image of R-IN32M3-CL and Gigabit Ethernet PHY

Remark. m = 0, 1, x = 0 to 7

8.1 Selection of GMII Peripheral Components

Select the parts with care to the following.

- Selection of PHY

  Full-duplex products IEEE802.3 1000BASE-T.

  Parts that have the auto-negotiation function.

  Parts with a GMII interface.

  Parts that have the auto MDI/MDIX negotiation function.

  Operable parts at 125 MHz about MDC clock frequency.

- Selection of the crystal oscillator for PHY

  Regarding Jitter and frequency, select the parts to adapt to the requirement of the PHY.

8.2 Circuit Design around GMII

Design the GMII peripheral circuits with care to the following.

- Wiring of GMII

  Put the damping resistor of overshoot/undershoot protection.

- For PHY address

  Set to the same address as the port number of the R-IN32M3-CL to the PHY address.

  Connect the PHY assigned to address 0 to MAC port 0, and connect the PHY assigned to address 1 to MAC port 1.

8.3 Pattern Design around GMII

Design the pattern of GMII peripheral circuits with care to the following.

- Wiring of GMII

  The wiring pattern of the signal (GMII) to connect R-IN32M3-CL and PHY should be the shortest. Choose the thickness of the wiring pattern and signal lines for the pattern to be an impedance of 50Ω.

  Do not bend at 45 degrees or less to signal pattern.

  For the power/GND pattern, use the wiring with a thick pattern as much as possible.

9. CC-Link Pins

The connection example for CC-Link Remote device station is shown in Figure 9.1.

For notes on the implementation of the CC-Link, refer to *CC-Link Specifications: Implementation Specification* (BAP-05027) issued by the CC-Link Partner Association. Please contact the CC-Link Partner Association (CLPA) with any requests for the corresponding material.

CC-Link Partner Association (CLPA)	TEL: 052-919-1588
	FAX: 052-916-8655
	Email: info@cc-link.org
	Web: https://www.cc-link.org/

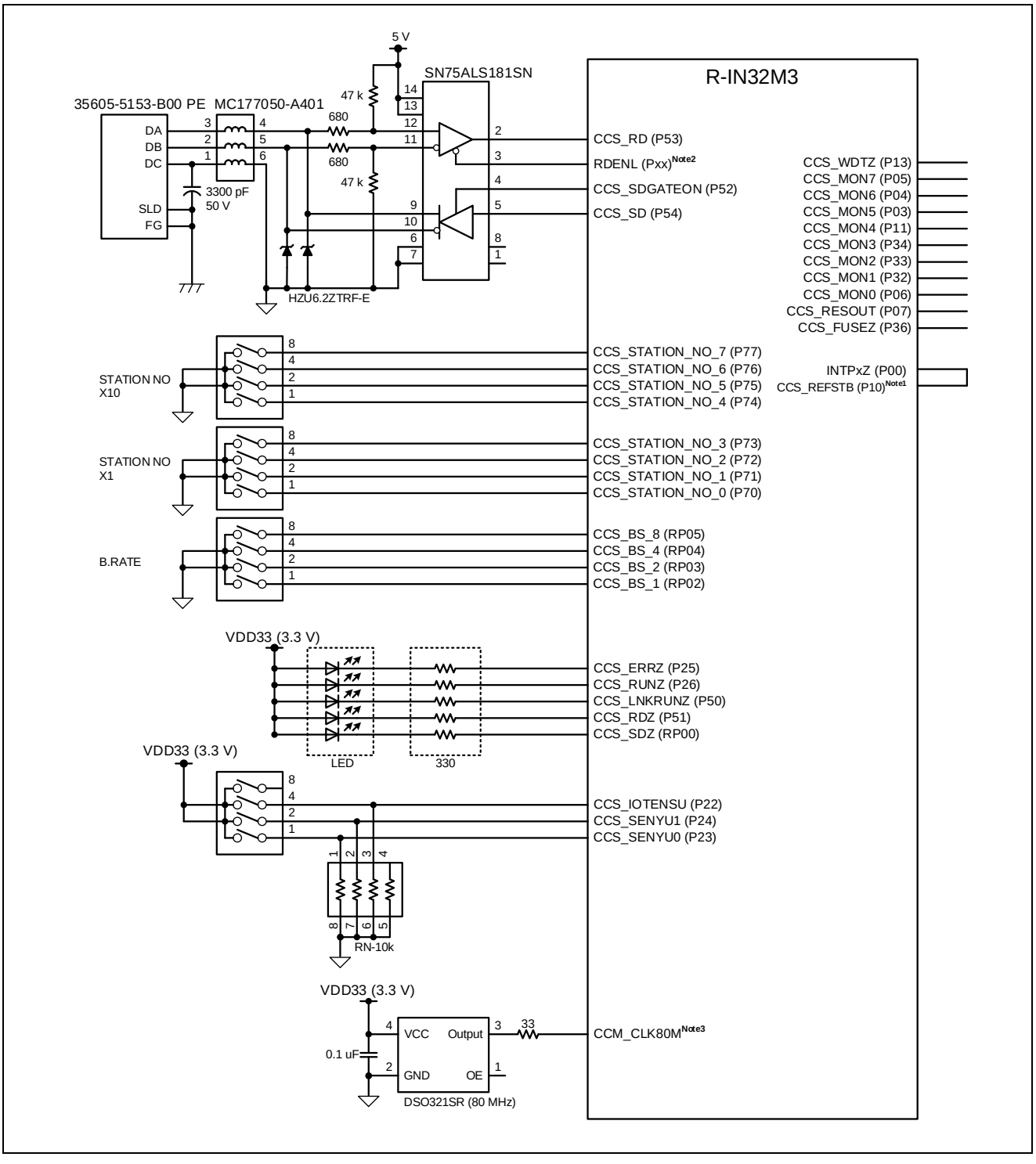


Figure 9.1 Connection Example for CC-Link Remote Device Station

Notes 1. The CCS_REFSTB (P10) pin is needed to be connected to the port pin which has external interrupt function (INTPZ).

2. The RDENL pin should be connected to a general output port.

3. This pin is multiplexed with CC-Link (intelligent device station).

10. Notes of CC-Link IE Field Use (Only R-IN32M3-CL)

When booting in external memory boot mode, external serial flash ROM boot mode, and instruction RAM boot mode, drive the P33 (multiplexed with CCI_WAITEDGEH) and P34 (multiplexed with CCI_WRLENH) pins high during a reset.

If the P33 and P34 pins are driven low during a reset, accessing the CC-Link IE field from the CPU in the R-IN32M3 is not possible.

11. External MCU/Memory Interface Pins

This LSI is able to connect to an external MCU or memory.

The connection mode is decided by the signal level of the MEMIFSEL, MEMCSEL, HIFSYNC, and ADMUXMODE pins as shown in Table 11.1.

Table 11.1 Mode Selection of External MCU/Memory Connection

Mode Setting				External Connection Mode
MEMIFSEL	MEMCSEL	HIFSYNC	ADMUXMODE	
Low	Low	-	-	External memory interface Asynchronous SRAM MEMC
	High	-	-	External memory interface Synchronous burst access MEMC
High	Low	Low	-	External MCU interface Asynchronous SRAM interface mode
		High	-	External MCU interface Synchronous SRAM interface mode Note
	High	Low	-	Setting prohibited
		High	Low	Setting prohibited
			High	External MCU interface Synchronous SRAM-type transfer mode (address/data multiplexed)

Note. Before access to the CC-Link IE field, select the synchronous SRAM interface mode (MEMIFSEL high, MEMCSEL low, HIFSYNC high). (The CC-Link IE field is incorporated only in the R-IN32M3-CL.)

The connection example for each modes is shown in the following sections.

11.1 External MCU Interface

The external MCU interface is multiplexed with the external memory interface. When the MEMIFSEL pin is set to the high level, it functions as the external MCU interface.

The external MCU interface supports the asynchronous SRAM interface mode and the synchronous SRAM interface mode. When the level of a HIFSYNC pin is high, it functions as a synchronous SRAM interface, and when HIFSYNC is set to low, it functions as an asynchronous SRAM interface. (see Table 11.1.)

Moreover, the external MCU interface supports the synchronous SRAM type transfer of clock synchronization so that mass data can be accessed at high speed. This function is enabled by setting the MEMIFSEL and MEMCSEL pins to the high level.

11.1.1 Asynchronous SRAM Interface Mode

The following figure shows a general connection example in asynchronous SRAM interface mode, when this LSI chip is connected as a slave device to an external MCU.

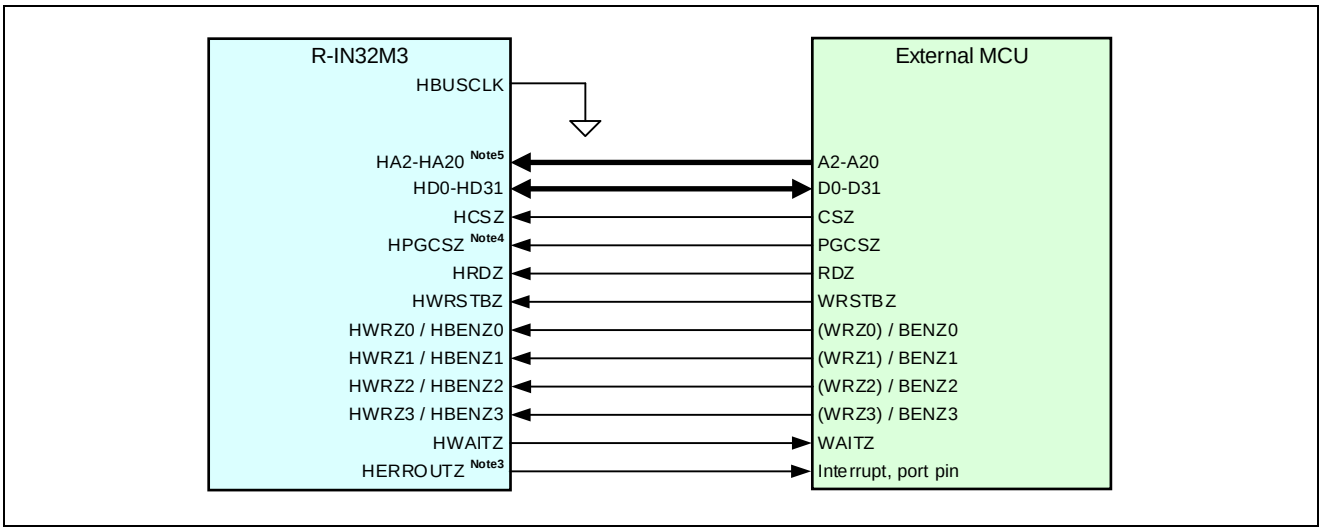


Figure 11.1 Connection Example of 32-Bit External MCU Interface (Asynchronous SRAM Interface Mode)

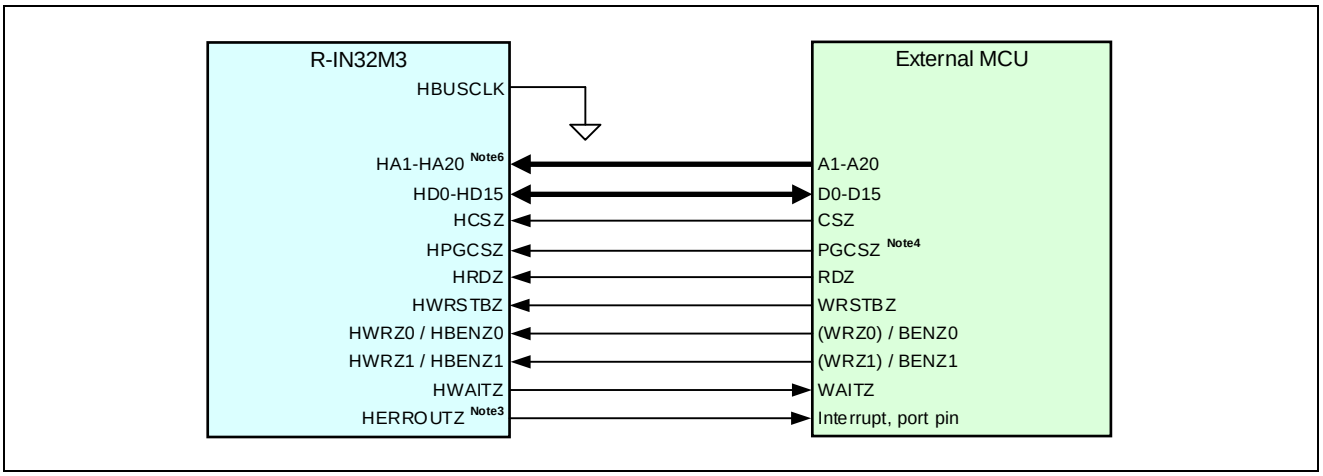


Figure 11.2 Connection Example of 16-Bit External MCU Interface (Asynchronous SRAM Interface Mode)

Notes 1. The details of signal connection depend on the bus interface specification of the host MCU. Confirm the product specification of MCU which is connected to this LSI.

2. HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are multiplexed on the same pins, and the pin functions are selected by the level on the HWRZSEL pin.

3. Connecting the HERROUTZ signal is not indispensable. Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

4. **This is a chip-select signal supporting paged access. Connect it if required.**
5. **Connected the address signal for a 4-byte boundary from the destination to the HA2 pin of this LSI.**
6. **Connected the address signal for a 2-byte boundary from the destination to the HA1 pin of this LSI.**

11.1.2 Synchronous SRAM Interface Mode

The following figure shows a general connection example in synchronous SRAM interface mode, when this LSI chip is connected as a slave device to an external MCU.

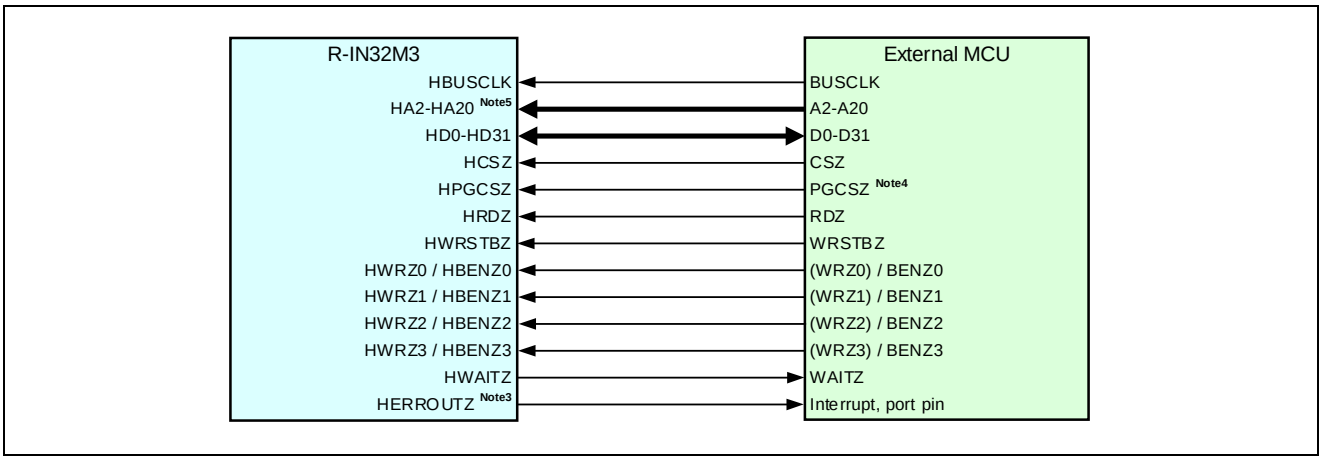


Figure 11.3 Connection Example of 32-Bit External MCU Interface (Synchronous SRAM Interface Mode)

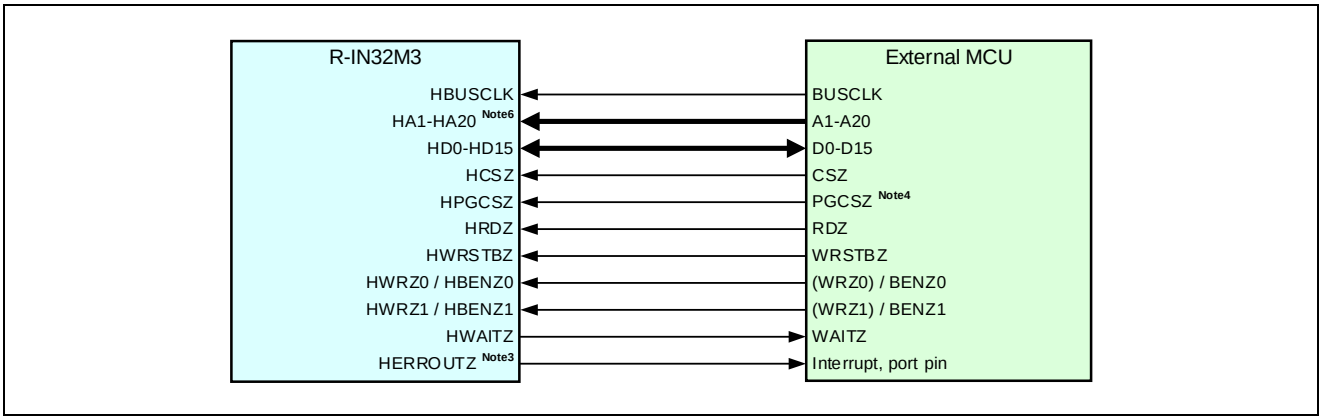


Figure 11.4 Connection Example of 16-Bit External MCU Interface (Synchronous SRAM Interface Mode)

Notes 1. The details of signal connection depend on the bus interface specification of the host MCU. Confirm the product specification of MCU which is connected to this LSI.

2. HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are multiplexed on the same pins, and the pin functions are selected by the level on the HWRZSEL pin.

3. Connecting the HERROUTZ signal is not indispensable. Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

4. This is a chip-select signal supporting paged access. Connect it if required.

5. Connected the address signal for a 4-byte boundary from the destination to the HA2 pin of this LSI.

6. Connected the address signal for a 2-byte boundary from the destination to the HA1 pin of this LSI.

11.1.3 Synchronous SRAM-Type Transfer Mode

The following figure shows a general connection example in synchronous SRAM-type transfer mode, when this LSI chip is connected as a slave device to an external MCU. When setting this mode, enable "address/data multiplex" function (the ADMUXMODE pin should be driven high).

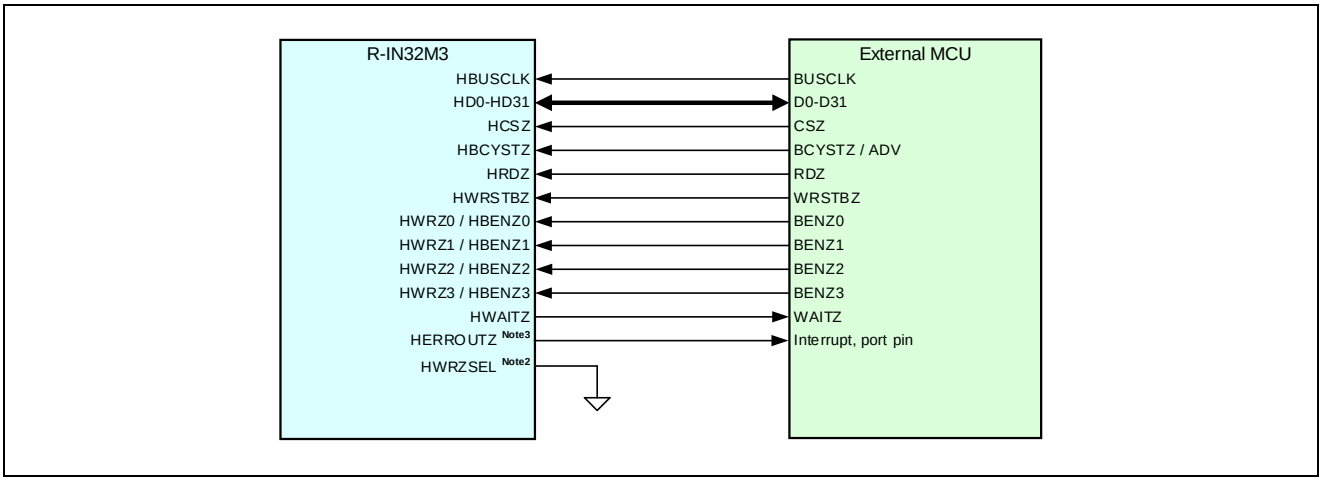


Figure 11.5 Connection Example of 32-Bit External MCU Interface (Synchronous SRAM-Type Transfer Mode)

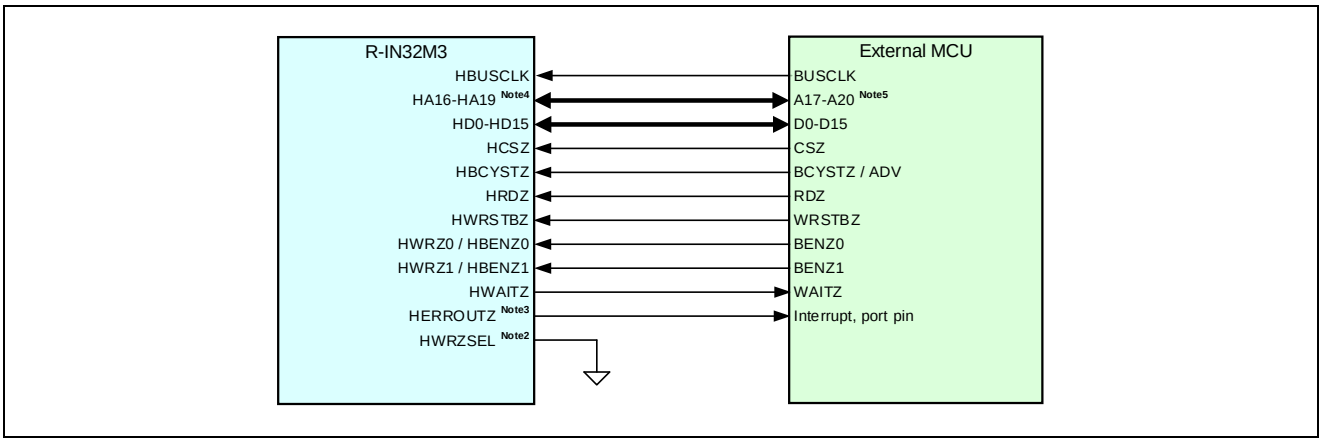


Figure 11.6 Connection Example of 16-Bit External MCU Interface (Synchronous SRAM-Type Transfer Mode)

Notes 1. The details of signal connection depend on the bus interface specification of the host MCU. Confirm the product specification of MCU which is connected to this LSI.

2. In this mode, the HWRZSEL pin has to be set to low level.

3. Connecting the HERROUTZ signal is not indispensable. Connect it to an interrupt or general-purpose port input of the MCU to be connected, if required.

4. Connected the address signal for a 128-Kbyte boundary from the destination to the HA16 pin of this LSI.

5. Accessed is by byte-wise addressing.

11.2 External Memory Interface

This section describes the connection as a master device to an external memory.

The operating connection mode of the external memory interface depends on the level of the signal on the MEMCSEL pin (see Table 11.1).

11.2.1 Asynchronous SRAM MEMC

The asynchronous SRAM MEMC is externally connectable to paged ROM, ROM, SRAM, or peripheral devices with an interface similar to the SRAM interface via a 16- or 32-bit bus.

The external MCU interfaces for the asynchronous SRAM MEMC and the synchronous method burst access MEMC are multiplexed with each other. When both the MEMCSEL and MEMIFSEL pins are at the low level, the asynchronous SRAM MEMC can be used.

When both the BOOT0 and BOOT1 pins are at the low level, booting up proceeds from the memory connected to CSZ0.

11.2.1.1 Connection Example with SRAM

The following figure shows an example when this LSI chip is connected to SRAM.

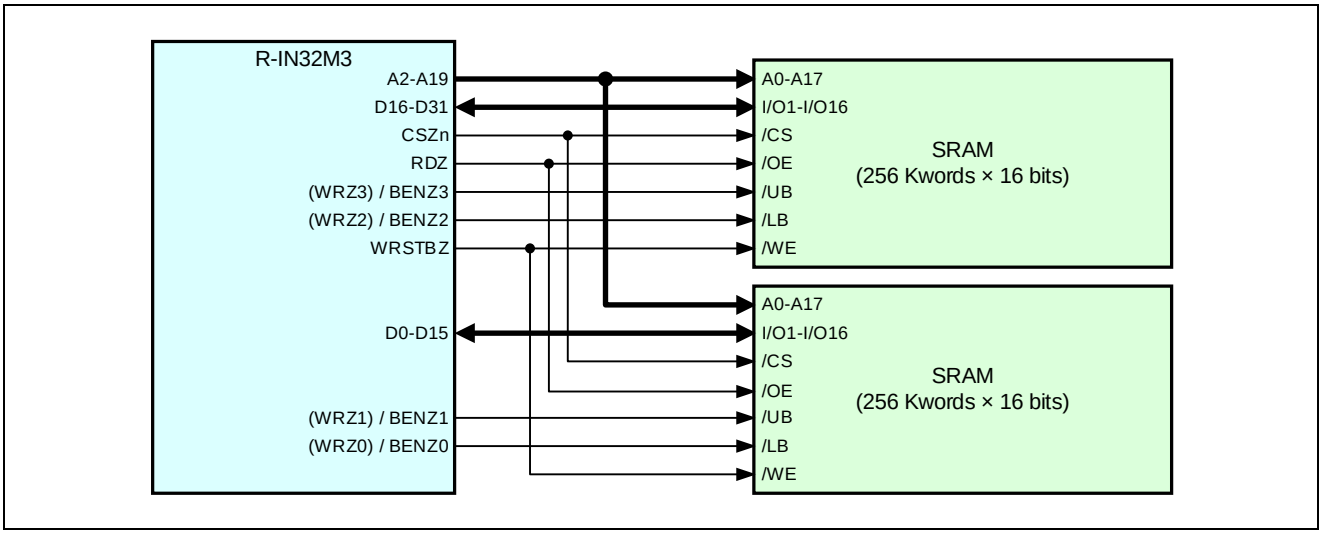


Figure 11.7 Connection Example with 32-Bit SRAM (Asynchronous SRAM MEMC)

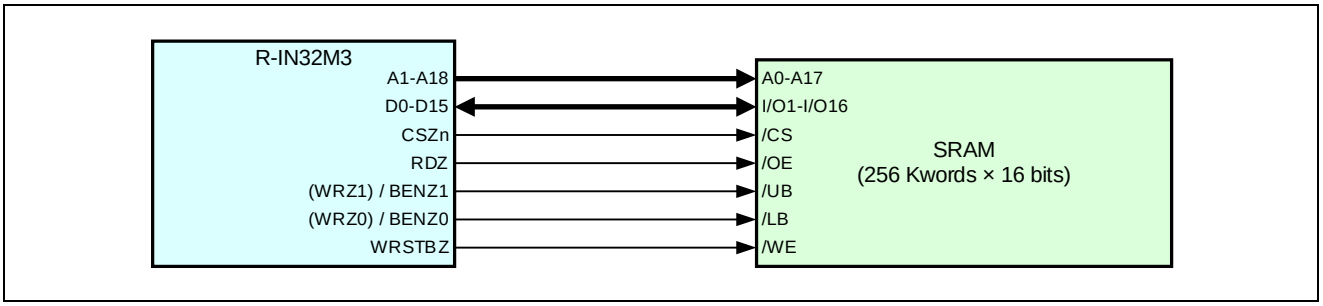


Figure 11.8 Connection Example with 16-Bit SRAM (Asynchronous SRAM MEMC)

Remark. n = 0 to 3

11.2.1.2 Connection Example with Paged ROM

The following figure shows an example when this LSI chip is connected to paged ROM.

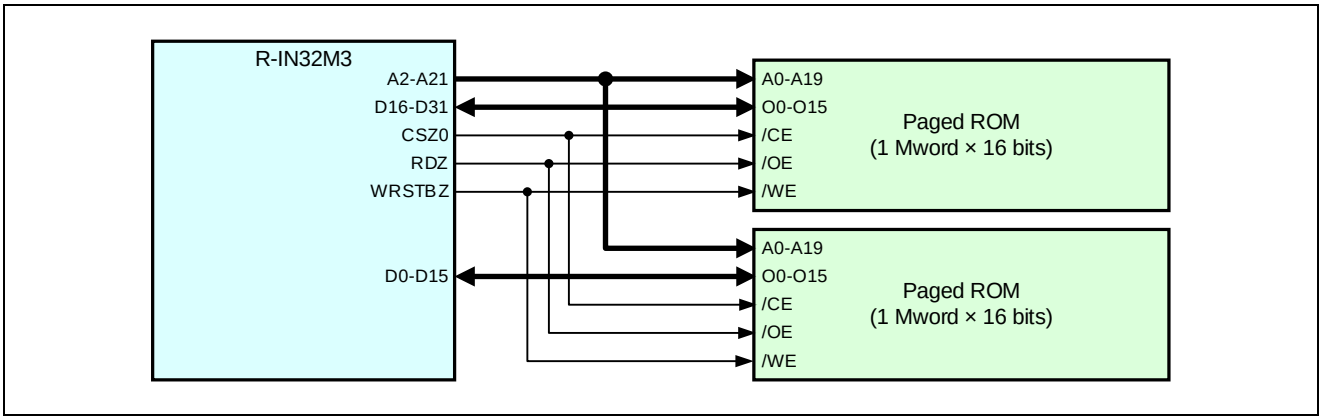


Figure 11.9 Connection Example with 32-Bit Paged ROM (Asynchronous SRAM MEMC)

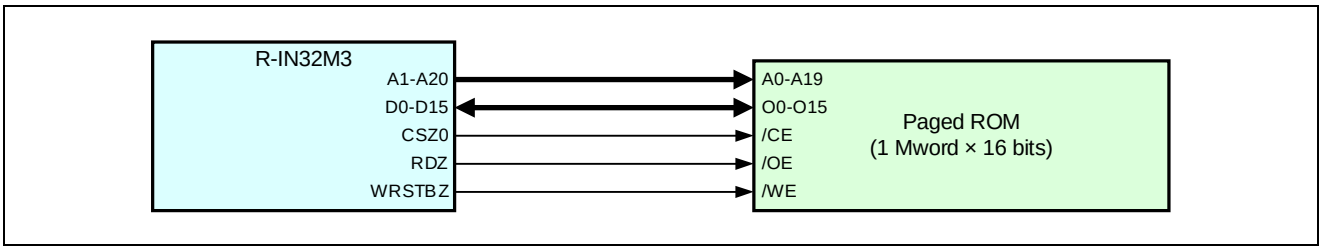


Figure 11.10 Connection Example with 16-Bit Paged ROM (Asynchronous SRAM MEMC)

Caution. The on-page mode of paged ROM is available only when the ROM is connected to CSZ0.

11.2.2 Synchronous Burst Access MEMC

The synchronous burst access MEMC is externally connectable to paged ROM, ROM, SRAM, PSRAM, NOR-flash memory, or peripheral devices with an interface similar to the SRAM interface via a 16- or 32-bit bus.

By setting the ADMUXMODE pin to high level, the address signals can be multiplexed to be output from data pins.

The external MCU interfaces for the synchronous burst access MEMC and the asynchronous SRAM MEMC are multiplexed with each other. When the MEMCSEL and MEMIFSEL pins are set to high level and low level respectively, the synchronous burst access MEMC can be used.

When both the BOOT0 and BOOT1 pins are at low level, booting up proceeds from the memory connected to CSZ0.

11.2.2.1 Connection Example with SRAM

The following figure shows an example when this LSI chip is connected to SRAM.

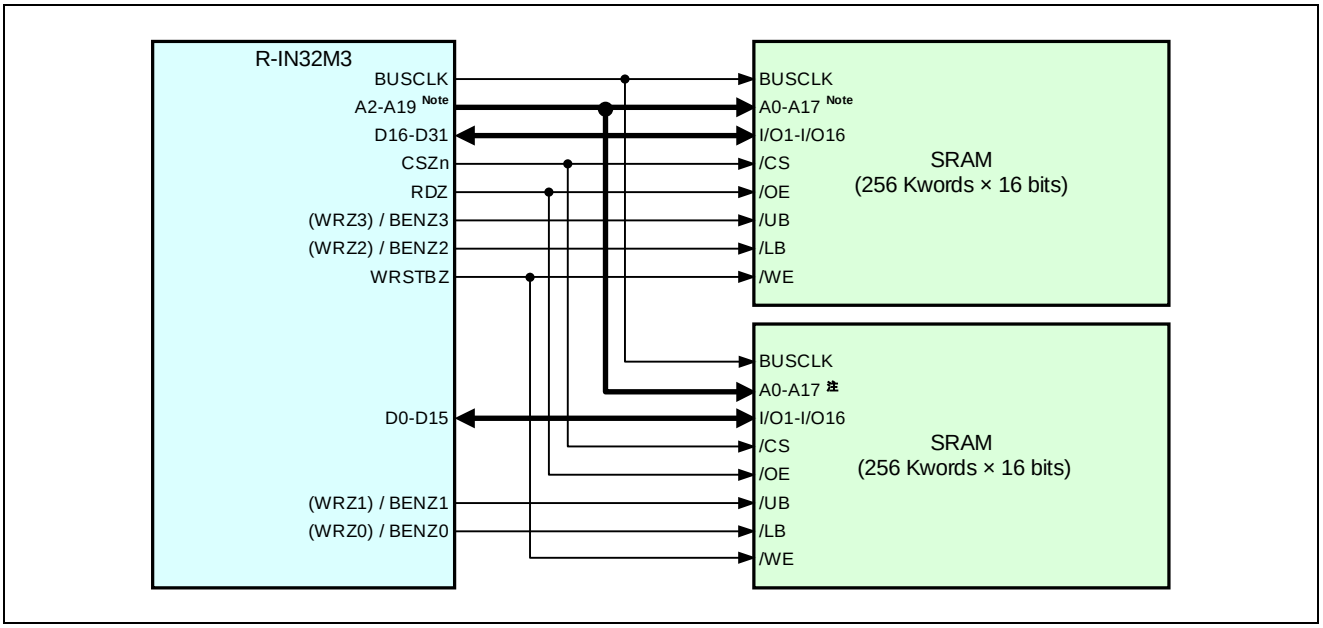


Figure 11.11 Connection Example with 32-Bit SRAM (Synchronous Burst Access MEMC)

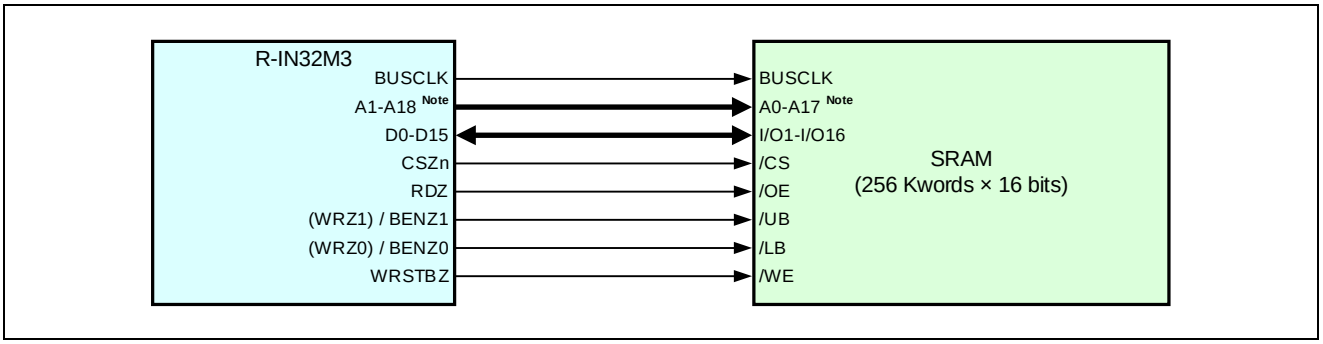


Figure 11.12 Connection Example with 16-Bit SRAM (Synchronous Burst Access MEMC)

Remark. n = 0 to 3

Note: When the "address/data multiplexing" feature is enabled (the ADMUXMODE pin is at the high level), separate connection of the address bus is not required.

11.2.2.2 Connection Example with Paged ROM

The following figure shows an example when this LSI chip is connected to paged ROM.

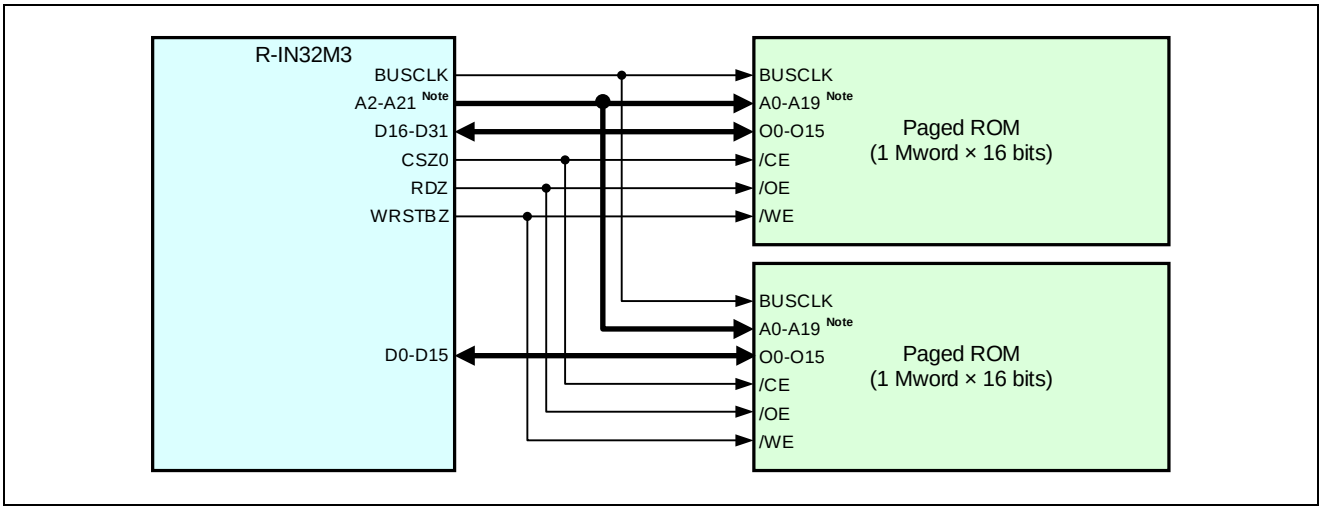


Figure 11.13 Connection Example with 32-Bit Paged ROM (Synchronous Burst Access MEMC)

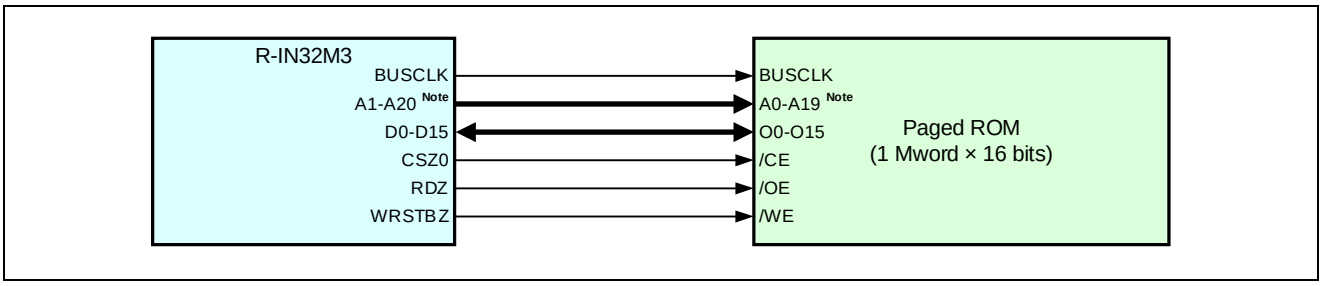


Figure 11.14 Connection Example with 16-Bit Paged ROM (Synchronous Burst Access MEMC)

Caution. The on-page mode of page ROM is available only when the ROM is connected to CSZ0.

Note. When the "address/data multiplexing" feature is enabled (the ADMUXMODE pin is at the high level), separate connection of the address bus is not required.

12. Serial Flash ROM Connection Pins

This LSI chip has a memory controller to connect the serial flash ROM that supports the SPI compatible interface.

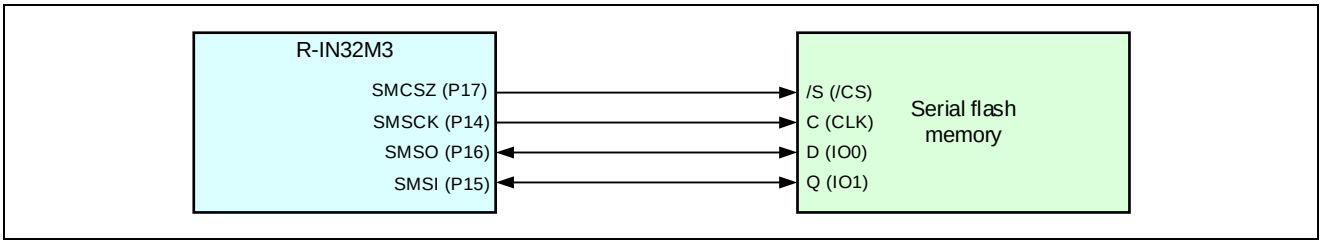


Figure 12.1 Connection Example with Serial Flash ROM <R>

13. Asynchronous Serial Interface J Connection Pins

Figure 13.1 shows a connection example between the R-IN32M3 and the asynchronous serial interface J (UARTJn) device.

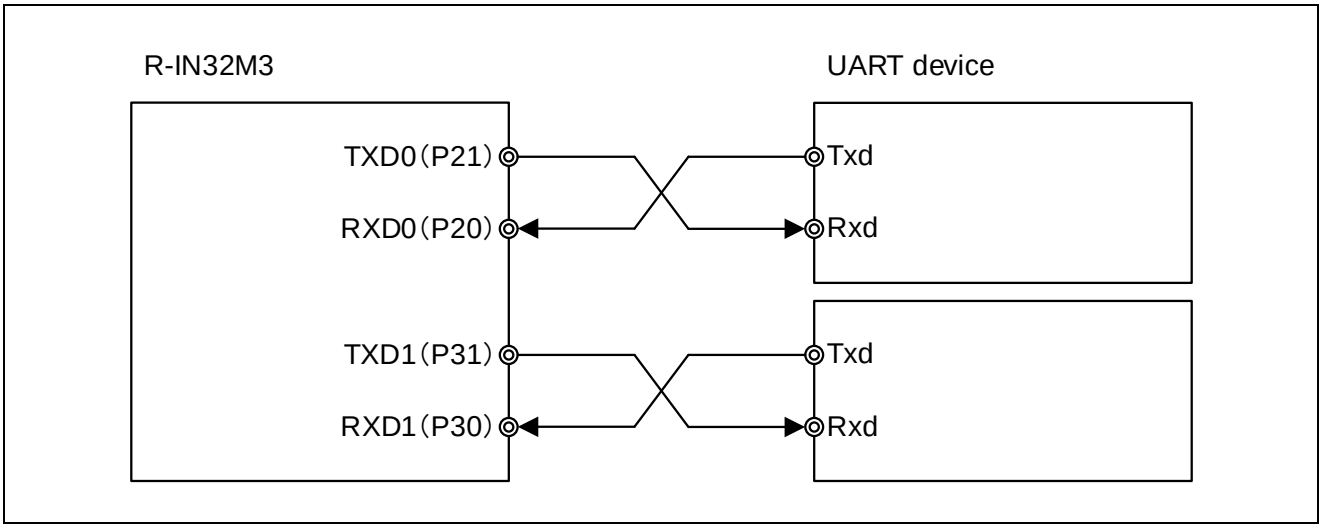


Figure 13.1 Connection Example between R-IN32M3 and UART Device

14. I^2C Connection Pins

Figure 14.1 shows a connection example between the R-IN32M3 and the I^2C slave device.

Since the serial clock line and serial data line are N-ch. open drain outputs, external pull-up resistors are required.

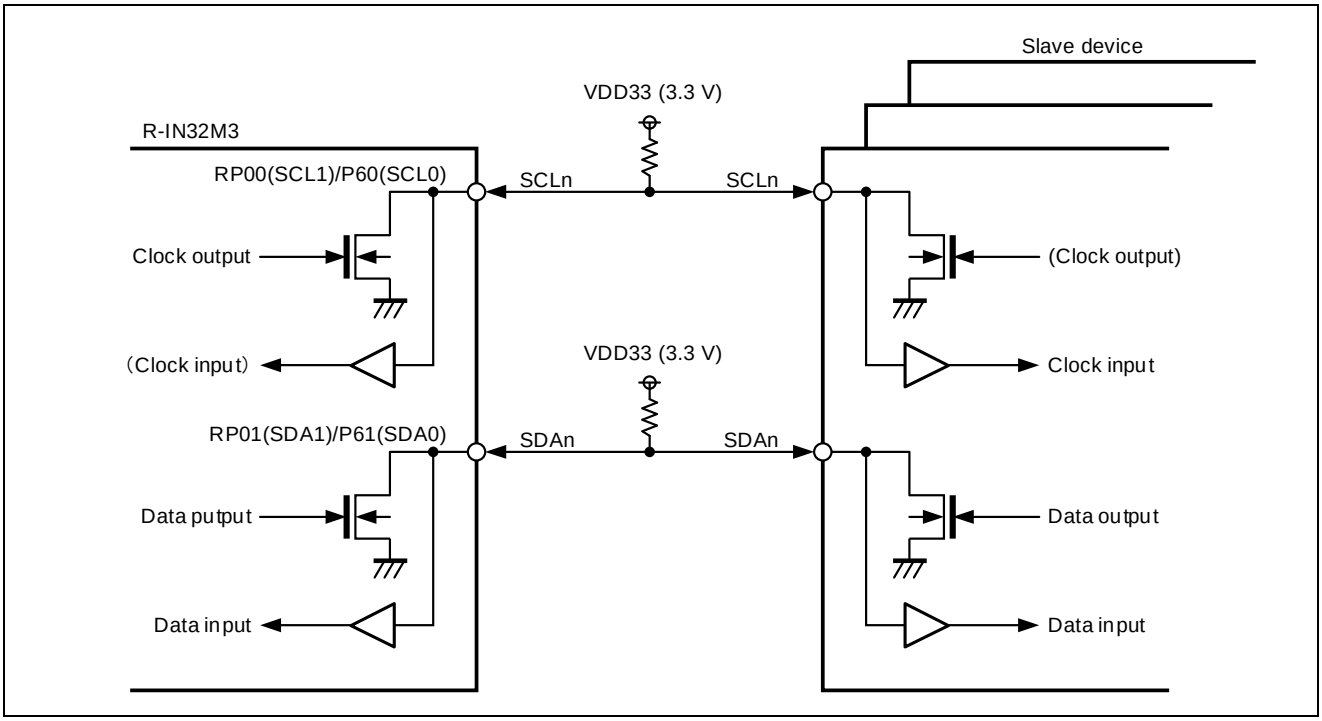


Figure 14.1 Connection Example between R-IN32M3 and I^2C Slave Device

15. EtherCAT EEPROM I^2C Connection Pins (R-IN32M3-EC Only)

In the case of using the EtherCAT® protocol, the user needs to connect to the external EEPROM with the dedicated EEPROM I^2C connection pins.

The EEPROM I^2C connection pins are following two pins.

- CATI2CCLK pin (shared with the P22 function): EtherCAT EEPROM I^2C clock output
- CATI2CDATA pin (shared with the P23 function): EtherCAT EEPROM I^2C data

Figure 15.1 shows a connection example between the R-IN32M3-EC and the EEPROM.

Since the serial clock line and serial data line are N-ch. open drain outputs, external pull-up resistors are required.

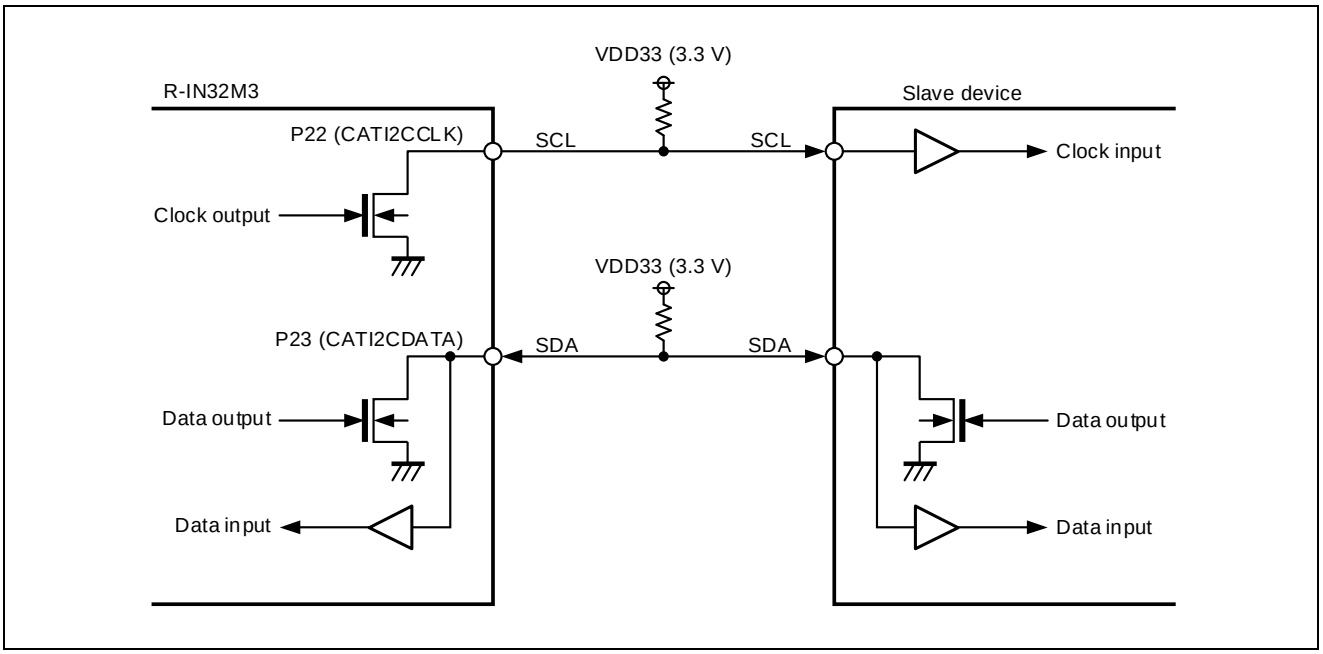


Figure 15.1 Connection Example between R-IN32M3-EC and EtherCAT EEPROM

16. CAN Pins

Figure 16.1 shows a connection example between the R-IN32M3 and the CAN transceiver.

The CAN transceiver is used to connect the CAN bus.

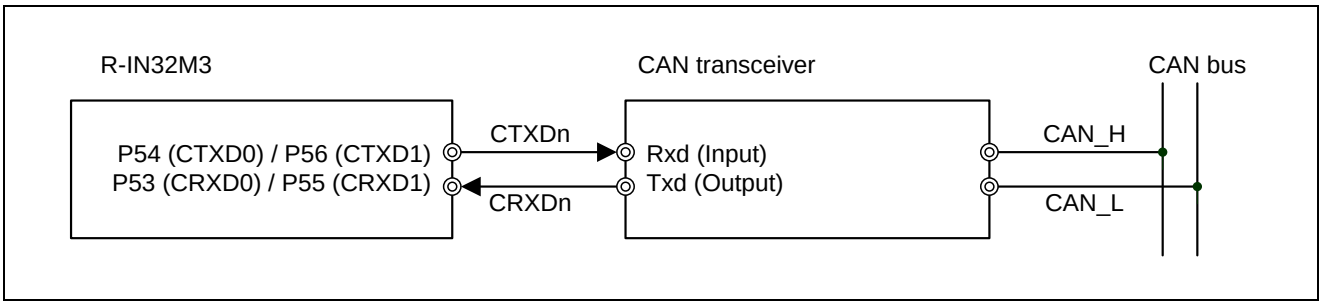


Figure 16.1 Connection Example between R-IN32M3 and CAN Transceiver

Remark. n = 0 or 1

17. CSIH Pins <R>

Examples of connections of an R-IN32M3 with a CSI master and slave are given below.

17.1 One Master and One Slave

The following figure illustrates the connections between one master and one slave.

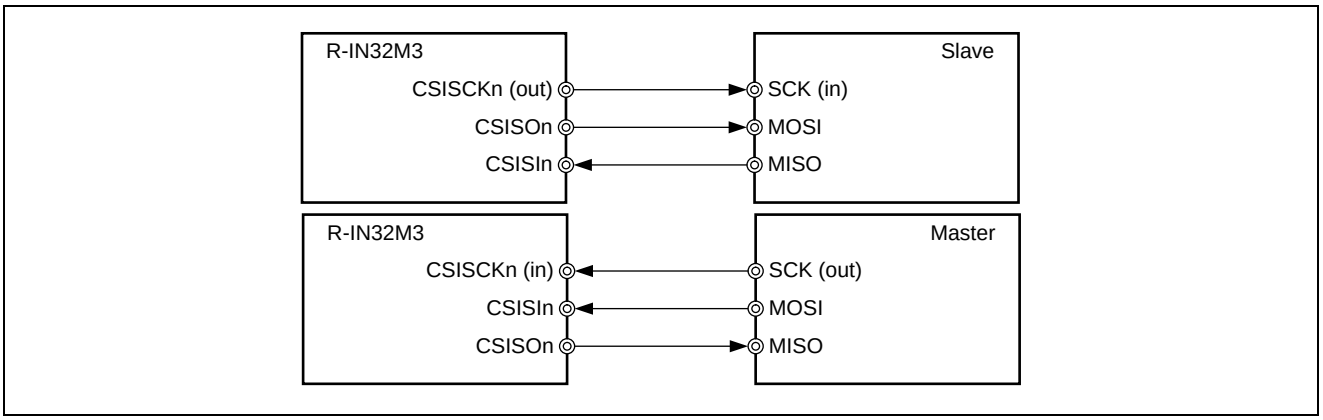


Figure 17.1 Direct Master/Slave Connection

Remark: n = 0, 1

17.2 One Master and Two Slaves

The following figure illustrates the connections between an R-IN32M3 as a master and two slaves. In this example, an R-IN32M3 supplies one chip select (CS) signal to each of the slaves. This signal is connected to the slave select input (SSI) of the slave.

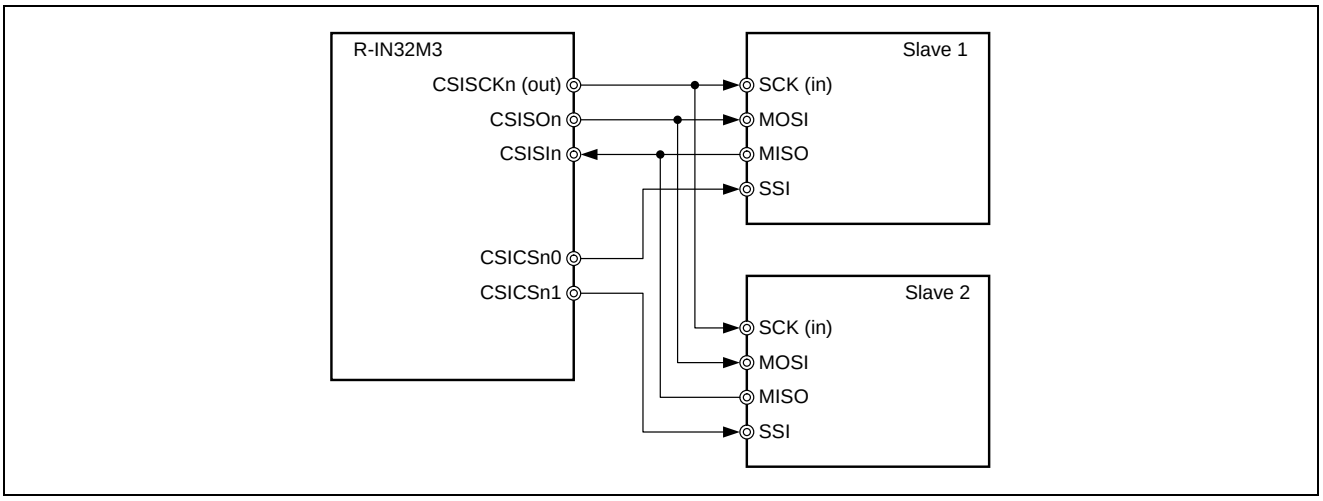


Figure 17.2 Connection between One Master and Two Slaves

Remark: n = 0, 1

18. JTAG/Trace Pins

The following figures show examples when this LSI chip is connected to the ICE (in-circuit emulator).

They are examples when connected to the 20-pin half-pitch connecter or 20-pin full-pitch connecter of standard.

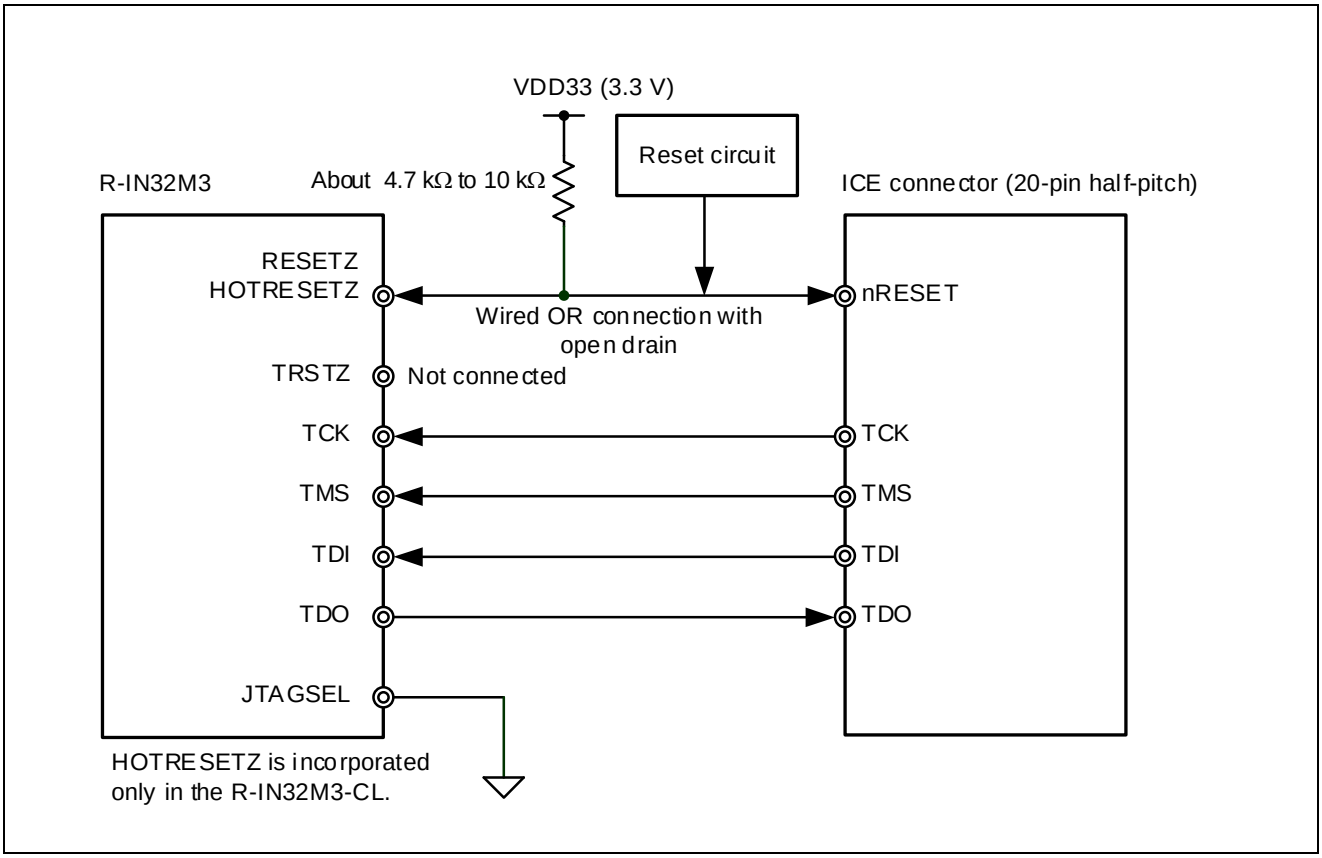


Figure 18.1 Connection Example of JTAG Interface (20-Pin Half-Pitch without Trace)

As long as nRESET is input to RESETZ, nRESET is not required to input to HOTRESETZ.

RESETZ resets the entire LSI, but the internal PLL is not reset in the case of only HOTRESETZ. Please use it to meet your needs.

In addition, nRESET should not be connected to PONRZ.

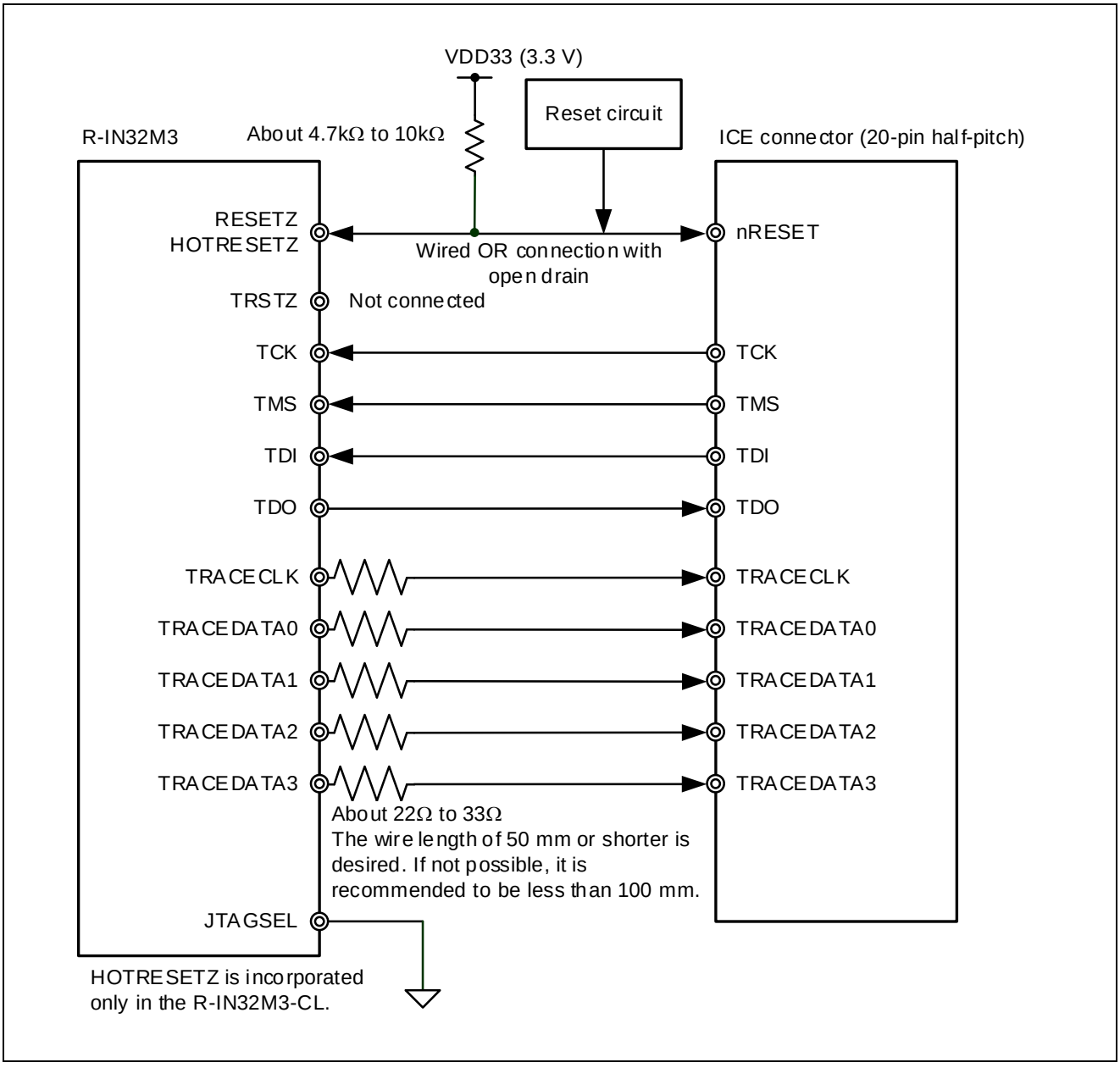


Figure 18.2 Connection Example of JTAG Interface (20-Pin Half-Pitch with Trace)

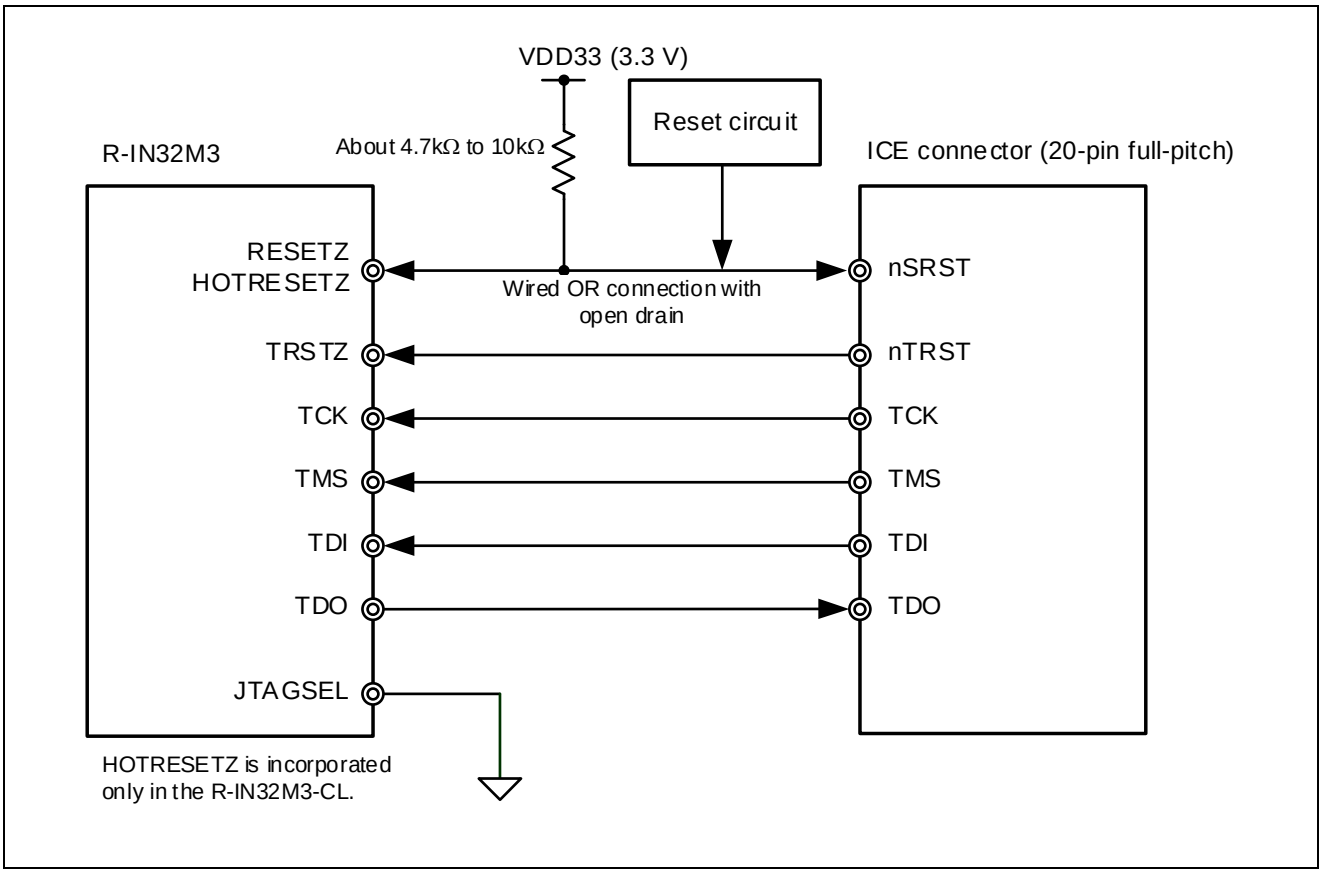


Figure 18.3 Connection Example of JTAG Interface (20-Pin Full-Pitch)

19. Implementation Conditions

Figure 19.1 and Figure 19.2 show implementation conditions of the R-IN32M3.

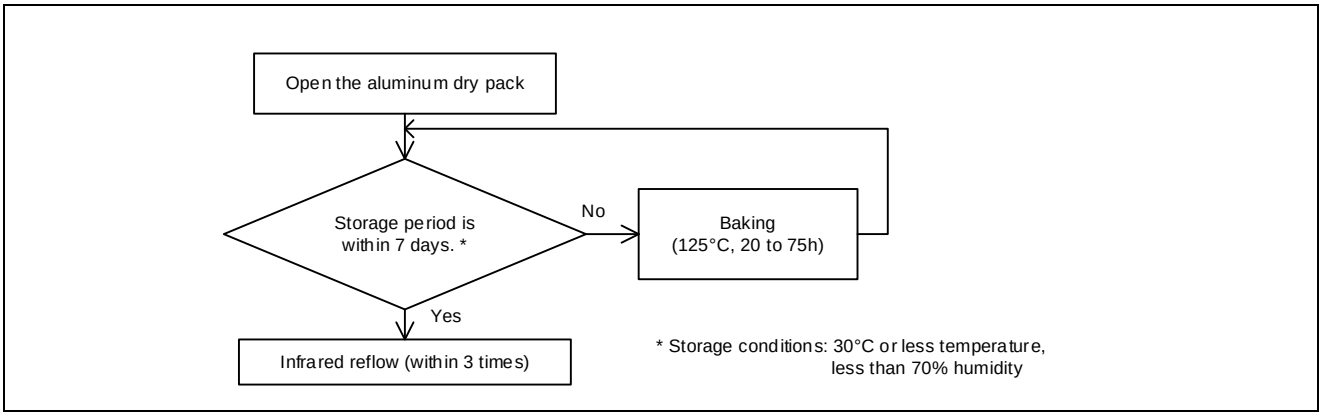


Figure 19.1 Implementation Flow

- Maximum temperature (package surface temperature) : 260°C or below
- Time of maximum temperature : 10 s or less
- Time which temperature is 220°C or more : 60 s or less
- Time of preheat temperature (160 to 180°C) : 60 to 120 s
- Number of maximum reflow times : 3 times
- Chloric content of the rosin flux (the weight percentage) : 0.2% or less
- Safe-keeping restriction period after opening the dry pack : Within 7 days

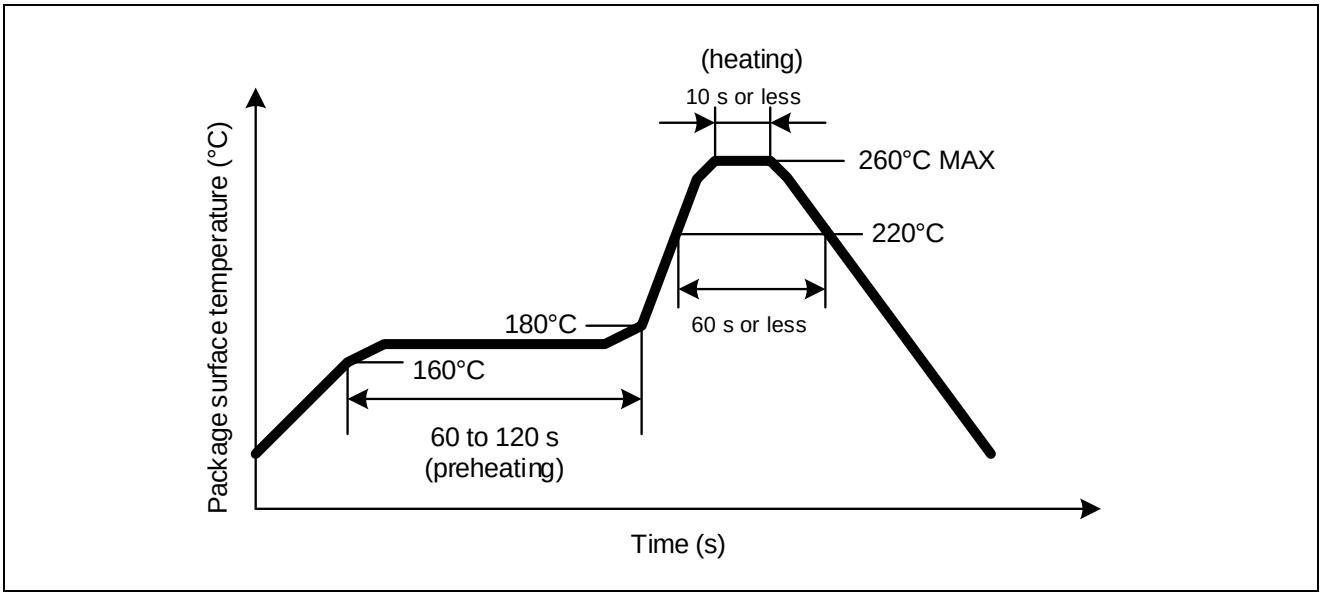
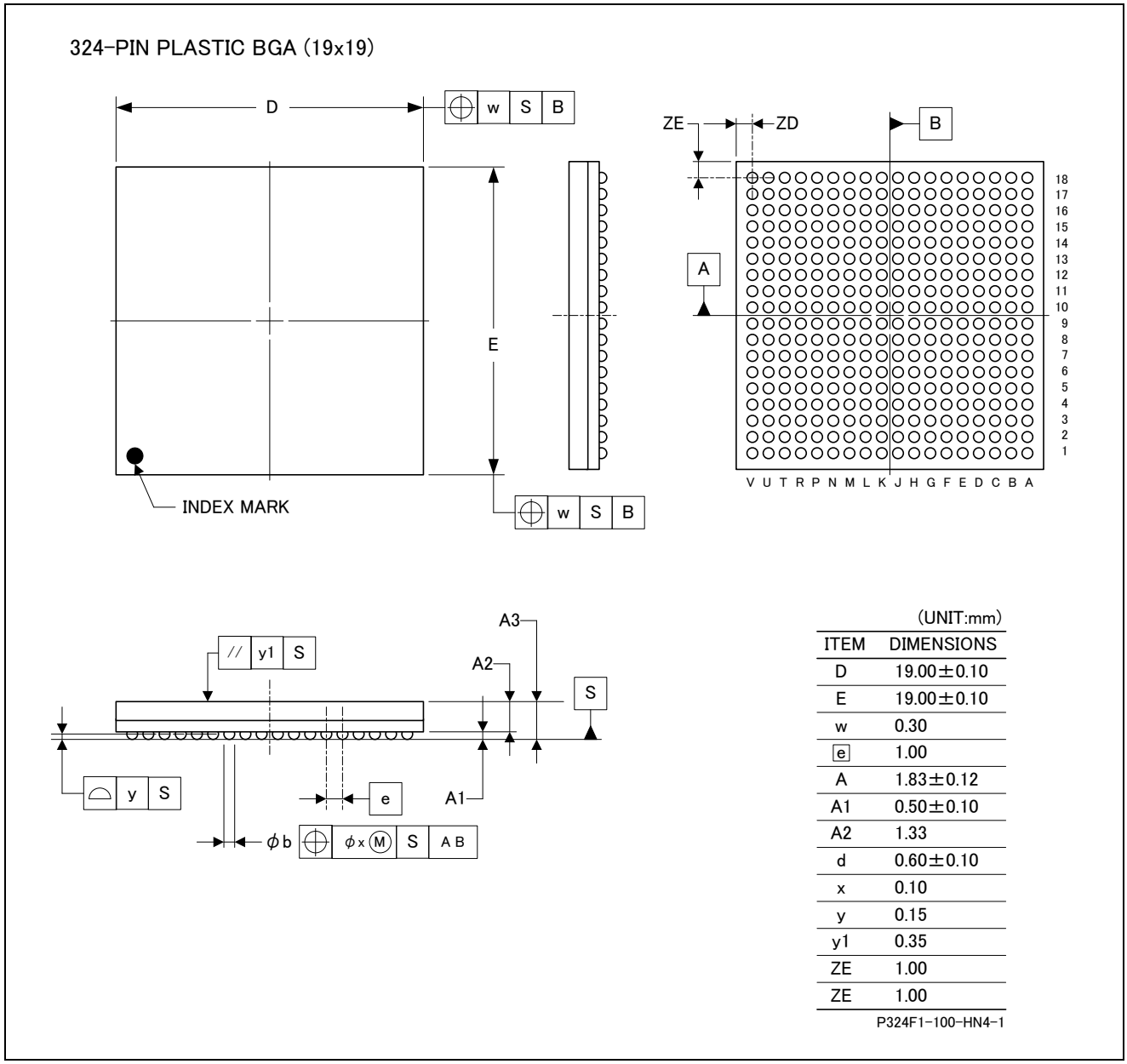


Figure 19.2 Infrared Reflow Temperature Profile

20. Package Information

Figure 20.1 shows the package information.



(UNIT:mm)

ITEM	DIMENSIONS
D	19.00±0.10
E	19.00±0.10
w	0.30
e	1.00
A	1.83±0.12
A1	0.50±0.10
A2	1.33
d	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZE	1.00
ZE	1.00

P324F1-100-HN4-1

Figure 20.1 Package Information

21. Mount Pad Information

Figure 21.1 shows the mount pad information.

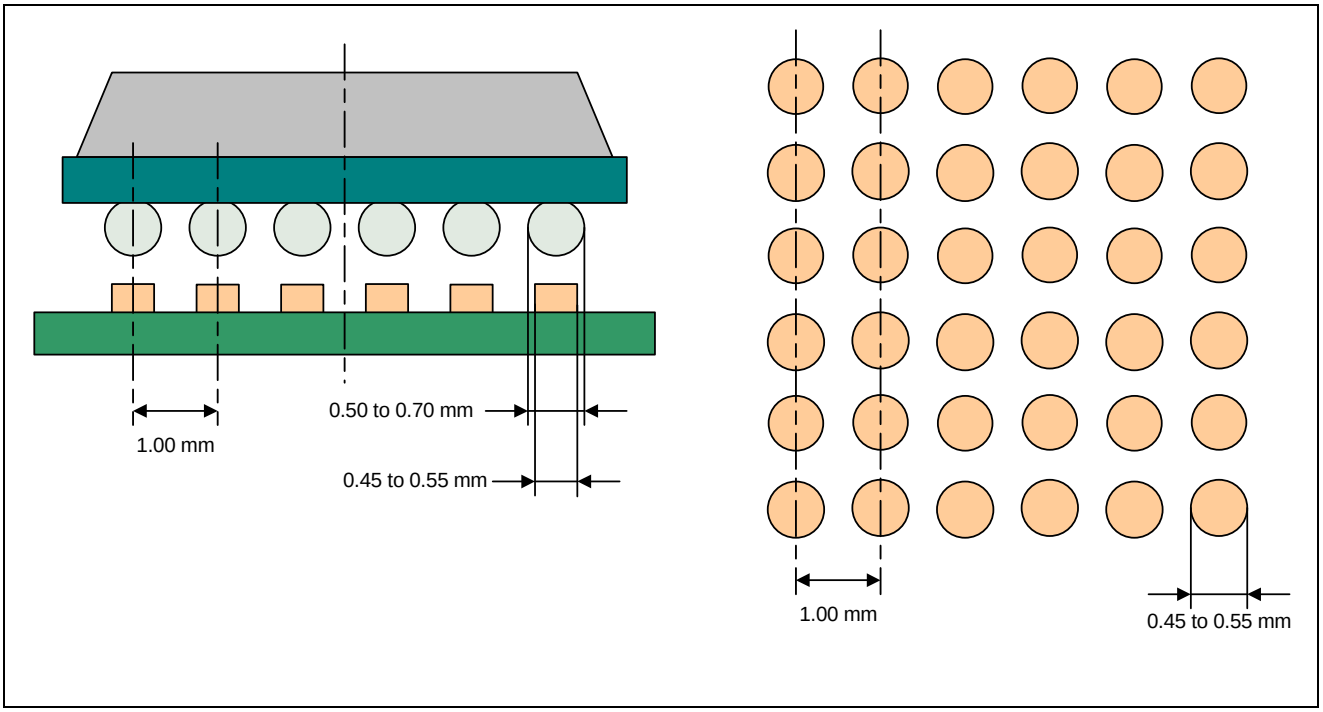


Figure 21.1 Mount Pad Sizes

22. BSCAN Information

R-IN32M3 provides the BSDL file.

Caution. If the other device is connected to an input pin without the pin being pulled up or down, clamp the level on the board or set the logic in the other device.
Placing the 3rd pin in the Hi-Z state creates a possibility of a floating current flowing.

22.1 BSCAN Operating Conditions

Fix the level of the pins as follows.

- JTAGSEL: Fix to the high level
- TMODE0: Fix to the low level
- TMODE1: Fix to the low level
- TMODE2: Fix to the low level

22.2 Maximum Operating Frequency of TCK

The maximum operating frequency of TCK is 10 MHz.

22.3 IDCODE

IDCODE is as follows.

(1) R-IN32M3-CL

IDCODE 0x081A3447	
<breakdown>	
Version	0000
Part number	1000000110100011
Manufacturer number: Renesas Electronics	01000100011
Fixed code	1

(2) R-IN32M3-EC

IDCODE 0x081A4447	
<breakdown>	
Version	0000
Part number	1000000110100100
Manufacturer number: Renesas Electronics	01000100011
Fixed code	1

22.4 BSCAN Non-Supported Pins

The following pins do not support BSCAN.

Table 22.1 List of BSCAN Non-Supported Pins<R>

R-IN32M3-CL	R-IN32M3-EC
XT1	XT1
XT2	XT2
PONRZ	PONRZ
JTAGSEL	JTAGSEL
TMODE0	TMODE0
TMODE1	TMODE1
TMODE2	TMODE2
TMS	TMS
TDI	TDI
TDO	TDO
TRSTZ	TRSTZ
TCK	TCK
TMC1	TMC1
TMC2	TMC2
	P0_RX_P
	P0_RX_N
	P1_RX_P
	P1_RX_N
	P0_TX_P
	P0_TX_N
	P1_TX_P
	P1_TX_N
	TEST1
	TEST2
	TEST3
	ATP
	LX
	EXTRES
	FB
	P0_SD_N
	P1_SD_N

22.5 How to Get BSDL

With regard to obtain the BSDL file, please contact a Renesas Sales Representative or Distributor in your area.

22.6 Notes on Using BSDL <R>

When the BSDL file is used, the control cell that is not used on the BSDL may cause the following errors. When the error occurs, treat it as a pseudo error.

Error log <Partially excerpted>:

Error, Line 1112, Control cell 236 does not enable any driver.
Error, Line 1112, Control cell 238 does not enable any driver.
Error, Line 1112, Control cell 240 does not enable any driver.
Error, Line 1112, Control cell 242 does not enable any driver.
Error, Line 1112, Control cell 244 does not enable any driver.
Error, Line 1112, Control cell 246 does not enable any driver.

23. IBIS Information

Please obtain the IBIS information from the following website.

https://www.renesas.com/en-us/products/factory-automation/multi-protocol-communication.html

24. Marking Information

24.1 R-IN32M3-EC

Product name: MC-10287BF1-HN4-A, MC-10287BF1-HN4-M1-A

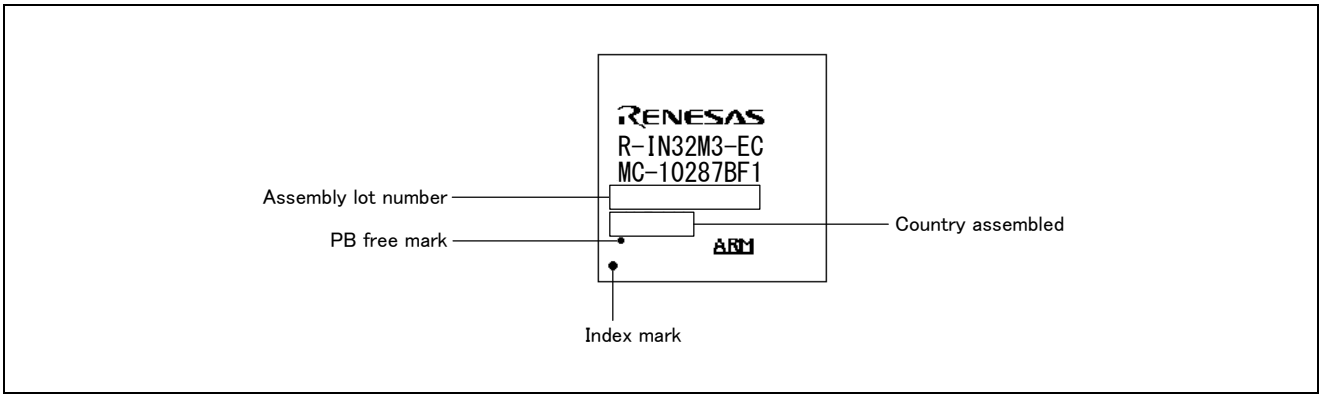


Figure 24.1 R-IN32M3-EC Marking Information

24.2 R-IN32M3-CL

Product name: UPD60510BF1-HN4-A, UPD60510BF1-HN4-M1-A

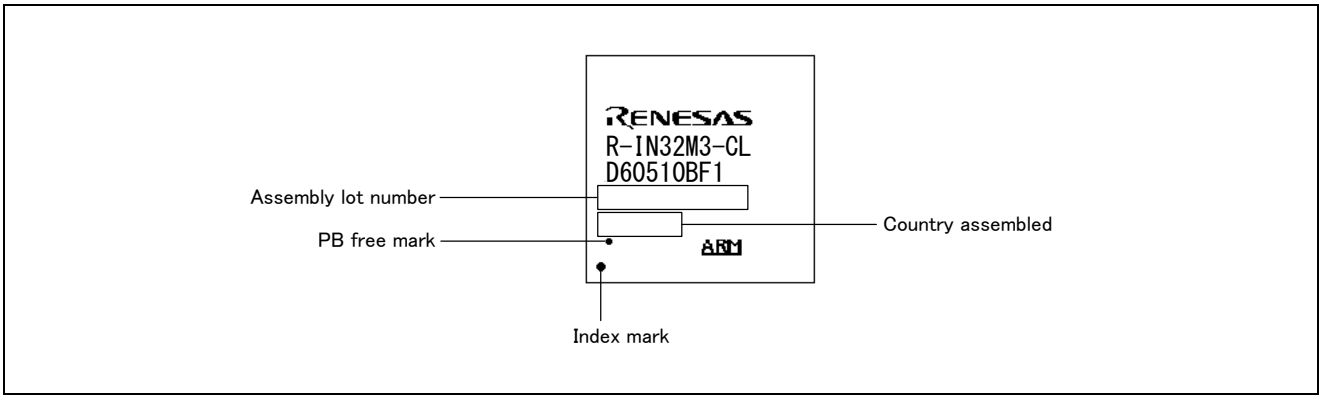


Figure 24.2 R-IN32M3-CL Marking Information

25. Thermal Design <R>

This section describes the thermal characteristics of the R-IN32M3, and includes notes that require attention in the design of the board on which the device is mounted in terms of the dissipation of heat and the prevention of abnormal heating.
Since the R-IN32M3-EC incorporates an Ethernet PHY module, large-capacity memory, and a regulator, it requires greater consideration of heat than most devices.
Design the board and casing in consideration of heat dissipation.

25.1 Deciding on whether Particular Measures for Heat Dissipation are Required

25.1.1 Estimating Tj

Take Tj ≤ 110°C as the criterion for Tj of the R-IN32M3. Estimate Tj from the following formulae.

Tj = Tt + Ψjt x power or Tj = Ta + θja x power

Tj	: Junction temperature [°C]
Tt	: Package surface temperature [°C]
Ta	: Ambient temperature [°C]
θja	: Thermal resistance [°C/W] between the junction (at temperature Tj) and the ambient environment (at Ta) (See section 25.1.3, Thermal Resistances under the JEDEC Conditions (for θja and Ψjt).)
Ψjt	: Thermal resistance [°C/W] between the junction (at temperature Tj) and the surface of the package (at Tt) (See section 25.1.3, Thermal Resistances under the JEDEC Conditions (for θja and Ψjt).)
Power	: Power consumption [W] (1.0-V sub-systems + 3.3-V sub-systems; that for the 1.5-V sub-systems must also be added when the internal regulator is not in use)

If Tj ≤ 110°C is satisfied, the semiconductor device does not require further measures for heat dissipation.
However, if the semiconductor device is to be installed in ways that have varying criteria for determining increases in temperature, prepare measures for heat dissipation as required.
If Tj ≤ 110°C is not satisfied, heat dissipation solutions are necessary.

25.1.2 Estimating Power Consumption

For the 3.3-V sub-systems, estimate the power consumption from the value for current on the R-IN32M3 Series Data Sheet.
Since it is temperature dependent, the power consumption of the 1.0-V sub-systems is estimated from the following formula according to the operating temperature.

$$\text{Power (1.0-V sub-systems)} = 140 + 103 \times e^{(0.0179 \times Tj)} \text{ [mW]}$$

The list in 25.1.4, Results of Estimating Power Consumption of the 1-V Sub-Systems at Tj, gives results of estimation under specific conditions.

25.1.3 Thermal Resistances under the JEDEC Conditions (for θja and Ψjt)

The thermal resistances under the JEDEC-2S2P conditions are as follows.
However, these values are for the devices alone; care is required since the actual thermal resistances will depend on the board, casing, and peripheral components.

	θja [°C/W]	Ψjt [°C/W]
R-IN32M3-EC	16.3	0.10
R-IN32M3-CL	14.9	0.12

25.1.4 Results of Estimating Power Consumption of the 1-V Sub-Systems at Tj

The results of calculating power consumption by the 1-V sub-systems vary with the effects of θja and Ta on Tj.

(1) R-IN32M3-EC

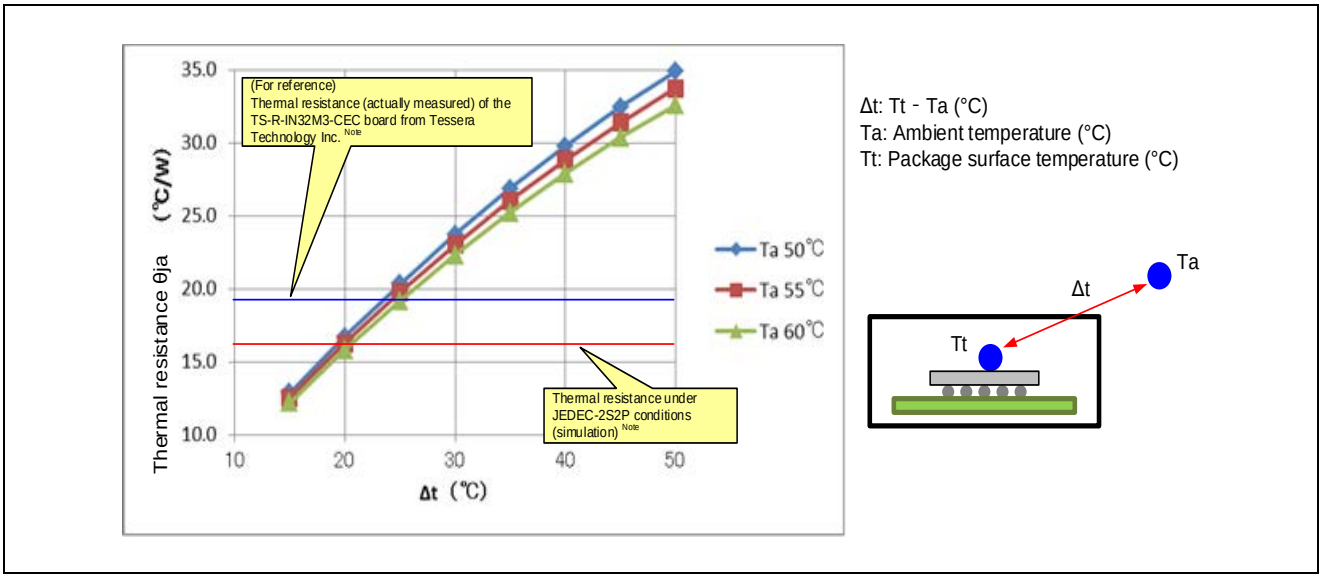
θja [°C/W] / Ta [°C]	Tj [°C]				Power Consumption by 1-V Sub-Systems [mW]			
	16.3 (JEDEC)	20	25	30	16.3 (JEDEC)	20	25	30
-40	-25.9	-22.6	-18.1	-13.6	205	209	214	221
-35	-20.8	-17.5	-13.0	-8.3	211	215	222	229
-30	-15.7	-12.3	-7.8	-3.1	218	223	230	238
-25	-10.6	-7.2	-2.5	2.2	225	231	238	247
-20	-5.4	-2.0	2.7	7.5	233	239	248	258
-15	-0.3	3.2	8.0	12.9	243	249	259	270
-10	4.9	8.4	13.3	18.3	252	260	271	283
-5	10.1	13.6	18.6	23.7	263	272	284	298
0	15.3	18.9	24.0	29.2	275	284	298	314
5	20.5	24.2	29.4	34.8	289	299	314	332
10	25.7	29.5	34.8	40.4	303	315	332	352
15	31.0	34.8	40.3	46.0	319	332	352	375
20	36.3	40.2	45.9	51.8	337	352	374	400
25	41.6	45.7	51.5	57.7	357	373	399	429
30	46.9	51.1	57.2	63.7	379	397	427	462
35	52.3	56.7	62.9	69.8	403	424	458	499
40	57.8	62.3	68.8	76.1	430	454	493	542
45	63.2	67.9	74.8	82.5	460	488	533	591
50	68.8	73.7	81.0	89.3	493	525	579	649
55	74.4	79.6	87.3	96.3	530	568	631	718
60	80.1	85.5	93.8	103.8	572	616	692	801
65	85.8	91.6	100.6	N/A	619	671	763	N/A
70	91.7	97.9	107.7	N/A	672	734	848	N/A
75	97.7	104.3	N/A	N/A	732	807	N/A	N/A
80	103.8	N/A	N/A	N/A	800	N/A	N/A	N/A
85	110.0	N/A	N/A	N/A	879	N/A	N/A	N/A

(2) R-IN32M3-CL

θja [°C/W] / Ta [°C]	Tj [°C]				Power Consumption by 1-V Sub-Systems [mW]			
	14.9 (JEDEC)	20	25	30	14.9 (JEDEC)	20	25	30
-40	-34.6	-32.8	-30.9	-29.0	195	197	199	201
-35	-29.6	-27.6	-25.8	-23.8	201	203	205	207
-30	-24.5	-22.5	-20.6	-18.6	207	209	211	214
-25	-19.4	-17.4	-15.4	-13.4	213	215	218	221
-20	-14.3	-12.2	-10.2	-8.2	220	223	226	229
-15	-9.1	-7.1	-5.0	-2.9	227	231	234	238
-10	-4.0	-1.9	0.2	2.4	236	240	243	248
-5	1.1	3.3	5.5	7.7	245	249	254	258
0	6.3	8.5	10.8	13.1	255	260	265	270
5	11.4	13.7	16.1	18.5	266	272	277	283
10	16.6	19.0	21.4	23.9	279	285	291	298
15	21.8	24.3	26.8	29.4	292	299	306	314
20	27.0	29.6	32.2	34.9	307	315	323	332
25	32.3	35.0	37.7	40.5	324	333	342	353
30	37.6	40.3	43.2	46.2	342	352	363	376
35	42.9	45.8	48.8	52.0	362	374	387	401
40	48.2	51.3	54.4	57.8	384	398	413	430
45	53.5	56.8	60.2	63.8	409	425	443	463
50	58.9	62.4	66.0	70.0	436	455	476	500
55	64.4	68.1	72.0	76.3	466	488	514	543
60	69.9	73.8	78.0	82.7	500	526	556	593
65	75.5	79.7	84.3	89.5	538	569	605	651
70	81.1	85.6	90.7	96.6	580	617	662	720
75	86.8	91.7	97.3	104.1	627	672	728	803
80	92.6	98.0	104.3	N/A	680	735	806	N/A
85	98.5	104.5	N/A	N/A	741	808	N/A	N/A

25.1.5 Relation between Temperature Increases (Δt) and Thermal Resistance (θja) at a Given Ambient Temperature

The thermal resistance (θja) depends on the board, casing, and peripheral components. If respective criteria for the temperature rise (Δt = Tt - Ta) apply to the end product, refer to the graph below that shows the required θja to reach the target Δt. Take these values into consideration in the thermal design of the board.
As an example, the graph also shows the thermal resistance (actually measured) of the TS-R-IN32M3-CEC board from Tessera Technology Inc. Measures for heat release as described in 25.2.1, Measures for Heat Release in Designing the Board, have been applied for this board.



Note. The value for the board manufactured by Tessera Technology Inc. and the result of simulation under JEDEC-2S2P conditions were obtained without a casing.

25.2 Examples of Measures for Heat Dissipation

We classify measures for heat dissipation into two types. For details, see the following pages.

(1) Measures for heat release in designing the board
- Take these types of measures into consideration when designing the board.
- The following measures are highly effective, so implement them as a matter of course.

(I) Thermal vias
(II) VDD/GND pattern
(III) Increase the number of board layers, and bring the GND pattern out to the surface layer.
(IV) Consider other factors of placement that will affect heat flows and take the appropriate action[Note]

(2) Heat dissipation from the periphery (including the casing)
- If the measures listed in (1) above still don't achieve your criterion for Δt or satisfy the condition Tj = 110°C or below, further measures for heat dissipation in the form of heat sinks or heat dissipating gels should be applied, including for the casing as a whole if this is required.

Note. Take special care in placement in terms of the regulator, since this operates at particularly high temperatures.

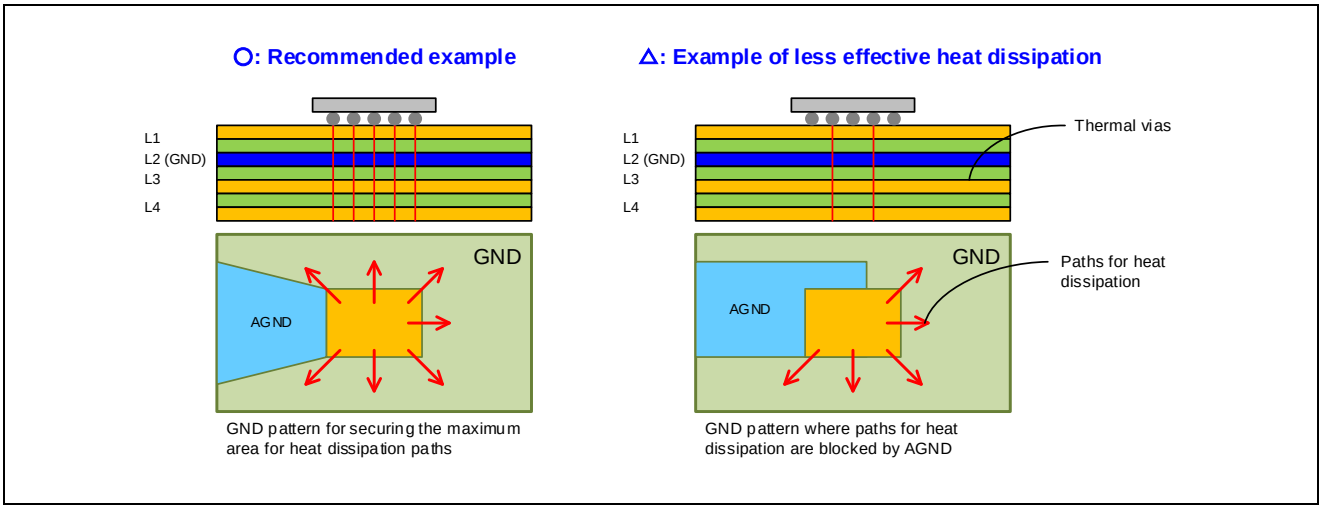
25.2.1 Measures for Heat Release in Designing the Board

(1) Thermal Vias

Placing as many vias to the power supply and GND areas as possible below the center of the package increases the number of paths for the flow of heat in the z direction. We recommend placing one via for each power supply and GND ball.

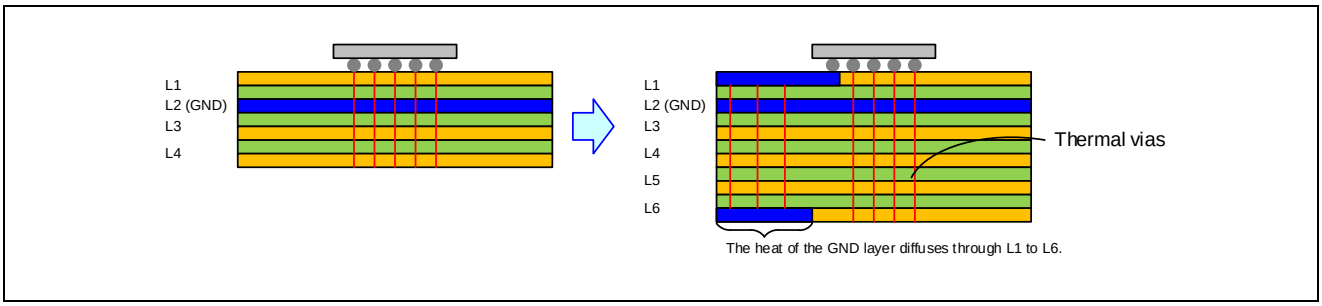
(2) Power Supply and GND Planes

Secure as large an area as is possible for the power supply and GND planes of the board. This enables the broad diffusion of heat through vias in the direction of the surface plane. Dividing paths for heat dissipation from plane to plane decreases the effectiveness of heat dissipation. Therefore, place the GND pattern in such a way that the paths are divided as little as is possible. We recommend L2 for the GND layer.



(3) Increase the Number of Board Layers, and Bring the GND Pattern out to the Surface Layer

Increasing the number of Cu wiring layers in the printed circuit board expands the area for hear release. Where possible, place areas of the GND pattern on the surface layer and connect them to the main GND pattern via thermal vias. This further improves heat dissipation. The board should have at least four layers, and we recommend six.



(4) Consider Other Factors of Placement that will Affect Heat Flows and Take the Appropriate Action

Placing heat-generating components close to this device affects its heat efficiency, so do not place heat-generating components in its vicinity.

Caution. For example, placing a regulator with high power consumption in the vicinity of this device has the effect of significantly reducing its heat dissipation.

(5) Residual Copper Ratio of Cu Layers

Increasing the residual copper ratio in all layers of the board layers increases the breadth of the paths for heat transfer.

(6) Cu Thickness

Designing all Cu layers of the board to be thick increases the volume of paths for heat dissipation. Since thinner Cu layers reduce the effectiveness of heat dissipation, care is required on this point. We recommend that the power supply and GND layers be at least 35-um thick.

25.2.2 Heat Dissipation from the Periphery (Including the Casing)

(1) Incorporating a Heat Sink

Incorporating a heat sink increases the area for heat dissipation, making heat dissipation from the surface of the device more efficient.

(2) Heat Conduction to the Casing

Placing heat dissipating gel on the surface of the device and connecting this to the metal surface of the casing increases the efficiency of heat dissipation from the surface of the device.

(3) Placing a Fan in the Casing

Including a fan improves thermal conductivity through convection, which decreases the ambient temperature.

(4) Obtaining a Chimney Effect

Since heat tends to be released in the z direction, placing the board vertically leads to heat convection from the surface of the device, improving the thermal conductivity rate there.

(5) Enlarging Ventilation Holes

Larger ventilation holes accelerate the heat exchange between the air within the casing and that outside, lowering the temperature in the vicinity of the device.

(6) Thermal Insulation by Shielding Plates

If there is a particular source of much heat within the casing, thermal insulation by using shielding plates is effective. Shielding the device from the effects of such heat sources reduces the effect of the heat on the device.

25.3 Points for Caution

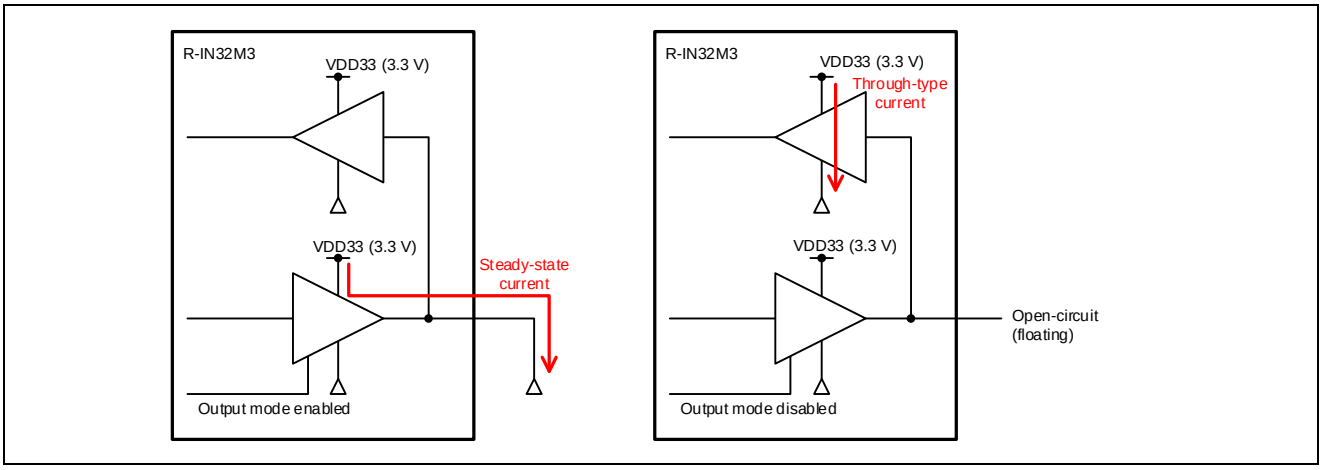
This section describes points of incorrect design that may lead to abnormal heating.

25.3.1 Internal Regulator

The 1.5V regulator incorporated in the R-IN32M3-EC requires an external smoothing circuit. This smoothing circuit not operating stably (e.g. oscillating around 1.5 V) reduces the efficiency of the regulator and may lead to the supply of a current above the rated value. Inappropriate equivalent series resistances (ESRs) for capacitors are the most likely source of such problems. Thus, when using components other than those recommended, use a capacitor with an ESR in the range from about 75 mΩ to 300 mΩ and check that the output voltage is stable. When using tantalum capacitors is not possible, a ceramic capacitor and a combination of a 100-mΩ resistor and ceramic capacitor can be used for C2 and C1, respectively.

25.3.2 Handling of Unused Pins

If an unused pin is clamped to the GND or power supply on the board, the corresponding pin must have the input attribute as a fixed setting. If it is set as an output, and the level of the point where it is clamped is opposite that of the pin, a large steady-state current will continuously flow through the output buffer.
On the other hand, if an unused pin is open-circuit on the board, the corresponding pin can have either a fixed output attribute or an input attribute with enabling of pull-up or pull-down resistors. Setting a pin as an input without enabling a pull-up or pull-down resistor may lead to the pin being in a floating state and the flow of a through-type current.
Since the above factors lead to unnecessary heating, be sure to check the settings made by the software.



26. Countermeasure for Noise <R>

This section describes a countermeasure for noise in circuits that include an R-IN32M3.

26.1 Stopping Clock Output

If the BUSCLK pin is not in use, output on the pin from an R-IN32M3 can be stopped. See section 2.2.2, Clock Control Registers (CLKGTD0, CLKGTD1) in the *R-IN32M3 Series User's Manual: Peripheral Modules* regarding control of the GCBCLK bit in the CLKGTD0 register, which enables or disables output from the BUSCLK pin.

REVISION HISTORY R-IN32M3 Series User's Manual (Board design edition)

Rev.	Date	Description	
		Page	Summary
1.00	Jul 26, 2013	-	First edition issued
1.01	Dec 02, 2013	10,12	Add the TEST pin processing
		22	Add " 9. Notes of CC-Link IE FIeld user (only R-IN32M3-CL)"
2.00	Dec 26, 2013	11	Add a description of 6.GPIO port pins
		20	Add a description of 8.GMII pins
		23	Modify a description of 10. Notes of CC-Link IE Field use
		24	Add a description of "11. External MPU/memory interface pins"
		33	Add a description of "12. Serial Flash ROM memory connection pins"
		34	Add a description of "13. Asynchronous Serial Interface J(UARTJ) connection pins"
		35	Add a description of "14. I^2C connection pins"
		36	Add a description of "15. EtherCAT EEPROM I^2C connection pins"
		37	Add a description of "17. CAN pins"
		38	Add a description of "17.JTAG/trace pins"
2.01	Feb 07, 2014	24	Modify the mode description of the case of MEMCSEL=High and HIFSYNC=Low.
		25,26	Delete HBCYSTZ pin connection of "Fig 11.1" and "Fig 11.2" Modifiy the width of data bus of "Fig 11.2" Add the description of Note4-6 of "Fig 11.1" and "Fig 11.2"
		27,28	Delete HBCYSTZ pin connection of "Fig 11.3" and "Fig 11.4" Modifiy the width of data bus of "Fig 11.4" Modifiy the width of address bus of "Fig 11.4" Add the description of Note4-6 of "Fig 11.3", "Fig 11.4"
		29, 30	Separete and add the description about "synchronous SRAM type transmission mode"
2.02	May 30, 2014	2	Add a notes of "2.1 Power-on-off sequence"
		1-9	Modify Eglish expression about capter 1-4
2.03	Sep 30, 2014	11	Modify part name of inductor VLC5028T to VLCF5028T in "5.1Built-in regulator used" Modify ESR value of condenser 300 ohm to 300 mohm in "5.1Built-in regulator used"
		25-29	Fig.11.1-11.6 Modify signal name BUSCLK to HBUSCLK
		40	Add a description in "17.JTAG/trace pins"
2.04	Dec 25, 2014	22, 23	Add Fig. 9.1 in ***9.CC-Link pins***
		29, 30	Modify Fig.11.5, 11.6 to add HBCYSTZ connection, modify Adress bus number, and delete HHPGCSZ connection. And modify Note2, 4, 5 description in ***11.1.3 Synchronous SRAM type transmission mode***
3.00	Feb. 28, 2017	1	"1.1 Definition of Pin Handling and Symbols in This Manual" was newly added.
		7	3.3 Oscillation Circuit Configuration Example Pin handling and the GND description in Figure 3.2 were modified. Caution on a resonator was modified.
		8	4.1 Recommended Configuration of Filter Pin handling and the GND description in Figure 4.1 were modified.

Rev.	Date	Description	
		Page	Summary
3.00	Feb. 28, 2017	10	5.1 Built-in Regulator Used Pin handling and the GND description in Figure 5.1 were modified. The description on the capacitor substitution method was added.
		11	5.1 Built-in Regulator Used Table 5.1 was added to complement the list of the recommended parts.
		12	5.2 Built-in Regulator Unused Pin handling and the GND description in Figure 5.3 were modified.
		13	6. GPIO Port Pins The reference in separate user's manuals, modified
		14	7. Ethernet PHY Pins (R-IN32M3-EC Only) The description that this section was for the R-IN32M3-EC only was added to the section title.
			7.1 Ethernet PHY Power Supply Pins Pin names of Rx/Tx analog power supply pins and the description of power supply pins were modified.
		15	7.2 100Base-TX Pins Pin handling and the GND description in Figure 7.2 were modified. Remark and Notes were moved to outside of the figure frame.
		16	7.2 100Base-TX Pins Pin handling and the GND description in Figure 7.3 were modified. Remark and Notes were moved to outside of the figure frame.
			7.2 100Base-TX Pins Note was added to R1 to R6 in Table 7.1.
		19	7.3 100Base-FX Pins (Optical Fiber) Pin handling and the GND description in Figure 7.7 were modified. Remark was moved to outside of the figure frame.
		20	8. GMII Pins (R-IN32M3-CL Only) Pin handling in Figure 8.1 was modified. Remark was moved to outside of the figure frame.
		21	8.2 Circuit Design around GMII The description of the number for Ethernet ports was modified.
		23	9. CC-Link Pins Pin handling and the GND description in Figure 9.1 were modified. The name for CC-Link clock pins was modified. Note 3 was added.
		25	11. External MCU/Memory Interface Pins As the mode setting pin, the ADMUXMODE pin was added. Note when accessing the CC-Link IE field wad added.
		27	11.1.1 Asynchronous SRAM Interface Mode The description of pin handling in Figure 11.1 and Figure 11.2 was modified. The position for the HBUSCLK pin and Note was modified.
		29	11.1.2 Synchronous SRAM Interface Mode The position for the HBUSCLK pin in Figure 11.3 and Figure 11.4 was modified.
		30	11.1.3 Synchronous SRAM-Type Transfer Mode The description of pin handling in Figure 11.5 and Figure 11.6 was modified. The position for the HBUSCLK pin and Note was modified.

Rev.	Date	Description	
		Page	Summary
3.00	Feb. 28, 2017	31	11.2 External Memory Interface As it was not needed, the description on the MEMIFSEL pin was deleted.
		32	11.2.1.1 Connection Example with SRAM Remarks in Figure 11.7 and Figure 11.8 were moved to outside of the figure frame.
		35	11.2.2.1 Connection Example with SRAM Remarks in Figure 11.11 and Figure 11.12 were moved to outside of the figure frame. The description of Note was modified.
		36	11.2.2.2 Connection Example with Paged ROM The description of Note in Figure 11.13 and Figure 11.14 was modified.
		37	12. Serial Flash ROM Connection Pins The name of port pin was added to the pin name in Figure 12.1.
		38	13. Asynchronous Serial Interface J Connection Pins The section title was modified. The name of port pin was modified in Figure 13.1.
		39	14. I^2C Connection Pins Pin handling in Figure 14.1 was modified. The name of I^2C pin was added to the port pin.
		40	15. EtherCAT EEPROM I^2C Connection Pins (R-IN32M3-EC Only) The description of pin handling in Figure 15.1 was modified. The name of the multiplexing port was added to the EtherCAT pin.
		41	16. CAN Pins The name of port pin was modified in Figure 16.1. The name of the CAN pin was added. Remark was moved to outside of the figure frame.
		42	17. JTAG/Trace Pins The connection of the ICE connector to the nRESET pin in Figure 17.1 was modified. Pin handling and the GND description were modified.
		43	17. JTAG/Trace Pins The connection of the ICE connector to the nRESET pin in Figure 17.2 was modified. The description on the wiring limitation was modified. Pin handling and the GND description were modified.
		44	17. JTAG/Trace Pins The connection of the ICE connector to the nRESET pin in Figure 17.3 was modified. Pin handling and the GND description were modified.
		51	22. IBIS Information The website was modified.
		52	23.1 R-IN32M3-EC The product name and the marking information of the R-IN32M3-EC were modified.
			23.2 R-IN32M3-CL The product name and the marking information of the R-IN32M3-CL were modified.
		53 to 61	“24. Guide to Thermal Design” was newly added.
4.00	Dec. 28, 2018	37	Figure 12.1 Connection Example with Serial Flash ROM The names of R-IN pins were modified in the connection example.
		42	17 CSIH Pins Newly added

Rev.	Date	Description	
		Page	Summary
4.00	Dec. 28, 2018	50	Table 22.1 List of BSCAN Non-Supported Pins FB, P0_SD_N, and P1_SD_N were added in the R-IN32M3-EC.
		51	22.6 Notes on Using BSDL The description on notes on using BSDL was added.
		54	25. Thermal Design Section title was modified.
		64	26. Countermeasure for Noise Newly added
		—	Error corrected, description modified, and contents and expressions adjusted

[Memo]

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