User Manual

Industrial Ethernet PHY

Dual PHY ASSP

uPD60620
uPD60620A
uPD60621A

Renesas Electronics
www.renesas.com

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The following usage notes are applicable to all ASSP products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of ASSP Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

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6. Patent for IEEE1588
   A number of patents exist for systems related to IEEE1588. Renesas would request that customers ensure they comply with the relevant rights for these patents. Renesas does not accept any responsibility for infringement of any patent rights by the customer.

How to Use This Manual

(1) Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the PHY. It is intended for users designing application systems incorporating the PHY. A basic knowledge of electric circuits, logical circuits, and PHYs is necessary in order to use this manual. The manual comprises an overview of the product; descriptions of the PHY, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the Ethernet PHY products . Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description. Note: Refer to the application notes for details on using peripheral functions.	User's manual Industrial Ethernet PHY Dual PHY ASSP	This User's manual R19UH0083ED0100
Application Note	Information on using peripheral functions and application examples. Sample programs. Information on writing programs in assembly language and C.	Application Note industrial Ethernet Dual PHY ASSP Layout recommendation and design rule	R19AN0015ED0100
Renesas Technical Update	Product specifications, updates on documents, etc.	Customer Notification Ethernet PHY Operating Precautions	R19TU0004ED0100

(2) Notation of Numbers and Symbols

Abbreviation	Full Form
Register p.n	Register n at PHY address p
Register p.n.b	Bit ‘b’ in register address n at PHY address p
Register PHY.n	PHY stands for PHY address “0” or “1” so this would mean register n in any of the two PHYs, can by PHY address 0 or PHY address 1.

(3) Register Notation

Abbreviation	Full Form
RW	Readable or writeable
SC	Self Clearing
RO	Read Only
WO	Write Only
LH	Latch High, when the device sets the register it stays high until actively written to 0 even if the condition that set it disappears
LL	Latch Low, the register stays low until actively written to 1
WC	Cleared by hardware after writing
RC	Cleared after reading by hardware
NASR	Not affected by software reset

(4) List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PU	Pull Up
PD	Pull Down
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
PTP	Precision Timer Protocol
VCO	Voltage Controlled Oscillator

Table of Contents

General Description

The extended dual-channel 10/100 Ethernet PHYs uPD60620 uPD60620A and uPD60621A are fully integrated Physical layer devices to connect to standard IEEE802.3 Ethernet networks. Today's industrial networking standards often implement daisy-chain or ring structures, in which a dual-channel PHY configuration makes a perfect fit.

These devices specifically focus on low latency and low jitter to support today's industrial Ethernet standards. In addition, the uPD60621A features hardware support for IEEE1588 V2. Renesas Electronics' specific enhanced diagnosis features allow permanent cable quality monitoring for easy maintenance in factory automation applications.

The PHY can connect to unshielded twisted-pair (UTP) cable via external magnetics or to optical fiber via fiber PMD modules. It interfaces to an Ethernet MAC layer through the IEEE 802.3 Standard Media Independent Interface (MII) or reduced MII (RMII) interface.

The uPD60621A also includes support for PTP according to IEEE1588 Version 1 and 2. To support this, an 80-bit clock is included in the PHY. Timestamps with a resolution of as low as 1ns can be taken from received and transmitted frames and events on external pins. The device also supports one-step and two-step timestamp insertion and supports transparent mode.

1.1 Overview of product features

- Two channel PHY
- Fully standard compliant with IEEE 802.3i/802.3u for 100BASE-TX, 100BASE-FX and 10BASE-T
- Integrated PMD sub-layer featuring adaptive equalization and baseline wander correction
- IEEE 802.3u auto-negotiation and parallel detection
- Full and half duplex operation
- Supports automatic polarity detection and correction
- Supports automatic MDI/MDI-X crossover
- Supports IEEE1588 V1 and V2 (uPD60621A only)
- Up to 20 programmable GPIO's for trigger and capture (uPD60621A only)
- 2.5V and 3.3V MAC interface
- Flexible MAC interface: MII and RMII (uPD60620 only)
- Serial management port (MDC/MDIO)
- Supports user programmable interrupts

- Enables software power-up/down and automatic power up/down by energy detection
- Single 3.3 V power supply with optional separated 1.5V
- Operating temperature: $T_{ambient}$ = -40 to +85°C ($T_{junction}$ from -40 to +125°C)
- LQFP80 package (7 mm x 7 mm)

1.2 Special product features

- Low latency and low jitter for industrial networking
- Fast link-up option in auto-negotiation
- Fast link-loss detection
- Cable monitoring and error detection
- Permanent cable quality tracking
- Enhanced system testability (such as bypass, loopback and cable length measurement by TDR)
- 1 ns resolution timer for hardware support of IEEE1588 (uPD60621A only)
- Timestamping function to timestamp incoming and outgoing frames and pin activity (uPD60621A only)
- Output pins controllable by internal clock (uPD60621A only)
- 100BASE-TX, 100BASE-FX Repeater (uPD60620A, uPD60621A only)
- 100BASE-TX to 100BASE-FX Media converter (uPD60620A, uPD60621A only)

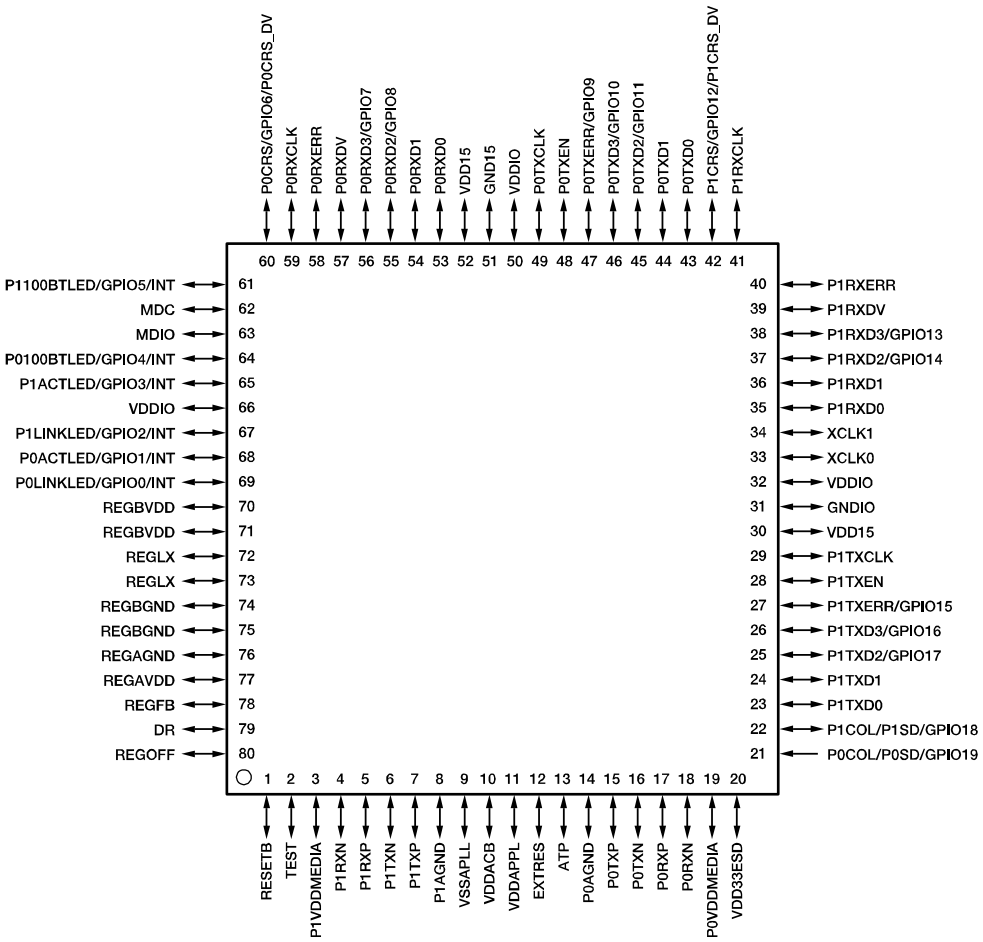
1.3 Applications

- Industrial networking such as Profinet, Ethernet/IP, CIPsync, ModbusTCP, EtherCAT and SercosIII
- 10/100 Mbps LAN on motherboard (LOM) and network interface card (NIC)
- Switches, routers and repeaters with 10/100 Mbps capable ports
- Mobile base stations
- Test and measurement applications
- Home servers, broadband routers, printers, and IP phones
- Telecom base stations
- Real-time networking

Pin Functions

2.1 Pin-out Information

2.1.1 Pin Layout



2.1.2 Port Pins

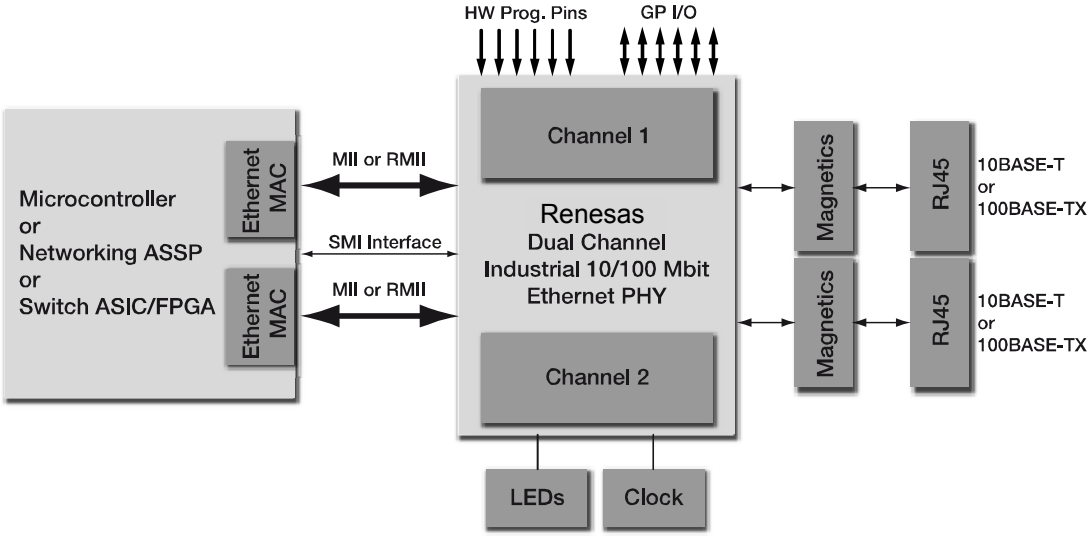
Power Supply	Pins	Comment
REGBVDD	70, 71	3.3V voltage regulator input
REGBGND	74, 75	GND for voltage regulator
VDDIO	32, 50, 66	3.3V/2.5V IO power supply
VDD33ESD	20	3,3V input
P1AGND, P0AGND	8, 14	Analog GND for PHY
REGAGND	76	Analog GND for regulator
REGAVDD	77	Analog 3.3V power supply for regulator
GNDIO	31	GND for I/O
GND15	51	GND for digital core
VDD15	30, 52	1.5V Digital VDD
VSSAPLL	9	Analog GND for PLL
VDDAPLL	11	Analog 1.5V power supply for PLL
VDDACB	10	Analog 3.3V power supply (common for both channels)
P1VDDMEDIA, P0VDDMEDIA	3, 19	Analog 1.5V power supply for PHY
REGLX	72, 73	Output voltage regulator, connect to external coil
REGFB	78	Feedback to voltage regulator, connect to external capacitor
REGOFF	80	Regulator disable, Hi: Regulator disabled Low: Regulator enabled

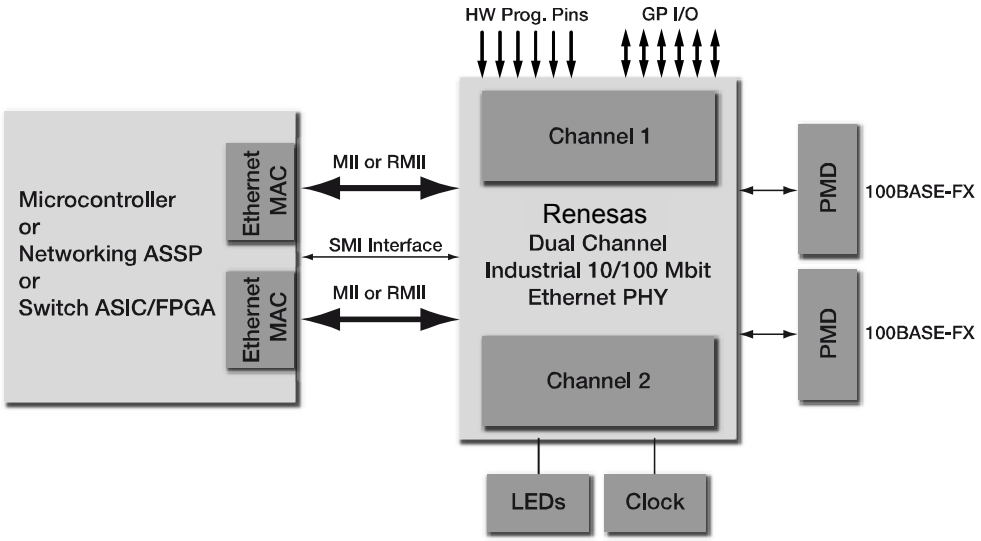
Pin Name	I/O	Function	Alternate Function	Pin Number	Comment
RESETB	I	RESET		1	
TEST	I	TEST		2	Connect to GND
P1RXN	I	Media Interface		4	
P1RXP	I			5	
P1TXN	O			6	
P1TXP	O			7	
P0RXN	I			18	
P0RXP	I			17	
P0TXN	O			16	
P0TXP	O			15	
EXTRES		Resistor		12	Connect to GND via 12.4kΩ resistor
ATP		Test		13	Pull Down (5kΩ)
P0COL	O	P0COL	P0SD/GPIO19	21	
P1COL	O	P1COL	P1SD/GPIO18	22	

P1TXD0	I	PHY1MII		23	
P1TXD1	I			24	
P1TXD2	I		GPIO17	25	
P1TXD3	I		GPIO16	26	
P1TXERR	I		GPIO15	27	
P1TXEN	I			28	
P1TXCLK	O			29	
XCLK0	I	XCLK0	50MHz (RMII)	33	Clock input in external clock mode
XCLK1	O	XCLK1		34	Open in external clock mode
P1RXD0	O	PHY1MII		35	
P1RXD1	O			36	
P1RXD2	O		GPIO14	37	
P1RXD3	O		GPIO13	38	
P1RXDV	O		P1CRS_DV	39	
P1RXERR	O			40	
P1RXCLK	O			41	
P1CRS	O		GPIO12	42	
P0TXD0	I	PHY0MII		43	
P0TXD1	I			44	
P0TXD2	I		GPIO11	45	
P0TXD3	I		GPIO10	46	
P0TXERR	I		GPIO9	47	
P0TXEN	I			48	
P0TXCLK	O			49	
P0RXD0	O	PHY0MII		53	
P0RXD1	O			54	
P0RXD2	O		GPIO8	55	
P0RXD3	O		GPIO7	56	
P0RXDV	O		P0CRS_DV	57	
P0RXERR	O			58	
P0RXCLK	O			59	
P0CRS	O		GPIO6	60	
P1100BTLED	O	LED	GPIO5/INT	61	
MDC	I	SMI		62	
MDIO	I/O			63	
P0100BTLED	O	LED	GPIO4/INT	64	
P1ACTLED	O		GPIO3/INT	65	
P1LINKLED	O		GPIO2/INT	67	
P0ACTLED	O		GPIO1/INT	68	
P0LINKLED	O		GPIO0/INT	69	
DR	O	Device Ready		79	

System Diagram

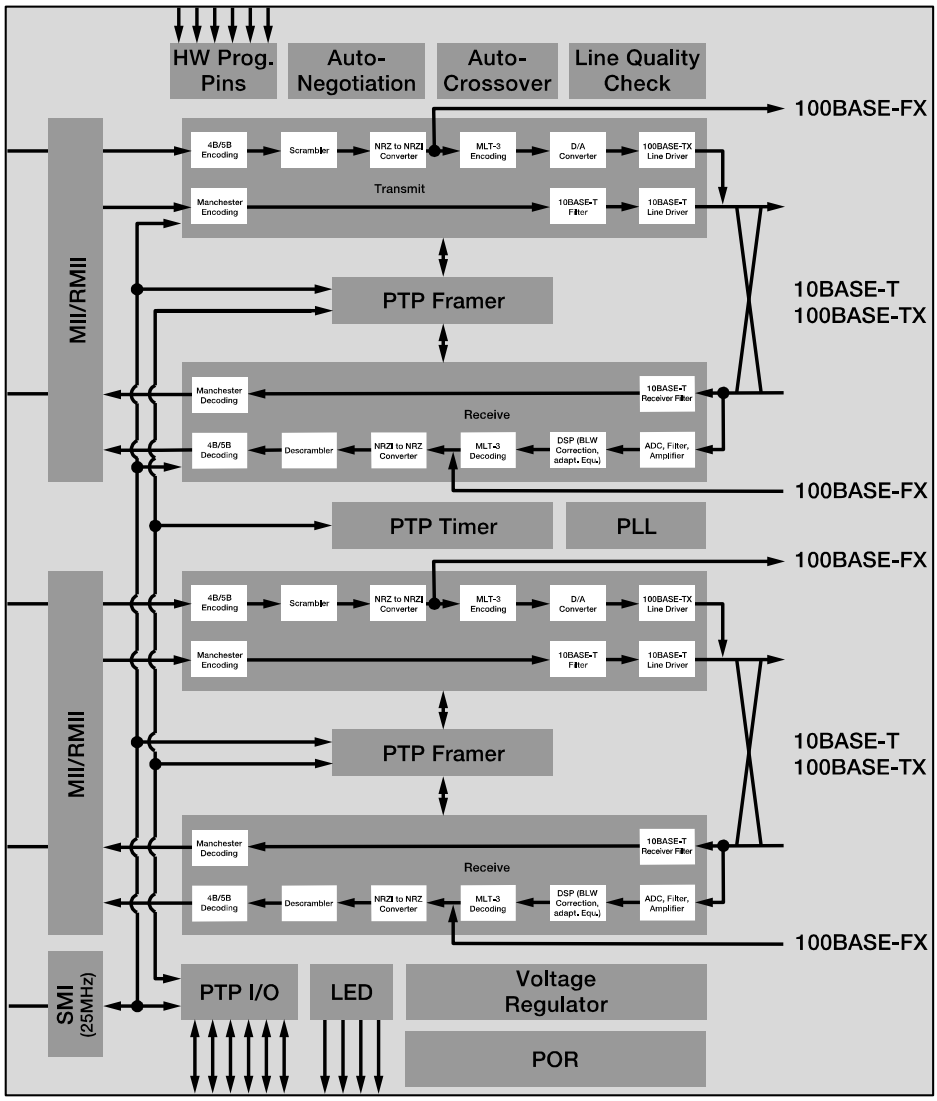
The picture below shows the system diagram. The PHY is connected to the MAC through a MII or RMII interface. On the other side it is connected either to a CAT5 cable through magnetics or to a fibre cable.





3.1 Device block diagram

The device consists of two PHY's each connected to a PTP Framer block used to de-/encode the PTP frames and timestamp them, a PTP timer block containing the PTP clock, and an I/O block for general configuration and I/O handling. The PTP support is only available on the uPD60621A.

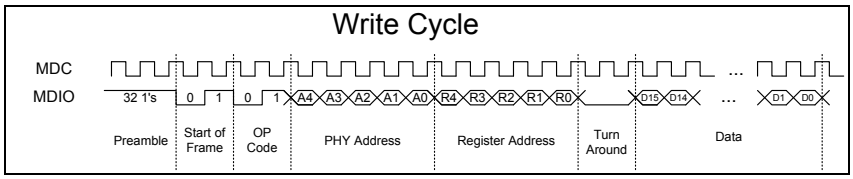


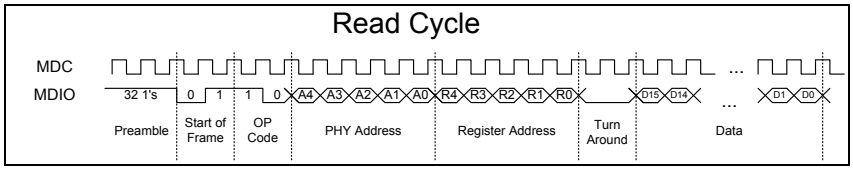
Global Hardware Description

The device consists of two Ethernet PHYs combined in a single package. In addition it includes a control block which is used to control shared resources such as LED outputs, interrupts, and low-power modes. All are accessible through a two wire bidirectional Serial Management Interface.

4.1 Register Access

All registers can be accessed through the MII / SMI interface. The SMI is a serial interface defined in IEEE802.3 for access to PHY registers. The following picture shows a typical access using the SMI interface:





The PHY address denotes the address of the PHY, while the register address is the address of the register within the addressed PHY. The device uses the PHY addresses to support access to the PTP block and the Global Configuration registers. The address table is as follows:

PHY Address (Binary)	Ressource	Comments
NM000	PHY0	
NM001	PHY1	
NM010	reserved	
NM011	Reserved	
NM100	Reserved	
NM101	Reserved	
NM110	PTP	uPD60621A only
NM111	GLOBAL_CONFIG PTP	

The values of the bits N and M can be configured as a strap option.

4.2 General SMI Control Register 7.31

The following register is used for configuration of the SMI:

Bit	Name	Description	Mode	Reset
15	RESET	1: Initiates a hardware reset of the complete device (stays active until cleared by software) 0: Release Reset	W	0
14	SMI_SHORT_PREAMBLE	1: Enable short preamble support. 0: Short Preamble mode for SMI interface not enabled	RW	0
13:9	Reserved	Write as 0	RW	0
8	Reserved	Write as 0	RW	1
7:2	Reserved	Write as 0	RW	0
1	PHY1_DISREGARD_ADDRESS	1: PHY 1 ignores the PHY address when the device is being written 0: The PHY checks for the PHY address	RW	0
0	PHY0_DISREGARD_ADDRESS	1: PHY 0 ignores the PHY address when the device is being written 0: The PHY checks for the PHY address	RW	0

4.3 Power Control Register 7.30

The following register is used for configuration of the power options:

Bit	Name	Description	Mode	Reset
15:13	POWER_STATUS	100: Device ready. Other than 100: Device not ready	RO	0
12	Reserved		RW	0
11	STOP	1: Device is disabled; only access to registers 7.25-7.31 in the GLOBAL_CONFIG area is possible. 0: Device is enabled	RW	0
10	PULSE_PWD	0: Pulse Output logic is enabled 1: Pulse Output logic for GPIO is powered down	RW	1
9	CAP_PWD	1: Capture logic is enabled 0: Capture logic for GPIO is powered down	RW	1
8	PTP_PWD	1: PTP is powered down 0: PTP is enabled	RW	1
7	Reserved	Write as 1	RW	1
6	Reserved	Write as 0	RW	0
5	C2C_STRAP_DIS	1: Strap option for channel to channel loopback disable 0: Strap option for channel to channel loopback enable	RW	0
4	C2C_EN	if "C2C_STRAP_DIS" = 1, 1: channel to channel loopback enable (repeater mode) 0: channel to channel loopback disable (normal mode) if "C2C_STRAP_DIS" = 0, don't care (Strap option effective)	RW	0
3:2	Reserved		RW	0
1	PHY1PWD	1: The analog and digital part of the PHY1 is powered down. The PLL is powered down if all PHYs are powered down 0: PHY1 is enabled	RW	0
0	PHY0PWD	1: The analog and digital part of the PHY0 is powered down. The PLL is powered down if all PHYs are powered down 0: PHY0 is enabled	RW	0

4.4 PHY Status Register 7.28

The following register shows the status of the PHYs.

Bit	Name	Description	Mode	Reset
15:10	Reserved	Write as 0	RW	0
9	PHY1_LINK	0: PHY 1 has no link 1: PHY 1 has link	RO	0
8	PHY0_LINK	0: PHY 0 has no link 1: PHY 0 has link	RO	0
7:2	Reserved	Write as 0	RW	0
1	PHY1_ SYSRST	1: PHY is powered up and able to operate, Reset not active 0: PHY is still powering up	RO	0
0	PHY0_ SYSRST	1: PHY is powered up and able to operate, Reset not active 0: PHY is still powering up	RO	0

The SYSRST registers are set by the PHY after the PLL has been powered up and has stabilized. They need to be 1 for the device to operate and to get access to all functions. Otherwise the internal 125 MHz clock is not available.

4.5 Strap option Register 7.27

The following register shows the strap option value latched after reset

Bit	Name	Description	Mode	Reset
15	QUICK_AUTONEG	Autonegotiation strap setting	RO	Strap option
14	AUTO_NEG	Quick Autonegotiation strap setting	RO	Strap option
13	AUTO_MDIX	Auto MDIX strap setting	RO	Strap option
12	FAST_JK	Fast JK strap setting	RO	Strap option
11	DUPLEX	Duplex strap setting	RO	Strap option
10	ADDR4	PHY address bit 4 strap setting	RO	Strap option
9	ADDR3	PHY address bit 3 strap setting	RO	Strap option
8	ETHERCAT	MII timing strap setting	RO	Strap option
7	MII	MII/RMII strap setting	RO	Strap option
6:2	Reserved	Reserved	RO	0
1	PHY1 TX	100BASE-TX / 100BASE-FX strap setting for PHY1	RO	Strap option
0	PHY0 TX	100BASE-TX / 100BASE-FX strap setting for PHY0	RO	Strap option

4.6 PHY LED Status Register 7.24

The following register shows the status of the PHYs after power up. To read the LED status for the PHYs first PHY_SELECT must be written with the number of the required PHY and then the data for this PHY can be read from the register. The ACTIVE_LED_BLINK bit can be used to control the LED outputs of the device. If a GPIO is configured for link detection setting this register will cause the GPIO to blink while data transmission is ongoing.

Bit	Name	Description	Mode	Reset
15	Reserved	Write as 0	RO	0
14	P0SD	Signal Detect signal is active	RO	0
13	PHY_TXACT	1: PHY had TX activity since last reading 0: PHY had no TX activity since last reading Cleared when read	R/LH	0
12	PHY_RXACT	1: PHY had RX activity since last reading 0: PHY had no RX activity since last reading Cleared when read	R/LH	0
11	PHY_FD	1: PHY runs on full duplex 0: PHY runs not on fill duplex	RO	1
10	PHY_LINK	1: PHY has LINK 0: PHY has no LINK	RO	0
9	PHY_100MB	1: PHY runs on 100 MBit 0: PHY runs not on 100 MBit	RO	1
8	PHY_10MB	1: PHY runs on 10 MBit 0: PHY runs not on 10 MBit	RO	0
7:4	Reserved		RO	0
3	ACTIVE_LED_BLINK	1: Link LED blinks if activity is detected and ON if link is up 0: Link LED does not blink on activity When written this is set for the PHY number in PHY_SELECT	RW	0
2:0	PHY_SELECT	Select number of the PHY for which the other bits of this register will be read. 000: Write to PHY0 001: Write to PHY1 Others: Reserved	RW	0

4.7 Interrupt Status register 7.20

To have a centralized register to get a summary of all possible interrupt sources an interrupt status register is placed at the top level in addition to the specific interrupt registers. The bits in this register are only set if the corresponding interrupt is enabled in the interrupt source modules.

Bit	Name	Description	Mode	Reset
15	TIMESTAMP_RX1_INT	PHY1 has received a telegram which caused a timestamp to be taken (uPD60621A only)	RC	0
14	TIMESTAMP_TX1_INT	PHY1 has transmitted a telegram which caused a timestamp to be taken (uPD60621A only)	RC	0
13	CAP_TS_STORED	The PTP capture unit stored an event (uPD60621A only)	RC	0
12	CAP_MEM_FULL_INT	PTP capture buffer is full (uPD60621A only)	R	0
11	RESERVED		R/LH	0
10	PTP_PERIOD_INT	Pulse generator started new period (uPD60621A only)	RC	0
9	TIMESTAMP_RX0_INT	PHY0 has received a telegram which caused a timestamp to be taken (uPD60621A only)	RC	0
8	TIMESTAMP_TX0_INT	PHY0 has transmitted a telegram which caused a timestamp to be taken (uPD60621A only)	RC	0
7	PHY1_LINK_DOWN_INT	PHY1 has triggered a Link Down Interrupt	RC	0
6	PHY1_BER_OVER_INT	PHY1 has triggered a BER Interrupt	RC	0
5	PHY1_FEQ_INT	PHY1 has triggered a FEQ interrupt	RC	0
4	PHY1_GENERAL_INT	PHY1 has triggered one of its internal interrupts except for Link Down, BER and FEQ interrupts	RC	0
3	PHY0_LINK_DOWN_INT	PHY0 has triggered a Link Down Interrupt	RC	0
2	PHY0_BER_OVER_INT	PHY0 has triggered a BER Interrupt	RC	0
1	PHY0_FEQ_INT	PHY0 has triggered a FEQ interrupt	RC	0
0	PHY0_GENERAL_INT	PHY0 has triggered one of its internal interrupts except for Link Down, BER and FEQ interrupts	RC	0

4.8 Interrupt Mask register 7.21

To provide a summary of all possible interrupt sources an interrupt mask register is placed at the top level in addition to the specific interrupt registers. Note that this is just an additional option to mask all interrupts at a central register; all Interrupts need to be enabled at their respective location within the PHY or PTP register set. Therefore the mask register is by default enabled while the interrupt sources are by default disabled.

Bit	Name	Description	Mode	Reset
15	TIMESTAMP_RX 1_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
14	TIMESTAMP_TX 1_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
13	CAP_TS_STORE D_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
12	CAP_MEM_FUL L_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
11	RESERVED		R/LH	0
10	PTP_PERIOD_IN T_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
9	TIMESTAMP_RX 0_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
8	TIMESTAMP_TX 0_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled (uPD60621A only)	R/W	0
7	PHY1_LINK_DO WN_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
6	PHY1_BER_OVE R_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
5	PHY1_FEQ_INT _MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
4	PHY1_GENERA L_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
3	PHY0_LINK_DO WN_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
2	PHY0_BER_OVE R_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
1	PHY0_FEQ_INT _MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0
0	PHY0_GENERA L_INT_MASK	0: Interrupt is enabled 1: Interrupt is disabled	R/W	0

4.9 GPIO

The GPIO pins can be configured depending on the application. Thus it is possible to repurpose unused pins for additional LEDs or PTP I/O. It is also possible to use the LED pins for PTP debug signals. The GPIO registers are located in the GLOBAL_CONFIG address range.

Each GPIO pin has a 4-bit configuration register assigned. The register configuration is only used if the pin is not used for Ethernet handling. So, for example, if MII is used many pins are used for MII. If RMII is used the unused pins can be configured for other purposes.

Note that if a GPIO is configured for LED usage, the polarity is reversed so a LED is always enabled if pulled down.

4.9.1 GPIO_CONFIG_0 Register 7.0

Bit	Pin	Description	Mode	Reset
15:12	GPIO3	Same as GPIO0:	RW	1100 P1ACTIVELED
11:8	GPIO2	Same as GPIO0 except: 0101: GPIO is Output for PTP Packet transmitted on PHY 1, If PTP is disabled on this PHY the start of any telegram will activate the pin. (uPD60621A only) 0110: GPIO is Output for PTP packet received on PHY 1, If PTP is disabled on this PHY the start of any telegram will activate the pin. (uPD60621A only)	RW	1000 P1LINKLED
7:4	GPIO1	Same as GPIO0	RW	1011 P0ACTIVELED
3:0	GPIO0	0000: No change when written 0001: GPIO is Output for PPS (Pulse per second) (uPD60621A only) 0010: GPIO is Output for PTP-OUT1 (Output of Pulse Out unit 1) (uPD60621A only) 0011: GPIO is Output for PTP-OUT2 (Output of Pulse Out unit 2) (uPD60621A only) 0100: GPIO is Output for PTP-OUT3 (Output of Pulse Out unit 3) (uPD60621A only) 0101: GPIO is Output for PTP Packet transmitted on PHY0, If PTP is disabled on this PHY the start of any telegram will activate the pin. (uPD60621A only) 0110: GPIO is Output for PTP packet received on PHY 0. If PTP is disabled on this PHY the start of any telegram will activate the pin.	RW	0111 P0LINKLED

		(uPD60621A only) 0111: GPIO is Output for P0LINKLED 1000: GPIO is Output for P1LINKLED 1001: GPIO is Output for P0_100BT-LED 1010: GPIO is Output for P1_100BT-LED 1011: GPIO is Output for P0ACTIVELED 1100: GPIO is Output for P1ACTIVELED 1101: GPIO is Output for INT 1110: GPIO is Output for CHIP_SYNC (uPD60621A only) 1111: GPIO is Input		

4.9.2 GPIO_CONFIG_1 Register 7.1

Bit	Name	Description	Mode	Reset
15:12	GPIO7	MII mode: always P0RXD3, regardless of setting. RMII mode: same coding as GPIO0 except for: 1110: CHIP_SYNC (uPD60621A only)	RW	1110 in RMII
11:8	GPIO6	RMII Mode: P0CRS_DV MII Mode: Same as GPIO0 except 1110: P0CRS	RW	0111 P0CRS
7:4	GPIO5	Same as GPIO0 except 1110: GPIO is output for P1COL	RW	1010 P1_100BT_LED
3:0	GPIO4	Same as GPIO0 except: 1110: GPIO is output for P0COL	RW	1001 P0_100BT_LED

4.9.3 GPIO_CONFIG_2 Register 7.2

Bit	Name	Description	Mode	Reset
15:12	GPIO11	MII mode: always P0TXD2, regardless of setting. RMII mode: coding is same as GPIO0 1110: SOF_TX0 Start of frame PHY0 TX path (uPD60621A only)	RW	1111 in RMII
11:8	GPIO10	MII mode: always P0TXD3, regardless of setting. RMII mode: coding is same as GPIO0 1110: SOF_TX0 Start of frame PHY0 TX path (uPD60621A only)	RW	1111 in RMII
7:4	GPIO9	Same as GPIO0 except 0101: Input for P0TXERR	RW	0101
3:0	GPIO8	MII mode: always P0RXD2, regardless of setting. RMII mode coding is same as GPIO0 1110: SOF_RX0 Start of frame PHY0 RX path (uPD60621A only)	RW	1111 in RMII

4.9.4 GPIO_CONFIG_3 Register 7.3

Bit	Name	Description	Mode	Reset
15:12	GPIO15	Same as GPIO0 except 0101: Input for P1TXERR	RW	0101
11:8	GPIO14	MII mode: always P1RXD2, regardless of setting. RMII mode: coding is same as GPIO0 except 1110: SOF_RX1 Start of frame PHY1 RX path (uPD60621A only)	RW	0010 in RMII else P1RXD2
7:4	GPIO13	MII mode: always P1RXD3, regardless of setting RMII mode: coding same as GPIO0 except 1110: GPIO is output for SOF_RX1 (uPD60621A only)	RW	0001 in RMII else P1RXD3
3:0	GPIO12	RMII mode: always P1CRS_DV MII mode: Same as GPIO0 except 0101: GPIO is output for PTP Packet transmitted on PHY 1 (uPD60621A only) 0110: GPIO is output for PTP packet received on PHY 1 (uPD60621A only) 1110: GPIO is output for P1CRS	RW	1110 P1CRS

4.9.5 GPIO_CONFIG_4 Register 7.4

Bit	Name	Description	Mode	Reset
15:12	GPIO19	PHY 0 in FX mode: always P0SD PHY 0 in TX mode: coding is same as GPIO0 except 1110: P0COL	RW	1110 P0COL
11:8	GPIO18	PHY 1 in FX Mode: always P1SD PHY 1 in TX mode: coding is same as GPIO0 except 1110: P1COL	RW	1110 P1COL
7:4	GPIO17	MII mode: always P1TXD2, regardless of setting RMII mode: coding is same as GPIO0 except 0101: GPIO is output for PTP Packet transmitted on PHY 1 (uPD60621A only) 0110: GPIO is output for PTP packet received on PHY 1 (uPD60621A only) 1110: SOF_TX1 Start of frame PHY1 TX path (uPD60621A only)	RW	0100 in RMII
3:0	GPIO16	MII mode: always P1TXD3, regardless of setting. RMII mode: coding is same as GPIO0 except 1110: SOF_TX1 Start of frame PHY1 TX path (uPD60621A only)	RW	0011 in RMII

4.10 Strap Options

The device offers several configurations which can be selected as strap options. The related I/Os have integrated 40 kΩ pull-up or pull-down resistors which configure the device as described below. To change this configuration an external resistor of maximum 5 kΩ must be connected to the pin. An external resistor supporting the internal resistor is also advisable in case the device is used in a very noisy environment.

The following table shows the possible configuration options and the related pins. Unless otherwise noted all configuration options apply to both PHYs.

Table 4-1 Strap options

Pin Name	Function	Default value
P1RXD1	0: Autonegotiation disabled, 100BaseT 1: Autonegotiation enabled, 100BaseT	1, PU
P1RXD0	If Autonegotiation disabled: 0: Half Duplex 1: Full Duplex If Autonegotiation enabled: 0: Parallel detect ends in half duplex mode 1: Forced Full Duplex in parallel detect	1, PU
P1RXCLK	0: Disable Quick Autonegotiation 1: Quick Autonegotiation, shortest times (Autonegotiation required) See also special strap modes in table 4-2	1, PU
P0RXERR	0: Configure RMII Interface 1: Configure MII Interface	1, PU
P1RXERR	0: Standard Mode, “JK” required for Start of Frame detection 1: Fast Mode, Only “J” required for Start of Frame detection	1, PU
P0RXCLK	0: AUTOMDI-X disabled. 1: AUTOMDI-X enabled	1, PU
P0RXDV	0: FX Mode for PHY0, in this case the values of Autonegotiation, Duplex are ignored for this PHY. 1: TX Mode for PHY0	1, PU
P1RXDV	0: FX Mode for PHY1, in this case the values of Autonegotiation, Duplex ignored for this PHY. 1: TX Mode for PHY1	1, PU
P0RXD0 / P0RXD1	Configures the upper two bits N and M of the PHY addresses 00: device uses address 00xxx for SMI 01: device uses address 01xxx for SMI 10: device uses address 10xxx for SMI 11: device uses address 11xxx for SMI	00, PD

P1TXCLK	0: Synchronous mode for TXCLK. TXCLK is synchronous to XCLK0. This must be used for MACs that supply the MII TX data synchronously to the XCLK0 signal. 1: Asynchronous mode for TXCLK. This mode reduces the TX Latency, but requires a MAC that handles the TXCLK signal to supply the MII TX data. This is the typical behavior.	1, PU

To configure the PHY via strap pins to special modes unusual combinations of the strap pins are used. The PHY modes are shown and described in table 4-2.

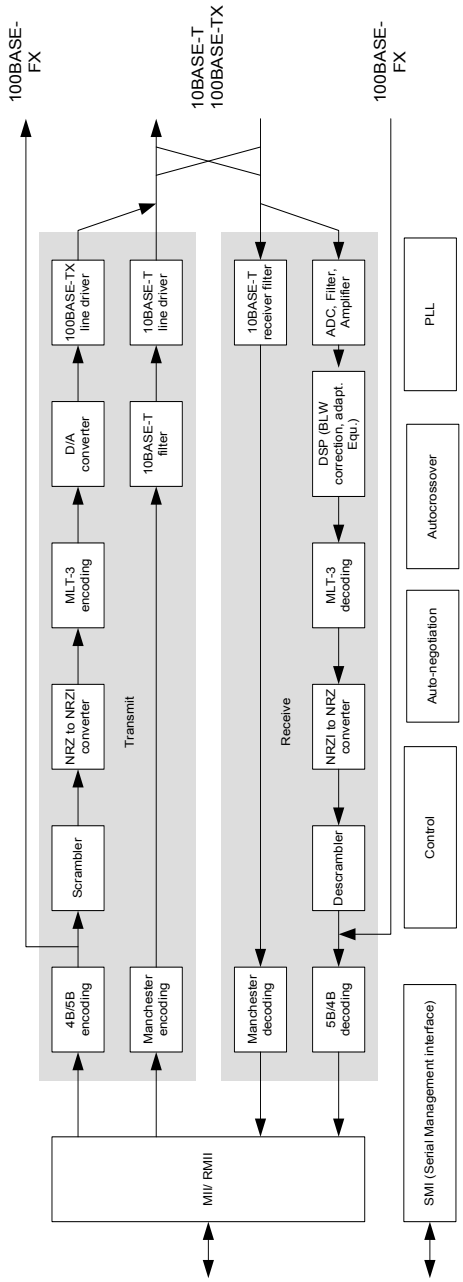
Table 4-2 Special strap options

Mode	Description	Strap combination
Special Isolate Mode	In this mode the PHYs will not set up a link unless programmed and enabled through the SMI	Autonegotiation OFF ➔ PD at P1RXD1 Quick Autonegotiation ON ➔ PU at P1RXCLK (default) Full Duplex ➔ PU at P1RXD0 (default)
Repeater Mode	In this mode a channel to channel loopback is enabled. The data from the RX ports is forwarded to the TX port of the other channel. PHY configuration in repeater mode is 100BT FD.	Autonegotiation OFF ➔P1RXD1 Quick Autonegotiation ON ➔ PU at P1RXCLK (default) Half Duplex ➔ PD at P1RXD0

PHY

5.1 General Description

The device contains two PHYs. The block diagram for each is shown below:



5.2 Clock Generator PLL

The PLL is a 125 MHz PLL which generates the clock for the 125 MHz part. It generates 32 output phases. The DSP selects which of these phases is used to sample the incoming signal. A single PLL is used for both PHYs. Therefore a Power Down of a PHY will only power down the PLL if both PHYs are powered down.

5.3 Analog Frontend

The analog frontend consists of two Programmable Gain Amplifiers, a low pass filter and the ADC.

5.3.1 Adaptive Equalizing

The adaptive equalizer compensates for phase and amplitude distortion caused by the Physical channel consisting of magnetics, connectors, and CAT-5 cable. The equalizer can restore the signal for any good quality CAT-5 cable.

5.3.2 100Base TX Receiver ADC

The Receiver ADC is part of the analog block. It is clocked with a 125 MHz clock which can be selected by the DSP from one of 32 phases.

5.4 Digital Signal Handling

The following chapters describe how the signal is handled in the digital part of the PHY.

5.4.1 DSP

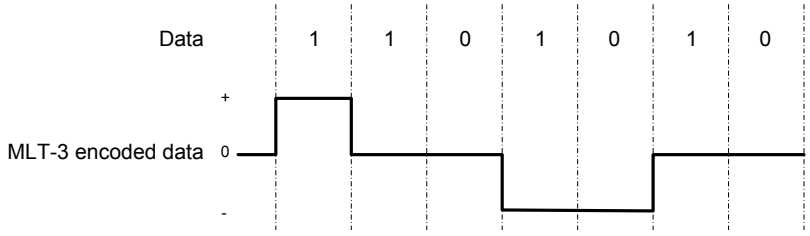
The DSP is re-shaping the received signal so it can be further processed. The ADC samples the signal at 125MHz. However the frequency of the signal is significantly lower than 125MHz due to the MLT-3 coding. Based on the received and decoded signal the DSP can measure the quality of the signal and either adjust internal filters or adjust the sampling phase of the ADC. One of the internal filters can be read to observe the cable quality.

5.4.2 Baseline Wander Correction

If the DC content of the signal is such that the low-frequency components fall below the low-frequency pole of the isolation transformer, then the drop characteristics of the transformer will become significant and baseline wander (BLW) on the received signal will result. To prevent corruption of the received data, the DSP corrects for baseline wander.

5.4.3 NRZI/MLT-3 Encoding / Decoding

MLT3 is a specific version of a NRZI coding using a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”. Basically it uses the NRZI coding as input but the ‘1’ is flipped to ‘-1’ every second time. The main advantage is that it reduces the effective frequency on the cable to 1/4 or 125/8 MHz. The decoder converts the MLT-3 data coming from the DSP to a NRZ data stream. The conversion of data to NRZI/ MLT-3 encoded data is shown in the following picture.



This code is used on the Ethernet data lines in 100TX mode.

5.4.4 Scrambler / Descrambler

To reduce EMI the data sent is scrambled before it goes on the line and descrambled in the receiver. This reduces the emission at specific frequencies and spreads the emissions over a wider frequency band.

Scrambling the data helps eliminate large narrow-band peaks for repeated data patterns, and spreads the signal power more uniformly over the entire channel bandwidth. The seed for the scrambler is generated from the PHY address, ensuring that in multiple-PHY applications each PHY will have its own scrambler sequence.

The descrambler descrambles the decoded NRZ cipher-text bit from the MLT-3 decoder. The cipher-text bit stream is decoded by addition (modulo 2) of a key stream to produce a plain-text bit stream.

During reception of IDLE symbols, the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

5.4.5 5B/4B Encoding / Decoding

The data on the line is coded 4B/5B and decoded on the receive path. The main purpose is to remove repeated values, i. e. 0000 is replaced by 11110 to ensure there is a signal change after a certain period. In addition it allows detection of faulty transmissions and adds control data.

The following table shows the relationship between payload data and the 5B interpretation.

PCS code-group [4:0]	Name	MII (TXD/RXD) [3:0]	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 0 1 1	5	0 1 0 1	Data 5
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE; Used as inter-stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; Always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; Always used in pairs with J
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter, Part 1 of 2; Always used in pairs with R
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter, Part 2 of 2; Always used in pairs with T
0 0 1 0 0	H	Undefined	Transmit Error; Used to force signaling errors
0 0 0 0 0	V	Undefined	Invalid code
0 0 0 0 1	V	Undefined	Invalid code
0 0 0 1 0	V	Undefined	Invalid code
0 0 0 1 1	V	Undefined	Invalid code
0 0 1 0 1	V	Undefined	Invalid code
0 0 1 1 0	V	Undefined	Invalid code
0 1 0 0 0	V	Undefined	Invalid code
0 1 1 0 0	V	Undefined	Invalid code
1 0 0 0 0	V	Undefined	Invalid code
1 1 0 0 1	V	Undefined	Invalid code

5.5 Functional Description

5.5.1 Collision detection

When transmissions from two stations overlap, the resulting contention is called a collision. Collisions occur only in half duplex mode, where a collision indicates that there is more than one station attempting to use the shared Physical medium.

5.5.2 Carrier Sense detection

Carrier Sense (CRS) is asserted by the PHY when either transmit or receive medium is non-idle. For half-duplex mode, Carrier Sense is asserted during transmission or reception. For full-duplex mode, Carrier Sense is asserted during reception.

5.5.3 Auto Crossover (MDI/MDI-X)

The PHY automatically detects and corrects for the MDI/MDI-X crossover in TX modes. Auto-Crossover is disabled in FX Mode. If this function is disabled, crossover may be corrected manually through the Serial Management Interface. The status of the crossover function can be read from a status register. The detection process is started whenever the PHY is turned on and Auto Crossover is activated. As soon as the partner PHY is transmitting it will immediately adjust the crossover as required.

5.5.3.1 Auto-Crossover when using 100BT Fix Mode

In 100BT manual mode the transmitter continuously transmits idles on the TX line. As the incoming echo from the transmitter path needs to be blocked there is no chance to listen on that line. Therefore a special non-standard implementation called 100BT idle burst mode is employed. The idle burst mode has two states, a period of idle burst and a period of random silence to detect incoming signals on the TX line. The time for the next transmission will be picked randomly. The decision to do a switchover will be made based on the reception of two signals within a specific time period.

The PHY will transmit bursts of 1 µs after a waiting time of 0 - 63 µs. In parallel it checks both lines for a signal. If a valid signal is received on the RX line, it will continue normal operation. If a valid signal is received on the TX line it will wait for 500µs and then reverse the setting (exchange TX and RX). Again after a time of 0 - 63µs it will send a burst of 1 us and in parallel check if there is a signal on one of the lines. This will continue until a valid signal is detected on the RX line.

The PHY will only do a crossover if it detects signals on the actual TX line. On an open line it will not exchange the RX/TX lines as it cannot receive any signals.

The duration of this process can be <1 µs if the signal is initially recognized correctly and approximately 565µs if crossover is required.

5.5.3.2 Auto-Crossover when using Autonegotiation or 10BT Mode

Since the auto-negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link, the energy detection upon FLPs bursts is the same as the NLPs. The NLP is a pulse transmitted every 16±8 ms. and its pulse width is 100ns. Typical burst width is 2 ms.

After reset the PHY will check for a signal on the incoming lines. As it is in its "Break_link_timer" state it will not start transmission before this timer is expired. If there is a signal detected in that period it will adjust the MDI/X accordingly and continue. If no signal is detected it will start transmitting the FL-Pulses to establish a connection. As the switchover is in general done during the duration of the Break_link_timer, there is no additional time required for Auto-Crossover in Autonegotiation Mode.

5.5.3.3 Auto-Crossover when connecting Autonegotiation and 100BT Mode

This is a situation in which one link partner A is in auto-negotiation mode and the other partner F is set to 100 Mb/s fix mode.

After power-up the forced PHY F will start sending FLP while the other link partner A is in Transmit disable state. So while PHY A will wait for its ***break_link_timer*** time (1200ms-1500ms) the forced PHY F will turn itself off randomly for every time period of ***sample timer*** (62±2us) to listen for a signal on its TX line. It will not change its transmit line pair unless it detects a contention. PHY A adjusts its Autocrossover state as it received a signal during its break_link_timer expiration time. When PHY A moves to ABILITY_DETECT mode and transmits FLP PHY F detects these pulses. As PHY A has already adjusted its autocrossover mechanism correctly, there is no need for PHY F to do so.

5.5.4 Auto-Polarity

The PHY automatically detects and corrects for polarity reversal in wiring in 10BASE-T mode. The result of polarity detection is indicated by the flag "XPOL", bit 4 in register PHY.27. Polarity is checked at end of packets in 10BASE-T.

5.5.5 Auto-Negotiation

The objective of the auto-negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-negotiation protocol is a purely Physical layer activity and proceeds independently of the MAC controller.

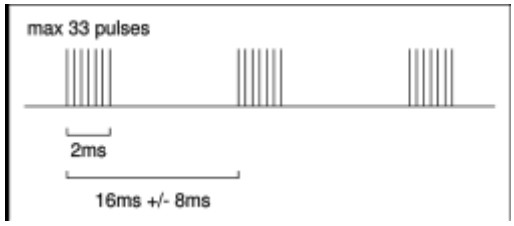
Prior to the start of any kind of negotiation the PHY is required by the IEEE 802.3 Chapter 28 to wait the Break_Link_Timer time which is defined to be between 1200 ms and 1500 ms. This time is defined to make sure both PHYs are reset and reach a defined status prior to starting the negotiation process.

For the auto-negotiation function, the two PHYs communicate by sending FLP (Fast link Pulse) bursts for exchanging information with its link partner. A FLP burst consists of 33 pulse positions. The 17 odd-numbered pulse positions

contain a link pulse and represent clock information. The 16 even-numbered pulse positions represent data information. The data transmitted by an FLP burst is known as a "Link Code Word". These are fully defined in clause 28 of the IEEE 802.3 specification.

After the Break Link Timer has expired, the link down status is achieved and, if auto-negotiation is enabled, the PHY starts to send FLP bursts while trying to receive signals on its receive path. If it detects signals according to 10BaseT, 100BaseTX or 100BaseT standard, it will wait for FLP bursts and check the received signals until the autoneg_wait_timer period (typically 500ms) has expired and then switch to fix mode according to the received signal.

The following picture shows the FLP burst.



These 33 pulses contain an acknowledge bit which is cleared at the start of the sequence. Each partner starts to send FLP bursts and tries to receive them from the other with the acknowledge bit cleared.

After one partner has successfully received three identical FLP bursts it continues sending FLP bursts with the acknowledge bit set. The other partner will wait until it has received this answer for three times. After that both partners will send 6-8 FLP bursts with the acknowledge bit set to ensure that they have understood each other successfully. After that both PHYs will resolve the information and decide on the optimum configuration.

Therefore it is required that at least 9 FLP bursts are sent to initiate a successful auto-negotiation. Thus a successful auto-negotiation will last at least 72 ms up to 216 ms depending on the burst length, if all transmissions are successful and the next page function is not used. In case a pulse is distorted the process will start over again.

To improve the linkup time for two Renesas PHYs the nominal 16ms frame rate is reduced to allowed 8 ms and shortening the frame transmission time. In this case two Renesas PHYs are able to negotiate within 72 ms without hurting the IEEE spec.

This PHY supports auto-negotiation and implements the “Base page”, defined by IEEE 802.3. It also supports the optional “Next page” function to get the remote fault number code.

5.5.5.2 Disabling Auto-Negotiation

Auto-negotiation can be disabled by register setting or by setting the appropriate strap pins. When auto-negotiation is disabled, the speed and duplex modes are decided by setting management interface registers or Parallel Detection.

5.5.5.3 Priority Resolution

There are four possible operating modes. In the order of priority these are:

100M full duplex (highest priority)

100M half duplex

10M full duplex

10M half duplex

Since two devices (local device and remote device) may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. Full duplex solutions are always higher in priority than their half duplex counterparts.

10BASE-T is the lowest common denominator and therefore has the lowest priority. If a link is formed via parallel detection, then bit 0 in Register PHY.6 is cleared to indicate that the link partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, bit 4 of register PHY.6 is set. Register PHY.5 is used to store the link partner ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then register PHY.5 is updated after completion of parallel detection to reflect the speed capability of the link partner.

5.5.5.4 Next Page Function

Additional information beyond that required by base page exchange is also sent via “next pages”. This PHY supports the optional “next page” function.

Next page exchange occurs after the base page has been exchanged. Next page exchange consists of using the normal auto-negotiation arbitration process to send next page messages. Two message encodings are defined: Message pages, which contain predefined 11 bit codes, and unformatted pages.

Next page transmission ends when both ends of a link segment set their next page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its next page information, it shall transmit message pages with null message codes and the NP bit set to logic zero while its link partner continues to transmit valid next pages. Auto negotiation capable devices shall recognize reception of message pages with null message codes as the end of its link partner’s next page information.

The default value of the next page support is disabled (bit 15 of register PHY.4). To enable next page support, bit 15 of Register PHY.4 should be set to “1”. Auto-negotiation should be restarted, and the message code should be written to bit [10:0] of register PHY.7.

5.5.5.5 Re-negotiation

When auto-negotiation is enabled, it may be re-started by one of the following events:

1. Link status is down.

2. Setting Auto-Negotiation Restart bit to high.

Auto-negotiation is started (not re-started) when 1) Hardware reset, 2) Software reset or 3) setting Auto-Negotiation Enable from low to high.

5.5.5.6 Parallel Detection

The parallel detection function allows detection of link partners that support 100BASE-TX and/or 10BASE-T, but do not support auto-negotiation or are set to fix mode. The PHY is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Link Pulses. If the PHY detects either mode, it automatically reverts to the corresponding operating mode.

In this case the link is always half duplex as defined in the IEEE spec. If a link is formed via parallel detection, then register PHY.6.0 is cleared to indicate that the link partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, register PHY.6.4 is set. register PHY.5 is used to store the link partner ability information, which is coded in the received FLPs. If the link partner is not auto-negotiation capable, then register PHY.5 is updated after completion of parallel detection to reflect the speed capability of the link partner.

Similar to the auto-negotiation process the PHY waits for the Break_Link_Timer duration before starting parallel detection. After reception of the first link signals, the parallel detection process waits for another 500 ms to check if FLP bursts are received.

5.5.5.7 Parallel Detection → Speculative Full Duplex

In modern Ethernet systems it is unlikely that a 100 MBit fix mode PHY is actually using half duplex. However if the IEEE 802.3 is fulfilled the PHY doing auto-negotiation will revert to half duplex operation following the parallel detect operation. Thus the result of the parallel detect mode is one PHY running at 100 MBit full duplex and the other running at 100 MBit half duplex. Although communication is possible this will lead to many errors as the half duplex configured PHY will continuously detect collisions when the full duplex PHY is transmitting and receiving simultaneously.

To avoid this situation the PHY can be configured to go into full duplex instead of half duplex in parallel detection mode by means of a strap option.

5.5.6 Bad Line recognition

The PHY features a number of functions to control and observe the line to be able to ensure a reliable connection.

5.5.6.1 BER-Monitor

The PHY can continuously measure the bit error rate (BER) on the line and trigger an interrupt or put the link down if a configurable threshold is reached.

Bit errors are detected by checking the received symbols against the list of allowed symbols. There are two basic conditions for this check:

1. IDLE situation: When the PHY is in idle mode it should only receive IDLE symbols or the start of frame delimiter which is a J symbol. All other symbols indicate that a bit error has happened and are counted as errors.

2. Data transmission: During data transmission there are 32 possible symbols of which only 19 are valid symbols. The rest indicate a bit error and will be counted as such. Note that the /H/ symbol is also counted as an error symbol.

A pre-condition of the BER mechanism operation is the lock of the descrambler; it will try to adjust itself while receiving IDLE patterns and is considered locked if a reasonable number of IDLE patterns have been received and descrambled. Unless the descrambler is locked, the BER monitor is not operable, and no data can be received.

Register PHY.23 – BER

Bit	Name	Description	Mode	Default
23:15	BER_LNK_OK	Link quality indication – indicates state of link monitor. '0' – Not in 'Good Link' state '1' – In 'Good Link' state Will go up as soon as the counter is below the trigger level after start up. Can be used to detect link up after start up.	R	0
23:14	BER_CNT_LNK_EN	1: A trigger on the BER or on the FEQ monitor will cause a link down. 0: A trigger on the BER/FEQ will just cause the state machine to leave “Good Link” state.	RW	1
23.13:11	BER_CNT_TRIG	Trigger level for BER Count to define link up/down Counter in 2^(n -1) errors 0: >0 errors will trigger 1: >1 triggers 2: >2 triggers 3: >4 triggers 4: >8 triggers 5: > 16 triggers 6: >32 triggers 7: > 64 errors triggers	RW	2

23.10:7	BER_WINDOW	Length of time for BER counter in 0.005 * 2^n ms 0: BER counter functions disabled 1: 0.01 ms 2: 0.02 ms 3: 0.04 ms … 14: 81.92 ms 15: unlimited run window. Writing a 0 resets the BER counter and restarts the time window.	RW	1 (0.01 ms)
23:6:0	BER_COUNT	Counter for bit errors, shows the amount of errors in the past time window. Is updated every 100 µs if BER_WINDOW = 15	R	0x0

5.5.6.2 FEQ-Monitor

In order to optimize the reception of the incoming data, the DSP continuously adapts its filters to the incoming signal. To be able to monitor the line quality, one of the DSP filter coefficients can be monitored and an interrupt or link down can be triggered if programmable limits are exceeded.

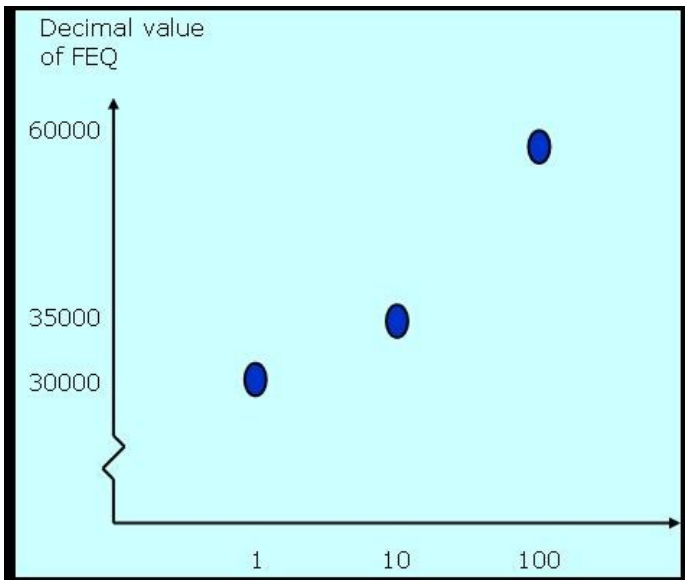
The FEQ2 coefficient changes as the DSP tries to re-adapt to match a changed line characteristic caused for example by a line break or increased resistance due to corrosion. This change is done within 1 to 9µs when the line condition changes depending on line length and cable quality. So by using the FEQ monitor, line changes can be safely detected within 9 µs.

The FEQ2 value is latched at link up time. By programming the FEQ2_DELTA field in register PHY.24 the allowed deviation of this value can be set. Whenever the FEQ2 is outside of this border due to changes in line condition an interrupt or link down is initiated. Note that after a link down the FEQ2 value is relatched so then a link is established based on the then actual FEQ2 value. In this case the application needs to take control and decide how to continue.

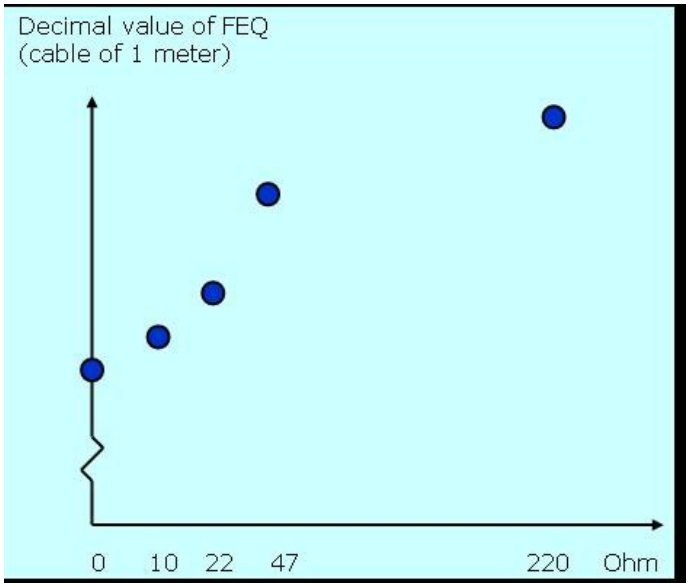
Register PHY.24: FEQ Monitor Control Register

Bit	Name	Description	Mode	Default
24.15:0	FEQ_DELTA	Minimum change of value (compared to the reference value latched when the monitor is enabled after link up) that will trigger the FEQ interrupt and link down. If the FEQ value differs by more than FEQ_DELTA the link goes down if the BER_CNT_LNK_EN is 1 and the BER monitor is enabled, The interrupt is also triggered if enabled. 'FFFF' – will disable monitor and cause the reference value to be re-latched continuously. 'FFFE' – will not change the FEQ_DELTA value but will instead allow read out the current reference value from FEQ_VAL. Writing any other value will disable this mode.	W	0xFFFF
24.15:0	FEQ_VAL	If FEQ_DELTA == FFFE Bit 17:2 of the reference value. Else Bits 17:2 of the current FEQ2 coefficient.	R	Undefined

The following picture gives an example of the value of the FEQ coefficient for several line lengths (in meters.)



The following picture gives an example of the dependency of the FEQ coefficient on the resistance of the line. The 0 Ohm resistance is the value for a 1 meter line, for the other values a resistor has been added to the RX line.



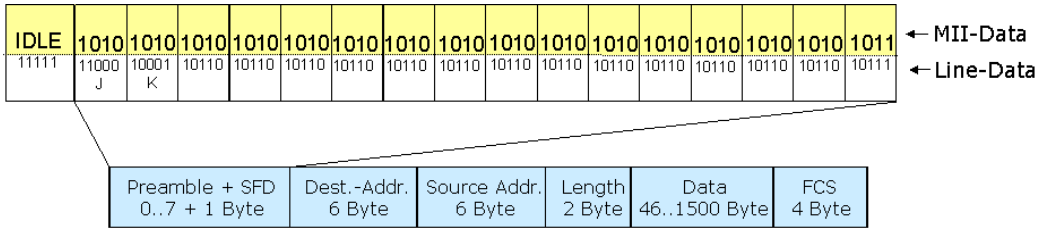
The blue circles indicate the typical variation of the FEQ2 value.

5.5.7 Latency

The latency is the length of time it takes for data to pass through the PHY from the line interface to the MII and also from the MII to the line interface on the TX side. For industrial real-time applications a short latency is very important as it has a significant influence on the cycle times that can be achieved and the accuracy at which a system can be operated. Both the latency itself and the variation in latency (jitter) should be as small as possible.

Although the Renesas PHY has already a very short latency, the PHY has a special mode that will reduce the latency even further. This mode is called “J-only mode” and is available on all devices of the PHY family.

A new telegram is initiated by two symbols “J” and “K” as shown in the picture below:



Before data is sent it is transformed from a 4-bit notation at the MII to a 5 bit notation on the line to ensure that enough transitions are available for the clock regeneration. In addition the 5-bit coding allows for transmission of additional control symbols to indicate start of frame and end of frame. A start of frame is indicated by the symbol 11000 or “J” followed by a 10001 or “K”.

Standard devices (conforming to the Ethernet standard) must detect the leading “J”- and “K”- symbol of a telegram as start-of-frame, before they can start to output data on the MII interface. Thus two symbols have to be received before output can be started on the MII interface. The Renesas PHY offers a special mode to only decode the leading J-symbol and start receiving the data immediately. The PHY will thus output data on the MII following the first “J” symbol without waiting for the reception of the “K” symbol.

This reduces the roundtrip delay by 40ns. This PHY family is thus able to support a roundtrip delay <200ns. In the unlikely case that the “J” detection was due to a bit error and the next “K” symbol is not received the RX_ERR signal is asserted and reception resumes.

5.5.8 Special Isolation Mode

In many applications it is desirable to have a more flexible option to configure the PHY compared to strap options which need to be decided when the board is produced. Usually a PHY will read the configuration from the strap pins and try to connect immediately after power up. This does not leave time for a microcontroller to change the configuration before the communication and setup with the partner PHY has been started. In special isolation mode the PHY will not connect to its partner PHY but stay quiet on the line until enabled by software. This mode provides time for a microcontroller to configure the PHY which means configuration can be controlled by firmware instead of hardware.

5.5.9 Repeater / Media converter

This PHY supports channel to channel loopback mode and can be used as physical repeater. In this mode, the received frame at each port is directly forwarded to the other port. Channel to channel loopback mode is configured by strap option or register setting. (Refer to 4.10 Strap Options and 4.3 Power Control Register 7.30)

As an application of repeater function, this PHY works as media converter (100BASE-TX to 100BASE-FX) by setting each port as 100BASE-TX and 100BASE-FX respectively,

5.6 PHY Register List

The PHY registers can be accessed at PHY address 0 for PHY 0 or PHY address 1 for PHY 1. These registers control only the PHY they belong to. Some of these registers are duplicated on the PHY address 7 registers to ease software handling.

5.6.1 Register PHY.0 - Basic Control

Bit	Name	Description	Mode	Default
15	RESET	1 = software reset 0 = normal operation When setting this bit do not set other bits in this register	RW/SC	0
14	LOOPBACK	1 = enable internal loopback mode 0 = disable internal loopback mode	RW	0
13	SPEED_ SELECTION	1 = 100 Mb/s 0 = 10 Mb/s This bit is ignored if auto-negotiation is enabled (0.12=1).	RW	1
12	AUTO-NEGOTIATION_ ENABLE	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process	RW	Strap option
11	POWERDOWN	1 = General Power down 0 = normal operation	RW	0
10	ISOLATE	1 = Electrically isolate PHY from MII 0 = Normal operation	RW	0
9	RESTART_ AUTONEGOTIATION	1 = restart auto-negotiation process 0 = normal operation	RW/SC	0
8	DUPLEX_MODE	1 = Full duplex 0 = Half Duplex This bit is ignored if auto-negotiation is enabled (0.12=1).	RW	Strap option
7	COLLISION_TEST	1 = enable COL signal test 0 = disable COL signal test	RW	0
6:0	RESERVED	Write as 0, ignore on Read	RO	0

Writing to Register PHY.0 in order to change modes from 10BT to 100BT and vice versa (Autonegotiation disabled), will take approximately 2us. Mode changes from HD to FD and vice versa is instantaneous.

5.6.2 Register PHY.1 - Basic Control

Bit	Name	Description	Mode	Default
15	100BASE_T4	1 = 100BASE-T4 able 0 = no 100BASE-T4 ability	RO	0
14	100BASE_TX_ FULL_DUPLEX	1 = 100BASE-TX ability with full duplex 0 = no 100BASE-TX full duplex ability	RO	1
13	100BASE_TX_ HALF_DUPLEX	1 = 100BASE-TX ability with half duplex 0 = no 100BASE-TX half duplex ability	RO	1
12	10MB_FULL_ DUPLEX	1 = 10Mb/s ability with full duplex 0 = no 10M b/s full duplex ability	RO	1
11	10MB_HALF_ DUPLEX	1 = 10Mb/s ability with half duplex 0 = no 10Mb/s half duplex ability	RO	1
10:6	RESERVED	Ignore on read	RO	0
5	AUTO-NEGOTIATION COMPLETE	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	RO	0
4	REMOTE FAULT	1 = remote fault condition detected 0 = no remote fault condition detected	RO/LH	0
3	AUTO-NEGOTIATION ABILITY	1 = able to perform auto-negotiation 0 = unable to perform auto-negotiation	RO	1
2	LINK STATUS	1 = link is up 0 = link is down	RO/LL	0
1	JABBER DETECT	1 = jabber condition detected 0 = no jabber condition detected	RO/LH	0
0	EXTENDED CAPABILITY	1 = extended register capabilities 0 = basic register set capabilities only	RO	1

5.6.3 Register PHY.2 - PHY Identifier

Bit	Name	Description	Mode	Default
15:0	PHY ID NUMBER	Assign to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI)	RO	0xb824

5.6.4 Register PHY.3 - PHY Identifier

Bit	Name	Description	Mode	Default
15:10	PHY ID NUMBER	Assigned to the 19th through 24th bits of the OUI	RO	0x0a
9:4	MODEL NUMBER	Manufacturer's model number	RO	0x2
3:0	REVISION NUMBER	Manufacturer's revision number	RO	0x4

5.6.5 Register PHY.4 - Auto-Negotiation Advertisement

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = next page capable 0 = no next page ability	RW	0
14	RESERVED	Write as "0", Ignore on read	RO	0
13	REMOTE FAULT	1 = remote fault detected 0 = no remote fault detected	RW	0
12	RESERVED	Write as "0", ignore on read	RW	0
11:10	PAUSE OPERATION	00 = no PAUSE 01 = asymmetric PAUSE toward link partner 10 = Symmetric PAUSE 11 = both symmetric PAUSE and asymmetric PAUSE toward local device	RW	00
9	100BASE-T4	1 = 100BASE-T4 capable 0 = no 100BASE-T4 ability This PHY does not support 100BASE-T4	RO	0
8	100BASE-TX FULL DUPLEX	1 = 100BASE-TX full duplex able 0 = no 100BASE-Tx ability	RW	1
7	100BASE-TX	1 = 100BASE-TX able 0 = no 100BASE-TX ability	RW	1
6	10BASE-T FULL DUPLEX	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RW	1
5	10BASE-T	1 = 10Mbps able 0 = no 10Mbps ability	RW	1
4:0	SELECTOR FIELD	00001 : IEEE Std. 802.3	RW	00001

5.6.6 Register PHY.5 - Auto-Negotiation Link Partner Ability (Base Page)

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = additional next page will follow 0 = last page	RO	0
14	ACKNOWLEDGE	1 = successfully received link partner's link code word 0 = not successfully received link partner's link code word	RO	0
13	REMOTE FAULT	1 = remote fault condition 0 = no remote fault condition	RO	0
12:11	RESERVED	Ignore on read	RO	0
10	PAUSE OPERATION	1 = pause operation is supported by remote MAC 0 = pause operation is not supported by remote MAC	RO	0
9	100BASE-T4	1 = 100BASE-T4 able 0 = no 100BASE-T4 ability	RO	0
8	100BASE-TX FULL DUPLEX	1 = 100BASE-TX with full duplex 0 = no 100BASE-TX full duplex ability	RO	0
7	100BASE-TX	1 = 100BASE-TX able 0 = no 100BASE-TX ability	RO	0
6	10BASE-T FULL DUPLEX	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RO	0
5	10BASE-T	1 = 10Mbps able 0 = no 10Mbps ability	RO	0
4:0	SELECTOR FIELD	00001 : IEEE Std. 802.3	RO	00001

5.6.7 Register PHY.5 - Auto-Negotiation Link Partner Ability (Next Page)

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = additional next page will follow 0 = last page	RO	0
14	ACKNOWLEDGE	1 = successfully received link partner's link code word 0 = not successfully received link partner's link code word	RO	0
13	MESSAGE PAGE	0 = unformatted page 1 = message page	RO	0
12	ACKNOWLEDGE 2	0 = cannot comply with message 1 = will comply with message	RO	0
11	TOGGLE	0 = previous value of the transmitted link code word equaled logic one. 1 = previous value of the transmitted link code word equaled logic zero.	RO	0
10:0	MESSAGE/ UNFORMAT TED CODE FIELD	11 bit code word received from link partner	RO	All 0

5.6.8 Register PHY.6 - Auto-Negotiation Expansion

Bit	Name	Description	Mode	Default
15:5	RESERVED	Ignore on read	RO	0
4	PARALLEL DETECTION FAULT	1 = fault has been detected 0 = no fault has been detected	RO/LH	0
3	LINK PARTNER NEXT PAGE ABLE	1 = link partner is next page able 0 = link partner is not next page able	RO	0
2	NEXT PAGE ABLE	1 =local device is next page able 0 = local device is not next page able	RO	1
1	PAGE RECEIVED	1 = a new page has been received 0 = a new page has not been received	RO/LH	0
0	LINK PARTNER AUTO-NEGOTIATION ABLE	1 = link partner is auto-negotiation able 0 = link partner is not auto-negotiation able	RO	0

5.6.9 Register PHY.7 - Auto-Negotiation Next Page Transmit

Bit	Name	Description	Mode	Default
15	NEXT PAGE	1 = next page exists 0 = next page does not exist	RW	0
14	RESERVED	Write as “0”, ignore on read	RO	0
13	MESSAGE PAGE	1 = message page 0 = unformatted page	RW	1
12	ACKNOWLEDGE2	0 = cannot comply with message 1 = will comply with message	RW	0
11	TOGGLE	1 = previous value equaled logic zero 0 = previous value equaled logic one	RO	0
10:0	MESSAGE/ UNFORMATTED CODE	11 bit code word to be transmitted to link partner	RW	0x001

5.6.10 Register PHY.16 - Silicon Revision

Bit	Name	Description	Mode	Default
15:10	RESERVED	Ignore on read	RO	0
9:6	SILICON REVISION	Four bit silicon revision identifier	RO	0001
5:0	RESERVED	Ignore on read	RO	0

5.6.11 Register PHY.17 - Mode Control/Status

Bit	Name	Description	Mode	Default
15	RESERVED	Write as 0; ignore on read.	RW	0
14	FASTRIP	10BASE-T fast mode: 0 = normal operation 1 = activates PHYT_10 test mode Note: this bit can be used for simulation	RW, NASR	0
13	EDPWRDOWN	Enable the energy detect power-down mode: 0 = energy detect power-down is disabled 1 = energy detect power-down is enabled	RW	0
12	RESERVED	Write as 0; ignore on read.	RW	0
11	LOWSQEN	Low squelch signal 0 = imply a higher threshold (less sensitive) 1 = imply a lower threshold (more sensitive)	RW	0
10	RESERVED	Write as 0; ignore on read.	RW	0
9	FARLOOP BACK	Remote loopback enable All the received packets are sent back simultaneously (in 100BASE-TX/FX only).	RW	0
8	FASTEST	Auto-negotiation test mode 0 = normal operation 1 = activates test mode Note: This bit can be used for simulation. In this mode, expanded time of S/W reset becomes shorter,too.	RW	0
7	AUTOMDIX_EN	AutoMDIX enable bit 1 = Auto-detect MDI/MDIX mode 0 = Manual set of MDI/MDIX mode According to bit MDI mode (Register PHY.17.6). AutoMDIX is disabled in FX Mode.	RW	Strap option
6	MDI MODE	MDI/MDIX mode control/status 1 = MDIX mode 0 = MDI mode When AutoMDIX_en (17.7) is disabled, this bit is used for manual control of MDI/MDIX mode. If AutoMDIX_en (Bit 17.7) is enabled it shows the status and	RW	0

		will not be written to		
5	RESERVED	Write as 0, ignore on read	RW	0
4	DCD_PAT_GEN	When in test mode, 1 = Enables DCD measuring pattern generation	RW	0
3	RESERVED	Write as 0, ignore on read	RW	0
2	FORCE GOOD LINK STATUS	1 = Force 100BASE-X link active 0 = normal operation Note: this bit should be set only testing	RW	0
1	ENERGYON	Indicates whether energy is detected on the line. If no valid energy is detected within 256ms, this bit goes to 0.	RO	0
0	RESERVED	Write as 0, ignore on read	RW	0

5.6.12 Register PHY.18 - Special Modes

Bit	Name	Description	Mode	Default
15:11	Reserved	Write as 0, ignore on read	RW NASR	0
10	FX_MODE	Enable 100BASE-FX mode 1 = FX mode enable When PHYMODE should be set to “0011” or “0010” only.	RW NASR	Strap option
9:	Reserved	Write as “0”. Ignore on read	RW	0
8:5	PHYMODE	PHY mode of operation. Is set according to strap pin setting after reset. 0000: 10BT, HD, no autonegotiation 0001: 10BT, FD, no autonegotiation 0010: 100BT, HD, no autonegotiation 0011: 100BT, FD, no autonegotiation 0100: 100BT, HD advertised, autonegotiation 0101: 100BT, HD advertised, autonegotiation 0110: Reserved 0111: All speeds, FD or HD, Autoneg enabled 1000: All speeds, Forced Full duplex, 1100: All speeds, HD in parallel detect, 1111: Loopback	RW NASR	Indirect Strap option
4:3	PHY_ADD_DEV	PHY address upper two bits The PHY address is used to address the whole device and for the initialization of the Cipher (Scrambler) key.	RW NASR	Strap option
2:0	PHY_ADD_MOD	PHY address lower three bits The PHY address is used to address the PHY and for the initialization of the Cipher (Scrambler) key.	RW NASR	000

5.6.13 Register PHY.19 - Elastic Buffer Status register (Loopback Mode only)

Bit	Name	Description	Mode	Default
15:8	reserved	Ignore on read	RO	0

7	T_EL_BUF_OVF	Transmitter elastic overflow	RO/LH	0
6	T_EL_BUF_UDF	Transmitter elastic underflow	RO/LH	0
5	R_EL_BUF_OVF	Receiver elastic overflow	RO/LH	0
4	R_EL_BUF_UDF	Receiver elastic underflow	RO/LH	0
3:0	reserved	Ignore on read	RO	0

5.6.14 Register PHY.20 – Reserved

Bit	Name	Description	Mode	Default
15:0	Reserved	Ignore on read	RW	0

5.6.15 Register PHY.21 – Reserved

Bit	Name	Description	Mode	Default
15:0	Reserved	Ignore on read	RO	0

5.6.16 Register PHY.22 – Reserved (TSTREAD2 / TSTWRT)

Bit	Name	Description	Mode	Default
15:0	Reserved	Ignore on read	RW	0

5.6.17 Register PHY.23 – BER Counter

Bit	Name	Description	Mode	Default
15	BER_LNK_OK	Link quality indication – indicates state of link monitor FSM. '0' – FSM is not in 'Good Link' state '1' – indicates FSM in 'Good Link' state Will go high as soon as the counter is below the trigger level after start up. Can be used to detect reliably link up after start up.	RO	0
14	BER_CNT_ LNK_EN	1: A trigger on the BER or on the FEQ monitor will cause a link down 0: A trigger on the BER/FEQ will just cause the state machine to leave “Good Link” state.	RW	1
13:11	BER_CNT_TRIG	Trigger level for BER Count to define link up/down counter in 1 * 2^(n -1) errors 0: >0 errors will trigger 1: >1 error will trigger 2: >2 errors will trigger 3: >4 errors will trigger 4: >8 errors will trigger 5: >16 errors will trigger 6: >32 errors will trigger 7: >64 errors will trigger	RW	2
10:7	BER_WINDOW	Length of time for BER Counter in 0.005 * 2^n ms 0: BER Counter functions disabled 1: 0.01 ms 2: 0.02 ms 3: 0.04 ms ….. 14 : 81.92 ms 15: unlimited run Writing a 0 resets the BER counter and restarts the time window.	RW	1 (0.01 ms)
6:0	BER-COUNT	Counter for bit errors, shows the amount of errors in the past time window or every 100 µs if BER_WINDOW = 15. Writing 00 resets the BER counter and restarts the time window.	RO	0x0

5.6.18 Register PHY.24 – FEQ monitor Register

Bit	Name	Description	Mode	Default
15:0	FEQ_DELTA	Minimum change of value compared to the reference value latched when the monitor is enabled, which will trigger the FEQ interrupt and link down. If the FEQ value differs by more than that value, the link goes down, if the BER_CNT_LNK_EN is 1 and the BER Monitor is enabled, The interrupt is triggered if enabled. 'FFFF' – will disable monitor and cause the reference value to be relatched continuously 'FFFE' – will not change the FEQ_DELTA value but enable to read out the current reference value, when FEQ_VAL is read, instead of the current value. Writing any other value will disable this mode.	W	0xFFFF
15:0	FEQ_VAL	If FEQ_DELTA == FFFE Bit 17:2 of the reference value. Else Bits 17:2 of the current FEQ2 coefficient.	RO	

5.6.19 Register PHY.25 – Diagnosis Control/Status Register

Bit	Name	Description	Mode	Default
15	Reserved	Write with 0; ignore on read	RW	0
14	DIAG_INIT	When set to '1' , create one cycle pulse - init TDR test	RW (self cleared)	0
13:8	ADC_MAX_ VALUE	Shows the signed maximum/minimum value of the reflected wave. After the TDR process has been started the PHY will send out a trigger pulse and wait for the reflected wave for 255 clock cycles of 8 ns. After the time has elapsed the DIAG_DONE bit is set. The ADC MAX_VALUE will indicate the maximum of the received wave if positive or the minimum if negative.	R	0
13:8	ADC_Trigger	Threshold for pulse detection. – should be 0.5V / 00111 for cable length detection or 1.5V / 01111 for no cable detection. MSB should always be 0.	W	0
7	DIAG_DONE	Indicates that the counter has been stopped either by counter overrun or by a ADC trigger. Cleared after reading	RO	0
6	DIAG_POL	0: Counter stopped by positive trigger level 1: Counter stopped by negative trigger level	RO	0
5	DIAG_SEL_LINE	1: perform diagnosis on TX line 0: perform diagnosis on RX line	RW	0
4:0	PW_DIAG	Pulse width for Diagnosis 0: Diagnosis turned off Other: Pulse width = value*8ns	RW	0

5.6.20 Register PHY.26 – Diagnosis Counter Register

Bit	Name	Description	Mode	Default
15:8	CNT_WINDOW	Minimum time after which the counter stops. Used to filter out any pulses or reflections generated from the local connector or similar sources. One tick equals approximately 0.8m	RW	0
7:0	DIAGCNT	Indicates the location of the received signal which exceeded the threshold ; When DIAG_INIT is set to '1' - initiated by HW to '000000' . '1111111' – indicates no reflection. Any value different from zero indicates a valid measurement. When no cable is present, the value will be '000001' (assuming threshold is set to the correct value). One counter tick equals approximately 0.8 m	RO	0

5.6.21 Register PHY.27 - Special Control/Status Indications

Bit	Name	Description	Mode	Default
15:13	Reserved	Write as “000”. Ignore on read	RW	0
12	SWRST_FAST	SW reset counter testing 1 = accelerates SW reset counter from 256us to 10 us for production testing.	RW	0
11	SQEOFF	Disable the SQE test(Heartbeat) 1 = SQE test is disabled 0 = SQE test is enabled. Set ‘1’ when repeater mode	RW NASR	0
10:6	Reserved	Write as 0, ignore on read.	RW	0
5	FEFIEN	Far End fault indication enable 1 = FEFI generation and detection are enabled 0 = FEFI generation and detection are disabled (default when FXMODE configuration input is High during reset)	RW	Strap option
4	XPOL	Polarity state of the 10BASE-T 1 = Reversed polarity 0 = normal polarity	RO	0
3:0	Reserved	Ignore on read.	RO	0001

5.6.22 Register PHY.28 - Reserved

Do not write or read this register

5.6.23 Register PHY.29 - Interrupt Source Flags

Bit	Name	Description	Mode	Default
15:11	Reserved	Ignore on Read		0
10	INT10	BER counter trigger	RO	0
9	INT9	FEQ trigger	RO	0
8	Reserved	Ignore on read	RO	0
7	INT7	1 = ENERGYON generated	RO	0
6	INT6	1 = auto-negotiation complete	RO	0
5	INT5	1 = remote fault detected	RO	0
4	INT4	1 = link down	RO	0
3	INT3	1 = auto-negotiation Last Page acknowledge	RO	0
2	INT2	1 = parallel detection fault	RO	0
1	INT1	1 = auto-negotiation page received	RO	0
0	Reserved		RO	0

5.6.24 Register PHY.30 - Interrupt Enable

Bit	Name	Description	Mode	Default
15.11	Reserved	Write as 0, Ignore on read	RO	0
10:9	Mask Bits	1 = interrupt source is enabled 0 = interrupt source is masked	RW	0
8	Reserved	Write as 0, Ignore on read	RO	0
7:0	Mask Bits	1 = interrupt source is enabled 0 = interrupt source is masked	RW	0

5.6.25 Register PHY.31 - PHY Special Control/Status

Bit	Name	Description	Mode	Default
15:14	Reserved	Write as 0. ignore on read.	RW	0
13	Reserved	Write as 0. ignore on read.	RW	0
12	AUTODONE	Auto-negotiation done indication 1 = auto-negotiation is done 0 = auto-negotiation is not done or disabled (or not active)	RO	0
11:7	Reserved	Write as “00000”. Ignore on read	RW	0
6	ENABLE 4B5B MII MODE	1 = Enable 4B/5B Encoding/Decoding. MAC interface must be configured in 0 = Bypass encoder/decoder	RW	1
5	Reserved	Write as 0, ignore on Read.	RW	0
4:2	SPEED INDICATION	HCDSPEED value: 001 = 10Mbps half-duplex 101 = 10Mbps full-duplex 010 = 100BASE-TX half-duplex 110 = 100BASE-TX full-duplex	RO	000
1	RX_DV_J2T	’0’ – rx_dv rises on “JK” delimiter falls on “TR” delimiter ‘1’ – J_ONLY_MODE, rx_dv rises on “J” delimiter falls on “T” delimiter	RW	0
0	SCRAMBLE DISABLE	1 = disable data scrambling 0 = enable data scrambling	RW	0

External Components

6.1 Clock

The devices can be operated on an external 25 MHz clock in MII mode or an external 50 MHz clock in RMII mode. In addition for MII mode it contains an internal oscillator which may generate the required 25 MHz clock using an external 25 MHz crystal connected to the pins XCLK0 and XCLK1.

6.2 Internal Switching Regulator

The device contains an internal switching regulator which generates the internal 1.6V for the PHY from the external 3.3V power supply. It can be disabled by tying REGOF to 3.3V and connecting the pins mentioned below directly to a 1.6V power supply. Otherwise the REGOFF pin must be connected to GND.

Pin name	Pin number	Description
VDD15	30, 52	1.5V Digital VDD
VDDAPLL	11	Analog 1.5V power supply for PLL
P1VDDMEDIA, P0VDDMEDIA	3, 19	Analog 1.5V power supply for PHY

6.2.1 Power-Up Sequence

In case the internal voltage regulator is not used and the 1.5V supply is supplied form an external source a special power up sequence is not required. However both power supplies must be stable within 100ms.

Support of IEEE1588 (uPD60621A only)

Renesas Electronics' Ethernet PHY implements the precision time protocol (PTP) according to IEEE1588 to support the requirements of higher precision and faster production.

The PHY supports IEEE1588 V1 and V2 including transparent clock mode and one-step or two-step mode. Furthermore the PHY can timestamp incoming messages with a resolution of 1ns.

The following clock modes are supported:

- Ordinary clock
- Boundary clock
- Transparent clock

The PHY can timestamp events on any of the GPIO pins. Based on the internal synchronized clock it may generate up to three output signals which may generate single pulses or repetitive pulses with programmable pulse length. It is also possible to output a Pulse-Per-Second (PPS) signal. Resolution for the event time-stamping unit and the pulse generation unit is 8ns. Reception of a PTP message, transmission of a PTP message, an event on the event unit and the pulse generator can generate an interrupt.

7.1 IEEE1588

The basic purpose of IEEE1588 is to synchronize clocks in different nodes and have them run at the same phase and frequency. One clock in a node is selected as the master clock and all other clocks (called "slave clocks") in the system are synchronized to the master clock. Special PTP frames are exchanged between the nodes to distribute the time value of the master clock and measure the travel times. Based on the master clock time value and the travel times of the slave clocks can be adjusted and synchronized.

To measure the travel time, timestamps can be taken when frames leave the PHY or when they are received by the PHY. The more precise these timestamps, the more precise the calculations of the travel times are, and the better the synchronization of the clocks. For the transmit frames the data is always sent at the clock edge of the 125 MHz clock and therefore the time-stamping logic, which is running at the same clock as the transmit logic, has an optimal accuracy. However, receive frames can arrive at any time within the 125MHz/8ns clock period so the receive time-stamping logic has an error of up to 8ns depending on the actual arrival time of the data within the clock period.

To optimize the reception of the incoming data, the receive DSP continuously shifts the time at which the data is sampled. This is done by using one of the phases of the 125MHz clock from the PLL. Thus the selected phase of the PLL is a precise indicator for the exact sampling time at which the incoming data arrived at the PHY. As each of these phases represents a 1ns timeslot it can be used to define the exact arrival time within the 8ns clock period. This data is also stored together with the timestamp.

There are two ways in which timestamps can be transmitted between the nodes. One way is called “One Step”. In this mode the timestamps for transmit frames are directly embedded in the telegram itself.. This approach reduces the software overhead at the expense of increased latency. The other method is called a “Two Step” approach. In this mode the timestamps are taken at the time of transmit, but sent afterward in a “follow up” telegram. This method provides lower latency but generates more traffic and requires more software overhead.

7.2 Register access to PTP

Many registers within the PTP block are 80 bits or 48 bits wide to control the whole width of the time representation. To read or write these registers they must be accessed 5 times (5 * 16 bits = 80 bits) or 3 times for the 48 bit wide registers in a row. Unless otherwise noted accesses are done with the least significant word (bits 15:0) first. The values are latched internally after the last value has been written.

7.3 1588 Clock Control

The clock keeps the time which is to be synchronized between the different nodes and it can bedirectly set, accelerated, decelerated, or adjusted over a defined period.

The accessible clock is 80 bits wide with the upper 48 bits counting the seconds and the lower 32 bit counting the nanoseconds. Thus the ns clock overflow is not at 0xFFFFFFFF but at 10^9 ns (0x3B9ACA00). Internally, the clock also maintains 30 extra bits of sub-nanosecond resolution to handle drift correction.

As the clock is running at 125 MHz, the clock value is increased by 8ns with every clock cycle. This value can be adjusted to speed up or slow down the clock. So, although the clock is still incremented based on the 125 MHz clock, it can be fine-tuned so that the value reflects real time.

To access the clock, read the register five times to retrieve 16 bits each time.

7.3.1 CLOCK_STATUS Register 6.0

Bit	Name	Description	Mode	Default
14	EN_OFFSET_CORR	1: Enable offset correction 0: Disable offset correction Automatically cleared after the offset correction is finished.	RW	0
13	OFFSET_RUN	1: offset correction in process 0: offset correction done	R	0
12	EN_DRIFT_CORR	1: enable drift correction 0: disable drift correction	R/W	0
11:9	CLOCK_READ_POS	Value of pointer pointing to the CLOCK_READ register. If 0 next read is from least significant word of clock latch.	R	0
8:6	CLOCK_WRITE_POS	Value of pointer pointing to the CLOCK_WRITE register. If 0 next write goes toleast significant word of clock latch.	R	0
5:3	OFFSET_WRITE_POS	Value of pointer pointing to the CLOCK_OFFSET register. If 0 next write goes toleast significant word off offset latch.	R	0
2:0	DRIFT_WRITE_POS	Value of pointer pointing to the CLOCK_DRIFT register. If 0 next write goes toleast significant word off offset latch.	R	0

7.3.2 CLOCK_READ Register 6.1

The CLOCK_READ register is used to read the actual value of the clock. It must be accessed five consecutive times to read the complete data. Any read to another register will reset the internal pointer and the next read will then again read the highest word. All accesses are done with the most significant word first.

Bit	Name	Description	Mode	Default
79:0	CLOCK_READ	Clock read register.	R	0

7.3.3 CLOCK_WRITE Register 6.2

This register can be used to set the clock to a value. It must be written five consecutive times. The data is latched into the clock when the 5th word is written. All accesses are done with the most significant word first.

Bits	Name	Description	Mode	Default
79:0	CLOCK_WRITE	Clock write register	W	

7.3.4 CLOCK_OFFSET Register 6.3

This register is used to adjust the clock to a new value. To avoid sudden jumps the offset is not added all at once; instead the “OFFSET” is added/subtracted to the clock value after “OFFSET_INTERVAL” for “OFFSET_COR_COUNT” times. Thus the clock is slowly adjusted to the new value value and jumps are avoided.

All values are latched internally when the offset correction is stopped either when it is finished or if it is manually disabled and reenabled with the EN_OFFSET_CORR register bit.

Bit	Name	Description	Mode	Default
47	OFFSET_SIGN	Sign, 1: Subtract offset 0: Add offset	W	0
46:44	OFFSET	Increase value in ns	W	0
43	Reserved	Write as 0	W	0
42:32	OFFSET_INTERVAL	Interval in steps 0: No interval 1: No interval 2: add every 2nd step 3: add every 3rd step …	W	0
29:0	OFFSET_COR_COUNT	Count, how often the “step” value is added	W	0

7.3.5 CLOCK_DRIFT Register 6.4

This register contains a correction value, which can be used to continuously correct the clock value to compensate for oscillator drift. The value in the DELTA_VAL register is summed up every clock cycle (125MHz), as soon as the sum has exceeded 0x3fffffff a value of 1 an additional ns is depending on the DELTA_SIGN bit added/subtracted from the clock value. This register is latched internally when the EN_DRIFT_CORR register bit is set.

The value for the DELTA_VAL register is calculated based on the following formula:

$$DELTA\_VAL = \frac{drift \cdot 10^3 \cdot 2^{30}}{125[MHz] \Big/ (1 \pm drift)}$$

$$where:$$

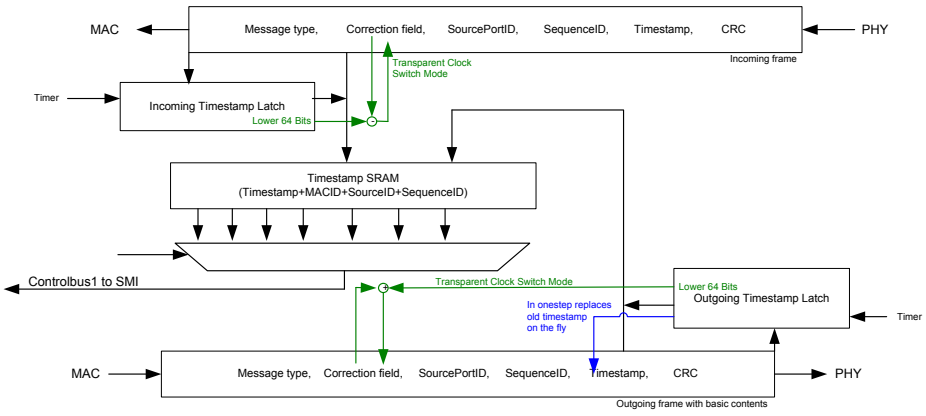
$$drift[s/s] is\ correction\ value\ for\ clock$$

$$\pm : use + when\ DELTA\_SIGN = 1, use - when\ DELTA\_SIGN = 0$$

Bit	Name	Description	Mode	Default
31	DELTA_SIGN	Sign of the delta value. 1: Clock is slowed down 0: Clock is speeded up	RW	0
30	Reserved	Ignore on read, write as 0	RW	0
29:0	DELTA_VAL	Delta in fractions of ns, by which the increment value is corrected. So bit 29 represents ½ ns, bit 28 1/4th ns, bit 27 1/8th ns, etc.	RW	0

7.4 Frame Handling Unit

The following picture shows the block diagram for the frame handling unit. The incoming telegram is time stamped as it arrives and the timestamp is then stored together with other related information in the timestamp SRAM. This data enables software to handle two-step PTP. When an event happens -- either due to transmission or reception of a PTP message -- an interrupt can be generated.



7.4.1 One step mode

For one-step PTP the timestamp is stored in the outgoing timestamp latch and is then integrated into the timestamp field of the frame before it is sent. The CRC is also corrected accordingly. Note that for one-step mode the latency through the PHY is increased as the insertion of the time stamp in the frame requires some processing of the frame.

7.4.2 Two step mode

For two-step PTP the timestamp of the Synch telegram is stored in the outgoing timestamp latch and is not integrated into the timestamp field of the frame before it is sent. It then needs to be read by software and is transmitted to the receiver in a separate FollowUp telegram.

7.4.3 Transparent Clock Mode

Transparent Clock is used to improve the accuracy of the time synchronization in long networks by eliminating the uncertainty it takes for synch telegrams to pass through switches. Depending on the load of the switch the residence time of a synch telegram in the switch varies. By measuring the time a synch frame stays in the switch and writing this value into the frame the accuracy is greatly improved as the slave clock can use this value to adjust its calculation of the master clock value.

To support Transparent Clock mode in hardware the PHY modifies the respective telegrams. When a PTP synch telegram is received in transparent clock mode, the lower 2(sec)+32(ns) bits of the timestamp value taken at reception are converted to ns and subtracted from the correction field. When a PTP telegram is sent, the transmit timestamp lower 2(sec)+32 (ns) bits are converted to ns and added to the correction field. Thus the correction field is incremented by the difference between transmit and reception time and the correction field correctly updated even if a telegram is received on one PHY and transmitted on the other. This handling can be enabled separately for each PHY and for transmit and receive.

The Transparent Clock function can only be used in one step mode. In two step mode the Transparent Clock function is not required but can be handled by using one of the Ordinary Clock modes for time stamping and handling the protocol in software based on the FollowUp telegrams. However even if the system typically uses two step mode it is still possible to use the one step mode setting.

For End to End Transparent clock the time a synch telegram takes to pass through the node is measured and either stored in the correction field of the telegram or the correction field of the FollowUp telegram. The correction field at the slave then contains the time that the telegram spend in the different switches etc. which act as a transparent clock. The PTP stack can use this value to calculate the raw line delay and eliminate the jitter that comes from the varying residence times in the switchesPeer to Peer Transparent Clock

For peer-to-peer transparent clock each node measures the delay to all surrounding nodes using the PdelayReq and Pdelay_Resp mechanism. Thus all line delays in a network are known. Each node through which a Synch message passes adds the own residence time plus the line delay of the incoming link to the correction field. When this synch telegram arrives at the slave node it contains the complete line delay plus the residence times in its correction field except for the very last link. The delay on the last link is known to the slave and

thus the complete line delay is known. Although this method is more complex than the End to end transparent clock it offers much faster reconfiguration in case of line breaks.

7.4.4 Timestamp Status Register 6.6

The Timestamp Status register shows the status for each buffer:

Bit	Name	Description	Mode	Default
15:12	Reserved write as 0, ignore on read		RW	
11	BUF_EMPTY_TX_PHY1	Buffer empty for TX bufferPHY1	RW	0
10	BUF_EMPTY_RX_PHY1	Buffer empty for RX buffer PHY1	RW	0
9	BUF_EMPTY_TX_PHY0	Buffer empty for TX buffer PHY0	RW	0
8	BUF_EMPTY_RX_PHY0	Buffer empty for RX buffer PHY0	RW	0
7:4	Reserved write as 0, ignore on read		RW	
3	OVERFLOW_BUF_TX_PHY1	Buffer overflow for TX buffer PHY1	RW	0
2	OVERFLOW_BUF_RX_PHY1	Buffer overflow for RX buffer PHY1	RW	0
1	OVERFLOW_BUF_TX_PHY0	Buffer overflow for TX buffer PHY0	RW	0
0	OVERFLOW_BUF_RX_PHY0	Buffer overflow for RX buffer PHY0	RW	0

7.4.5 Timestamp Config Register 6.7

The Timestamp Configuration register is used to configure the framer unit and is used to select which register of the timestamp memory is read.

Bit	Name	Description	Mode	Default
15:8		Reserved, write as 0, ignore on read	RW	0
7	DISREGARD_OLDEST_TIMESTAMP	0: Do not overwrite timestamp if buffer overruns / newest timestamp is lost 1: Overwrite oldest timestamp if buffer overruns / oldest timestamp is lost	RW	0
6:4	TIMESTAMP_SELECT	Address at which timestamp buffer is read for the following access to the TIMESTAMP_LINE_EVENT register. 001: Next read will get TX timestamp on PHY0 000: Next read will get RX timestamp on PHY0 011: Next read will get TX timestamp on PHY1 010: Next read will get RX timestamp on PHY1 Others: Undefined	RW	0
3:2		Reserved, ignore on read, write as 0	RW	
1	TS_EN_PHY1	Enable timestamping for PHY1	RW	0
0	TS_EN_PHY0	Enable timestamping for PHY0	RW	0

7.4.1 TIMESTAMP_LINE_EVENT Register 6.8

The TIMESTAMP_LINE_EVENT register gives access to the timestamp memory which stores the time stamps generated by the framer logic when a PTP frame was transmitted or received. It stores transmit or receive timestamps separately for TX and RX frames. The TIMESTAMP_SELECT bits in the TIMESTAMP_CONGIGURATION register define if the TX or the RX buffer is accessed. The timestamp memory can hold up to four timestamps for RX and four timestamps for TX, A read will always retrieve the oldest valid dataset.

A timestamp set is combined of the timestamp itself, the source port identity and the sequence ID stored in a 192 bit wide register. This is organized as shown below:

Bit	Name	Description	Mode	Default
191:176	MESSAGE_ID	Message Type of the received message 001: PTP Sync message 010: PDelayReq message 011: PDelayResp message 100 : Delay Req. message	RO	Undefined
175:96	TIMESTAMP	Timestamp of the related event described in bits 95:0. Bits 175:128: seconds Pits 127:96: ns	RO	Undefined
95:16	SOURCEPORTIDENTITY	sourcePortIdentity extracted from the PTP telegram . If TS_ALL_FRAMES_nn is set and a NonPTPFrame is received this field is empty.	RO	Undefined
15:0	SEQUENCE_ID	Rolling number assigned by sending port and extracted from telegram. If TS_ALL_FRAMES is set, and also normal non-PTP telegrams are timestamped there may be no SEQUENCE_ID in the telegram, thus the SEQUENCE_ID is generated internally starting with 0.	RO	Undefined

To read a data set the timestamp memory register has to be accessed 12 times. The least significant word is read first. The TIMESTAMP_SELECT register must be written prior to each individual access to the timestamp memory register.

7.4.2 PTP_CONFIG_n Register 6.9 / 6.13

The PTP Config register is used to configure the framer unit. There is one PTP config register for each PHY. The config register for PHY 0 is located at address 6.9, for PHY1 at 6.13.

Bit	Name	Description	Mode	Default
15:12		Reserved, ignore on read, write as 0	RW	
11	TS_ALL_ FRAMES_RX	1: Enable timestamping for all received frames. The IPV4 and IPV6 filter bits are still used. 0: Disable timestamping for all received frames	RW	0
10	TS_ALL_ FRAMES_TX	1: Enable timestamping for all transmitted frames. The IPV4 and IPV6 filter bits are still used. 0: Disable timestamping for all transmitted frames.	RW	0
9	L2	1: Timestamp all Layer 2 frames 0: Do not timestamp layer 2 frames	RW	0
8	IPV4	1: Timestamp frames containing IPV4 frames 0: Do not timestamp IPV4 frames	RW	0
7	IPV6	1: Timestamp frames containing IPV6 frames 0: Do not timestamp IPV6 frames	RW	0
6	ONE_STEP	1: Enable one step mode for the PHY. In this mode the taken transmit timestamp is integrated in the frame on the fly and the CRC corrected. 0: Selct two step mode, the transmit timestamp is not integrated in the outgoing frame.	RW	0
5:4	P2P_DELAY_ WRITE_POS	Current position of the PORT_DELAY_PHY_n register	R	0
3:2	MODE_TX	Set the PTP mode for TX 00: BC_PTP_V1 (boundary clock mode) 01: BC_PTP_V2 (boundary clock mode) 10: TC_E2E_PTP_V2 (transparent clock end-to-end mode) 11: TC_P2P_PTP_V2	RW	1

		(transparent clock peer-to-peer mode)		
1:0	MODE_RX	Set the PTP mode for RX 00: BC_PTP_V1 (boundary clock mode) 01: BC_PTP_V2 (boundary clock mode) 10: TC_E2E_PTP_V2 (transparent clock endto-end mode) 11: TC_P2P_PTP_V2 (transparent clock peer-to-peer mode)	RW	0

The following table gives an overview on how the different telegram types are handled depending on the configuration. An empty field means that nothing is done.

TX Path:

Frame type	**OC/BC V1 One Step**	**OC/BC V1 Two Step**	**OC/BC V2 E2E/P2P One Step**	**OC/BC V2 E2E/P2P Two Step**	**TC E2E One Step**	**TC P2P One Step**
Sync	Store TS	Copy TS to TS field	Copy TS to TS field	Store TS	Add TS to Cor. field	Add TS to Cor. field
FollowUp	-	-				
DelayReq	Store TS	Store TS	Store TS	Store TS	Add TS to Cor. field	
DelayResp	-	-				
PeerDelayReq	-	-	Store TS	Store TS	Add TS to Cor. field	Store TS
PeerDelayResp	-	-	Add TS to TS field	Store TS	Add TS to Cor. field	Add TS to Cor. field
PeerDelayResp FollowUp	-	-				

RX Path:

Frame type	OC/BC V1 One Step	OC/BC V1 Two Step	OC/BC V2 E2E/P2P One Step	OC/BC V2 E2E/P2P Two Step	TC E2E One Step	TC P2P One Step
Sync	Store TS	Store TS	Store TS	Store TS	Sub TS from Cor. field, Store TS	Sub TS from Cor. Field Store TS
FollowUp	-	-				
DelayReq	Store TS	Store TS	Store TS	Store TS	Sub TS from Cor. field,	
DelayResp	-	-				
PeerDelayReq	-	-	Sub TS from Cor. field	Store TS	Sub TS from Cor. field,	Sub TS from Cor. field
PeerDelayResp	-	-	Store TS	Store TS	Sub TS from Cor. field	Store TS
PeerDelayResp FollowUp	-	-				

7.4.3 PHY_DELAY_TX_n Register 6.11 / 6.15

The PORT_DELAY_PORT_n register is used to adjust the timestamp by the latency of the PHY's TX path. This is by default set to 0 but may be corrected to also compensate for delays caused be the transformer. There is one register for each PHY. PTP assumes that the line delay including the PHY latency in both directions is identical, this may not be the case if PHYs from different vendors are used in a network. In this case the PHY_DELAY_TX_PORT and PHY_DELAY_RX_PORT values should be set. This value should be set to 40.

Bit	Name	Description	Mode	Default
15:0	PHY_DELAY_ TX_PORT_n	Value in ns by which timestamps taken for the PHYn on the TX side are corrected.	RW	0

7.4.4 PHY_DELAY_RX_n Register 6.12 / 6.16

The PORT_DELAY_PORT_n register is used to adjust the timestamp by the latency of the PHYs RX path. This is by default set to the actual value but may be corrected to also compensate for delays caused be the transformer. Typically this value should be 190 if Fast-JK mode is used, otherwise 230.

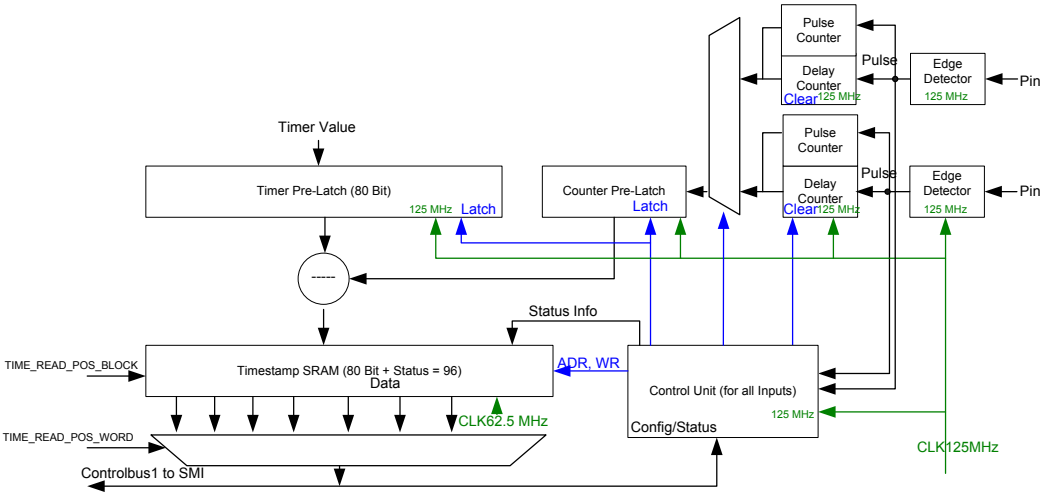
Bit	Name	Description	Mode	Default
15:0	PHY_DELAY_ RX_PORT_n	Value in ns by which timestamps taken for the PHYn on the RX side are corrected.	RW	0

7.5 Input Capture Unit

The input capture unit can be used to timestamp events on any of the GPIO pins. The timestamps are stored in a special memory area which can be accessed through the SMI via dedicated registers. The memory is configured as a FIFO structure; timestamps are written in consecutive addresses. . To read out certain addresses can be selected. Up to 64 timestamps can be stored.

Each GPIO has its own edge detection unit which can be configured to react on a rising edge, falling edge, or both. If an event occurs, the value of the timer is latchedlocally. Each pin has its own counter to count the events that have occurred, The value of this counter is stored as a “rolling number” together with the timestamp. Thus it can be easily determined if an event has been missed by looking for gaps in the rolling number when the timestamp is read. The input capture unit also stores the GPIO number at which the event occurred and the edge that triggered the event together with the timestamp data. Each detection unit can store up to one event which needs to be stored before the next event occurs.

The input capture unit needs 4 clock cycles of 125 MHz to store an event, thus the maximum frequency at which the input edges can be captured is 31.25 MHz. If multiple events happen simultaneously they are stored in the order of the GPIO pin number, i.e. GPIO1 is stored before GPIO2**.** If a new event happens before the event is stored the old event data is lost. As the input capture unit is shared for all pins this frequency applies to all enabled pins together. In any case, the limiting factor for edges is the speed at which the data can be read through the SMI.



7.5.1 Input Event Control Register 7.12

The Input Event Control register is used to configure the input event unit.

Bit	Name	Description	Mode	Default
15	ALL_PTR_RES	Reset all pointers	WC	0
14		Reserved, ignore on read, write as 0	R	0
13	READ_WORD_NEXT	1: Reading next word, when accessing Read Register 0: No impact	RW	0
12	OVRRUN_ANY_GPIO	0: No overrun on any GPIO 1: One of the edge detection unit got a pulse before it could handle the previous one. This means that the frequency of pulses on the GPIO is too high.	RW	0
11	TIMEOUT_ANY_CHAN	0: No Timeout on any GPIO 1: An edge detection unit latched an event, but it could not be stored timely. This means that the frequency of all GPIO events together is too high.	RC	0
10	TIMESTAMP_ ENABLE	1: Enable time stamping unit 0: Disable time stamping unit	RW	0
9	TS_ OVWR_EN	0: New timestamps can overwrite older ones when the buffer is full. 1: New timestamps are not stored if memory has not been read out (no overwrite) and then buffer is full	RW	0
8	TS_RAM_ OVERFLOW	1: Timestamps were overwritten 0: Timestamps were not overwritten	R	0
6:0	TIMESTAMP_ WRITE_POS	Pointer to the timestamp for the next event (96 bit word pointer) incremented by the event manager after writing	R	0

7.5.2 Input Capture Pin Control register 7.8

The Input Capture Pin Control register is used to enable time-stamping for GPIO 0 to 7 and is used to configure the edge on which it should trigger.

Bit	Name	Description	Mode	Default
15:14	IN_CAP_GPIO7	00: Disable event timestamping for GPIO7 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
13:12	IN_CAP_GPIO6	00: Disable event timestamping for GPIO6 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
11:10	IN_CAP_GPIO5	00: Disable event timestamping for GPIO5 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
9:8	IN_CAP_GPIO4	00: Disable event timestamping for GPIO4 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
7:6	IN_CAP_GPIO3	00: Disable event timestamping for GPIO3 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
5:4	IN_CAP_GPIO2	00: Disable event timestamping for GPIO2 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
3:2	IN_CAP_GPIO1	00: Disable event timestamping for GPIO1 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
1:0	IN_CAP_GPIO0	00: Disable event timestamping for GPIO0 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0

7.5.3 Input Capture Pin Control register 7.9

The Input Capture Pin Control register is used to enable timestamping GPIO 8 to 15and is used to configure the edge on which it should trigger.

Bit	Name	Description	Mode	Default
15:14	IN_CAP_GPIO15	00: Disable event timestamping for GPIO15 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
13:12	IN_CAP_GPIO14	00: Disable event timestamping for GPIO14 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
11:10	IN_CAP_GPIO13	00: Disable event timestamping for GPIO13 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
9:8	IN_CAP_GPIO12	00: Disable event timestamping for GPIO12 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
7:6	IN_CAP_GPIO11	00: Disable event timestamping for GPIO11 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
5:4	IN_CAP_GPIO10	00: Disable event timestamping for GPIO10 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
3:2	IN_CAP_GPIO9	00: Disable event timestamping for GPIO9 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
1:0	IN_CAP_GPIO8	00: Disable event timestamping for GPIO8 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0

7.5.4 Input Capture Pin Control register 7.10

The Input Capture Pin Control register is used to enable time-stamping for GPIO 16 to 19 and is used to configure the edge on which it should trigger.

Bit	Name	Description	Mode	Default
15:8		Reserved	RW	0
7:6	IN_CAP_GPIO19	00: Disable event timestamping for GPIO19 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
5:4	IN_CAP_GPIO18	00: Disable event timestamping for GPIO18 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
3:2	IN_CAP_GPIO17	00: Disable event timestamping for GPIO17 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0
1:0	IN_CAP_GPIO11	00: Disable event timestamping for GPIO16 01: Timestamp on rising edge 10: Timestamp on falling edge 11: Timestamp on both edges	RW	0

7.5.5 INPUT_EVENT_DATA_READ_WORD Register 7.15

The INPUT_EVENT_DATA_READ_WORD register gives access to the stored timestamps. To read the complete timestamp the register has to be accessed six times. The least significant word is read first. The location of the data is as follows:

Bit	Name	Description	Mode
95:16	TIMESTAMP	Timestamp of the related event described in bits 15:0.	R
15:14	BUFFER_ STATUS	00: Timestamp buffer is empty 01: Next timestamp is available 10: Only two buffer for timestamp left 11: Buffer is full (immediate next read required or data will be lost)	R
13	TIMESTAMP_ EDGE	1: Rising edge triggered the event 0: Falling edge triggered the event	R
12:8	TIMESTAMP_ GPIO	GPIO number of the pin that triggered the event 00000: GPIO0 00001: GPIO1 00010: GPIO2 …	R
7	TIMER_ERROR	1: Timer overflow, the event has not been processed on time and the timestamp may be broken 0: The timestamp is intact	R
6	OVERRUN	1: An event was detected on the pin but could not be processed 0: All events were processed on time	R
5:0	TIMESTAMP_ NUMBER	Rolling number for events on that pin	R

It may not be required to read the complete timestamp since the first words usually do not change very often, so the PHY provides a direct access to the next timestamp: the INPUT_EVENT_DATA_READ_BLOCK register will always return the LSW of the next timestamp in memory.

To read a timestamp the INPUT_EVENT_DATA_BLOCK_READ is read once and will return bits 15:0 of the next timestamp data. Then the INPUT_EVENT_DATA_WORD_READ is read up to 5 times and will return bits 31:16, bits 47:32 and so on. To get bits 15:0 of the next timestamp, read the INPUT_EVENT_DATA_BLOCK_READ. It is not required to read the complete timestamp.

7.5.6 INPUT_EVENT_DATA_BLOCK_READ Register 7.14

Bit	Name	Description	Mode	Default
15:0	TIMESTAMP_ READ_ BLOCK	Returns the least significant word (bits 15:0) of the next timestamp	R	0

7.5.7 INPUT_CAPTURE_DATA_POINTER Register 7.13

Bit	Name	Description	Mode	Default
14:8	FILLING_LEVEL	Number of data sets in memory 0: Event memory is empty 64: Event memory is full	R	0
5:0	TIMESTAMP_ READ_POS_BL OCK	Value of the pointer to the data sets event memory 0: Next read will read from address 0 of timestamp memory … 63: Next read will read from address 63 of timestamp memory	R	0

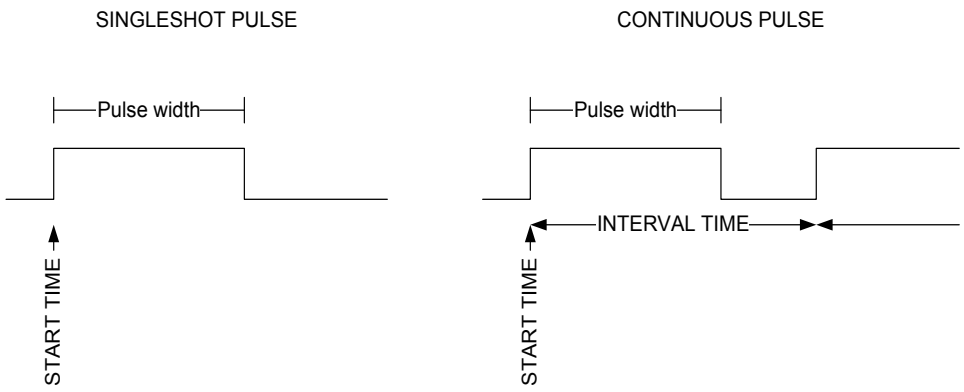
7.6 Pulse Generator Unit

The device has three pulse generator units which can generate pulses or events based on the PTP timer. Each can run in either of two different modes: single-shot or continuous pulse generation.

A pulse is triggered when the START_TIME exceeds the time from the PTP timer. Although the START_TIME has a resolution of 1/32 ns, the exact output time may be up to 8 ns later as the output signal is running on the 125 MHz clock. However, the start time is internally calculated with 1/32 ns accuracy so that the error does not accumulate.

To program a new pulse generation: disable the current pulse generation for the respective channel, write the values, and then re-enable the pulse generation by writing PULSE_GO with one and setting PULSE_CONFIG to the required value..

For continuous pulse the start times are calculated by taking the previous start time, adding the interval time, comparing the result to the timer, and generating the next pulse when the timer value exceeds the start time.



There are four registers which control the pulse generators. All registers are shadow registers that can be written first and are transferred to the pulse channel in PULSE_CHANNEL at the moment the PULSE_GO bit is set to ‘1’. After writing the PULSE_CHANNEL register, these registers are updated with the actual value for this channel and can subsequently be read.

7.6.1 Pulse Output Control Register 7.16

The Pulse Output Control register controls the pulse units. All data written is stored for the channel selected in PULSE_CHANNEL.

Bit	Name	Description	Mode	Default
15:8		Reserved, write as 0, ignore on read	R/W	
9	LATCH_WIDTH	Latch newly-written data from PULSE_WIDTH register and use for the next pulse. This bit is set after the PULSE_WIDTH register has been written and the new values should be applied. Until this is done the old value is used. This is only valid for the pulse width and the interval data. The time unit must be stopped before updating the start time.	RW	0
8	LATCH_INTERVAL	Latch newly-written latch interval data from the PULSE_INTERVAL register and use for the next pulse. All other values remain the same. This bit is set after the PULSE_INTERVAL register has been written and the new values should be applied. Until this is done the old value is used. This is only valid for the pulse width and the interval data. The time unit must be stopped before updating the start time.	RW	0
7	PULSE_GO	Latch newly written data and use for next pulse. This bit is set after the PULSE_DATA register has been written and the new values should be used. Until this is done the old value is used. This is only valid for the pulse width and the interval data. The time unit must be stopped before updating the start time.	RW	0
6	INT_EN	Enable interrupt for this channel An interrupt is triggered when the timer is larger than the current PULSE_STARTTIME (continuously updated according to PULSE_INTERVAL)	RW	0
5	Channel_inv	Invert output of channel in 2:0	RW	0
4:3	PULSE_ CONFIG	Configuration for pulse. 00: Off	RW	0

		01: Single shot 10: Continuous 11: Reserved		
2:0	PULSE_ CHANNEL	000: Values in bits 9:3 and respective shadow registers PULSE_STARTTIME, PULSE_WIDTH and PULSE_INTERVAL will be written to channel 0 001: Values in bits 9:3 and respective shadow registers will be written to channel 1 010: Values in bits 9:3 will be written to channel 2	RW	0

7.6.2 PULSE_STARTTIME Register 7.17

The PULSE_STARTTIME register gives the start time for the next pulse. For continuous pulses it is incremented with the PULSE_INTERVAL value after the pulse has been triggered. The updated value can be read after writing the PULSE_CHANNEL value. . Do not set the PULSE_STARTTIME to a value in the past. This register has to be accessed five times with the most significant word first.

Word	Name	Description	Mode	Default
79:0	PULSE_ STARTTIME	Actual start time for pulse. Will be updated whenever a pulse was generated and a new start time is calculated based on PULSE_INTERVAL.	R	0
79:0	INITIAL_PULSE_ STARTTIME	Initial start time for pulse.	W	0

7.6.3 PULSE_WIDTH Register 7.19

Bit	Name	Description	Mode	Default
47:38	PULSE_ WIDTH_SEC	Pulse high width seconds for single and continuous pulse. The shortest pulse width value is 24 ns.	RW	0
37:5	PULSE_ WIDTH_NS	Pulse high width nanoseconds for single and continuous pulse. The shortest pulse width value is 24 ns.	RW	0
4:0	PULSE_ WIDTH_FNS	Pulse high width fractions of nanoseconds for single and continuous pulse. The shortest pulse width value is 24 ns.	RW	0

7.6.4 PULSE_INTERVAL Register 7.18

Bit	Name	Description	Mode	Default
47:35	PULSE_ INTERVAL_SEC	Pulse interval seconds after which the next pulse is generated (only for continuous pulse). The shortest pulse interval value is 24 ns.	RW	0
Bits 34:5	PULSE_ INTERVAL_NS	Pulse interval nanoseconds after which the next pulse is generated (only for continuous pulse). The shortest pulse interval value is 24 ns.	RW	0
Bit 4:0	PULSE_ INTERVAL_FNS	Pulse interval fractions of nanoseconds after which the next pulse is generated (only for continuous pulse). The shortest pulse interval value is 24 ns.	RW	0

8.1 AC Timing

8.1.1 Serial Management Interface (SMI) Timing

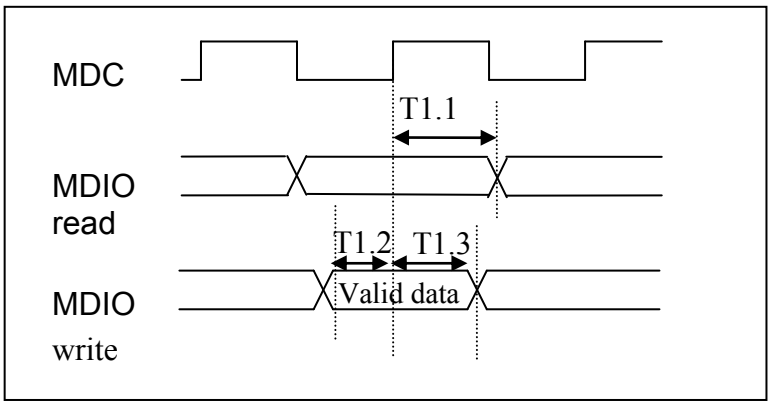


Figure 1: SMI Timing

ara-meter	Description	Min	Typ	Max	Units	Notes
T1.1	MDC to MDIO delay	0		15	ns	Data output from PHY
T1.2	MDC to MDIO setup	10			ns	
T1.3	MDC to MDIO hold	10			ns	
	MDC frequency			25	MHz	

8.1.2 Reset Timing

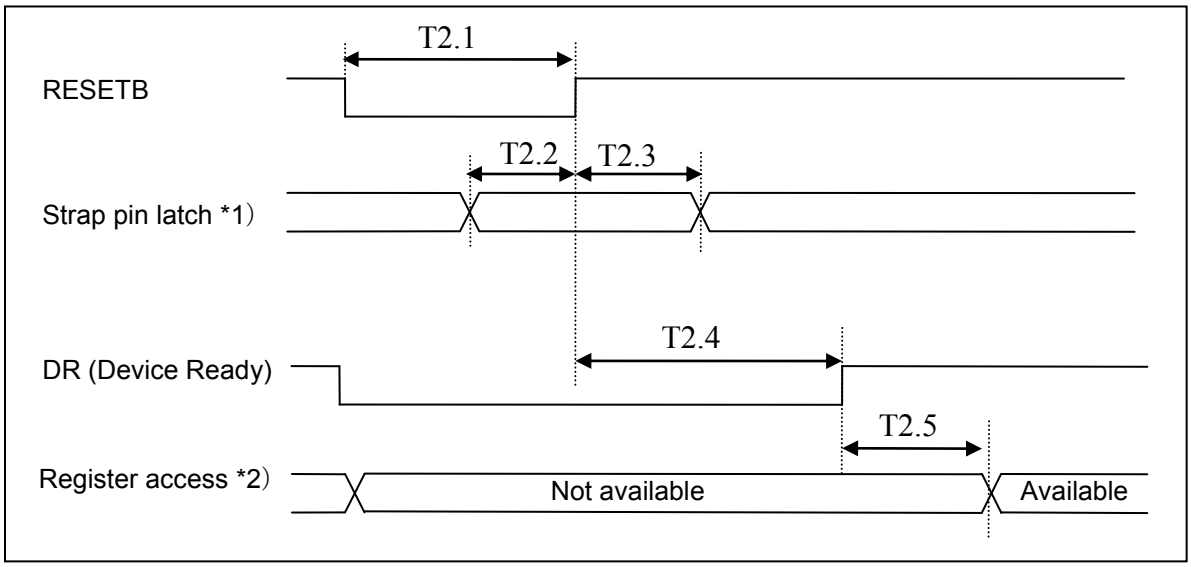


Figure 2: Reset Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T2.1	RESETB pulse width	100			us	
T2.2	Strap input setup to RESETB rising	200			ns	
T2.3	Strap input hold after RESETB rising	400			ns	
T2.4	Device Ready rising after RESETB rising		600		ns	
T2.5	Register access available after Device Ready rising			5	ms	

*1) Strap options are latched. (Refer to 4.9 Strap Options)
*2) PHY register access through SMI is available T2.5 after Device Ready rising

8.1.3 Clock Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
-	Reference clock frequency (25MHz / 50 MHz selectable)		25		MHz	MII
			50		MHz	RMII
-	Clock frequency tolerance *1)	-100		100	ppm	
-	Duty cycle	40	50	60	%	
-	Jitter tolerance		20		ps (rms)*1)	

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*1) Root Mean Square

8.1.4 100Base-TX Timings

8.1.4.1 100M MII Receive Timing

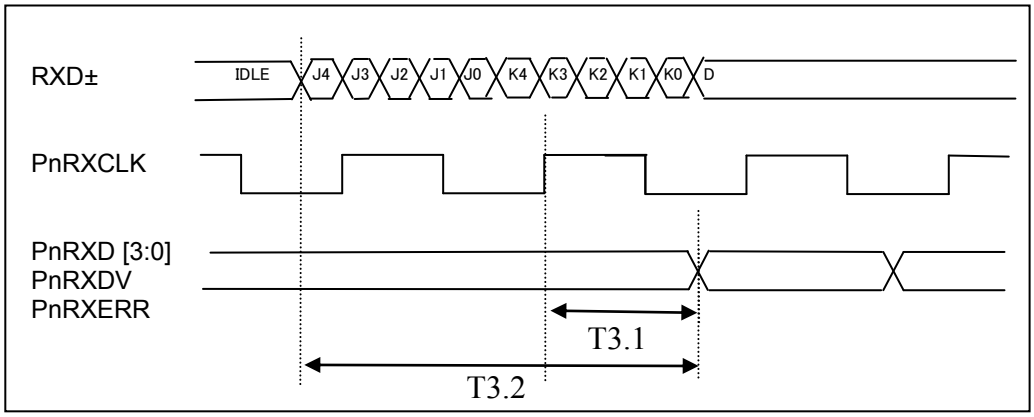


Figure 3: 100BT MII receive timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T3.1	Received signals output delay after rising edge of PnRXCLK	15		27	ns	
T3.2	Start of RX-bit to PnRXDV valid		170		ns	RX_DV_J2T (Register PHY.31.1) set
			210		ns	RX_DV_J2T (Register PHY.31.1) cleared
	PnRXCLK frequency		25		MHz	
	PnRXCLK duty-cycle	45	50	55	%	

*1) Note that glitch may occur on output signals between min and max value of T3.1 after rising edge of P*RXCLK. However, it is compliant with IEEE802.3 standard because the setup time at the input of MAC is 13ns (=Period 40ns - max value > 10ns) and the hold time is 15ns (= min value > 10ns).

8.1.4.2 100M MII Transmit Timing

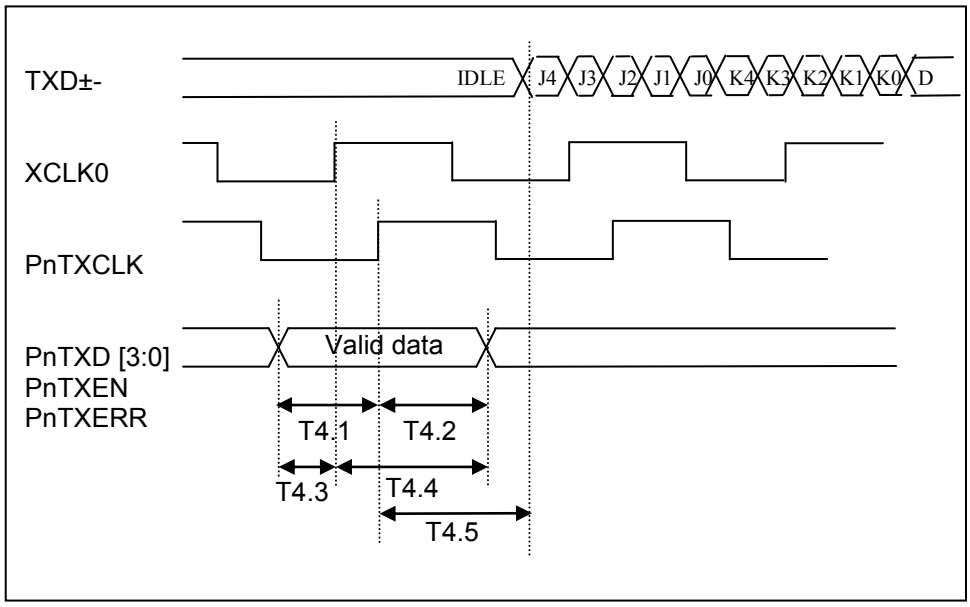


Figure 4: 100BT MII Transmit Timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T4.1	Transmit signals setup to PnTXCLK rising	13			ns	Normal MII timing *1)
T4.2	Transmit signals hold after PnTXCLK rising			0	ns	
T4.3	Transmit signals setup to XCLK0 rising	8			ns	EtherCAT MII timing *1
T4.4.	Transmit signals hold after XCLK0 rising			0	ns	
T4.5	PnTXD latch until start of TX-bit		50		ns	Normal MII timing *1)
			90			EtherCAT MII timing *1
-	PnTXCLK frequency		25		MHz	
-	PnTXCLK duty-cycle	45	50	55	%	

*1) Note that the timing is configurable by strap option (P1TXCLK)
Refer to 4.9 Strap Options.

8.1.5 10Base-T Timings

8.1.5.1 10M MII Receive Timing

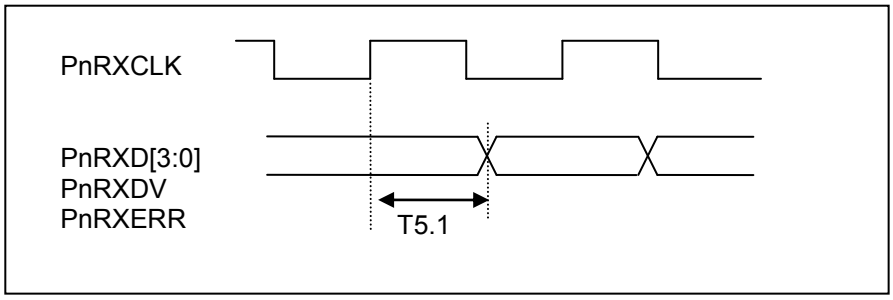


Figure 5: 10BT MII receive timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T5.1	Received signals output delay after rising edge of P*RXCLK	100		300	ns	
	PnRXCLK frequency		2.5		MHz	
	PnRXCLK duty-cycle	45	50	55	%	

8.1.5.2 10M MII Transmit Timing

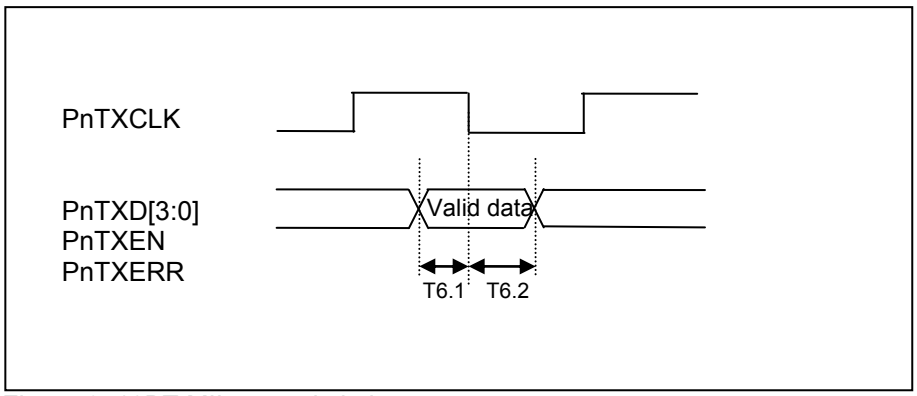


Figure 6: 10BT MII transmit timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T6.1	Transmit signals setup to falling edge of PnTXCLK	0			ns	
T6.2	Transmit signals hold to falling edge of PnTXCLK			100	ns	
	PnTXCLK frequency		2.5		MHz	
	PnTXCLK duty-cycle	45	50	55	%	

8.1.6 RMII 10/100Base-TX Timings

8.1.6.1 RMII Receive Timing

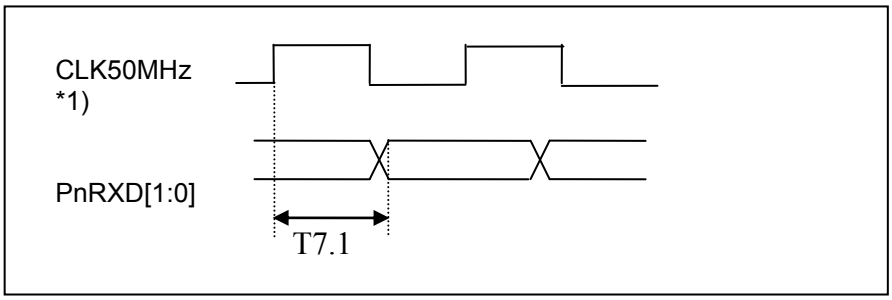


Figure 7: RMII receive timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T7.1	Receive signals output delay after rising edge of CLK50MHz	2		14	ns	
	CLK50MHz frequency		50		MHz	

*1) External 50MHz clock input

8.1.6.2 RMII Transmit Timing

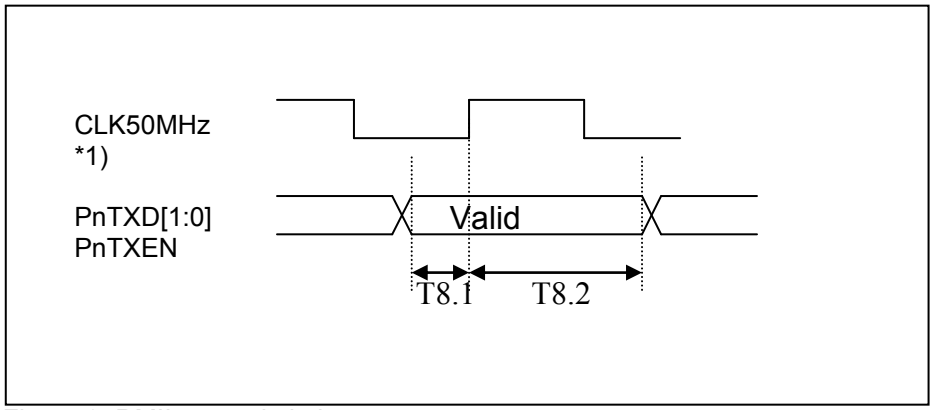


Figure 8: RMII transmit timing

Para-meter	Description	Min	Typ	Max	Units	Notes
T8.1	Transmit signals setup to rising edge of CLK50MHz	4			ns	
T8.2	Transmit signals hold after rising edge of CLK50MHz	2			ns	
	CLK50MHz frequency		50		MHz	

*1) External 50MHz clock input

8.1.7 Sequence for turn on

RESETB must be released after all external power is ready.

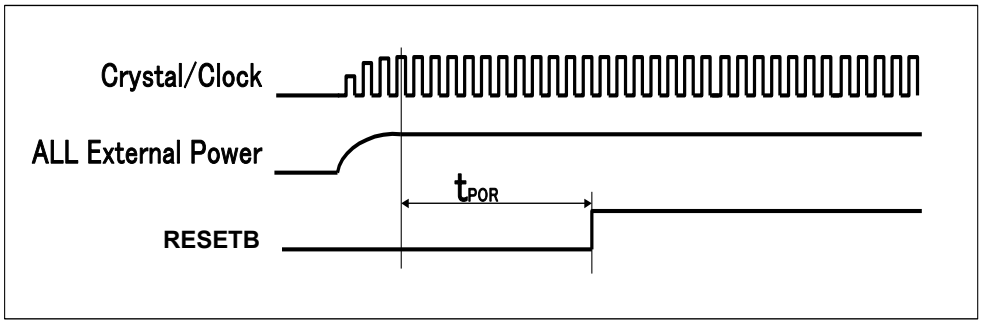


Figure 9: Reset timing

Parameter	Description	Min	Typ	Max	Units	Notes
t_{POR}	Power on Reset timing	4			ms	

8.10 DC Characteristics

8.10.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Units
Analogue power supply voltage	P1VDDMEDIA, P2VDDMEDIA, VDDAPLL		-0.5 to +2.0	V
Digital Power Supply Voltage	VDD15		-0.5 to +2.0	V
I/O Voltage	VDDIO		-0.5 to +4.6	V
Analog 3.3V power supply	VDDACB		-0.5 to 4.6	V
Analog 3.3V power supply	REGAVDD REGBDD		-0.5 to 4.6	V
Analog 3.3V power supply	VDD33ESD		-0.5 to 4.6	V
Output Current	P0LINKLED/GPIO0,P0ACTLED/GPIO1,P1LINKLED/GPIO2,P1ACTLED/GPIO3,P0100BTLED/GPIO4,P1100BTLED/GPIO5, P0TXERR/GPIO9,P0TXD3/GPIO10,P0TXD2/GPIO11,P0TXCLK,P1TXERR/GPIO15,P1TXD3/GPIO16,P1TXD2/GPIO17,P1TXCLK,MDIO,P0TXD1,P1TXD1		21	mA
Output Current	P0CRS/P0CRS_DV/GPIO6,P0RXD3/GPIO7,P0RXD2/GPIO8,P0RXD1,P0RXD0,P0RXCLK, P0RXERR,P0RXDV,P1CRS/P1CRS_DV/GPIO12,P1RXD3/GPIO13,P1RXD2/GPIO14,P1RXD1,P1RXD0,P1RXCLK,P1RXERR,P1RXDV,P0COL/GPIO18,P1COL/GPIO19		11	mA
Storage temperature	Tstg		-65 to +150	°C

8.10.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Rating	Units
Analogue power supply voltage	P1VDDMEDIA, P2VDDMEDIA, VDDAPLL		1.425 to 1.575	V
Digital Power Supply Voltage	VDD15		1.425 to 1.575	V
I/O Voltage	VDDIO		2.25 to 2.75 3.0 to 3.6	V
Analog 3.3V power supply	VDDACB		3.0 to 3.6	V
Analog 3.3V power supply	REGAVDD REGBVDD		3.0 to 3.6	V
Analog 3.3V power supply	VDD33ESD		3.0 to 3.6	V
Output Current	P0LINKLED/GPIO0 ,P0ACTLED/GPIO1 ,P1LINKLED/GPIO 2,P1ACTLED/GPIO 3,P0100BTLED/GP IO4,P1100BTLED/ GPIO5,P0TXERR/ GPIO9,P0TXD3/GP IO10,P0TXD2/GPI O11,P0TXCLK,P1T XERR/GPIO15,P1T XD3/GPIO16,P1TX D2/GPIO17,P1TXC LK,MDIO,P0TXD1, P1TXD1		6	mA
Output Current	P0CRS/P0CRS_D V/GPIO6,P0RXD3/ GPIO7,P0RXD2/G PIO8,P0RXD1,P0R XD0,P0RXCLK, P0RXERR,P0RXD V,P1CRS/P1CRS_ DV/GPIO12,P1RX D3/GPIO13,P1RXD 2/GPIO14,P1RXD1 ,P1RXD0,P1RXCL K,P1RXERR,P1RX DV,P0COL/GPIO18 ,P1COL/GPIO19		3	mA
Value for EXTRES	EXTRES		12.4±1%	kΩ
Operating ambient temperature	T_a		-40 to +85	°C

8.10.3 DC Electrical Characteristics

Parameter	Symbol	Conditions			Min	Typ	Max	Unit
Current Consumption	-	100B	External 1.5V supplied	3.3V		140		mA
				1.5V		180		mA
			Internal Regulater used	3.3V		240		mA
				1.5V		0		mA
		10B	External 1.5V supplied	3.3V		240		mA
				1.5V		90		mA
			Internal Regulater used	3.3V		290		mA
				1.5V		0		mA
Internal pull up strap resistor	R_{stru}				14.2	31.9	80.7	kΩ
Internal pull down strap resistor	R_{strd}				20.6	44.9	116.4	kΩ
Input voltage, low	-	VDDIO = 2.5V			0		0.7	V
Input voltage, high	-	VDDIO = 2.5V			1.7		VDD	V
Input voltage, low	-	VDDIO = 3.3V			0		0.8	V
Input voltage, high	-	VDDIO = 3.3V			2.0		VDD	V
Output voltage low	Vol	VDDIO=2.5V Iol=0mA					0.1	V
Output voltage high	Voh	VDDIO=2.5V Ioh=0mA			Vdd-0.1			V
Output voltage low	Vol	VDDIO=3.3V Iol=0mA					0.1	V
Output voltage high	Voh	VDDIO=3.3V Ioh=0mA			Vdd-0.1			V

8.10.4 Differential Parameters on Secondary Side of Transformer.

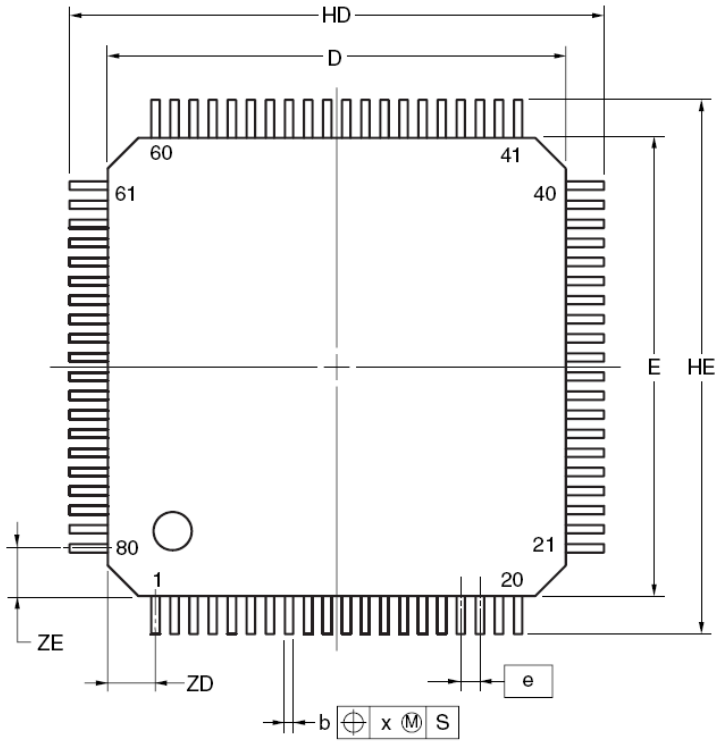
Description	Min	Typ	Max	Units	Notes
100M TX output high	.95		1.05	V	
100M TX mid-level	-50		50	mV	
100M TX output low	-.95		-1.05	V	
10M TX output high	2.2		2.8	V	

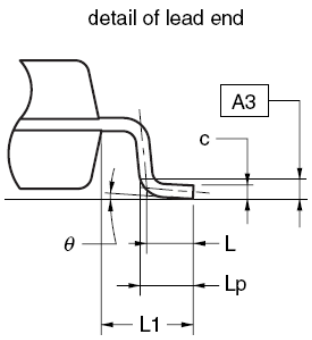
8.10.5 100Base-FX Output Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage - Low [V] Vol-VDDIO	-	-	-1.81		-1.55	V
Output Voltage - High [V] Voh-VDDIO	-	-	-1.12		-0.88	V

Physical dimensions

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P80GK-50-GAK

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

Revision history

Date	Revision	Changes
March 19, 2013	1.00	Initial release

Industrial Ethernet PHY