

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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H8S/2268 Series E6000 Emulator  
HS2268EPI61H  
Supplementary Information



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- Emulator station
- User system interface cables
- PC interface boards
- Optional SIMM memory module

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# SAFETY PAGE

## READ FIRST

- **READ** this user's manual before using this emulator product.
- **KEEP** the user's manual handy for future reference.

Do not attempt to use the emulator product until you fully understand its mechanism.

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This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.



**DANGER** indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.



**WARNING** indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.



**CAUTION** indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.



**CAUTION** used without the safety alert symbol indicates a potentially hazardous situation which, if not avoided, may result in property damage.

**NOTE** emphasizes essential information.

# **WARNING**

**Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.**

- 1. Do not repair or remodel the emulator product by yourself for electric shock prevention and quality assurance.**
- 2. Always switch OFF the E6000 emulator and user system before connecting or disconnecting any CABLES or PARTS.**
- 3. Always before connecting any CABLES, make sure that pin 1 on both sides are correctly aligned.**
- 4. Supply power according to the power specifications and do not apply an incorrect power voltage. Use only the provided power cable.**

# **CAUTION**

**This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.**

# Preface

Thank you for purchasing the H8S/2268 series E6000 emulator.

The H8S/2268 series E6000 emulator (hereafter referred to as the E6000) was designed as a software and hardware development tool for systems based on Hitachi's original microcomputers HD64F2268.

The E6000 provides a CD-R that contains the Hitachi Debugging Interface (HDI) system program, test program, and the user's manual.

There are three manuals for the E6000: the H8S series E6000 Emulator User's Manual, this Supplementary Information, and the Hitachi Debugging Interface User's Manual. The E6000 Emulator User's Manual describes E6000 functions common to all H8S series microcomputers. This Supplementary Information describes the functions specialized for each microcomputer supported by the H8S/2268 series E6000 emulator. Please read this manual before using the E6000.

To connect the E6000 to the user system, a user system interface cable for each package type is available. For details on the user system interface cable, refer to the User System Interface Cable User's Manual.

The following shows the related manuals:

- H8S Series E6000 Emulator User's Manual (HS2000EPI61HE)
- Hitachi Debugging Interface User's Manual (HS6400DIIW5SE)
- User System Interface Cable User's Manual (HS2268ECH61HE, etc)
- The PC interface board user's manual which will be the following manuals:
  - ISA Bus Interface Board User's Manual (HS6000EII01HE)
  - PCI Bus Interface Board User's Manual (HS6000EIC01HE, HS6000EIC02HE)
  - PCMCIA Interface Card User's Manual (HS6000EIP01HE)
  - LAN Adapter (HS6000ELN01HE)
- Option Memory Board User's Manual
  - 1M SIMM Memory Board User's Manual (HS6000EMS11HE)
  - 4M SIMM Memory Board User's Manual (HS6000EMS12HE)

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# Contents

Section 1 Overview .....	1
1.1 Environment Conditions .....	1
1.2 Supported MCUs and User System Interface Cables.....	2
1.3 Operating Voltage and Frequency Specifications.....	2
Section 2 User System Interface.....	4
2.1 Signal Protection.....	4
2.2 User System Interface Circuits.....	4
Section 3 Notes on Use.....	7
3.1 I/O Register Differences between Actual MCU and E6000 .....	7
3.2 Access to the Reserved Area.....	7
3.3 Use of an Internal RAM Area as External Memory.....	8
3.4 Support of Flash Memory .....	8
3.5 Hardware Standby.....	8
3.6 Interrupts in Watch Mode and Software Standby Mode.....	8
Section 4 HDI Parameters .....	11
4.1 Address Areas .....	11
4.2 Access Status.....	12
4.3 I/O Modules .....	13
Section 5 Diagnostic Test Procedure.....	14
5.1 System Set-Up for Test Program Execution .....	14
5.2 Diagnostic Test Procedure Using the Test Program .....	15



## Figures

Figure 2.1	Default User System Interface Circuit.....	5
Figure 2.2	User System Interface Circuit for MD2, MD1, and NMI.....	5
Figure 2.3	User System Interface Circuit for RESET.....	5
Figure 2.4	User System Interface Circuit for AN0-AN9, SEG1-SEG40, C1, C2, COM1-COM4, TONED, V1-V3, AVcc, AVss and Vref Signals.....	6
Figure 3.1	Enable automatic re-execution from interrupt break Check Box.....	9
Figure 3.2	Emulator Processing Flow When an Interrupt Occurs in the Watch Mode or the Software Standby Mode.....	10

## Tables

Table 1.1	Environment Conditions.....	1
Table 1.2	H8S/2268 Series MCU and User System Interface Cable.....	2
Table 1.3	Operating Voltage and Frequency Specifications.....	2
Table 1.4	Clock Selections.....	3
Table 4.1	Address Area Parameters.....	11
Table 4.2	Access Status Parameters.....	12
Table 4.3	I/O Modules.....	13



# Section 1 Overview

The H8S/2268 series E6000 emulator (hereafter referred to as the E6000) is an efficient software and hardware development support tool for application systems using Hitachi's original microcomputers H8S/2268 series.

## 1.1 Environment Conditions

**Table 1.1 Environment Conditions**

<b>Item</b>	<b>Specifications</b>	
Temperature	Operating: +10 to +35°C	
	Storage: -10 to +50°C	
Humidity	Operating: 35 to 80% RH; no condensation	
	Storage: 35 to 80% RH; no condensation	
Ambient gases	No corrosive gases	
AC Power supply voltage	100 V to 240 V AC $\pm 5\%$ 50/60 Hz 0.6 A max.	
AC input cable*	HS2268EPI61H	HS2268EPI61HB
	100 V-120 V (UL)	200 V-240 V (BS)
User system voltage (UVcc)	Depends on the target MCU within the range 2.7 V to 5.5 V	

Note: HS2268EPI61H must be used at AC100 V-120 V input voltage.  
HS2268EPI61HB must be used at AC200 V-240 V input voltage.

## 1.2 Supported MCUs and User System Interface Cables

Table 1.2 show the correspondence between the MCUs and the user system interface cables supported by the E6000.

**Table 1.2 H8S/2268 Series MCU and User System Interface Cable**

No.	MCU Type Number	Package	E6000 User System Interface Cables
1	HD64F2268 HD6432268 HD6432266	100-pin QFP, 100-pin TQFP (FP-100B/TFP-100B)	HS2268ECH61H
2		100-pin TQFP (TFP-100G)	HS2268ECN61H

## 1.3 Operating Voltage and Frequency Specifications

Table 1.3 shows examples of the MCU operating voltage and frequency specifications supported by the E6000. If the E6000 is used in an environment that exceeds the operating voltage range and operating frequency range guaranteed for the MCU operation, normal emulator operation is not guaranteed.

**Table 1.3 Operating Voltage and Frequency Specifications**

MCU Types	Operating Voltage (V)	Operating Frequency (φ) (MHz)
H8S/2268 series	4.0-5.5	2-20.5
	2.7-4.0	2-13.5

# NOTE

**For details on the operating voltage and frequency specifications, refer to the MCU hardware manual.**

In the E6000, the clock can be selected by using the Configuration window or the Clock command.

**Table 1.4 Clock Selections**

Clock Command Parameter		Configuration Window Setting		Notes
Main clock	Subclock	Main clock	Subclock	
10	32	10MHz internal clock	32 kHz internal clock	Default
	t		Target clock	
20	32	20 MHz internal clock	32 kHz internal clock	
	t		Target clock	
t	t	Target	Target clock	
t2	t	Target/2	Target clock	

## NOTE

The system clock ( $\phi$ ) frequency is the same clock frequency input to the XTAL and EXTAL when external clock t is specified. For example, when a 20-MHz crystal oscillator is connected to the XTAL and EXTAL of the user system, the system clock ( $\phi$ ) frequency is 20 MHz. When external clock t2 is specified, the system clock ( $\phi$ ) frequency is 1/2 of the clock frequency input to the XTAL and EXTAL.

The frequency of the E6000 internal clock specified with the HDI CLOCK command is applied to the system clock ( $\phi$ ).

## Section 2 User System Interface

All user system interface signals are directly connected to the MCU in the E6000 with no buffering except for those listed below which are connected to the MCU through control circuits:

- NMI
- RESET
- MD2, MD1
- XTAL
- EXTAL
- OSC1
- OSC2
- STBY

### 2.1 Signal Protection

All user system interface signals are protected from over- or under-voltage by use of diode arrays except for the AVcc and Vref.

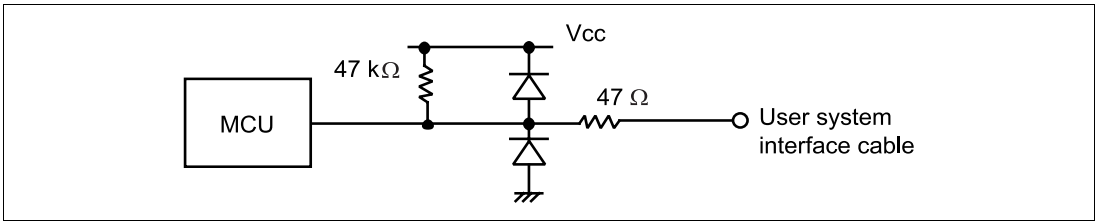
The Vcc pins (except for the AVcc pin) at the head of the user system interface cable are connected together. The E6000 monitors the voltage level of the Vcc pins and displays the power-supply status in the Status Window.

### 2.2 User System Interface Circuits

The interface circuit between the MCU in the E6000 emulator and the user system has a signal delay of about 8 ns due to the user system interface cable. And high-impedance signals will be pulled up to the high level by pull-up resistors. When connecting the E6000 emulator to a user system, adjust the user system hardware to compensate for propagation delays.

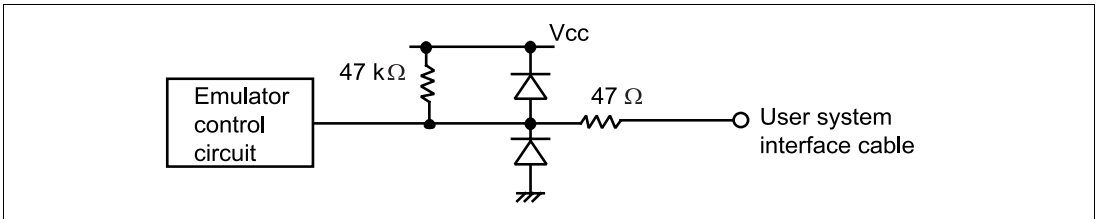
The following diagrams show the interface signal circuits

**Default:**



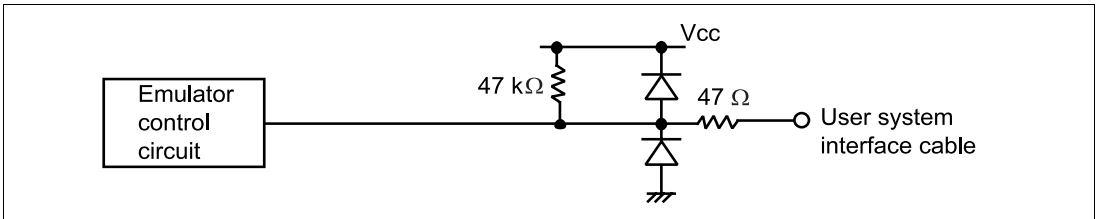
**Figure 2.1 Default User System Interface Circuit**

**Mode Pins (MD2 and MD1) and NMI:** The NMI signal is input to the MCU through the emulator control circuit. The rising/falling time of the NMI signal must be 8 ns/V or less. The mode pins are only monitored. The CPU mode depends on the HDI Configuration settings.



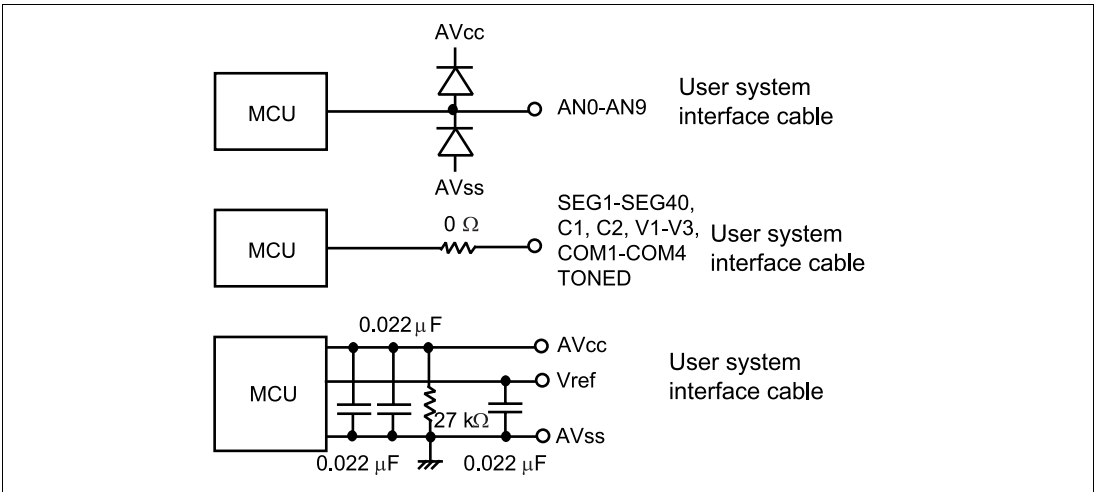
**Figure 2.2 User System Interface Circuit for MD2, MD1, and NMI**

**RESET:**



**Figure 2.3 User System Interface Circuit for RESET**

**AN0-AN9, SEG1-SEG40, C1, C2, COM1-COM4, TONED, V1-V3, AVcc, AVss and Vref:**



**Figure 2.4 User System Interface Circuit for AN0-AN9, SEG1-SEG40, C1, C2, COM1-COM4, TONED, V1-V3, AVcc, AVss and Vref Signals**



## Section 3 Notes on Use

### 3.1 I/O Register Differences between Actual MCU and E6000

In the E6000, one evaluation chip emulates several types of MCU. Therefore, there are some differences in I/O registers between an actual MCU and the E6000. Note these differences when accessing the I/O registers.

I/O port is in the input state at default. The I/O register contents indicate the emulator port status. When the user system interface cable is not connected, the read value is 1 due to the emulator's pull-up resistors.

In the E6000, accesses to the following registers for controlling the flash memory are invalid.

- RAM emulation register (RAMER: H'FEDB)
- Flash memory control register 1 (FLMCR1: H'FFA8)
- Flash memory control register 2 (FLMCR2: H'FFA9)
- Erase block register 1 (EBR1: H'FFAA)
- Erase block register 2 (EBR2: H'FFAB)

Flash memory power control register (FLPWCR: H'FFAC)

### 3.2 Access to the Reserved Area

When accessing the reserved area, note the following:

If the reserved area is used, the operation in the actual MCU cannot be guaranteed. If the user program extends to the reserved area during debugging, select the MCU having the largest ROM capacity.

### **3.3 Use of an Internal RAM Area as External Memory**

An internal RAM area can be used as an external address when the RAME bit of the SYSCR is cleared to 0. An emulator (optional memory) cannot be specified for the internal RAM area. Only user memory can be accessed as an external address. Option memory cannot be accessed as an external address. In this case, Memory Mapping must be set to Internal RAM.

### **3.4 Support of Flash Memory**

The E6000 does not emulate the flash memory control operation in the MCU.

### **3.5 Hardware Standby**

When the User Standby enable check box is selected in the Configuration window, the STBY signal of the user system is directly input to the E6000.

When the STBY signal is input, the E6000 hardware is initialized and the E6000 stops emulation. Therefore, the User Standby enable check box should be cleared (not selected) for general emulation.

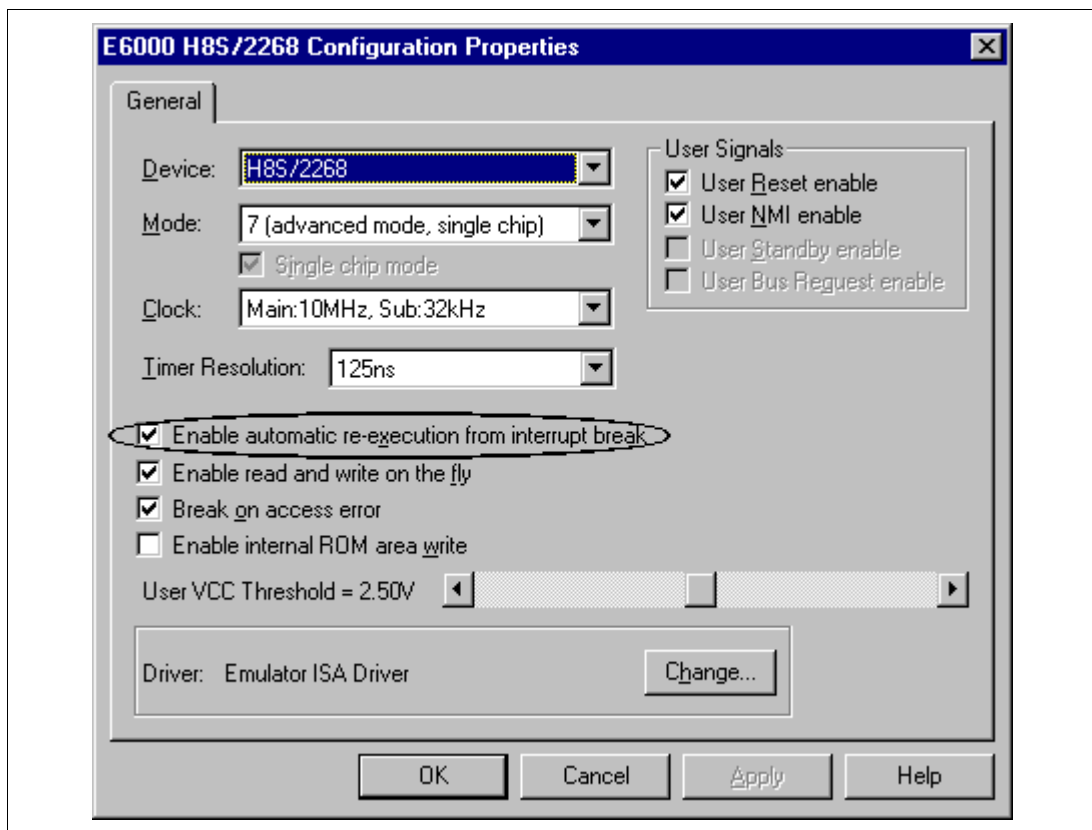
### **3.6 Interrupts in Watch Mode and Software Standby Mode**

There are the following limitations on using the emulator due to the restrictions of the emulator hardware.

1. When a wakeup interrupt (WKPO to 7) occurs in the software standby mode, the software standby mode cannot be cancelled. When the wakeup interrupt occurs, the user program is forcibly terminated. On termination, the emulator enters the active mode.
2. When an 8-bit reload timer (TMR\_4) overflow interrupt (OVI4 to 7) or a wakeup interrupt (WKPO to 7) occurs in the watch mode, the watch mode cannot be cancelled. When the interrupt occurs, the user program is forcibly terminated. On termination, the emulator enters the active mode regardless of the LSON value.

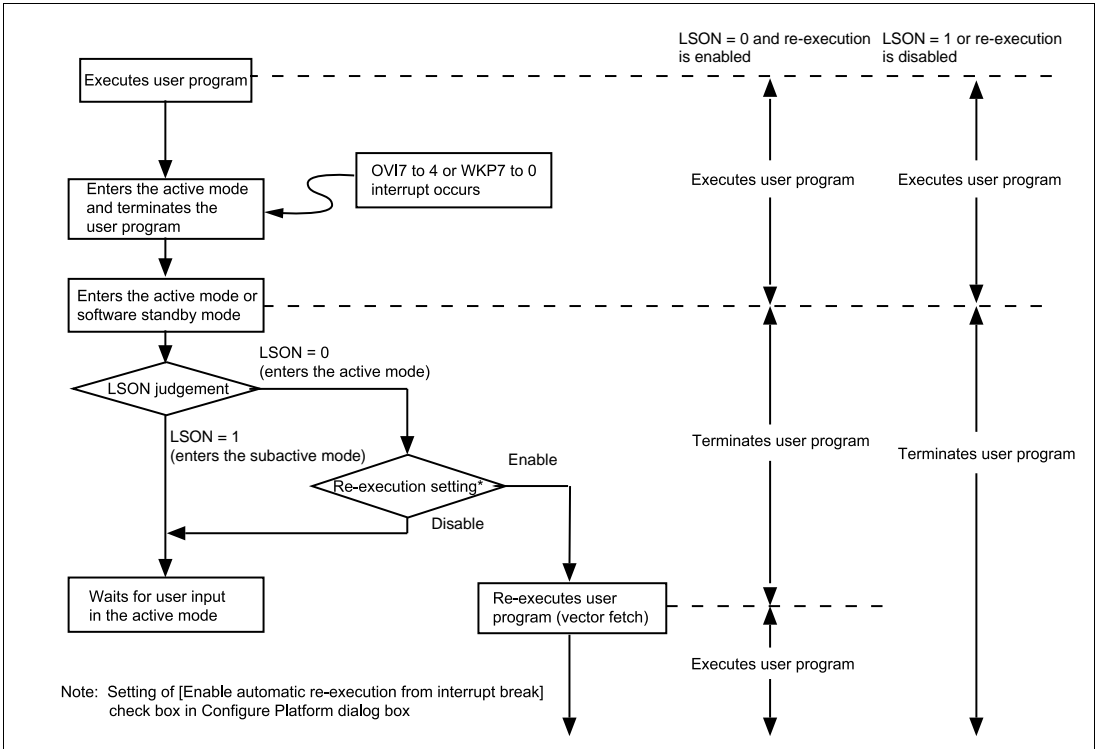
When Enable automatic re-execution from interrupt break check box has been checked in Configure Platform dialog box and the execution of the user program is terminated by one of the above causes, the user program is re-executed automatically only when the high-speed mode or medium-speed mode (LSON = 0) is entered after resuming from the interrupt.

When Enable automatic re-execution from interrupt break check box is not checked, the user program is not re-executed automatically.



**Figure 3.1 Enable automatic re-execution from interrupt break Check Box**

By checking the Enable automatic re-execution from interrupt break check box, the state transition when an interrupt occurs can be pseudo-emulated. Note that the timing of the state transition from the interrupt occurrence is different from that of the actual MCU. The emulator processing flow and the timing of the termination of the user program is shown in figure 3.2.



**Figure 3.2 Emulator Processing Flow When an Interrupt Occurs in the Watch Mode or the Software Standby Mode**

## Section 4 HDI Parameters

### 4.1 Address Areas

Table 4.1 lists the parameters for address areas (Area) that can be specified with HDI command line interface or displayed as trace results.

**Table 4.1 Address Area Parameters**

<b>HDI Parameter (Trace Display)</b>	<b>Address Area</b>	<b>Description</b>
rom	On-chip ROM	MCU's on-chip ROM, which can be read but cannot be written to.
ram	On-chip RAM	MCU's on-chip RAM (except for DTC RAM), which can be read and written to.
IO16 (I/O-16)	Internal I/O registers (16-bit bus)	MCU's internal I/O registers for the 16-bit bus.
IO8 (I/O-8)	Internal I/O registers (8-bit bus)	MCU's internal I/O registers for the 8-bit bus.
IO	Internal I/O registers	MCU's internal I/O registers for the 8-bit bus and 16-bit bus.
ext16 (EXT-16)	External area (16-bit bus)	External area for the 16-bit bus, which can be allocated to the user system memory or the optional SIMM memory module in the E6000.
ext8 (EXT-8)	External area (8-bit bus)	External area for the 8-bit bus, which can be allocated to the user system memory or the optional SIMM memory module in the E6000.
ext	External area	External area for the 8-bit bus and 16-bit bus, which can be allocated to the user system memory or optional SIMM memory module in the E6000.
Dtcram (RAM/DTC)	DTC RAM	MCU's on-chip RAM for DTC.

## 4.2 Access Status

Table 4.2 lists the parameters for access status (Status) that can be specified with HDI command line interface or displayed as trace results.

**Table 4.2 Access Status Parameters**

<b>HDI Parameter (Trace Display)</b>	<b>Access Status</b>	<b>Description</b>
dmac	On-chip DMAC	Access by the MCU's DMAC (Cannot be accessed by the EXDMA controller.)
dtc	On-chip DTC	Access by the MCU's DTC
refresh	Refresh	Refresh cycle by the MCU's refresh controller
prefetch (PROG)	CPU prefetch	Instruction prefetch cycle by the CPU
data (DATA)	CPU data access	Data access for instruction execution by the CPU

## 4.3 I/O Modules

Table 4.3 lists the parameters for I/O module selection in the custom setting of the HDI configuration window.

**Table 4.3 I/O Modules**

HDI Parameter	I/O Module
PWM14	MCU's 14-bit PWM.
D/A	MCU's D/A.
TMR2-3	MCU's 8-bit timer (TMR2-3).
WDT1	MCU's WDT (WDT1).
IIC1	MCU's I2C bus (IIC1).
IIC0	MCU's I2C bus (IIC0).
IrDA	MCU's IrDA.
DTC	MCU's DTC.
TPU3-5	MCU's 16-bit timer pulse unit (TPU3-5).
MULT	Set SCI0 and SCI1 to support the multiprocessor communication/smart card interface. SCI2 is always enabled.
DMAC	MCU's DMAC.
REFRESH	MCU's refresh controller.
a/d (4   8)	A/D converter. Four or eight data registers can be selected.
sci (1   2   3   4)	Serial communication interface. The number of channels can be selected as follows: 1: SCI0, 1 2: SCI0, 1, 2 3: SCI0, 1, 2, 3 4: SCI0, 1, 2, 3, 4

# Section 5 Diagnostic Test Procedure

This section describes the diagnostic test procedure using the E6000 test program.

## 5.1 System Set-Up for Test Program Execution

To execute the test program, use the following hardware; do not connect the user system interface cable and user system.

- E6000 (HS2268EPI61H)
- Host computer
- The E6000 PC interface board which will be one of the following boards or card:  
Select one interface board from the following depending on the PC interface specifications.  
ISA bus interface board (HS6000EII01H)  
PCI bus interface board (HS6000EIC01H or HS6000EIC02H)  
PCMCIA interface card (HS6000EIP01H)

1. Install the E6000 PC interface board in the host computer and connect the supplied PC interface cable to the board.
2. Connect the PC interface cable to the E6000.
3. Connect the supplied AC adapter to the E6000.
4. Initiate the host computer to make it enter DOS prompt command input wait state.
5. Turn on the E6000 switch.



## 5.2 Diagnostic Test Procedure Using the Test Program

Insert the CD-R (HS2268EPI61SR supplied with the E6000) into the CD-ROM drive of the host computer by pressing the Shift key, move the current directory to <Drive>:\Diag with a command prompt, and enter one of the following commands according to the PC interface board used to initiate the test program:

1. ISA bus interface board (HS6000EII01H)  
> TM2268 –ISA (RET)
2. PCI bus interface board (HS6000EIC01H or HS6000EIC02H)  
> TM2268 –PCI (RET)
3. PCMCIA interface card (HS6000EIP01H)  
> TM2268 –PCCD (RET)

The HDI must be installed before the test program is executed.

Be sure to initiate the test program from <Drive>:\Diag. Do not initiate it from a directory other than <Drive>:\Diag, such as > <Drive>:\Diag\TM2268 –ISA (RET). If the test program is initiated when the current directory is not <Drive>:\Diag, the test program will not operate correctly.

When –S is added to the command line such as > TM2268 –ISA –S (RET), steps 1 to 20 will be repeatedly executed. To stop the execution, enter Q.

- Notes:
1. When the CD-R is inserted into the CD-ROM drive without pressing the Shift key, the HDI installation wizard is automatically started.  
In such a case, exit the HDI installation wizard.
  2. <Drive> is a drive name for the CD-ROM drive.
  3. Do not remove the CD-R from the CD-ROM drive during test program execution.

It will take about 3 minutes to execute the test program when the host computer using Windows®2000 runs at 1GMHz and the PCMCIA interface card is used. The following messages are displayed during the test.

Message	Description
E6000 H8S/2268 Emulator Tests Vx.x Copyright (c) 2001 Hitachi Ltd.	Test program start message. Vx.x shows the version number.
Loading driver .....OK (Use ISA) Initializing driver .....OK Searching for interface card .....OK	Shows that the PC interface board is correctly installed in the host computer.
Checking emulator is connected .....OK	Shows that the E6000 is correctly connected to the host computer.

Emulator Board Information:

Main Board ID: H'5

Shows the ID number of the lower board of the E6000 (always 5).

Emulation Board ID:H'0d

Shows the ID number of the middle board of the E6000 (always 0d).

SUB Board ID: H'6

Shows the ID number of the upper board of the E6000 (always 6).

1) Test Register

- A) IDR0 Register.....OK
- B) PAGE Register.....OK
- C) TRACE G/A Register.....OK
- D) PERFM G/A Register.....OK
- E) CES GA register .....OK
- F) IDR1 Register.....OK
- G) IDR2 Register.....OK

Shows the check results for the registers in the E6000 (normal completion).

2) Test DPRAM

- A) Decode Test .....OK
- B) Marching Test .....OK

Shows the results of decoding test and step test for the dual-port RAM in the E6000 (normal completion).

3) Test Firmware RAM

- A) Decode Test page[H'700 - H'71f] .....OK Shows the results of decoding test for the firmware RAM in the E6000 (normal completion).
  
- B) Marching Test page[H'700 - H'71f] .....OK Shows the results of step test for the firmware RAM in the E6000 (normal completion).

4) Test Trace memory

- A) Decode Test page[H'000 - H'04f](Lower 32K) ..OK Shows the results of decoding test for the trace RAM (first half) in the E6000 (normal completion).
  
- B) Marching Test page[H'000 - H'04f](Lower 32K) .OK Shows the results of step test for the trace RAM (first half) in the E6000 (normal completion).
  
- C) Decode Test page[H'000 - H'04f](Upper 32K) ..OK Shows the results of decoding test for the trace RAM (last half) in the E6000 (normal completion).
  
- D) Marching Test page[H'000 - H'04f](Upper 32K) .OK Shows the results of step test for the trace RAM (last half) in the E6000 (normal completion).

- 5) Test Map control memory
  - A) Decode Test      page[H'200 - H'27f] .....OK      Shows the results of decoding test for the mapping RAM in the E6000 (normal completion).
  
  - B) Marching Test    page[H'200 - H'27f] .....OK      Shows the results of step test for the mapping RAM in the E6000 (normal completion).
  
- 6) Test Internal ROM and RAM      Shows the results of
  - A) Decode Test      (Internal ROM) .....OK      decoding test and step
  - B) Marching Test    (Internal ROM) .....OK      test for internal ROM and
  - C) Decode Test      (Internal RAM) .....OK      RAM in the E6000
  - D) Marching Test    (Internal ROM) .....OK      (normal completion).
  
- 7) RESERVED
  
- 8) Test Emulation RAM STEP Operation      Shows the check results
  - A) Step Operation .....OK      for the step execution controlling circuits in the E6000 (normal completion).
  
- 9) Test Keybreak      Shows the check results
  - A) Key Break .....OK      for the forced break controlling circuits in the E6000 (normal completion).

- 10) Test Emulation RAM Hardware Break  
 A) GRD Break .....OK  
 B) WPT Break .....OK  
 C) WPT(ROM) Break .....OK
- Shows the check results for the illegal access break controlling circuits in the E6000 (normal completion).
- 11) Test Internal ROM Write-Protect  
 A) Write-Protect .....OK
- Shows the check results for the internal ROM write-protection controlling circuits in the E6000 (normal completion).
- 12) Test Hardware Break  
 A)Break Point Initialized .....OK  
 B)Event Detectors CES channel 1-12 ...OK  
 C)Test Sequencing 1 .....OK  
 D)Check Range Break .....OK  
 E)Range Break Test for Data .....OK  
 F)Check Compare Either .....OK
- Shows the check results for the hardware break control circuits in the E6000 (normal completion).
- 13) Test Emulation RAM Trace  
 A)Free Trace .....OK  
 B)Range Trace .....OK  
 C)Point to Point Trace .....OK  
 D)Start and Stop Event Trace .....OK  
 E)Trace memory Overflow .....OK  
 F)Time STAMP Trace (20MHz) .....OK  
 G)Time STAMP Trace (10MHz) .....OK  
 H)Time STAMP Trace (TEST mode).....OK
- Shows the check results for the trace controlling circuits in the E6000 (normal completion).
- 14) Test Runtime counter  
 A)Runtime counter (20.0MHz) .....OK  
 B)Runtime counter (10.0MHz) .....OK  
 C)Runtime counter (SUB:32.768kHz) ...OK
- Shows the check results for the run-time counter in the E6000 (normal completion).
- 15) Test Emulation Monitor  
 A)EMA23-EMA0 .....OK  
 B)ACST2-ACST0 .....OK  
 C)ASEST3-ASEST0 .....OK  
 D)ASEBRKACK .....OK  
 E)CNN .....OK  
 F)NOCLK,NOCLK2 .....OK  
 G)WINDOW .....OK  
 H)SUBACT .....OK  
 I)OTHER .....OK
- Shows the check results for the emulation monitor controlling circuits in the E6000 (normal completion).

- 16) Test PERFM G/A Shows the check results  
for the performance  
analysis controlling  
circuits in the E6000  
(normal completion).
  - A)Time Measure .....OK
  - B)RESERVED .....OK
  - C)Subroutine Count Measurement .....OK
  - D)Timeout Function (TIMOT Bit) .....OK
  - E)Timeout Function (TIMOP Bit) .....OK
  
- 17) Test Bus Monitor Shows the check results  
for the bus monitor  
controlling circuits in the  
E6000 (normal  
completion).
  - A) Register.....OK
  - B) Parallel RAM.....OK
  - C) SPRSEL2.....OK
  - D) RAM monitor.....OK
  
- 18) Test Parallel Access Shows the check results  
for the parallel access  
controlling circuits in the  
E6000 (normal  
completion).
  - A)Internal ROM Parallel Read Access(WORD) .....OK
  - B)Internal ROM Parallel Write Access(WORD) .....OK
  - C)Internal ROM Parallel Write Access(High Byte) .OK
  - D)Internal ROM Parallel Write Access(Low Byte) ..OK
  - E)Internal RAM Parallel Read Access(WORD) .....OK
  - F)Internal RAM Parallel Write Access(WORD) .....OK
  - G)Internal RAM Parallel Write Access(High Byte) .OK
  - H)Internal RAM Parallel Write Access(Low Byte) ..OK
  - I)RESERVED
  - J)RESERVED
  - K)RESERVED
  - L)RESERVED
  
- 19) Test H8S/2268 Register Read/Write Shows the check results  
for the register in the  
H8S/2268 series (normal  
completion).
  - A) Register Read.....OK
  - B) Register Decode Test.....OK
  - C) LCDRAM Marching Test.....OK
  - D) Register Reset.....OK
  - E) Medium-speed mode Register access.....OK
  
- 20) Test TMR\_4 Shows the check results  
for the TMR4 register  
(normal completion).
  - A) OVI4(Clock select PHI/8).....OK
  - B) OVI5(Clock select PHISUB/2).....OK
  - C) OVI6(Clock select PHI/8).....OK
  - D) OVI7(Clock select PHISUB/2).....OK
  - E) Exiting Watch Mode by OVI.....OK

Tests run for xH:xM:xS Shows the check time.

0 total errors Total number of errors.

Tests passed, emulator functioning correctly Shows that the E6000 is  
correctly operating.