# EVB-RTP100E2P6G1FL

Low-Voltage GaN RTP100E2P6G1FL

## Description

The EVB-RTP100E2P6G1FL evaluation board is a synchronous buck converter, which contains two Renesas low-voltage GaNs (RTP100E2P6G1FL) in a half-bridge configuration driven by Renesas gate driver. The low-voltage GaNs are 2.6mΩ 100V enhancement-mode Gallium Nitride (GaN) FET in a 5 × 6 FCLGA package. Its footprint is compatible with standard silicon counterparts. The RRP68150 gate driver is a high-frequency, half-bridge driver designed specifically for enhancement mode GaN FETs.

The buck converter has a DC48V input, a DC12V output, a maximum output power of 330W, and operates between 250kHz and 500kHz switching frequencies. The dimension of the evaluation board is 53 × 53 mm.

The evaluation board allows users to evaluate the electrical performance of the Renesas low-voltage GaN, including how to optimize the circuit board to enable a high-efficiency and high-power density board capable of operating at high frequencies. The board has some test points for easy measurement of the low-voltage GaN switching waveforms and energy efficiency.

## Features

- Highly flexible and user-friendly buck converter evaluation board
- Performance testing of the Renesas low-voltage GaN over a wide range of Vin, Vout, Fsw, and Pout
- Experience system performance using Renesas gate driver, RRP68150

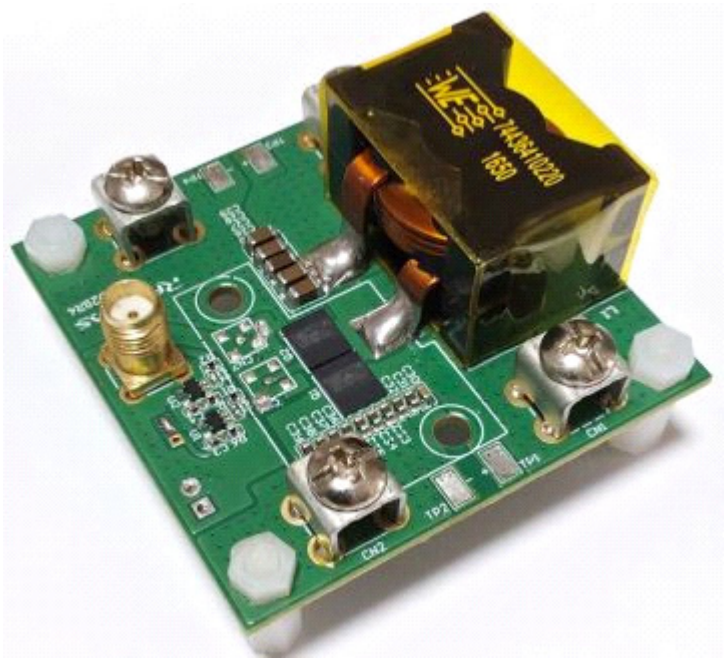


**Figure 1. EVB-RTP100E2P6G1FL Evaluation Board**


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# 1. Functional Description

## 1.1 Overview

The evaluation board's circuitry is divided into four parts as shown in Figure 3. The first part is a DC5V regulator, which provides a stable and accurate DC5V voltage to the PWM and gate drive circuits. The second part is the PWM and dead-time control circuits. It converts the single square wave signal provided by the signal generator into two independent signals to drive the high-side and low-side GaNs, while adding an appropriate dead time to prevent shoot-through. The third part is the gate driver, which provides 2A sourcing and 5.3A sinking peak current for the GaN devices switching. The last part is the power stage (two GaN devices RTP100E2P6G1FL, an inductor, and some input/output capacitors), which is the core part of the entire board, and is responsible for converting DC48V to DC12V.



Figure 2. EVB-RTP100E2P6G1FL

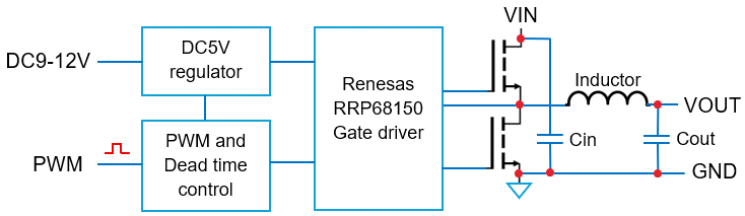



Figure 3. Block Diagram of the Buck Converter

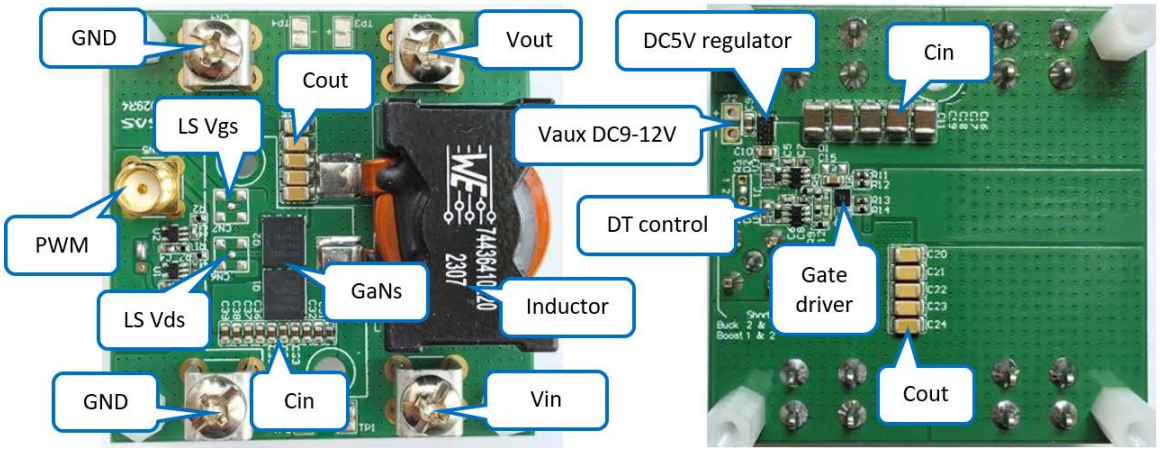



Figure 4. Top (Left) and Bottom (Right) Views

Table 1. EVB Product Specification

| | |
|---|---|
| Input (V) | DC48V typical – DC80V (80% GaN-FET rated voltage) |
| Output (V) | DC12V typical – DC16V (Maximum output capacitor rated voltage) |
| Output (A) | 28A maximum |
| Switching Frequency | 250kHz – 500kHz |
| Auxiliary Power Supply | DC9V – 12V |
| Renesas GaN FET | RTP100E2P6G1FL |
| Renesas Gate Driver | RRP68150 |

## 1.2 Renesas GaN FET (RTP100E2P6G1FL)

The RTP100E2P6G1FL 100V, 2.6mΩ is an enhancement mode Gallium Nitride (GaN) FET in a 5 × 6 mm FCLGA package using Renesas' Gen I REXGaN® platform. Using advanced packaging technology, these devices deliver high-speed switching and enhanced thermal performance. Designed with footprint compatibility to standard silicon counterparts, the devices simplify the transition to GaN technology.

Features:

- Ultra-fast switching E-mode GaN HEMT
- JEDEC-qualified GaN technology
- Package footprint compatible to Si counterpart
- Low static losses
- Simplified thermal design
- Zero reverse recovery charge
- Low gate charge and output charge

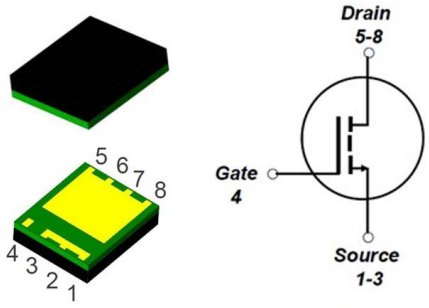



**Figure 5. RTP100E2P6G1FL and Schematic Symbol**

| | |
|---|---|
| $V_{DS}$ (V) | 100 |
| $R_{DS(ON)}$ (mΩ) Typical | 2.6 |
| $Q_{OSS}$ (nC) | 46 |
| $Q_G$ (nC) | 9.4 |
| $Q_{rr}$ (nC) | 0 |

## 1.3 Renesas Gate Driver (RRP68150)

The RRP68150 gate driver is a 5V-powered, high-frequency half-bridge driver for enhancement mode GaN FETs and low-threshold N-channel MOSFETs. It features 2A source and 5.3A sink current capability with its switching node supporting up to 100V DC. The driver's PWM inputs are 3.3/5V CMOS logic-compatible and can tolerate input voltages up to 14V, independent of the VDD supply voltage. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.4V. This clamping action prevents the gate voltage from exceeding the maximum gate-source voltage rating of the GaN FET. Its 5V operational supply enables convenient supply sharing with the controller.

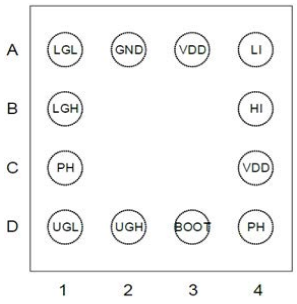



**Figure 6. Pin Assignments WLCSP12-2x2 – Top View**

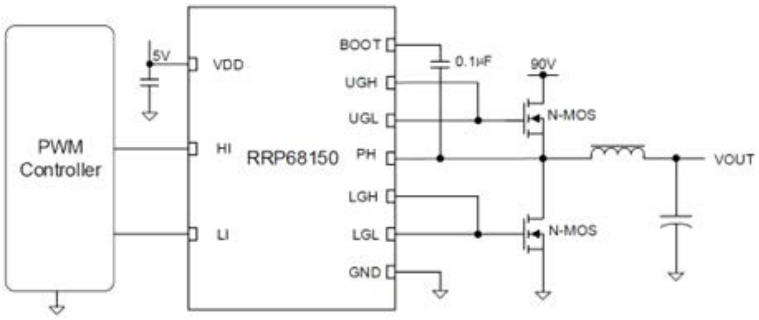



**Figure 7. Typical Application**

# 2. Board Features

## 2.1 Input PWM Signal

The evaluation board requires an input PWM signal to set the switching frequency and adjust the duty cycle to obtain the desired output voltage value. The PWM signal must be a square waveform, 0V for low-level signal and 5V (maximum 6.5V) for high-level signal. The input signal is connected to connector CN5. Figure 8 shows the connector (Type SMA-KE) and Figure 9 is an example of the PWM signal.

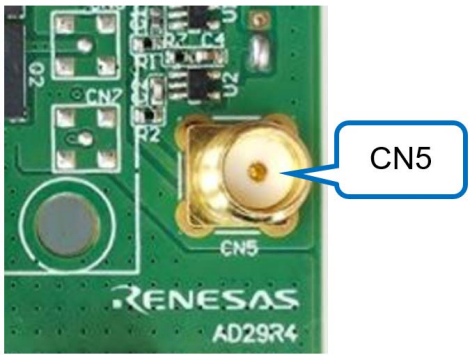



**Figure 8. SMA-KE Connector**

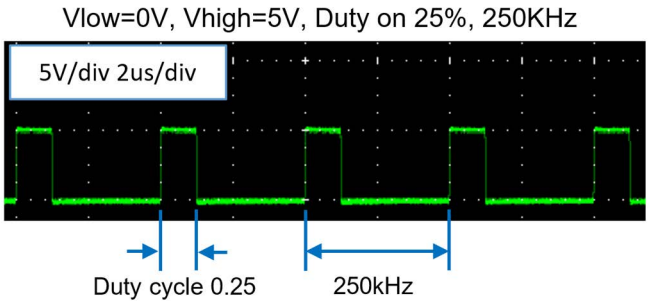



**Figure 9. Input PWM Signal**

## 2.2 Duty Cycle

The evaluation board is a buck converter, so the duty cycle can be calculated using the following formula. As the input voltage is DC48V, output voltage is DC12V. The calculated duty cycle is 0.25. In real applications, the actual duty cycle is higher than the calculated value due to power loss. To adjust the duty cycle, set the other output voltages within 0 to 16V (16V is the maximum output capacitor rated voltage).

$$D = \frac{V_{out}}{V_{in}}$$

## 2.3 Dead Time

Synchronous buck converters consist of high-side and low-side GaNs. If the dead time is not set correctly, it may lead to a shoot-through. To prevent this, set a reasonable time according to the GaN FET's switching behavior and PCB layout optimization. If the design is correct, it is recommended to set the dead time between 5ns and 15ns. It can effectively reduce the power loss without shoot-through.

Resistor R3 sets the dead time of the high-side GaN FET, and resistor R4 sets the dead time of the low-side GaN FET (see Figure 10 and Figure 11). The required resistance value can be calculated using the formula in the figure.

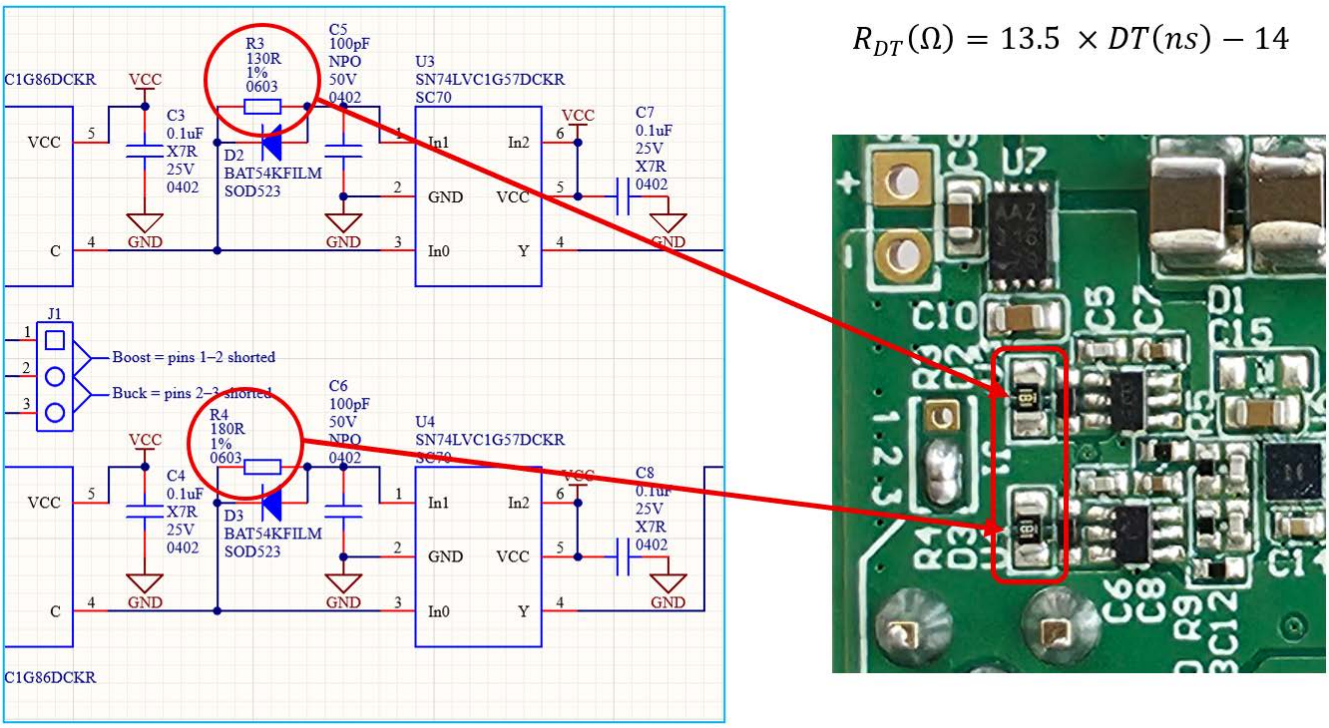



**Figure 10. Resistors R3 and R4**

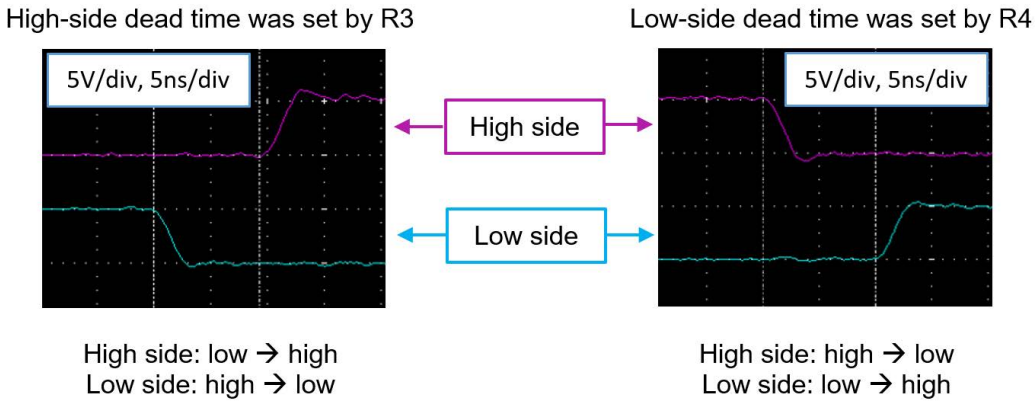



**Figure 11. Resistor R3 and R4 Dead Time**

## 2.4 Split-Gate Output

The gate driver on the evaluation board features split-gate outputs with strong sink capability, enabling independent control of turn-on and turn-off drive strength for optimized switching performance. In the schematic diagram in Figure 12, resistors R11 and R12 control the on/off state of the high-side GaN Q1, while R13 and R14 control the on/off state of the low-side GaN Q2.

Users can adjust these four resistor values according to the buck converter's design parameters, such as switching frequency, input/output voltage values, and output power level, to control the drain-source voltage and gate-source voltage overshoot issues of the GaN FET.

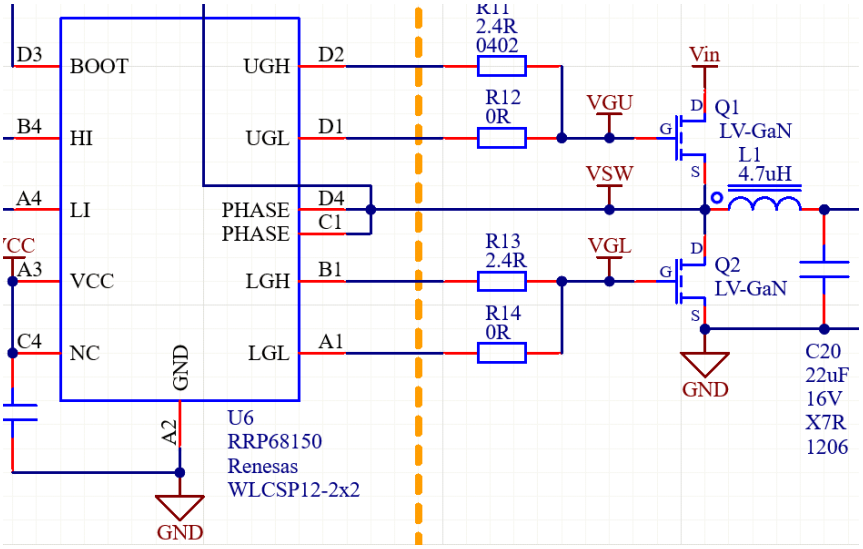



**Figure 12. Gate Drive Resistors**

# 3. Test Setup

## 3.1 Setup Procedure

1. Turn off the power before connecting any device.
2. Connect a signal generator to SMA-KE connector CN5 as shown in item 1 of Figure 13.
3. Connect a DC9V–12V power supply with a current limit of 0.5A to terminal J2 as shown in item 2.
4. Connect a DC48V power supply with a current limit of 9A to connectors CN1(+) and CN2(-) as shown in item 3.
5. Connect a DC voltage meter to TP1(+) and TP2(-) to measure input voltage as shown in item 4.
6. Connect an electronic load to connectors CN3(+) and CN4(-) for output load current measurement and TP3(+) and TP4(-) for output voltage measurement as shown in item 5.

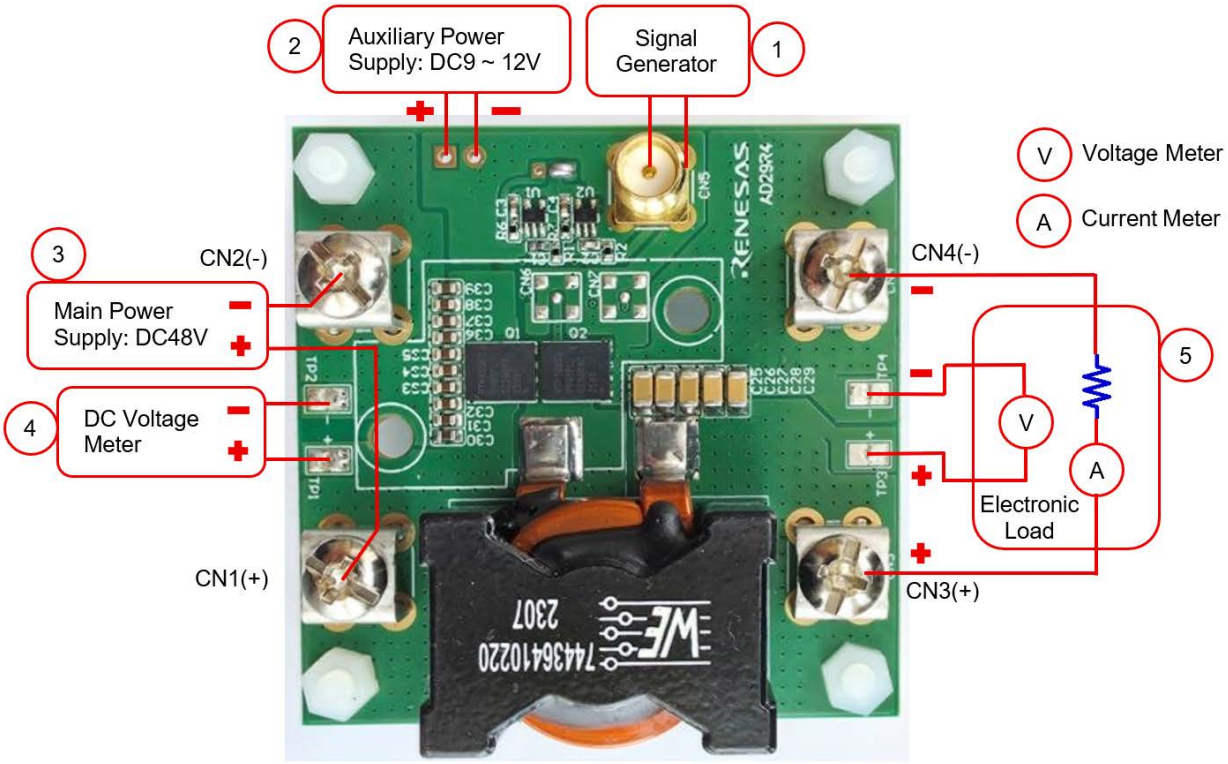



**Figure 13. Setup Key**

7. Place an axial fan (NMB: 4710PS-22T-B30) 13cm from the evaluation board and provide an air flow of 63.5 CFM as shown in item 6 of Figure 14.

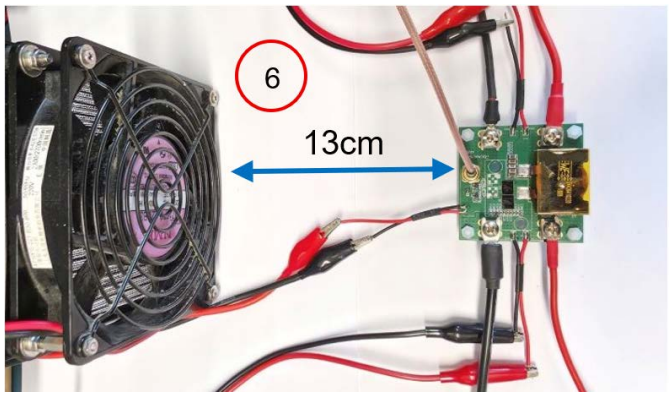



**Figure 14. Axial Fan Airflow**

## 3.2 Power-On Procedure

1. Complete the Setup Procedure.
2. Set up the PWM signal on the signal generator as shown in Figure 15, then turn on the PWM signal to the board.
   - Square wave
   - Vlow: 0V
   - Vhigh: 5V (typ), 6.5V (max)
   - Duty cycle: 0.25
   - Switching frequency: 250kHz

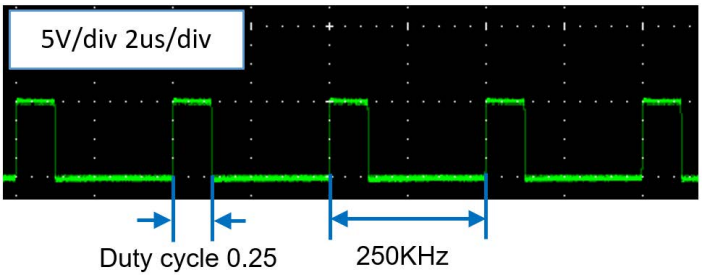



**Figure 15. PWM Signal**

3. Turn on the auxiliary power supply and adjust the output voltage to DC9V or DC12V. The Vgs voltage waveform of the low-side GaN FET Q2 is shown in Figure 16.

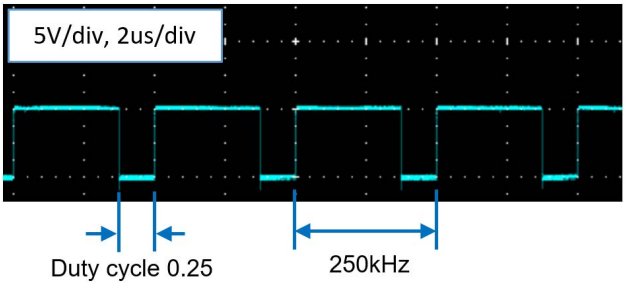



**Figure 16. Vgs Voltage Waveform**

There are two methods for measuring the Vgs switching waveform. The first method is to directly measure the component traces using a passive probe as shown in Figure 17. Use a spring clip to get a small ground loop. The second method is to measure the switching waveform using the MMCX jack at CN7 as shown in Figure 18 (the jack at CN7 is not provided).

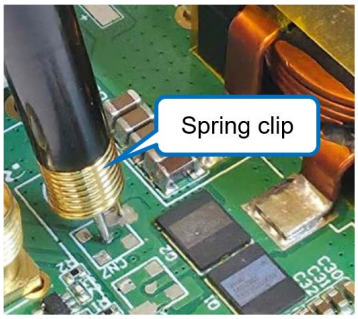



**Figure 17. Passive Probe**

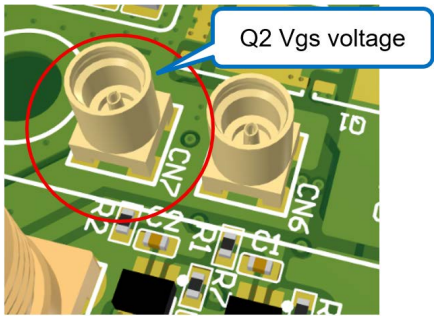



**Figure 18. MMCX Jack**

4. Making sure the initial main power supply voltage is 0V, turn on the power and slowly increase the voltage to DC48V. The Vds voltage waveform of the low-side GaN FET Q2 is shown in the Figure 19. The same methods can be used to measure the Vds voltage at Q2 as shown in Figure 20 and Figure 21.

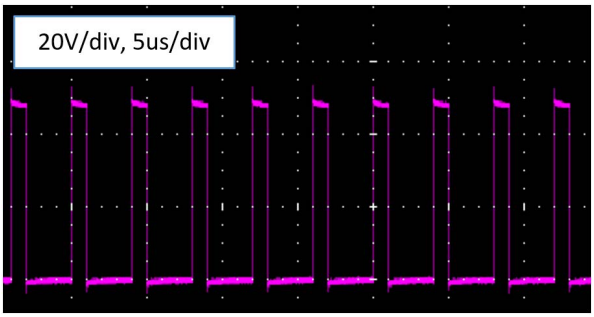



**Figure 19. Vds Voltage Waveform**

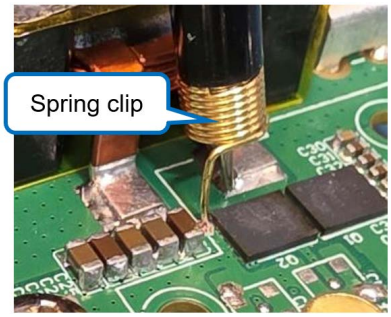



**Figure 20. Passive Probe**

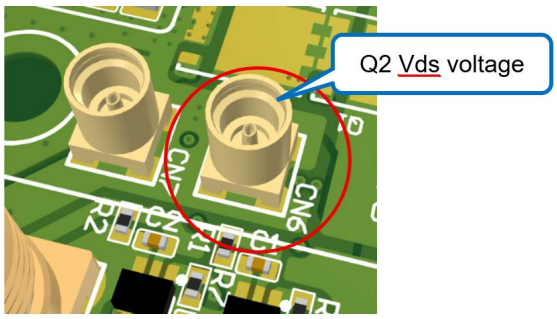



**Figure 21. MMCX Jack**

5. When the output voltage of the buck converter reaches DC12V, the output load current can be increased gradually to check the switching behavior, energy efficiency, and other parameters.
6. For the shut-down procedure, follow the steps in reverse.

# 4. Test Results

## 4.1 Energy Efficiency and Power Loss

Test conditions:

- Input voltage was measured at TP1(+) and TP2(-).
- Output voltage was measured at TP3(+) and TP4(-).
- The energy efficiency was tested at an airflow of 63.5 CFM.
- The distance between evaluation board and axial fan is 13cm.

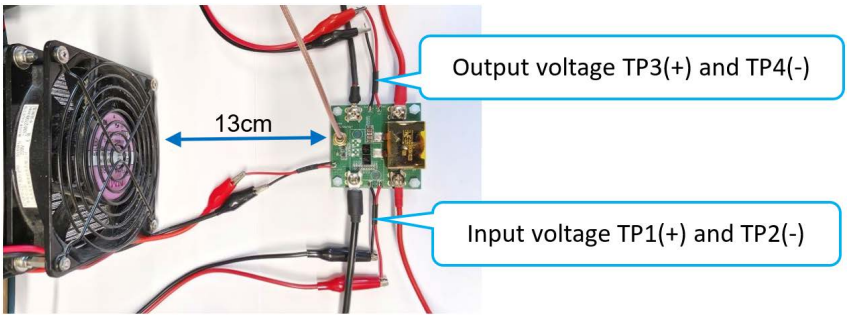



**Figure 22. Axial Fan Layout**

Figure 23 and Figure 24 show the energy efficiency and power loss results of the circuit board at three different switching frequencies (250kHz, 350kHz, 500kHz). Input voltage is DC48V. Output voltage is DC12V. Output current is 28A maximum. Inductor is 2.2µH Wurth 74436410220.

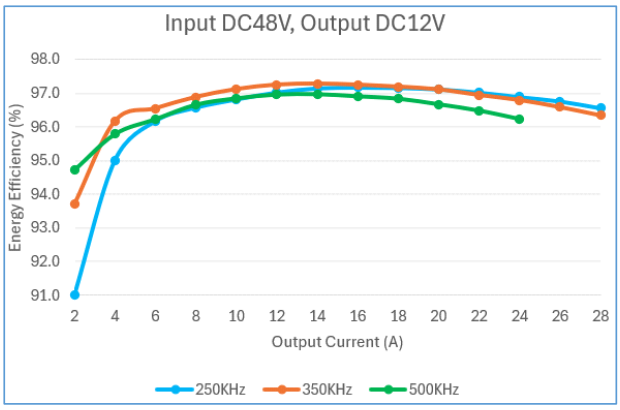



**Figure 23. Energy Efficiency at Different Output Currents and Switching Frequencies**

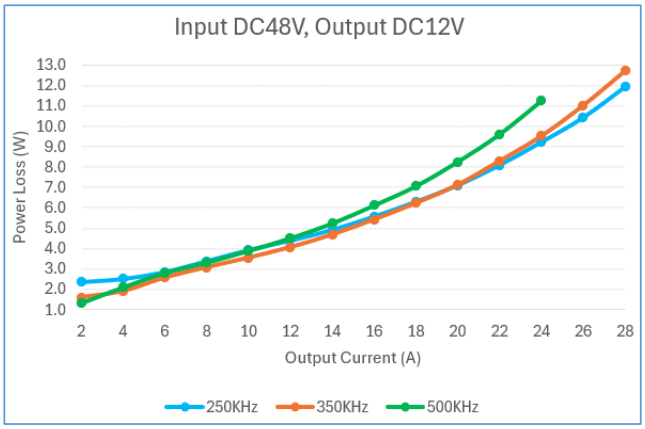



**Figure 24. Power Loss at Different Output Currents and Switching Frequencies**

## 4.2 Thermal Performance

Table 2 shows the maximum output current that the GaNs can achieve at around 100°C, with and without airflow, and at different switching frequencies. Thermistors were used to test the temperature of the components.

**Table 2. Component Temperature**

| Switching Frequency | No Axial Fan | | | | Axial Fan NMB: 4710PS-22T-B30, CFM 63.5 | | | |
|---|---|---|---|---|---|---|---|---|
| | Max. OP Current | Component Temp. at 25˚C | | | Max. OP Current | Component Temp. at 25˚C | | |
| | | HS GaN | LS GaN | L1 | | HS GaN | LS GaN | L1 |
| 250kHz | 19.0A | 99.0˚C | 99.5˚C | 84.4˚C | 29.5A | 98.9˚C | 98.6˚C | 59.0˚C |
| 500kHz | 14.8A | 103.0˚C | 90.3˚C | 70.4˚C | 23.0A | 101.2˚C | 84.7˚C | 49.7˚C |

Figure 25 shows the measurement location. An axial fan was used in the thermal test the same test setup as measuring the energy efficiency.

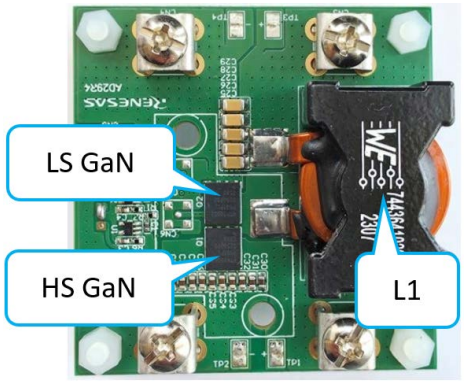



**Figure 25. Measurement Location**

## 4.3 Switching Node Voltage Waveforms

Figure 26 shows the switching node waveforms (low-side GaN Q2 Vds voltage) at an input of DC48V, an output of DC12V 28A, and a switching frequency of 250kHz. The Vds voltage was measured 55.8Vpeak, which is far away from the maximum rating of 100V Vdss voltage. Another important value is slew rate. It must be optimized so that you can balance between the efficiency and the EMI compliance.

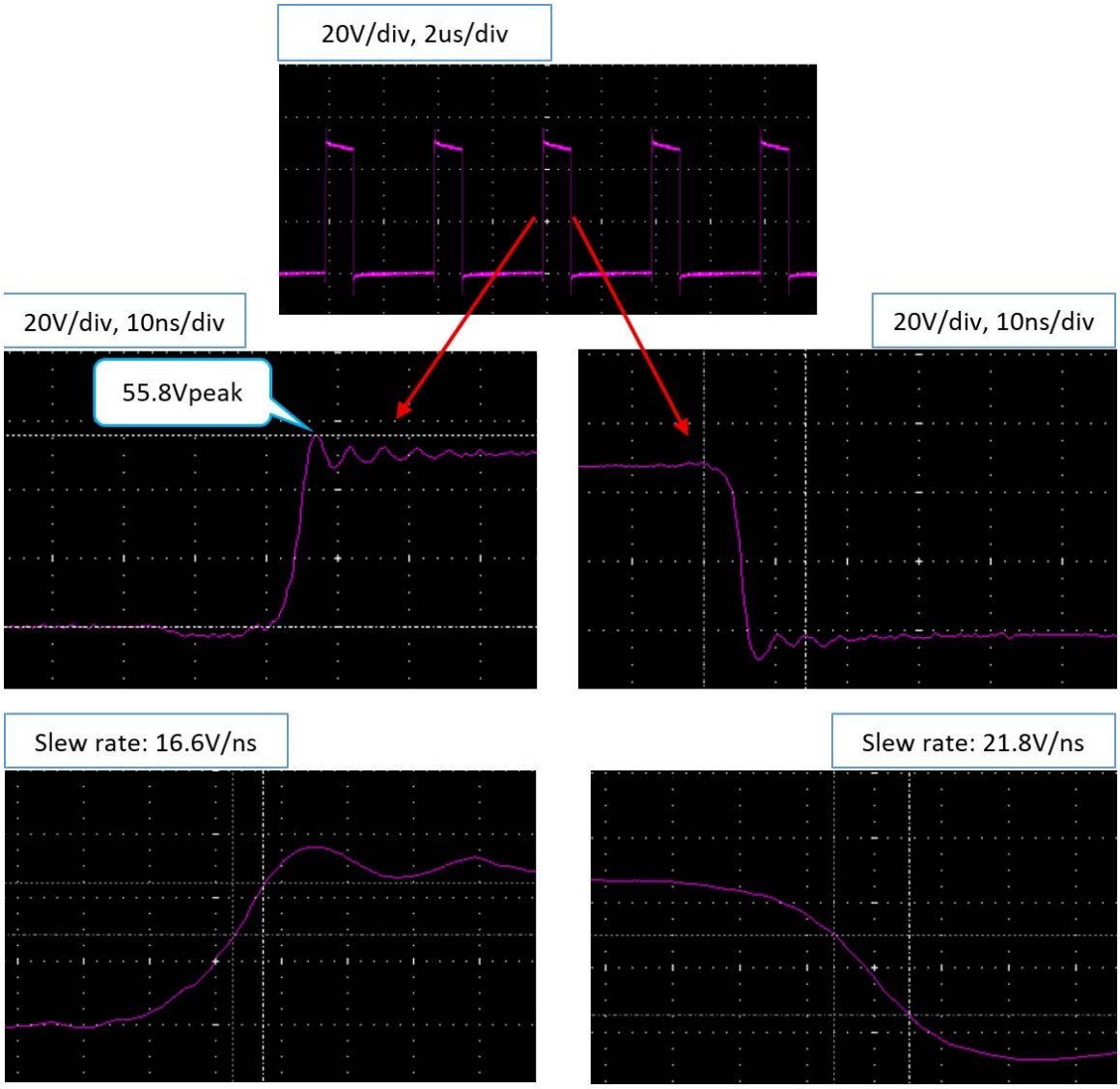



**Figure 26. Switching Node Waveforms**

# 5. Board Design

## 5.1 Board Schematic

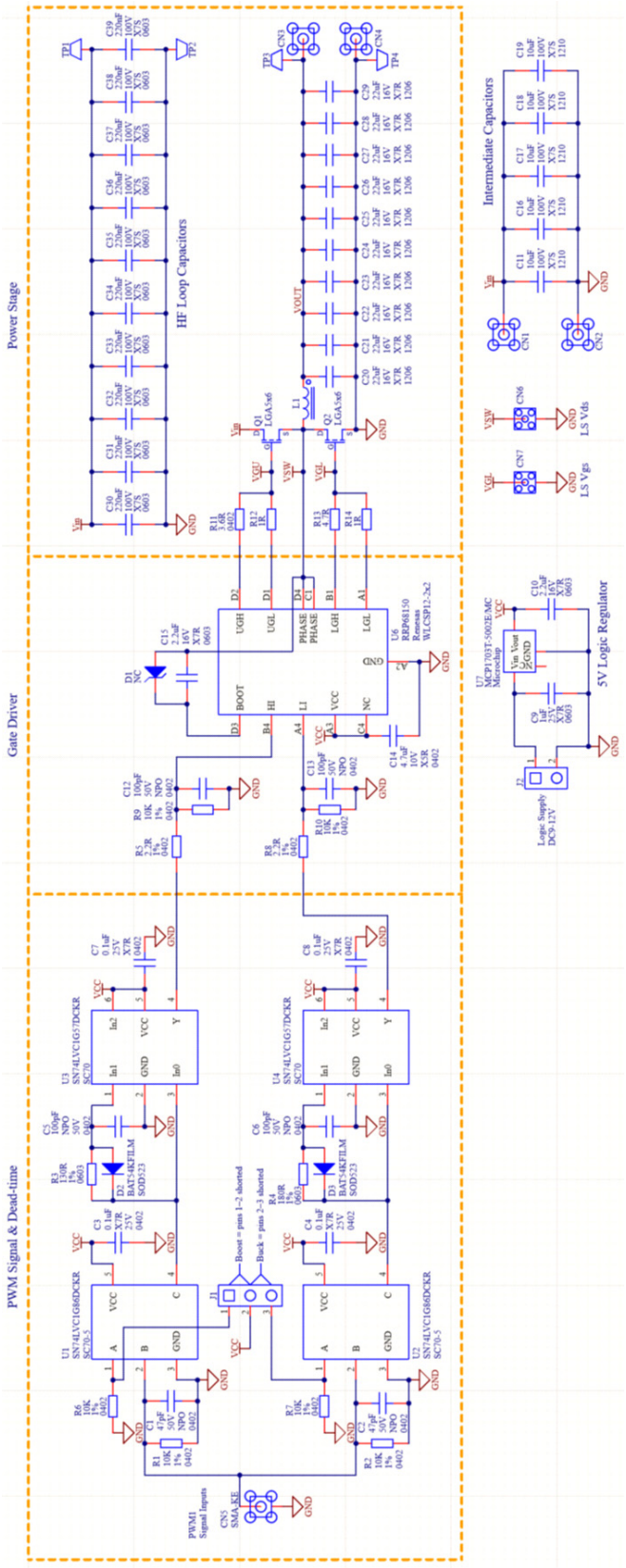



**Figure 27. Board Schematic**

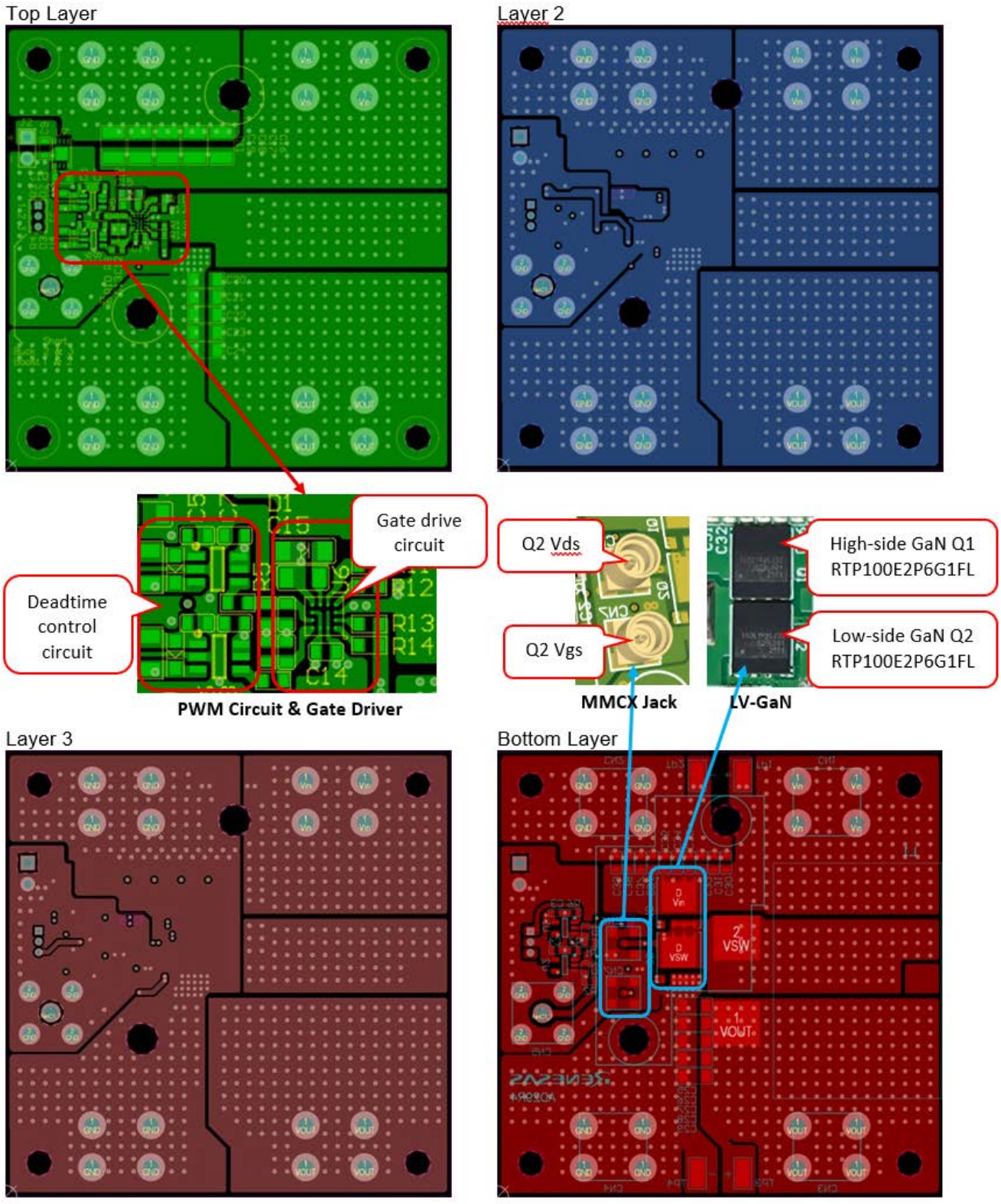



**Figure 28. PCB Layout**

PCB specification:

- PCB file name: AD29R4
- Size: 53 × 53 mm.
- Thickness: 1.6mm
- Material: FR4, 2oz for all layers

## 5.2 Bill of Materials

**Table 3. Bill of Materials**

| Item | Qty | Reference | Part Description | Manufacturer | Part Number |
|---|---|---|---|---|---|
| 1 | 2 | C1, C2 | 47pF, 50V, NPO, 0402 | | |
| 2 | 4 | C3, C4, C7, C8 | 0.1uF, 25V, X7R, 0402 | | |
| 3 | 4 | C5, C6, C12, C13 | 100pF, 50V, NPO, 0402 | | |
| 4 | 1 | C9 | 1uF, 25V, X7R, 0603 | | |
| 5 | 1 | C10 | 2.2uF, 16V, X7R, 0603 | | |
| 6 | 1 | C14 | 4.7uF, 10V, X5R, 0402 | | |
| 7 | 1 | C15 | 2.2uF, 16V, X7R, 0603 | | |
| 8 | 5 | C11, C16, C17, C18, C19 | 10uF, 100V, X7S, 1210 | | |
| 9 | 10 | C20, C21, C22, C23, C24, C25, C26, C27, C28, C29 | 22uF, 16V, X7R, 1206 | | |
| 10 | 10 | C30, C31, C32, C33, C34, C35, C36, C37, C38, C39 | 220nF, 100V, X7R, 0603 | | |
| 11 | 4 | CN1, CN2, CN3, CN4 | Connector | Keystone | 7701 |
| 12 | 1 | CN5 | Connector | Kinghelm | KH-SMA-KE-Z |
| 13 | 0 | CN6, CN7 | MMCX Jack | Molex | 734152063 |
| 14 | 2 | D2, D3 | 40 V 30 mA | ST | BAT54KFILM |
| 15 | 1 | L1 | 2.2uH | Wurth | 74436410220 |
| 16 | 2 | Q1, Q2 | 100V, 2.6mΩ, LV-GaN | Renesas | RTP100E2P6G1FL |
| 17 | 6 | R1, R2, R6, R7, R9, R10 | 10K, 1%, 0402 | | |
| 18 | 1 | R3 | 130Ω, 1%, 0603 | | |
| 19 | 1 | R4 | 180Ω, 1%, 0603 | | |
| 20 | 2 | R5, R8 | 2.2Ω, 5%, 0402 | | |
| 21 | 1 | R11 | 3.6Ω, 1%, 0402 | | |
| 22 | 2 | R12, R14 | 1Ω, 0402 | | |
| 23 | 1 | R13 | 4.7Ω, 1%, 0402 | | |
| 24 | 2 | U1, U2 | SN74LVC1G86DCKR | TI | SN74LVC1G86DCKR |
| 25 | 2 | U3, U4 | SN74LVC1G57DCKR | TI | SN74LVC1G57DCKR |
| 26 | 1 | U6 | 100V, 2A Source, 5.3A Sink, 5V-Powered High-Frequency GaN/MOSFET Half-Bridge Drivers with Anti-Shoot-Through Protection | Renesas | RRP68150 |
| 27 | 1 | U7 | 5.0 V 250 mA DFN | Microchip | MCP1703T-5002E/MC |
| 28 | 1 | PCB | Size: 53x53mmx1.6mm, 4 layers, 2oz | JDB | AD29R4 |
| 29 | 4 | M1, M2, M3, M4 | M3*10+6, Nylon, Hex Standoff, White | | |
| 30 | 0 | D1, J1, J2, | No components | | |
| 31 | 0 | TP1, TP2, TP3, TP4 | No components | | |

# 6. Ordering Information

| Part Number | Description |
|---|---|
| EVB-RTP100E2P6G1FL | Low-voltage GaN RTP100E2P6G1FL Evaluation Board |

# 7. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.01 | Oct 13, 2026 | Updated Figure 4. |
| 1.00 | Sep 2, 2026 | Initial release |

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