

RX64M Group

Renesas Starter Kit+ User's Manual
For e² studio

RENESAS MCU
RX Family / RX600 Series

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The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK+ hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK+ platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK+ and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RX64M Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	RSK+RX64M User's Manual	R20UT2593EG
Tutorial Manual	Provides a guide to setting up RSK+ environment, running sample code and debugging programs.	RSK+RX64M Tutorial Manual	R20UT2594EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample, on a single A4 sheet.	RSK+RX64M Quick Start Guide	R20UT2595EG
Code Generator Tutorial	Provides a guide to code generation and importing into the e ² studio IDE.	RSK+RX64M Code Generator Tutorial Manual	R20UT2930EG
Schematics	Full detail circuit schematics of the RSK+.	RSK+RX64M Schematics	R20UT2589EG
User's Manual: Hardware	Provides technical details of the RX64M microcontroller.	RX64M Group User's Manual: Hardware	R01UH0377EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	Bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
E1	Renesas On-chip Debugging Emulator
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electrostatic Discharge
I ² C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not applicable
n/c (NC)	Not connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification (Link valid at 26Jun2013)
POE	Port Output Enable
RAM	Random Access Memory
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TFT	Thin Film Transistor
TPU	Timer Pulse Unit
USB	Universal Serial Bus
WDT	Watchdog timer

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1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK+ hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK+ board contains all the circuitry required for microcontroller operation.

1.3 Board specification

Board specification was shown in **Table 1-1** below.

Item	Specification
Microcontroller	Part No : R5F564MLCDFC
	Package : 176-pin LQFP
	On-Chip Memory : ROM 4MB+64KB, RAM 512KB+32KB+8KB
On-Board Memory	SDRAM (MT48LC8M16A2P-6A) : 128Mbit
	I ² C EEPROM (R1EX24016ASAS0G) : 16Kbit
	SPI Serial Flash (MX25L3235EM2I-10G) : 32Mbit x 2
Input Clock	RX64M Main : 24MHz
	RX64M Sub : 32.768kHz
	RL78/G1C Main: 12MHz
	Ethernet PHY (for MII) : 25MHz
	Ethernet PHY (for RMII) : 50MHz
Power Supply	DC Power Jack : 5 V Input
	Power Supply IC : RAA230214 (5V Input, 3.3V Output DC/DC Converter + LDO)
Coin Cell Holder	CR2032 Coin Cell Holder for Battery Backup Function
Debug Interface	E1 14-pin box header
DIP Switch	Mode Configuration : 4-pole x 1
	Function Configuration : 10-pole x 5
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer(for ADC)	Single-turn, 10kΩ
LED	5V Power indicator: green x 1
	3.3V Power Indicator : green x 1
	User : green x 1, orange x 1, red x 2
	Ethernet Status: green x 4, yellow x 2
Ethernet *1	Connector : RJ45 x 2
	PHY : uPD60620 (Dual Channel PHY)
SDHI *2	SD Card Slot (4-bit) x 1
CAN	Connector : 2.54mm pitch, 3-pin x 1
	Driver : R2A25416SP (ISO-11898-2 compliance, support for high-speed communication of 1Mbps (max))
USB	USB0-Function : USB-MiniB
	USB0-Host : USB-TypeA
	USBA-Function : USB-MiniB
	USBA-Host : USB-TypeA
USB to Serial Converter Interface	Connector : USB-MiniB
	Driver : RL78/G1C Microcontroller (Part No R5F10JBCANA)
Pmod	PMOD1 (for LCD) : Angle type, 12-pin Connector
	PMOD2 (spare) : Straight type, 12-pin Connector
PDC Interface *3	2.54 mm pitch, 20-pin x 1 (J26)
SSI Interface *3	2.54 mm pitch, 12-pin x 1 (J25)
LCD Direct Drive Interface *3	2.54 mm pitch, 50-pin x 1 (TFT)
Application Board Interface *3	2.54mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

Table 1-1: Board specification

*1. The uPD60620 is non-promotion device. Please do not refer Ethernet circuit of this board for your target system design.

*2. The RX64M Group incorporates an SD host interface (SDHI) which is compliant with the SD Specifications. When developing host devices that are compliant with the SD Specifications, the user must enter into the SD Host/Ancillary Product License Agreement (SD HALA).

*3. The connector is not included to a product.

2. Power Supply

2.1 Requirements

An E1 emulator is able to power the RSK+ board with up to 200mA. When the board is connected to another system then that system should supply power to the board. This board have an optional centre positive supply connector using a 2.0mm barrel power jack.

This RSK+ board supports one external voltage input. Details of the external power supply connection are shown in **Table 2-1** and **Table 2-2** below.

Connector	Supply voltage
PWR	Input 5VDC

Table 2-1: PWR connector Requirements

There are RSK products which supports the 12V voltage input. Since this board is supporting the 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally. Moreover, the main power supply connected to PWR should supply a minimum of 10W to ensure full functionality.

Supply Source	Regulator IC Output
PWR connector /EXT_BATT/VBUSA/VBUS0/CON_5V/Unregulated_VCC	3.3V
CON_3V3	None

Table 2-2: Main Power Supply Requirements

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the 'Release' or stand-alone code from the example tutorial software pre-programmed into the Renesas microcontroller. On powering up the board the LCD panel will show 'RSK+RX64M', 'Tutorial' and 'Press Any Switch' in the bottom left and will respond to any switch press by performing an A/D conversion and displaying the result in the main part of the LCD panel.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

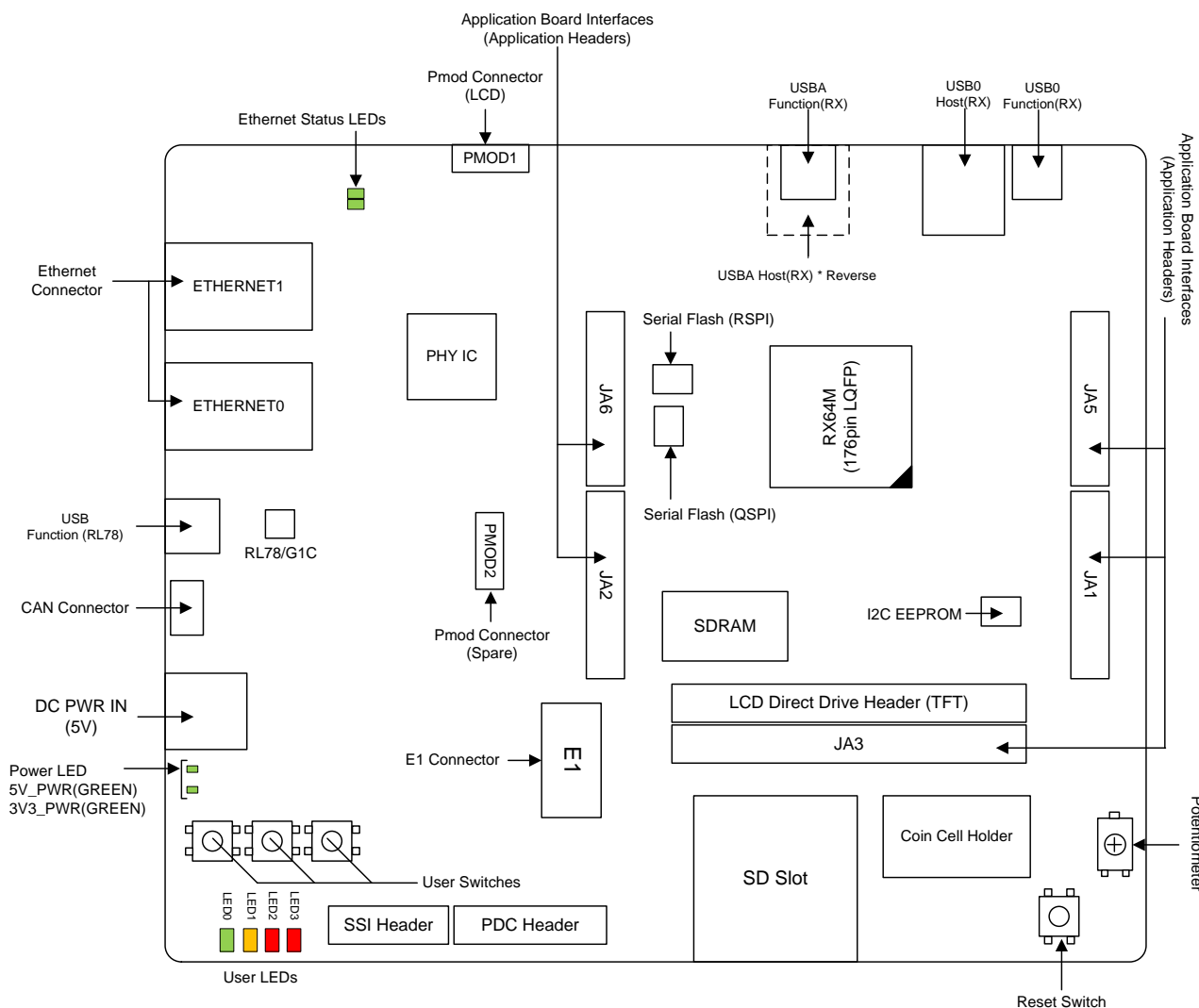


Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.

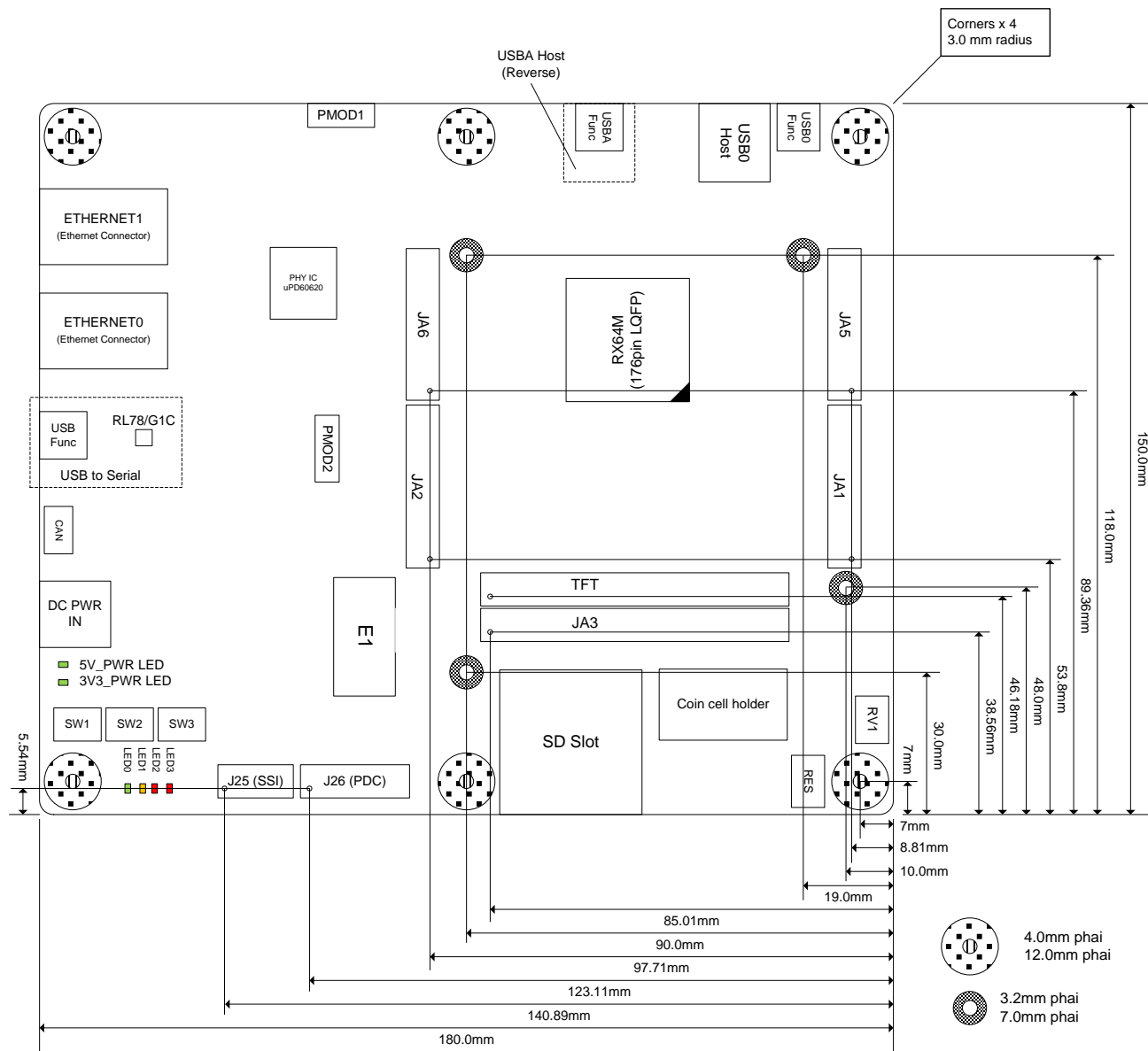


Figure 3-2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB – bottom-side component placement can be seen in Figure 3-4. Component types and values can be looked up using the board schematics.

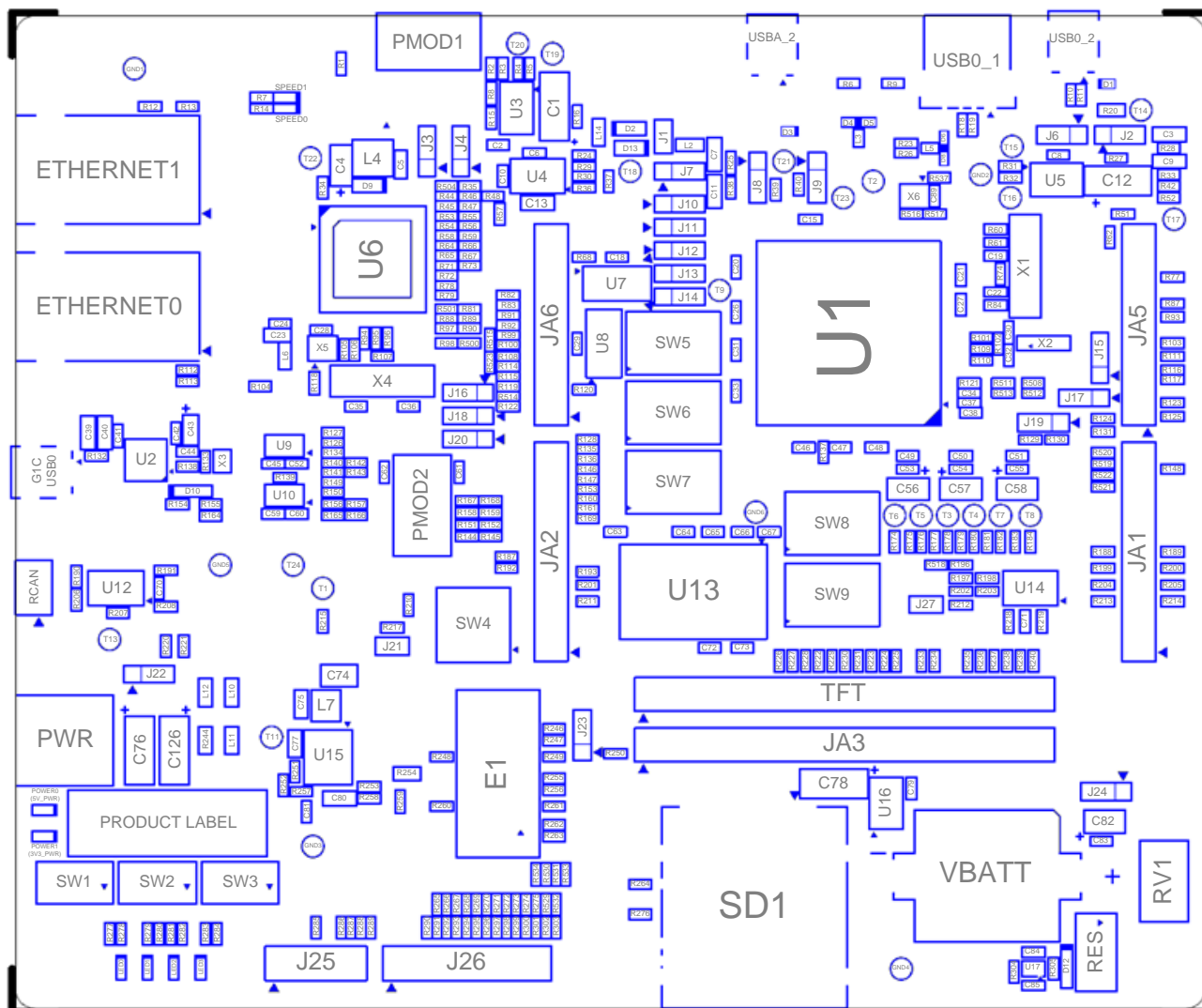


Figure 3-3: Top-Side Component Placement

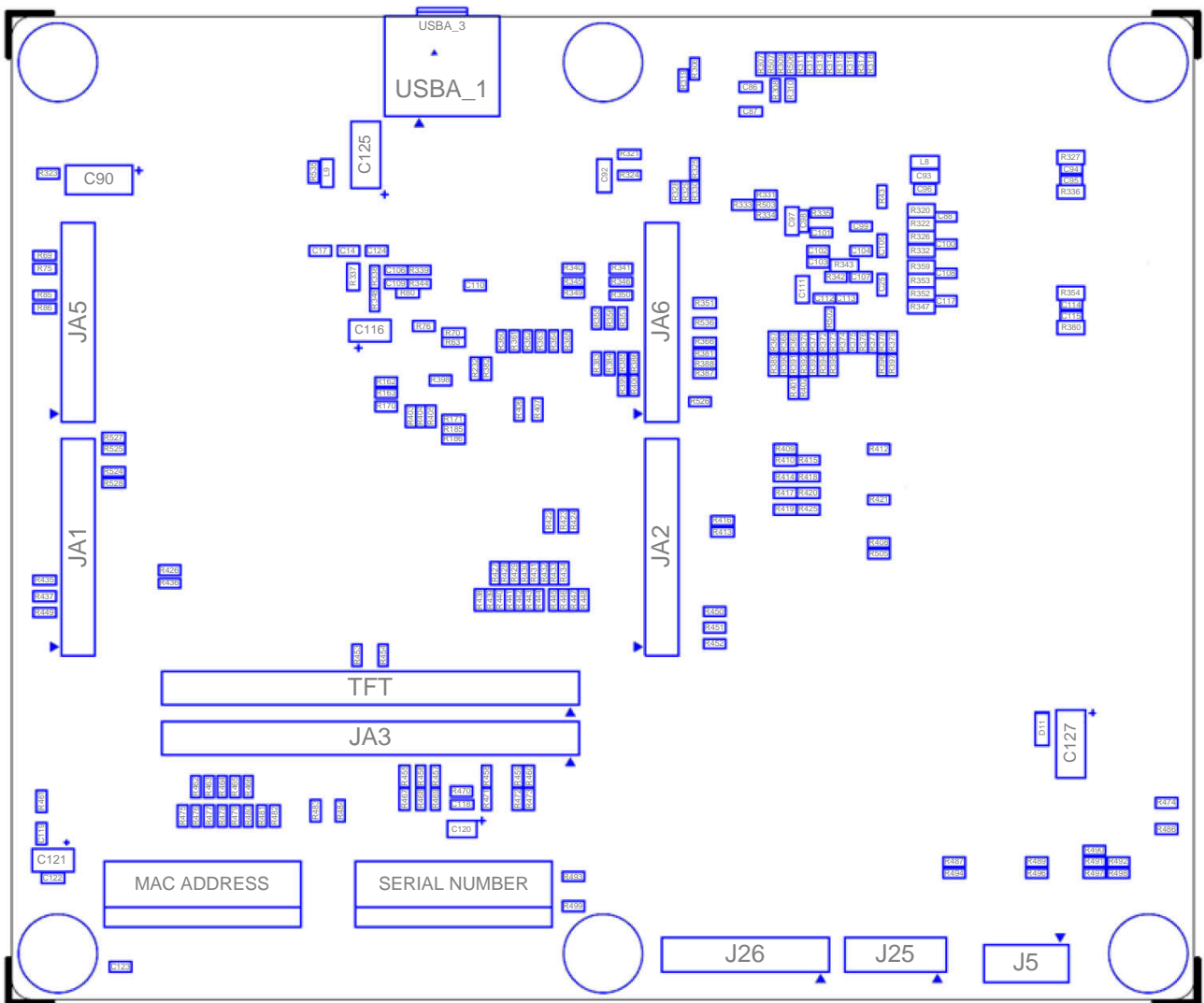


Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal RSK+ Connections

The diagram below shows the RSK+ board components and their connectivity to the MCU.

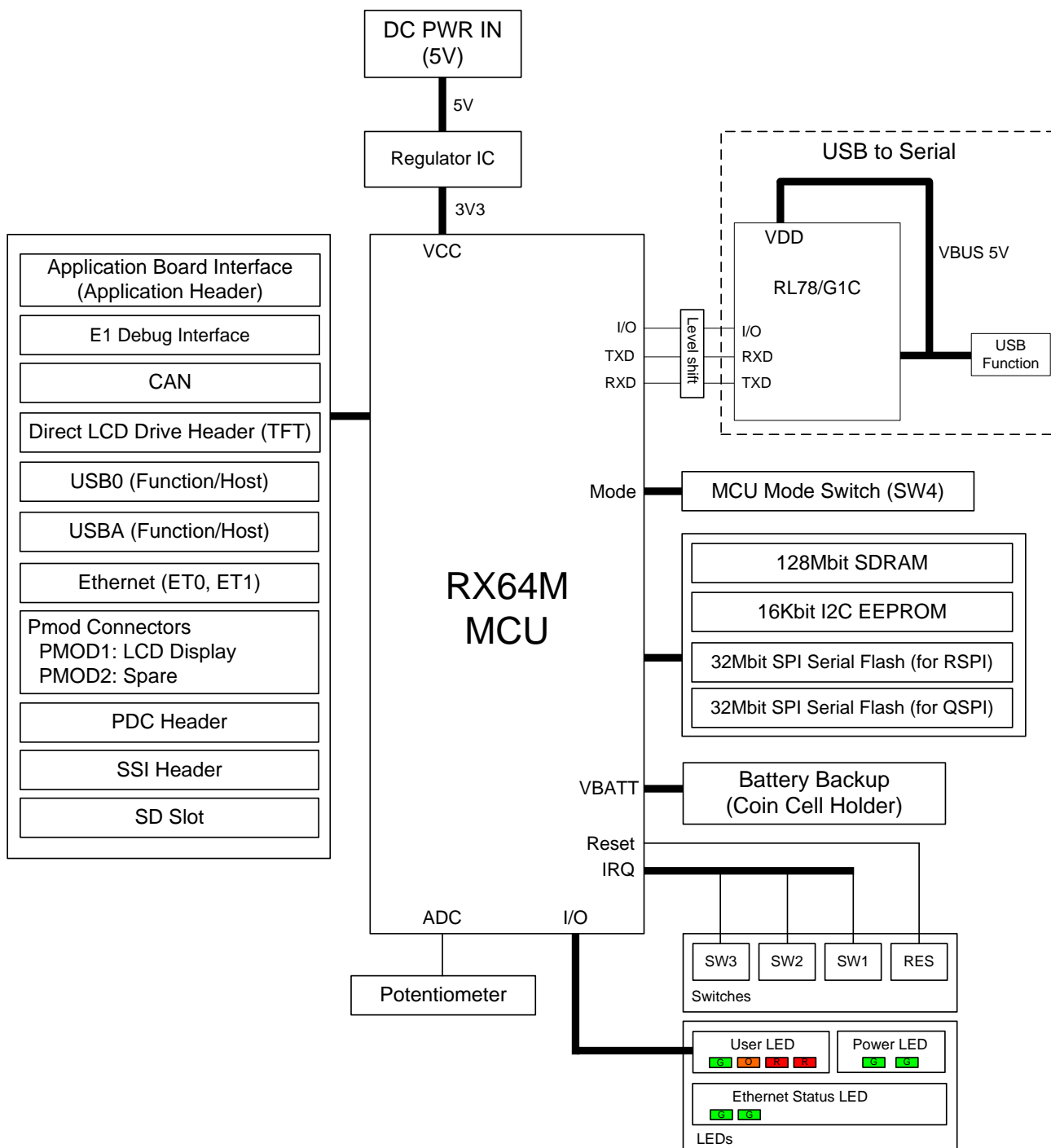


Figure 4-1: Internal RSK+ Block Diagram

4.2 Debugger Connections

The diagram below shows the connections between the RSK+, E1 debugger and the host PC.

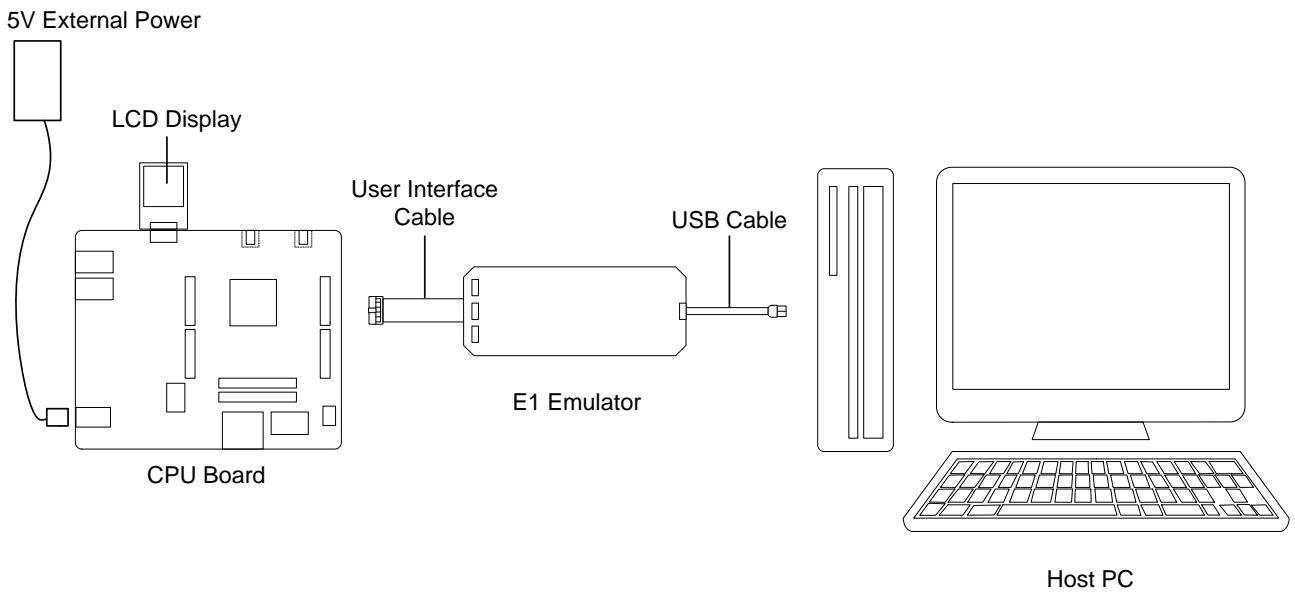


Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the RSK+ to generate the required reset signal, and is triggered from the RES switch. Refer to the RX64M User's Manual: Hardware for details regarding the reset signal timing requirements, and the RSK+ schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the RSK+ to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX/RX600 Group Hardware Manual and the RL78/G1C Group hardware manual for details regarding the clock signal requirements, and the RSK+RX64M board schematics for information regarding the clock circuitry in use on the RSK+. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Crystal Oscillator	Function	Default Placement	Frequency	Device Package
X1	Main MCU crystal for RX64M	Fitted	24MHz	Encapsulated, SMT
X2	Real time Clock for RX64M	Fitted	32.768kHz	Encapsulated, SMT
X3	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT
X4	Crystal for Ethernet (MII)	Fitted	25MHz	Encapsulated, SMT
X5	Oscillator for Ethernet (RMII)	Fitted	50MHz	Encapsulated, SMT
X6	Crystal for USBA Module*	Not Fitted	48MHz	Encapsulated, SMT

Table 5-1: Oscillators

* This board does not require this oscillator connecting.

5.3 Switches

There are four switches located on the RSK+ board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the RSK+ board schematics.

Switch	Function	MCU	
		Signal (Port)	Pin
RES	When pressed, the microcontroller is reset.	RES#	21
SW1	Connects to an IRQ input for user controls.	IRQ5 (P15)	50
SW2	Connects to an IRQ input for user controls.	IRQ2 (P12)	53
SW3	Connects to an ADTRG input for ADC controls. (P07 can be used also as IRQ15).	ADTRG0n (P07)	176

Table 5-2: Switch Connections

5.4 LEDs

There are 12 LEDs on the RSK+ board. The function of each LED, its colour, and its connections are shown in **Table 5-3**.

LED	Colour	Function	MCU	
			Port	Pin
3V3_PWR	Green	Indicates the status of the Board_3V3 power rail.	NC	NC
5V_PWR	Green	Indicates the status of the Board_5V power rail.	NC	NC
LED0	Green	User operated LED.	P03	4
LED1	Orange	User operated LED.	P05	2
LED2	Red	User operated LED.	P26	37
LED3	Red	User operated LED.	P27	36
SPEED0	Green	Ethernet LED (Speed)	NC	NC
ETHERNET0 Connector	Green	Ethernet LED (Link)	P34	27
ETHERNET0 Connector	Yellow	Ethernet LED (Activity)	NC	NC
SPEED1	Green	Ethernet LED (Speed)	NC	NC
ETHERNET1 Connector	Green	Ethernet LED (Link)	P93	159
ETHERNET1 Connector	Yellow	Ethernet LED (Activity)	NC	NC

Table 5-3: LED Connections

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin 173. The potentiometer can be used to create a voltage between Board_3V3 and ground.

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RX64M Group User's Manual: Hardware for further details.

5.6 Pmod™ Debug LCD Module

A Pmod™ Compatible debug LCD module is supplied with the RSK+ board, and should be connected to the PMOD1 header.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible header uses a SPI interface. Some RSKs will be provided with a monochrome display, others will have a colour display. Code for the appropriate display will be included in the product software support. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-4** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK+ designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011

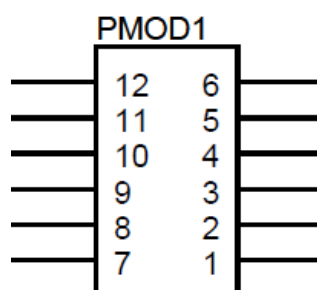


Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	CTS6RTS6	PJ3	13	7	IRQ8	P20	45
	P45	P45	167				
2	TXD6	P00	8	8	IRQ9	P21	44
3	RXD6	P01	7	9	P46	P46	166
4	SCK6	P02	6	10	P47	P47	165
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-4: Pmod™1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	P-CTS7RTS7	P93	159	7	IRQ10-DS	P42	170
2	P-TXD7	P90	163	8	IRQ11-DS	P43	169
3	P-RXD7	P92	160	9	P96	P96	152
4	P-SCK7	P91	161	10	P97	P97	149
5	GROUND	-	-	11	GROUND	-	-
6	Board_3V3	-	-	12	Board_3V3	-	-

Table 5-5: Pmod™2 Header Connections

5.7 USB Serial Port

A USB serial port implemented in another Renesas low power microcontroller (RL78/G1C) is fitted on the RSK+ board to the microcontroller Serial Communications Interface (SCI) module. Multiple options are provided to allow re-use of the serial interface.

Connections between the USB to Serial converter and the microcontroller are listed in **Table 5-6** below.

Signal Name	Function	MCU	
		Port	Pin
TXD1*1	SCI1 Transmit Signal.	PF0	35
RXD1*1	SCI1 Receive Signal	PF2	31
TXD2*1	SCI2 Transmit Signal.	P50	72
RXD2*1	SCI2 Receive Signal	P52	70
A-TXD7	SCI7 Transmit Signal.	P90	163
A-RXD7	SCI7 Receive Signal	P92	160
RS232TX*1	External SCI Transmit Signal.	-	-
RS232RX*1	External SCI Receive Signal.	-	-
RXCTS*2	Clear To Send	P41	171
RXRTS*2	Request to Send	PJ5	11

Table 5-6: Serial Port Connections

*1 This connection is not available in the default RSK+ configuration - refer to §6 for the required modifications.

*2 CTS & RTS control is not supported by the signal formed in extension now. There is no plan which now extends this feature.

When the RSK+ board is first connected to a PC running Windows with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in Figure 5.2. The exact messages may vary depending upon operating system.

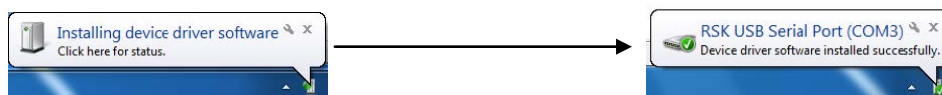


Figure 5-2: USB-Serial Windows Installation message

5.7.1 Reading the Virtual COM Port Number

In order for the PC to be able to communicate with the RSK+ board via the USB virtual COM port, the correct COM port number must be determined. If the COM port number is not known, follow this process:

1. Connect the PC to the serial/USB port.
2. On the PC, go to Start -> Control Panel -> Device Manager. Go to the “Ports (COM & LPT)” section and the COM port should be listed there. To verify the correct port, the USB cable can be disconnected and re-connected to show the COM port appearing and disappearing.

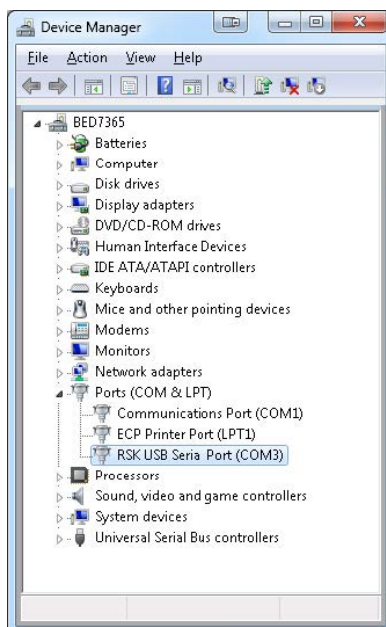


Figure 5-3: Device Manager

5.7.2 Changing the Virtual COM Port Number

Some PC applications will only work with particular COM port numbers. COM port numbers for the RSK+ serial/USB are assigned automatically at the time of first connection to the PC. It is possible to assign a different value manually. The procedure to do this is as follows:

1. Right-click the USB-Serial port in device manager and select “Properties”

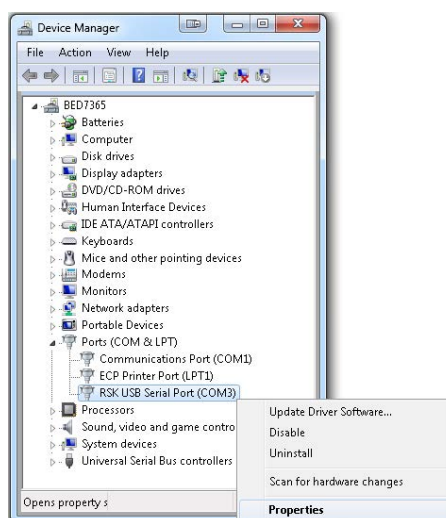


Figure 5-4: Device Manager Properties-1

2. Select the “Port Settings” tab and click “Advanced...”



Figure 5-5: Device Manager Properties-2

3. Select the new COM port from the drop down list. Bear in mind that the “in use” label on various ports listed may not actually mean that that port is in use at this current point in time.

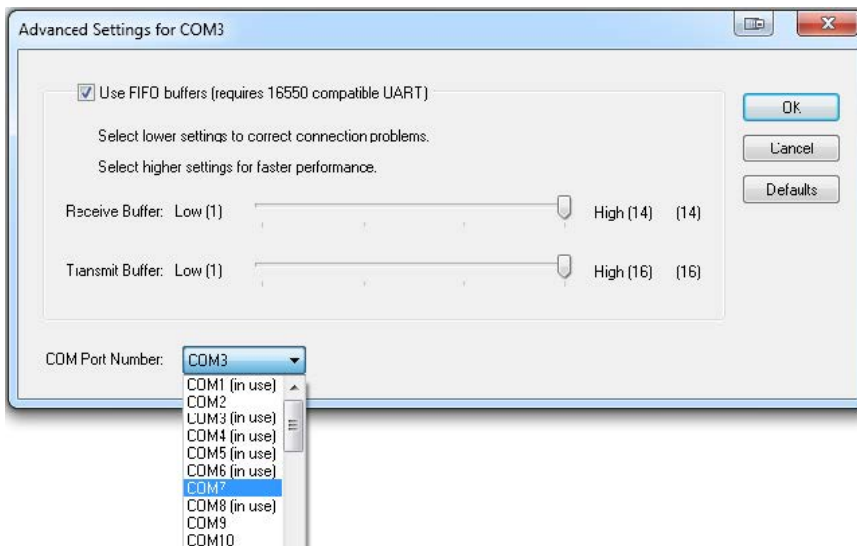


Figure 5-6: Device Manager Properties-3

4. Click OK to complete the process.

5.8 Controller Area Network (CAN)

A CAN transceiver IC is fitted to the RSK+ board, and connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX64M Group User's Manual: Hardware.

The connections for the CAN microcontroller signals are listed in **Table 5-7** below.

CAN Signal	Function	MCU	
		Port	Pin
CTX0	CAN Data Transmission.	P32	29
CRX0	CAN Data Reception.	P33	28

Table 5-7: CAN Connections

5.9 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the RSK+RX64M PCB as a sticker, and should be always be used with this device ensured to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

An Ethernet controller IC is fitted to the RSK+ board, and is connected to the Ethernet MCU peripheral. The RX64M MCU supports full duplex 10Mb/s and 100Mb/s transmission and reception. The connections for the Ethernet controller are listed in **Table 5-8** and **Table 5-9** below.

Ethernet signal	Function	MCU	
		Port	Pin
ET0MDIO	Management data serial I/O	P71	102
ET0MDC	Management serial clock	P72	101
ET0TXCLK	Transmit clock	PC4	82
ET0TXEN_RMII0TXDEN	Transmit enable.	P80	81
ET0TXER	Transmit error.	PC3	83
ET0ETXD0_RMII0TXD0	Transmit data bit 0.	P81	80
ET0ETXD1_RMII0TXD1	Transmit data bit 1.	P82	79
ET0ETXD2	Transmit data bit 2.	PC5	78
ET0ETXD3	Transmit data bit 3.	PC6	77
ET0RXCLK	Receive clock.	P76	85
ET0RXDV	Receive data valid.	PC2	86
ET0RXER_RMII0RXER	Receive data error.	P77	84
ET0ERXD0_RMII0RXD0	Receive data bit 0.	P75	87
ET0ERXD1_RMII0RXD1	Receive data bit 1.	P74	88
ET0ERXD2	Receive data bit 2.	PC1	89
ET0ERXD3	Receive data bit 3.	PC0	91
ET0COL	Collision detect.	PC7	76
ET0LINKSTA	Link status input.	P34	27
ET0CRS_RMII0CRSDV	Carrier sense	P83	74

Table 5-8: Ethernet Connections (ET0)

Ethernet signal	Function	MCU	
		Port	Pin
ET1MDIO	Management data serial I/O	P30	33
ET1MDC	Management serial clock	P31	32
ET1TXCLK	Transmit clock	PG2	123
ET1TXEN_RMII1TXDEN	Transmit enable.	P60	141
ET1TXER	Transmit error.	PG7	111
ET1ETXD0_RMII1TXD0	Transmit data bit 0.	PG3	121
ET1ETXD1_RMII1TXD1	Transmit data bit 1.	PG4	119
ET1ETXD2	Transmit data bit 2.	PG5	116
ET1ETXD3	Transmit data bit 3.	PG6	113
ET1RXCLK	Receive clock.	PG0	146
ET1RXDV	Receive data valid.	P90	163
ET1RXER_RMII1RXER	Receive data error.	PG1	144
ET1ERXD0_RMII1RXD0	Receive data bit 0.	P94	157
ET1ERXD1_RMII1RXD1	Receive data bit 1.	P95	155
ET1ERXD2	Receive data bit 2.	P96	152
ET1ERXD3	Receive data bit 3.	P97	149
ET1COL	Collision detect.	P91	161
ET1LINKSTA	Link status input.	P93	159
ET1CRS_RMII1CRSDV	Carrier sense	P92	160

Table 5-9: Ethernet Connections (ET1)

5.10 Universal Serial Bus (USB)

This RSK+ board is fitted with a USB host socket (type A) and a function socket (type Mini B). USB module USB0 is connected to the host and function socket, and can operate as either a host or function device. USB module USBA is connected to the host and function socket, and can operate as either a host or function device. The connections for the USB0 module and USBA module are shown in **Table 5-10** and **Table 5-11** below.

USB Signal	Function	MCU	
		Port	Pin
USB0DP	Positive differential data signal.	USB0_DP	56
USB0DM	Negative differential data signal.	USB0_DM	55
USB0VBUS	Cable monitor pin.	P16	48
USB0VBUSEN	VBUS power supply enable.		
USB0OVRCURA	Over-current detection signal A.	P14	51

Table 5-10: USB0 Module Connections

USB Signal	Function	MCU	
		Port	Pin
USBADP	Positive differential data signal.	USBA_DP	64
USBADM	Negative differential data signal.	USBA_DM	63
USBAVBUS	Cable monitor pin.	P11	67
USBAVBUSEN	VBUS power supply enable.		
USBAOVRCURA	Over-current detection signal A.	P10	68
USBAOVRCURB	Over-current detection signal B.	P22	43
USBAEXICEN	Low-power control signal	P21	44
USBAID	ID input signal	P20	45

Table 5-11: USBA Module Connections

* This RSK+ board is equipped with the OTG (On The Go™) circuit for USB module USBA. When evaluating OTG, it is necessary to mount the socket for OTG separately. (Manufacture name: Model-name: Hirose Electric, ZX62 R-AB-5P)

5.11 LCD Direct Drive Header (TFT)

This RSK+ board is fitted with a LCD Direct Drive thru-hole pattern, which allows connection to compatible Renesas LCD application boards.

The pin connections of this header are listed in **Table 5-12** below.

LCD Direct Drive Header (TFT)							
Pin	Header Name	MCU		Pin	Header Name	MCU	
		Port	Pin			Port	Pin
1	5V	-		2	5V	-	
3	3V3	-		4	3V3	-	
5	Reserved	-		6	Reserved	-	
7	B1	PD0	158	8	B2	PD1	156
9	B3	PD2	154	10	B4	PD3	150
11	B5	PD4	148	12	G0	PD5	147
13	G1	PD6	145	14	G2	PD7	143
15	G3	PE0	135	16	G4	PE1	134
17	G5	PE2	133	18	R1	PE3	132
19	R2	PE4	131	20	R3	PE5	130
21	R4	PE6	126	22	R5	PE7	125
23	EDACK	P83	74	24	HSYNC	PJ3	13
25	DOTCLK	P34	27	26	LCDDEN	PC1	89
27	VSYNC	P26	37	28	EDREQ	P82	79
29	SSCK	P77	84	30	SSI	PC4	82
31	SSO	PC3	83	32	SCS	P76	85
33	RESET	RES#	21	34	GND	-	-
35	BACKLIGHT	P27	36	36	SD_DOTCLK	-	-
37	GND	-	-	38	GND	-	-
39	GND	-	-	40	GND	-	-
41	X_DRIVE	PJ5	11	42	Y_DRIVE	P41	171
43	X_INPUT1	P44	168	44	Y_INPUT1	P45	167
45	X_INPUT2	P46	166	46	Y_INPUT2	P47	165
47	Reserved	-	-	48	Reserved	-	-
49	Reserved	-	-	50	Reserved	-	-

Table 5-12: Generic LCD Header Connections

5.12 External Bus

The RX64M features an external data bus, which is connected to various devices on the RSK+ board. Details of the devices connected to the external data bus are listed in **Table 5-13** below. Further details of the devices connected to the external bus can be found in the board schematics.

Chip Select	Device Name	Device Description	Address Space
CS0	JA3	Application Header	FF000000h to FFFFFFFFh (16Mbytes)
SDCS	U13	128MBit SDRAM	08000000h to 0FFFFFFFh (128Mbytes)
	JA3	Application Header	08000000h to 0FFFFFFFh (128Mbytes)
CS1 to CS3	-	Unused	05000000h to 07FFFFFFh (3 x 16Mbytes)
CS4	JA3	Application Header	04000000h to 04FFFFFFh (16Mbytes)
CS5 to CS7	-	Unused	01000000h to 03FFFFFFh (3 x 16Mbytes)

Table 5-13: External Bus Address Space

5.13 Renesas Serial Peripheral Interface (RSPI)

The RX64M features one Renesas Serial Peripheral Interface module (Renesas SPI or RSPI). **Table 5-14** below details the connected devices, and their connections to the MCU.

Slave Select	Device Name	Device Description
SSLA1-A	U7	Serial Flash, 32Mbits

Table 5-14: RSPI Connections

5.14 Quad Serial Peripheral Interface (QSPI)

The RX64M features one Quad Serial Peripheral Interface modules (QSPI). **Table 5-15** below details the connected devices, and their connections to the MCU.

Slave Select	Device Name	Device Description
QSSLA-A (BD_QSSLA-A)	U8	Serial Flash, 32Mbits
QSSLA-A (TFT_QSSLA-A)	TFT	Generic LCD Header

Table 5-15: QSPI Connections

5.15 I²C Bus (Inter-IC Bus)

The RX64M features two I²C (Inter-IC Bus) interface modules. RIIC2 is connected to a 16Kbit EEPROM (Electrically-Erasable Programmable Read Only Memory). Specific details of the EEPROM device and the connections can be found in the board schematics.

On board EEPROM only supports single device on bus. To allow external I²C device, option links have to be modified – refer to §6 for further details.

5.16 SD Host Interface (SDHI)

A SD Card Slot is fitted to the RSK+ board, and connected to the SD Host Interface (SDHI) MCU peripheral. For further details regarding the SDHI operation, please refer to the RX64M Group User's Manual: Hardware. The connections for the SDHI signals are listed in **Table 5-16** below.

SD Card Slot (SD1)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	SDD3-B	PD3	150	2	SDCMD-B	PD4	148
3	GROUND	-	-	4	SDPWREN	PF5	9
5	SDCLK-B	PD5	147	6	GROUND	-	-
7	SDD0-B	PD6	145	8	SDD1-B	PD7	143
9	SDD2-B	PD2	154	10	SDCD-B	PE6	126
11	GROUND	-	-	12	SDWP-B	PE7	125

Table 5-16: SDHI Connections

5.17 Parallel Data Capture Unit (PDC)

This RSK+ board is fitted with a Parallel Data Capture Unit (PDC) thru-hole pattern. The connections for the PDC signals are listed in **Table 5-17** below.

PDC Header (J26)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_5V	-	-	2	Board_3V3	-	-
3	GROUND	-	-	4	GROUND	-	-
5	PCKO	P33	28	6	RESn	RESn	21
7	GND	-	-	8	PIXCLK	P24	40
9	VSYNC	P32	29	10	HSYNC	P25	38
11	PIXD7	P23	42	12	PIXD6	P22	43
13	PIXD5	P21	44	14	PIXD4	P20	45
15	PIXD3	P17	46	16	PIXD2	P87	47
17	PIXD1	P86	49	18	PIXD0	P15	50
19	PDC_SSDA6	P00	8	20	PDC_SSCL6	P01	7

Table 5-17: PDC Connections

5.18 Serial Sound Interface (SSI)

This RSK+ board is fitted with a Serial Sound Interface (SSI) thru-hole pattern. The connections for the PDC signals are listed in **Table 5-18** below.

SSI Header (J25)							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	Board_5V	-		2	Board_3V3	-	
3	GROUND	-	-	4	GROUND	-	-
5	AUDIOCLK	P22	43	6	GROUND	-	-
7	GROUND	-	-	8	NC	-	-
9	SSISCK0	P23	42	10	SSIRXD0	P20	45
11	SSIWS0	P21	44	12	SSITXD0	P17	46

Table 5-18: SSI Connections

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way RSK+ operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the RSK+ is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the RSK+ is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX64M Group User's Manual: Hardware and RSK+RX64M schematics for further information.

6.2 MCU Operating Modes

Table 6-1 below details the option links associated with configuring the MCU operating modes.

Reference	Pin1	Pin2	Pin3	Explanation	Related Ref.
SW4	OFF	OFF	OFF	Single Chip Mode	-
	ON	OFF	OFF	User Boot Mode USB Boot Mode (Bus-powered)	-
	OFF	ON	OFF	Single Chip Mode	-
	ON	ON	OFF	SCI Boot Mode	-
	OFF	OFF	ON	Single Chip Mode	-
	ON	OFF	ON	User Boot Mode USB Boot Mode (Self-powered)	-
	OFF	ON	ON	Single Chip Mode	-
	ON	ON	ON	SCI Boot Mode	-

Table 6-1: MCU Mode Switch Settings

6.3 E1 Debugger Configuration

Table 6-2 below details the function of the option links associated with E1 Debugger configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ET0COL_MISOA-A_PC7	76	PC7	MISOA-A	J12.Pin1-2	-	U7.2	-	-
			ET0COL	J12.Pin2-3, SW6.3.ON	SW6.4.OFF	U6.21	R379	-
			PC7	J12.Pin2-3, SW6.4.ON	SW6.3.OFF	SW4.2 E1.10	- R248	- -
TDO_TXD1	35	PF0	TDO	R255	R142	E1.5	-	-
			TXD1	R142	R255	U9.3 JA6.8	R140 R122	R126, R134, R141 -
TCK_SCK1	34	PF1	TCK	R263	R381	E1.1	-	-
			SCK1	R381	R263	JA6.10	R108	-
TDI_RXD1	31	PF2	TDI	R246	R157	E1.11	-	-
			RXD1	R157	R246	U10.3 JA6.7	R156 R120	R149, R150, R165 -
EMLE	10	-	EMLE	-	-	J19.2	-	-
						E1.4	R260	-

Table 6-2: E1 Debugger Option Links

Table 6-3 below details the function of the jumpers associated with the E1 Debugger.

Reference	Jumper Position	Explanation	Related Ref.
J19	Shorted Pin1-2	Enables E1 debugging with Hot plug-in function.	-
	Shorted Pin2-3	Enables E1 normal debugging and MCU single operation (without E1).	-
	All open	DO NOT SET.	-

Table 6-3: E1 Debugger Jumper Settings

6.4 Power Supply Configuration

Table 6-4 below details the function of the option links associated with power supply configuration.

Reference	Exclusive Function			Connection
	Function	Enable	Disable	Interface Function
VBUS0, VBUSA	Connects VBUS0 to 5V Power rail.	J2.Pin2-3, J22.Pin2-3, R221	R220	U15
	Connects VBUSA to 5V Power rail.	J7.Pin2-3, J22.Pin2-3, R220	R37, R221	U15
Board_5V	Connects 5V power rail to Board_5V.	R244	-	IIC Pull-up resistors(R528, R534), 5V_PWR, U12.3, U14(R218), J25.1, J26.1, TFT.1, 2
SD_3V3	Connects 3.3V power rail to SD_3V3.	R254	-	U16.5, 7
CON_3V3	Connects CON_3V3 to 3.3V power rail.	R259	-	JA1.3, U15.2
VCCUSB	Connects 3V3 power rail to VCCUSB.	R215	R210	U1(VCC_USB)
	Connects UC_VCC to VCCUSB.	R210	R215	U1(VCC_USB)
UC_VCC	Connects 3.3V power rail to UC_VCC	R217	-	U1(VCC)

Table 6-4: Power Supply Option Links

Table 6-5 below details the function of the jumpers associated with the power supply.

Reference	Jumper Position	Explanation	Related Ref.
J22	Shorted Pin1-2	Enables external battery input.	-
	Shorted Pin2-3	Enables VBUS input.	R221, R220
	All open	Disables external battery input and VBUS input.	-
J21	Shorted Pin1-2	Connects 3.3V power rail to UC_VCC.	R217
	All open	Enables current probe for measurement MCU current consumption.	R217
J24	Shorted Pin1-2	Connects UC_VCC to VBAT.	-
	Shorted Pin2-3	Connects external coin cell input.	-
	All open	Do not setting.	-

Table 6-5: Power Supply Jumper Settings

6.5 Clock Configuration

Table 6-6 below details the function of the option links associated with clock configuration.

Reference	Exclusive Function			Connection
	Function	Enable	Disable	Interface Function
XTAL, EXTAL, CON_EXTAL	Connects 24MHz crystal (X1) to RX64M.	R61, R84	R60	U1(EXTAL, XTAL)
	Connects CON_EXTAL to RX64M.	R60	R61, R84	U1(EXTAL)
XCIN, XCOU	Connects 32.768kHz crystal (X2) to RX64M.	R101, R109	R110	U1(XCIN, XCOU)
	Disconnects X2 from RX64M.	R110	R101, R109	U1(XCIN, XCOU)
P13, MTIOC0B_IRQ3	Connects P13 (o/p) to JA2.9 or JA5.9.	R517	R516, R537	JA2.9, JA5.9
	Connects 48MHz oscillator (X6) to RX64M P13. X6 NOT FITTED BY DEFAULT	R516	R517, R537	U1.52
REF50CK0, REF50CK1	Connects 25MHz crystal (X4) to PHY.	R95, R96	R94	U6(XCLK0, XCLK1)
	Connects 50MHz oscillator (X5) to PHY and REF50CK0 (RX64M).	R94, R106	R95, R96, R118	U6(XCLK0), U1.85
	Connects 50MHz oscillator (X5) to PHY and REF50CK1 (RX64M).	R94, R105	R95, R96, R118	U6(XCLK0), U1.146

Table 6-6: Clock Option Links

6.6 Analog Power & ADC & DAC Configuration

Table 6-7 below details the function of the option links associated with ADC & DAC configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
AN000	173	P40	AN000	-	-	RV1	R461	-
						JA1.9 (Direct Input via JA1.9)	R205	R214, R435
						JA1.9 (Input via Voltage Division Resistor)	R214, R435	R205
AN001_RXCTS_YDRIVE	171	P41	AN001	R204	R236, R421	JA1.10	-	-
			RXCTS	R421	R204, R236	U10.2	-	-
			YDRIVE	R236	R204, R421	TFT.42	-	-
AN002_IRQ10-DS	170	P42	AN002	R200	R145	JA1.11	-	-
			IRQ10-DS	R145	R200	PMOD2.7	-	-
AN003_IRQ11-DS	169	P43	AN003	R199	R152	JA1.12	-	-
			IRQ11-DS	R152	R199	PMOD2.8	-	-
AN004_XINPUT1	168	P44	XINPUT1	R237	R125	TFT.43	-	-
			AN004	R125	R237	JA5.1	-	-
AN005_YINPUT1_P45	167	P45	YINPUT1	R238	R131, R505	TFT.44	-	-
			AN005	R131	R238, R505	JA5.2	-	-
			P45	R505	R131, R238	PMOD1.1	R408	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R239	R123, R506	TFT.45	-	-
			AN006	R123	R239, R506	JA5.3	-	-
			P46	R506	R123, R239	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R240	R124, R507	TFT.46	-	-
			AN007	R124	R240, R507	JA5.4	-	-
			P47	R507	R124, R240	PMOD1.10	-	-
LED0_DAO	4	P03	LED0	R277	R189	LED0	-	-
			DAO	R189	R277	JA1.13	-	-
LED1_DA1	2	P05	LED1	R280	R188	LED1	-	-
			DA1	R188	R280	JA1.14	-	-
ADTRG0n	176	P07	ADTRG0n	-	-	SW3	R494	-
						JA1.8	-	-
VREFH0	174	-	UC_VCC	R175	R176	-	-	-
			CON_VREFH0	R176	R175	JA1.7	-	-
VREFL0	172	-	GROUND	R174	-	-	-	-
AVCC0	175	-	UC_VCC	R178	R177, R179	-	-	-
			CON_AVCC0	R177	R178, R179	JA1.5	-	-
			Board_3V3	R179, R180	R177, R178	-	-	-
AVSS0	1	-	GROUND	R182	R181	-	-	-
			CON_AVSS0	R181	R182	JA1.6	-	-
VREFH	3	-	UC_VCC	R183	-	-	-	-
VREFL	5	-	GROUND	R184	-	-	-	-

Table 6-7: Analog Power & ADC & DAC Option Links

6.7 BUS & SDRAM Configuration

Table 6-8 to Table 6-11 below details the function of the option links associated with BUS & SDRAM configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
USBAOVRCURA_ALE_MTIC5W	68	P10	USBAOVRCURA	R351	R83, R478	U3.2	R4	R29
			ALE	R478	R83, R351	U4.5	R29	R4
			MTIC5W	R83	R351, R478	JA3.46	R464	R445
WRn_WR0n_TXD2_SSDA2	72	P50	WRn	R115	R114, R119, R514	JA5.14	R86	R82
			WR0n	R119	R114, R115, R514	JA6.16	R82	R86
			TXD2	R114	R115, R119, R514	JA3.26	R387	R429
			SSDA2	R514	R114, R115, R119	JA3.48	R462	R427
WR1n_WAITn_SCK2	71	P51	WR1n	R476	R481, R482	U9.3	R126	R134, R140, R141
			SCK2	R482	R476, R481	JA6.9	-	-
			RDn	R100	R99, R515	JA1.25	R520	R519
RDn_RXD2_SSCL2	70	P52	RXD2	R99	R100, R515	JA3.45	R466	R465
			SSCL2	R515	R99, R100	JA3.47	R463	R442
BCLK	69	P53	BCLK	R338	-	JA6.11	-	-
ET1TXEN_RMII1TXDEN_CS0n	141	P60	ET1TXEN_RMII1TXDEN	R374	R403	JA3.25	-	-
			CS0n	R403	R374	U10.3	R150	R149, R156, R165
SDCSn	139	P61	BD_SDCSn	R433	R404	JA6.12	-	-
			CON_SDCSn	R404	R433	JA1.26	R522	R521
RASn	138	P62	RASn	-	-	JA3.44	R348	R443
CASn	137	P63	CASn	-	-	U6.28	-	-
						JA3.45	R465	R466
WEn	136	P64	WEn	-	-	U13.19	-	-
						JA3.28	-	-
CKE	124	P65	CKE	-	-	U13.18	-	-
						JA3.50	-	-
DQM0_MTI0C7D	122	P66	DQM0	R428	R51	U13.17	-	-
			MTI0C7D	R51	R428	JA3.49	-	-
DQM1_MTI0C7C	120	P67	DQM1	R441	R62	U13.16	-	-
			MTI0C7C	R62	R441	JA3.26	R429	R387

Table 6-8: BUS & SDRAM Option Links (1)

Signal name	MCU		Exclusive Function			Connection		
	P.in	P.out	Signal	Enable	Disable	Interface Function	Enable	Disable
SDCLK	128	P70	SDCLK	R398	-	U13.38	R444	-
						JA3.44	R443	R348
ET0ERXD1_RMII0RXD1_CS4n	88	P74	ET0ERXD1_RMII0RXD1_CS4n	SW6.7.ON	SW6.8.OFF	U6.54	-	-
			CS4n	SW6.8.ON	SW6.7.OFF	JA3.27	-	-
A0_MTI0C6D	118	PA0	A0	R250	R69	JA3.1	-	-
			MTI0C6D	R69	R250	JA5.20	-	-
A1_MTI0C7B	114	PA1	A1	R423	R63	U13.23, JA3.2	-	-
			MTI0C7B	R63	R423	JA5.23	-	-
A2_MTI0C7A	112	PA2	A2	R424	R70	U13.24, JA3.3	-	-
			MTI0C7A	R70	R424	JA5.21	-	-
A3	110	PA3	A3	-	-	U13.25, JA3.4	-	-
A4	109	PA4	A4	-	-	U13.26, JA3.5	-	-
A5_MTI0C6B	108	PA5	A5	R448	R76	U13.29, JA3.6	-	-
			MTI0C6B	R76	R448	JA5.19	-	-
A6	107	PA6	A6	-	-	U13.30, JA3.7	-	-
A7	106	PA7	A7	-	-	U13.31, JA3.8	-	-
A8	104	PB0	A8	-	-	U13.32, JA3.9	-	-
A9	100	PB1	A9	-	-	U13.33, JA3.10	-	-
A10	99	PB2	A10	-	-	U13.34, JA3.11	-	-
A11	98	PB3	A11	-	-	U13.22, JA3.12	-	-
A12	97	PB4	A12	-	-	U13.35, JA3.13	-	-
A13_POE4n	96	PB5	A13	R344, R422	R80	U13.20, JA3.14	-	-
			POE4n	R344, R80	R422	JA5.16	-	-
A14	95	PB6	A14	-	-	U13.21, JA3.15	-	-
A15	94	PB7	A15	-	-	JA3.16	-	-
A16_ET0ERXD3_SSLA1-A	91	PC0	SSLA1-A	J11.Pin1-2	-	U7.1	-	-
			A16_ET0ERXD3	J11.Pin2-3	-	JA3.37	-	-
			ET0ERXD3	J11.Pin2-3, SW5.1.ON	-	JA3.37, U6.56	R54	-
A17_ET0ERXD2_MTI0C3A	89	PC1	A17_ET0ERXD2_MTI0C3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.55	R58	-
			MTI0C3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A18_ET0RXDV_MTI0C4B	86	PC2	A18_ET0RXDV_MTI0C4B	-	-	JA3.39	-	-
			ET0RXDV	SW5.4.ON	SW5.5.OFF	JA3.39, U6.57	R53	R503
			MTI0C4B	SW5.5.ON	SW5.4.OFF	JA3.39, JA2.17	-	-

Table 6-9: BUS & SDRAM Option Links (2)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
A19_ET0TXER_QIOA0-A_MTI0C4D	83	PC3	A19_ET0TXER_QIOA0-A_MTI0C4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, U6.47	-	-
			BD_QIOA0-A	SW5.7.ON, R365	SW5.6.OFF, SW5.8.OFF, R364	JA3.40, U8.5	-	-
			TFT_QIOA0-A	SW5.7.ON, R364	SW5.6.OFF, SW5.8.OFF, R365	JA3.40, TFT.31	R233	-
			MTI0C4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-
A20_ET0TXCLK_QIOA1-A_POE0n	82	PC4	A20_ET0TXCLK_QIOA1-A_POE0n	R339	-	JA3.41	-	-
			ET0TXCLK	R339, SW5.9.ON	SW5.10.OFF	JA3.41, U6.49	R71	-
			BD_QIOA1-A	R339, SW5.10.ON, R361	SW5.9.OFF, R360, R362	JA3.41, U8.2	-	-
			TFT_QIOA1-A	R339, SW5.10.ON, R360	SW5.9.OFF, R361, R362	JA3.41, TFT.30	R224	-
			POE0n	R339, SW5.10.ON, R362	SW5.9.OFF, R360, R361	JA3.41, JA2.24	-	-
A21_ET0ETXD2_RSPCKA-A	78	PC5	RSPCKA-A	J13.Pin1-2	-	U7.6	-	-
			A21_ET0ETXD2	J13.Pin2-3	-	JA3.42	-	-
			ET0ETXD2	J13.Pin2-3, SW6.1.ON	-	JA3.42, U6.45	-	-
A22_ET0ETXD3_MOSIA-A	77	PC6	MOSIA-A	J14.Pin1-2	-	U7.5	-	-
			A22_ET0ETXD3	J14.Pin2-3	-	JA3.43	-	-
			ET0ETXD3	J14.Pin2-3, SW6.2.ON	-	JA3.43, U6.46	-	-
D0	158	PD0	D0	-	-	U13.2, JA3.17, TFT.7	-	-
D1	156	PD1	D1	-	-	U13.4, JA3.18, TFT.8	-	-
D2_SDD2-B	154	PD2	D2	SW8.1.ON	SW8.2.OFF	U13.5, JA3.19, TFT.9	-	-
			SDD2-B	SW8.2.ON	SW8.1.OFF	SD1.9	-	-
D3_SDD3-B	150	PD3	D3	SW8.3.ON	SW8.4.OFF	U13.7, JA3.20, TFT.10	-	-
			SDD3-B	SW8.4.ON	SW8.3.OFF	SD1.1	-	-
D4_SDCMD-B	148	PD4	D4	SW8.5.ON	SW8.6.OFF	U13.8, JA3.21, TFT.11	-	-
			SDCMD-B	SW8.6.ON	SW8.5.OFF	SD1.2	-	-
D5_SDCLK-B	147	PD5	D5	SW8.7.ON	SW8.8.OFF	U13.10, JA3.22, TFT.12	-	-
			SDCLK-B	SW8.8.ON	SW8.7.OFF	SD1.5	-	-

Table 6-10: BUS Option Links (3)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
D6_SDD0-B	145	PD6	D6	SW8.9.ON	SW8.10.OFF	U13.11, JA3.23, TFT.13	-	-
			SDD0-B	SW8.10.ON	SW8.9.OFF	SD1.7	-	-
D7_SDD1-B	143	PD7	D7	SW9.1.ON	SW9.2.OFF	U13.13, JA3.24, TFT.14	-	-
			SDD1-B	SW9.2.ON	SW9.1.OFF	SD1.8	-	-
D8_IO0	135	PE0	D8	R440	R186	U13.42, JA3.29, TFT.15	-	-
			IO0	R186	R440	JA1.15	-	-
D9_IO1	134	PE1	D9	R439	R185	U13.44, JA3.30, TFT.16	-	-
			IO1	R185	R439	JA1.16	-	-
D10_IO2	133	PE2	D10	R438	R171	U13.45, JA3.31, TFT.17	-	-
			IO2	R171	R438	JA1.17	-	-
D11_IO3	132	PE3	D11	R226	R170	U13.47, JA3.32, TFT.18	-	-
			IO3	R170	R226	JA1.18	-	-
D12_IO4	131	PE4	D12	R227	R163	U13.48, JA3.33, TFT.19	-	-
			IO4	R163	R227	JA1.19	-	-
D13_IO5	130	PE5	D13	R228	R162	U13.50, JA3.34, TFT.20	-	-
			IO5	R162	R228	JA1.20	-	-
D14_SDCD-B_MTI0C6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U13.51, JA3.35, TFT.21	-	-
			SDCD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTI0C6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDWP-B_MTI0C6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U13.53, JA3.36, TFT.22	-	-
			SDWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTI0C6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-

Table 6-11: BUS Option Links (4)

6.8 CAN Configuration

Table 6-12 below details the function of the option links associated with CAN configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
CTX0_VSYNC_MTIIOC0C_IRQ2-DS	29	P32	VSYNC	R267	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R267	U12.1	R208	-
						JA5.5	-	-
			MTIIOC0C_IRQ2-DS	J15.Pin2-3	R267	JA2.23	R147	R146
					JA5.10	R103	-	
CRX0_PCKO_MTIIOC0D	28	P33	PCKO	R290	J17.Open	J26.5	-	-
			CRX0	J17.Pin1-2	R290	U12.4	R191	-
						JA5.6	-	-
			MTIIOC0D	J17.Pin2-3	R290	JA2.21	-	-

Table 6-12: CAN Option Links

6.9 LCD Direct Drive (TFT) Configuration

Table 6-13 to Table 6-16 below details the function of the option links associated with LCD Direct Drive (TFT) configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
LED2_MTIIOC2A	37	P26	LED2	R281	R117	LED2	-	-
			MTIIOC2A	R117	R281	JA5.9	R116	R111
						TFT.27	-	-
LED3_MTIIOC2B_BACKLIGHT	36	P27	LED3	J23.Pin1-2	-	LED3	-	-
			MTIIOC2B	J23.Pin2-3, R169	R234	JA2.19	-	-
			BACKLIGHT	J23.Pin2-3, R234	R169	TFT.35	-	-
ETOLINKSTA_MTIIOC0A_IRQ4	27	P34	ETOLINKSTA	SW6.5.ON	SW6.6.OFF	U6.69, ETHERNET0.11	-	-
			MTIIOC0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R148	R497
						JA2.7	R211	-
					TFT.25	-	-	
AN001_RXCTS_YDRIVE	171	P41	AN001	R204	R236, R421	JA1.10	-	-
			RXCTS	R421	R204, R236	U10.2	-	-
			YDRIVE	R236	R204, R421	TFT.42	-	-
AN004_XINPUT1	168	P44	XINPUT1	R237	R125	TFT.43	-	-
			AN004	R125	R237	JA5.1	-	-

Table 6-13: LCD Direct Drive (TFT) Option Links (1)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
AN005_YINPUT1_P45	167	P45	YINPUT1	R238	R131, R505	TFT.44	-	-
			AN005	R131	R238, R505	JA5.2	-	-
			P45	R505	R131, R238	PMOD1.1	R408	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R239	R123, R506	TFT.45	-	-
			AN006	R123	R239, R506	JA5.3	-	-
			P46	R506	R123, R239	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R240	R124, R507	TFT.46	-	-
			AN007	R124	R240, R507	JA5.4	-	-
			P47	R507	R124, R240	PMOD1.10	-	-
ET0RXCLK_REF50CK0_QSSLA-A	85	P76	REF50CK0	J10.Pin1-2, R57	R48	U6.33, X5.3	R94, R106	R95, R96, R118
			ET0RXCLK	J10.Pin1-2, R48	R57	U6.59	R44	-
			BD_QSSLA-A	J10.Pin2-3, R386	R400	U8.1	-	-
			TFT_QSSLA-A	J10.Pin2-3, R400	R386	TFT.32	-	-
ET0RXER_RMII0RXER_QSPCLK-A	84	P77	ET0RXER_RMII0RXER	SW6.9.ON	SW6.10.OFF	U6.58	-	-
			BD_QSPCLK-A	SW6.10.ON, R382	SW6.9.OFF, R232	U8.6	-	-
			TFT_QSPCLK-A	SW6.10.ON, R232	SW6.9.OFF, R382	TFT.29	R225	-
ET0ETXD1_RMII0TXD1_MTIOC4A_EDREQ1	79	P82	ET0ETXD1_RMII0TXD1	SW7.7.ON	SW7.8.OFF	U6.44	-	-
			EDREQ1	SW7.8.ON, R231	SW7.7.OFF, R453	JA6.1, TFT28	-	-
			MTIOC4A	SW7.8.ON, R453	SW7.7.OFF, R231	JA2.15	-	-
ET0CRS_RMII0CRSDV_MTIOC4C_EDACK1	74	P83	ET0CRS_RMII0CRSDV	SW7.9.ON	SW7.10.OFF	U6.60	R504	R503
			EDACK1	SW7.10.ON, R229	SW7.9.OFF, R454	JA6.2, TFT23	-	-
			MTIOC4C	SW7.10.ON, R454	SW7.9.OFF, R229	JA2.16	-	-
A17_ET0ERXD2_MTIOC3A	89	PC1	A17_ET0ERXD2_MTIOC3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.55	R58	-
			MTIOC3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A19_ET0TXER_QIOA0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIOA0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, U6.47	-	-
			BD_QIOA0-A	SW5.7.ON, R365	SW5.6.OFF, SW5.8.OFF, R364	JA3.40, U8.5	-	-
			TFT_QIOA0-A	SW5.7.ON, R364	SW5.6.OFF, SW5.8.OFF, R365	JA3.40, TFT.31	R233	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-
A20_ET0TXCLK_QIOA1-A_POE0n	82	PC4	A20_ET0TXCLK_QIOA1-A_POE0n	R339	-	JA3.41	-	-
			ET0TXCLK	R339, SW5.9.ON	SW5.10.OFF	JA3.41, U6.49	R71	-
			BD_QIOA1-A	R339, SW5.10.ON, R361	SW5.9.OFF, R360, R362	JA3.41, U8.2	-	-
			TFT_QIOA1-A	R339, SW5.10.ON, R360	SW5.9.OFF, R361, R362	JA3.41, TFT.30	R224	-
			POE0n	R339, SW5.10.ON, R362	SW5.9.OFF, R360, R361	JA3.41, JA2.24	-	-

Table 6-14: LCD Direct Drive (TFT) Option Links (2)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
D0	158	PD0	D0	-	-	U13.2, JA3.17, TFT.7	-	-
D1	156	PD1	D1	-	-	U13.4, JA3.18, TFT.8	-	-
D2_SDD2-B	154	PD2	D2	SW8.1.ON	SW8.2.OFF	U13.5, JA3.19, TFT.9	-	-
			SDD2-B	SW8.2.ON	SW8.1.OFF	SD1.9	-	-
D3_SDD3-B	150	PD3	D3	SW8.3.ON	SW8.4.OFF	U13.7, JA3.20, TFT.10	-	-
			SDD3-B	SW8.4.ON	SW8.3.OFF	SD1.1	-	-
D4_SDCMD-B	148	PD4	D4	SW8.5.ON	SW8.6.OFF	U13.8, JA3.21, TFT.11	-	-
			SDCMD-B	SW8.6.ON	SW8.5.OFF	SD1.2	-	-
D5_SDCLK-B	147	PD5	D5	SW8.7.ON	SW8.8.OFF	U13.10, JA3.22, TFT.12	-	-
			SDCLK-B	SW8.8.ON	SW8.7.OFF	SD1.5	-	-
D6_SDD0-B	145	PD6	D6	SW8.9.ON	SW8.10.OFF	U13.11, JA3.23, TFT.13	-	-
			SDD0-B	SW8.10.ON	SW8.9.OFF	SD1.7	-	-
D7_SDD1-B	143	PD7	D7	SW9.1.ON	SW9.2.OFF	U13.13, JA3.24, TFT.14	-	-
			SDD1-B	SW9.2.ON	SW9.1.OFF	SD1.8	-	-
D8_IO0	135	PE0	D8	R440	R186	U13.42, JA3.29, TFT.15	-	-
			IO0	R186	R440	JA1.15	-	-
D9_IO1	134	PE1	D9	R439	R185	U13.44, JA3.30, TFT.16	-	-
			IO1	R185	R439	JA1.16	-	-
D10_IO2	133	PE2	D10	R438	R171	U13.45, JA3.31, TFT.17	-	-
			IO2	R171	R438	JA1.17	-	-
D11_IO3	132	PE3	D11	R226	R170	U13.47, JA3.32, TFT.18	-	-
			IO3	R170	R226	JA1.18	-	-
D12_IO4	131	PE4	D12	R227	R163	U13.48, JA3.33, TFT.19	-	-
			IO4	R163	R227	JA1.19	-	-

Table 6-15: LCD Direct Drive (TFT) Option Links (3)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
D13_IO5	130	PE5	D13	R228	R162	U13.50, JA3.34, TFT.20	-	-
			IO5	R162	R228	JA1.20	-	-
D14_SDCD-B_MTI0C6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U13.51, JA3.35, TFT.21	-	-
			SDCD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTI0C6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDWP-B_MTI0C6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U13.53, JA3.36, TFT.22	-	-
			SDWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTI0C6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-
CTS6RTS6_MTI0C3C	13	PJ3	CTS6RTS6	R318	R230	PMOD1.1	R1	R408
			MTI0C3C	R230	R318	JA2.11, TFT.24	-	-
RXRTS_XDRIVE	11	PJ5	RXRTS	R412	R235	U9.2	-	-
			XDRIVE	R235	R412	TFT.41	-	-

Table 6-16: Direct Drive LCD (TFT) Option Links (4)

6.10 Ethernet Configuration

Table 6-17 to Table 6-21 below details the function of the option links associated with Ethernet configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ETOLINKSTA_MTI0C0A_IRQ4	27	P34	ETOLINKSTA	SW6.5.ON	SW6.6.OFF	U6.69, ETHERNET0.11	-	-
			MTI0C0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R148	R497
				SW6.6.ON	SW6.5.OFF	JA2.7	R211	-
ETOMDIO	102	P71	ETOMDIO	-	-	U6.63	J3.Pin1-2	-
ETOMDC	101	P72	ETOMDC	-	-	U6.62	J4.Pin1-2	-
ETOERXD1_RMII0RXD1_CS4n	88	P74	ETOERXD1_RMII0RXD1_CS4n	SW6.7.ON	SW6.8.OFF	U6.54	-	-
			CS4n	SW6.8.ON	SW6.7.OFF	JA3.27	-	-
ETOERXD0_RMII0RXD0	87	P75	ETOERXD0_RMII0RXD0	-	-	U6.53	-	-
ETORXCLK_REF50CK0_QSSLA-A	85	P76	REF50CK0	J10.Pin1-2, R57	R48	U6.33, X5.3	R94, R106	R95, R96, R118
			ETORXCLK	J10.Pin1-2, R48	R57	U6.59	R44	-
			BD_QSSLA-A	J10.Pin2-3, R386	R400	U8.1	-	-
			TFT_QSSLA-A	J10.Pin2-3, R400	R386	TFT.32	-	-
ETORXER_RMII0RXER_QSPCLK-A	84	P77	ETORXER_RMII0RXER	SW6.9.ON	SW6.10.OFF	U6.58	-	-
			BD_QSPCLK-A	SW6.10.ON, R382	SW6.9.OFF, R232	U8.6	-	-
			TFT_QSPCLK-A	SW6.10.ON, R232	SW6.9.OFF, R382	TFT.29	R225	-

Table 6-17: Ethernet Option Links (1)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ET0TXEN_RMII0TXDEN_QIOA2-A_MTI0C3B	81	P80	ET0TXEN_RMII0TXDEN	SW7.1.ON	SW7.2.OFF, SW7.3.OFF	U6.48	-	-
			QIOA2-A	SW7.2.ON	SW7.1.OFF, SW7.3.OFF	U8.3	-	-
			MTI0C3B	SW7.3.ON	SW7.1.OFF, SW7.2.OFF	JA2.13	-	-
ET0ETXD0_RMII0TXD0_QIOA3-A_MTI0C3D	80	P81	ET0ETXD0_RMII0TXD0	SW7.4.ON	SW7.5.OFF, SW7.6.OFF	U6.43	-	-
			QIOA3-A	SW7.5.ON	SW7.4.OFF, SW7.6.OFF	U8.7	-	-
			MTI0C3D	SW7.6.ON	SW7.4.OFF, SW7.5.OFF	JA2.14	-	-
ET0ETXD1_RMII0TXD1_MTI0C4A_EDREQ1	79	P82	ET0ETXD1_RMII0TXD1	SW7.7.ON	SW7.8.OFF	U6.44	-	-
			EDREQ1	SW7.8.ON, R231	SW7.7.OFF, R453	JA6.1, TFT28	-	-
			MTI0C4A	SW7.8.ON, R453	SW7.7.OFF, R231	JA2.15	-	-
ET0CRS_RMII0CRSDV_MTI0C4C_EDACK1	74	P83	ET0CRS_RMII0CRSDV	SW7.9.ON	SW7.10.OFF	U6.60	R504	R503
			EDACK1	SW7.10.ON, R229	SW7.9.OFF, R454	JA6.2, TFT23	-	-
			MTI0C4C	SW7.10.ON, R454	SW7.9.OFF, R229	JA2.16	-	-
A16_ET0ERXD3_SSLA1-A	91	PC0	SSLA1-A	J11.Pin1-2	-	U7.1	-	-
			A16_ET0ERXD3	J11.Pin2-3	-	JA3.37	-	-
			ET0ERXD3	J11.Pin2-3, SW5.1.ON	-	JA3.37, U6.56	R54	-
A17_ET0ERXD2_MTI0C3A	89	PC1	A17_ET0ERXD2_MTI0C3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.55	R58	-
			MTI0C3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A18_ET0RXDV_MTI0C4B	86	PC2	A18_ET0RXDV_MTI0C4B	-	-	JA3.39	-	-
			ET0RXDV	SW5.4.ON	SW5.5.OFF	JA3.39, U6.57	R53	R503
			MTI0C4B	SW5.5.ON	SW5.4.OFF	JA3.39, JA2.17	-	-
A19_ET0TXER_QIOA0-A_MTI0C4D	83	PC3	A19_ET0TXER_QIOA0-A_MTI0C4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, U6.47	-	-
			BD_QIOA0-A	SW5.7.ON, R365	SW5.6.OFF, SW5.8.OFF, R364	JA3.40, U8.5	-	-
			TFT_QIOA0-A	SW5.7.ON, R364	SW5.6.OFF, SW5.8.OFF, R365	JA3.40, TFT.31	R233	-
			MTI0C4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-

Table 6-18: Ethernet Option Links (2)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
A20_ET0TXCLK_QIOA1-A_POE0n	82	PC4	A20_ET0TXCLK_QIOA1-A_POE0n	R339	-	JA3.41	-	-
			ET0TXCLK	R339, SW5.9.ON	SW5.10.OFF	JA3.41, U6.49	R71	-
			BD_QIOA1-A	R339, SW5.10.ON, R361	SW5.9.OFF, R360, R362	JA3.41, U8.2	-	-
			TFT_QIOA1-A	R339, SW5.10.ON, R360	SW5.9.OFF, R361, R362	JA3.41, TFT.30	R224	-
			POE0n	R339, SW5.10.ON, R362	SW5.9.OFF, R360, R361	JA3.41, JA2.24	-	-
A21_ET0ETXD2_RSPCKA-A	78	PC5	RSPCKA-A	J13.Pin1-2	-	U7.6	-	-
			A21_ET0ETXD2	J13.Pin2-3	-	JA3.42	-	-
			ET0ETXD2	J13.Pin2-3, SW6.1.ON	-	JA3.42, U6.45	-	-
A22_ET0ETXD3_MOSIA-A	77	PC6	MOSIA-A	J14.Pin1-2	-	U7.5	-	-
			A22_ET0ETXD3	J14.Pin2-3	-	JA3.43	-	-
			ET0ETXD3	J14.Pin2-3, SW6.2.ON	-	JA3.43, U6.46	-	-
ET0COL_MISOA-A_PC7	76	PC7	MISOA-A	J12.Pin1-2	-	U7.2	-	-
			ET0COL	J12.Pin2-3, SW6.3.ON	SW6.4.OFF	U6.21	R379	-
			PC7	J12.Pin2-3, SW6.4.ON	SW6.3.OFF	SW4.2 E1.10	- R248	- -

Table 6-19: Ethernet Option Links (3)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ET1MDIO	33	P30	ET1MDIO	-	-	U6.63	J3.Pin2-3	-
ET1MDC	32	P31	ET1MDC	-	-	U6.62	J4.Pin2-3	-
ET1TXEN_RMII1TXDEN_CS0n	141	P60	ET1TXEN_RMII1TXDEN	R374	R403	U6.28	-	-
			CS0n	R403	R374	JA3.45	R465	R466
ET1RXDV_A-TXD7_P-TXD7	163	P90	ET1RXDV	J16.Pin1-2	-	U6.39	R368	R500
			A-TXD7	J16.Pin2-3, R143	R414	U9.3 JA2.6	R141	R126, R134, R140
			P-TXD7	J16.Pin2-3, R414	R143	PMOD2.2	-	-
ET1COL_A-SCK7_P-SCK7	161	P91	ET1COL	J20.Pin1-2	-	U6.22	R378	-
			A-SCK7	J20.Pin2-3, R192	R419	JA2.10	-	-
			P-SCK7	J20.Pin2-3, R419	R192	PMOD2.4	-	-

Table 6-20: Ethernet Option Links (4)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ET1ERXD0_RMII1RXD0	157	P94	ET1ERXD0_RMII1RXD0	-	-	U6.35	-	-
ET1ERXD1_RMII1RXD1	155	P95	ET1ERXD1_RMII1RXD1	-	-	U6.36	-	-
ET1ERXD2_P96	152	P96	ET1ERXD2	R402	R159	U6.37	R370	-
			P96	R159	R402	PMOD2.9	-	-
ET1ERXD3_P97	149	P97	ET1ERXD3	R401	R168	U6.38	R369	-
			P97	R168	R401	PMOD2.10	-	-
ET1RXCLK_REF50CK1	146	PG0	ET1RXCLK	R90	R137	U6.41	R88	-
			REF50CK1	R137	R90	U6.33, X5.3	R105, R94	R95, R96, R118
ET1RXER_RMII1RXER	144	PG1	ET1RXER_RMII1RXER	-	-	U6.40	-	-
ET1TXCLK	123	PG2	ET1TXCLK	-	-	U6.29	R373	-
ET1ETXD0_RMII1TXD0	121	PG3	ET1ETXD0_RMII1TXD0	-	-	U6.23	-	-
ET1ETXD1_RMII1TXD1	119	PG4	ET1ETXD1_RMII1TXD1	-	-	U6.24	-	-
ET1ETXD2	116	PG5	ET1ETXD2	-	-	U6.25	-	-
ET1ETXD3	113	PG6	ET1ETXD3	-	-	U6.26	-	-
ET1TXER	111	PG7	ET1TXER	-	-	U6.27	-	-

Table 6-21: Ethernet Option Links (5)

6.11 General IO & LED Configuration

Table 6-22 and Table 6-23 below details the function of the option links associated with General IO & LED configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
AN005_YINPUT1_P45	167	P45	YINPUT1	R238	R131, R505	TFT.44	-	-
			AN005	R131	R238, R505	JA5.2	-	-
			P45	R505	R131, R238	PMOD1.1	R408	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R239	R123, R506	TFT.45	-	-
			AN006	R123	R239, R506	JA5.3	-	-
			P46	R506	R123, R239	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R240	R124, R507	TFT.46	-	-
			AN007	R124	R240, R507	JA5.4	-	-
			P47	R507	R124, R240	PMOD1.10	-	-
ET1ERXD2_P96	152	P96	ET1ERXD2	R402	R159	U6.37	R370	-
			P96	R159	R402	PMOD2.9	-	-
ET1ERXD3_P97	149	P97	ET1ERXD3	R401	R168	U6.38	R369	-
			P97	R168	R401	PMOD2.10	-	-
D8_IO0	135	PE0	D8	R440	R186	U13.42, JA3.29, TFT.15	-	-
			IO0	R186	R440	JA1.15	-	-
D9_IO1	134	PE1	D9	R439	R185	U13.44, JA3.30, TFT.16	-	-
			IO1	R185	R439	JA1.16	-	-
D10_IO2	133	PE2	D10	R438	R171	U13.45, JA3.31, TFT.17	-	-
			IO2	R171	R438	JA1.17	-	-
D11_IO3	132	PE3	D11	R226	R170	U13.47, JA3.32, TFT.18	-	-
			IO3	R170	R226	JA1.18	-	-
D12_IO4	131	PE4	D12	R227	R163	U13.48, JA3.33, TFT.19	-	-
			IO4	R163	R227	JA1.19	-	-
D13_IO5	130	PE5	D13	R228	R162	U13.50, JA3.34, TFT.20	-	-
			IO5	R162	R228	JA1.20	-	-

Table 6-22: General IO & LED Option Links (1)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
D14_SDCD-B_MTIOC6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U13.51, JA3.35, TFT.21	-	-
			SDCD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTIOC6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDWP-B_MTIOC6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U13.53, JA3.36, TFT.22	-	-
			SDWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTIOC6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-
LED0_DA0	4	P03	LED0	R277	R189	LED0	-	-
			DA0	R189	R277	JA1.13	-	-
LED1_DA1	2	P05	LED1	R280	R188	LED1	-	-
			DA1	R188	R280	JA1.14	-	-
LED2_MTIOC2A	37	P26	LED2	R281	R117	LED2	-	-
			MTIOC2A	R117	R281	JA5.9 TFT.27	R116	R111
LED3_MTIOC2B_BACKLIGHT	36	P27	LED3	J23.Pin1-2	-	LED3	-	-
			MTIOC2B	J23.Pin2-3, R169	R234	JA2.19	-	-
			BACKLIGHT	J23.Pin2-3, R234	R169	TFT.35	-	-

Table 6-23: General IO & LED Option Links (2)

6.12 I2C & EEPROM Configuration

Table 6-24 and Table 6-25 below details the function of the option links associated with I2C & EEPROM configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
USB0VBUS_USB0VBUSEN_SCL2-DS	48	P16	SCL2-DS	J27.Pin1-2	J6.Open	U14.6	R203	-
						JA1.26	R521	R522
			USB0VBUS	J6.Pin1-2	J27.Open	USB0 Function Bus-Powered	R52	R42
						USB0 Function Self-Powered	R42	R52
SSITXD0_PIXD3_SDA2-DS	46	P17	SSITXD0	R288	R273, R518	J25.12	-	-
			PIXD3	R273	R288, R518	J26.15	-	-
			SDA2-DS	R518	R273, R288	U14.5	R198	-
						JA1.25	R519	R520

Table 6-24: I2C & EEPROM Option Links (1)

Reference	Exclusive Function			Connection
	Function	Enable	Disable	Interface Function
SSDA2, SSCL2	Connects pull-up resistor to Board_3V3.	R527	R528	SSDA2, SSCL2
	Connects pull-up resistor to Board_5V.	R528	R527	SSDA2, SSCL2
SSDA6, SSCL6	Connects pull-up resistor to Board_3V3.	R533	R534	SSDA6, SSCL6
	Connects pull-up resistor to Board_5V.	R534	R533	SSDA6, SSCL6
SDA2-DS, SCL2-DS	Connects pull-up resistor and EEPROM power pin to Board_3V3.	R219	R218	SDA2-DS, SCL2-DS, U14
	Connects pull-up resistor and EEPROM power pin to Board_5V.	R218	R219	SDA2-DS, SCL2-DS, U14

Table 6-25: I2C & EEPROM Option Links (2)

6.13 MTU & TPU & POE Configuration

Table 6-26 to Table 6-29 below details the function of the option links associated with MTU & TPU & POE configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
USBAOVRCURA_ALE_MTIC5W	68	P10	USBAOVRCURA	R351	R83, R478	U3.2	R4	R29
			ALE	R478	R83, R351	U4.5	R29	R4
			MTIC5W	R83	R351, R478	JA3.46	R464	R445
						JA5.14	R86	R82
USBAVBUS_USBAVBUSEN_MTIC5V	67	P11	MTIC5V	R40	J9.Open	JA6.16	R82	R86
			USBAVBUS	J9.Pin1-2	R40	JA5.13	R87	R68
						JA6.15	R68	R87
			USBAVBUSEN	J9.Pin2-3	R40	J8.1	J8.Pin1-2	-
						J8.3	J8.Pin2-3	-
MTIC5U_IRQ2	53	P12	MTIC5U	R92	R536	U3.1	R5	R30
			IRQ2	R536	R92	U4.4	R30	R5
P13	52	P13	MTIOC0B_IRQ3	R517	R516	JA5.12	R93	R91
						JA6.14	R91	R93
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R317	R36, R136, R270, R286	JA2.9	R201	R111
			USBAID	R36	R136, R270, R286, R317	JA5.9	R111	R116, R201
			SSIRXD0	R286	R36, R136, R270, R317	PMOD1.7	-	-
			PIXD4	R270	R36, R136, R286, R317	U4.3	-	-
			MTIOC1A	R136	R36, R270, R286, R317	J25.10	-	-
					J26.14	-	-	
					JA2.23	R146	R147	

Table 6-26: MTU & TPU & POE Option Links (1)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
USBAOVR CURB_AUDIOCLK_PIXD6_MTCLKC	43	P22	AUDIOCLK	R285	R77, R268, R321	J25.5	-	-
			USBAOVR CURB	R321	R77, R268, R285	U4.6	-	-
			PIXD6	R268	R77, R285, R321	J26.12	-	-
			MTCLKC	R77	R268, R285, R321	JA5.17	-	-
SSISCK0_PIXD7_MTCLKD	42	P23	SSISCK0	R287	R75, R269	J25.9	-	-
			PIXD7	R269	R75, R287	J26.11	-	-
			MTCLKD	R75	R269, R287	JA5.18	-	-
PIXCLK_MTCLKA	40	P24	PIXCLK	R265	R135	J26.8	-	-
			MTCLKA	R135	R265	JA2.25	-	-
HSYNC_MTCLKB	38	P25	HSYNC	R266	R128	J26.10	-	-
			MTCLKB	R128	R266	JA2.26	-	-
LED2_MTI0C2A	37	P26	LED2	R281	R117	LED2	-	-
			MTI0C2A	R117	R281	JA5.9 TFT.27	R116	R111
LED3_MTI0C2B_BACKLIGHT	36	P27	LED3	J23.Pin1-2	-	LED3	-	-
			MTI0C2B	J23.Pin2-3, R169	R234	JA2.19	-	-
			BACKLIGHT	J23.Pin2-3, R234	R169	TFT.35	-	-
CTX0_VSYNC_MTI0C0C_IRQ2-DS	29	P32	VSYNC	R267	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R267	U12.1 JA5.5	R208	-
			MTI0C0C_IRQ2-DS	J15.Pin2-3	R267	JA2.23 JA5.10	R147 R103	R146
CRX0_PCKO_MTI0C0D	28	P33	PCKO	R290	J17.Open	J26.5	-	-
			CRX0	J17.Pin1-2	R290	U12.4 JA5.6	R191	-
			MTI0C0D	J17.Pin2-3	R290	JA2.21	-	-
ET0LINKSTA_MTI0C0A_IRQ4	27	P34	ET0LINKSTA	SW6.5.ON	SW6.6.OFF	U6.69, ETHERNET0.11	-	-
			MTI0C0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23 JA2.7 TFT.25	R148 R211	R497
DQM0_MTI0C7D	122	P66	DQM0	R428	R51	U13.15 JA3.48	R427	R462
			MTI0C7D	R51	R428	JA5.24	-	-
DQM1_MTI0C7C	120	P67	DQM1	R441	R62	U13.39 JA3.47	R442	R463
			MTI0C7C	R62	R441	JA5.22	-	-
ET0TXEN_RMII0TXDEN_QIOA2-A_MTI0C3B	81	P80	ET0TXEN_RMII0TXDEN	SW7.1.ON	SW7.2.OFF, SW7.3.OFF	U6.48	-	-
			QIOA2-A	SW7.2.ON	SW7.1.OFF, SW7.3.OFF	U8.3	-	-
			MTI0C3B	SW7.3.ON	SW7.1.OFF, SW7.2.OFF	JA2.13	-	-
ET0ETXD0_RMII0TXD0_QIOA3-A_MTI0C3D	80	P81	ET0ETXD0_RMII0TXD0	SW7.4.ON	SW7.5.OFF, SW7.6.OFF	U6.43	-	-
			QIOA3-A	SW7.5.ON	SW7.4.OFF, SW7.6.OFF	U8.7	-	-
			MTI0C3D	SW7.6.ON	SW7.4.OFF, SW7.5.OFF	JA2.14	-	-

Table 6-27: MTU & TPU & POE Option Links (2)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ET0ETXD1_RMII0TXD1_MTIOC4A_EDREQ1	79	P82	ET0ETXD1_RMII0TXD1	SW7.7.ON	SW7.8.OFF	U6.44	-	-
			EDREQ1	SW7.8.ON, R231	SW7.7.OFF, R453	JA6.1, TFT28	-	-
			MTIOC4A	SW7.8.ON, R453	SW7.7.OFF, R231	JA2.15	-	-
ET0CRS_RMII0CRSDV_MTIOC4C_EDACK1	74	P83	ET0CRS_RMII0CRSDV	SW7.9.ON	SW7.10.OFF	U6.60	R504	R503
			EDACK1	SW7.10.ON, R229	SW7.9.OFF, R454	JA6.2, TFT23	-	-
			MTIOC4C	SW7.10.ON, R454	SW7.9.OFF, R229	JA2.16	-	-
PIXD1_TIOCA0	49	P86	PIXD1	R275	R160	J26.17	-	-
			TIOCA0	R160	R275	JA2.22	-	-
PIXD2_TIOCA2	47	P87	PIXD2	R272	R161	J26.16	-	-
			TIOCA2	R161	R272	JA2.20	-	-
A0_MTIOC6D	118	PA0	A0	R250	R69	JA3.1	-	-
			MTIOC6D	R69	R250	JA5.20	-	-
A1_MTIOC7B	114	PA1	A1	R423	R63	U13.23, JA3.2	-	-
			MTIOC7B	R63	R423	JA5.23	-	-
A2_MTIOC7A	112	PA2	A2	R424	R70	U13.24, JA3.3	-	-
			MTIOC7A	R70	R424	JA5.21	-	-
A5_MTIOC6B	108	PA5	A5	R448	R76	U13.29, JA3.6	-	-
			MTIOC6B	R76	R448	JA5.19	-	-
A13_POE4n	96	PB5	A13	R344, R422	R80	U13.20, JA3.14	-	-
			POE4n	R344, R80	R422	JA5.16	-	-
A17_ET0ERXD2_MTIOC3A	89	PC1	A17_ET0ERXD2_MTIOC3A	-	-	JA3.38	-	-
			ET0ERXD2	SW5.2.ON	SW5.3.OFF	JA3.38, U6.55	R58	-
			MTIOC3A	SW5.3.ON	SW5.2.OFF	JA3.38, JA6.13, TFT.26	-	-
A18_ET0RXDV_MTIOC4B	86	PC2	A18_ET0RXDV_MTIOC4B	-	-	JA3.39	-	-
			ET0RXDV	SW5.4.ON	SW5.5.OFF	JA3.39, U6.57	R53	R503
			MTIOC4B	SW5.5.ON	SW5.4.OFF	JA3.39, JA2.17	-	-
A19_ET0TXER_QIOA0-A_MTIOC4D	83	PC3	A19_ET0TXER_QIOA0-A_MTIOC4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, U6.47	-	-
			BD_QIOA0-A	SW5.7.ON, R365	SW5.6.OFF, SW5.8.OFF, R364	JA3.40, U8.5	-	-
			TFT_QIOA0-A	SW5.7.ON, R364	SW5.6.OFF, SW5.8.OFF, R365	JA3.40, TFT.31	R233	-
			MTIOC4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-

Table 6-28: MTU & TPU & POE Option Links (3)

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
A20_ET0TXCLK_QIOA1-A_POE0n	82	PC4	A20_ET0TXCLK_QIOA1-A_POE0n	R339	-	JA3.41	-	-
			ET0TXCLK	R339, SW5.9.ON	SW5.10.OFF	JA3.41, U6.49	R71	-
			BD_QIOA1-A	R339, SW5.10.ON, R361	SW5.9.OFF, R360, R362	JA3.41, U8.2	-	-
			TFT_QIOA1-A	R339, SW5.10.ON, R360	SW5.9.OFF, R361, R362	JA3.41, TFT.30	R224	-
			POE0n	R339, SW5.10.ON, R362	SW5.9.OFF, R360, R361	JA3.41, JA2.24	-	-
D14_SDCD-B_MTI0C6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U13.51, JA3.35, TFT.21	-	-
			SDCD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTI0C6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDWP-B_MTI0C6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U13.53, JA3.36, TFT.22	-	-
			SDWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTI0C6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-
CTS6RTS6_MTI0C3C	13	PJ3	CTS6RTS6	R318	R230	PMOD1.1	R1	R408
			MTI0C3C	R230	R318	JA2.11, TFT.24	-	-

Table 6-29: MTU & TPU & POE Option Links (4)

6.14 IRQ & NMI & Switch Configuration

Table 6-30 below details the function of the option links associated with IRQ & NMI & Switch configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ADTRG0n	176	P07	ADTRG0n	-	-	SW3 JA1.8	R494 -	- -
MTIC5U_IRQ2	53	P12	MTIC5U	R92	R536	JA5.12 JA6.14	R93 R91	R91 R93
			IRQ2	R536	R92	SW2	R496	-
PIXD0_IRQ5	50	P15	IRQ5	R490	R274	SW1 JA1.23	R498 R497	- R148
			PIXD0	R274	R490	J26.18	-	-
USBAID_SSIKXD0_PIXD4_MTI OC1A_IRQ8	45	P20	IRQ8	R317	R36, R136, R270, R286	PMOD1.7	-	-
			USBAID	R36	R136, R270, R286, R317	U4.3	-	-
			SSIKXD0	R286	R36, R136, R270, R317	J25.10	-	-
			PIXD4	R270	R36, R136, R286, R317	J26.14	-	-
USBAEXICEN_SSIWS0_PIXD5_ IRQ9	44	P21	IRQ9	R330	R271, R289, R329	PMOD1.8	-	-
			USBAEXICEN	R329	R271, R289, R330	U4.11	-	-
			SSIWS0	R289	R271, R329, R330	J25.11	-	-
			PIXD5	R271	R289, R329, R330	J26.13	-	-
CTX0_VSYNC_MTI0C0C_IRQ2- DS	29	P32	VSYNC	R267	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R267	U12.1 JA5.5	R208 -	- -
			MTI0C0C_IRQ2-DS	J15.Pin2-3	R267	JA2.23 JA5.10	R147 R103	R146 -
ET0LINKSTA_MTI0C0A_IRQ4	27	P34	ET0LINKSTA	SW6.5.ON	SW6.6.OFF	U6.69, ETHERNET0.11	-	-
			MTI0C0A_IRQ4	SW6.6.ON	SW6.5.OFF	JA1.23	R148	R497
						JA2.7 TFT.25	R211	- -
AN002_IRQ10-DS	170	P42	AN002	R200	R145	JA1.11	-	-
			IRQ10-DS	R145	R200	PMOD2.7	-	-
AN003_IRQ11-DS	169	P43	AN003	R199	R152	JA1.12	-	-
			IRQ11-DS	R152	R199	PMOD2.8	-	-

Table 6-30: IRQ & Switch Option Links

6.15 PDC Configuration

Table 6-31 and Table 6-32 below detail the function of the option links associated with PDC configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
TXD6_SSDA6	8	P00	TXD6	R508	-	PMOD1.2	-	-
			SSDA6	R511	-	J26.19	R303	-
RXD6_SSCL6	7	P01	RXD6	R512	-	PMOD1.3	-	-
			SSCL6	R513	-	J26.20	R302	-
PIXD0_IRO5	50	P15	IRO5	R490	R274	SW1	R498	-
			PIXD0	R274	R490	JA1.23	R497	R148
SSITXD0_PIXD3_SDA2-DS	46	P17	SSITXD0	R288	R273, R518	J25.12	-	-
			PIXD3	R273	R288, R518	J26.15	-	-
			SDA2-DS	R518	R273, R288	U14.5	R198	-
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRO8	R317	R36, R136, R270, R286	PMOD1.7	-	-
			USBAID	R36	R136, R270, R286, R317	U4.3	-	-
			SSIRXD0	R286	R36, R136, R270, R317	J25.10	-	-
			PIXD4	R270	R36, R136, R286, R317	J26.14	-	-
			MTIOC1A	R136	R36, R270, R286, R317	JA2.23	R146	R147
USBAEXICEN_SSIWS0_PIXD5_IRO9	44	P21	IRO9	R330	R271, R289, R329	PMOD1.8	-	-
			USBAEXICEN	R329	R271, R289, R330	U4.11	-	-
			SSIWS0	R289	R271, R329, R330	J25.11	-	-
USBAOVRCURB_AUDIOCLK_PIXD6_MTCLKC	43	P22	AUDIOCLK	R285	R77, R268, R321	J25.5	-	-
			USBAOVRCURB	R321	R77, R268, R285	U4.6	-	-
			PIXD6	R268	R77, R285, R321	J26.12	-	-
			MTCLKC	R77	R268, R285, R321	JA5.17	-	-
SSISCK0_PIXD7_MTCLKD	42	P23	SSISCK0	R287	R75, R269	J25.9	-	-
			PIXD7	R269	R75, R287	J26.11	-	-
			MTCLKD	R75	R269, R287	JA5.18	-	-
PIXCLK_MTCLKA	40	P24	PIXCLK	R265	R135	J26.8	-	-
			MTCLKA	R135	R265	JA2.25	-	-
HSYNC_MTCLKB	38	P25	HSYNC	R266	R128	J26.10	-	-
			MTCLKB	R128	R266	JA2.26	-	-
CTX0_VSYNC_MTIOC0C_IRQ2-DS	29	P32	VSYNC	R267	J15.Open	J26.9	-	-
			CTX0	J15.Pin1-2	R267	U12.1	R208	-
			MTIOC0C_IRQ2-DS	J15.Pin2-3	R267	JA5.5	-	-
CRX0_PCKO_MTIOC0D	28	P33	PCKO	R290	J17.Open	J26.5	-	-
			CRX0	J17.Pin1-2	R290	U12.4	R191	-
			MTIOC0D	J17.Pin2-3	R290	JA5.6	-	-
			MTIOC0D	J17.Pin2-3	R290	JA2.21	-	-
PIXD1_TIOCA0	49	P86	PIXD1	R275	R160	J26.17	-	-
			TIOCA0	R160	R275	JA2.22	-	-
PIXD2_TIOCA2	47	P87	PIXD2	R272	R161	J26.16	-	-
			TIOCA2	R161	R272	JA2.20	-	-

Table 6-31: PDC Interface Option Links(1)

Reference	Exclusive Function			Connection
	Function	Enable	Disable	Interface / Function
SSDA6, SSCL6	Connects pull-up resistor to Board_3V3.	R533	R534	SSDA6, SSCL6
	Connects pull-up resistor to Board_5V.	R534	R533	SSDA6, SSCL6

Table 6-32: PDC Interface Option Links (2)

6.16 PMOD1 Configuration

Table 6-33 below details the function of the option links associated with PMOD1 Interface configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
TXD6_SSDA6	8	P00	TXD6	R508	-	PMOD1.2	-	-
			SSDA6	R511	-	J26.19	R303	-
RXD6_SSCL6	7	P01	RXD6	R512	-	PMOD1.3	-	-
			SSCL6	R513	-	J26.20	R302	-
SCK6	6	P02	SCK6	-	-	PMOD1.4	-	-
USBAID_SSIRXD0_PIXD4_MTI0C1A_IRQ8	45	P20	IRQ8	R317	R36, R136, R270, R286	PMOD1.7	-	-
			USBAID	R36	R136, R270, R286, R317	U4.3	-	-
			SSIRXD0	R286	R36, R136, R270, R317	J25.10	-	-
			PIXD4	R270	R36, R136, R286, R317	J26.14	-	-
			MTI0C1A	R136	R36, R270, R286, R317	JA2.23	R146	R147
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R330	R271, R289, R329	PMOD1.8	-	-
			USBAEXICEN	R329	R271, R289, R330	U4.11	-	-
			SSIWS0	R289	R271, R329, R330	J25.11	-	-
			PIXD5	R271	R289, R329, R330	J26.13	-	-
AN005_YINPUT1_P45	167	P45	YINPUT1	R238	R131, R505	TFT.44	-	-
			AN005	R131	R238, R505	JA5.2	-	-
			P45	R505	R131, R238	PMOD1.1	R408	R1
AN006_XINPUT2_P46	166	P46	XINPUT2	R239	R123, R506	TFT.45	-	-
			AN006	R123	R239, R506	JA5.3	-	-
			P46	R506	R123, R239	PMOD1.9	-	-
AN007_YINPUT2_P47	165	P47	YINPUT2	R240	R124, R507	TFT.46	-	-
			AN007	R124	R240, R507	JA5.4	-	-
			P47	R507	R124, R240	PMOD1.10	-	-
CTS6RTS6_MTI0C3C	13	PJ3	CTS6RTS6	R318	R230	PMOD1.1	R1	R408
			MTI0C3C	R230	R318	JA2.11, TFT.24	-	-

Table 6-33: PMOD1 Interface Option Links

6.17 PMOD2 Configuration

Table 6-34 below details the function of the option links associated with PMOD2 Interface configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
AN002_IRQ10-DS	170	P42	AN002	R200	R145	JA1.11	-	-
			IRQ10-DS	R145	R200	PMOD2.7	-	-
AN003_IRQ11-DS	169	P43	AN003	R199	R152	JA1.12	-	-
			IRQ11-DS	R152	R199	PMOD2.8	-	-
ET1RXDV_A-TXD7_P-TXD7	163	P90	ET1RXDV	J16.Pin1-2	-	U6.39	R368	R500
			A-TXD7	J16.Pin2-3, R143	R414	U9.3	R141	R126, R134, R140
			P-TXD7	J16.Pin2-3, R414	R143	JA2.6	-	-
ET1COL_A-SCK7_P-SCK7	161	P91	ET1COL	J20.Pin1-2	-	U6.22	R378	-
			A-SCK7	J20.Pin2-3, R192	R419	JA2.10	-	-
			P-SCK7	J20.Pin2-3, R419	R192	PMOD2.4	-	-
ET1CRS_RMII1CRSDV_A-RXD7_P-RXD7	160	P92	ET1CRS_RMII1CRSDV	J18.Pin1-2	-	U6.42	R501	R500
			A-RXD7	J18.Pin2-3, R166	R417	U10.3	R165	R149, R150, R156
			P-RXD7	J18.Pin2-3, R417	R166	JA2.8	-	-
ET1LINKSTA_A-CTS7RTS7_P-CTS7RTS7	159	P93	ET1LINKSTA	R409	R187, R410	U6.67, ETHERNET1.11	-	-
			A-CTS7RTS7	R187	R409, R410	JA2.12	-	-
			P-CTS7RTS7	R410	R187, R409	PMOD2.1	-	-
ET1ERXD2_P96	152	P96	ET1ERXD2	R402	R159	U6.37	R370	-
			P96	R159	R402	PMOD2.9	-	-
ET1ERXD3_P97	149	P97	ET1ERXD3	R401	R168	U6.38	R369	-
			P97	R168	R401	PMOD2.10	-	-

Table 6-34: PMOD2 Interface Option Links

6.18 QSPI Configuration

Table 6-35 below details the function of the option links associated with QSPI configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
ET0RXCLK_REF50CK0_QSSLA-A	85	P76	REF50CK0	J10.Pin1-2, R57	R48	U6.33, X5.3	R94, R106	R95, R96, R118
			ET0RXCLK	J10.Pin1-2, R48	R57	U6.59	R44	-
			BD_QSSLA-A	J10.Pin2-3, R386	R400	U8.1	-	-
			TFT_QSSLA-A	J10.Pin2-3, R400	R386	TFT.32	-	-
ET0RXER_RMII0RXER_QSPCLK-A	84	P77	ET0RXER_RMII0RXER	SW6.9.ON	SW6.10.OFF	U6.58	-	-
			BD_QSPCLK-A	SW6.10.ON, R382	SW6.9.OFF, R232	U8.6	-	-
			TFT_QSPCLK-A	SW6.10.ON, R232	SW6.9.OFF, R382	TFT.29	R225	-
ET0TXEN_RMII0TXDEN_QIOA2-A_MTI0C3B	81	P80	ET0TXEN_RMII0TXDEN	SW7.1.ON	SW7.2.OFF, SW7.3.OFF	U6.48	-	-
			QIOA2-A	SW7.2.ON	SW7.1.OFF, SW7.3.OFF	U8.3	-	-
			MTI0C3B	SW7.3.ON	SW7.1.OFF, SW7.2.OFF	JA2.13	-	-
ET0ETXD0_RMII0TXD0_QIOA3-A_MTI0C3D	80	P81	ET0ETXD0_RMII0TXD0	SW7.4.ON	SW7.5.OFF, SW7.6.OFF	U6.43	-	-
			QIOA3-A	SW7.5.ON	SW7.4.OFF, SW7.6.OFF	U8.7	-	-
			MTI0C3D	SW7.6.ON	SW7.4.OFF, SW7.5.OFF	JA2.14	-	-
A19_ET0TXER_QIOA0-A_MTI0C4D	83	PC3	A19_ET0TXER_QIOA0-A_MTI0C4D	-	-	JA3.40	-	-
			ET0TXER	SW5.6.ON	SW5.7.OFF, SW5.8.OFF	JA3.40, U6.47	-	-
			BD_QIOA0-A	SW5.7.ON, R365	SW5.6.OFF, SW5.8.OFF, R364	JA3.40, U8.5	-	-
			TFT_QIOA0-A	SW5.7.ON, R364	SW5.6.OFF, SW5.8.OFF, R365	JA3.40, TFT.31	R233	-
			MTI0C4D	SW5.8.ON	SW5.6.OFF, SW5.7.OFF	JA3.40, JA2.18	-	-
A20_ET0TXCLK_QIOA1-A_POE0n	82	PC4	A20_ET0TXCLK_QIOA1-A_POE0n	R339	-	JA3.41	-	-
			ET0TXCLK	R339, SW5.9.ON	SW5.10.OFF	JA3.41, U6.49	R71	-
			BD_QIOA1-A	R339, SW5.10.ON, R361	SW5.9.OFF, R360, R362	JA3.41, U8.2	-	-
			TFT_QIOA1-A	R339, SW5.10.ON, R360	SW5.9.OFF, R361, R362	JA3.41, TFT.30	R224	-
			POE0n	R339, SW5.10.ON, R362	SW5.9.OFF, R360, R361	JA3.41, JA2.24	-	-

Table 6-35: QSPI Option Links

6.19 RSPI Configuration

Table 6-36 below details the function of the option links associated with RSPI configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
A16_ET0ERXD3_SSLA1-A	91	PC0	SSLA1-A	J11.Pin1-2	-	U7.1	-	-
			A16_ET0ERXD3	J11.Pin2-3	-	JA3.37	-	-
			ET0ERXD3	J11.Pin2-3, SW5.1.ON	-	JA3.37, U6.56	R54	-
A21_ET0ETXD2_RSPCKA-A	78	PC5	RSPCKA-A	J13.Pin1-2	-	U7.6	-	-
			A21_ET0ETXD2	J13.Pin2-3	-	JA3.42	-	-
			ET0ETXD2	J13.Pin2-3, SW6.1.ON	-	JA3.42, U6.45	-	-
A22_ET0ETXD3_MOSIA-A	77	PC6	MOSIA-A	J14.Pin1-2	-	U7.5	-	-
			A22_ET0ETXD3	J14.Pin2-3	-	JA3.43	-	-
			ET0ETXD3	J14.Pin2-3, SW6.2.ON	-	JA3.43, U6.46	-	-
ET0COL_MISOA-A_PC7	76	PC7	MISOA-A	J12.Pin1-2	-	U7.2	-	-
			ET0COL	J12.Pin2-3, SW6.3.ON	SW6.4.OFF	U6.21	R379	-
			PC7	J12.Pin2-3, SW6.4.ON	SW6.3.OFF	SW4.2 E1.10	-	R248

Table 6-36: RSPI Option Links

6.20 SDHI Configuration

Table 6-37 below details the function of the option links associated with SD Host Interface configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
D2_SDD2-B	154	PD2	D2	SW8.1.ON	SW8.2.OFF	U13.5, JA3.19, TFT.9	-	-
			SDD2-B	SW8.2.ON	SW8.1.OFF	SD1.9	-	-
D3_SDD3-B	150	PD3	D3	SW8.3.ON	SW8.4.OFF	U13.7, JA3.20, TFT.10	-	-
			SDD3-B	SW8.4.ON	SW8.3.OFF	SD1.1	-	-
D4_SDCMD-B	148	PD4	D4	SW8.5.ON	SW8.6.OFF	U13.8, JA3.21, TFT.11	-	-
			SDCMD-B	SW8.6.ON	SW8.5.OFF	SD1.2	-	-
D5_SDCLK-B	147	PD5	D5	SW8.7.ON	SW8.8.OFF	U13.10, JA3.22, TFT.12	-	-
			SDCLK-B	SW8.8.ON	SW8.7.OFF	SD1.5	-	-
D6_SDD0-B	145	PD6	D6	SW8.9.ON	SW8.10.OFF	U13.11, JA3.23, TFT.13	-	-
			SDD0-B	SW8.10.ON	SW8.9.OFF	SD1.7	-	-
D7_SDD1-B	143	PD7	D7	SW9.1.ON	SW9.2.OFF	U13.13, JA3.24, TFT.14	-	-
			SDD1-B	SW9.2.ON	SW9.1.OFF	SD1.8	-	-
D14_SDCCD-B_MTI0C6C_IO6	126	PE6	D14	SW9.3.ON	SW9.4.OFF, SW9.5.OFF, SW9.6.OFF	U13.51, JA3.35, TFT.21	-	-
			SDCCD-B	SW9.4.ON	SW9.3.OFF, SW9.5.OFF, SW9.6.OFF	SD1.10	-	-
			MTI0C6C	SW9.5.ON	SW9.3.OFF, SW9.4.OFF, SW9.6.OFF	JA5.11	-	-
			IO6	SW9.6.ON	SW9.3.OFF, SW9.4.OFF, SW9.5.OFF	JA1.21	-	-
D15_SDWP-B_MTI0C6A_IO7	125	PE7	D15	SW9.7.ON	SW9.8.OFF, SW9.9.OFF, SW9.10.OFF	U13.53, JA3.36, TFT.22	-	-
			SDWP-B	SW9.8.ON	SW9.7.OFF, SW9.9.OFF, SW9.10.OFF	SD1.12	-	-
			MTI0C6A	SW9.9.ON	SW9.7.OFF, SW9.8.OFF, SW9.10.OFF	JA5.15	-	-
			IO7	SW9.10.ON	SW9.7.OFF, SW9.8.OFF, SW9.9.OFF	JA1.22	-	-

Table 6-37: SD Host Interface Option Links

6.21 Serial & USB to Serial Configuration

Table 6-38 below details the function of the option links associated with Serial & USB to Serial configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
AN001_RXCTS_YDRIVE	171	P41	AN001	R204	R236, R421	JA1.10	-	-
			RXCTS	R421	R204, R236	U10.2	-	-
			YDRIVE	R236	R204, R421	TFT.42	-	-
WRn_WR0n_TXD2_SSDA2	72	P50	WRn	R115	R114, R119, R514	JA3.26	R387	R429
			WR0n	R119	R114, R115, R514	JA3.48	R462	R427
			TXD2	R114	R115, R119, R514	U9.3	R126	R134, R140, R141
			SSDA2	R514	R114, R115, R119	JA6.9	-	-
WR1n_WAITn_SCK2	71	P51	WAITn	R481	R476, R482	JA3.45	R466	R465
			WR1n	R476	R481, R482	JA3.47	R463	R442
			SCK2	R482	R476, R481	JA6.11	-	-
RDn_RXD2_SSCL2	70	P52	RDn	R100	R99, R515	JA3.25	-	-
			RXD2	R99	R100, R515	U10.3	R150	R149, R156, R165
			SSCL2	R515	R99, R100	JA6.12	-	-
ET1RXDV_A-TXD7_P-TXD7	163	P90	ET1RXDV	J16.Pin1-2	-	U6.39	R368	R500
			A-TXD7	J16.Pin2-3, R143	R414	U9.3	R141	R126, R134, R140
			P-TXD7	J16.Pin2-3, R414	R143	JA2.6	-	-
ET1COL_A-SCK7_P-SCK7	161	P91	ET1COL	J20.Pin1-2	-	U6.22	R378	-
			A-SCK7	J20.Pin2-3, R192	R419	JA2.10	-	-
			P-SCK7	J20.Pin2-3, R419	R192	PMOD2.4	-	-
ET1CRS_RMII1CRS_DV_A-RXD7_P-RXD7	160	P92	ET1CRS_RMII1CRSDV	J18.Pin1-2	-	U6.42	R501	R500
			A-RXD7	J18.Pin2-3, R166	R417	U10.3	R165	R149, R150, R156
			P-RXD7	J18.Pin2-3, R417	R166	JA2.8	-	-
TDO_TXD1	35	PF0	TDO	R255	R142	E1.5	-	-
			TXD1	R142	R255	U9.3	R140	R126, R134, R141
TCK_SCK1	34	PF1	TCK	R263	R381	E1.1	-	-
			SCK1	R381	R263	JA6.10	R108	-
TDI_RXD1	31	PF2	TDI	R246	R157	E1.11	-	-
			RXD1	R157	R246	U10.3	R156	R149, R150, R165
RXRTS_XDRIVE	11	PJ5	RXRTS	R412	R235	U9.2	-	-
			XDRIVE	R235	R412	TFT.41	-	-
RS232TX	-	-	RS232TX	-	-	U9.3	R134	R126, R140, R141
RS232RX	-	-	RS232RX	-	-	U10.3	R149	R150, R156, R165

Table 6-38: Serial & USB to Serial Option Links

6.22 SSI Configuration

Table 6-39 below details the function of the option links associated with Serial Sound Interface configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
SSITXD0_PIXD3_SDA2-DS	46	P17	SSITXD0	R288	R273, R518	J25.12	-	-
			PIXD3	R273	R288, R518	J26.15	-	-
			SDA2-DS	R518	R273, R288	U14.5	R198	-
						JA1.25	R519	R520
USBAID_SSIRXD0_PIXD4_MTIOC1A_IRQ8	45	P20	IRQ8	R317	R36, R136, R270, R286	PMOD1.7	-	-
			USBAID	R36	R136, R270, R286, R317	U4.3	-	-
			SSIRXD0	R286	R36, R136, R270, R317	J25.10	-	-
			PIXD4	R270	R36, R136, R286, R317	J26.14	-	-
			MTIOC1A	R136	R36, R270, R286, R317	JA2.23	R146	R147
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R330	R271, R289, R329	PMOD1.8	-	-
			USBAEXICEN	R329	R271, R289, R330	U4.11	-	-
			SSIWS0	R289	R271, R329, R330	J25.11	-	-
			PIXD5	R271	R289, R329, R330	J26.13	-	-
USBAOVR CURB_AUDIOCLK_PIXD6_MTCLKC	43	P22	AUDIOCLK	R285	R77, R268, R321	J25.5	-	-
			USBAOVR CURB	R321	R77, R268, R285	U4.6	-	-
			PIXD6	R268	R77, R285, R321	J26.12	-	-
			MTCLKC	R77	R268, R285, R321	JA5.17	-	-
SSISCK0_PIXD7_MTCLKD	42	P23	SSISCK0	R287	R75, R269	J25.9	-	-
			PIXD7	R269	R75, R287	J26.11	-	-
			MTCLKD	R75	R269, R287	JA5.18	-	-

Table 6-39: Serial Sound Interface Option Links

6.23 USB Configuration

Table 6-40 and **Table 6-41** below details the function of the option links associated with the USB Configuration.

Signal name	MCU		Exclusive Function			Connection		
	Pin	Port	Signal	Enable	Disable	Interface Function	Enable	Disable
USBAOVRCURA_ALE_MTIC5W	68	P10	USBAOVRCURA	R351	R83, R478	U3.2	R4	R29
			ALE	R478	R83, R351	U4.5	R29	R4
			MTIC5W	R83	R351, R478	JA3.46	R464	R445
						JA5.14	R86	R82
USBAVBUS_USBAVBUSEN_MTIC5V	67	P11	MTIC5V	R40	J9.Open	JA6.16	R82	R86
			USBAVBUS	J9.Pin1-2	R40	JA5.13	R87	R68
						JA6.15	R68	R87
			USBAVBUSEN	J9.Pin2-3	R40	J8.1	J8.Pin1-2	-
USB00VRCURA	51	P14	USB00VRCURA	-	-	J8.3	J8.Pin2-3	-
						U3.1	R5	R30
USB0VBUS_USB0VBUSEN_SCL2-DS	48	P16	SCL2-DS	J27.Pin1-2	J6.Open	U4.4	R30	R5
			USB0VBUS	J6.Pin1-2	J27.Open	U5.2	-	-
						U14.6	R203	-
			USB0VBUSEN	J6.Pin2-3	J27.Open	JA1.26	R521	R522
USBAID_SSIWXD0_PIXD4_MTI0C1A_IRQ8	45	P20	IRQ8	R317	R36, R136, R270, R286	USB0 Function Bus-Powered	R52	R42
			USBAID	R36	R136, R270, R286, R317	USB0 Function Self-Powered	R42	R52
			SSIWXD0	R286	R36, R136, R270, R317	U5.1	-	-
			PIXD4	R270	R36, R136, R286, R317	PMOD1.7	-	-
			MTI0C1A	R136	R36, R270, R286, R317	U4.3	-	-
USBAEXICEN_SSIWS0_PIXD5_IRQ9	44	P21	IRQ9	R330	R271, R289, R329	J25.10	-	-
			USBAEXICEN	R329	R271, R289, R330	J26.14	-	-
			SSIWS0	R289	R271, R329, R330	J25.11	-	-
			PIXD5	R271	R289, R329, R330	J26.13	-	-
USBAOVRCURB_AUDIOCLK_PIXD6_MTCLKC	43	P22	AUDIOCLK	R285	R77, R268, R321	JA2.23	R146	R147
			USBAOVRCURB	R321	R77, R268, R285	U4.11	-	-
			PIXD6	R268	R77, R285, R321	J25.5	-	-
			MTCLKC	R77	R268, R285, R321	U4.6	-	-

Table 6-40: USB Option Links (1)

Reference	Exclusive Function			Connection
	Function	Enable	Disable	Interface Function
USB0VBUS	Enables Self-powered.	R42	R52	J2
	Enables Bus-powered.	R52	R42	J2
ILIM	Sets current limit as 0.7A.	R3	R15	U3.4
	Sets current limit as 1.95A.	R15	R3	U3.4
VBUSA	Enables USBA OTG mode.	R37	J7.Open	U4.1
VBUS0, VBUSA	Connects VBUSA to J22.3	R220	R221	J22.3
	Connects VBUS0 to J22.3	R221	R220	J22.3

Table 6-41: USB Option Links (2)

Table 6-42 below details the function of the option links associated with the USB Configuration.

Reference	Jumper Position	Explanation	Related Ref.
J1	Shorted Pin1-2	Connects USBA VBUS to EXT_CHG.	-
	All open	Disconnects USBA VBUS from EXT_CHG.	-
J2	Shorted Pin1-2	Enables USB0 Host mode.	-
	Shorted Pin2-3	Enables USB0 Function mode.	R42, R52
	All open	Do not setting.	-
J7	Shorted Pin1-2	Enables USBA Host mode.	-
	Shorted Pin2-3	Enables USBA Function mode.	J8
	All open	Enables USBA OTG mode.	R37
J8	Shorted Pin1-2	Enables Bus-powered.	J7
	Shorted Pin2-3	Enables Self-powered.	J7
	All open	Do not setting.	-
J22	Shorted Pin1-2	Enables external battery input.	-
	Shorted Pin2-3	Enables VBUS input.	R221, R220
	All open	Disables external battery input and VBUS input.	-

Table 6-42: USB Option Settings

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Application Header JA1					
Pin	Function	MCU Pin	Pin	Function	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	5V	-	2	0V	-
	CON_5V			GROUND	
3	3V3	-	4	0V	-
	CON_3V3			GROUND	
5	AVCC	175	6	AVSS	1
	CON_AVCC0			CON_AVSS0	
7	AVREF	174	8	ADTRG	176
	CON_VREFH0			ADTRG0n	
9	ADC0	173	10	ADC1	171
	AN000			AN001	
11	ADC2	170	12	ADC3	169
	AN002			AN003	
13	DAC0	4	14	DAC1	2
	DA0			DA1	
15	IO_0	135	16	IO_1	134
	IO0			IO1	
17	IO_2	133	18	IO_3	132
	IO2			IO3	
19	IO_4	131	20	IO_5	130
	IO4			IO5	
21	IO_6	126	22	IO_7	125
	IO6			IO7	
23	IRQ3 / IRQAEC / M2_H SIN0	50 / NC / 27	24	IIC_EX	NC
	IRQ5 / MTIOC0A_IRQ4			NC	
25	IIC_SDA	46 / 72	26	IIC_SCL	48 / 70
	SDA2-DS / SSSDA2			SCL2-DS / SSCL2	

Table 7-1: Application Header JA1 Connections

Table 7-2 below lists the connections of the application header, JA2.

Application Header JA2					
Pin	Function	MCU Pin	Pin	Function	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	RESET	21	2	EXTAL	24
	RESn			CON_EXTAL	
3	NMI	26	4	Vss1	-
	NMI			GROUND	
5	WDT_OVF	NC	6	SClaTX	163
	NC			A-TXD7	
7	IRQ0 / WKUP / M1_H SIN0	27 / NC / 27	8	SClaRX	160
	MTIOC0A_IRQ4			A-RXD7	
9	IRQ1 / M1_H SIN1	52 / 52	10	SClaCK	161
	MTIOC0B_IRQ3			A-SCK7	
11	M1_UD	13	12	CTSRTS	159
	MTIOC3C			A-CTS7RTS7	
13	M1_UP	81	14	M1_UN	80
	MTIOC3B			MTIOC3D	
15	M1_VP	79	16	M1_VN	74
	MTIOC4A			MTIOC4C	
17	M1_WP	86	18	M1_WN	83
	MTIOC4B			MTIOC4D	
19	TimerOut	36	20	TimerOut	47
	MTIOC2B			TIOCA2	
21	TimerIn	28	22	TimerIn	49
	MTIOC0D			TIOCA0	
23	IRQ2 / M1_EncZ / M1_H SIN2	29 / 45 / 29	24	M1_POE	82
	MTIOC0C_IRQ2-DS / MTIOC1A			POE0n	
25	M1_TRCCLK	40	26	M1_TRDCLK	38
	MTCLKA			MTCLKB	

Table 7-2: Application Header JA2 Connections

Table 7-3 below lists the connections of the BUS application header, JA3.

Application Header JA3 (Bus)					
Pin	Function	MCU Pin	Pin	Function	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	A0	118	2	A1	114
	A0			A1	
3	A2	112	4	A3	110
	A2			A3	
5	A4	109	6	A5	108
	A4			A5	
7	A6	107	8	A7	106
	A6			A7	
9	A8	104	10	A9	100
	A8			A9	
11	A10	99	12	A11	98
	A10			A11	
13	A12	97	14	A13	96
	A12			A13	
15	A14	95	16	A15	94
	A14			A15	
17	D0	158	18	D1	156
	D0			D1	
19	D2	154	20	D3	150
	D2			D3	
21	D4	148	22	D5	147
	D4			D5	
23	D6	145	24	D7	143
	D6			D7	
25	RDn	70	26	WR / SDWE	72 / 136
	RDn			WRn / WEn	
27	CSa	88	28	CSb	139
	CS4n			CON_SDCSn	
29	D8	135	30	D9	134
	D8			D9	
31	D10	133	32	D11	132
	D10			D11	
33	D12	131	34	D13	130
	D12			D13	
35	D14	126	36	D15	125
	D14			D15	
37	A16	91	38	A17	89
	A16_ET0ERXD3			A17_ET0ERXD2_MTI0C3A	
39	A18	86	40	A19	83
	A18_ET0RXDV_MTI0C4B			A19_ET0TXER_QIOA0-A_MTI0C4D	
41	A20	82	42	A21	78
	A20_ET0TXCLK_QIOA1-A_POE0n			A21_ET0ETXD2	
43	A22	77	44	SDCLK	128 / 69
	A22_ET0ETXD3			SDCLK / BCLK	
45	CSc / Wait	141 / 71	46	ALE / SDCKE	68 / 124
	CS0n / WAITn			ALE / CKE	
47	HWRn / DQM1	71 / 120	48	LWRn / DQM0	72 / 122
	WR1n / DQM1			WR0n / DQM0	
49	CAS	137	50	RAS	138
	CASn			RASn	

Table 7-3: Application Header JA3 Connections

Table 7-4 below lists the connections of the application header, JA5.

Application Header JA5					
Pin	Function	MCU Pin	Pin	Function	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	ADC4	168	2	ADC5	167
	AN004			AN005	
3	ADC6	166	4	ADC7	165
	AN006			AN007	
5	CAN1TX	29	6	CAN1RX	28
	CTX0			CRX0	
7	CAN2TX	NC	8	CAN2RX	NC
	NC			NC	
9	IRQ4 / M2_EncZ / M2HSIN1	52 / 37 / 52	10	IRQ5 / M2_HSIN2	29 / 29
	MTIOC0B_IRQ3 / MTIOC2A			MTIOC0C_IRQ2-DS	
11	M2_UD	126	12	M2_Uin	53
	MTIOC6C			MTIC5U	
13	M2_Vin	67	14	M2_Win	68
	MTIC5V			MTIC5W	
15	M2_Toggle	125	16	M2_POE	96
	MTIOC6A			POE4n	
17	M2_TRCCLK	43	18	M2_TRDCLK	42
	MTCLKC			MTCLKD	
19	M2_UP	108	20	M2_Un	118
	MTIOC6B			MTIOC6D	
21	M2_VP	112	22	M2_Vn	120
	MTIOC7A			MTIOC7C	
23	M2_WP	114	24	M2_Wn	122
	MTIOC7B			MTIOC7D	

Table 7-4: Application Header JA5 Connections

Table 7-5 below lists the connections of the application header, JA6.

Application Header JA6					
Pin	Function	MCU Pin	Pin	Function	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	DREQ	79	2	DACK	74
	EDREQ1			EDACK1	
3	TEND	NC	4	STBYn	NC
	NC			NC	
5	RS232TX	NC	6	RS232RX	NC
	RS232TX			RS232RX	
7	SCIbRX	31	8	SCIbTX	35
	RXD1			TXD1	
9	SClTX	72	10	SClCK	34
	TXD2			SCK1	
11	SClCK	71	12	SClRX	70
	SCK2			RXD2	
13	M1_Toggle	89	14	M1_Uin	53
	MTIOC3A			MTIC5U	
15	M1_Vin	67	16	M1_Win	68
	MTIC5V			MTIC5W	
17	EXT_USB_VBUS	-	18	Reserved	NC
	EXT_VBUS			NC	
19	EXT_USB_BATT	-	20	Reserved	NC
	EXT_BATT			NC	
21	EXT_USB_CHG	-	22	Reserved	NC
	EXT_CHG			NC	
23	Unregulated_VCC	-	24	Vss	-
	Unregulated_VCC			GROUND	

Table 7-5: Application Header JA6 Connections

7.2 Generic Headers

Generic headers, used to provide easy connections to various pins from devices fitted to the RSK+.

Table 7-6 below lists the connections of the LCD Direct Drive (TFT) Header.

LCD Direct Drive Header (TFT)					
Pin	Header Name	MCU Pin	Pin	Header Name	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	5V	-	2	5V	-
	Board_5V			Board_5V	
3	3V3	-	4	3V3	-
	Board_3V3			Board_3V3	
5	Reserved	NC	6	Reserved	NC
	NC			NC	
7	B1	158	8	B2	156
	D0			D1	
9	B3	154	10	B4	150
	D2			D3	
11	B5	148	12	G0	147
	D4			D5	
13	G1	145	14	G2	143
	D6			D7	
15	G3	135	16	G4	134
	D8			D9	
17	G5	133	18	R1	132
	D10			D11	
19	R2	131	20	R3	130
	D12			D13	
21	R4	126	22	R5	125
	D14			D15	
23	EDACK	74	24	HSYNC	13
	EDACK1			MTIOC3C	
25	DOTCLK	27	26	LCDDEN	89
	MTIOC0A_IRQ4			MTIOC3A	
27	VSYNC	37	28	EDREQ	79
	MTIOC2A			EDREQ1	
29	SSCK	84	30	SSI	82
	TFT_QSPCLK-A			TFT_QIOA1-A	
31	SSO	83	32	SCS	85
	TFT_QIOA0-A			TFT_QSSLA-A	
33	RESET	21	34	GND	-
	RESn			GROUND	
35	BACKLIGHT	36	36	SD_DOTCLK	NC
	BACKLIGHT			NC	
37	GND	-	38	GND	-
	GROUND			GROUND	
39	GND	-	40	GND	-
	GROUND			GROUND	
41	X_DRIVE	11	42	Y_DRIVE	171
	XDRIVE			YDRIVE	
43	X_INPUT1	168	44	Y_INPUT1	167
	XINPUT1			YINPUT1	
45	X_INPUT2	166	46	Y_INPUT2	165
	XINPUT2			YINPUT2	
47	Reserved	NC	48	Reserved	NC
	NC			NC	
49	Reserved	NC	50	Reserved	NC
	NC			NC	

Table 7-6: TFT Connector Connections

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via an E1/E20 debugger. An E1 debugger is supplied with this RSK+ product.

For further information regarding the debugging capabilities of the E1/E20 debuggers, refer to E1/E20 Emulator Additional Document for User's Manual (R20UT0399EJ).

8.2 Compiler Restrictions

The version of the compiler provided with this RSK+ is fully functional for 60 days and then code size limited to 128kbytes of Code and Data. This restriction can be removed by purchasing a licenced copy of the tools.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip and Boot modes (SCI and USB), which are configured on the RSK+ board. Details of the modifications required can be found in §6.2. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX64M group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK+ is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 emulator (as supplied with this RSK+) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer RX Family E1/E20 Emulator User's Manual (R20UT0398EJ).

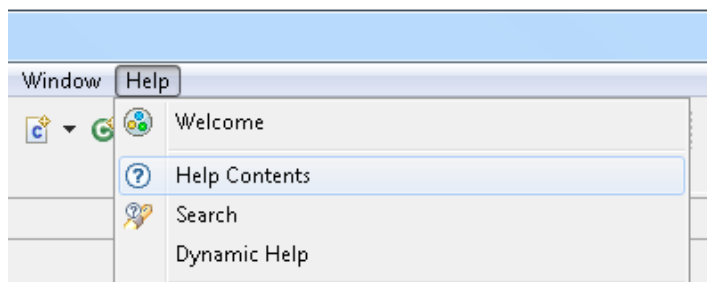
8.5 Address Space

Figure 8-1 below details the address space of the MCU. This diagram is taken from the User's Manual: Hardware. For further details, refer to the RX64M Group User's Manual: Hardware.

9. Additional Information

Technical Support

For details on how to use e² studio, refer to the help file by opening e² studio, then selecting Help > Help Contents from the menu bar.



For information about the RX/RX600 series microcontrollers refer to the RX/RX600 Group Hardware Manual.

For information about the RX assembly language, refer to the RX Series Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 9 of the “Quick Start Guide”

General information on Renesas microcontrollers can be found on the Renesas website at:

<http://www.renesas.com/>

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Rev.	Date	Description	
		Page	Summary
1.00	Jun 20, 2014	—	First Edition issued
1.10	Jun 25, 2015	—	Table of Contents was updated.
		—	Section 1. Purpose and Target Readers was corrected. - RSKRX64M Code Generator Tutorial Manual was corrected to RSK+RX64M Code Generator Tutorial Manual.
		13, 14	Sentences about Figure 3-4 were corrected. Figure 3-3 and 3-4 was updated. (part number can be searched)
		27	Section 5.15 I ² C Bus (Inter-IC Bus) was fixed. - Channel of RIIC connecting to EEPROM was corrected.
		32	Enable & Disable setting of Table 6-6 (P13, MTIOC0B_IRQ3) was fixed.
		33	AVSS0 explanation of Table 6-7 was fixed.
		68	Figure 8-1 was removed.

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