

RX63N Group

Renesas Starter Kit+ User's Manual
For CubeSuite+

RENESAS MCU
RX Family / RX600 Series

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- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK+ hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK+ platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK+ and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSK+RX63N-256K. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	RSK+RX63N-256K User Manual	R20UT3072EG
Tutorial Manual	Provides a guide to setting up RSK environment, running sample code and debugging programs.	RSK+RX63N-256K Tutorial Manual	R20UT3073EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample, on a single A4 sheet.	RSK+RX63N-256K Quick Start Guide	R20UT3074EG
USB Function Manual	Provides sample instructions to configure the RSK and Host PC for running the USB function sample code.	RSK+RX63N USB Function Manual	R20UT0442EG
Schematics	Full detail circuit schematics of the RSK.	RSK+RX63N-256K Schematics	R20UT0437EG
User's Manual: Hardware	Provides technical details of the RX63N microcontroller.	RX63N Group, RX631 Group User's Manual: Hardware	R01UH0041EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
BC	Battery Charging
bps	Bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DIP	Dual In-line Package
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
E1	Renesas On-chip Debugging Emulator
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GPT	General PWM Timer
I ² C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Micro-controller Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not applicable
n/c (NC)	Not connected
NMI	Non-maskable Interrupt
OTG	On The Go™
PC	Personal Computer
PDC	Parallel Data Capture Unit
PLL	Phase Locked Loop
POE	Port Output Enable
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
RTC	Realtime Clock
SAU	Serial Array Unit
SCI	Serial Communications Interface
SFR	Special Function Registers
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
TAU	Timer Array Unit
TFT	Thin Film Transistor
TPU	Timer Pulse Unit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog timer

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1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK+ hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK+ board contains all the circuitry required for microcontroller operation.

1.3 Scope

This manual covers the RSK+RX63N-256K which is fitted a R5F563NFDDFC microcontroller.

For the legacy RSK+RX63N please refer to <http://www.renesas.com/rskrx63n>.

2. Power Supply

2.1 Requirements

This RSK+ is supplied with an E1 debugger. The debugger is able to supply the RSK+ board with up to 200mA.

In applications requiring more than 200mA or when the E1 debugger is not used, the RSK+ must be powered externally. All RSK and RSK+ boards have a centre positive supply connector using a 2.0mm barrel power jack.

This RSK+ supports a wide range of voltage inputs, and requires specific configuration for different inputs. Details of the external power supply connections are shown in **Table 2-1** below.

Connector	Supply Voltages	J8 Setting	J9 Setting
PWR1	Regulated, 5V DC	Shorted	Shorted
	Unregulated, 7 to 15V DC	Open	Open

Table 2-1: Main Power Supply Requirements

The main power supply connected to PWR1 should supply a minimum of 5W to ensure full functionality.

This RSK+ features an independent USB power supply, which allows a user to power the USB host/OTG modules from a second external power supply. Connections for the external USB power supply are detailed in **Table 2-2** below.

Connector	Supply Voltages
PWR2 (USB_3V3)	Regulated, 3.3V DC
PWR3 (USB_5V)	Regulated, 5V DC

Table 2-2: USB Power Supply Requirements

The USB power supplies connected to PWR2 and PWR3 should both supply a minimum of 600mA to ensure full USB host functionality. Note: The OTG module is limited to supply a maximum of 200mA when operating as host.

The RSK+ can also be powered directly from the USB VBUS, when a suitable host device is connected to the USB0 connector and the RSK+ is correctly configured (refer to §6). This will limit the current consumption of the RSK+ to 500mA (USB maximum), therefore full functionality cannot be achieved whilst being powered from the USB VBUS.

This RSK+ also features a coin cell backup battery function which is used to power the real-time clock and sub-clock oscillator when the voltage drop at the VCC pin is detected. Connections for the backup battery power supply are detailed in **Table 2-3** below.

Connector	Supply Voltage
PWR4	2.3V to 3.6V DC

Table 2-3: Backup Battery Power Supply Requirements

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the 'Release' or stand-alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. After 200 flashes or after pressing any switch, the LEDs will flash at a rate controlled by the potentiometer.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

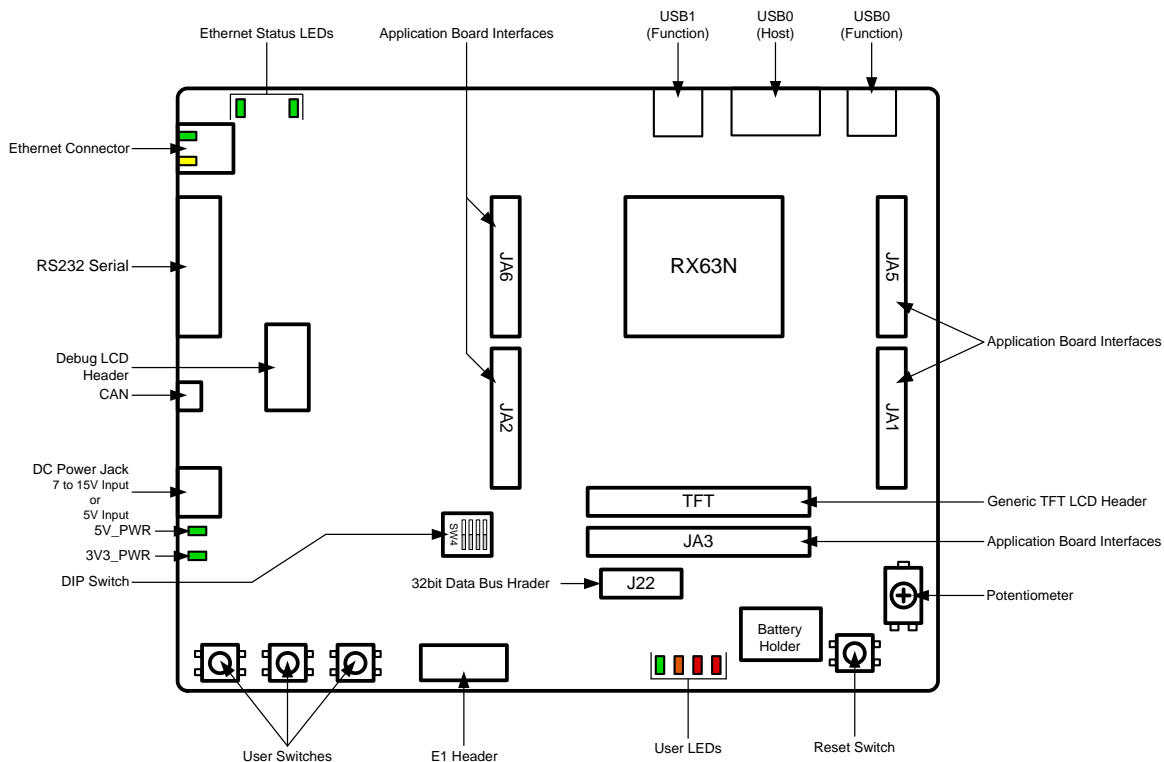


Figure 3-1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.

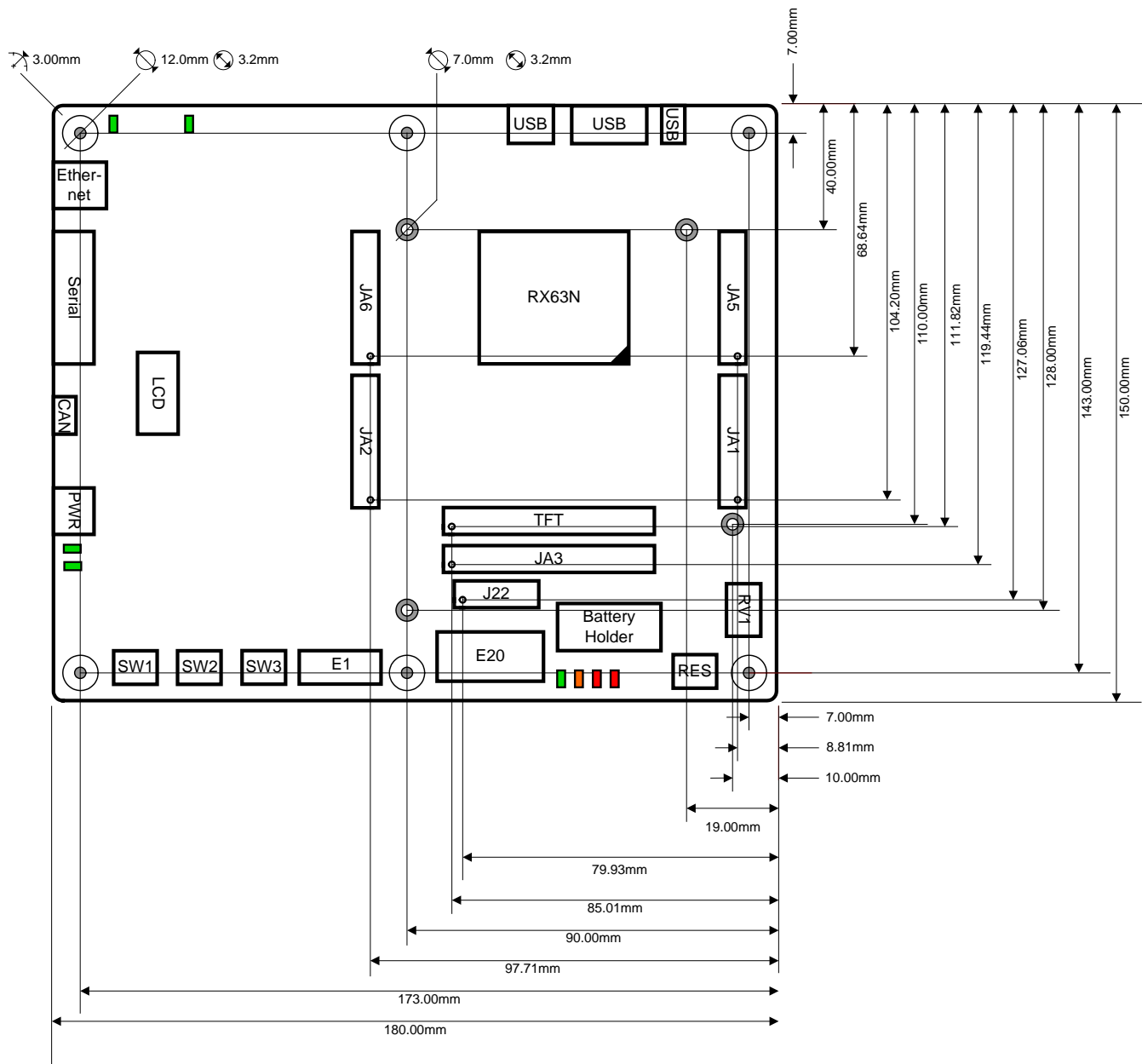


Figure 3-2: Board Dimensions

Figure 3-4 below shows the component placement on the bottom-side of the RSK+ board.

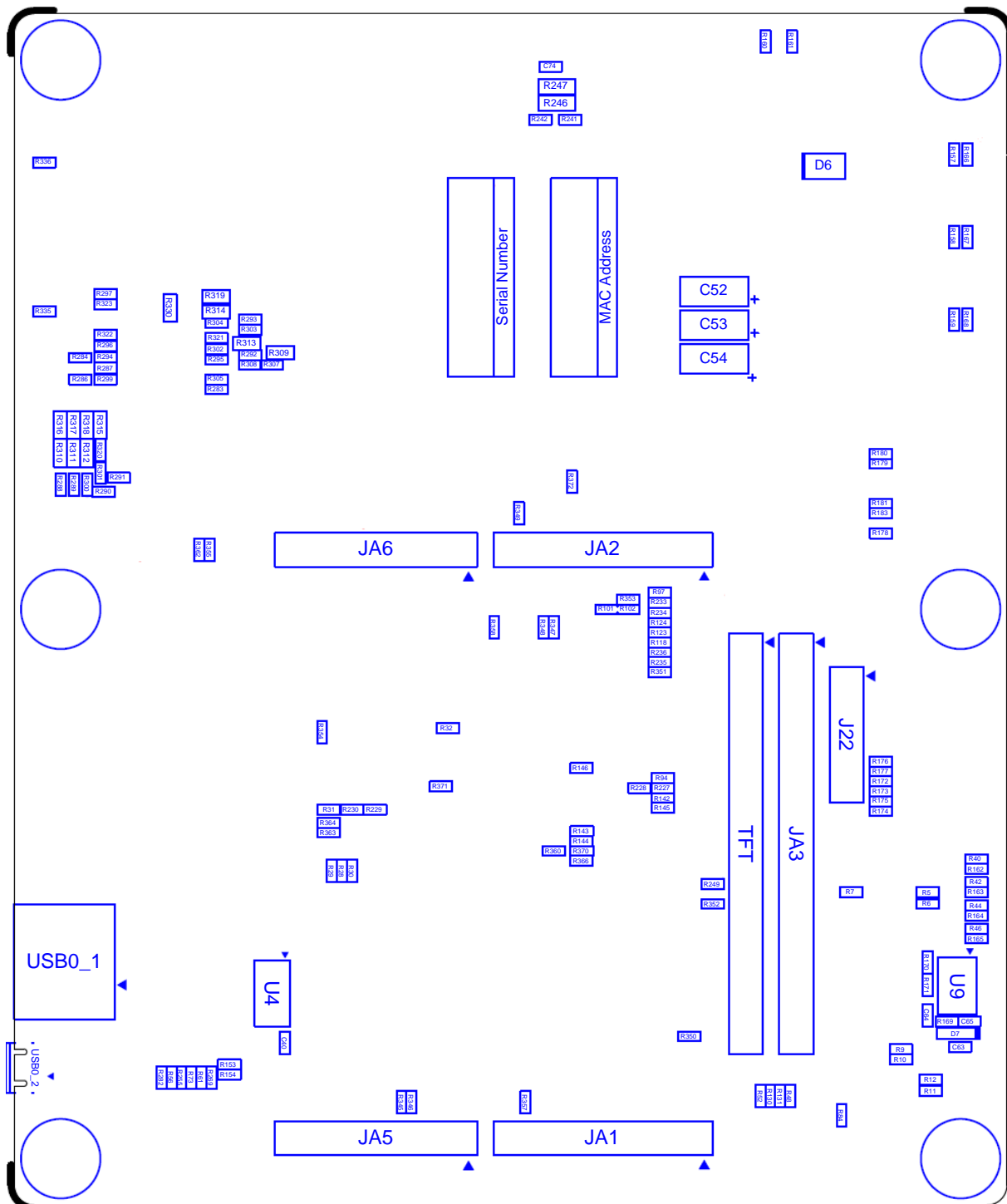


Figure 3-4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal RSK+ Connections

The diagram below shows the RSK+ board components and their connectivity to the MCU.

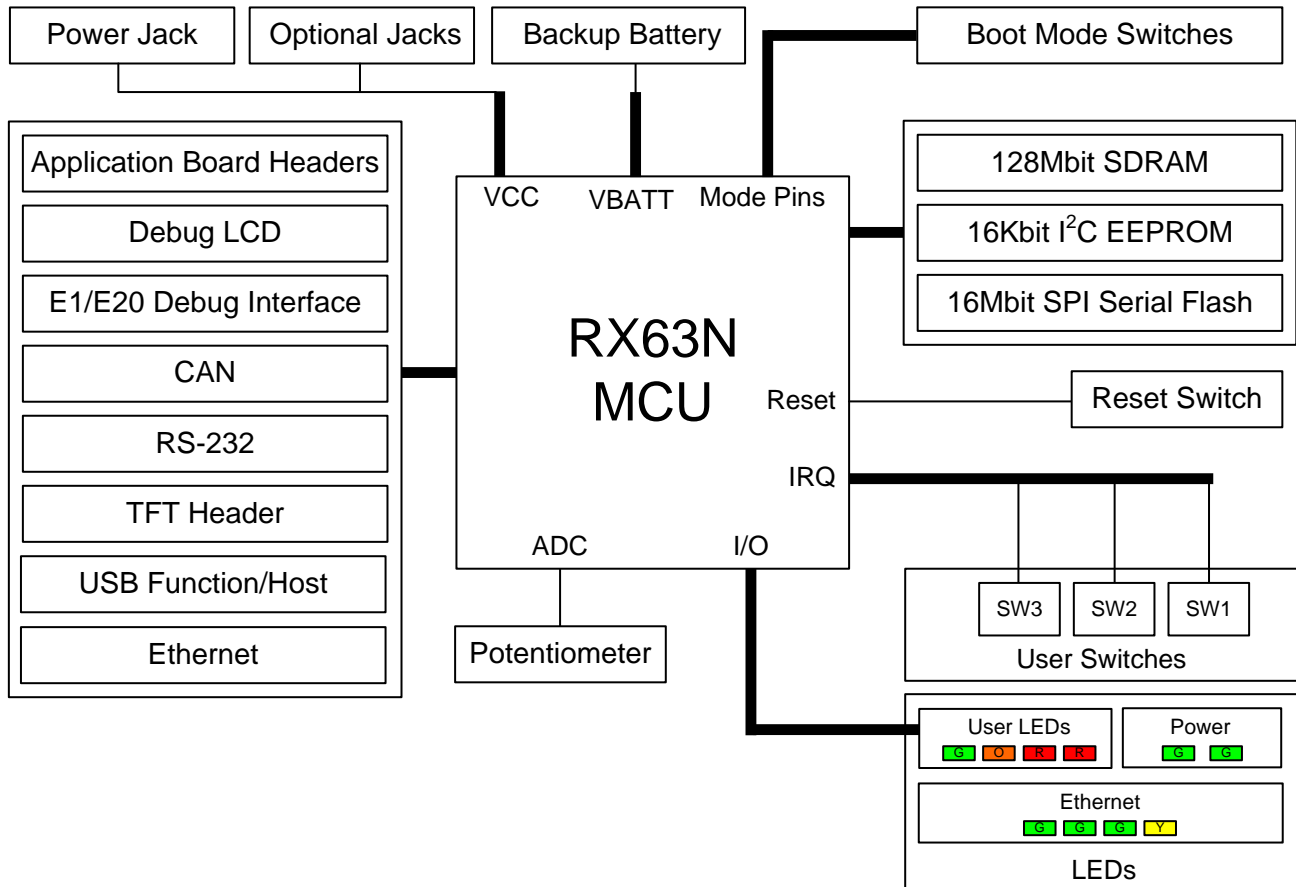


Figure 4-1: Internal RSK+ Block Diagram

4.2 Debugger Connections

The diagram below shows the connections between the RSK+, E1 debugger and the host PC.

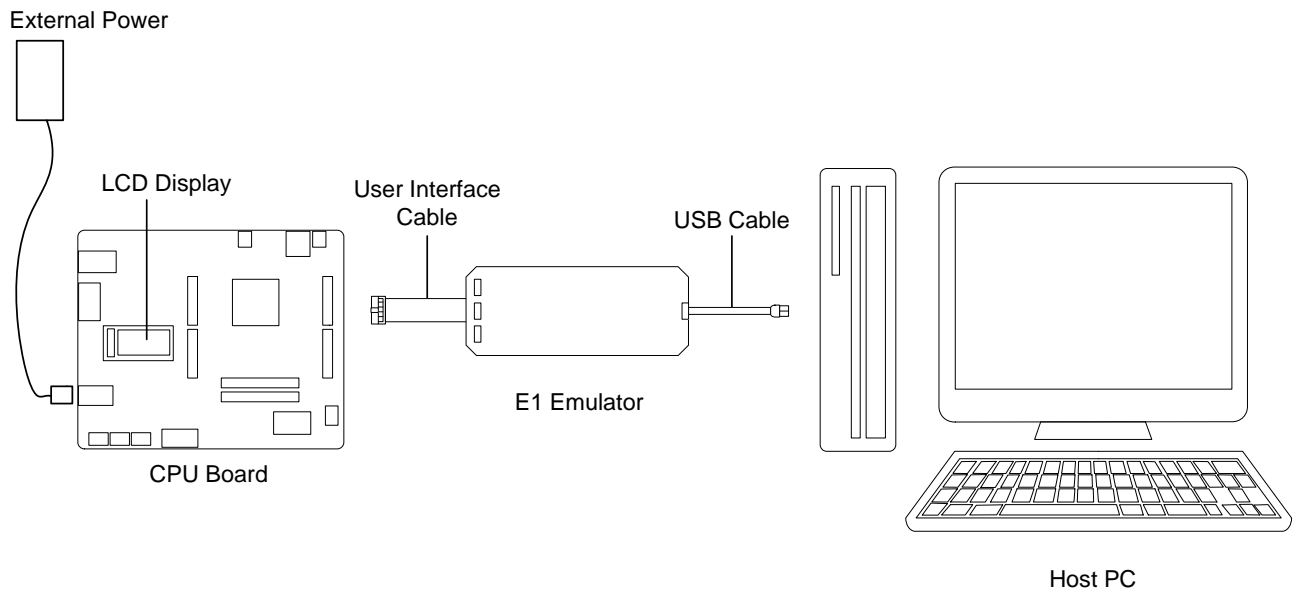


Figure 4-2: Debugger Connection Diagram

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the RSK+ to generate the required reset signal, and is triggered from the RES switch. Refer to the RX63N Group, RX631 Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the RSK+RX63N board schematics for information regarding the reset circuitry in use on the RSK+.

5.2 Clock Circuit

A clock circuit is fitted to the RSK+ to generate the required clock signal to drive the MCU, and associated peripherals. Refer to the RX63N Group, RX631 Group User's Manual: Hardware for details regarding the clock signal requirements, and the RSK+RX63N board schematics for information regarding the clock circuitry in use on the RSK+. Details of the oscillators fitted to the RSK+ are listed in **Table 5-1** below.

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MCU oscillator.	Fitted	12MHz	HC49/4U
X2	Internal RSK+ Testing Only	Unfitted	n/a	n/a
X3	Real time Clock	Fitted	32.768kHz	Encapsulated, SMT
X4	Ethernet Clock (MII)	Fitted	25MHz	HC49/4U
X5	Ethernet Clock (RMII)	Unfitted	50MHz	Encapsulated, SMT

Table 5-1: Oscillators

5.3 Switches

There are four switches located on the RSK+ board. The function of each switch and its connection is shown in **Table 5-2**. For further information regarding switch connectivity, refer to the RSK+RX63N board schematics.

Switch	Function	MCU Connection
RES	When pressed, the microcontroller is reset.	RES#, Pin 21
SW1	Connects to an IRQ input for user controls.	IRQ10, Pin 6
SW2	Connects to an IRQ input for user controls.	IRQ8, Pin 8
SW3/ADTRG	Connects to an IRQ input for user controls. The switch is also connected to an ATRG input, and is used to trigger AD conversions.	IRQ15/ADTRG0#, Pin 176

Table 5-2: Switch Connections

5.4 LEDs

There are ten LEDs on the RSK+ board. The function of each LED, its colour and connections are shown in **Table 5-3**.

LED	Colour	Function	MCU Connection
3V3_PWR	Green	Indicates the status of the 3.3V power rail.	No connection
5V_PWR	Green	Indicates the status of the 5V power rail.	No connection
LED0	Green	User operated LED.	P03, Pin 4
LED1	Orange	User operated LED.	P05, Pin 2
LED2	Red	User operated LED.	P10, Pin 56
LED3	Red	User operated LED.	P11, Pin 55
SPEED	Green	Ethernet speed status LED.	No connection
DUPLEX	Green	Ethernet duplex status LED.	No connection
Built into Ethernet con.	Green	Ethernet link status LED.	P54, Pin 67*
Built into Ethernet con.	Yellow	Ethernet activity status LED.	No connection

Table 5-3: LED Connections

* This connection is not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN000, pin 173. The potentiometer can be used to create a voltage between AVCC0 and ground (by default, AVCC0 is connected to the MCU power supply UC_VCC).

The potentiometer offers an easy method of supplying a variable analog input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the device hardware manual for further details.

5.6 Debug LCD Module

A debug LCD module is supplied with the RSK+, and should be connected to the LCD header, LCD1.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The debug LCD module uses a 4-bit interface to reduce pin allocation. No contrast control is provided, as this is set by a resistor supplied on the display module. Connection information for the debug LCD is provided in **Table 5-4**.

Debug LCD Header					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	Ground	-	2	Board_5V	-
3	No Connection	-	4	DLCDRS	PJ5, Pin 11
5	R/W (Pulled to ground)	-	6	DLCDE	PF5, Pin 9
7	No Connection	-	8	No Connection	-
9	No Connection	-	10	No Connection	-
11	DLCDD4_XDRIVE	P84, Pin 69	12	DLCDD5_YDRIVE	P85, Pin 52
13	DLCDD6_BACKLIGHT	P86, Pin 49	14	DLCDD7	P87, Pin 47

Table 5-4: LCD Header Connections

5.7 RS232 Serial Port

Serial port SCI0 is connected to the standard RS232 header fitted to the RSK+. Alternatively, serial port SCI1 or SCI6 can be connected to the RS232 transceiver by making changes to the configurations to the jumpers and option links (refer to §6). Connections between the RS232 header and the microcontroller are listed in the **Table 5-5**.

SCI Signal	Function	MCU Connection	RS232 Connection
TxD0	SCI0 Transmit Signal.	P20, Pin P45	Pin 13
RxD0	SCI0 Receive Signal.	P21, Pin P44	Pin 15
TxD1	SCI1 Transmit Signal.	PF0, Pin 35	Pin 13*
RxD1	SCI1 Receive Signal.	PF2, Pin 31	Pin 15*
TxD6	SCI6 Transmit Signal.	P00, Pin 8	Pin 12*
RxD6	SCI6 Receive Signal.	P01, Pin 7	Pin 10*

Table 5-5: Serial Port Connections

* This connection is not available in the default RSK+ configuration - refer to §6 for the required modifications.

5.8 Controller-Area Network (CAN)

A CAN transceiver IC is fitted to the RSK+, and is connected to the CAN MCU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RX63N Group, RX631 Group User's Manual: Hardware.

The connections for the CAN microcontroller signals are listed in **Table 5-6** below.

CAN Signal	Function	MCU Connection
CTX1	CAN Data Transmission.	P54, Pin 67
CRX1	CAN Data Reception.	P55, Pin 66
CANEN	CAN Transceiver Device Enable Control.	PG1, Pin 144
CANERRn	CAN Error and Power Status.	P25, Pin 38
CANSTBn	CAN Standby Mode Control.	PG0, Pin 146

Table 5-6: CAN Connections

5.9 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the RSK+RX63N PCB as a sticker, and should always be used with this device to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

An Ethernet controller IC is fitted to the RSK+, and is connected to the Ethernet MCU peripheral. The RX63N MCU supports full duplex 10Mb/s and 100Mb/s transmission and reception. The Ethernet status LEDs (LED6 – 9) are detailed in §5.4. The connections for the Ethernet controller are listed in **Table 5-7** below.

Ethernet Signal	Function	MCU Connection
ETMDIO	Management data serial I/O	P71, Pin 102
ETMDC	Management serial clock	P72, Pin 101
ETTXCLK	Transmit clock	PC4, Pin 82
ETTXEN	Transmit enable.	P80, Pin 81
ETTXER	Transmit error.	PC3, Pin 83
ETETXD0	Transmit data bit 0.	P81, Pin 80
ETETXD1	Transmit data bit 1.	P82, Pin 79
ETETXD2	Transmit data bit 2.	PC5, Pin 78
ETETXD3	Transmit data bit 3.	PC6, Pin 77
ETRXCLK	Receive clock	P76, Pin 85
ETRXDV	Receive data valid.	PC2, Pin 86
ETRXER	Receive data error.	P77, Pin 84
ETERXD0	Receive data bit 0.	P75, Pin 87
ETERXD1	Receive data bit 1.	P74, Pin 88
ETERXD2	Receive data bit 2.	PC1, Pin 89
ETERXD3	Receive data bit 3.	PC0, Pin 91
ETCOL	Collision detect.	PC7, Pin 76
ETLINKSTA	Link status	P54, Pin 67
ETCRS	Carrier sense.	P83, Pin 74

Table 5-7: Ethernet Connections

5.10 Universal Serial Bus (USB)

This RSK+ device is fitted with a USB host socket (type A) and a function socket (type Mini B). USB module USB0 is connected to the host and function socket, and can operate as either a host or function device. Module USB1 is connected to a dedicated function port. The connections for the USB0 module are shown in **Table 5-8** below.

USB Signal	Function	MCU Connection
USB0DP	Positive differential data signal.	USB0_DP, Pin 59
USB0DM	Negative differential data signal.	USB0_DM, Pin 58
USB0VBUS	Cable monitor pin.	P16, Pin 48
USB0EXICEN	OTG low-power control signal.	P21, Pin 44*
USB0VBUSEN-H	VBUS power supply enable (Host).	P16, Pin 48
USB0VBUSEN-O	VBUS power supply enable (OTG).	P24, Pin 40*
USB0OVRCURA	Over-current detection signal A.	P14, Pin 51
USB0OVRCURB	Over-current detection signal B.	P16, Pin 48*
USB0ID	USB ID pin.	P20, Pin 45*
USB0DPUPE-O	Positive differential data pull-up control signal (OTG).	P23, Pin 42*
USB0DPUPE-F	Positive differential data pull-up control signal (Function).	P14, Pin 51
USB0DPRPD	Differential data pull-down control signal.	P25, Pin 38
USB0DRPD	Differential data pull-down control signal.	P22, Pin 43

Table 5-8: USB0 Module Connections

Note:

- When evaluating OTG, ensure to replace the default USB connector (USB0_D) with a USB Micro-AB connector.
- Connectors such as the one manufactured by Hirose Electric with part number ZX62R-AB-5P, can be used.

The connections for the USB1 module are shown in **Table 5-9** below.

USB Signal	Function	MCU Connection
USB1DP	Positive differential data signal.	USB1_DP, Pin 64
USB1DM	Negative differential data signal.	USB1_DM, Pin 63
USB1VBUS	VBUS power supply	P17, Pin 46
USB1DPUPE	Positive differential data pull-up control signal.	P15, Pin 50

Table 5-9: USB1 Module Connections

5.11 Generic LCD Header

This RSK+ device is fitted with a generic TFT LCD header, that allows connection to compatible Renesas LCD application boards.

The pin connections of this header are listed in **Table 5-10** below.

Generic LCD Header (TFT)					
Pin	Circuit Net Name	MCU Pin	Pin	Circuit Net Name	MCU Pin
1	5V	-	2	5V	-
3	3V3	-	4	3V3	-
5	Reserved	NC	6	Reserved	NC
7	B1	PD0, Pin 158	8	B2	PD1, Pin 156
9	B3	PD2, Pin 154	10	B4	PD3, Pin 150
11	B5	PD4, Pin 148	12	G0	PD5, Pin 147
13	G1	PD6, Pin 145	14	G2	PD7, Pin 143
15	G3	PE0, Pin 135	16	G4	PE1, Pin 134
17	G5	PE2, Pin 133	18	R1	PE3, Pin 132
19	R2	PE4, Pin 131	20	R3	PE5, Pin 130
21	R4	PE6, Pin 126	22	R5	PE7, Pin 125
23	EDACK	P56, Pin 62	24	HSYNC	P32, Pin 29
25	DOTCLK	PJ3, Pin 13	26	LCDDEN	P34, Pin 27
27	VSYNC	P24, Pin 40	28	EDREQ	P57, Pin 61
29	SSCK	P27, Pin 36	30	SSI	P30, Pin 33
31	SSO	P26, Pin 37	32	SCS	P50, Pin 72
33	RESET	RES#, Pin 21	34	GND	-
35	BACKLIGHT	P86, Pin 49	36	SD_DOTCLK	-
37	GND	-	38	GND	-
39	GND	-	40	GND	-
41	X_DRIVE	P84, Pin 69	42	Y_DRIVE	P85, Pin 52
43	X_INPUT1	P44, Pin 168	44	Y_INPUT1	P45, Pin 167
45	X_INPUT2	P46, Pin 166	46	Y_INPUT2	P47, Pin 165
47	Reserved	NC	48	Reserved	NC
49	Reserved	NC	50	Reserved	NC

Table 5-10: Generic LCD Header Connections

5.12 External Bus

The RX63N features an external data bus, which is connected to various devices on the RSK+ board. Details of the devices connected to the external data bus are listed in **Table 5-11** below. Further details of the devices connected to the external bus can be found in the board schematics.

Chip Select	Device Name	Device Description	Address Space
CS0	JA3	Application Header	FF000000h to FFFFFFFFh (16Mbytes)
SDCS	U3	128MBit SDRAM	08000000h to 0FFFFFFFh (128Mbytes)
	JA3	Application Header	08000000h to 0FFFFFFFh (128Mbytes)
CS1 to CS2	-	Unused	06000000h to 07FFFFFFh (2 x 16Mbytes)
CS3	JA3	Application Header	05000000h to 05FFFFFFh (16Mbytes)
CS4 to CS7	-	Unused	01000000h to 04FFFFFFh (4 x 16Mbytes)

Table 5-11: External Bus Address Space

5.13 Renesas Serial Peripheral Interface (RSPI)

The RX63N features three Renesas Serial Peripheral Interface modules (Renesas SPI or RSPI). **Table 5-12** below details the connected devices, and their connections to the MCU.

RSPI Channel	Slave Select	Device Name	Device Description
RSPI1	SSLB0	U4	Serial Flash, 16Mbits
RSPI1	SSLB1	TFT	Generic LCD Header

Table 5-12: SPI Connections

5.14 I²C Bus (Inter-IC Bus)

The RX63N features four I²C (Inter-IC Bus) interface modules. I²C module 0 is connected to a 16Kbit EEPROM (Electrically-Erasable Programmable Read Only Memory). Specific details of the EEPROM device and the connections can be found in the board schematics.

This device is configured to respond to the address 0x3. The first bit of the device address can be configured by modifying option links – refer to §6 for further details.

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way RSK+ operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the RSK+ is supplied with. Refer to the component placement diagram (§3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the RSK+ is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the RSK+.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RX63N Group, RX631 Group User's Manual: Hardware and RSK+RX63N board schematics for further information.

6.2 MCU Configuration

Table 6-1 below details the option links associated with configuring the MCU operating modes.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R169	Connects RESn (U1B, pin 21) to the reset switch RES.	Disconnects RESn (U1B, pin 21) from the reset switch RES.	U9

Table 6-1: MCU Option Links

Table 6-2 below details the function of the switches associated with configuring the emulator support.

Reference	Pin 1	Pin 2	Operating Mode	Related Ref.
SW4	OFF	OFF	Single chip mode	-
	ON	OFF	Boot mode (SCI)	-
	OFF	ON	Single chip mode	-
	ON	ON	User Boot Mode USB Boot Mode	-
Reference	Pin 3	Pin 4	Operating Mode	Related Ref.
SW4	OFF	x	USB boot mode bus-powered*	-
	ON	x	USB boot mode self-powered*	-

Table 6-2: MCU Setting DIP Switches

x – Mode selection is irrespective of this pin changing (i.e. “Don’t care”).

* To configure the device to power from the USB VBUS, see the USB configuration section (§6.7).

Table 6-3 below details the different configurations and functions of the MCU operating mode jumpers.

Reference	Position One	Position Two	Position Three	Related Ref.
J6	Pins 1 and 2 shorted. Connects EMLE (U1B, pin 10) to Board_VCC.	Pins 2 and 3 shorted. Connects EMLE (U1B, pin 10) to GROUND.	All pins open. EMLE is left to float – DO NOT SET.	-

Table 6-3: MCU Operating Mode Jumpers

6.3 ADC Configuration

Table 6-4 & Table 6-5 below details the function of the option links associated with the Analog-to-Digital circuit.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R5	Connects VREFH0 (U1A, pin 174) to UC_VCC.	Disconnects VREFH0 (U1A, pin 174) from UC_VCC.	R6*
R6*	Connects VREFH0 (U1A, pin 174) to CON_VREFH0 (JA1, pin 7).	Disconnects VREFH0 (U1A, pin 174) from CON_VREFH0 (JA1, pin 7).	R5
R7	Connects VREFL0 (U1A, pin 172) to GROUND.	Disconnects VREFL0 (U1A, pin 172) from GROUND.	-
R9	Connects AVCC0 (U1A, pin 175) to UC_VCC.	Disconnects AVCC0 (U1A, pin 175) from UC_VCC.	R10*
R10*	Connects AVCC0 (U1A, pin 175) to CON_AVCC0 (JA1, pin 5).	Disconnects AVCC0 (U1A, pin 175) from CON_AVCC0 (JA1, pin 5).	R9
R11	Connects AVSS0 (U1A, pin 1) to GROUND.	Disconnects AVSS0 (U1A, pin 1) from GROUND.	R12*
R12*	Connects AVSS0 (U1A, pin 1) to CON_AVSS0 (JA1, pin 6).	Disconnects AVSS0 (U1A, pin 1) from CON_AVSS0 (JA1, pin 6).	R11
R13	Connects ADPOT (RV1) to Board_VCC.	Disconnects ADPOT (RV1) from Board_VCC.	R14*
R14*	Connects ADPOT (RV1) to CON_AVCC0 (JA1, pin 5).	Disconnects ADPOT (RV1) from CON_AVCC0 (JA1, pin 5).	R13
R15	Connects VREFH (U1A, pin 3) to UC_VCC.	Disconnects VREFH (U1A, pin 3) from UC_VCC.	-
R16	Connects VREFL (U1A, pin 5) to GROUND.	Disconnects VREFL (U1A, pin 5) from GROUND.	**
R83*	Connects AN000_ADPOT (U1C, pin 173) to AN000 (JA1, pin 9).	Disconnects AN000_ADPOT (U1C, pin 173) from AN000 (JA1, pin 9).	R84
R84	Connects AN000_ADPOT (U1C, pin 173) to ADPOT (RV1).	Disconnects AN000_ADPOT (U1C, pin 173) from ADPOT (RV1).	R83*
R85*	Connects AN004_XINPUT1 (U1C, pin 168) to AN004 (JA5, pin 1).	Disconnects AN004_XINPUT1 (U1C, pin 168) from AN004 (JA5, pin 1).	-

Table 6-4: ADC Option Links (Continued Overleaf)

* Do not fit the related reference link when the reference link is fitted.

** Do not remove.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R87*	Connects AN005_YINPUT1 (U1C, pin 167) to AN005 (JA5, pin 2).	Disconnects AN005_YINPUT1 (U1C, pin 167) from AN005 (JA5, pin 2).	R88
R89*	Connects AN006_XINPUT2 (U1C, pin 166) to AN006 (JA5, pin 3).	Disconnects AN006_XINPUT2 (U1C, pin 166) from AN006 (JA5, pin 3).	R90
R91*	Connects AN007_YINPUT2 (U1C, pin 165) to AN007 (JA5, pin 4).	Disconnects AN007_YINPUT2 (U1C, pin 165) from AN007 (JA5, pin 4).	R92

Table 6-5: ADC Option Links (Continuation)

* Do not fit the related reference link when the reference link is fitted.

6.4 RS232 Serial Port Configuration

Table 6-6 & Table 6-7 below details the function of the option links associated with serial port configuration.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R35*	Connects IRQ8_TXD6 (U1B, pin 8) to TXD6 (JA6, pin 8).	Disconnects IRQ8_TXD6 (U1B, pin 8) from TXD6 (JA6, pin 8)	R34
R37*	Connects IRQ9_RXD6 (U1B, pin 7) to RXD6 (JA6, pin 7).	Disconnects IRQ9_RXD6 (U1B, pin 7) from RXD6 (JA6, pin 7).	R36
R39	Connects IRQ10_SCK6 (U1B, pin 6) to SCK6 (JA6, pin 10).	Disconnects IRQ10_SCK6 (U1B, pin 6) from SCK6 (JA6, pin 10).	R38
R59	Connects TXD0_TRIGb_USB0ID (U1B, pin 45) to TXD0 (JA2, pin 6)	Disconnects TXD0_TRIGb_USB0ID (U1B, pin 45) from TXD0 (JA2, pin 6)	R60*, R61*
R62	Connects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) to RXD0 (JA2, pin 8)	Disconnects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) from RXD0 (JA2, pin 8)	R63*, R64*, R65*
R66	Connects SCK0_TMR0_USB0DRPD (U1B, pin 43) to SCK0 (JA2, pin 10)	Disconnects SCK0_TMR0_USB0DRPD (U1B, pin 43) from SCK0 (JA2, pin 10)	R67*, R68*
R69	Connects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) to CTS0RTS0 (JA2, pin 12).	Disconnects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) from CTS0RTS0 (JA2, pin 12).	R70*, R71*
R185	Connects TDO_TXD1 (U1B, pin 35) to TXD1 (JA6, pin 9)	Disconnects TDO_TXD1 (U1B, pin 35) from TXD1 (JA6, pin 9)	R184
R189	Connects TDI_RXD1 (U1B, pin 31) to RXD1 (JA2, pin 8)	Disconnects TDI_RXD1 (U1B, pin 31) from RXD1 (JA2, pin 8)	R188
R187*	Connects TCK_SCK1 (U1B, pin 34) to SCK1 (JA2, pin 10)	Disconnects TCK_SCK1 (U1B, pin 34) from SCK1 (JA2, pin 10)	R186
R215	Connects TXD6 (JA6, pin 8) to T2IN (U10, pin 12).	Disconnects TXD6 (JA6, pin 8) from T2IN (U10, pin 12).	R34, R35*
R216	Connects RXD6 (JA6, pin 7) to R2OUT (U10, pin 10).	Disconnects RXD6 (JA6, pin 7) from R2OUT (U10, pin 10).	R36, R37*

Table 6-6: RS232 Serial Port Option Links

* Not fitted by default.

Table 6-7 below details the different configurations and functions of the RS232 serial jumpers.

Reference	Position One (Pin 1 and 2 Shorted)	Position Two (Pin 2 and 3 Shorted)	Position Three (All Pins Open)	Related Ref.
J12	Connects TXD0 (U1B, pin 45) to T1IN (U10, pin 13)	Connects TXD1 (U1B, pin 35) to T1IN (U10, pin 13)	Disconnects both lines.	R59, R60* R61*, R184 R185, R213**
J13	Connects RXD0 (U1B, pin 44) to R1OUT (U10, pin 15)	Connects RXD1 (U1B, pin 31) to R1OUT (U10, pin 15)	Disconnects both lines.	R62, R63*, R64*, R65*, R188, R189, R214**

Table 6-7: RS232 Serial Port Jumpers

* Ensure to only fit one option link relating to TXD0 and RXD0.

** When fitted, set the configuration to 'Position One'.

6.5 CAN Configuration

Table 6-8 & Table 6-9 below details the function of the option links associated with CAN configuration.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R74	Connects CANERRn_MTI0C4C_USB0DPRPD (U1B, pin 38) to CANERRn (U11, pin 8).	Disconnects CANERRn_MTI0C4C_USB0DPRPD (U1B, pin 38) from CANERRn (U11, pin 8).	R75*, R76*
R96	Connects CTX1_ALE_ETLINKSTA (U1C, pin 67) to CTX1 (JA5, pin 5).	Disconnects CTX1_ALE_ETLINKSTA (U1C, pin 67) from CTX1 (JA5, pin 5).	R97*, R98*
R99	Connects CRX1_WAITn (U1C, pin 66) to CRX1 (JA5, pin 6).	Disconnects CRX1_WAITn (U1C, pin 66) from CRX1 (JA5, pin 6).	R100*
R239	Connects CTX1 to TXD (U11, pin 1).	Disconnects CTX1 from TXD (U11, pin 1).	R96
R240	Connects CRX1 to RXD (U11, pin 4).	Disconnects CRX1 from RXD (U11, pin 4).	R99
R244	Connects WAKE (U11, pin 9) to GROUND.	Disconnects WAKE (U11, pin 9) from GROUND.	-
R245	Connects VBAT (U11, pin 10) to Board_5V.	Disconnects VBAT (U11, pin 10) from Board_5V.	J14 *
R371	Connects D24_CANSTBn (U1C, pin 146) to CANSTBn (U11, pin 14).	Disconnects D24_CANSTBn (U1C, pin 146) from CANSTBn (U11, pin 14).	-
R372	Connects D25_CANEN (U1C, pin 144) to CANEN (U11, pin 6).	Disconnects D25_CANEN (U1C, pin 144) from CANEN (U11, pin 6).	-

Table 6-8: CAN Option Links

* Not fitted by default.

Table 6-9 below details the different configurations and functions of the CAN jumpers.

Reference	Position One (Pin 1 and 2 Shorted)	Position Two (Pin 2 and 3 Shorted)	Position Three (All Pins Open)	Related Ref.
J14*	Connects VBAT (U11, pin 10) to Board_5V.	Connects VBAT (U11, pin 10) to Unregulated_VCC.	VBAT (U11, pin 10) is not connected to a power supply.	R245

Table 6-9: CAN Jumpers

* Not fitted by default. J14 is bypassed by R245, connecting VBAT to Board_5V.

6.6 External Bus Configuration

Table 6-10 & Table 6-11 below details the function of option links related to configuring the MCU's external bus.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R93*	Connects WR0n_WRn_SSLB1 (U1C, pin 72) to WR0n (JA3, pin 48).	Disconnects WR0n_WRn_SSLB1 (U1C, pin 72) from WR0n (JA3, pin 48).	R94, R95, R237
R94	Connects WR0n_WRn_SSLB1 (U1C, pin 72) to WRn (JA3, pin 26).	Disconnects WR0n_WRn_SSLB1 (U1C, pin 72) from WRn (JA3, pin 26).	R93*, R95, R227
R97*	Connects CTX1_ALE_ETLINKSTA (U1C, pin 67) to ALE (JA3, pin 46).	Disconnects CTX1_ALE_ETLINKSTA (U1C, pin 67) from ALE (JA3, pin 46).	R96, R98*, R233
R100*	Connects CRX1_WAITn (U1C, pin 66) to WAITn (JA3, pin 45).	Disconnects CRX1_WAITn (U1C, pin 66) from WAITn (JA3, pin 45).	R99, R232*
R101	Connects SDCSn (U1C, pin 139) to BD_SDCSn (U3, pin 19).	Disconnects SDCSn (U1C, pin 139) from BD_SDCSn (U3, pin 19)	R102*
R102*	Connects SDCSn (U1C, pin 139) to CON_SDCSn (JA3, pin 28).	Disconnects SDCSn (U1C, pin 139) from CON_SDCSn (JA3, pin 28).	R101
R217*	Connects RSPCKB (U1B, pin 36) to TFT_RSPCKB.	Disconnects RSPCKB (U1B, pin 36) from TFT_RSPCKB.	R28, R248
R218*	Connects MOSIB (U1B, pin 37) to TFT_MOSIB.	Disconnects MOSIB (U1B, pin 37) from TFT_MOSIB.	R29, 250
R219*	Connects MISOB (U1B, pin 33) to TFT_MISOB.	Disconnects MISOB (U1B, pin 33) from TFT_MISOB.	R30, R249
R227	Connects WRn (U1C, pin 72) to JA3_PIN26 (JA3, pin 26).	Disconnects WRn (U1C, pin 72) from JA3_PIN26 (JA3, pin 26).	R228*
R228*	Connects WEn (U1C, pin 136) to JA3_PIN26 (JA3, pin 26).	Disconnects WEn (U1C, pin 136) from JA3_PIN26 (JA3, pin 26).	R227
R229*	Connects SDCLK (U1C, pin 128) to JA3_PIN44 (JA3, pin 44).	Disconnects SDCLK (U1C, pin 128) from JA3_PIN44 (JA3, pin 44).	R230*

Table 6-10: External Bus Option Links (Continued Overleaf)

* Not fitted by default.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R230*	Connects BCLK (U1C, pin 68) to JA3_PIN44 (JA3, pin 44).	Disconnects BCLK (U1C, pin 68) from JA3_PIN44 (JA3, pin 44).	R229*
R232*	Connects WAITn (U1C, pin 66) to JA3_PIN45 (JA3, pin 45).	Disconnects WAITn (U1C, pin 66) from JA3_PIN45 (JA3, pin 45).	R100*, R231
R231	Connects CON_CS0n to JA3_PIN45 (JA3, pin 45).	Disconnects CON_CS0n from JA3_PIN45 (JA3, pin 45).	R232*, R360 R361*
R233	Connects ALE to JA3_PIN46 (JA3, pin 46).	Disconnects ALE from JA3_PIN46 (JA3, pin 46).	R234*
R234*	Connects CKE (U1C, pin 124) to JA3_PIN46 (JA3, pin 46).	Disconnects CKE (U1C, pin 124) from JA3_PIN46 (JA3, pin 46).	R233
R235	Connects WR1n to JA3_PIN47 (JA3, pin 47).	Disconnects WR1n from JA3_PIN47 (JA3, pin 47).	R236*
R236*	Connects DQM1 to JA3_PIN47 (JA3, pin 47).	Disconnects DQM1 from JA3_PIN47 (JA3, pin 47).	R235
R237	Connects WR0n to JA3_PIN48 (JA3, pin 48).	Disconnects WR0n from JA3_PIN48 (JA3, pin 48).	R238*
R238	Connects DQM0 to JA3_PIN48 (JA3, pin 48).	Disconnects DQM0 from JA3_PIN48 (JA3, pin 48).	R237
R360	Connects CS0n (U1C, pin 141) to BD_CS0n (U6*, pin 32).	Disconnects CS0n (U1C, pin 141) from BD_CS0n (U6*, pin 32).	R361*, R370*
R361*	Connects CS0n (U1C, pin 141) to JA3_PIN45 (JA3, pin 45).	Disconnects CS0n (U1C, pin 141) to JA3_PIN45 (JA3, pin 45).	R231, R360
R366*	Connects ETRXER_RMIIRXER_CS7n (U1C, pin 84) to CS7n (U6*, pin 32).	Disconnects ETRXER_RMIIRXER_CS7n (U1C, pin 84) from CS7n (U6*, pin 32).	R365, R370*
R368*	Connects ETCRS_RMIICRS DV_RYBYn (U1C, pin 74) to RYBYn (U6*, pin 17).	Disconnects ETCRS_RMIICRS DV_RYBYn (U1C, pin 74) from RYBYn (U6*, pin 17).	R367

Table 6-11: External Bus Option Links (Continuation)

* Not fitted by default.

6.7 USB Configuration

Table 6-12 & Table 6-13 below details the function of option links related to configuring the USB ports.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R55	Connects MTCLKB_USB1DPUPE (U1B, pin 50) to USB1DPUPE.	Disconnects MTCLKB_USB1DPUPE (U1B, pin 50) from USB1DPUPE.	R54*
R56*	Connects USB0VBUS_USB0VBUSEN-H_USB0OVRCURB (U1B, pin 48) to USB0OVRCURB.	Disconnects USB0VBUS_USB0VBUSEN-H_USB0OVRCURB (U1B, pin 48) from USB0OVRCURB.	J4
R58	Connects MTIOC3A_USB1VBUS (U1B, pin 46) to USB1VBUS.	Disconnects MTIOC3A_USB1VBUS (U1B, pin 46) from USB1VBUS.	R57*
R61*	Connects TXD0_TRIGb_USB0ID (U1B, pin 45) to USB0ID.	Disconnects TXD0_TRIGb_USB0ID (U1B, pin 45) from USB0ID.	R59, R60*
R65*	Connects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) to USB0EXICEN.	Disconnects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) from USB0EXICEN.	R62, R63*, R64*
R68*	Connects SCK0_TMR0_USB0DRPD (U1B, pin 43) to USB0DRPD.	Disconnects SCK0_TMR0_USB0DRPD (U1B, pin 43) from USB0DRPD.	R66, R67*
R71*	Connects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) to USB0DPUPE-O.	Disconnects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) from USB0DPUPE-O.	R69, R70*
R73*	Connects MTIOC4A_USB0VBUSEN-O (U1B, pin 40) to USB0VBUSEN-O.	Disconnects MTIOC4A_USB0VBUSEN-O (U1B, pin 40) from USB0VBUSEN-O.	R72
R76*	Connects CANERRn_MTI0C4C_USB0DPRPD (U1B, pin 38) to USB0DPRPD.	Disconnects CANERRn_MTI0C4C_USB0DPRPD (U1B, pin 38) from USB0DPRPD.	R74, R75* J15
R254	Connects USB0OVRCURA to FLG (U12, pin 2).	Disconnects USB0OVRCURA from FLG (U12, pin 2).	R255*, R53* J3
R255*	Connects USB0OVRCURA to STATUS1 (U13, pin 5).	Disconnects USB0OVRCURA from STATUS1 (U13, pin 5).	R254
R258*	Connects SHDN (U13, pin 11) to USB0EXICEN. Shuts down U13 and reduces supply current.	Disconnects SHDN (U13, pin 11) from USB0EXICEN. Enables the OTG normal operation.	R65*, R64*, R63*, R62
R265	Connects USB0VBUS to VBUS0 (USB Connectors: USB0_1, USB0_2 and USB0_3).	Disconnects USB0VBUS from VBUS0 (USB Connectors: USB0_1, USB0_2 and USB0_3).	J17*, J18
R270	Connects VBUS (USB Connectors: USB0_1, USB0_2 and USB0_3) to USB0_VBUSEL (J18, pin 2).	Disconnects VBUS (USB Connectors: USB0_1, USB0_2 and USB0_3) from USB0_VBUSEL (J18, pin 2).	L2*
R271	Connects FRAME (USB Connectors: USB0_1, USB0_2 and USB0_3) to GROUND.	Disconnects FRAME (USB Connectors: USB0_1, USB0_2 and USB0_3) from GROUND.	-
R272	Connects USB1VBUS to VBUS (USB Connector: USB1 Function).	Disconnects USB1VBUS from VBUS (USB Connector: USB1 Function).	J19*
R276	Connects VBUS (USB Connector: USB1 Function) to USB1VBUS.	Disconnects VBUS (USB Connector: USB1 Function) from USB1VBUS.	L3*, R272

Table 6-12: USB Option Links (Continued Overleaf)

* Not fitted by default.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R280	Connects FRAME (USB Connectors: USB_1 Function) to GROUND.	Disconnects FRAME (USB Connectors: USB_1 Function) from GROUND.	-
R281*	Connects VBUS0 to VBUS	Disconnects VBUS0 from VBUS.	J20*
R373	Connects USB0DP (U1B, pin 59) to D+ (USB Connectors: USB0_2 and USB0_3).	Disconnects USB0DP (U1B, pin 59) from D+ (USB Connectors: USB0_2 and USB0_3).	-
R374	Connects USB0DM (U1B, pin 58) to D- (USB Connectors: USB0_2 and USB0_3).	Disconnects USB0DM (U1B, pin 58) from D- (USB Connectors: USB0_2 and USB0_3).	-

Table 6-13: USB Option Links (Continuation)

* Not fitted by default.

Table 6-14 below details the different configurations for the USB0DPUPE-F and USB0OVRCURA USB jumpers.

Reference	Position One (Pin 1 and 2 Shorted)	Position Two (Pin 2 and 3 Shorted)	Position Three (All Pins Open)	Related Ref.
J3	Connects MTCLKA_USB0DPUPE-F_USB0OVRCURA (U1B, pin 51) to USB0DPUPE-F.	Connects MTCLKA_USB0DPUPE-F_USB0OVRCURA (U1B, pin 51) to USB0OVRCURA.	Do not set. Unless R53 is fitted.	R53*
J4	Connects USB0VBUS_USB0VBUSEN-H_USB0OVRCURB (U1B, pin 48) to USB0VBUS.	Connects USB0VBUS_USB0VBUSEN-H_USB0OVRCURB (U1B, pin 48) to USB0VBUSEN-H	Do not set. Unless R56 is fitted.	R56*

Table 6-14: USB Jumpers USB0DPUPE-F / USB0OVRCURA Configuration

* Not fitted by default.

Table 6-15 below details the different configurations and functions for the USB0OVRCURA Selection.

Reference	R254	R255	Function	Related Ref.
Link Configuration	Fitted	Removed	Host mode	R53*, J3
	Removed	Fitted	OTG mode	

Table 6-15: USB Mode USB0OVRCURA Configuration

* Not fitted by default.

Table 6-16 below details the different configurations and functions of the USB jumpers.

Reference	Position One (Pin 1 and 2 Shorted)	Position Two (All Pins Open)	Related Ref.
J15/J16*	Host mode	Function and OTG mode	-

Table 6-16: USB Jumpers (USB0DPRPD, DRPD Pull-down Configuration)

* Ensure J15 and J16 are set to the same position.

Table 6-17 below details the different configurations and functions of the USB jumpers.

Reference	J17*	J20*	Function
Position	Pin 1 and 2 shorted	Pin 1 and 2 shorted (via R281)	Bus-powered
	Pin 2 and 3 shorted (via R265)	All open	Self-powered

Table 6-17: USB Jumpers (VBUS0 Self-powered/Bus-powered Configuration)

* Not fitted by default. Ensure J17 and J20 have the same configuration.

Table 6-18 below details the different configurations and functions of the USB jumpers.

Reference	Position One (Pin 1 and 2 Shorted)	Position Two (Pin 2 and 3 Shorted)	Position Three (All Pins Open)	Related Ref.
J18	Host mode. (Ensure R269 is removed)	Function mode. (Ensure R269 is removed)	OTG mode. (Ensure R269 is fitted)	R269*

Table 6-18: USB Jumpers (VBUS0 Host/Function/OTG Select)

* Not fitted by default.

Table 6-19 below details the different configurations and functions of the USB jumpers.

Reference	J19*	J20*	Function
Position	Pin 1 and 2 shorted	Pin 2 and 3 shorted	Bus-powered
	Pin 2 and 3 shorted (via R272)	All open	Self-powered

Table 6-19: USB Jumpers (VBUS1 Self-powered/Bus-powered Configuration)

* Not fitted by default.

Note:

The RSK+RX63N board is configured for Function mode USB operations. **Table 6-20** below lists the required changes to configure the board for USB Host mode.

Reference	J3	J4	J15	J16	J18
Position	Pin 2 and 3 shorted	Pin 2 and 3 shorted	Pin 1 and 2 shorted	Pin 1 and 2 shorted	Pin 1 and 2 shorted

Table 6-20: USB0 Jumpers (Host Mode Configuration)

6.8 Ethernet Configuration

Table 6-21 & Table 6-22 below details the function of option links related to configuring the MCU's Ethernet peripheral.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R98*	Connects CTX1_ALE_ETLINKSTA to ETLINKSTA (U14, pin 10).	Disconnects CTX1_ALE_ETLINKSTA from ETLINKSTA (U14, pin 10).	R96, R97*
R105	Connects ETRXDV_MTI0C4B to ETRXDV (U14, pin 19).	Disconnects ETRXDV_MTI0C4B from ETRXDV (U14, pin 19)	R106*, R299
R107	Connects ETTXER_MTI0C4D to ETTXER (U14, pin 1).	Disconnects ETTXER_MTI0C4D from ETTXER (U14, pin 1)	R108*, R295, R307*, R308*
R109	Connects ETTXCLK_MTI0C3D to ETTXCLK (U14, pin 22).	Disconnects ETTXCLK_MTI0C3D from ETTXCLK (U14, pin 22)	R110*, R294
R111	Connects ETETXD2_MTI0C3B to ETETXD2 (U14, pin 26).	Disconnects ETETXD2_MTI0C3B from ETETXD2 (U14, pin 26)	R112*, R296, R322*
R294	Connects ETTXCLK to U14 (pin 22) via U15 (pin 15).	Disconnects ETTXCLK from U14 (pin 22).	R109, R110*
R295	Connects ETTXER to U14 (pin 1) via U15 (pin 14) and (R107).	Disconnects ETTXER from U14 (pin 1).	R107, R307* R308*
R296	Connects ETETXD2 to U14 (pin 26) via U15 (pin 16) and (R111).	Disconnects ETETXD2 from U14 (pin 26).	R111, R322*
R297	Connects ETETXD3 to U14 (pin 27) via U15 (pin 17).	Disconnects ETETXD3 from U14 (pin 27).	R323*
R298	Connects ETRXCLK_REF50CK (U1C, pin 85) to U14 (pin 20).	Disconnects ETRXCLK_REF50CK (U1C, pin 85) from U14 (pin 20).	-
R299	Connects ETRXDV to U14 (pin 19) via U15 (pin 13).	Disconnects ETRXDV from U14 (pin 19).	R105
R300	Connects ETERXD2 to U14 (pin 16) via U15 (pin 12).	Disconnects ETERXD2 from U14 (pin 16).	R318*
R301	Connects ETERXD3 to U14 (pin 15) via U15 (pin 11).	Disconnects ETERXD3 from U14 (pin 15).	R320
R302	Connects ETCOL to U14 (pin 36) via U15 (pin 18).	Disconnects ETCOL from U14 (pin 36).	R303*
R303*	Connects ETCRS_RMI0CRSDV to U14 (pin 36).	Disconnects ETCRS_RMI0CRSDV from U14 (pin 36).	R302, R304
R304	Connects ETCRS_RMI0CRSDV to U14 (pin 3).	Disconnects ETCRS_RMI0CRSDV from U14 (pin 3).	R319*
R320	Connects ETERXD3 to GROUND, via R315.	Disconnects ETERXD3 from GROUND.	R315, R301
R322*	Connects ETETXD2 to GROUND.	Disconnects ETETXD2 from GROUND.	R296
R323*	Connects ETETXD3 to GROUND.	Disconnects ETETXD3 from GROUND.	R297
R324	Connects XTAL1 (U14, pin 14) to X4 (pin 1).	Disconnects XTAL1 (U14, pin 14) from X4 (pin 1).	R326

Table 6-21: Ethernet Option Links (Continued Overleaf)

* Not fitted by default.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R325	Connects XTAL2 (U14, pin 13) to X4 (pin 2).	Disconnects XTAL2 (U14, pin 13) from X4 (pin 2).	-
R326*	Connects XTAL1 (U14, pin 14) to X5 (pin 3).	Disconnects XTAL1 (U14, pin 14) from X5 (pin 3).	R327*, R324
R327*	Connects X5 (pin 3) to ETRXCLK_REF50CK (U1C, pin 85) and U14 (pin 20).	Disconnects X5 (pin 3) from ETRXCLK_REF50CK (U1C, pin 85) and U14 (pin 20).	R326, R298
R328	Connects X5 (pin 1) to GROUND.	Disconnects X5 (pin 1) from GROUND.	-
R339*	Connects U14 (pin 9) to GROUND.	Disconnects U14 (pin 9) from GROUND.	-
R340*	Connects U14 (pin 12) to GROUND	Disconnects U14 (pin 12) from GROUND	-
R341*	Connects U14 (pin 11) to GROUND.	Disconnects U14 (pin 11) from GROUND.	-
R342*	Connects U14 (pin 10) to GROUND	Disconnects U14 (pin 10) from GROUND	-
R344	Connects ETHERNET port (pin 10) to GROUND.	Disconnects ETHERNET port (pin 10) from GROUND.	R303*, R304, R368*
R365	Connects ETRXER_RMIIRXER_CS7n (U1C, pin 84) to ETRXER_RMIIRXER (U14, pin 21).	Disconnects ETRXER_RMIIRXER_CS7n (U1C, pin 84) from ETRXER_RMIIRXER (U14, pin 21).	R366*
R367	Connects ETCRS_RMIICRS DV_RYBYn (U1C, pin 74) to ETCRS_RMIICRS DV (U14, pin 3 or pin 36).	Disconnects ETCRS_RMIICRS DV_RYBYn (U1C, pin 74) from ETCRS_RMIICRS DV (U14, pin 3 and pin 36).	R303*, R304, R368*

Table 6-22: Ethernet Option Links (Continuation)

* Not fitted by default.

6.9 Multi-Function Timer Pulse Unit (MTU) Configuration

Table 6-23 & Table 6-24 details the function of option links related to configuring the MCU's MTU pins.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R45*	Connects LED2_MTIC5W (U1B, pin 56) to MTIC5W (JA6, pin 16).	Disconnects LED2_MTIC5W (U1B, pin 56) from MTIC5W (JA6, pin 16).	R44
R47*	Connects LED3_MTIC5V (U1B, pin 55) to MTIC5V (JA6, pin 15).	Disconnects LED3_MTIC5V (U1B, pin 55) from MTIC5V (JA6, pin 15).	R46
R49*	Connects MTIC5U_SCL0 (U1B, pin 54) to MTIC5U (JA6, pin 14).	Disconnects MTIC5U_SCL0 (U1B, pin 54) from MTIC5U (JA6, pin 14).	R48
R50*	Connects MTIOC0B_IRQ3_SDA0 (U1B, pin 53) to MTIOC0B (JA2, pin 9).	Disconnects MTIOC0B_IRQ3_SDA0 (U1B, pin 53) from MTIOC0B (JA2, pin 9).	R51*, R52, R223*
R53*	Connects MTCLKA_USB0DPUPE-F_USB0OVRCURA (U1B, pin 51) to MTCLKA (JA2, pin 25).	Disconnects MTCLKA_USB0DPUPE-F_USB0OVRCURA (U1B, pin 51) from MTCLKA (JA2, pin 25).	J3
R54*	Connects MTCLKB_USB1DPUPE (U1B, pin 50) to MTCLKB (JA2, pin 26).	Disconnects MTCLKB_USB1DPUPE (U1B, pin 50) from MTCLKB (JA2, pin 26).	R55
R57*	Connects MTIOC3A_USB1VBUS (U1B, pin 46) to MTIOC3A (JA6, pin 13).	Disconnects MTIOC3A_USB1VBUS (U1B, pin 46) from MTIOC3A (JA6, pin 13).	R58
R60*	Connects TXD0_TRIGb_USB0ID (U1B, pin 45) to TRIGb (JA2, pin 22).	Disconnects TXD0_TRIGb_USB0ID (U1B, pin 45) from TRIGb (JA2, pin 22).	R59, R61*
R63*	Connects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) to MTIOC1B (JA2, pin 23).	Disconnects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) from MTIOC1B (JA2, pin 23).	R62, R64*, R65*, R224, R255*, R226*
R64*	Connects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) to TRIGa (JA2, pin 21).	Disconnects RXD0_MTI0C1B_TRIGa_USB0EXICEN (U1B, pin 44) from TRIGa (JA2, pin 21).	R62, R63*, R65*
R67*	Connects SCK0_TMR0_USB0DRPD (U1B, pin 43) to TMR0 (JA2, pin 19).	Disconnects SCK0_TMR0_USB0DRPD (U1B, pin 43) from TMR0 (JA2, pin 19).	R66, R68*
R70*	Connects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) to TMR1 (JA2, pin 20).	Disconnects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) from TMR1 (JA2, pin 20).	R69, R71*
R72	Connects MTIOC4A_USB0VBUSEN-O (U1B, pin 40) to MTIOC4A (JA2, pin 15).	Disconnects MTIOC4A_USB0VBUSEN-O (U1B, pin 40) from MTIOC4A (JA2, pin 15).	R73*
R75*	Connects CANERRn_MTI0C4C_USB0DPRPD (U1B, pin 38) to MTIOC4C (JA2, pin 16).	Disconnects CANERRn_MTI0C4C_USB0DPRPD (U1B, pin 38) from MTIOC4C (JA2, pin 16).	R74, R76*
R77	Connects MTIOC0C_IRQ2 (U1B, pin 29) to MTIOC0C (JA2, pin 23).	Disconnects MTIOC0C_IRQ2 (U1B, pin 29) from MTIOC0C (JA2, pin 23).	R224, R225*, R226*, R78
R81	Connects MTIOC0A_IRQ4 (U1B, pin 27) to MTIOC0A (JA2, pin 7).	Disconnects MTIOC0A_IRQ4 (U1B, pin 27) from MTIOC0A (JA2, pin 7).	R82*, R220*, R221

Table 6-23: MTU Option Links (Continued Overleaf)

* Not fitted by default.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R106*	Connects ETRXDV_MTI0C4B (U1C, pin 86) to MTI0C4B (JA2, pin 17) via U15.	Disconnects ETRXDV_MTI0C4B (U1C, pin 86) from MTI0C4B (JA2, pin 17).	R105
R108*	Connects ETTXER_MTI0C4D (U1C, pin 83) to MTI0C4D (JA2, pin 18) via U15.	Disconnects ETTXER_MTI0C4D (U1C, pin 83) from MTI0C4D (JA2, pin 18).	R107
R110*	Connects ETTXCLK_MTI0C3D (U1C, pin 82) to MTI0C3D (JA2, pin 14) via U15.	Disconnects ETTXCLK_MTI0C3D (U1C, pin 82) from MTI0C3D (JA2, pin 14).	R109
R112*	Connects ETETXD2_MTI0C3B (U1C, pin 78) to MTI0C3B (JA2, pin 13) via U15.	Disconnects ETETXD2_MTI0C3B (U1C, pin 78) from MTI0C3B (JA2, pin 13).	R111
R221	Connects MTI0C0A (U1B, pin 27) to JA2_PIN7 (JA2, pin 7).	Disconnects MTI0C0A (U1B, pin 27) from JA2_PIN7 (JA2, pin 7).	R81, R220*
R223*	Connects MTI0C0B (U1B, pin 53) to JA2_PIN9 (JA2, pin 9).	Disconnects MTI0C0B (U1B, pin 53) from JA2_PIN9 (JA2, pin 9).	R50, R222
R225*	Connects MTI0C1B (U1B, pin 44) to JA2_PIN23 (JA2, pin 23).	Disconnects MTI0C1B (U1B, pin 44) from JA2_PIN23 (JA2, pin 23).	R63, R224, R226*
R226*	Connects MTI0C0C (U1B, pin 29) to JA2_PIN23 (JA2, pin 23).	Disconnects MTI0C0C (U1B, pin 29) from JA2_PIN23 (JA2, pin 23).	R77, R224, R225*

Table 6-24: MTU Option Links (Continuation)

* Not fitted by default.

6.10 IRQ & General I/O Pin Configuration

Table 6-25 & Table 6-26 below details the function of the option links associated with IRQ and general I/O pin configuration.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R28	Connects RSPCKB to U1B (pin 36)	Disconnects RSPCKB from U1B (pin 36)	-
R29	Connects MOSIB to U1B (pin 37)	Disconnects MOSIB from U1B (pin 37)	-
R30	Connects MISOB to U1B (pin 33)	Disconnects MISOB from U1B (pin 33)	-
R31	Connects BCLK to U1C (pin 68)	Disconnects BCLK from U1C (pin 68)	-
R32	Connects SDCLK to U1C (pin 128)	Disconnects SDCLK from U1C (pin 128)	-
R34	Connects IRQ8_TXD6 (U1B, pin 8) to IRQ8 (JA1, pin 23).	Disconnects IRQ8_TXD6 (U1B, pin 8) from IRQ8 (JA1, pin 23).	R35*, R167
R36	Connects IRQ9_RXD6 (U1B, pin 7) to IRQ9 (JA5, pin 9).	Disconnects IRQ9_RXD6 (U1B, pin 7) from IRQ9 (JA5, pin 9).	R37*
R38	Connects IRQ10_SCK6 (U1B, pin 6) to IRQ10 (JA5, pin 10).	Disconnects IRQ10_SCK6 (U1B, pin 6) from IRQ10 (JA5, pin 10).	R39*, R166 R307*

Table 6-25: IRQ & General I/O Option Links (Continued Overleaf)

* Not fitted by default.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R40	Connects LED0_DA0 (U1B, pin 4) to LED0	Disconnects LED0_DA0 (U1B, pin 4) from LED0	R41*
R42	Connects LED1_DA1 (U1B, pin 2) to LED1	Disconnects LED1_DA1 (U1B, pin 2) from LED1	R43*
R44	Connects LED2_MTIC5W (U1B, pin 56) to LED2	Disconnects LED2_MTIC5W (U1B, pin 56) from LED2	R45*
R46	Connects LED3_MTIC5V (U1B, pin 55) to LED3	Disconnects LED3_MTIC5V (U1B, pin 55) from LED3	R47*
R48	Connects MTIC5U_SCL0 (U1B, pin 54) to SCL0 (U5, pin 6)	Disconnects MTIC5U_SCL0 (U1B, pin 54) from SCL0 (U5, pin 6)	R136, R49*
R51*	Connects MTIOC0B_IRQ3_SDA0 (U1B, pin 53) to IRQ3 (JA2, pin 9).	Disconnects MTIOC0B_IRQ3_SDA0 (U1B, pin 53) from IRQ3 (JA2, pin 9).	R50*, R52, R222
R52	Connects MTIOC0B_IRQ3_SDA0 (U1B, pin 53) to SDA0 (U5, pin 5)	Disconnects MTIOC0B_IRQ3_SDA0 (U1B, pin 53) from SDA0 (U5, pin 5)	R50*, R51, R135
R78*	Connects MTIOC0C_IRQ2 (U1B, pin 29) to IRQ2 (JA2, pin 23).	Disconnects MTIOC0C_IRQ2 (U1B, pin 29) from IRQ2 (JA2, pin 23).	R77
R82*	Connects MTIOC0A_IRQ4 (U1B, pin 27) to IRQ4 (JA2, pin 7).	Disconnects MTIOC0A_IRQ4 (U1B, pin 27) from IRQ4 (JA2, pin 7).	R81, R220*
R69	Connects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) to CTS0RTS0 (JA2, pin 12)	Disconnects CTS0RTS0_TMR1_USB0DPUPE-O (U1B, pin 42) from CTS0RTS0 (JA2, pin 12)	R70*, R71*
R86	Connects AN004_XINPUT1 (U1C, pin 168) to XINPUT1 (TFT connector, pin 43)	Disconnects AN004_XINPUT1 (U1C, pin 168) from XINPUT1 (TFT connector, pin 43)	R85*
R88	Connects AN005_YINPUT1 (U1C, pin 167) to YINPUT1 (TFT connector, pin 44)	Disconnects AN005_YINPUT1 (U1C, pin 167) from YINPUT1 (TFT connector, pin 44)	R87*
R90	Connects AN006_XINPUT2 (U1C, pin 166) to XINPUT2 (TFT connector, pin 45)	Disconnects AN006_XINPUT2 (U1C, pin 166) from XINPUT2 (TFT connector, pin 45)	R89*
R92	Connects AN007_YINPUT2 (U1C, pin 165) to YINPUT2 (TFT connector, pin 46)	Disconnects AN007_YINPUT2 (U1C, pin 165) from YINPUT2 (TFT connector, pin 46)	R91*
R95	Connects WR0n_WRn_SSLB1 (U1C, pin 72) to SSLB1 (TFT connector, pin 32)	Disconnects WR0n_WRn_SSLB1 (U1C, pin 72) from SSLB1 (TFT connector, pin 32)	R94, R93*
R220*	Connects IRQ4 (U1B, pin 27) to JA2_PIN7 (JA2, pin 7).	Disconnects IRQ4 (U1B, pin 27) from JA2_PIN7 (JA2, pin 7).	R82*, R221
R222	Connects IRQ3 (U1B, pin 54) to JA2_PIN9 (JA2, pin 9).	Disconnects IRQ3 (U1B, pin 54) from JA2_PIN9 (JA2, pin 9).	R51*, R223*
R224	Connects IRQ2 (U1B, pin 29) to JA2_PIN23 (JA2, pin 23).	Disconnects IRQ2 (U1B, pin 29) from JA2_PIN23 (JA2, Pin23)	R78*, R225*, R226*

Table 6-26: IRQ & General I/O Option Links (Continuation)

* Not fitted by default.

Table 6-27 below details the function of the jumpers associated with IRQ and general I/O pin configuration.

Reference	Position One	Position Two	Position Three	Related Ref.
J5	Pins 1 and 2 shorted. Connects ETCOL_PC7 (U1C, pin 76) to ETCOL (U14, pin 36), via U15.	Pins 2 and 3 shorted. Connects ETCOL_PC7 (U1C, pin 76) to PC7 (E1 interface, pin 10), via U15.	All pins open.	SW4 R302 R201

Table 6-27: IRQ & General I/O Jumpers

Table 6-28 below details the function of option links related to configuring the bus switches U2 and U15.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
J2*	Enables bus switch U2.	Disables bus switch U2.	-
J21	Enables bus switch U15.	Disables bus switch U15.	-

Table 6-28: Bus Switch Jumper Links

* Not fitted by default.

6.11 Power Supply Configuration

Table 6-29 & Table 6-30 below details the function of the option links associated with power supply configuration.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R147	Enables Unregulated_VCC to be supplied power from PWR1connector or VBUS (USB connectors).	Unregulated_VCC is not supplied power.	-
R148	Enables CON_5V to be supplied power from PWR1connector or VBUS (USB connectors).	CON_5V is not supplied power.	J9
R149	Enables Board_5V to be supplied power from PWR1connector or VBUS (USB connectors).	Board_5V is not supplied power.	J9
R150	Connects U8's (voltage regulator) 3.3V output to CON_3V3, Board_VCC and UC_VCC (MCU power).	Disconnects U8's (voltage regulator) 3.3V output from CON_3V3, Board_VCC and UC_VCC (MCU power).	R151, R152 J10*
R151	CON_3V3 (JA1, pin 3) is supplied power from U8 or Board_VCC.	CON_3V3 (JA1, pin 3) is not supplied power from U8 or Board_VCC.	R150
R152	UC_VCC (MCU power) is supplied power from U8 or Board_VCC.	UC_VCC (MCU power) is not supplied power from U8 or Board_VCC.	R150, J10*

Table 6-29: Power Supply Option Links (Continued Overleaf)

* Not fitted by default.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R153*	CON_3V3USB is supplied power from Board_VCC.	CON_3V3USB is not supplied power from Board_VCC.	R154
R154	Enables Board_VCC to supply power to CON_3V3USB and 3V3USB.	Disables Board_VCC from supplying power to CON_3V3USB and 3V3USB.	R150
R155*	CON_5VUSB is supplied power from Board_5V.	CON_5VUSB is not supplied power from Board_5V.	R156, R149 J9
R156	Enables Board_5V to supply power to CON_5VUSB and 5VUSB.	Disables Board_5V from supplying power to CON_5VUSB and 5VUSB.	R149, J9

Table 6-30: Power Supply Option Links (Continuation)

* Not fitted by default.

Table 6-31 below details the function of the jumpers associated with power supply configuration.

Reference	Position One	Position Two	Position Three	Related Ref.
J10*	Pins 1 and 2 shorted. Enables UC_VCC (MCU power) to be supplied from Board_VCC or U8.	Pins 1 and 2 open. UC_VCC is not supplied power. ENSURE TO SHORT J10 OR FIT R152.	-	R152, R150
PWR2	Enables CON_3V3USB to be supplied externally.	Pins 1 and 2 open.	-	R153*, R154
PWR3	Enables CON_5VUSB to be supplied externally.	Pins 1 and 2 open.	-	R155*, R156
PWR4	Enables a CR2032 battery to be fitted. Supplies power to the RTC and sub-clock oscillator when a UC_VCC voltage drop is detected.	Battery not fitted.	-	J1, R4*

Table 6-31: Power Supply Jumpers

* Not fitted by default.

6.12 Clock Configuration

Table 6-32 below details the function of the option links associated with clock configuration.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R17*	X1 feedback resistor. Connects X1 pins 1 and 2.	X1 feedback resistor. Disconnected from X1 pins 1 and 2.	-
R18	Connects XTAL (U1B, pin 22) to X1 (pin 1).	Disconnects XTAL (U1B, pin 22) from X1 (pin 1).	R21*
R19	Connects EXTAL (U1B, pin 24) to X1 (pin 2).	Disconnects EXTAL (U1B, pin 24) from X1 (pin 2).	R22*, R23*
R20*	Connects X2 feedback resistor. Connects X2's pins 1 and 2.	X2 feedback resistor. Disconnected from X2 pins 1 and 2.	-
R21*	Connects XTAL (U1B, pin 22) to X2 (pin 1).	Disconnects XTAL (U1B, pin 22) from X2 (pin 1).	-
R22*	Connects EXTAL (U1B, pin 24) to X2 (pin 2).	Disconnects EXTAL (U1B, pin 24) from X2 (pin 2).	-
R23*	Connects EXTAL (U1B, pin 24) to CON_EXTAL (JA2, pin 2).	Disconnects EXTAL (U1B, pin 24) from CON_EXTAL (JA2, pin 2).	R18**, R19**
R24*	X3 feedback resistor. Connects X3 pins 1 and 2.	X3 feedback resistor. Disconnected from X3 pins 1 and 2.	-
R25	Connects XCIN (U1B, pin 19) to X3 (pin 1).	Disconnects XCIN (U1B, pin 19) from X3 (pin 1).	R27*
R26	Connects XCOU (U1B, pin 20) to X3 (pin 4).	Disconnects XCOU (U1B, pin 20) from X3 (pin 4).	-
R27*	Connects XCIN (U1B, pin 19) to GROUND.	Disconnects XCIN (U1B, pin 19) from GROUND.	R25

Table 6-32: Clock Option Links

* Not fitted by default.

** If option link R23 is to be fitted and an external clock signal is to be used, ensure to remove R18 and R19.

6.13 External Memory Configuration

Table 6-33 & Table 6-34 below details the function of the option links associated with external memory configuration.

Reference	Link Fitted Configuration	Link Removed Configuration	Related Ref.
R118	Connects SDCLK (U1C, pin 128) to CLK (U3, pin 38) via R32.	Disconnects SDCLK (U1C, pin 128) from CLK (U3, pin 38).	R32
R128	Connects WP# (U4, pin 3) to GROUND. Disables writing to the flash IC.	Disconnects WP# (U4, pin 3) from GROUND. Enables writing to the flash IC.	-
R129	Connects HOLD# (U4, pin 7) to GROUND. Enables suspensions on the serial flash IC operations.	Disconnects HOLD# (U4, pin 7) from GROUND. Disables suspension of serial flash IC operations.	-

Table 6-33: External Memory Configuration

Table 6-34 below details the function of the jumper associated with external memory configuration.

Reference	Position One	Position Two	Position Three	Related Ref.
J7	Pins 1 and 2 shorted. Connects WP (U5, pin 7) to GROUND, disabling write protection on the I²C EEPROM IC (bypassed by R137).	All pins open. WP (U5, pin 7) is disconnected from GROUND, enabling write protection on the I ² C EEPROM IC (still connectable by R137).	-	R137*

Table 6-34: External EEPROM Memory Configuration

* Not fitted by default.

7. Headers

7.1 Application Headers

This RSK+ is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.

Table 7-1 below lists the connections of the application header, JA1.

Application Header JA1					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	5V	-	2	0V	-
	CON_5V			GROUND	
3	3V3	-	4	0V	-
	CON_3V3			GROUND	
5	AVCC	175	6	AVSS	1
	CON_AVCC0			CON_AVSS0	
7	AVREF	174	8	ADTRG	176
	CON_VREFH0			ADTRG0n	
9	ADC0	173	10	ADC1	171
	AN000			AN001	
11	ADC2	170	12	ADC3	169
	AN002			AN003	
13	DAC0	4	14	DAC1	2
	DA0			DA1	
15	IO_0	158	16	IO_1	156
	IO0			IO1	
17	IO_2	154	18	IO_3	150
	IO2			IO3	
19	IO_4	148	20	IO_5	147
	IO4			IO5	
21	IO_6	145	22	IO_7	143
	IO6			IO7	
23	IRQ3 / IRQAEC / M2_H SIN0	8 / NC / NC	24	IIC_EX	NC
	IRQ8			NC	
25	IIC_SDA	53	26	IIC_SCL	54
	JA1_SDA (SDA0)			JA1_SCL0 (SCL0)	

Table 7-1: Application Header JA1 Connections

Table 7-2 below lists the connections of the application header, JA2.

Application Header JA2					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	RESET	21	2	EXTAL	24
	RESn			CON_EXTAL	
3	NMI	26	4	Vss1	-
	NMIIn			GROUND	
5	WDT_OVF	NC	6	SCIaTX	45
	NC			TXD0	
7	IRQ0 / WKUP / M1_H SIN0	27 / NC / 27	8	SCIaRX	44
	IRQ2 / NC / MTIOC0A			RXD0	
9	IRQ1 / M1_H SIN1	53 / 53	10	SCIaCK	43
	IRQ3 / MTIOC0B			SCK0	
11	M1_UD	13	12	CTSRTS	42
	MTIOC3C			CTS0RTS0	
13	M1_UP	78	14	M1_UN	82
	MTIOC3B			MTIOC3D	
15	M1_VP	40	16	M1_VN	38
	MTIOC4A			MTIOC4C	
17	M1_WP	86	18	M1_WN	83
	MTIOC4B			MTIOC4D	
19	TimerOut	43	20	TimerOut	42
	TMR0			TMR1	
21	TimerIn	44	22	TimerIn	45
	TRIGa			TRIGb	
23	IRQ2 / M1_EncZ / M1_H SIN2	29 / 44/ 29	24	M1_POE	28
	IRQ2 / MTIOC1B / MTIOC0C			POE3n	
25	M1_TRCCLK	51	26	M1_TRDCLK	50
	MTCLKA			MTCLKB	

Table 7-2: Application Header JA2 Connections

Table 7-3 below lists the connections of the BUS application header, JA3

Bus Application Header JA3					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	A0	118	2	A1	114
	A0			A1	
3	A2	112	4	A3	110
	A2			A3	
5	A4	109	6	A5	108
	A4			A5	
7	A6	107	8	A7	106
	A6			A7	
9	A8	104	10	A9	100
	A8			A9	
11	A10	99	12	A11	98
	A10			A11	
13	A12	97	14	A13	96
	A12			A13	
15	A14	95	16	A15	94
	A14			A15	
17	D0	158	18	D1	156
	D0_IO0			D1_IO1	
19	D2	154	20	D3	150
	D2_IO2			D3_IO3	
21	D4	148	22	D5	147
	D4_IO4			D5_IO5	
23	D6	145	24	D7	143
	D6_IO6			D7_IO7	
25	RDn	70	26	WR / SDWE	72 / 136
	RDn			WRn / WEn	
27	CSa	93	28	CSb	139
	CS3n			CON_SDCSn	
29	D8	135	30	D9	134
	D8			D9	
31	D10	133	32	D11	132
	D10			D11	
33	D12	131	34	D13	130
	D12			D13	
35	D14	126	36	D15	125
	D14			D15	
37	A16	91	38	A17	89
	A16_ETERXD3			A17_ETERXD2	
39	A18	86	40	A19	83
	A18_ETRXDV_MTI0C4B			A19_ETTXER_MTI0C4D	
41	A20	82	42	A21	78
	A20_ETTXCLK_MTI0C3D			A21_ETETXD2_MTI0C3B	
43	A22	77	44	SDCLK	128 / 68
	A22_ETETXD3			SDCLK / BCLK	
45	CSc / Wait	14 / 66	46	ALE / SDCKE	67 / 124
	CON_SC0n / WAITn			ALE / CKE	
47	HWRn / DQM1	71 / 120	48	LWRn / DQM0	72 / 122
	WR1n / DQM1			WR0n / DQM0	
49	CAS	137	50	RAS	138
	CASn			RASn	

Table 7-3: Bus Application Header JA3 Connections

Table 7-4 below lists the connections of the application header, JA5.

Application Header JA5					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	ADC4	168	2	ADC5	167
	AN004			AN005	
3	ADC6	166	4	ADC7	165
	AN006			AN007	
5	CAN1TX	67	6	CAN1RX	66
	CTX1			CRX1	
7	CAN2TX	NC	8	CAN2RX	NC
	NC			NC	
9	IRQ4 / M2_EncZ / M2HSIN1	7 / NC / NC	10	IRQ5 / M2_H SIN2	6 / NC
	IRQ9 / NC / NC			IRQ10 / NC	
11	M2_UD	NC	12	M2_Uin	NC
	NC			NC	
13	M2_Vin	NC	14	M2_Win	NC
	NC			NC	
15	M2_Toggle	NC	16	M2_POE	NC
	NC			NC	
17	M2_TRCCLK	NC	18	M2_TRDCLK	NC
	NC			NC	
19	M2_UP	NC	20	M2_Un	NC
	NC			NC	
21	M2_VP	NC	22	M2_Vn	NC
	NC			NC	
23	M2_WP	NC	24	M2_Wn	NC
	NC			NC	

Table 7-4: Application Header JA5 Connections

Table 7-5 below lists the connections of the application header, JA6.

Application Header JA6					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	DREQ	61	2	DACK	62
	EDREQ1			EDACK1	
3	TEND	NC	4	STBYn	NC
	NC			NC	
5	RS232TX	NC	6	RS232RX	NC
	RS232TX			RS232RX	
7	SClBRX	7	8	SClBTX	8
	RXD6			TXD6	
9	SClCTX	35	10	SClBCK	6
	TXD1			SCK6	
11	SClCCK	34	12	SClCRX	31
	SCK1			RXD1	
13	M1_Toggle	46	14	M1_Uin	54
	MTIOC3A			MTIC5U	
15	M1_Vin	55	16	M1_Win	56
	MTIC5V			MTIC5W	
17	Reserved	NC	18	Reserved	NC
	NC			NC	
19	Reserved	NC	20	Reserved	NC
	NC			NC	
21	Reserved	NC	22	Reserved	NC
	NC			NC	
23	Unregulated_VCC	-	24	Vss	-
	Unregulated_VCC			GROUND	

Table 7-5: Application Header JA6 Connections

7.2 Generic Headers

Generic headers, used to provide easy connections to various pins from devices fitted to the RSK+.

Table 7-6 below lists the connections of the Data Bus Connector, J22.

32bit Data Bus Connector J22					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	D16	163	2	D17	161
	D16			D17	
3	D18	160	4	D19	159
	D18			D19	
5	D20	157	6	D21	155
	D20			D21	
7	D22	152	8	D23	149
	D22			D23	
9	D24	146	10	D25	144
	D24_CANSTBn			D25_CANEN	
11	D26	123	12	D27	121
	D26_TRDATA0			D27_TRDATA1	
13	D28	119	14	D29	116
	D28_TRSYNCn			D29_TRCLK	
15	D30	113	16	D31	111
	D30_TRDATA2			D31_TRDATA3	

Table 7-6: Data Bus Connector J22 Connections

Table 7-7 below lists the connections of the Generic LCD Header (TFT).

Generic LCD Header (TFT)					
Pin	Function (Header Name)	MCU Pin	Pin	Function (Header Name)	MCU Pin
	Circuit Net Name			Circuit Net Name	
1	5V	-	2	5V	-
	Board_5V			Board_5V	
3	3V3	-	4	3V3	-
	Board_VCC			Board_VCC	
5	Reserved	NC	6	Reserved	NC
	NC			NC	
7	B1	158	8	B2	156
	D0_IO0			D1_IO1	
9	B3	154	10	B4	150
	D2_IO2			D3_IO3	
11	B5	148	12	G0	147
	D4_IO4			D5_IO5	
13	G1	145	14	G2	143
	D6_IO6			D7_IO7	
15	G3	135	16	G4	134
	D8			D9	
17	G5	133	18	R1	132
	D10			D11	
19	R2	131	20	R3	130
	D12			D13	
21	R4	126	22	R5	125
	D14			D15	
23	EDACK	62	24	HSYNC	29
	EDACK1			MTIOC0C	
25	DOTCLK	13	26	LCDDEN	27
	MTIOC3C			MTIOC0A	
27	VSYNC	40	28	EDREQ	61
	MTIOC4A			EDREQ1	
29	SSCK	36	30	SSI	33
	TFT_RSPCKB			TFT_MISOB	
31	SSO	37	32	SCS	72
	TFT_MOSIB			SSLB1	
33	RESET	21	34	GND	-
	RESn			GROUND	
35	BACKLIGHT	49	36	SD_DOTCLK	NC
	DLCDD6_BACKLIGHT			NC	
37	GND	-	38	GND	-
	GROUND			GROUND	
39	GND	-	40	GND	-
	GROUND			GROUND	
41	X_DRIVE	69	42	Y_DRIVE	52
	DLCDD4_XDRIVE			DLCDD5_YDRIVE	
43	X_INPUT1	168	44	Y_INPUT1	167
	XINPUT1			YINPUT1	
45	X_INPUT2	166	46	Y_INPUT2	165
	XINPUT2			YINPUT2	
47	Reserved	NC	48	Reserved	NC
	NC			NC	
49	Reserved	NC	50	Reserved	NC
	NC			NC	

Table 7-7: TFT Connector Connections

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via an E1/E20 debugger. An E1 debugger is supplied with this RSK+ product.

For further information regarding the debugging capabilities of the E1/E20 debuggers, refer to the RX Family E1/E20 Emulator User's Manual (R20UT0398EJ).

8.2 Compiler Restrictions

The compiler supplied with this RSK+ is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 128k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

8.3 Mode Support

The MCU supports Single Chip, Boot and USB Boot modes, which are configured on the RSK+ board. Details of the modifications required can be found in §6. All other MCU operating modes are configured within the MCU's registers, which are listed in the RX63N Group, RX631 Group User's Manual: Hardware.

Only ever change the MCU operating mode whilst the RSK+ is in reset, or turned off; otherwise the MCU may become damaged as a result.

8.4 Debugging Support

The E1 emulator (as supplied with this RSK+) supports break points, event points (including mid-execution insertion) and basic trace functionality. It is limited to a maximum of 8 on-chip event points, 256 software breaks and 256 branch/cycle trace. For further details, refer RX Family E1/E20 Emulator User's Manual (R20UT0398EJ).

8.5 Address Space

Figure 8-1 below details the address space of MCU in its different operating modes. For further details, refer to the RX63N Group, RX631 Group User's Manual: Hardware.

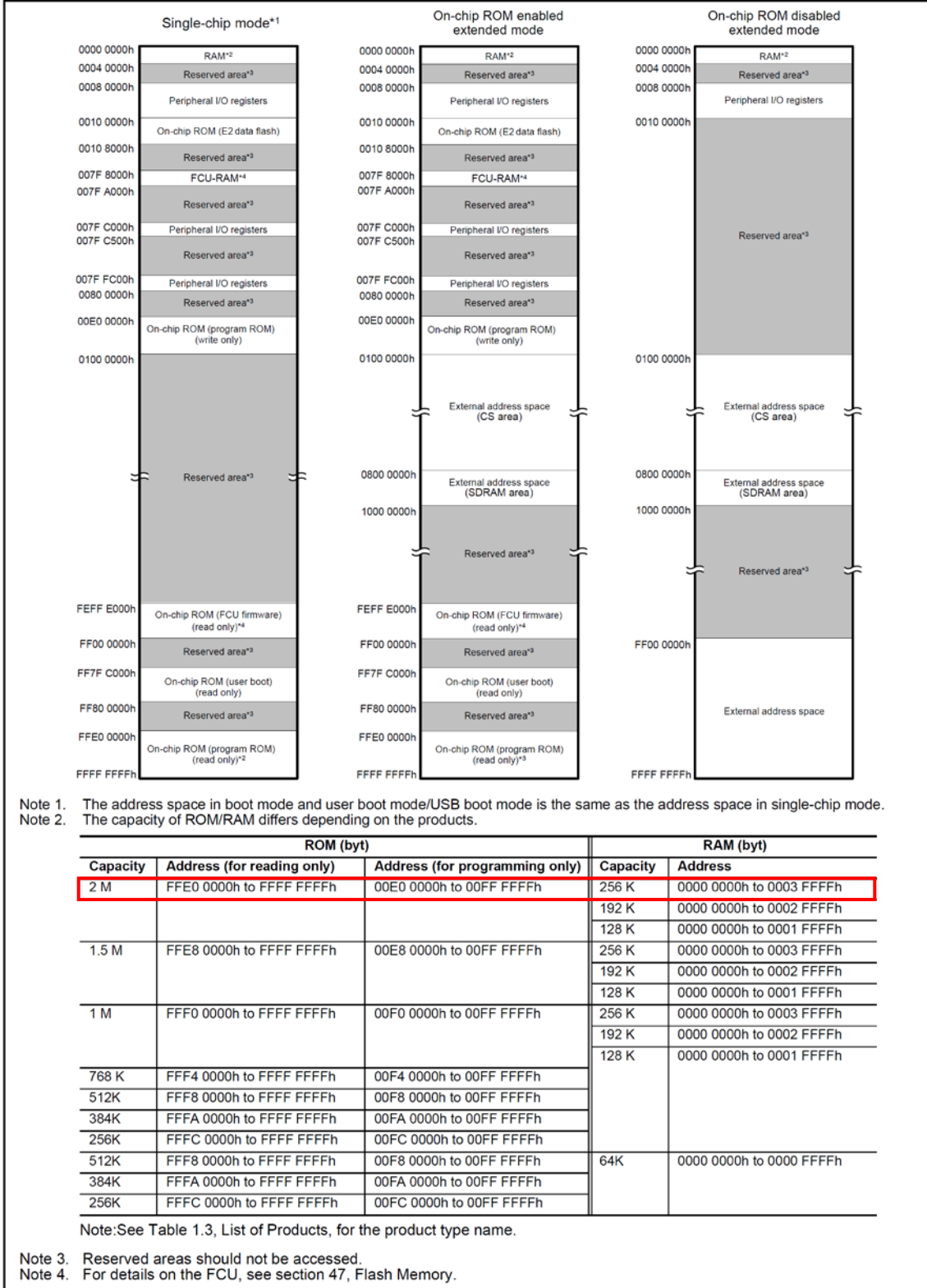
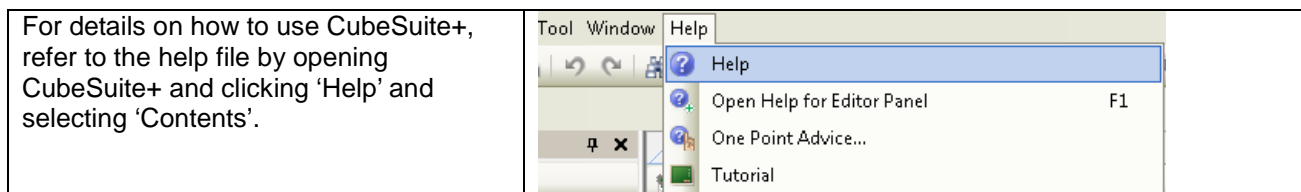


Figure 8-1: MCU Address Space Diagram

9. Additional Information



For details on how to use CubeSuite+, refer to the manual available on the DVD or from the web site.

For information about the RX63N Group microcontrollers refer to the RX63N Group, RX631 Group User's Manual: Hardware.

For information about the RX assembly language, refer to the RX Family Software Manual.

Online technical support and information is available at: <http://www.renesas.com/rskrx63n256k>

Technical Contact Details

Please refer to the “**Quick Start Guide**” for Renesas Technical contact details.

General information on Renesas Microcontrollers can be found on the Renesas website at: <http://www.renesas.com/>

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