

Contents

1	Introduction.....	2
2	Typical Application Schematic	3
3	Printed Circuit Board (PCB) Layout Guidelines	4
3.1.	PCB Layout Guidelines	5
3.1.1.	Placement of the ZSPM4023/ZSPM4022 and Connected Components.....	5
3.1.2.	Input Capacitor.....	6
3.1.3.	Inductor	6
3.1.4.	Output Capacitor.....	6
3.1.5.	Optional RC Snubber	6
4	Applied PCB Layout Design Methodology	7
4.1.	Example Layout.....	7
4.2.	Design Methodology for Minimizing Layout Effects on the Switching DC/DC Regulator.....	8
4.3.	Design Principle Examples Implemented in the ZSPM4023/ZSPM4022 Evaluation Board	10
4.4.	Implementation of the Optional RC Snubber.....	13
5	Recommended Bill of Materials	13
6	Related Documents.....	14
7	Glossary	15
8	Document Revision History	15

List of Figures

Figure 2.1	Application Schematic—Example using the ZSPM4023-12.....	3
Figure 3.1	Example of a ZSPM4023/ZSPM4022 Application Circuit Board Layout, Top and 2 nd Layers	4
Figure 3.2	Example of a ZSPM4023/ZSPM4022 Application Circuit Board Layout, 3 rd and Bottom Layers.....	5
Figure 4.1	Schematic ZSPM4023/ZSPM4022 Evaluation Kit Board	7
Figure 4.2	Evaluation Kit Board—Example showing ZSPM4023-12.....	8
Figure 4.3	Basic Principles of Switching Voltage/Voltage Regulators using ZSPM4023 as an Example	8
Figure 4.4	Current Loops using ZSPM4023 as an Example	9
Figure 4.5	Current Loop and Signal Analysis for the ZSPM4023/ZSPM4022 Evaluation Kit Board	11
Figure 4.6	Layout Design Methodology for the ZSPM4023/ZSPM4022 Evaluation Kit Board.....	12

List of Tables

Table 1.1	ZSPM4023/ZSPM4022 Product Variations	2
Table 5.1	External Component Requirements and Sources	13

1 Introduction

This application note covers layout guidelines and application details for the ZSPM4023/ZSPM4022 family of DC/DC synchronous switching regulators. Typical applications for the ZSPM4023/ZSPM4022 family include servers, workstations, routers, switches, telecom equipment, printers, and set-top boxes.

The ZSPM4023 and ZSPM4022 provide fully integrated power switches, internal compensation, and full fault protection for a broad range of applications. Depending on the product version, the output can support load currents of 6A, 9A, or 12A. This application note covers all product versions listed in Table 1.1, unless noted in the text. It uses the ZSPM4023-12 for examples.

Table 1.1 ZSPM4023/ZSPM4022 Product Variations

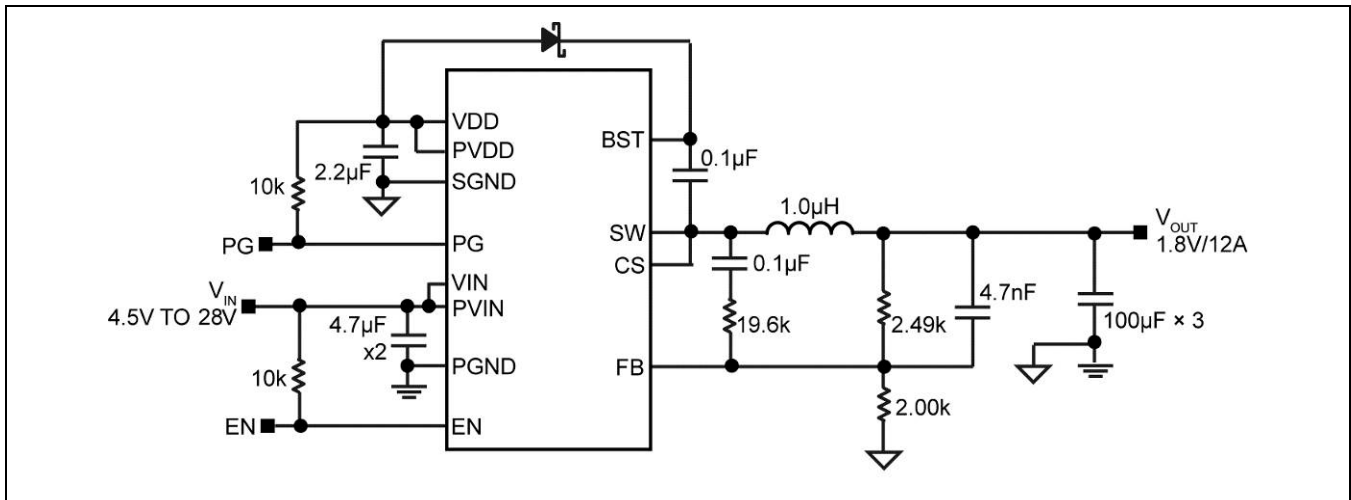
Product	Input Supply Range to be Regulated	Regulated Output Current	Output Voltage Adjustment Range (Typical Accuracy $\pm 1\%$)
ZSPM4023-12	4.5V to 28V	12A	0.8V to 5.5V
ZSPM4023-09	4.5V to 28V	9A	0.8V to 5.5V
ZSPM4023-06	4.5V to 28V	6A	0.8V to 5.5V
ZSPM4022-12	4.5V to 19V	12A	0.8V to 5.5V
ZSPM4022-09	4.5V to 19V	9A	0.8V to 5.5V
ZSPM4022-06	4.5V to 19V	6A	0.8V to 5.5V

2 Typical Application Schematic

The typical application circuit for the ZSPM4023/ZSPM4022 includes bypass capacitors on the VDD input pin, a resistive voltage divider to set the voltage on the FB feedback pin, a bootstrap capacitor on the BST pin, an output inductor, and output filtering capacitors. (See Figure 2.1.)

See the data sheet for the ZSPM4023/ZSPM4022 product version for additional requirements/recommendations for external components.

Figure 2.1 Application Schematic—Example using the ZSPM4023-12



3 Printed Circuit Board (PCB) Layout Guidelines

For proper operation and minimum EMI, care must be taken during PCB layout. An improper layout can lead to issues such as poor stability and regulation, noise sensitivity, and increased EMI radiation.

Figure 3.1 and Figure 3.2 provide an example of a proper layout for the ZSPM4023/ZSPM4022 using IDT's ZSPM4023/ZSPM4022 Evaluation Kit Board.

Figure 3.1 Example of a ZSPM4023/ZSPM4022 Application Circuit Board Layout, Top and 2nd Layers

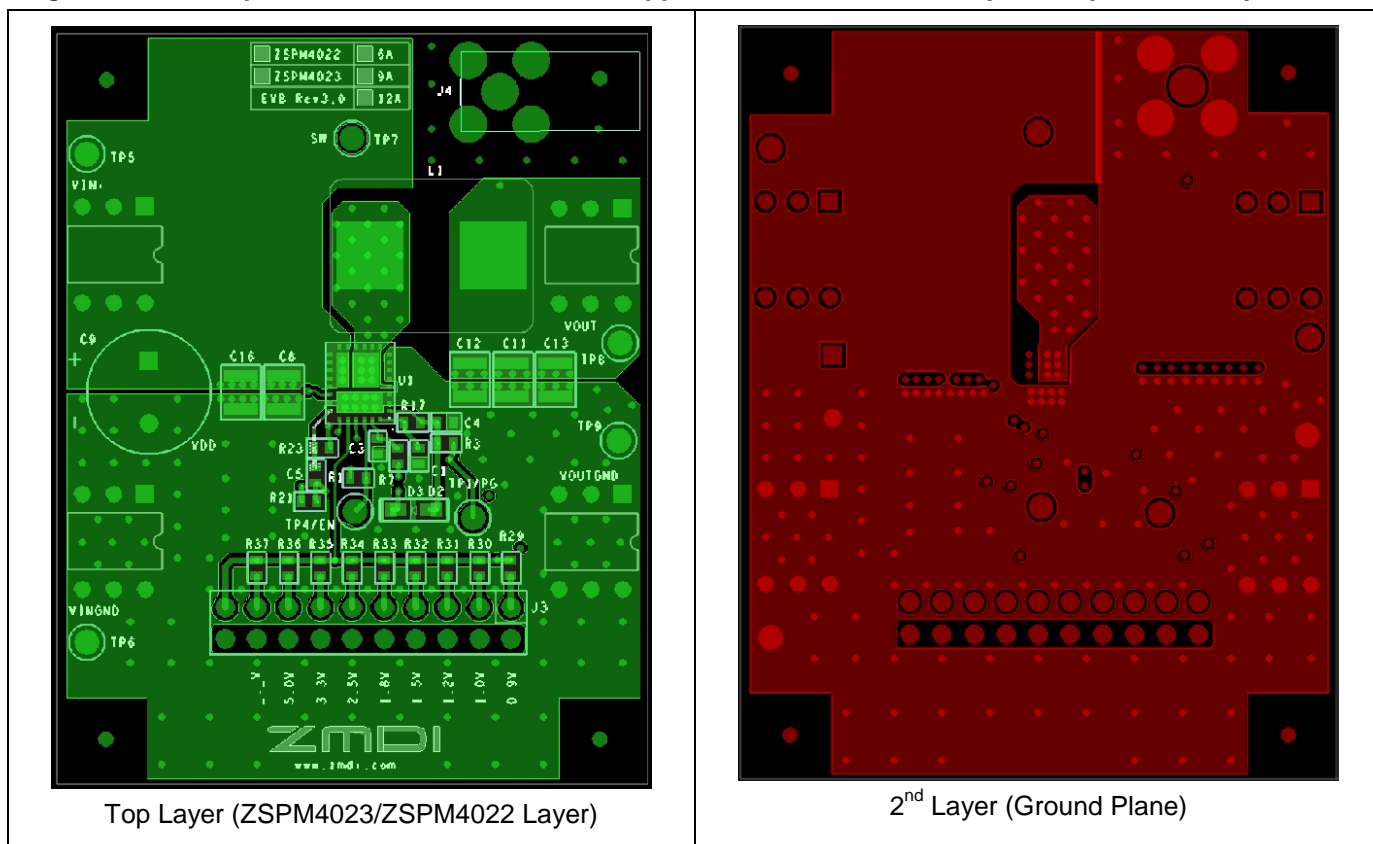
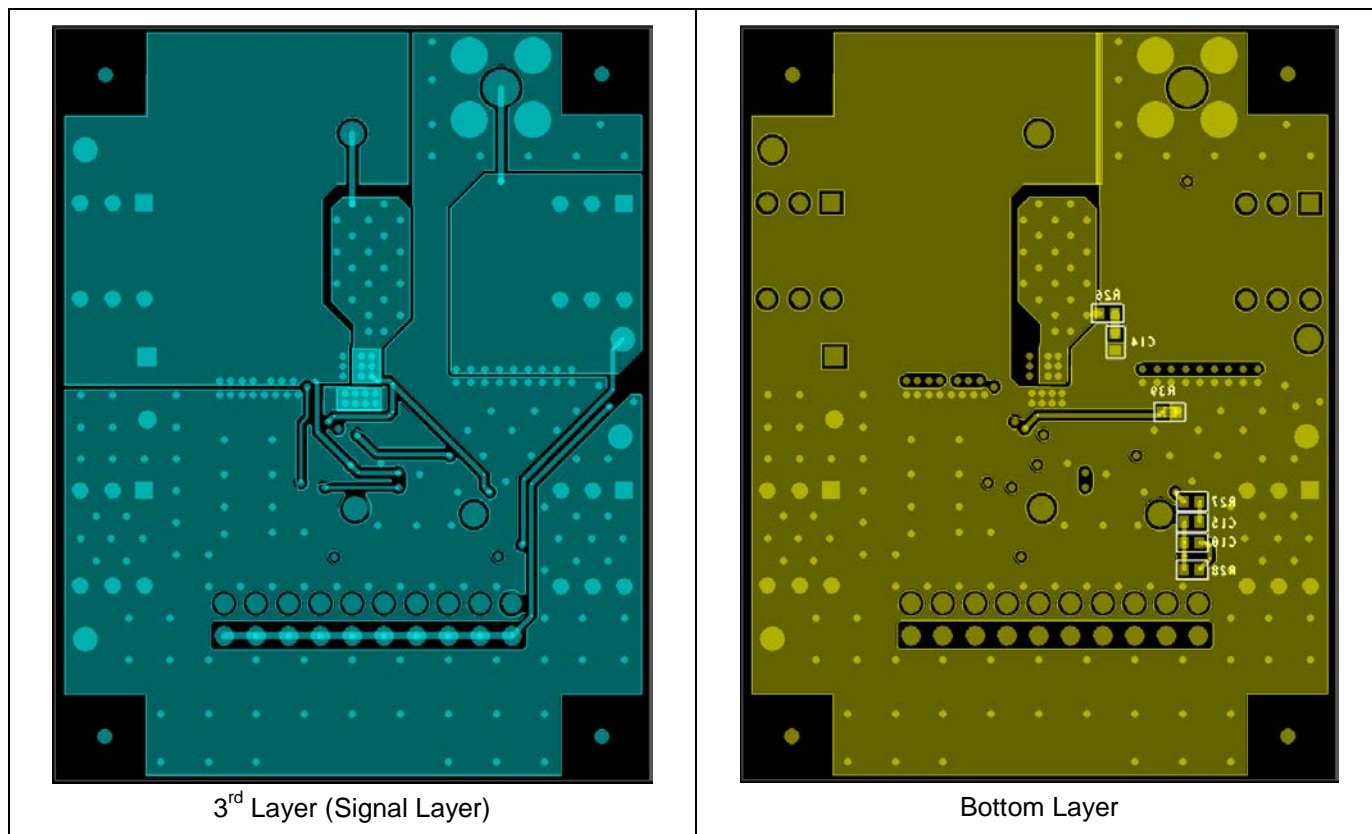


Figure 3.2 Example of a ZSPM4023/ZSPM4022 Application Circuit Board Layout, 3rd and Bottom Layers



3.1. PCB Layout Guidelines

Important warning: To minimize EMI and output noise, follow these layout recommendations.

Proper PCB layout is critical to achieving reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to ensure proper operation of the ZSPM4023/ZSPM4022 regulator.

3.1.1. Placement of the ZSPM4023/ZSPM4022 and Connected Components

- Connect a 2.2 μ F ceramic capacitor across the PVDD and PGND pins of the ZSPM4023/ZSPM4022 as close as possible to the IC. The PVDD pin typically emits relatively strong noise, and therefore the placement of the capacitor is critical. Use wide traces to connect the capacitor to the PVDD and PGND pins.
- Recommendation: Connect a 1.2 Ω resistor between the PVDD pin (bootstrapped power supply for the high-side switch) and the VDD pin. If this resistor is implemented, a 1.0 μ F ceramic capacitor must be placed immediately between the VDD pin and the signal ground pin SGND. Together the resistor and capacitor provide decoupling for PGND and SGND.

Note: The SGND must not be connected directly to the ground planes. Do not route the SGND pin to the PGND pad; instead connect SGND to the ground terminal of the output caps.

- Place the ZSPM4023/ZSPM4022 close to the point-of-load (POL).

- Use wide traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

3.1.2. Input Capacitor

- Place the input capacitors on the same side of the board as close to the ZSPM4023/ZSPM4022 as possible.
- Connect the input capacitors to the PVIN and PGND pins with traces that are as short as possible.
- Connect the ground terminals for the input capacitors to the ground plane using several vias placed as close to the terminals as possible.
- Use input capacitors with a dielectric that is either X7R or X5R. Do not use Y5V or Z5U type capacitors.
- Ensure that two of the input capacitors are parallel ceramic low-ESR MLCC 4.7 μ F capacitors. If needed, any type of capacitor can be placed in parallel with these input capacitors.
- In “Hot-Plug” applications, an additional tantalum or electrolytic bypass capacitor must be used in parallel with the low-ESR MLCC input capacitor(s) to limit the over-voltage spike seen on the input supply if power is suddenly applied.
- If a tantalum input capacitor is placed in parallel with the input capacitor, the tantalum capacitor must be recommended for switching regulator applications (low ESR) and its operating voltage must be de-rated by 50%.

3.1.3. Inductor

- Ensure that the inductor connection to the switch node (SW pin on the ZSPM4023/ZSPM4022) is short.
- Do not route any sensitive signal lines underneath or close to the inductor.
- Place the switch node (SW) traces away from the feedback (FB) pin on the ZSPM4023/ZSPM4022.
- The CS pin should be connected directly to the SW pins to ensure accurate sensing of the voltage across the low-side MOSFET.
- Do not place any ground area under the inductor because this might bridge the reference points of sensitive analog signals. The inductor might introduce an unwanted secondary voltage in the ground area due to eddy currents.
- Option: The inductor can be placed on the opposite side of the application circuit board with respect to the ZSPM4023/ZSPM4022. It does not matter whether the IC or the inductor is on the top or bottom as long as there is enough airflow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the ZSPM4023/ZSPM4022.

3.1.4. Output Capacitor

- Connect the ground terminals for the output capacitors to the ground plane using several vias placed as close to the terminals as possible.
- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Note that the output capacitor value and its ESR affect the phase margin.
- The feedback trace should be placed with a wide separation from the power trace and connected as close as possible to the output capacitor. Sensing a long, high-current load trace can degrade the DC load regulation.

3.1.5. Optional RC Snubber

- If the circuit includes an RC snubber, place it on either side of the board as close to the SW pin as possible.

4 Applied PCB Layout Design Methodology

4.1. Example Layout

The IDT's ZSPM4023/ZSPM4022 Evaluation Kit Board follows the design methodology presented in this application note. The schematic of the Evaluation Board is shown in Figure 4.1 below. An illustration of the Evaluation Board with bold white text highlighting key components is provided in Figure 4.2.

Figure 4.1 Schematic ZSPM4023/ZSPM4022 Evaluation Kit Board

Note: U1 is the ZSPM4023 or ZSPM4022.

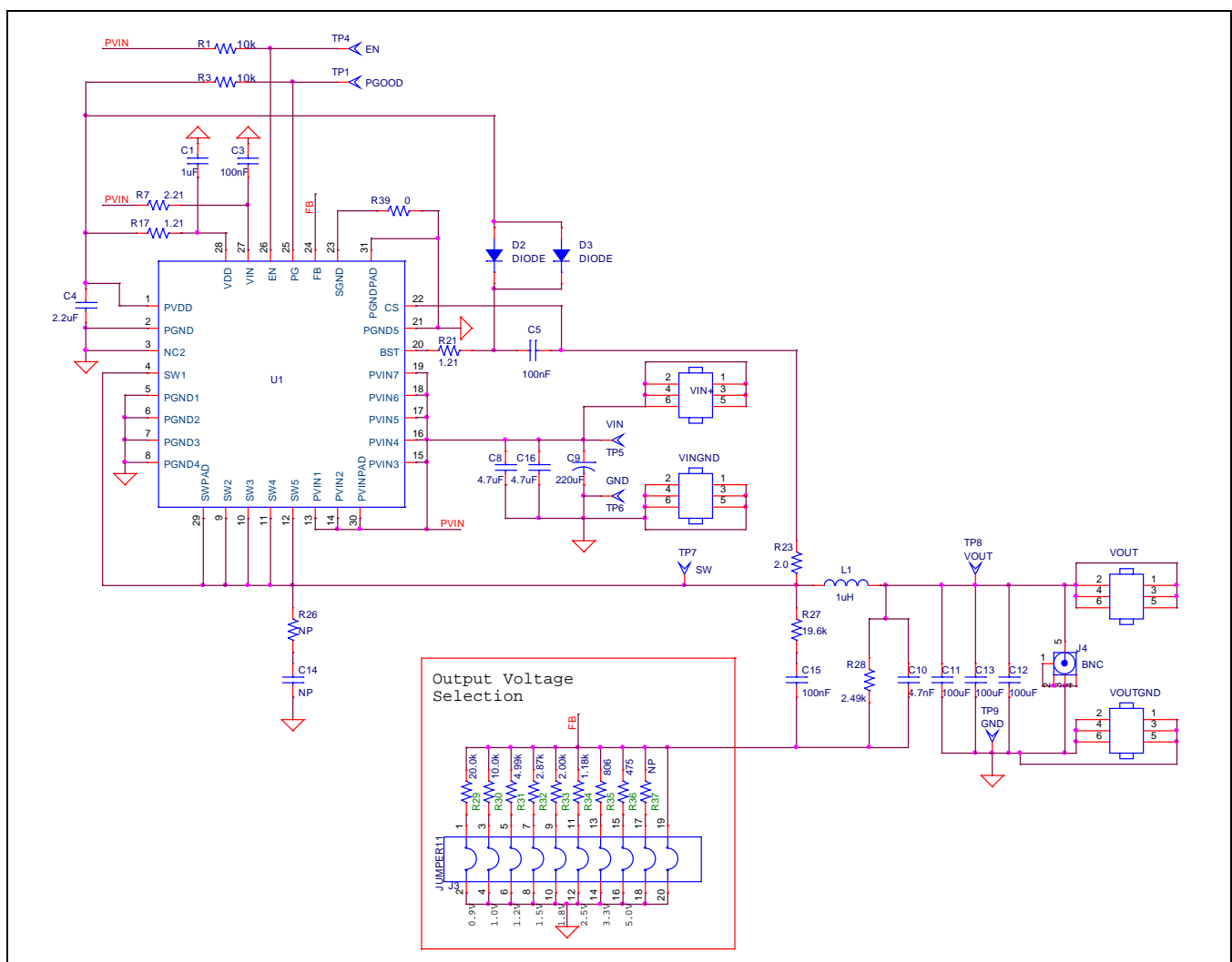
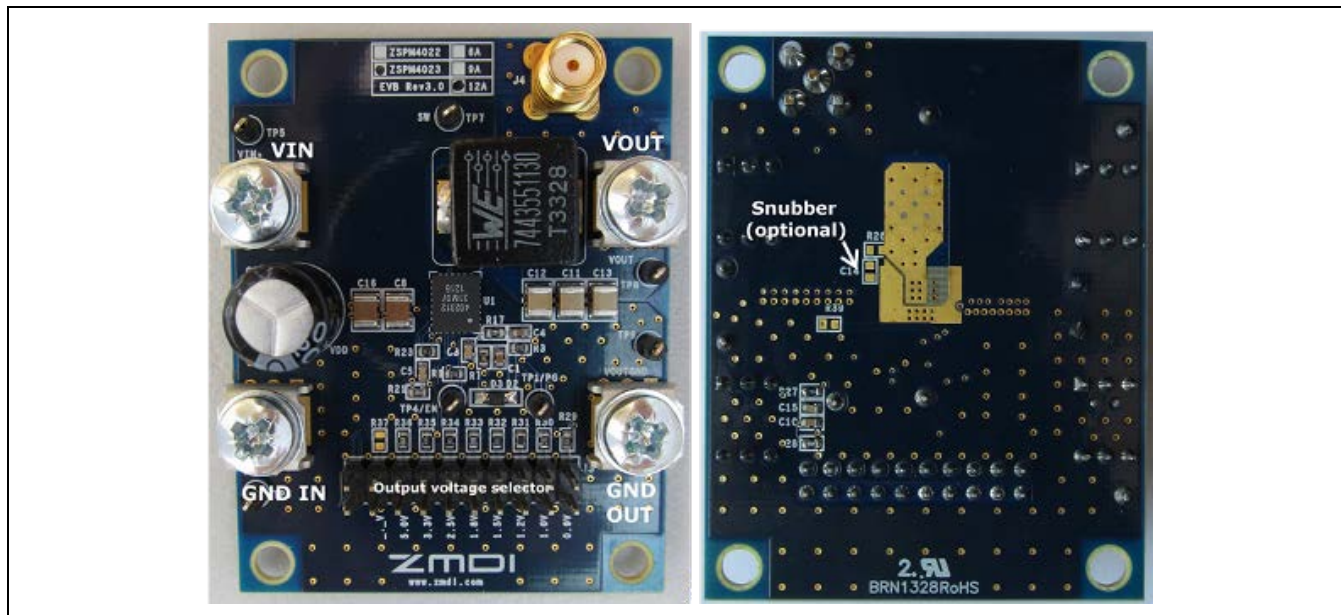


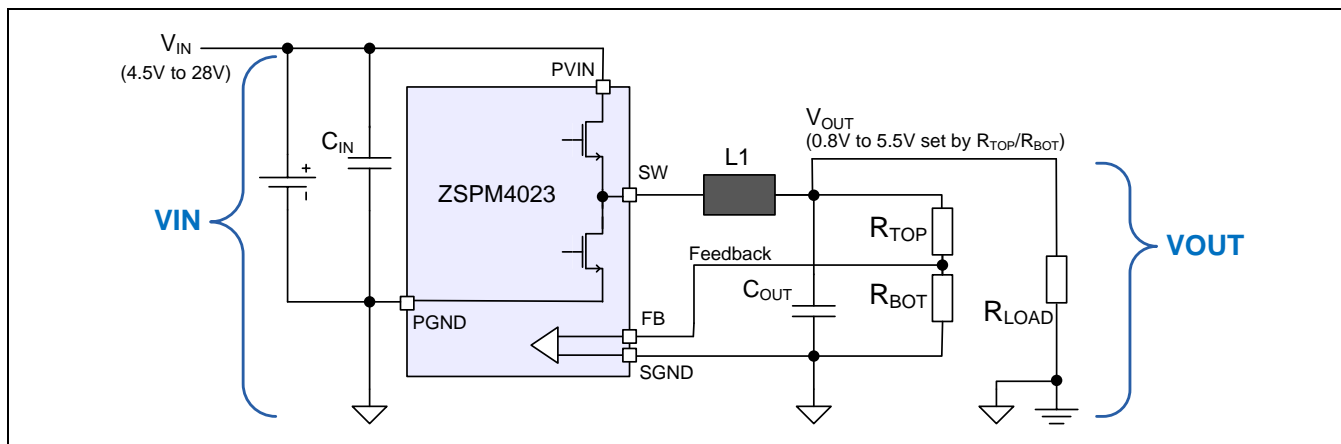
Figure 4.2 Evaluation Kit Board—Example showing ZSPM4023-12



4.2. Design Methodology for Minimizing Layout Effects on the Switching DC/DC Regulator

The ZSPM4023/ZSPM4022 is the central component of the switching voltage regulator (DC/DC converter) circuit shown in Figure 4.3. The ZSPM4023/ZSPM4022 can be considered as a high-side switch between the pins PVIN and SW (switch node connected to inductor), and as a low-side switch between SW and ground. Both switches are controlled by a regulator circuit that compares the output voltage with an internal reference voltage. This principle is illustrated in Figure 4.3.

Figure 4.3 Basic Principles of Switching Voltage/Voltage Regulators using ZSPM4023 as an Example

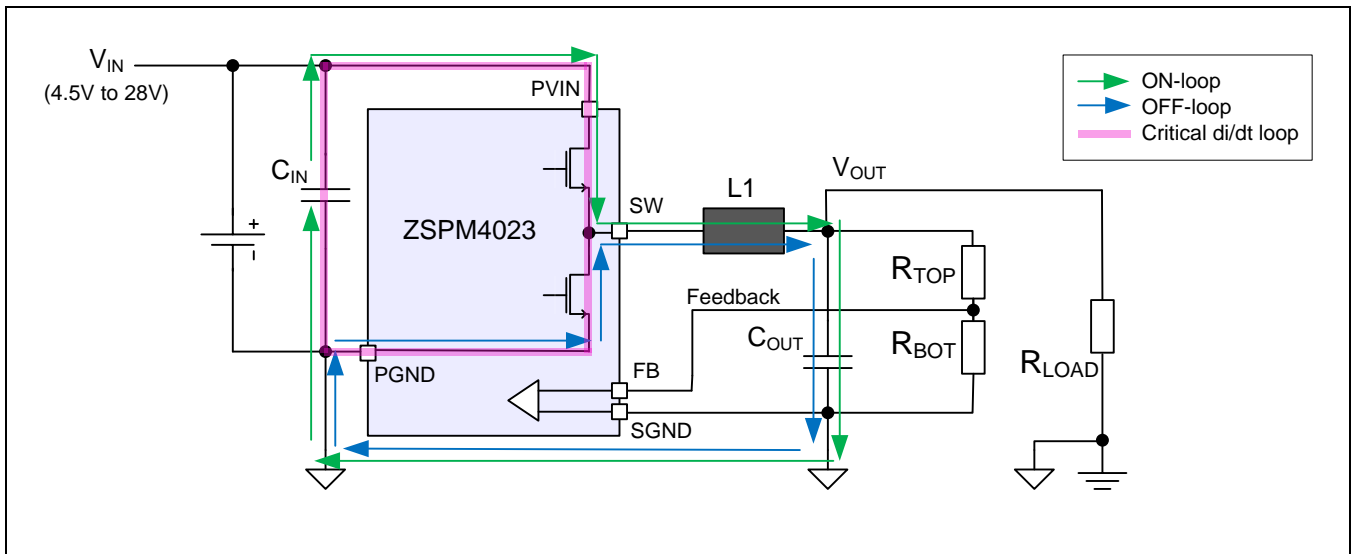


Several properties of switching converters, for instance EMC/EMI and energy efficiency, can be influenced by a proper PCB layout. It is crucial that high-frequency current loops and noise sensitive signals are taken into consideration when designing the PCB.

There are two time periods for which the current flow must be analyzed as diagrammed in Figure 4.4.

- ON-loop: The period when the power is taken from the external energy source and stored in the inductor or consumed at the external load (Figure 4.4 – current loop marked **green**).
- OFF-loop: The period when the energy is taken from the inductor to be consumed at the external load (Figure 4.4 – current loop marked **blue**).

Figure 4.4 Current Loops using ZSPM4023 as an Example



The branches in the application circuit that are exclusively affected by the current of either the ON-loop or the OFF-loop (Figure 4.4: marked with either **green** or **blue**; i.e., not marked with both colors) perform the critical di/dt loop. The PCB layout concerning this critical di/dt loop is crucial due to its effect on the EMI properties of the application circuit.

The basic objective for the PCB layout design is to optimize the EMC/EMI and energy efficiency properties of the application circuit. In this combination, the high-frequency impedance of the ON-loop and OFF-loop and consequently of the critical di/dt loop must be minimized using the following practicable layout design rules.

LAYOUT RULE: The impedance of each of three current loops can be minimized by reducing the loop-enclosed area on the PCB. This can be achieved by applying a specific order in designing the placement and routing of the PCB components; e.g., begin with $C_{in} \rightarrow$ ZSPM4023/ZSPM4022 (minimize critical di/dt loop) $\rightarrow C_{out}$ (minimize the ground path of both the ON-loop and the OFF-loop) $\rightarrow L1$ (minimize ON-loop and the OFF-loop).

Note: A folded loop (a “figure-8” loop) is advantageous since certain components of the magnetic field may compensate themselves.

After optimization of the high frequency current loops, the output voltage measurement (feedback/FB pin voltage) must be considered. This measurement must ensure an accurate determination of the output voltage as well as avoiding any interference by noise that is emitted by the switching regulator (di/dt loop and electrical node related to the SW pin are critical). Recommendation: use shielded wires between the FB pin and the voltage divider, and between the SGND pin and the ground terminals of the Cout capacitors.

Moreover, the voltage feedback must not be affected by voltage drops due to high currents on the same wire used for the output voltage measurement. Therefore, using the following “sense wire” principle is recommended.

LAYOUT RULE: Route the voltage feedback tracks away from the critical di/dt loop (magnetic field coupling) and away from the electrical node related to the SW pin (electrical and magnetic field coupling). Use shielded sense wires.

4.3. Design Principle Examples Implemented in the ZSPM4023/ZSPM4022 Evaluation Board

The design methodology discussed in section 4.2 was applied for the design of IDT’s ZSPM4023/ZSPM4022 Evaluation Kit Board. The current loop analysis of this application circuit reveals the path of the current loops as illustrated in Figure 4.5.

The next step was the optimization of the current loops. For the ZSPM4023/ZSPM4022 Evaluation Kit Board, the bypass capacitors C8 and C16 were placed as close as possible to the ZSPM4023/ZSPM4022 in order minimize the ON-loop. This also minimized the area of the critical loop.

Since input bypass capacitors C8, C16, and C9 are important in order to minimize conducted noise on the input lines and since the regulator takes the energy from those capacitors primarily when activating the ON-loop, a low ESR associated with those capacitors is important. The ZSPM4023/ZSPM4022 Evaluation Kit Board design supports this with a built-in PCB stack-up capacitor located in the left upper corner of the PCB as illustrated in Figure 4.6.

The optimization of the OFF-loop is done with the placement and routing of the inductor L1 and the output bypass capacitors C11, C12, and C13. The ESR of those capacitors significantly influences the noise on the output voltage. Another PCB stack-up capacitor has been implemented for this purpose in the right upper corner of the PCB as illustrated in Figure 4.6.

Finally, the PCB layout design must deal with the signals for the voltage feedback. The ZSPM4023/ZSPM4022 Evaluation Kit Board uses carefully routed sense lines with ground shielding on the left and right of the traces and ground shielding in the layer above and underneath the layer used for the voltage feedback signal.

Important: Do not connect the ZSPM4023/ZSPM4022’s signal ground pin SGND to commonly used ground areas or the ground plane. Provide a separate sense wire to the output bypass capacitors.

Figure 4.5 Current Loop and Signal Analysis for the ZSPM4023/ZSPM4022 Evaluation Kit Board

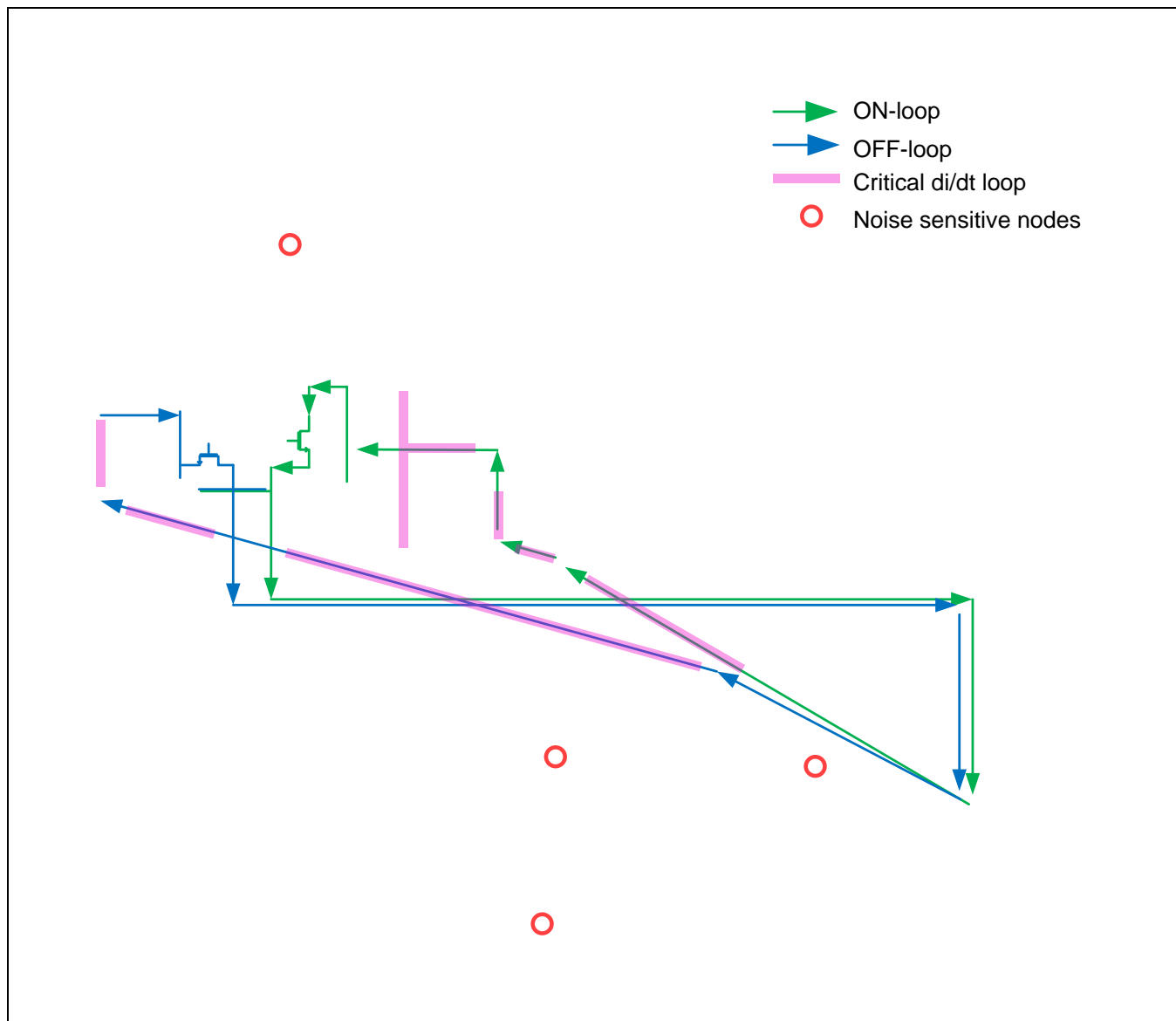
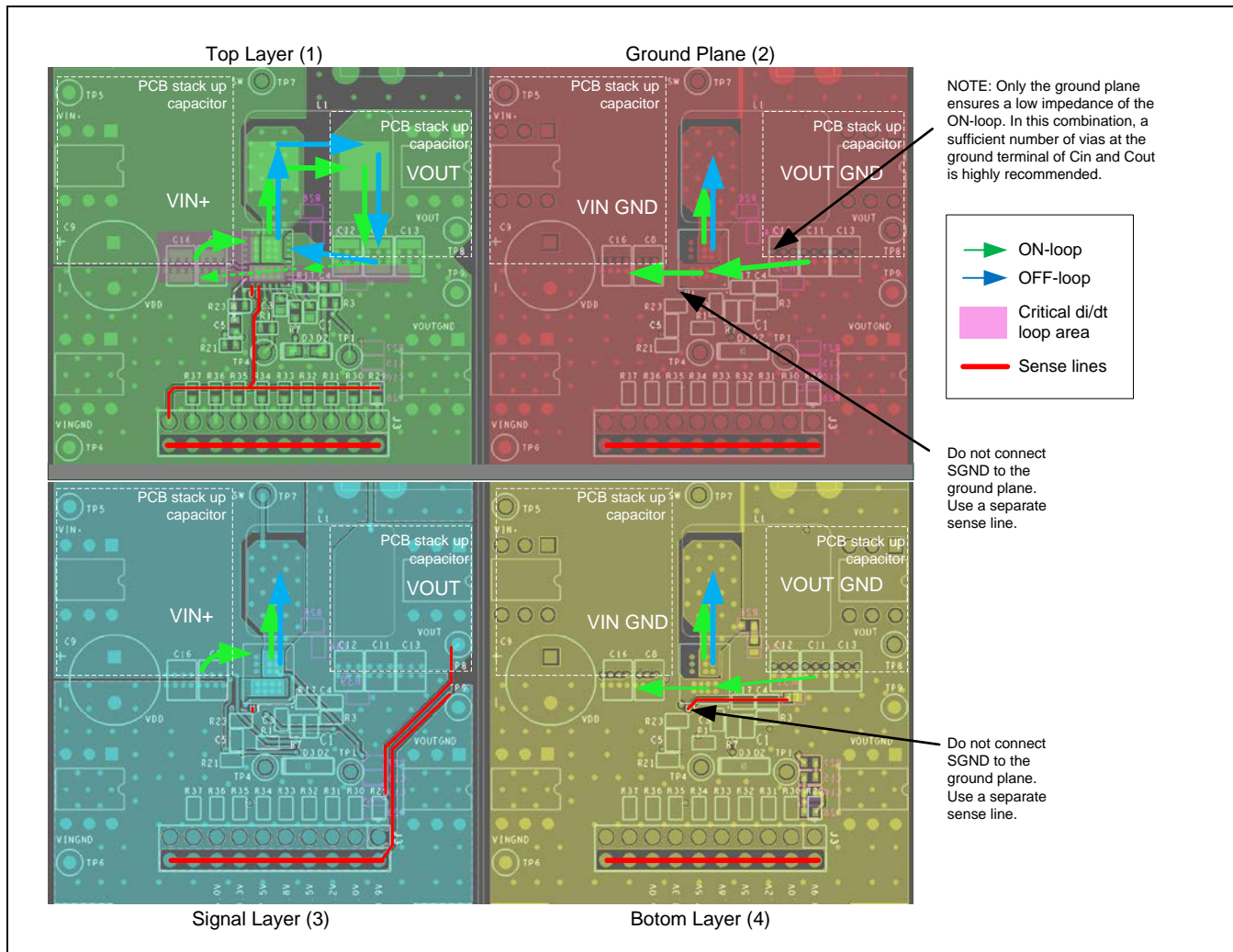


Figure 4.6 Layout Design Methodology for the ZSPM4023/ZSPM4022 Evaluation Kit Board



4.4. Implementation of the Optional RC Snubber

For further optimization of the EMC/EMI behavior, an RC snubber network (R26 and C14 on the ZSPM4023/ ZSPM4022 Evaluation Kit Board) can be added on the bottom side of the PCB (refer to Figure 4.2). The objective is to dampen any parasitic LC resonators that cause ringing in the waveform of the SW pin signal. This provides damping by putting a resistor in “parallel” with the oscillating circuit. The value of this snubber resistor should be approximately equal to the impedance of the resonance circuit at the target ringing frequency. At this frequency, the value of the snubber capacitors should be only a tenth of the impedance of the resonance circuit. With respect to the ZSPM4023/ ZSPM4022 Evaluation Kit Board, a combination of a 22Ω resistor and a 330pF capacitor reduce noise in the frequency range of 50MHz to 200MHz.

Generally recommended R26/C14 values are 10Ω/1nF to 33Ω/220pF.

Note: The RC snubber is not indented to reduce noise that is related to the operating frequency of the DC/DC regulator and its next harmonics. In order to overcome this noise, additional input and output filters are required. The design of those filters must be done according to the guidelines of the filter manufacturer.

5 Recommended Bill of Materials

Table 5.1 External Component Requirements and Sources

Item	Manufacturer Part Number	Manufacturer	Description	Quantity
C16, C8	C1210C475K5RACTU	Kemet	CAP CER 4.7UF 50V 10% X7R 1210	2
C11, C12, C13	C1210C107M9PACTU	Kemet	CAP CER 100UF 6.3V 20% X5R 1210	3
C3, C5, C15	C1608X7R1H104K080AA	TDK	CAP CER 0.1UF 50V 10% X7R 0603	3
C1	LMK107B7105KA-T	Taiyo Yuden	CAP CER 1UF 10V 10% X7R 0603	1
C4	CC0603KRX5R6BB225	Yageo	CAP CER 2.2UF 10V 10% X5R 0603	1
C14	Not placed		Open	1
C10	GRM188R71H472MA01D	Murata	CAP CER 4700PF 50V 20% X7R 0603	1
C9	ESC227M035AH1AA	Kemet	CAP ALUM 220UF 35V 20% RADIAL	1
D3	SD103AWS-7-F	Diodes Inc	DIODE SCHOTTKY 40V 350MA SOD323	1
J3	802-10-010-10-002000	Mill-Max	20 POS 2.54mm Solder ST Thru-Hole	1
J4	C02AN30P00101	Wellshow	CONN JACK SMA PCB VERT	1
L1	7443551130	WURTH	INDUCTOR, HCI 1365, 1.3UH 20% 25A	1
R7	RMCF0603FT2R21	Stackpole	RES TF 2.21 OHM 1% 0.1W 0603	1
R23	CRCW06032R00JNEA	Vishay Dale	RES 2.0 OHM 1/10W 5% 0603 SMD	1
R27	RMCF0603FT19K6	Stackpole	RES 19.6K OHM 1/10W 1% 0603 SMD	1
R28	RMCF0603FT2K49	Stackpole	RES 2.49K OHM 1/10W 1% 0603 SMD	1
R29	RMCF0603JT20K0	Stackpole	RES 20K OHM 1/10W 5% 0603 SMD	1
R1, R3, R30	RNCP0603FTD10K0	Stackpole	RES 10K OHM 1/8W 1% 0603 SMD	3

Item	Manufacturer Part Number	Manufacturer	Description	Quantity
R31	RMCF0603FT4K99	Stackpole	RES 4.99K OHM 1/10W 1% 0603 SMD	1
R32	RMCF0603FT2K87	Stackpole	RES 2.87K OHM 1/10W 1% 0603 SMD	1
R33	RMCF0603FT2K00	Stackpole	RES 2K OHM 1/10W 1% 0603 SMD	1
R34	CRCW06031K18FKEA	Vishay Dale	RES 1.18K OHM 1/10W 1% 0603 SMD	1
R35	RMCF0603FT806R	Stackpole	RES 806 OHM 1/10W 1% 0603 SMD	1
R36	RMCF0603FT475R	Stackpole	RES 475 OHM 1/10W 1% 0603 SMD	1
R37	Not placed		Open	
R39			short connection	1
R17, R21	RMCF0603FT1R21	Stackpole	RES TF 1.21 OHM 1% 0.1W 0603	2
R26	Not placed		Open	1
TP1, TP4, TP5, TP6, TP7, TP8,TP9,	5001	Keystone	TEST POINT PC MINI .040"D BLACK	7
VIN, VINGND, VOUT, VOUTGND	214788	ERNI	PowerTab_ERNI_M4-6pin	4
U1	ZSPM4023/ZSPM4022	IDT	Synchronous Buck DC-DC Regulator	1

6 Related Documents

Document
<i>ZSPM4022-06 Data Sheet</i>
<i>ZSPM4022-09 Data Sheet</i>
<i>ZSPM4022-12 Data Sheet</i>
<i>ZSPM4023-06 Data Sheet</i>
<i>ZSPM4023-09 Data Sheet</i>
<i>ZSPM4023-12 Data Sheet</i>

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

7 Glossary

Term	Description
BST	Bootstrap
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FB	Feedback
MLCC	Multilayer Ceramic Chip Capacitors
PCB	Printed Circuit Board

8 Document Revision History

Revision	Date	Description
1.00	October 4, 2013	First release.
	April 12, 2016	Changed to IDT branding.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.