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# SH7751 E10A Emulation Memory Board (HS7751EJH01H) User's Manual

Renesas Electronics

Rev.1.0 2002.09

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• READ this user's manual before using this emulation memory board.

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Do not attempt to use the emulation memory board until you fully understand its mechanism.

#### **Emulation Memory Board:**

Throughout this document, the term "emulation memory board" shall be defined as the following products produced only by Hitachi, Ltd. excluding all subsidiary products.

- Emulation memory board
- · Power cables supplied together with this emulation memory board

The user system or a host computer is not included in this definition.

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#### Figures:

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#### Limited Anticipation of Danger:

Hitachi cannot anticipate every possible circumstance that might involve a potential hazard. The warnings in this user's manual and on the emulation memory board are therefore not all inclusive. Therefore, you must use the emulation memory board safely at your own risk.

### **SAFETY PAGE**

### **READ FIRST**

- READ this user's manual before using this emulation memory board.
- KEEP the user's manual handy for future reference.

Do not attempt to use the emulation memory board until you fully understand its mechanism.

### **DEFINITION OF SIGNAL WORDS**



This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.



**DANGER** indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.



**WARNING** indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.



**CAUTION** indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury.



**CAUTION** used without the safety alert symbol indicates a potentially hazardous situation which, if not avoided, may result in property damage.

NOTE emphasizes essential information.

# **WARNING**

Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system, the emulation memory board, and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

- 1. Do not repair or remodel the emulation memory board by yourself for electric shock prevention and quality assurance.
- 2. Always switch OFF the emulator product, the emulation memory board, and the user system before connecting or disconnecting any CABLES or JUMPERS.
- 3. Always switch OFF the emulation memory board and the user system before connecting or disconnecting the IC socket or the user system interface connector.
- 4. When connecting the user system interface connector to the IC socket on the user system, ensure that pin 1 on both sides are correctly aligned.
- 5. Supply power according to the power specifications and do not supply an incorrect power voltage. Use only the provided power cables.

## Warnings on Emulation Memory Board Usage

Be sure to read and understand the warnings below before using this emulation memory board. Note that these are the main warnings, not a complete list.

# WARNING

Always switch OFF the emulator product, the emulation memory board, and the user system before connecting or disconnecting any CABLES, JUMPERS, or PARTS. Failure to do so will result in a FIRE HAZARD and will damage the emulator product, the emulation memory board, or the user system, or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

## CAUTION

Position the emulator product, the emulation memory board, and the user system so that no cable is bent or twisted. A bent or twisted cable will impose stress on the user system interface leading to connection or contact failure. Make sure that the emulation memory board is placed in a secure position so that it does not move during use nor impose stress on the user system interface.

### Preface

Thank you for purchasing the SH7751 E10A emulation memory board. The emulation memory board supports the development of systems using Hitachi microcomputer SH7751.

Read this user's manual before using the emulation memory board, and keep the manual handy for future reference.

# CAUTION

READ this user's manual before using the emulation memory board. Incorrect operation or connection will damage the emulation memory board and the user system. The USER PROGRAM will be LOST.

#### **Related Manuals:**

- SH7751 Hardware Manual
- SH7751 E10A Emulator User's Manual

Related Hardware: SH7751 E10A Emulators

- HS7751KCM01H
- HS7751KCM02H
- HS7751KCI01H
- HS7751KCI02H

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### Section 1 Overview

The SH7751 E10A emulation memory board (hereinafter referred to as the emulation memory board) has an SH7751 (hereafter referred to as the MCU), interface connectors (H-UDI port connectors) for the E10A emulator (hereinafter called the emulator), a user system interface connector, and SRAM devices. User programs can be emulated by connecting this emulation memory board to the emulator.

#### 1.1 Features

- The emulation memory board has emulator connectors and a user system interface connector (YQPACK256SE). When the user system has an IC socket (NQPACK256SE) but has no H-UDI connector, the user system can be connected to the emulator through the emulation memory board and the user program can be emulated.
- 2. The emulation memory board has SRAM devices that can be used as a substitute for the flash memory or EPROM devices. User programs can be emulated by connecting the emulation memory board to the emulator and supplying external power to the emulation memory board, even when no user system is connected to the emulator.
- 3. The emulation memory board has switches for various settings. These switches can select (1) the source of the power supplied to the emulation memory board,
  - (2) the source of the clock supplied to the MCU on the emulation memory board, and
  - (3) the destination of the CS0 signal output from the MCU.
- 4. The emulation memory board has a DIP switch, which can set the MCU's MD terminal status.

#### 1.2 Components

Figure 1.1 and table 1.1 show the components of the emulation memory board. Please make sure you have all of these components when unpacking.

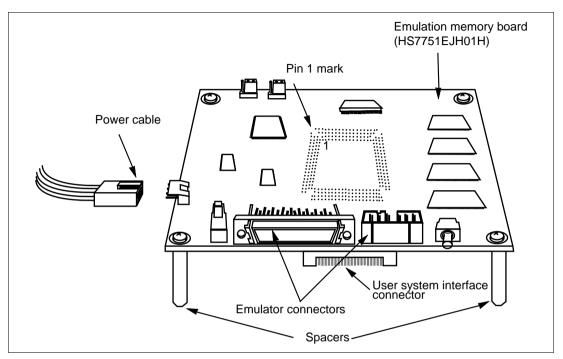


Figure 1.1 Emulation Memory Board Appearance

#### Table 1.1 Emulation Memory Board Components (HS7751EJH01H)

Item	Quantity	Notes
Emulation memory board	1	
Power cables (2 cables for 5 V and 2 cables for GND)	1 set	For an external power supply
Screws (M2 x 10 mm)	4	For fastening user system interface connector
NQPACK256SE	1	Connector for interfacing with the user system
Guide pins for NQPACK256SE	3	For determining the connector location
Screwdriver	1	For tightening screws
Spacers (13 mm)	4	Fixed to the emulation memory board
SH7751 E10A Emulation Memory Board User's Manual	1	This manual

# CAUTION

READ the following warnings before using the emulation memory board. Incorrect operation will damage the emulation memory board, the user system, and the emulator product. The USER PROGRAM will be LOST.

- 1. Cover the emulation memory board with a casing before using it. If using the emulation memory board without a casing, do not touch any component and prevent any short circuit.
- 2. Never place heavy objects on the emulation memory board.
- 3. Protect the emulation memory board from excessive impacts and stresses.
- 4. Do not supply power outside the specified voltage range.
- 5. When moving the emulation memory board, take care not to vibrate or damage it.
- 6. Supply power to the connected equipment only after connecting all cables. Cables must not be connected or removed while the power is on.
- 7. The emulation memory board may operate incorrectly due to static electricity. In this case, connect the GND patterns (the spacer-fixed sections at the four corners) on the emulation memory board to those of the user system through cables to discharge static electricity.
- 8. The emulation memory board can operate only when connected to the emulator; the emulation memory board cannot be used alone or only by connecting to the user system.

### Section 3 Emulation Memory Board Functions

The functions of the emulation memory board are listed in table 3.1.

Function	Specifications
Clock	• الأر(CPU clock) = 167 MHz (max.)
	Clock installed in this emulation memory board: 27.8 MHz (EXTAL input)
Substitution	Capacity: 4 Mbytes (8 blocks of 256 kwords x 16 bits)
emulation memory	<ul> <li>83 MHz (max.) = B (bus clock): Two wait cycles inserted by WCR2</li> </ul>
	<ul> <li>Can be allocated to the CS0 area (Substitution memory area: H'00000000 to H'003FFFFF)</li> </ul>
	<ul> <li>Data bus width can be selected from 16 or 32 bits (8-bit width is not supported)</li> </ul>
User interface	Supported package: 256 pin QFP
Crystal oscillator	Supported frequency for crystal oscillation: 9 MHz to 20 MHz
Switch settings	SW3: Selects the power source
	JP1: Selects the clock source
	JP2: Selects the CS0 signal output destination
DIP switch settings	SW2-1 to SW2-3: Selects the clock operating mode
	<ul> <li>SW2-4, SW2-5, and SW2-7: Selects the memory type and bus width for area 0</li> </ul>
	SW2-6: Selects the endian
	SW2-8: Selects the master or slave mode
	SW2-9: Selects the clock source
	<ul> <li>SW2-0: Selects whether or not to write-protect the substitution emulation memory</li> </ul>
RESET switch	SW1: Issues a RESET signal
LEDs	LED1: RESET and POWER
	LED2: RDY and U-RUN
	LED3: BREQ and NMI
	<ul> <li>LED4: STATUS1 and STATUS0</li> </ul>

 Table 3.1
 Emulation Memory Board Functions

Function	Specifications
Power supply	<ul> <li>The emulation memory board can operate without connecting the user system by supplying +5 V through power connector J1 (IL-4P-S3FP2: manufactured by Japan Aviation Electronics Industry, Ltd.) The power connector pins work as follows:         <ul> <li>Pin 1: GND (black)</li> <li>Pin 2: 5 V (red)</li> <li>Pin 4: GND (black)</li> </ul> </li> </ul>
	<ul> <li>When the emulation memory board is connected to the user system, supply +3.3 V from the VDDQ pin on the YQPACK256SE connector, respectively.</li> </ul>

#### Table 3.2 Emulation Memory Board Functions (cont)

- Notes: 1. For the substitution emulation memory, a 16-bit bus and a 32-bit bus are supported. Do not set the bus width to 8 bits when using the substitution emulation memory.
  - 2. When allocating substitution emulation memory to an area, set WCR2 of the bus state controller to provide an appropriate cycle access state.
  - 3. When connecting the emulation memory board to the user system, note that the RDY signal is pulled down to ground on the emulation memory board so that the bus processing will be completed if any area other than the substitution emulation memory (CS0 area) is accessed.

## CAUTION

Restriction on Buffer Control Using the RD Signal: RD signal output cannot be disabled from the emulator. Consequently, when the buffer control on the user system uses only the RD signal, data read from this emulation memory board and data output from the buffer may conflict. For this reason, when using the emulation memory board, be sure to control the data bus buffer of the user system with both the CS and RD (used in direction control) signals.

### Section 4 Emulation Memory Board Operation

The emulation memory board has a RESET switch (SW1) for issuing a reset signal, a DIP switch (SW2) and jumper switches (JP1 and JP2) for various settings, a switch (SW3) for selecting the power source, a socket (SP1) for installing a crystal oscillator, and LEDs for signal monitoring. Figure 4.1 shows the switches, socket, and LEDs.

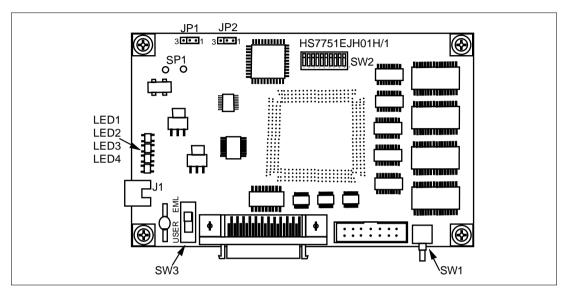


Figure 4.1 Switches, Socket, and LEDs

#### 4.1 Switch Setting

#### 4.1.1 Power Source Switch Setting

The SW3 selects whether the power for the emulation memory board is supplied from an external source or through the user system interface.



Always switch OFF the user system and the emulation memory board before power source switch setting. Failure to do so will damage the user system and the emulation memory board. The USER PROGRAM will be LOST.

To supply power from an external source (sliding the switch to EML):



To supply power through the user system interface (sliding the switch to USER):



#### 4.1.2 Jumper Switch Setting

The emulation memory board has two jumper switches JP1 and JP2 for the following settings.

**JP1 Function:** The JP1 selects whether the clock for the MCU is supplied from the emulation memory board or from the user system. When installing a crystal oscillator into the socket (SP1) on the emulation memory board, open JP1. In this case, set the jumper connector on pin 1 as shown below so that the jumper connector will not be lost.

To supply the clock from the emulation memory board (EML side: pins 2-1 closed):

JP1 3

To supply the clock from the user system (USER side: pins 3-2 closed):

JP1 3 ••• 1

To install a crystal oscillator into the SP1 socket on the emulation memory board (JP1 is open):

JP1 3

- Notes: 1. When closing 1-2 pins or 2-3 pins of JP1, turn switch 9 of SW2 ON (see table 4.5). When leaving JP1 open (installing a crystal oscillator), turn switch 9 of SW2 OFF.
  - 2. The emulation memory board supports the external clock input through the EXTAL pin and the clock generated by the crystal oscillator installed on the SP1 socket. Therefore, be sure to supply the clock to the EXTAL pin when using the user system clock. If the clock is supplied to the XTAL, EXTAL2, or XTAL2 pin, the emulation memory board cannot operate.

**JP2 Function:** The JP2 selects the CS0 signal output destination to specify whether the substitution memory on the emulation memory board or the memory of the user system is used.

## CAUTION

- Restriction on Buffer Control Using the RD Signal: RD signal output cannot be disabled from the emulator. Consequently, when the buffer control on the user system uses only the RD signal, data read from this emulation memory board and data output from the buffer may conflict. For this reason, when using the emulation memory board, be sure to control the data bus buffer of the user system with both the CS and RD (used in direction control) signals.
- 2. The substitution emulation memory is allocated to the 4 Mbytes from the start address of area 0. If the memory of the user system is allocated to area 0, that is, the same area as the substitution emulation memory, only the memory selected by the JP2 setting is used. When the substitution emulation memory is selected by JP2, the CS0 signal is not output to the user system.

To use the substitution memory on the emulation memory board (EML side: pins 2-1 closed):

JP2 3 •••1

To use the memory of the user system (USER side: pins 3-2 closed):

JP2 3 ••• 1

#### 4.1.3 DIP Switch (SW2) Setting

The emulation memory board has one DIP switch for the following settings.

- Selecting the clock operating mode: Three switches
- Selecting the memory type and bus width for area 0: Three switches
- Selecting the endian: One switch
- Selecting the master or slave mode: One switch
- Selecting the clock source: One switch
- Selecting whether or not to write-protect the substitution emulation memory: One switch

Tables 4.1 to 4.7 show the SW2 functions.

Note: For details on the mode control terminals (MD0 to MD10), refer to the SH7751 Hardware Manual.

# CAUTION

1. When a user system is connected to the emulation memory board, the DIP switch (SW2) settings are ignored, and the MD0 to MD10 signals input to the user system are used.

The setting on switch 0 of SW2 is only valid when JP2 is set to select the EML side (pins 2-1 closed), regardless of whether or not the user system is connected to the emulation memory board.

 When the emulation memory board is not connected to the user system, the PCI controller is not supported. In this case, the PCI mode setting (MD9 and MD10) cannot be modified.

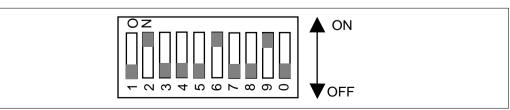


Figure 4.2 DIP Switch (SW2) Appearance and Settings at Shipment

**Clock Operating Mode Setting:** Select the clock operating mode as shown in table 4.1.

Table 4.1	Clock Operating Mode Setting (Switches 1 to 3 in SW2)
-----------	---

2 (MD1)	1 (MD0)	Clock Mode	Remarks	
ON	ON	0		
ON	OFF	1		
OFF	ON	2		
OFF	OFF	3		
ON	ON	4		
ON	OFF	5	Initial setting at shipment	
	ON ON OFF OFF ON	ONONONOFFOFFONOFFOFFONON	ONON0ONOFF1OFFON2OFFOFF3ONON4	

Switches in SW2 (Corresponding Mode Pins)

Area 0 Memory Type and Bus Width Setting: Select the memory type and bus width for area 0 as shown in table 4.2.

#### Memory Bus Width Setting (Switches 4, 5, and 7 in SW2) Table 4.2

(Correspo	nding Mode F	Pins)			
7 (MD6)	5 (MD4)	4 (MD3)	Memory Type	Bus Width	Remarks
ON	ON	ON	Reserved	Reserved	Do not use this setting
ON	ON	OFF	Reserved	Reserved	Do not use this setting
ON	OFF	ON	Reserved	Reserved	Do not use this setting
ON	OFF	OFF	MPX	32 bits	*1
OFF	ON	ON	Reserved	Reserved	Do not use this setting
OFF	ON	OFF	SRAM	8 bits	Do not use this setting <sup>*2</sup>
OFF	OFF	ON	SRAM	16 bits	
OFF	OFF	OFF	SRAM	32 bits	Initial setting at shipment

Switches in SW2

Notes: 1. When using the substitution emulation memory, turn off switch 7 (MD6)

2. The substitution emulation memory does not support the 8-bit bus width.

Endian Setting: Select the endian as shown in table 4.3.

#### Table 4.3Endian Setting (Switch 6 in SW2)

Switch in SW2 (Corresponding Mode Pin)		
6 (MD5)	Endian	Remarks
ON	Big endian	Initial setting at shipment
OFF	Little endian	

Master or Slave Mode Setting: Select the master or slave mode as shown in table 4.4.

#### Table 4.4Master or Slave Mode Setting (Switch 8 in SW2)

Switch in SW2 (Corresponding Pin)		
8 (MD7)	Master or Slave Mode	Remarks
ON	Slave mode	
OFF	Master mode	Initial setting at shipment

**Clock Source Setting:** Select whether to input the clock from the EXTAL or a crystal oscillator as shown in table 4.5.

# 

Always switch OFF the user system and the emulation memory board before installing or uninstalling the crystal oscillator to/from the SP1 socket. Failure to do so will damage the user system, the emulation memory board, and the crystal oscillator. The USER PROGRAM will be LOST.

Table 4.5Clock Source Setting (Switch 9 in SW2)

#### Switch in SW2 (Corresponding Pin)

9 (MD8)	Clock Source	Remarks
ON	External clock	Initial setting at shipment
OFF	Crystal oscillator	

Note: When setting this switch to ON, do not open JP1. When setting this switch to OFF, be sure to install a crystal oscillator into the SP1 socket on the emulation memory board.

**Write-Protection Setting:** Select whether to write-protect the substitution emulation memory while the user program is running as shown in table 4.6. When write-protection is not specified, the substitution emulation memory can be written to.

Table 4.6	Write-Protection Setting (Switch 0 in SW2)
Switch in S	W2 (Corresponding Pin)

0 (WP)	Write-Protection	Remarks
ON	Write-protected	
OFF	Write-enabled	Initial setting at shipment

- Notes: 1. In the following two situations, the substitution emulation memory will not be write-protected even when this switch is set to ON (write-protected): when an E10A emulator break is executed immediately after a write instruction and when single-step execution is performed.
  - 2. When JP2 is set to select the USER side (user system memory), the writeprotection setting switch (switch 0 in SW2) becomes invalid; the substitution emulation memory is not write-protected even when switch 0 in SW2 is set to ON (write-protected).

**PCI Mode Setting:** The PCI controller is not supported when the user system is not connected to the emulation memory board. The emulation memory board does not therefore have a switch for setting the PCI mode. When the user system is not connected, the PCI mode is PCI-disabled. When the user system is connected, the PCI mode is determined by the MD9 and MD10 signals from the user system.

Pins				
Mode	MD10	MD9	PCI Mode	
0	0	0	PCI host, external input clock	
1	0	1	PCI host, CKIO feedback input clock	
2	1	0	PCI not host, external input clock	
3	1	1	PCI disabled	

Note: When the user system is not connected to the emulation memory board, the PCI mode setting cannot be modified.

#### 4.1.4 RESET Switch (SW1)

The emulation memory board has RESET switch for issuing a reset signal.

The /RESETP signal to the MCU is obtained by ORing the reset signal from the RESET switch, that from the power-on reset circuit on the emulation memory board, and the /RESETP signal from the user system. The manual reset, on the other hand, is done using only the /RESETM signal from the user system. Figure 4.3 shows the logic diagram for the reset circuit.

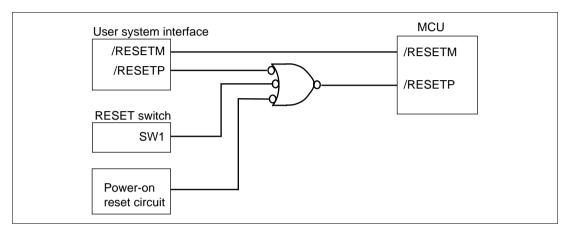


Figure 4.3 Reset Circuit Logic Diagram

#### 4.2 Monitor LEDs

The emulation memory board has LEDs for monitoring the operating state. Table 4.8 shows the LEDs and the states to be monitored.

For details on STATUS1 and STATUS0 signals, refer to the SH7751 Hardware Manual.

LED	Indication on the Board	LED Status	Remarks
LED1	RESET	Green LED lit when /RESETP is asserted	
	POWER	Red LED lit when power is supplied	
LED2	RDY	Green LED lit when /RDY is asserted	
	U-RUN	Red LED lit when in USER RUN state	Signal: ASEBRKAK
LED3	BREQ	Green LED lit when /BREQ is asserted	
	NMI	Red LED lit when /NMI is asserted	
LED4	STATUS1	Green LED lit when STATUS1 is 0 (low)	
	STATUS0	Red LED lit when STATUS0 is 0 (low)	

#### Table 4.8 LEDs and States to Be Monitored

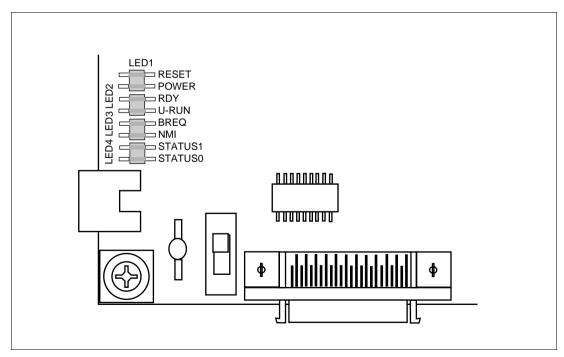


Figure 4.4 LED Location and Indication on the Board

### 5.1 Connecting Emulation Memory Board to Emulator and User System

Be sure to switch off the emulator and user system before connecting the emulation memory board, emulator, and user system. Do not supply power to the power connector on the emulation memory board when using the user system.

# A WARNING

Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system, the emulation memory board, and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

- 1. Always switch OFF the emulator product, the emulation memory board, and the user system before connecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or USER SYSTEM.
- 2. DO NOT supply power to the emulation memory board power connector (J1) when the emulation memory board is connected to the user system. When connected to the user system, the emulation memory board receives power from the VDDQ pin of the IC socket (NQPACK256SE) and operates by the user system power.

**Connecting Emulation Memory Board to Emulator:** Connect the emulator to the 14-pin connector (CN1) or 36-pin connector (CN2) on the emulation memory board, depending on the emulator type as follows:

HS7751KCM01H or HS7751KCI01H: 14-pin connector (CN1) HS7751KCM02H or HS7751KCI02H: 36-pin connector (CN2)

For details on the connection procedure, refer to the SH7751 E10A Emulator User's Manual.

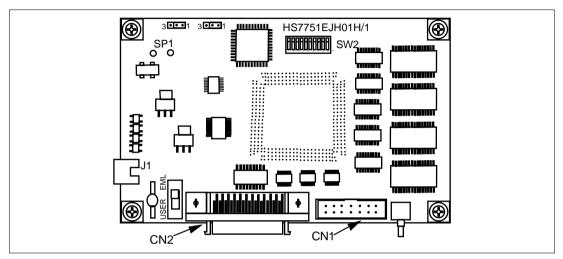


Figure 5.1 Connectors for Emulator

Connecting Emulation Memory Board to User System: Follow the instructions below.

# WARNING

Observe the precautions listed below. Failure to do so will result in a FIRE HAZARD and will damage the user system, the emulation memory board, and the emulator product or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

- 1. Always switch OFF the emulator product, the emulation memory board, and the user system before connecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or USER SYSTEM.
- 2. Use the recommended IC socket on the user system. Otherwise, excessive force will be applied to the emulation memory board and the user system when the emulation memory board is connected to or disconnected from the user system.

# CAUTION

- 1. Use NQPACK256SE (manufactured by Tokyo Eletech Corporation) as the QFP256 IC socket on the user system.
- 2. To mount the MCU directly on the NQPACK256SE socket, a socket cover must be used. Separately purchase HQPACK256SE (manufactured by Tokyo Eletech Corporation).

- 1. Confirm that the pins of the YQPACK connector on the emulation memory board are not bent.
- 2. Align pin 1 of the YQPACK connector on the emulation memory board with pin 1 of the NQPACK socket on the user system, and insert the connector into the socket.

# CAUTION

The structures of the YQPACK connector and NQPACK socket prevent the connector from being fully inserted in the wrong direction. If the connector cannot be inserted fully, pin 1 on the connector and that on the socket may not be aligned correctly. Check the pin 1 locations on the connector and socket and re-insert the YQPACK connector.

3. After inserting the YQPACK connector on the emulation memory board into the NQPACK socket of the user system, fix the emulation memory board in place with the supplied screws, as shown in figure 5.2.

# CAUTION

- 1. Use the supplied screwdriver.
- 2. The tightening torque must be 0.054 N•m or less. Stop tightening when the force required to turn the screw becomes significantly greater than that needed when first tightening.
- 3. If a screw is tightened too much, the screw head may break or an IC socket contact error may be caused by a crack in the IC socket solder.
- 4. If the emulator does not operate correctly, cracks might have occurred in the solder. Check conduction with a tester and re-solder the IC socket if necessary.

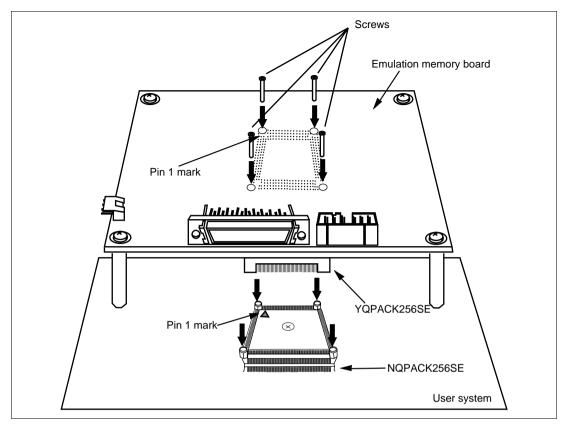


Figure 5.2 Connecting Emulation Memory Board to User System

**Power Supply Specifications:** When the user system is connected, the emulation memory board operates by the user system power. Supply the user system power according to the specifications and rising timing shown in table 5.1 and figure 5.3.

## CAUTION

- 1. Check that the SW3 switch is set to the power supply through the user system interface, and supply 3.3-V power to the VDDQ pin. Do not supply power to the power connector (J1) on the emulation memory board.
- 2. When power is supplied through the user system interface (YQPACK), only 3.3-V power should be supplied from the user system, and the emulation memory board generates 1.8-V power from the 3.3-V power. Therefore, the VDD pin (1.8 V) of the user system interface (YQPACK) is not connected to the MCU on the emulation memory board.

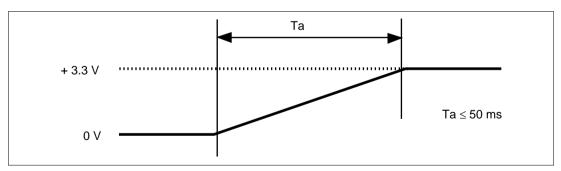
#### Table 5.1 Power Supply Specifications



+ 3.3 VDC ± 5%

1.1 A (max.)

**Current Consumption** 





#### 5.2 Operating Emulation Memory Board Without Connecting User System

Be sure to switch off the emulator and emulation memory board before connecting them together and before connecting the power cables to the emulation memory board.

# **WARNING**

Always switch OFF the emulator product and the emulation memory board before connecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or POWER CABLES. Failure to do so will result in a FIRE HAZARD and will damage the emulator product and the emulation memory board or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

**Connecting to the Emulator:** Connect the emulation memory board to the emulator by using the same procedure as in section 5.1, Connecting Emulation Memory Board to Emulator and User System.

**Connecting the Power Cables:** After making sure the alignment is correct, connect the provided power cables to the power connector (J1) on the emulation memory board to supply power, as shown in figure 5.4. (The power cable and connector structures will prevent the power cables from being connected in the wrong direction.)

Note that the red cables are for 5-V power and the black ones are for GND; connect them to the DC power source correctly.

# **WARNING**

Be sure to connect the power cables to the DC power source correctly, that is, the red cables to the 5-V power and the black ones to GND. Failure to do so will result in a FIRE HAZARD and will damage the emulator product and the emulation memory board or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

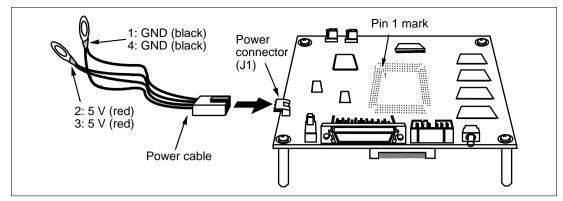


Figure 5.4 Connecting Power Cables to Power Connector

**Power Supply Specifications:** Table 5.2 shows the power supply specifications, and figure 5.5 shows the rising timing of the power.

#### Table 5.2 Power Supply Specifications

Allowable Power Range	Current Consumption
+ 5.0 VDC ± 5%	1.1 A (max.)

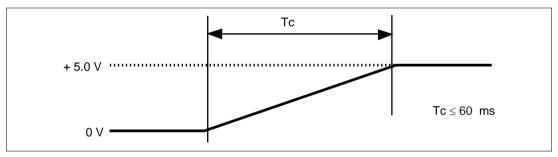


Figure 5.5 Characteristics of DC Rising Timing

#### 5.3 Disconnecting Emulation Memory Board from User System

Be sure to switch off the emulator and user system before disconnection.

## WARNING

Always switch OFF the emulator product, the emulation memory board, and the user system before disconnecting the EMULATOR PRODUCT, EMULATION MEMORY BOARD, or USER SYSTEM. Failure to do so will result in a FIRE HAZARD and will damage the emulator product, the emulation memory board, and the user system or will result in PERSONAL INJURY. The USER PROGRAM will be LOST.

Disconnecting Emulation Memory Board from User System: Follow the instructions below.

- 1. Remove the screws that connect the YQPACK connector and the NQPACK socket.
- 2. After removing all screws, remove the emulation memory board from the user system, taking care not to bend any of the pins.

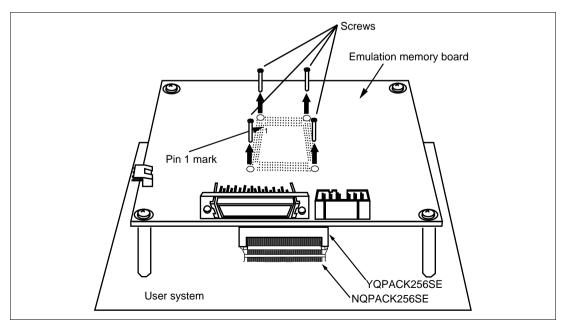


Figure 5.6 Disconnecting Emulation Memory Board

#### 5.4 Recommended Dimensions for User System Mount Pad

Figure 5.7 shows the recommended dimensions for the mount pad (footprint) for the user system with an IC socket for a QFP256 package (NQPACK256SE: manufactured by Tokyo Eletech Corporation). Note that the dimensions in figure 5.7 are somewhat different from those of the actual chip's mount pad.

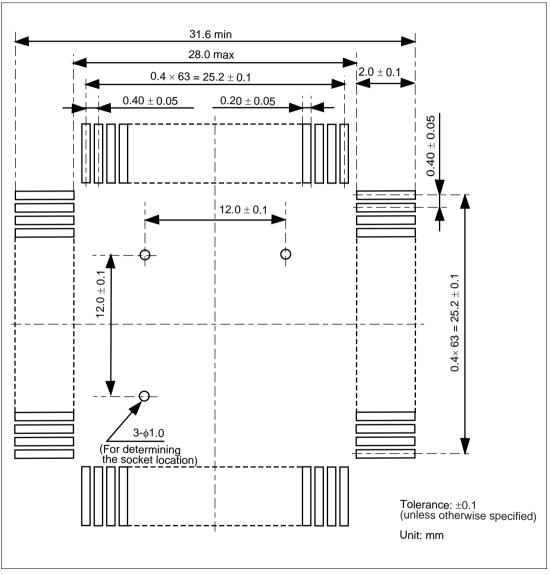


Figure 5.7 Recommended Dimensions for Mount Pad

### Section 6 Limitations

#### 6.1 Limitations on User System

To use the emulation memory board together with the user system, do not mount any components in the mount-prohibited areas (figure 6.1) of the user system. If any component is mounted on any of these areas, remove the corresponding spacer from the emulation memory board. In this case, take special care not to give any stress to the user system interface section (NQPACK).

The height of the mounted components must be 8.0 mm or shorter in the height-limited area (figure 6.1) of the user system. If any component in this area is higher than 8.0 mm, the emulation memory board cannot be connected to the user system.

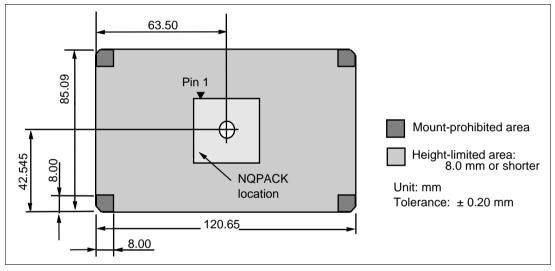


Figure 6.1 Mount-Prohibited and Height-Limited Areas of User System

### Section 7 User System Interface

#### 7.1 Pin Assignment and Handling of User System Interface Signals

The emulation memory board has a connector (YQPACK) for user system interface. Table 7.1 shows the pin assignment of the user system interface connector and signal handling on the emulation memory board.

	NO.	No. Signal Name	No. Signal Name Handling
	26	26 D8	26 D8
$ \begin{array}{c} 28\\ 29\\ 30\\ 31\\ 32\\ 33\\ 34\\ 35\\ 36\\ 36\\ 36\\ 36\\ 37\\ 38\\ 39\\ 40\\ 41\\ 42\\ 43\\ 44\\ 42\\ 43\\ 44\\ 45\\ 46\\ 45\\ 46\\ \end{array} $		D9	D9
30         31         32         33         34         35         36         37         38         39         40         41         42         43         44         45		D10	D10
$ \begin{array}{c} 31 \\ 32 \\ 33 \\ 34 \\ 35 \\ 36 \\ 37 \\ 38 \\ 39 \\ 40 \\ 41 \\ 42 \\ 43 \\ 44 \\ 45 \\ \end{array} $		VDDQ	VDDQ 3.3 V
32         33         34         35         36         37         38         39         40         41         42         43         44         45		VSSQ	VSSQ GND
$ \begin{array}{c} 33\\ 34\\ 35\\ 36\\ 37\\ 38\\ 39\\ 40\\ 41\\ 42\\ 43\\ 44\\ 45\\ \end{array} $		D11	D11
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	D12	D12
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	D13	D13
$ \begin{array}{c} 36\\ 37\\ 38\\ 39\\ 40\\ 41\\ 42\\ 43\\ 44\\ 45\\ \end{array} $		D14	D14
$ \begin{array}{c} 37 \\ 38 \\ 39 \\ 40 \\ 41 \\ 42 \\ 43 \\ 44 \\ 45 \\ \end{array} $		D15	D15
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		CAS0_N/DQM0	CAS0_N/DQM0
$ \begin{array}{c} 39 \\ 40 \\ 41 \\ 42 \\ 43 \\ 44 \\ 45 \\ \end{array} $	-	CAS1_N/DQM1	CAS1_N/DQM1
40 41 42 43 44 44 45		RD/WR_N	RD/WR_N
41           42           43           44           45		CKIO	CKIO Pull-up
42 43 44 45		Reserved	Reserved NC
43 44 45		VDDQ	VDDQ 3.3 V
44		VSSQ	VSSQ GND
45		Reserved	Reserved NC
		RD_N/CASS_N/ FRAME_N	
46		CKE	CKE
		RAS_N	RAS_N
47		VDD	VDD NC
48		VSS	VSS GND
49		CS2_N	CS2_N
50		CS3_N	CS3_N

#### Table 7.1 Pin Assignment and Handling of User System Interface

No.	Signal Name	Handling	Notes	No.	Signal Name	Handling	Notes
51	A0			81	VDD	NC	
52	A1			82	VSS	GND	
53	A2			83	D20		
54	A3			84	D21		
55	VDDQ	3.3 V		85	D22		
56	VSSQ	GND		86	D23		
57	A4			87	D24		
58	A5			88	D25		
59	A6			89	D26		
60	A7			90	D27		
61	S8			91	D28		
62	A9			92	D29		
63	A10			93	VDDQ	3.3 V	
64	A11			94	VSSQ	GND	
65	A12			95	D30		
66	A13			96	D31		
67	VDDQ	3.3 V		97	VDD	NC	
68	VSSQ	GND		98	VSS	GND	
69	A14			99	A18		
70	A15			100	A19		
71	A16			101	A20		
72	A17			102	A21		
73	CAS2_N/DQM2			103	A22		
74	CAS3_N/DQM3			104	A23		
75	D16			105	VDDQ	3.3 V	
76	D17			106	VSSQ	GND	
77	D18			107	A24		
78	D19			108	A25		
79	VDDQ	3.3 V		109	WE2_N/ICIORD_N		
80	VSSQ	GND		110	WE3_N/ICIOER_N		

#### Table 7.1 Pin Assignment and Handling of User System Interface (cont)

111     VDD     NC     141     AD22       112     VSS     GND     142     AD21       113     SLEEP_N     Pull-up     47 kΩ     143     VDDQ     3.3 V       114     PCIGNT4_N     144     VSSQ     GND       115     PCIGNT3_N     145     VDD     NC       116     PCIGNT2_N     146     VSS     GND       117     PCIREQ3_N/MD10     Pull-up     47 kΩ     148     AD19       119     VDQ     3.3 V     149     AD18       120     VSSQ     GND     150     AD17       121     PCIREQ2_N/MD9     Pull-up     47 kΩ     151     AD16       122     IDSEL     152     CBE2_N         124     PCIREQ2_N/MD9     Pull-up     47 kΩ     155     RCI       125     DSEL     154     IRDY_N        126     PCIREQ1_N/ REQUT_N     156     DEVSEL_N        127     PCIREQ1_N/ REQUT_N     156     DEVSEL_N        128     SER_N     158     VSSQ     GND       129     AD31     159     PCISTOP_N       130     AD30     160     PCILOCK_N       131	No.	Signal Name	Handling	Notes	No.	Signal Name	Handling	Notes
113       SLEEP_N       Pull-up       47 kΩ       143       VDDQ       3.3 V         114       PCIGNT4_N       144       VSSQ       GND         115       PCIGNT3_N       145       VDD       NC         116       PCIGNT2_N       146       VSS       GND         117       PCIREQ4_N       147       AD20	111	VDD	NC		141	AD22		
114       PCIGNT4_N       144       VSSQ       GND         115       PCIGNT3_N       145       VDD       NC         116       PCIGNT2_N       146       VSS       GND         117       PCIREQ4_N       147       AD20	112	VSS	GND		142	AD21		
15       PCIGNT3_N       145       VDD       NC         116       PCIGNT2_N       146       VSS       GND         117       PCIREQ4_N       147       AD20         118       PCIREQ3_N/MD10       Pull-up       47 kΩ       148       AD19         119       VDQ       3.3 V       149       AD18	113	SLEEP_N	Pull-up	47 kΩ	143	VDDQ	3.3 V	
116       PCIGNT_N       146       VSS       GND         117       PCIREQ_N       147       AD20	114	PCIGNT4_N			144	VSSQ	GND	
117       PCIREQ4_N       147       AD20         118       PCIREQ3_N/MD10       Pull-up       47 kΩ       148       AD19         119       VDQ       3.3 V       149       AD18	115	PCIGNT3_N			145	VDD	NC	
118       PCIREQ3_N/MD10       Pull-up       47 kΩ       148       AD19         119       VDQ       3.3 V       149       AD18         120       VSSQ       GND       150       AD17         121       PCIREQ2_N/MD9       Pull-up       47 kΩ       151       AD16         122       IDSEL       152       CBE2_N       151       AD16         122       IDSEL       152       CBE2_N       151       AD16         123       INTA_N       153       PCIFRAME_N       153       PCIFRAME_N         124       PCIRST_N       154       IRDY_N       154       IRDY_N         125       PCICLK       155       TRDY_N       155       IRDY_N       160       PCIGNT1_NV       REQUIT_N       156       DEVSEL_N       157       VDQ       3.3 V       3.3 V       160       PCICOCK_N       130       AD30       159       PCISTOP_N       150       AD17       150       ICOCK_N       150 <td>116</td> <td>PCIGNT2_N</td> <td></td> <td></td> <td>146</td> <td>VSS</td> <td>GND</td> <td></td>	116	PCIGNT2_N			146	VSS	GND	
119         VDDQ         3.3 V         149         AD18           120         VSSQ         GND         150         AD17           121         PCIREQ2_N/MD9         Pull-up         47 kΩ         151         AD16           122         IDSEL         152         CBE2_N         151         AD16           122         IDSEL         152         CBE2_N         151         AD16           123         INTA_N         153         PCIFRAME_N         151         AD17           124         PCIRST_N         154         IRDY_N         156         DEVSEL_N           125         PCICLK         155         TRDY_N         156         DEVSEL_N           126         PCIGNT1_N/ REQOUT_N         156         DEVSEL_N         157         VDDQ         3.3 V           128         SERR_N         158         VSSQ         GND         160         PCICOCK_N           130         AD30         160         PCICOCK_N         160         PCICOCK_N           131         VDDQ         3.3 V         161         PERR_N         162         PAR           133         AD29         GND         162         PAR         163         CBE1_N	117	PCIREQ4_N			147	AD20		
120         VSSQ         GND         150         AD17           121         PCIREQ2_N/MD9         Pull-up         47 kΩ         151         AD16           122         IDSEL         152         CBE2_N         151         AD16           123         INTA_N         153         PCIFRAME_N         152         CBE2_N           124         PCIRST_N         154         IRDY_N         154         IRDY_N           125         PCICLK         155         TRDY_N         156         DEVSEL_N           126         PCIGNT1_N/ REQOUT_N         156         DEVSEL_N         156         DEVSEL_N           127         PCIRE01_N/ GNTIN_N         158         VSSQ         GND         3.3 V           128         SERR_N         158         VSSQ         GND         161         PER_N           129         AD31         159         PCISTOP_N         130         AD30         160         PCILOCK_N         131           130         AD30         161         PERR_N         161         PERR_N         131           133         AD29         GND         162         PAR         133         161         Edet_N         161         161 <t< td=""><td>118</td><td>PCIREQ3_N/MD10</td><td>Pull-up</td><td>47 kΩ</td><td>148</td><td>AD19</td><td></td><td></td></t<>	118	PCIREQ3_N/MD10	Pull-up	47 kΩ	148	AD19		
121         PCIREQ2_N/MD9         Pull-up         47 kΩ         151         AD16           122         IDSEL         152         CBE2_N         151         AD16           123         INTA_N         153         PCIFRAME_N         153         PCIFRAME_N           124         PCIRST_N         154         IRDY_N         154         IRDY_N           125         PCICLK         155         TRDY_N         156         DEVSEL_N           126         PCIGNT1_N/ REQOUT_N         156         DEVSEL_N         157         VDDQ         3.3 V           127         PCIREQ1_N/ GNTIN_N         158         VSSQ         GND         161         PER_N         150         PCISTOP_N           128         SERR_N         159         PCISTOP_N         150         PCICK_N         151         160         PCILOCK_N         151         161         PER_N         151         161         PCISTOP_N         151         152         VSQ         GND         162         PAR         153         161         PCISTOP_N         153         162         PAR         153         AD29         163         CBE1_N         153         AD27         165         AD14         151         153         <	119	VDDQ	3.3 V		149	AD18		
122       IDSEL       152       CBE2_N         123       INTA_N       153       PCIFRAME_N         124       PCIRST_N       154       IRDY_N         125       PCICLK       155       TRDY_N         126       PCIGNT1_N/ REQOUT_N       156       DEVSEL_N         127       PCIREQ1_N/ GNTIN_N       156       DEVSEL_N         128       SERR_N       158       VSSQ       GND         129       AD31       159       PCISTOP_N       160       PCILOCK_N         130       AD30       161       PERR_N       162       PAR         133       AD29       3.3 V       161       PERR_N       155       AD14         134       AD28       164       AD15       155       AD14       155       AD14       155       AD14       135       AD27       166       AD13       137       AD25       167       AD12       138       AD24       168       AD11       139       CB3_N       169       VDDQ       3.3 V       169       VDDQ       3.3 V       165       AD14       166       AD13       165       AD14       166       AD13       167       AD12       168       AD11	120	VSSQ	GND		150	AD17		
123       INTA_N       153       PCIFRAME_N         124       PCIRST_N       154       IRDY_N         125       PCICLK       155       TRDY_N         126       PCIGNT1_N/ REQOUT_N       156       DEVSEL_N         127       PCIREQ1_N/ GNTIN_N       157       VDDQ       3.3 V         128       SERR_N       158       VSSQ       GND         129       AD31       159       PCISTOP_N       160         130       AD30       160       PCILOCK_N       161         131       VDDQ       3.3 V       161       PERR_N       153         133       AD29       163       CBE1_N       164       AD15         134       AD28       166       AD13       164       AD15         135       AD27       166       AD13       164       AD14         136       AD26       167       AD12       168       AD11         138       AD24       168       AD11       169       VDQ       3.3 V	121	PCIREQ2_N/MD9	Pull-up	47 kΩ	151	AD16		
124       PCIRST_N       154       IRDY_N         125       PCICLK       155       TRDY_N         126       PCIGNT1_N/ REQOUT_N       156       DEVSEL_N         127       PCIREQ1_N/ GNTIN_N       157       VDDQ       3.3 V         128       SERR_N       158       VSSQ       GND         129       AD31       159       PCISTOP_N	122	IDSEL			152	CBE2_N		
125       PCICLK       155       TRDY_N         126       PCIGNT1_N/ REQOUT_N       156       DEVSEL_N         127       PCIREQ1_N/ GNTIN_N       157       VDDQ       3.3 V         128       SERR_N       158       VSSQ       GND         129       AD31       159       PCISTOP_N       130         130       AD30       160       PCILOCK_N       131         131       VDDQ       3.3 V       161       PER_N         132       VSSQ       GND       162       PAR         133       AD29       163       CBE1_N       134         134       AD28       164       AD15       135         135       AD27       165       AD14       131         136       AD26       166       AD13       137         138       AD24       168       AD11       139       VDQ       3.3 V	123	INTA_N			153	PCIFRAME_N		
126       PCIGNT1_N/ REQOUT_N       156       DEVSEL_N         127       PCIREQ1_N/ GNTIN_N       157       VDDQ       3.3 V         128       SERR_N       158       VSSQ       GND         129       AD31       159       PCISTOP_N       100         130       AD30       160       PCILOCK_N       111         131       VDDQ       3.3 V       161       PERR_N       111         132       VSSQ       GND       162       PAR       111       111         133       AD29       163       CBE1_N       111	124	PCIRST_N			154	IRDY_N		
$\begin{array}{ c c c c c c } REQOUT_N & & & & & & & & & & & & & & & & & & &$	125	PCICLK			155	TRDY_N		
GNTIN_N       158       VSSQ       GND         128       SERR_N       159       PCISTOP_N         130       AD30       160       PCILOCK_N         131       VDQ       3.3 V       161       PERR_N         132       VSSQ       GND       162       PAR         133       AD29       163       CBE1_N	126	—			156	DEVSEL_N		
129       AD31       159       PCISTOP_N         130       AD30       160       PCILOCK_N         131       VDDQ       3.3 V       161       PERR_N         132       VSSQ       GND       162       PAR         133       AD29       163       CBE1_N       134         134       AD28       164       AD15       135         135       AD27       165       AD14       136         137       AD26       166       AD13       137         138       AD24       168       AD11       3.3 V         139       CBE3_N       169       VDDQ       3.3 V	127	_			157	VDDQ	3.3 V	
130       AD30       160       PCILOCK_N         131       VDDQ       3.3 V       161       PERR_N         132       VSSQ       GND       162       PAR         133       AD29       163       CBE1_N         134       AD28       164       AD15         135       AD27       165       AD14         136       AD26       166       AD13         137       AD25       168       AD11         138       AD24       168       AD11         139       CBE3_N       169       VDDQ       3.3 V	128	SERR_N			158	VSSQ	GND	
131     VDDQ     3.3 V     161     PERR_N       132     VSSQ     GND     162     PAR       133     AD29     163     CBE1_N       134     AD28     164     AD15       135     AD27     165     AD14       136     AD26     166     AD13       137     AD25     167     AD12       138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	129	AD31			159	PCISTOP_N		
132     VSSQ     GND     162     PAR       133     AD29     163     CBE1_N       134     AD28     164     AD15       135     AD27     165     AD14       136     AD26     166     AD13       137     AD25     167     AD12       138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	130	AD30			160	PCILOCK_N		
133       AD29       163       CBE1_N         134       AD28       164       AD15         135       AD27       165       AD14         136       AD26       166       AD13         137       AD25       167       AD12         138       AD24       168       AD11         139       CBE3_N       169       VDDQ       3.3 V	131	VDDQ	3.3 V		161	PERR_N		
134     AD28     164     AD15       135     AD27     165     AD14       136     AD26     166     AD13       137     AD25     167     AD12       138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	132	VSSQ	GND		162	PAR		
135     AD27     165     AD14       136     AD26     166     AD13       137     AD25     167     AD12       138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	133	AD29			163	CBE1_N		
136     AD26     166     AD13       137     AD25     167     AD12       138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	134	AD28			164	AD15		
137     AD25     167     AD12       138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	135	AD27			165	AD14		
138     AD24     168     AD11       139     CBE3_N     169     VDDQ     3.3 V	136	AD26			166	AD13		
139 CBE3_N 169 VDDQ 3.3 V	137	AD25			167	AD12		
	138	AD24			168	AD11		
140 AD23 170 VSSQ GND	139	CBE3_N			169	VDDQ	3.3 V	
	140	AD23			170	VSSQ	GND	

 Table 7.1
 Pin Assignment and Handling of User System Interface (cont)

No.	Signal Name	Handling	Notes	No.	Signal Name	Handling	Notes
171	AD10			201	NMI	Pull-up	47 kΩ
172	AD9			202	BACK_N/BSREQ_N	Pull-up	47 kΩ
173	AD8			203	BREQ_N/BSACK_N	Pull-up	47 kΩ
174	CBE0_N			204	MD6/IOIS16_N	Pull-up	47 kΩ
175	VDD	NC		205	RDY_N	Pull-down	4.7 kΩ
176	VSS	GND		206	TXD		
177	AD7			207	VDDQ	3.3 V	
178	AD6			208	VSSQ	GND	
179	AD5			209	VDD	NC	
180	AD4			210	VSS	GND	
181	AD3			211	MD2/RXD2	Pull-up	47 kΩ
182	AD2			212	RXD	Pull-up	47 kΩ
183	VDDQ	3.3 V		213	TCLK	Pull-up	47 kΩ
184	VSSQ	GND		214	MD8/RTS2_N	Pull-up	47 kΩ
185	AD1			215	SCK	Pull-up	47 kΩ
186	AD0			216	MD1/TXD2	Pull-up	47 kΩ
187	IRL0_N	Pull-up	47 kΩ	217	MD0/SCK2	Pull-up	47 kΩ
188	IRL1_N	Pull-up	47 kΩ	218	MD7/CTS2_N	Pull-up	47 kΩ
189	IRL2_N	Pull-up	47 kΩ	219	AUDSYNC	NC	
190	IRL3_N	Pull-up	47 kΩ	220	AUDCK	NC	
191	VSSQ	GND		221	VDDQ	3.3 V	
192	VDDQ	3.3 V		222	VSSQ	GND	
193	XTAL2	NC		223	AUDATA0	NC	
194	EXTAL2	NC		224	AUDATA1	NC	
195	VDD-RTC	3.3 V		225	VDD	NC	
196	VSS-RTC	GND		226	VSS	GND	
197	HARDSTB_N	Pull-up	47 kΩ	227	AUDATA2	NC	
198	RESET_N	Pull-up	47 kΩ	228	AUDATA3	NC	
199	TRST_N	NC		229	Reserved	NC	
200	MRESET_N	Pull-up	47 kΩ	230	MD3/CE2A_N	Pull-up	47 kΩ

Table 7.1	Pin Assignment ar	nd Handling of User	System Interface (cont)

lo.	Signal Name	Handling	Notes	No.	Signal Name	Handling	No
231	MD4/CE2B_N	Pull-up	47 kΩ	244	DREQ1_N	Pull-up	47
232	MD5	Pull-up	47 kΩ	245	ASEBRK_N/BRKACK	NC	
233	VDDQ	3.3 V		246	TDO	NC	
234	VSSQ	GND		247	VDDQ	3.3 V	
235	DACK0			248	VSSQ	GND	
236	DACK1			249	VDD-PLL2	NC	
237	DRAK0			250	VSS-PLL2	U-GND	
238	DRAK1			251	VDD-PLL1	NC	
239	VDD	NC		252	VSS-PLL1	GND	
240	VSS	GND		253	VDD-CPG	3.3 V	
241	STATUS0	Pull-up	47 kΩ	254	VSS-CPG	GND	
242	STATUS1	Pull-up	47 kΩ	255	XTAL	NC	
243	DREQ0_N	Pull-up	47 kΩ	256	EXTAL	Pull-up	47

 Table 7.1
 Pin Assignment and Handling of User System Interface (cont)

### CAUTION

When power is supplied through the user system interface (YQPACK), only 3.3-V power should be supplied from the user system, and the emulation memory board generates 1.8-V power from the 3.3-V power. Therefore, the VDD pin (1.8 V) of the user system interface (YQPACK) is not connected to the MCU on the emulation memory board.

#### Handling:

- Pull-up: The pin is pulled up to 3.3 V through a  $47-k\Omega$  resistor on the board.
- Pull-down: The pin is pulled down to GND through a 4.7-k $\Omega$  resistor on the board.
- 3.3 V: 3.3 V is supplied from the user system (when sliding the switch to USER).
- U-GND: The pin is connected to user system GND (to check whether or not the user system is connected).
- GND: The pin is connected to GND on the board.
- NC: The MCU pin is not connected to the user system interface connector.
- Blank: The MCU pin is directly connected to the user system interface connector.

# 7.2 Signal Line Handling on the Emulation Memory Board and User System

The emulation memory board is connected to the user system through the user system interface connector (YQPACK) and the IC socket (NQPACK). Figure 7.1 shows the signal line handling on the emulation memory board and the user system.

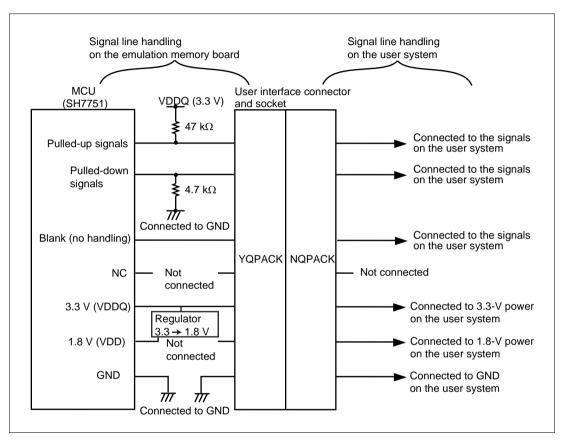


Figure 7.1 Signal Line Handling on the Emulation Memory Board and User System

### Section 8 Emulation Memory Board Block Diagram

The emulation memory board has an MCU (SH7751), a user system interface connector, emulator connectors, and memory. Figure 8.1 shows the block diagram of the emulation memory board.

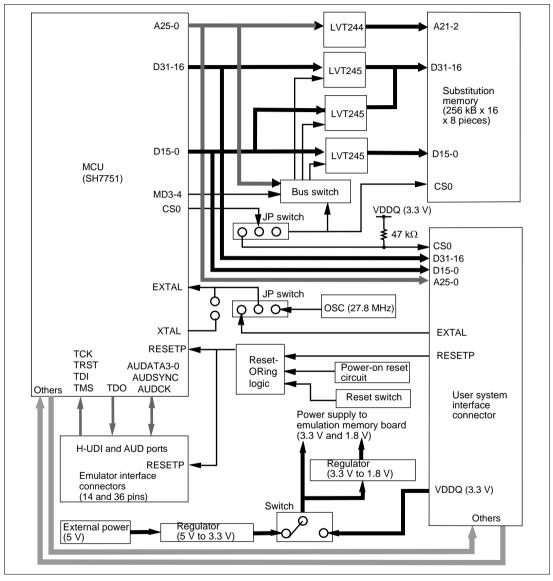


Figure 8.1 Emulation Memory Board Block Diagram