User's Manual

32

RX64M Group, RX71M Group Flash Memory

User's Manual: Hardware Interface

RENESAS 32-Bit MCU
RX Family / RX600 Series, RX700 Series

Renesas Electronics
www.renesas.com

Rev.1.21 Oct 2022

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Contents

1. Features

The features of the hardware interface of the flash memory are described below. See the User's Manual: Hardware for information on the capacity, block configuration, and addresses of the flash memory in this MCU.

Programming/Erasure

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via internal peripheral bus 6. The flash sequencer also supports the suspension or resumption of programming or erasure, and background operation (BGO).

Security Functions

The flash memory incorporates hardware functions to prevent falsification or unauthorized reading of data in flash memory.

Protection Functions

The flash memory incorporates hardware functions to prevent erroneous writing.

Interrupts

The flash memory supports an interrupt to indicate completion of processing by the flash sequencer and an error interrupt to indicate operations that were in error.

2. Module Configuration

Modules related to the flash memory are configured as shown in Figure 2.1. The flash sequencer is configured of the Flash Control Unit (FCU) and Flash Application Command Interface (FACI). The FCU basically controls of overwriting of the flash memory. The FCURAM is RAM for the storage of firmware that the FCU executes (FCU firmware). The FACI receives FACI commands via internal peripheral bus 6 and controls FCU operations accordingly.

The FACI transfers data to the option-setting memory in the configuration setting area of the flash memory during a reset.

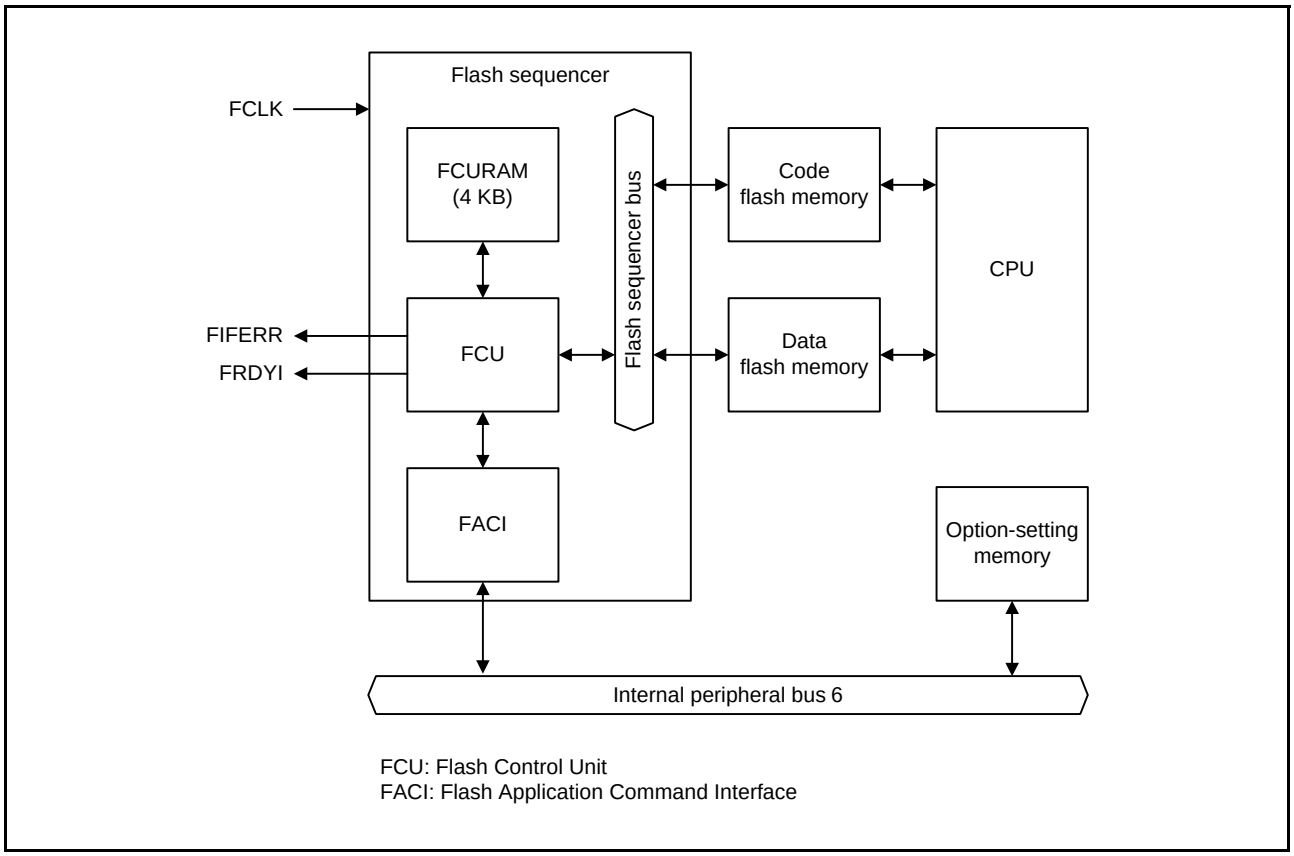


Figure 2.1 Configuration of Flash Memory-Related Modules

3. Address Space

Using the hardware interface with the flash memory requires accessing to the area containing registers of the hardware, that for the issuing of FACI commands, that for the FCURAM, and that for storage of the FCU firmware. Table 3.1 summarizes information on all of these areas.

Table 3.1 Information on the Hardware Interface Area

Area	Address	Capacity
Area containing the various registers of the hardware	See section 4, Registers.	See section 4, Registers.
FACI command-issuing area	007E 0000h	4 bytes
FCU firmware storage area	FEFF F000h to FEFF FFFFh	4 Kbytes
FCURAM area	007F 8000h to 007F 8FFFh	4 Kbytes
Configuration setting area	0012 0040h to 0012 00FFh	192 bytes

Refer to the User's Manual: Hardware for information on the addresses of the flash memory.

4. Registers

This section contains information on registers to which access is required when using the hardware interface of the flash memory. Reset registers that are not specifically mentioned to their initial states.
For information on the option-setting memory, see the User's Manual: Hardware for the product you are using.

Table 4.1 List of Registers

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Page
						ICLK ≥ PCLKB/FCLK	ICLK < PCLKB/FCLK	
0008 C296h	FLASH	Flash P/E Protect Register	FWEPROR	8	8	4 to 5 PCLKB	2 to 3 ICLK	10
007F E010h	FLASH	Flash Access Status Register	FASTAT	8	8	2 to 4 FCLK	2 to 3 ICLK	11
007F E014h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2 to 4 FCLK	2 to 3 ICLK	13
007F E018h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2 to 4 FCLK	2 to 3 ICLK	14
007F E030h	FLASH	FACI Command Start Address Register	FSADDR	32	32	2 to 4 FCLK	2 to 3 ICLK	15
007F E034h	FLASH	FACI Command End Address Register	FEADDR	32	32	2 to 4 FCLK	2 to 3 ICLK	16
007F E054h	FLASH	FCURAM Enable Register	FCURAME	16	16	2 to 4 FCLK	2 to 3 ICLK	17
007F E080h	FLASH	Flash Status Register	FSTATR	32	32	2 to 4 FCLK	2 to 3 ICLK	18
007F E084h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 to 4 FCLK	2 to 3 ICLK	22
007F E088h	FLASH	Flash Protection Register	FPROTR	16	16	2 to 4 FCLK	2 to 3 ICLK	23
007F E08Ch	FLASH	Flash Sequencer Set-Up Initialization Register	FSUINITR	16	16	2 to 4 FCLK	2 to 3 ICLK	24
007F E090h	FLASH	Lock Bit Status Register	FLKSTAT	8	8	2 to 4 FCLK	2 to 3 ICLK	25
007F E0A0h	FLASH	FACI Command Register	FCMDR	16	16	2 to 4 FCLK	2 to 3 ICLK	26
007F E0C0h	FLASH	Flash P/E Status Register	FPESTAT	16	16	2 to 4 FCLK	2 to 3 ICLK	27
007F E0D0h	FLASH	Data Flash Blank Check Control Register	FBCCNT	8	8	2 to 4 FCLK	2 to 3 ICLK	27
007F E0D4h	FLASH	Data Flash Blank Check Status Register	FBCSTAT	8	8	2 to 4 FCLK	2 to 3 ICLK	28
007F E0D8h	FLASH	Data Flash Programming Start Address Register	FPSADDR	32	32	2 to 4 FCLK	2 to 3 ICLK	28
007F E0E0h	FLASH	Flash Sequencer Processing Switching Register	FCPSR	16	16	2 to 4 FCLK	2 to 3 ICLK	29
007F E0E4h	FLASH	Flash Sequencer Processing Clock Notification Register	FPCKAR	16	16	2 to 4 FCLK	2 to 3 ICLK	30

4.1 Flash P/E Protect Register (FWEPROR)

Address(es): 0008 C296h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FLWE[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	FLWE[1:0]	Flash Program/Erase Enable	b1 b0 0 0: Program, block erase, blank check, and lock-bit program are disabled 0 1: Program, block erase, blank check, and lock-bit program are enabled 1 0: Program, block erase, blank check, and lock-bit program are disabled 1 1: Program, block erase, blank check, and lock-bit program are disabled	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register enables or disables the following four FACI commands for the code flash memory, data flash memory, or option-setting memory: program, block erase, blank check, and lock-bit program.
This register is initialized not only by a reset but also by a transition to deep software standby mode or a transition to software standby mode.

4.2 Flash Access Status Register (FASTAT)

Address(es): 007F E010h

	b7	b6	b5	b4	b3	b2	b1	b0
	CFAE	—	—	CMDLK	DFAE	—	—	ECRCT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECRCT	Error Flag	0: No error has occurred. 1: An error has occurred.	R
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DFAE	Data Flash Memory Access Violation Flag	0: No data flash memory access violation has occurred. 1: A data flash memory access violation has occurred.	R/W*1
b4	CMDLK	Command Lock Flag	0: The flash sequencer is not in the command-locked state. 1: The flash sequencer is in the command-locked state.	R
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CFAE	Code Flash Memory Access Violation Flag	0: No code flash memory access violation has occurred. 1: A code flash memory access violation has occurred.	R/W*1

Note 1. Only 0 can be written to clear the flag after 1 is read.

This register indicates whether a code flash memory or data flash memory access violation has occurred. If either of the CFAE, and DFAE flags is 1, the CMDLK flag is set to 1 and the flash sequencer enters the command-locked state (see section 7.2, Error Protection). To release it from the command-locked state, a status clear command or forced stop command must be issued by the FACI after setting the CFAE and DFAE flags in the FASTAT register to 0.

ECRCT Flag (Error Flag)

This flag indicates that a 1-bit error has been corrected by reading of the flash memory area (with parameters for configuration set or program) or the FCURAM by the flash sequencer.
When a 2-bit error is detected in reading of the FCURAM, CMDLK is set to 1 (the flash sequencer is in the command-locked state) and the ECRCT flag does not change.
[Setting Conditions]

- When a 1-bit error has been corrected by reading of the memory area (configuration set and program parameters) by the flash sequencer.
- When a 1-bit error is corrected by reading the FCURAM

[Clearing Condition]

- When the flash sequencer starts processing of a forced stop command while the FSTATR.FRCRCT flag is 1

DFAE Flag (Data Flash Memory Access Violation Flag)

This flag indicates whether a data flash memory access violation occurred. If this flag is set to 1, the FSTATR.ILGLERR flag is set to 1, placing the flash sequencer in the command-locked state.
[Setting Conditions]

- When an FACI command is issued in data flash memory P/E mode while the setting of b18 to b0 in the FSADDR register is 1 0000h to 7 FFFFh (the reserved portion of the data area)
- When a configuration set command is issued in data flash memory P/E mode while the setting of b18 to b0 in the FSADDR register is 0 0000h to 0 003Fh, or 0 0100h to 7 FFFFh

[Clearing Condition]

- When 0 is written after reading of 1

CMDLK Flag (Command Lock Flag)

This flag indicates that the flash sequencer is in the command-locked state.

[Setting Condition]

- When the flash sequencer detects any of errors listed in Table 7.1, Error Protection Type and transitions to the command-locked state

[Clearing Condition]

- When the flash sequencer starting to process a status clear or forced stop command while the CFAE or DFAE flag in the FASTAT register is 0

CFAE Flag (Code Flash Memory Access Violation Flag)

This flag indicates whether a code flash memory access violation has occurred. If this flag is set to 1, the FSTATR.ILGLERR flag is set to 1, placing the flash sequencer in the command-locked state.

[Setting Conditions]

- When an FACI command is issued in code flash memory P/E mode while the setting of b23 to b0 in the FSADDR register is 00 0000h to BF FFFFh (the reserved portion of the user area)

[Clearing Condition]

- When 0 is written after reading of 1

4.3 Flash Access Error Interrupt Enable Register (FAEINT)

Address(es): 007F E014h

	b7	b6	b5	b4	b3	b2	b1	b0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	ECRCTIE
Value after reset:	1	0	0	1	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	ECRCTIE	Error Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.ECRCT is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.ECRCT is set to 1.	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.DFAE is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.DFAE is set to 1.	R/W
b4	CMDLKIE	Command Lock Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.CMDLK is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CMDLK is set to 1.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.CFAE is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CFAE is set to 1.	R/W

This register enables or disables generation of a flash access error (FIFERR) interrupt request.

ECRCTIE Bit (Error Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a 1-bit error has been corrected in reading of the flash memory area (with parameters for configuration set or program) or the FCURAM by the flash sequencer, leading to setting of the FASTAT.ECRCT flag to 1.

DFAEIE Bit (Data Flash Memory Access Violation Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a data flash memory access violation occurs and the FASTAT.DFAE flag is set to 1.

CMDLKIE Bit (Command Lock Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when the flash sequencer enters the command-locked state and the FASTAT.CMDLK flag is set to 1.

CFAEIE Bit (Code Flash Memory Access Violation Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a code flash memory access violation occurs and the FASTAT.CFAE flag is set to 1.

4.4 Flash Ready Interrupt Enable Register (FRDYIE)

Address(es): 007F E018h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRDYIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRDYIE	Flash Ready Interrupt Enable	0: Generation of an FRDY interrupt request is disabled. 1: Generation of an FRDY interrupt request is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register enables or disables generation of a flash ready (FRDY) interrupt request.

FRDYIE Bit (Flash Ready Interrupt Enable)

This bit is used to enable or disable generation of an FRDY interrupt request when the FASTAT.FRDY flag is changed from 0 to 1 upon completion of processing by the flash sequencer of program, block erase, or a blank check command.

4.5 FACI Command Start Address Register (FSADDR)

Address(es): 007F E030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FSADDR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSADDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description		R/W
b31 to b0	FSADDR [31:0]	Start Address for FACI Command Processing	[Command]	[Address boundary]	R/W*1
			Program (code flash memory):	256-byte	
			Program (data flash memory):	4-byte	
			Block erase (code flash memory):	8-Kbyte or 32-Kbyte	
			Block erase (data flash memory):	64-byte	
			Blank check:	4-byte	
			Configuration set:	16-byte	
			Lock-bit program:	8-Kbyte or 32-Kbyte	
			Lock-bit read:	8-Kbyte or 32-Kbyte	

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored. Note that b0 and b1 are read-only.

This register specifies the address where the target area for command processing starts when the FACI command for program, block erase, blank check, configuration set, lock-bit program, or lock-bit read is issued.
The FSADDR register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FSADDR[31:0] Bits (Start Address for FACI Command Processing)

These bits specify the start address for FACI command processing. Bits 31 to 24 are ignored in FACI command processing for the code flash memory. Bits 31 to 19 are ignored in FACI command processing for the data flash memory. Bits corresponding to address bits of lower order than the corresponding boundary listed above are also ignored.
Refer to the User's Manual: Hardware for the start addresses of the code flash memory area and data flash memory area.
See Table 6.5, Address Used by Configuration Set Command for the start address of the configuration setting area.

4.6 FACI Command End Address Register (FEADDR)

Address(es): 007F E034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FEADDR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEADDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	FEADDR [31:0]	End Address for FACI Command Processing	The end address for FACI command processing	R/W*1

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored. Note that b0 and b1 are read-only.

This register specifies the address where the target area for blank check command processing ends. When incremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 0), the address specified in the FSADDR register should be smaller than the address in the FEADDR register. Conversely, the address in the FSADDR register should be larger than the address in the FEADDR register when decremental mode is selected as the addressing mode for blank checking (i.e. when FBCCNT.BCDIR = 1). If the settings of the FBCCNT.BCDIR bit and the FSADDR and FEADDR registers are inconsistent with the above rules, the flash sequencer enters the command-locked state (see section 7.2, Error Protection).

The FEADDR register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FEADDR[31:0] Bits (End Address for FACI Command Processing)

These bits specify the end address for blank check command processing. Bits 31 to 19, 1, and 0 are ignored in command processing.

Refer to the User's Manual: Hardware for the end address of the data flash memory area.

4.7 FCURAM Enable Register (FCURAME)

Address(es): 007F E054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	FRAMTRAN	FCRME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FCRME	FCURAM Enable	0: Disables access to the FCURAM. 1: Enables access to the FCURAM.	R/W*1
b1	FRAMTRAN	FCURAM Transfer Mode	0: Normal transfer mode Both read and write access to the FCURAM are possible. 1: High-speed write mode Only high-speed write access to the FCURAM is possible.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*2

Note 1. Writing to this bit is possible only when C4h is written to the KEY bits in 16-bit units.
Note 2. Written values are not retained by these bits. These bits are read as 0.

This register enables or disables access to the FCURAM area.

FCRME Bit (FCURAM Enable)

This bit enables or disables access to the FCURAM. Clear the FENTRYR register to 0000h to stop the flash sequencer before writing to the FCURAM.

FRAMTRAN Bit (FCURAM Transfer Mode)

This bit specifies transfer mode of the FCURAM.

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the FRAMTRAN and FCRME bits.

4.8 Flash Status Register (FSTATR)

Address(es): 007F E080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	FCUERR	FLWEERR	—	—	—	—	FRDTCT	FRCRCT
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRCRCT	1-Bit Error Correction Monitor Flag	0: A 1-bit error correction has not been detected. 1: A 1-bit error correction has been detected.	R
b1	FRDTCT	2-Bit Error Detection Monitor Flag	0: A 2-bit error has not been detected. 1: A 2-bit error has been detected.	R
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	FLWEERR	Flash P/E Protection Error Flag	0: An error has not occurred. 1: An error has occurred.	R
b7	FCUERR	FCU Error Flag	0: An error has not occurred during FCU processing. 1: An error has occurred during FCU processing.	R
b8	PRGSPD	Program Suspend Status Flag	0: The flash sequencer is in a state other than those corresponding to the value 1. 1: The flash sequencer is in the program suspend processing state or the program-suspended state.	R
b9	ERSSPD	Erase Suspend Status Flag	0: The flash sequencer is in a state other than those corresponding to the value 1. 1: The flash sequencer is in the erase suspend processing state or the erase-suspended state.	R
b10	DBFULL	Data Buffer Full Flag	0: The data buffer is empty. 1: The data buffer is full.	R
b11	SUSRDY	Suspend Ready Flag	0: The flash sequencer cannot receive P/E suspend commands. 1: The flash sequencer can receive P/E suspend commands.	R
b12	PRGERR	Program Error Flag	0: Program operation has been completed successfully. 1: An error has occurred during program operation.	R
b13	ERSERR	Erase Error Flag	0: Erase operation has been completed successfully. 1: An error has occurred during erase operation.	R
b14	ILGLERR	Illegal Command Error Flag	0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access. 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	R
b15	FRDY	Flash Ready Flag	0: Program, block erase, P/E suspend, P/E resume, forced stop, blank check, configuration set, lock-bit program, or lock-bit read command processing is in progress. 1: None of the above is in progress.	R
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register indicates the state of the flash sequencer.

FRCRCT Flag (1-Bit Error Correction Monitor Flag)

This flag indicates that a 1-bit error has been corrected by reading FCURAM by the FCU. When the FRCRCT flag is 1, the flash sequencer is not in the command-locked state.
[Clearing Condition]

- When the flash sequencer starts processing of a forced stop command

When this flag is 1, issue a forced stop command and initialize the FCU, and then reload the FCU firmware into the FCURAM.

FRDTCT Flag (2-Bit Error Detection Monitor Flag)

This flag indicates that a 2-bit error has been detected by reading FCURAM by the FCU. When the FRDTCT flag is 1, the flash sequencer is in the command-locked state.
[Clearing Condition]

- When the flash sequencer starts processing of a forced stop command

When this flag is 1, issue a forced stop command and initialize the FCU, and then reload the FCU firmware into the FCURAM.

FLWEERR Flag (Flash P/E Protection Error Flag)

This flag indicates a violation of the flash memory program/erase protection setting in the FWEPROR register. When this flag is 1, the flash sequencer is in the command-locked state.
[Clearing Condition]

- When the flash sequencer starts processing of a forced stop command

FCUERR Flag (FCU Error Flag)

This flag indicates that an error has occurred during FCU processing. When this flag is 1, the flash sequencer transitions to the command-locked state.
[Clearing Condition]

- When the flash sequencer starts processing of a forced stop command

When this flag is 1, issue a forced stop command and initialize the FCU, and then reload the FCU firmware into the FCURAM.

PRGSPD Flag (Program Suspend Status Flag)

This flag indicates that the flash sequencer is in the processing of program suspend or has transitioned to the program-suspended state.
[Setting Condition]

- When the flash sequencer starts processing in response to a program suspend command

[Clearing Conditions]

- When the flash sequencer has received a P/E resume command
  (after write access to the FACI command-issuing area is completed)
- When the flash sequencer starts processing of a forced stop command

ERSSPD Flag (Erase Suspend Status Flag)

This flag indicates that the flash sequencer is the processing of erase suspend or has transitioned to the erase-suspended state.
[Setting Condition]

- When the flash sequencer starts processing in response to an erase suspend command

[Clearing Conditions]

- Reception of the P/E resume command by the flash sequencer
  (after write access to the FACI command-issuing area is completed)
- When the flash sequencer starts processing of a forced stop command

DBFULL Flag (Data Buffer Full Flag)

This flag indicates the state of the data buffer when a program command is issued. The FACI incorporates a buffer for write data (data buffer). When data for writing to the flash memory are issued to the FACI command-issuing area while the data buffer is full, the FACI inserts a wait cycle in the peripheral bus 6.

[Setting Condition]

- When the data buffer becomes full while a program command is being issued

[Clearing Condition]

- When the data buffer becomes empty

SUSRDY Flag (Suspend Ready Flag)

This flag indicates whether the flash sequencer can receive a P/E suspend command.

[Setting Condition]

- When the flash sequencer is ready to accept the P/E suspend command after the program or erase sequence has started

[Clearing Conditions]

- When the flash sequencer has accepted the P/E suspend command or forced stop command (after write access to the FACI command-issuing area is completed)
- When the flash sequencer enters the command-locked state during programming or erasure
- When programming or erasure has been completed

PRGERR Flag (Program Error Flag)

This flag indicates the result of programming the flash memory. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting Conditions]

- When an error occurs during programming
- When a program or lock-bit program command is issued for an area where the lock bit setting is for protection

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

ERSERR Flag (Erase Error Flag)

This flag indicates the result of erasing the flash memory. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting Conditions]

- When an error has occurred during erasure
- When a block erase command is issued for an area where the lock bit setting is for protection

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

ILGLERR Flag (Illegal Command Error Flag)

This flag indicates that the flash sequencer has detected an illegal FACI command or flash memory access. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting Conditions] (See section 7.2, Error Protection)

- When the flash sequencer has detected an illegal command
- When the flash sequencer has detected illegal flash memory access
- When the setting of the FENTRYR register is invalid

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command while the DFAE and CFAE flag in the FASTAT register is 0

If the flash sequencer completes processing of a status clear or forced stop command while the CFAE or DFAE flag in the FASTAT register is 1, this flag is set to 1. This flag is temporarily set to 0 during processing of a forced stop command, and is re-set to 1 when the CFAE or DFAE flag is detected as 1 upon completion of command processing.

FRDY Flag (Flash Ready Flag)

This flag indicates the command processing state of the flash sequencer.

[Setting Conditions]

- When the flash sequencer completes command processing
- When the flash sequencer receives a P/E suspend command and suspends programming/erasure of the flash memory
- When the flash sequencer has received a forced stop command and ended command processing

[Clearing Conditions]

- When the flash sequencer receives the FACI command of the setting of the program and configuration and after the first write access is made to the FACI command-issuing area
- When the flash sequencer receives any FACI command other than of the setting of the program and configuration and after the last write access is made to the FACI command issuing area

4.9 Flash P/E Mode Entry Register (FENTRYR)

Address(es): 007F E084h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRYC	Code Flash Memory P/E Mode Entry	0: Code flash memory is in read mode. 1: Code flash memory is in P/E mode.	R/W*1, *2
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	Data Flash Memory P/E Mode Entry	0: Data flash memory is in read mode. 1: Data flash memory is in P/E mode.	R/W*1, *2
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored.
Note 2. Writing to this bit is possible only when AAh is written to the KEY bits in 16-bit units.
Note 3. Written values are not retained by these bits. These bits are read as 0.

This register is used to specify code flash memory P/E mode and data flash memory P/E mode. To specify code flash memory P/E mode or data flash memory P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.
Note that writing AA81h in this register causes the FSTATR.ILGLERR flag to be set to 1, and the flash sequencer to enter the command-locked state.
The FENTRYR register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FENTRYC Bit (Code Flash Memory P/E Mode Entry)

This bit specifies the P/E mode for code flash memory.
[Setting Condition]

- When 1 is written to the FENTRYC bit while writing to the FENTRYR register is enabled and the FENTRYR register is 0000h

[Clearing Conditions]

- When the FENTRYR register is accessed in 8-bit units while the FSTATR.FRDY flag is 1
- When a value other than AAh is specified in the KEY bits and the FENTRYR register is accessed in 16-bit units while the FSTATR.FRDY flag is 1
- When 0 is written to the FENTRYC bit while writing to the FENTRYR register is enabled
- When the FENTRYR register is written while writing to the FENTRYR register is enabled and the value of the FENTRYR register is other than 0000h

FENTRYD Bit (Data Flash Memory P/E Mode Entry)

This bit specifies the P/E mode for data flash memory.
[Setting Condition]

- When 1 is written to the FENTRYR.FENTRYD bit while writing to the FENTRYR register is enabled and the FENTRYR register is 0000h

[Clearing Conditions]

- When the FENTRYR register is written in 8-bit units while the FSTATR.FRDY flag is 1
- When a value other than AAh is specified for the KEY bits while the FSTATR.FRDY flag is 1, and the FENTRYR register is written in 16-bit units

- When 0 is written to the FENTRYD bit while writing to the FENTRYR register is enabled
- When the FENTRYR register is written while writing to FENTRYR register is enabled and the value of the FENTRYR register is other than 0000h

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the FENTRYD and FENTRYC bits.

4.10 Flash Protection Register (FPROTR)

Address(es): 007F E088h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	FPROTCN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FPROTCN	Lock Bit Protection Cancel	0: Enables protection by the lock bits. 1: Disables protection by the lock bits.	R/W*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*2

Note 1. Writing to this bit is possible only when 55h is written to the KEY bits in 16-bit units.
Note 2. Written values are not retained by these bits. These bits are read as 0.

This register enables or disables protection by the lock bits of the code flash memory against programming and erasure. The register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FPROTCN Bit (Lock Bit Protection Cancel)

This bit enables or disables protection by the lock bits of the code flash memory against programming and erasure.

[Setting Condition]

- When 1 is written to the FPROTCN bit while writing to the FPROTR register is enabled and the value of the FENTRYR register is other than 0000h

[Clearing Conditions]

- When the FPROTR register is written in 8-bit units
- When a value other than 55h specified for the KEY bits and the FPROTR register is written in 16-bit units
- When 0 is written to the FPROTRCN bit while writing to the FPROTR register is enabled
- When the value of FENTRYR is 0000h

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the FPROTCN bit.

4.11 Flash Sequencer Set-Up Initialization Register (FSUINITR)

Address(es): 007F E08Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SUINIT	Set-Up Initialization	0: The FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers keep their current values. 1: The FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.	R/W*1, *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored.
Note 2. Writing to these bits is possible only when 2Dh is written to the KEY bits in 16-bit units.
Note 3. Written values are not retained by these bits. This bit is read as 0.

This register is used for initialization of the flash sequencer set-up.

SUINIT Bit (Set-Up Initialization)

This bit initializes the following flash sequencer set-up registers.

- FEADDR
- FPROTR
- FCPSR
- FSADDR
- FENTRYR
- FBCCNT

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the SUINIT bit.

4.12 Lock Bit Status Register (FLKSTAT)

Address(es): 007F E090h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FLOCKST
Value after reset:	0	0	0	0	0	0	0	0

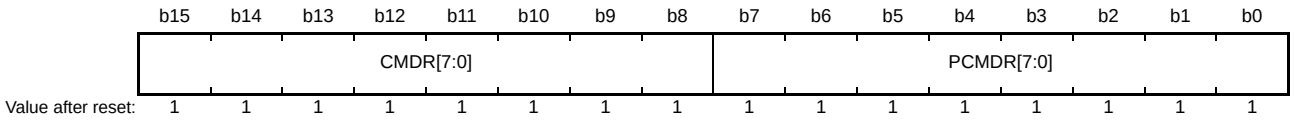
Bit	Symbol	Bit Name	Description	R/W
b0	FLOCKST	Lock Bit Status Flag	0: Protected state 1: Non-protected state	R
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FLOCKST Flag (Lock Bit Status Flag)

This flag reflects the value of the lock bit as read by executing a lock-bit read command. When the FSTATR.FRDY flag becomes 1 after the lock-bit read command is issued, the value of the target lock bit is stored in the FLOCKST flag. The value of the FLOCKST flag is retained until the next lock-bit read command is completed.

4.13 FACI Command Register (FCMDR)

Address(es): 007F E0A0h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCMDR[7:0]	Precommand Flag	The command immediately before the latest command is stored.	R
b15 to b8	CMDR[7:0]	Command Flag	The latest command is stored.	R

This register records the two most recent commands accepted by the FACI.

PCMDR[7:0] Flags (Precommand Flag)

These flags indicate the command received immediately before the last command received by the FACI.

CMDR[7:0] Flags (Command Flag)

These flags indicate the latest command received by the FACI.

Table 4.2 States of FCMDR after Receiving Commands

Command	CMDR	PCMDR
Program	E8h	Previous command
Block erase	D0h	20h
P/E suspend	B0h	Previous command
P/E resume	D0h	Previous command
Status clear	50h	Previous command
Forced stop	B3h	Previous command
Blank check	D0h	71h
Configuration set	40h	Previous command
Lock-bit program	D0h	77h
Lock-bit read	D0h	71h

4.14 Flash P/E Status Register (FPESTAT)

Address(es): 007F E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PEERRST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PEERRST [7:0]	P/E Error Status Flag	00h: No error 01h: Program error due to an area protected by its lock bit 02h: Program error for reasons other than lock-bit protection 11h: Erase error due to an area protected by its lock bit 12h: Erase error for reasons other than lock-bit protection	R
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register indicates the result of programming or erasing the flash memory.

PEERRST[7:0] Flags (P/E Error Status Flag)

These flags indicate the source of an error that occurred during processing for the programming or erasure of the code flash memory or data flash memory. The value of these flags is only valid if the ERSERR or PRGERR flag in the FSTATR register is 1 when the FSTATR.FRDY flag becomes 1. When the ERSERR and PRGERR flags are 0, these flags retain their value to indicate the source of the last error to have occurred.

4.15 Data Flash Blank Check Control Register (FBCCNT)

Address(es): 007F E0D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCDIR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCDIR	Blank Check Direction	0: Blank checking is executed from lower addresses to higher addresses (incremental mode). 1: Blank checking is executed from higher addresses to lower addresses (decremental mode).	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register specifies the addressing mode in processing of a blank check command.
The register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

BCDIR Bit (Blank Check Direction)

This bit specifies the addressing mode for blank checking.

4.16 Data Flash Blank Check Status Register (FBCSTAT)

Address(es): 007F E0D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCST	Blank Check Status Flag	0: The target area is in the non-programmed state (i.e. is blank; the area has been erased but has not yet been re-programmed). 1: The target area has been programmed with 0s or 1s.	R
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register stores the results of checking in response to a blank check command.

BCST Flag (Blank Check Status Flag)

This flag indicates the results of checking in response to a blank check command.
At the point where the FSTATR.FRDY flag is set to 1, the valid data is stored in the BCST flag.

4.17 Data Flash Programming Start Address Register (FPSADDR)

Address(es): 007F E0D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[18:16]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSADR[15:0]															
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b18 to b0	PSADR[18:0]	Programmed Area Start Address	The starting address of the programmed area to be found firstly	R
b31 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register indicates the starting address of the programmed area to be found firstly in processing of a blank check command.

PSADR[18:0] Bits (Programmed Area Start Address)

These bits indicate the starting address of the programmed area to be found firstly in processing of a blank check command. The address is an offset from the address where the data flash memory starts. The setting of these bits is valid only while the FBCSTAT.BCST flag is 1 and when the FSTATR.FRDY flag becomes 1. When the FBCSTAT.BCST flag is 0, the PSADR bit holds the address detected by the previous check.

4.18 Flash Sequencer Processing Switching Register (FCPSR)

Address(es): 007F E0E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESUSPMD	Erase Suspend Mode	0: Suspend priority mode 1: Erase priority mode	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is for selecting the erase suspend mode.
The register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

ESUSPMD Bit (Erase Suspend Mode)

This bit is for selecting the erase suspend mode when a P/E suspend command is issued while the flash sequencer is executing erase processing (see section 6.3.10, P/E Suspend Command). This bit should be set before issuing a block erase command.

4.19 Flash Sequencer Processing Clock Frequency Notification Register (FPCKAR)

Address(es): 007F E0E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								PCKA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCKA[7:0]	Flash Sequencer Operating Clock Frequency Notification	These bits are used to set the frequency of the FlashIF clock (FCLK) and notify the flash sequencer of the frequency used	R/W*1, *2
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored.
Note 2. Writing to these bits is possible only when 1Eh is written to the KEY[7:0] bits in 16-bit units.
Note 3. Written values are not retained by these bits. These bits are read as 0.

This register specifies the frequency of the FlashIF clock (FCLK) generated in the clock generator and notifies the flash sequencer of the frequency used. The flash sequencer determines the FACI command processing time based on the frequency notified by the FPCKAR register. The initial value is set to the maximum operating frequency of the FCLK.

PCKA[7:0] Bits (Flash Sequencer Operating Clock Frequency Notification)

These bits are used to specify the frequency of the FCLK generated in the clock generator and to notify the flash sequencer of the frequency used. Set the desired frequency in these bits before issuing an FACI command. Specifically, convert the frequency represented in MHz into a binary number and set it in these bits.

Example: When frequency is 35.9 MHz (PCKA[7:0] = 24h)
Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number.

If the value set in these bits is smaller than the frequency of the FCLK, the rewriting characteristics of the flash memory cannot be guaranteed. Conversely, if the value set in these bits is greater than the frequency of the FCLK, the rewriting characteristics of the flash memory can be guaranteed although the FACI command processing time such as time for rewriting will increase (the FACI command processing time becomes the shortest when the frequency of the FCLK is the same as the value set in the bits).

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the PCKA[7:0] bits.

5. Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in Figure 5.1. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the value of the FENTRYR register is 0000h, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and data flash memory are readable.

When the value of the FENTRYR register is 0001h, the flash sequencer is in code flash memory P/E mode where the code flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. In addition, the code flash memory is not readable when background operation (BGO) is disabled. When BGO is enabled, the code flash memory is readable. As for the conditions for enabling BGO, refer to the User's Manual: Hardware.

When the value of the FENTRYR register is 0080h, the flash sequencer is in data flash memory P/E mode where the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

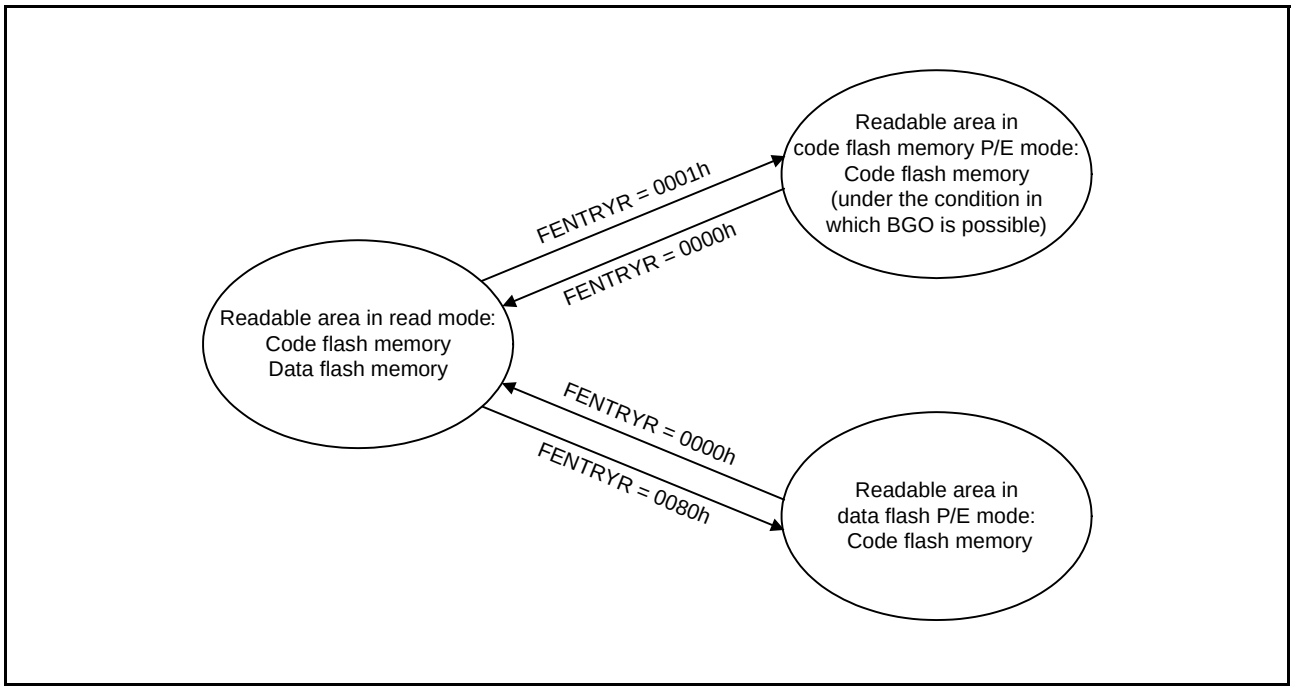


Figure 5.1 Modes of the Flash Sequencer

6. FACI Commands

6.1 List of FACI Commands

Table 6.1 List of FACI Commands

FACI Command	Description
Program	This is used to program the user area and data area. Units of programming are 256 bytes for the user area and 4 bytes for the data area.
Block erase	This is used to erase the user area, lock bits, or data area. The unit of erasure is one block.
P/E suspend	This suspends programming or erasure processing.
P/E resume	This resumes suspended programming or erasure processing.
Status clear	This initializes the ILGLERR, ERSERR, and PRGERR flags in the FSTATR register and releases the flash sequencer from the command-locked state.
Forced stop	This forcibly stops processing of FACI commands and initializes the FSTATR register.
Blank check	This is used to check if data areas are blank. Units of blank checking: 4 bytes to 64 Kbytes (specified in 4-byte units).
Configuration set	This is used to set the ID, security function, option-setting memory, and trusted memory (TM) function. Units of setting: 16 bytes.
Lock-bit program	This is used to program the lock bit for a user area. Units of programming: 1 bit (the lock bit for one block)
Lock-bit read	The lock bit for a user area is read and the result is stored in the FLKSTAT register. Units of reading: 1 bit (the lock bit for one block)

The FACI commands are issued by writing to the FACI command-issuing area (see Table 3.1). When write access as shown in Table 6.2 proceeds in the specified state, the flash sequencer executes the processing corresponding to the given command (see section 6.2, Relationship between the Flash Sequencer State and FACI Commands).

Table 6.2 FACI Command Formats

FACI Commands	Number of Write Access	Data to be Written to the FACI Command-Issuing Area			
		1st Access	2nd Access	3rd to (N+2)th Access	(N+3)th Access
Program (user area) 256-byte programming, N = 128	131	E8h	80h (= N)	WD_1 to WD_{128}	D0h
Program (data area) 4-byte programming: N = 2	N + 3	E8h	02h (= N)	WD_1 to WD_N	D0h
Block erase	2	20h	D0h	—	—
P/E suspend	1	B0h	—	—	—
P/E resume	1	D0h	—	—	—
Status clear	1	50h	—	—	—
Forced stop	1	B3h	—	—	—
Blank check	2	71h	D0h	—	—
Configuration set N = 8	11	40h	08h (= N)	WD_1 to WD_8	D0h
Lock-bit program	2	77h	D0h	—	—
Lock-bit read	2	71h	D0h	—	—

Note: WD_N (N = 1, 2,…): Nth 16-bit data to be programmed.

The flash sequencer clears the FSTATR.FRDY flag to 0 at the start of processing of a command other than the status clear command and sets this bit to 1 upon completion of command processing.
When the setting of the FRDYIE.FRDYIE bit is 1 and when the FSTATR.FRDY flag is set to 1, a flash ready (FRDY) interrupt is generated.

6.2 Relationship between the Flash Sequencer State and FACI Commands

Each FACI command can be accepted in a specific mode or state of the flash sequencer. FACI commands should be issued after the transition of the flash sequencer to the code flash memory P/E mode or data flash memory P/E mode and checking of the state of the flash sequencer. Use the FSTATR and FASTAT registers to check the state of the flash sequencer. In addition, the occurrence of errors in general can be checked by reading the FASTAT.CMDLK flag; its value is the logical OR of the ILGLERR, ERSERR, PRGERR, FCUERR, FRDTCT, and FLWEERR flags in the FSTATR register and the CFAE and DFAE flags in the FASTAT register.
Table 6.3 lists the available commands in each operating mode.

Table 6.3 Operating Mode and Available Commands

Operating Mode	FENTRYR Register Value	Available Commands
Read mode	0000h	None
Code flash memory P/E mode	0001h	Program Block erase P/E suspend P/E resume Status clear Forced stop Lock-bit program Lock-bit read
Data flash memory P/E mode	0080h	Program Block erase P/E suspend P/E resume Status clear Forced stop Blank check Configuration set

Table 6.4 shows the state of the flash sequencer and acceptable FACI commands. An appropriate mode is assumed to be set before the commands are executed.

Table 6.4 Acceptable FACI Commands and the State of the Flash Sequencer

	Processing of Programming or Erasure*5	Processing of Configuration Setting	Processing to Suspend Programming or Erasure	Blank checking or lock bit reading	Programming Suspended	Erasure Suspended	Programming while Erasure is Suspended	Command-Locked State (FRDY = 1)	Command-Locked State (FRDY = 0)	Lock-Bit Programming	Processing of Forced Stop Command	Other State
FRDY flag	0	0	0	0	1	1	0	1	0	0	0	1
SUSRDY flag	1	0	0	0	0	0	0	0	0	0	0	0
ERSSPD flag	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0	0
PRGSPD flag	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0	0
CMDLK flag	0	0	0	0	0	0	0	1	1	0	0	0
Program	×	×	×	×	×	✓ *3	×	×	×	×	×	✓
Block erase	×	×	×	×	×	×	×	×	×	×	×	✓
P/E suspend	✓	×	×	×	×	×	×	—	×	×	×	—
P/E resume	×	×	×	×	✓	✓	×	×	×	×	×	×
Status clear	×	×	×	×	✓	✓	×	✓	×	×	×	✓
Forced stop	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Blank check	×	×	×	×	✓ *1	✓ *1	×	×	×	×	×	✓ *1
Configuration set	×	×	×	×	×	×	×	×	×	×	×	✓ *1
Lock-bit program	×	×	×	×	×	×	×	×	×	×	×	✓ *2
Lock-bit read	×	×	×	×	✓ *2	✓ *2, *4	×	×	×	×	×	✓ *2

✓: Acceptable

×: Not acceptable (the sequencer in the command-locked state)

—: Ignored

Note 1. Acceptable only in data flash memory P/E mode

Note 2. Acceptable only in code flash memory P/E mode

Note 3. Program command can be issued to a block other than the erase-suspended block.

Note 4. The value read out is undefined when a lock-bit read command is issued for a block where erasure was suspended.

Note 5. Cases that the programming or erasure processing is completed while the P/E suspend command is accepted are also included.

6.3 Usage of FACI Commands

This section gives an overview of the usage of FACI commands.

6.3.1 Overview of Command Usage in Code Flash memory P/E Mode

Figure 6.1 and Figure 6.2 respectively show an overview of FACI command usage in code flash memory P/E mode for products in which background operation (BGO) is possible and that for products in which BGO is not possible. For which commands are available in code flash memory P/E mode, see Table 6.3.

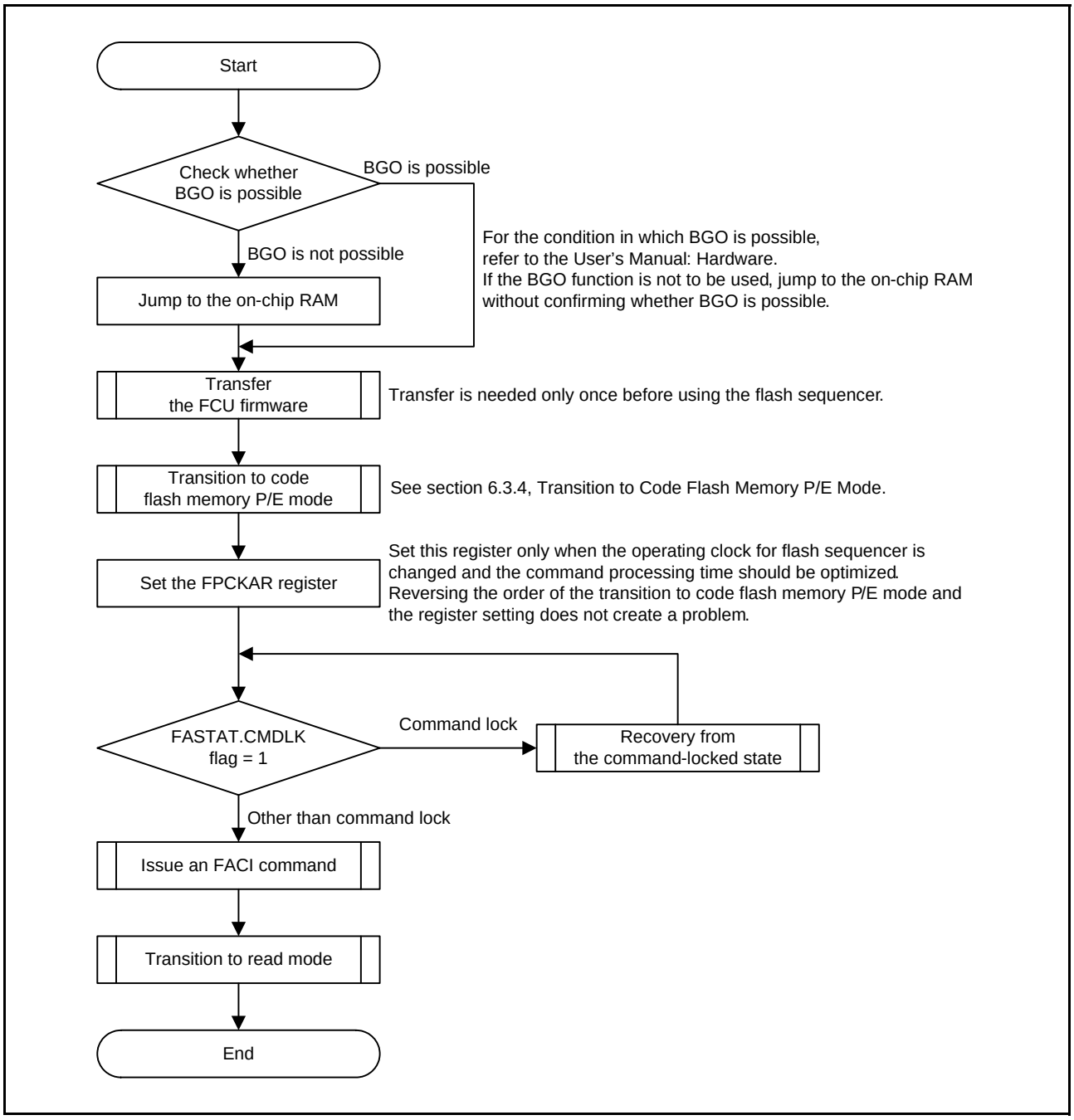


Figure 6.1 Overview of Command Usage in Code Flash Memory P/E Mode (for products in which BGO is possible)

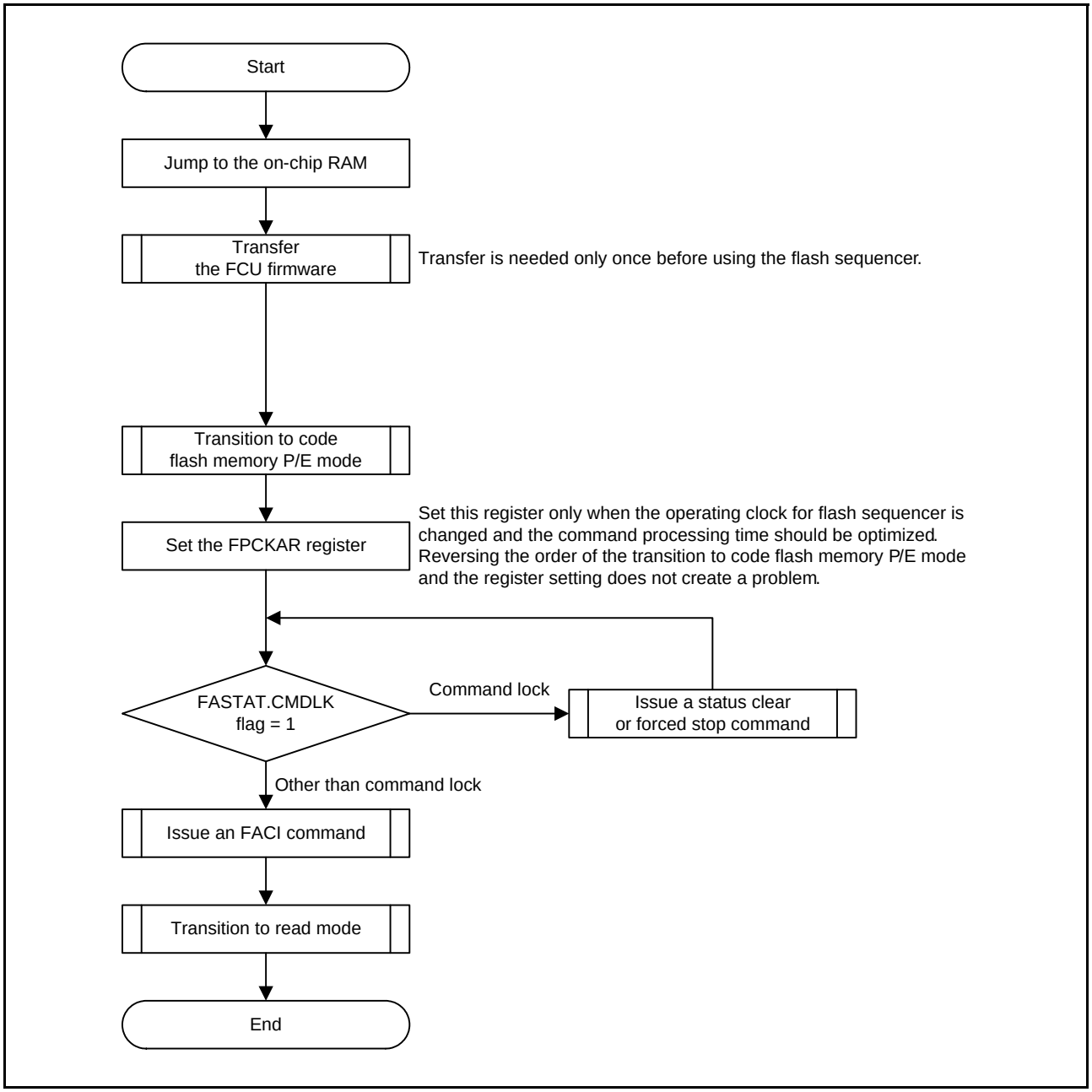


Figure 6.2 Overview of Command Usage in Code Flash Memory P/E Mode (for products in which BGO is not possible)

6.3.2 Overview of Command Usage in Data Flash Memory P/E Mode

An overview of FACI command usage in data flash memory P/E mode is shown below. For which commands are available in data flash memory P/E mode, see Table 6.3.

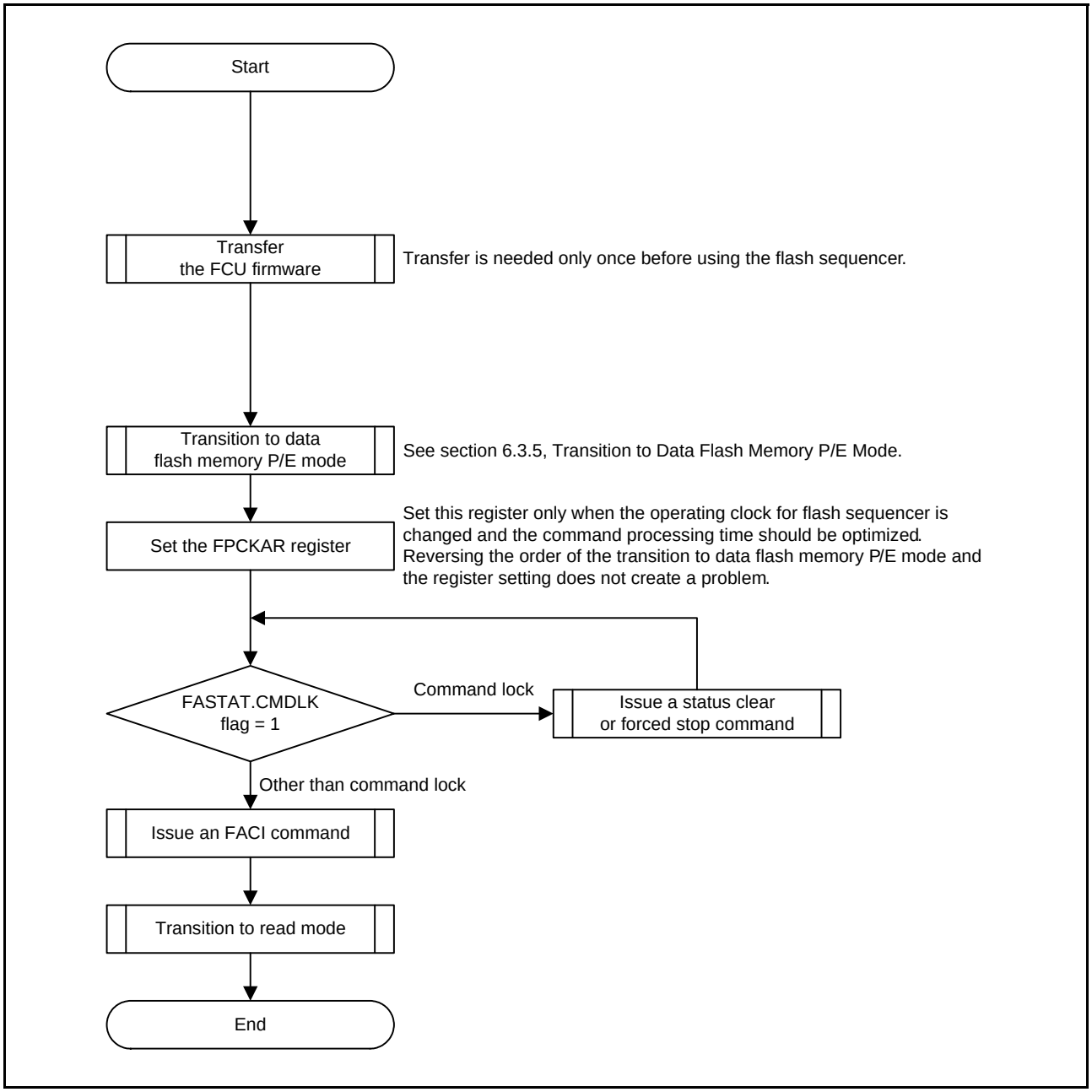


Figure 6.3 Overview of Command Usage in Data Flash Memory P/E Mode

6.3.3 Transferring the FCU Firmware

The flash sequencer can only be used when the firmware for the FCU is stored in the FCURAM. The FCURAM does not hold the FCU firmware immediately after the chip has been booted up, so the firmware must be copied from the FCU firmware storage area to the FCURAM. Since execution of the FACI command does not update the FCURAM, if the FCU firmware is copied only once before using the flash sequencer, re-updating of the FCURAM is not required.
As data stored in the FCURAM are undefined at boot up, writing to the FCURAM will lead to an ECC error. After copying the FCU firmware, issue a forced stop command and then initialize the FRCRCT and FRDTCT flags in the FSTATR register.
All processing of a forced stop command can be executed by hardware without intervention by the FCU firmware.

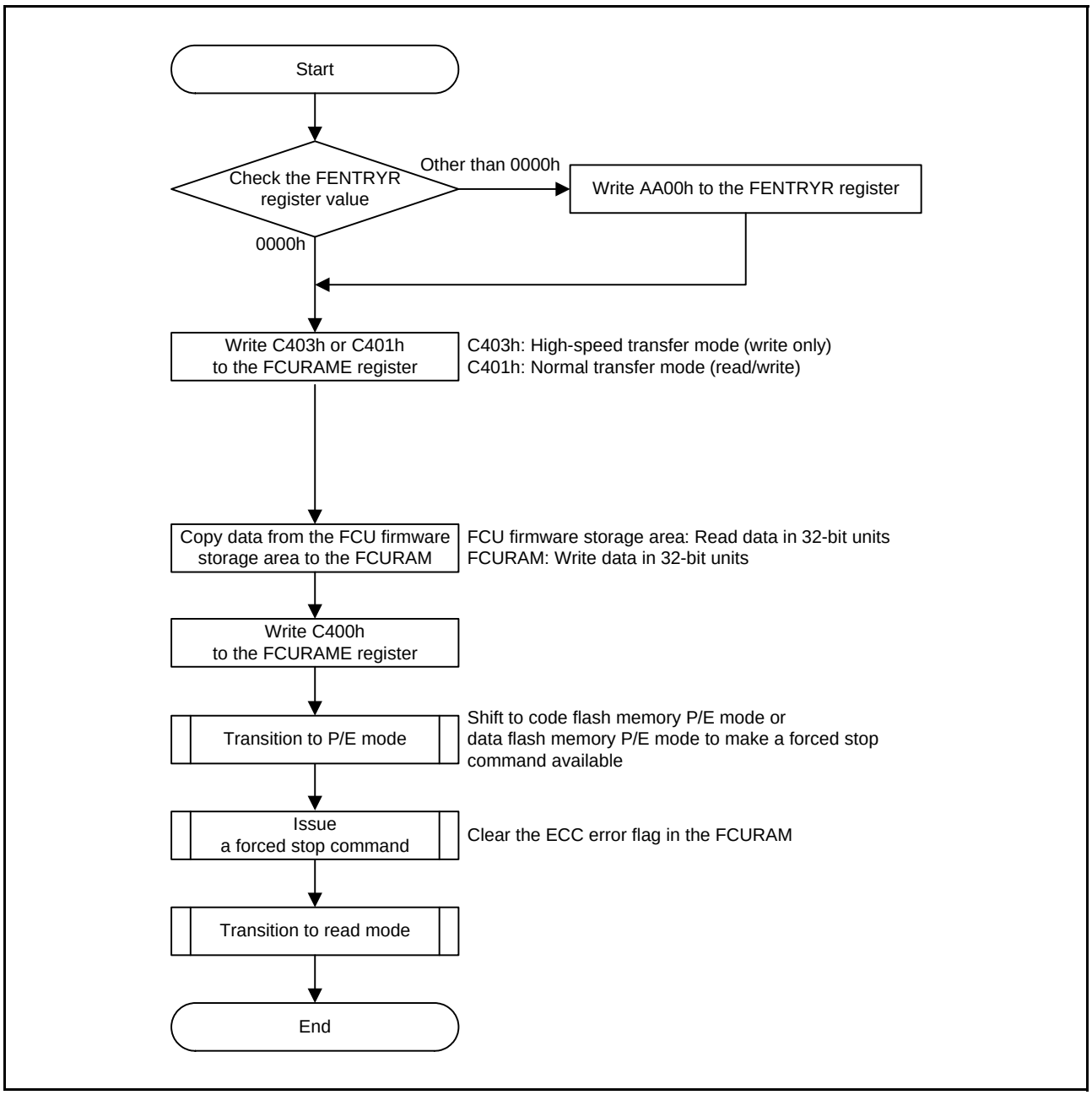


Figure 6.4 Flow for Transferring the FCU Firmware

6.3.4 Transition to Code Flash Memory P/E Mode

To use the FACI commands for the code flash memory, a transition to code flash memory P/E mode is required. To cause shift to code flash memory P/E mode, set the FENTRYR.FENTRYRC bit to 1.

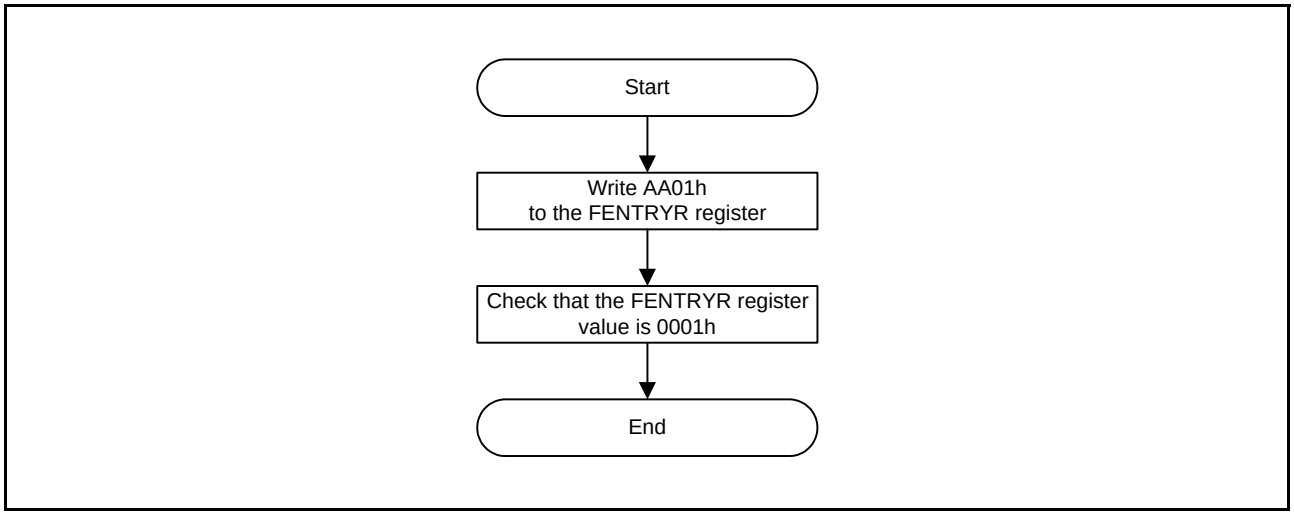


Figure 6.5 Procedure for Transition to Code Flash Memory P/E Mode

6.3.5 Transition to Data Flash Memory P/E Mode

To use the FACI commands for the data flash memory, a transition to data flash memory P/E mode is required. To shift to data flash memory P/E mode, set the FENTRYR.FENTRYRD bit to 1.

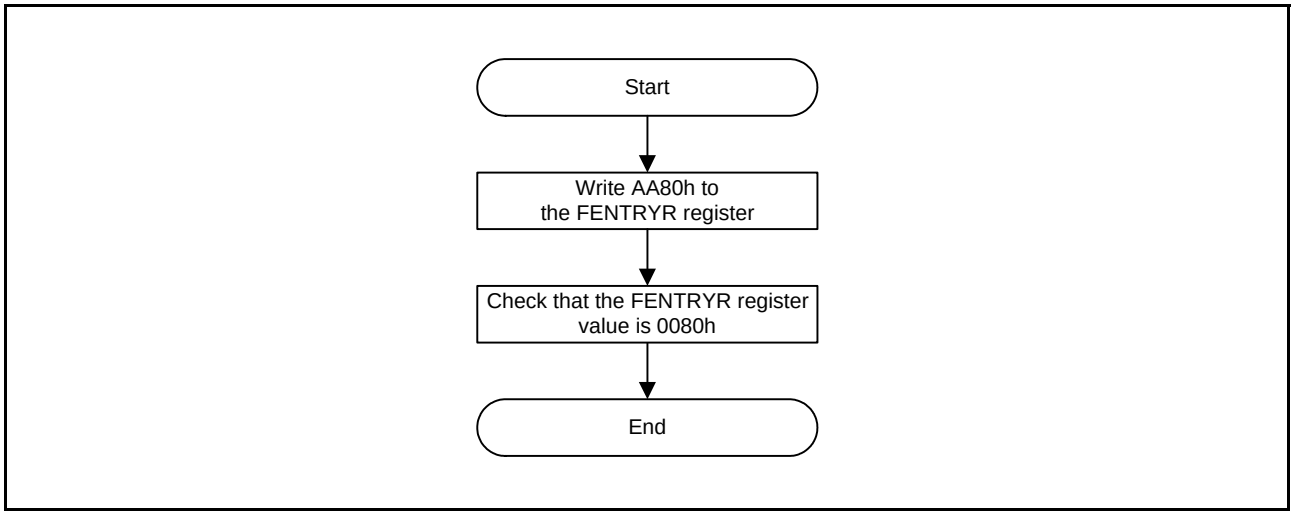
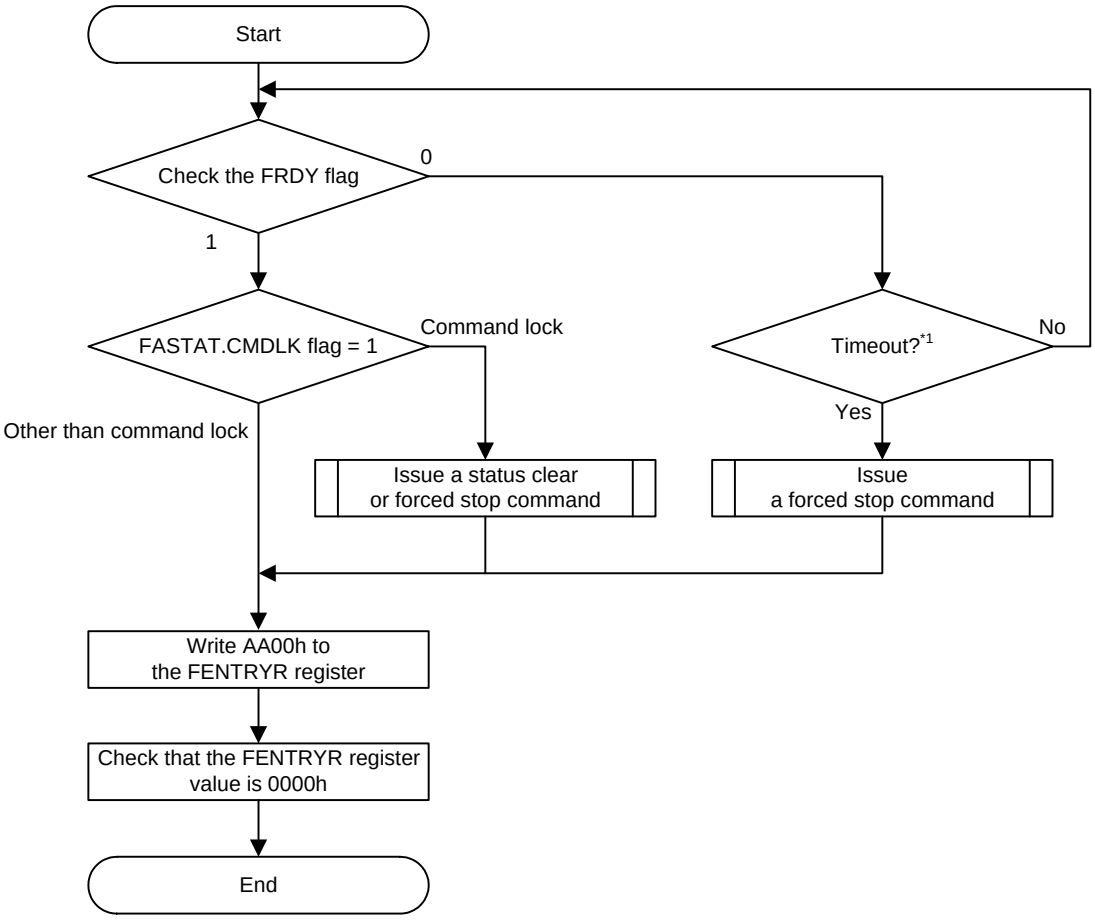


Figure 6.6 Procedure for Transition to Data Flash Memory P/E Mode

6.3.6 Transition to Read Mode

To read the flash memory without using the BGO function, a transition to read mode is required. To shift to read mode, set the FENTRYR register to 0000h. The transition to read mode should be made after processing by the flash sequencer is completed and while operation is in other than in the command-locked state.

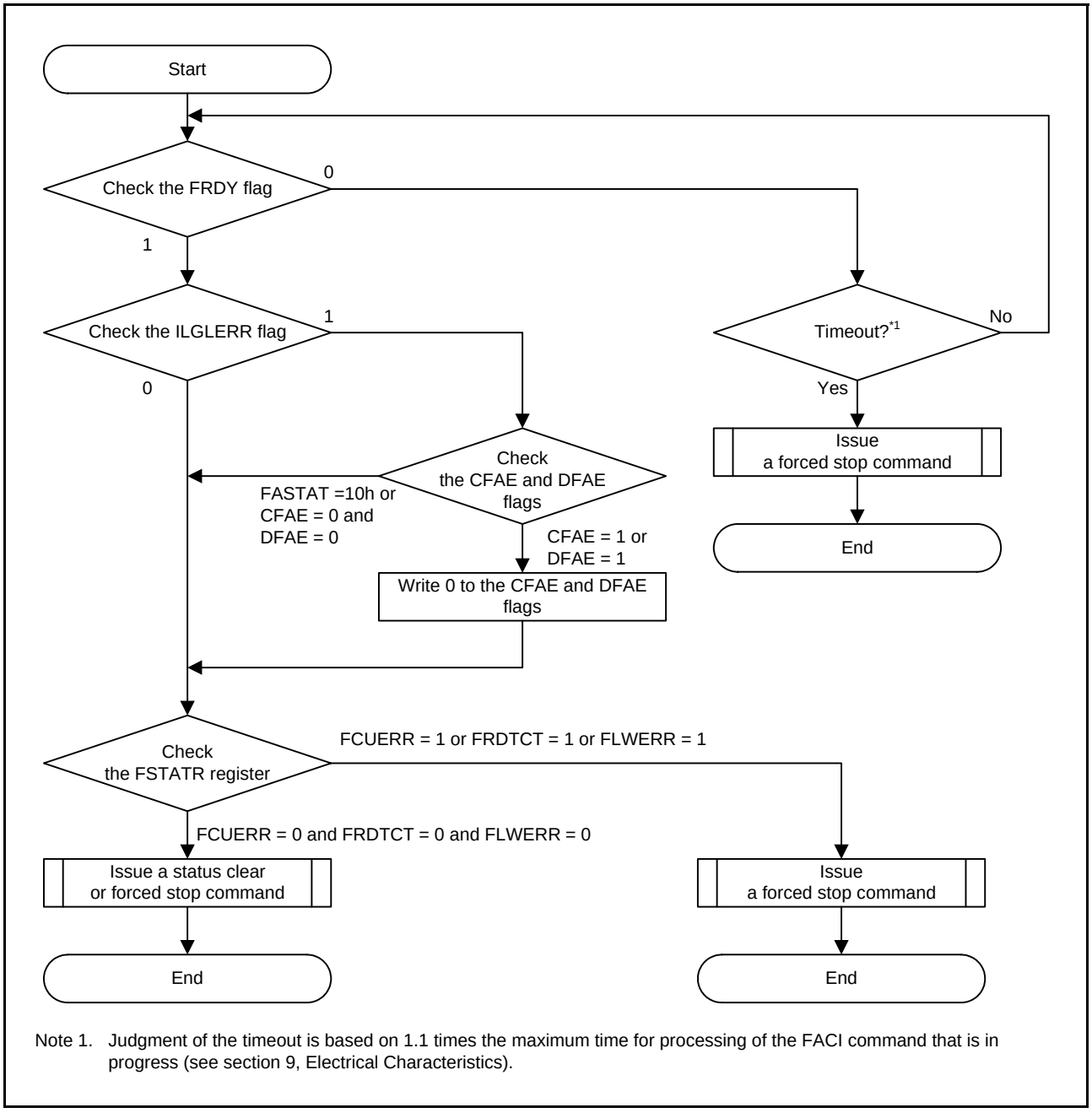


Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 9, Electrical Characteristics).

Figure 6.7 Procedure for Transition to Read Mode

6.3.7 Recovery from the Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the sequencer from the command-locked state, use the status clear command, forced stop command, or FASTAT register.
When the command-locked state is detected by checking for an error before issuing the P/E suspend command, the FSTATR.FRDY flag may hold 0 as the command processing has not been completed. If processing is not completed within the maximum program/erase time specified in the User's Manual: Hardware, this can be considered a timeout, and the flash sequencer should be stopped by the forced stop command.
When the FSTATR.ILGLERR flag is 1, check the FASTAT value. If the CFAE or DFAE flag in the FASTAT register is 1, set the CFAE or DFAE flag in the FASTAT register to 0 and then issue the status clear and forced stop commands.
The FCUERR, FRDTCT, and FLWERR flags in the FSTATR register are not changed from 1 to 0 by the status clear command. When these bits are set to 1, use the forced stop command for release from the command-locked state. The other bits that indicate the command-locked state can be changed from 1 to 0 by the status clear or forced stop command.

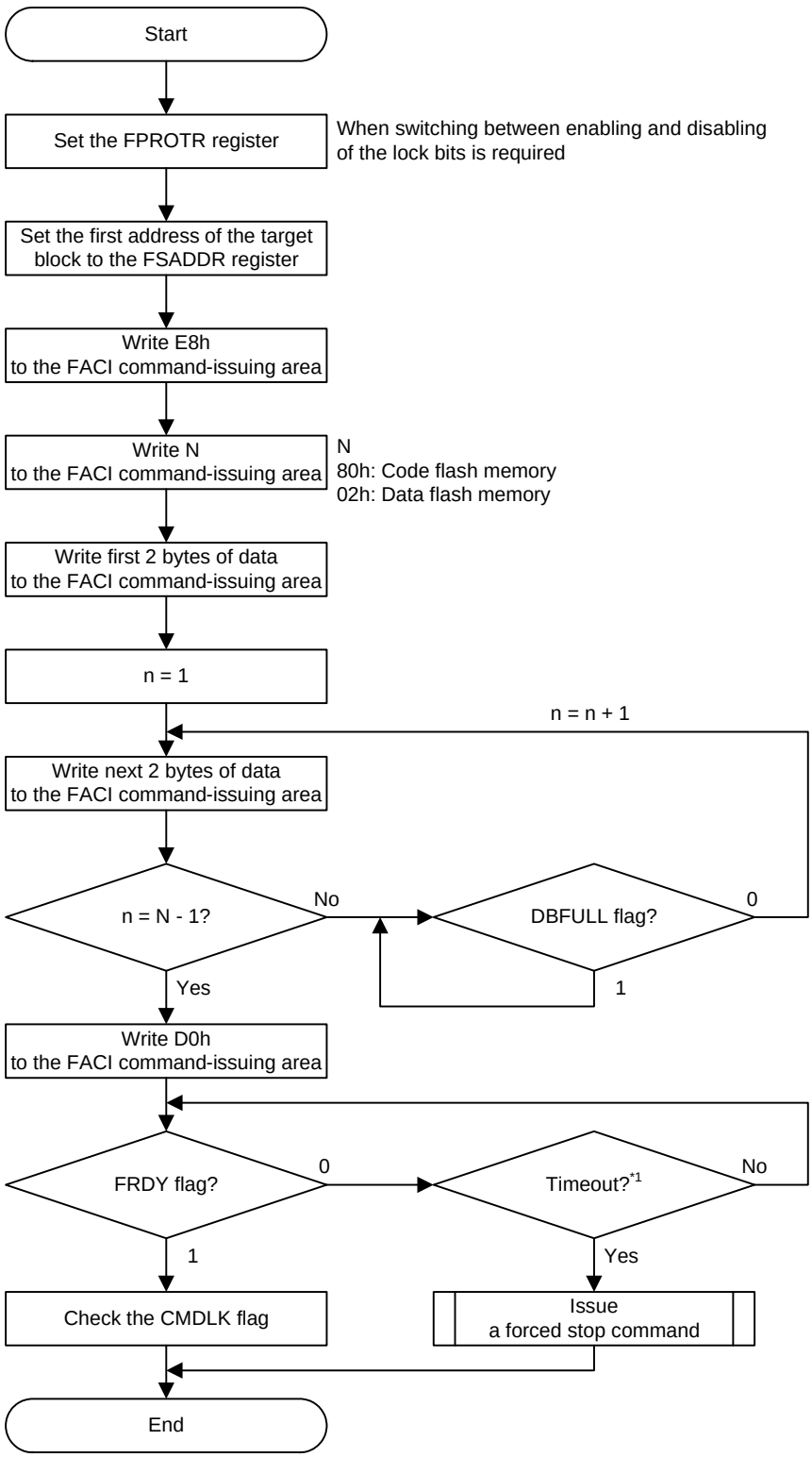


Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 9, Electrical Characteristics).

Figure 6.8 Recovery from the Command-Locked State

6.3.8 Program Command

A program command is used for writing to the user area and data area.
Before issuing a program command, set the first address of the target block in the FSADDR register.
Writing D0h to the FACI command-issuing area at the final access of the FACI command-issuing starts the program command processing. If the target area of program command processing contains the area not for writing, write FFFFh to the corresponding area.
The FPROTR register must be set before issuing a program command. To switch between enabling and disabling of the lock bits, the setting of the FPROTR register must be changed.
Issuing a program command consecutively while the FACI internal data buffer is full leads to a wait on the peripheral bus 6 and this may affect on the bus accesses of the other peripheral IP modules. To avoid the generation of such a wait, issue an FACI command while the FSTATR.DBFULL flag is 0.
Writing to the data area will not lead to the data buffer becoming full.

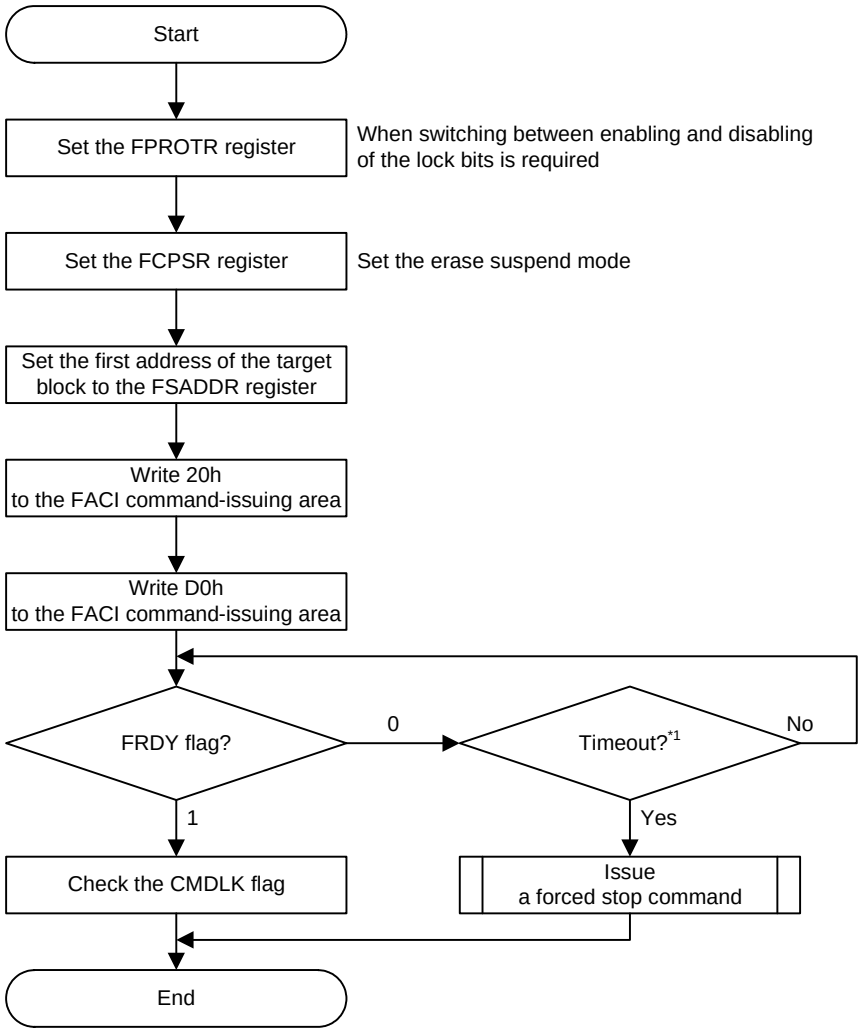


Note 1. Judgment of the timeout is based on 1.1 times 256-byte program time (max) for code flash memory.
For data flash memory, judgment is based on 1.1 times 4-byte program time (max).
For the 256-byte program time and 4-byte program time, see the User's Manual: Hardware.

Figure 6.9 Usage of the Program Command

6.3.9 Block Erase Command

A block erase command is used to erase the user area, lock bit, and data area.
Before issuing a block erase command, set the first address of the target block in the FSADDR register. Writing 20h and D0h to the FACI command-issuing area starts processing of a block erase command.
The FPROTR and FCPSR registers must be set before issuing the block erase command. To switch between enabling and disabling of the lock bits, the setting of the FPROTR register must be changed. To erase the lock bit, issue a block erase command while the FPROTR.FPROTCN bit is 1. The setting of the FCPSR register must be changed to switch the suspending method (suspend priority mode/erase priority mode) by the P/E suspend command.



Note 1. Judgment of the timeout is based on 1.1 times 32-Kbyte erase time (max) for code flash memory.
For data flash memory, judgment is based on 1.1 times 64-byte erase time (max).
For the 32-Kbyte erase time and 64-byte erase time, see the User's Manual: Hardware.

Figure 6.10 Usage of the Block Erase Command

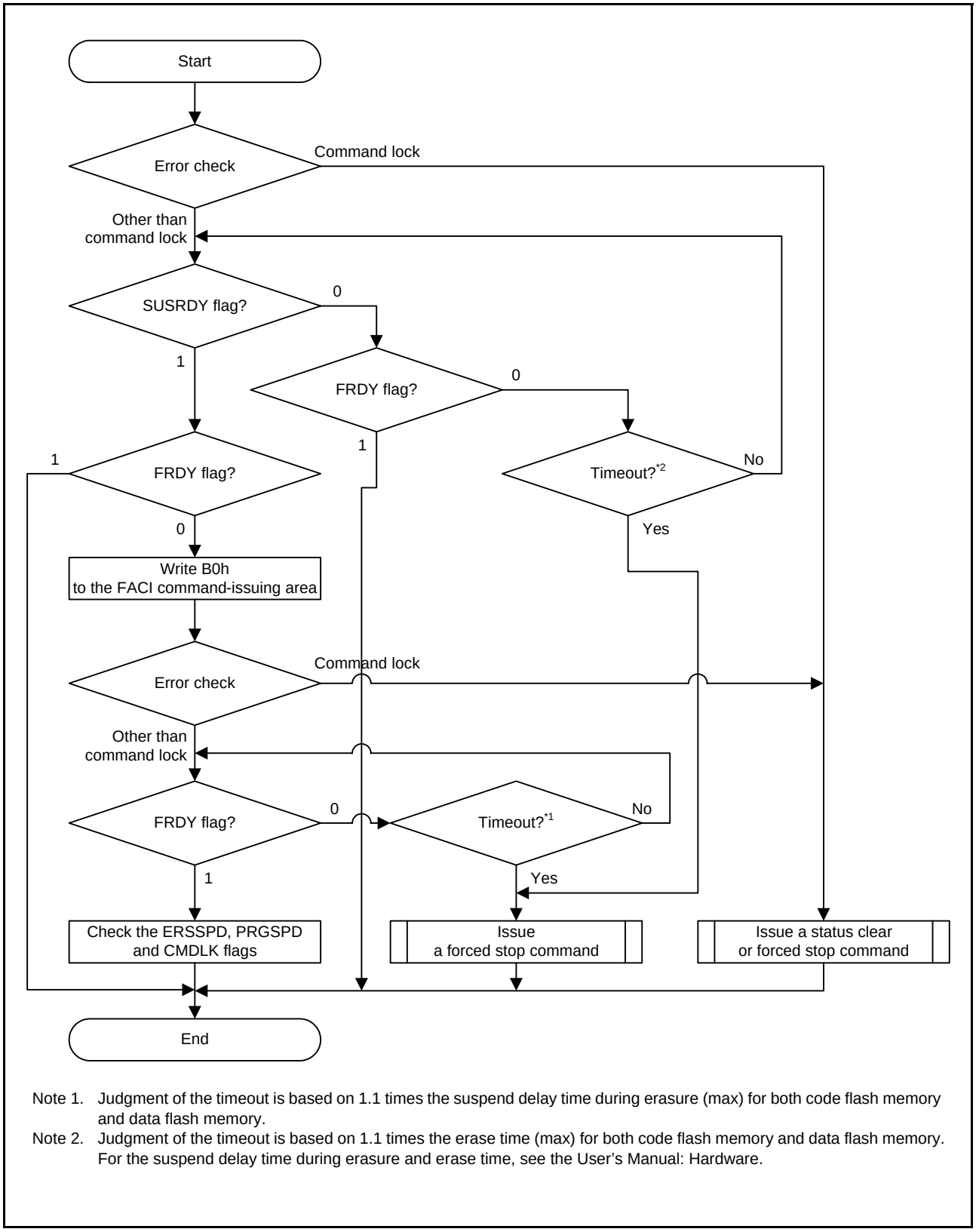
6.3.10 P/E Suspend Command

The P/E suspend command is used to suspend programming or erasure. Before issuing a P/E suspend command, check that the FASTAT.CMDLK flag is 0, and the execution of programming/erasure is normally performed. To confirm that the P/E suspend command can be received, also check that the FSTATR.SUSRDY flag is 1. After issuing a P/E suspend command, read the FASTAT.CMDLK flag to confirm that its value is not 1 (the flash sequencer is not in the command-locked state).

If programming or erasure processing has been completed between when the state of the FSTATR.SUSRDY flag is 1 is confirmed and when the P/E suspend command is accepted, any of errors listed in Table 7.1 does not occur and the device does not enter the suspension state (the FSTATR.FRDY flag is 1, and the FSTATR.ERSSPD and PRGSPD flags are 0).

When a P/E suspend command is received and then the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FSTATR.FRDY flag is set to 0, and the ERSSPD or PRGSPD flag in the FSTATR register is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD flag in the FSTATR register is 1 and the suspended state is entered, and then decide the subsequent flow. If a P/E resume command is issued in the subsequent flow although the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state (see section 7.2, Error Protection).

If the erase-suspended state is entered, programming to blocks other than the one currently suspended can be performed. In addition, the program- and erase-suspended states can move to read mode by clearing the FENTRYR register.



Note 1. Judgment of the timeout is based on 1.1 times the suspend delay time during erasure (max) for both code flash memory and data flash memory.
Note 2. Judgment of the timeout is based on 1.1 times the erase time (max) for both code flash memory and data flash memory. For the suspend delay time during erasure and erase time, see the User's Manual: Hardware.

Figure 6.11 Usage of the P/E Suspend Command

(1) Suspension during Programming

When issuing a P/E suspend command during the flash memory programming, the flash sequencer suspends programming processing. Figure 6.12 shows the suspend operation of programming. When receiving a program or P/E resume command, the flash sequencer sets the FSTATR.FRDY flag to 0 to start programming. When the flash sequencer is ready to accept the P/E suspend command after starting programming, it sets the FSTATR.SUSRDY flag to 1. When a P/E suspend command is issued, the flash sequencer receives the command and sets the FSTATR.SUSRDY flag to 0. When the flash sequencer receives a P/E suspend command while a program pulse is being applied, the flash sequencer continues applying the pulse. After the specified pulse application time, the flash sequencer finishes pulse application, and starts the programming suspend processing and sets the FSTATR.PRGSPD flag to 1.
When the suspend processing finishes, the flash sequencer sets the FSTATR.FRDY flag to 1 to enter the program-suspended state. When receiving a P/E resume command in the program-suspended state, the flash sequencer sets the FSTATR.FRDY and FSTATR.PRGSPD flags to 0 and resumes programming.

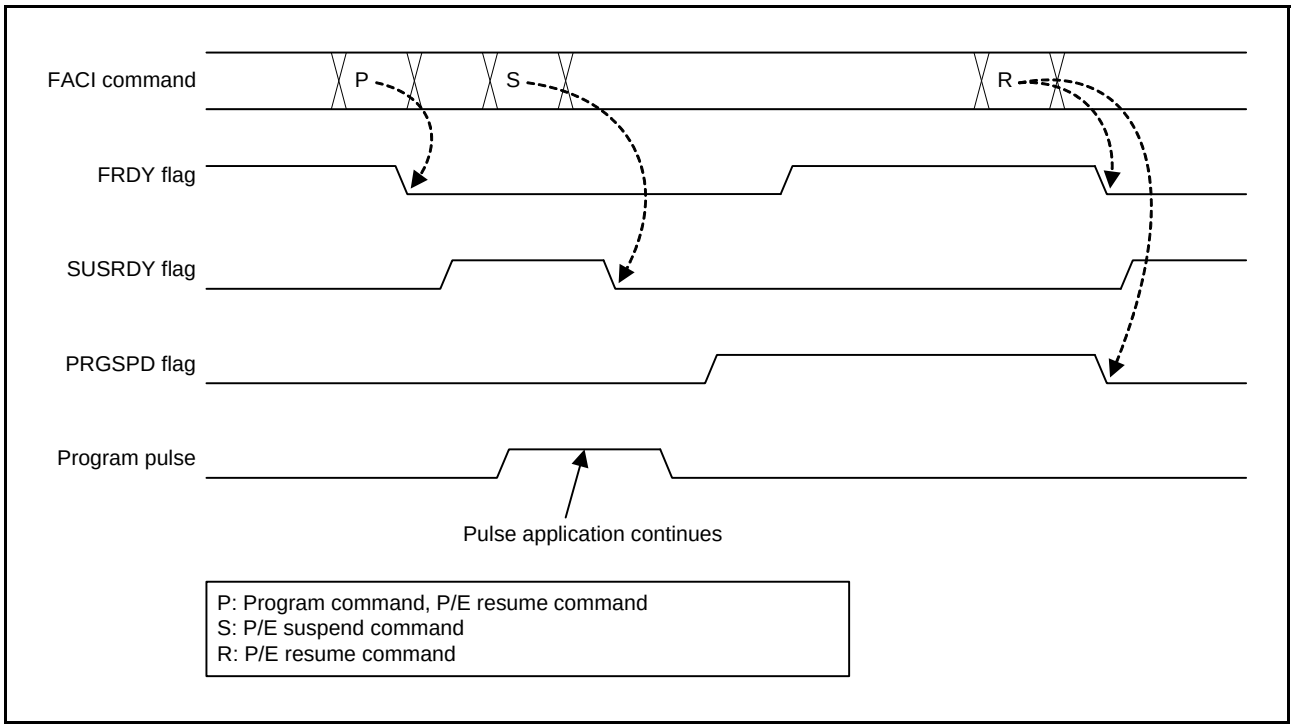


Figure 6.12 Suspension during Programming

(2) Suspension during Erasure (Suspend Priority Mode)

This MCU has a suspend priority mode for the suspension of erasure. Figure 6.13 shows the suspend operation of erasure in suspend priority mode (the FCPSR.ESUSPMD bit is 0).
When receiving a block erase or P/E resume command, the flash sequencer sets the FSTATR.FRDY flag to 0 to start erasure. When the flash sequencer is ready to accept the P/E suspend command after starting erasure, it sets the FSTATR.SUSRDY flag to 1. When a P/E suspend command is issued, the flash sequencer receives the command and sets the FSTATR.SUSRDY flag to 0. When receiving a P/E suspend command during erasure, the flash sequencer starts the suspend processing and sets the FSTATR.ERSSPD flag to 1 even if it is applying an erase pulse. When the suspend processing is completed, the flash sequencer sets the FSTATR.FRDY flag to 1 to enter the erase-suspended state. When receiving a P/E resume command in the erase-suspended state, the flash sequencer sets the FRDY and ERSSPD flags in the FSTATR register to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD flags in the FSTATR register at the suspension and resumption of erasure are the same, regardless of the erase suspend mode.
The setting of the erase suspend mode affects the control method of erase pulses. In suspension priority mode, when receiving a P/E suspend command while erase pulse A that has never been interrupted in the past is being applied, the flash sequencer suspends the application of erase pulse A and enters the erase-suspended state. When receiving a P/E suspend command while reapplying erase pulse A after erasure is resumed by a P/E resume command, the flash sequencer continues applying erase pulse A. After the specified pulse application time, the flash sequencer finishes erase pulse application and enters the erase-suspended state. When the flash sequencer receives a P/E resume command next and erase pulse B starts to be newly applied, and then the flash sequencer receives a P/E suspend command again, the application of erase pulse B is interrupted. In suspend priority mode, delay due to suspension can be minimized because the application of an erase pulse is interrupted once per pulse and priority is given to the suspend processing.

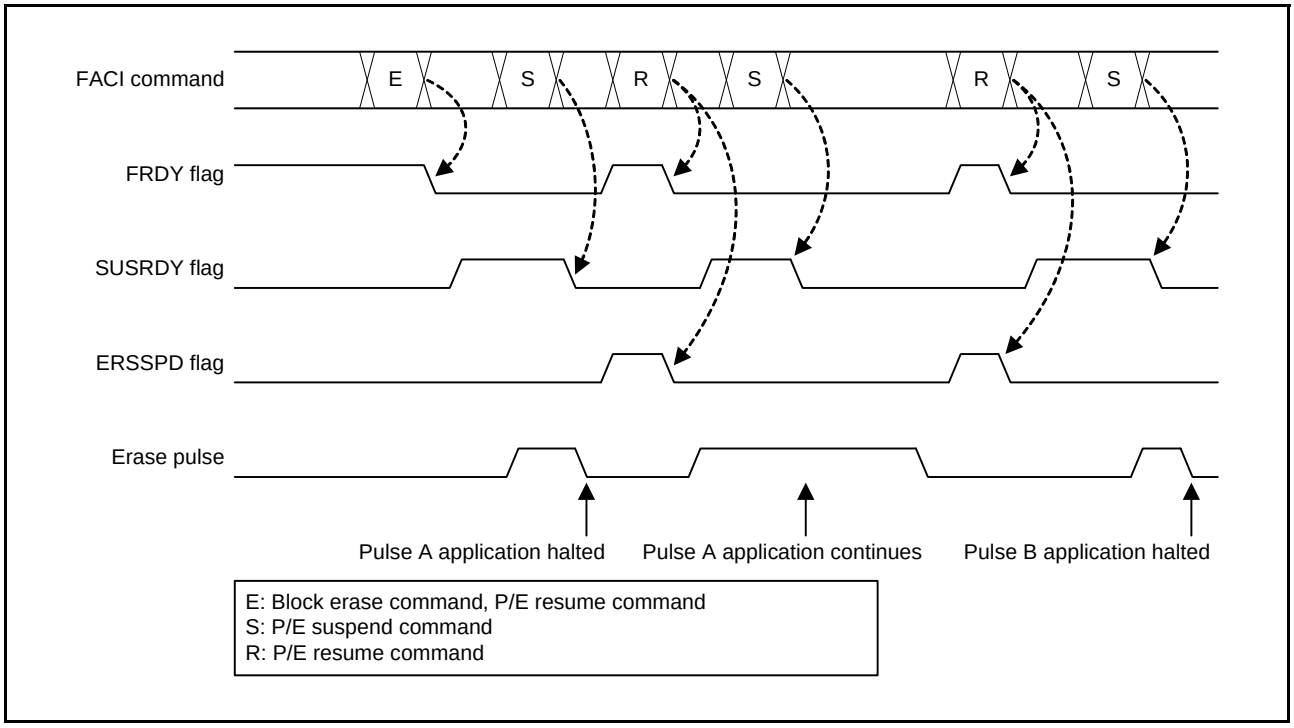


Figure 6.13 Suspension during Erasure (Suspend Priority Mode)

(3) Suspension during Erasure (Erase Priority Mode)

This MCU has an erase priority mode for the suspension of erasure.

Figure 6.14 shows the suspend operation of erasure when the erase suspend mode is set to the erase priority mode (the FCPSR.ESUSPMD bit is 1). The control method of erase pulses in erase priority mode is the same as that of program pulses for the program suspend processing.

When the flash sequencer receives a P/E suspend command while an erase pulse is being applied, the flash sequencer definitely continues applying the pulse. In this mode, the required time for the whole erasure processing can be reduced as compared with the suspend priority mode because the reapplication of erase pulses does not occur when a P/E resume command is issued.

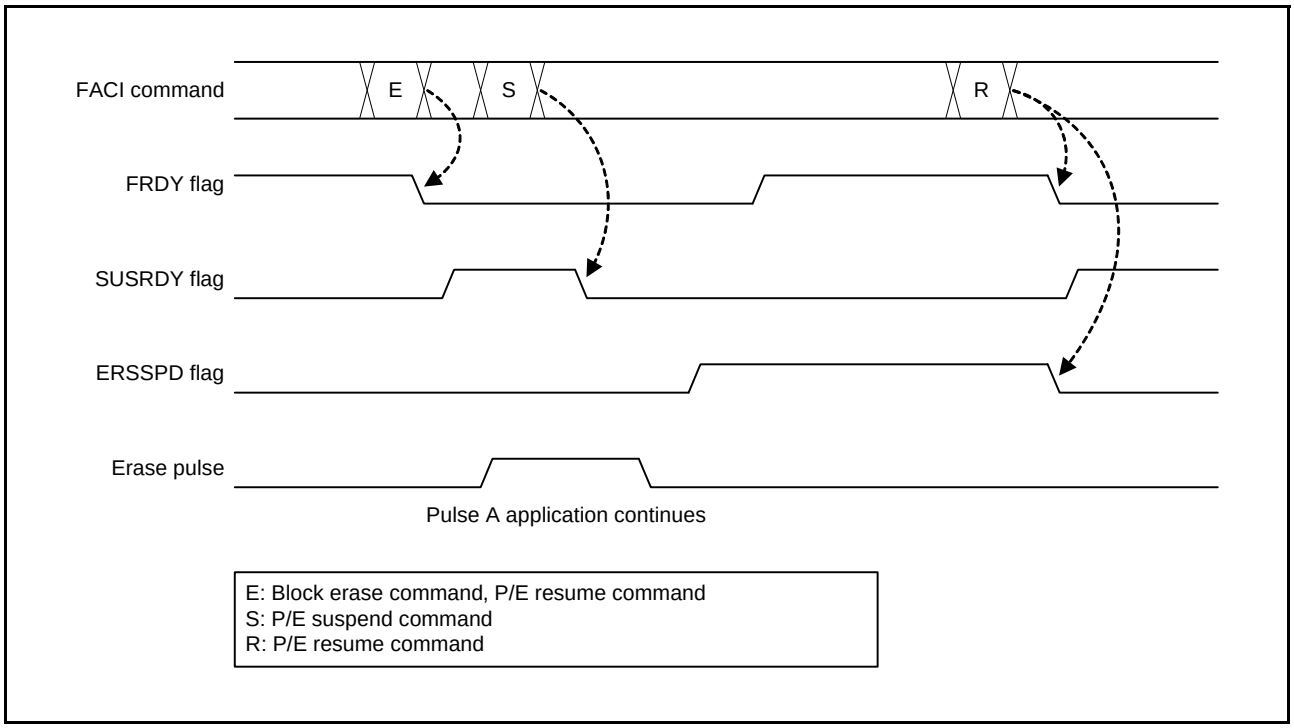
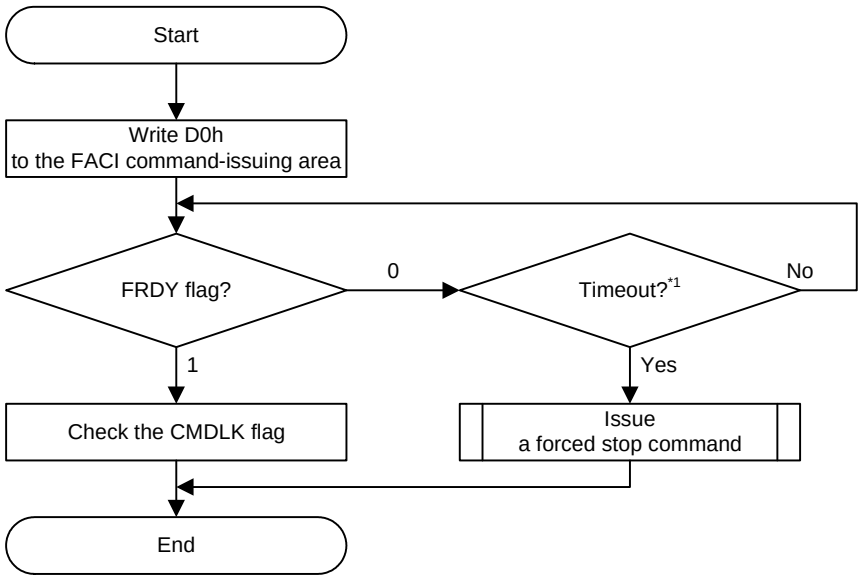


Figure 6.14 Suspension during Erasure (Erase Priority Mode)

6.3.11 P/E Resume Command

To resume suspended programming or erasure, use the P/E resume command. When the settings of the FENTRYR register are changed during suspend, reset the setting of the FENTRYR register to the value immediately before the P/E suspend command was issued, and then issue a P/E resume command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command (see section 9, Electrical Characteristics).

Figure 6.15 Usage of the P/E Resume Command

6.3.12 Status Clear Command

The status clear command is used to clear the command-locked state (see section 6.3.7, Recovery from the Command-Locked State). To clear the ILGLERR, ERSERR, and PRGERR flags in the FSTATR register in the command-locked state, the status clear command is available.
All processing of a status clear command can be executed by hardware without intervention by the FCU firmware.

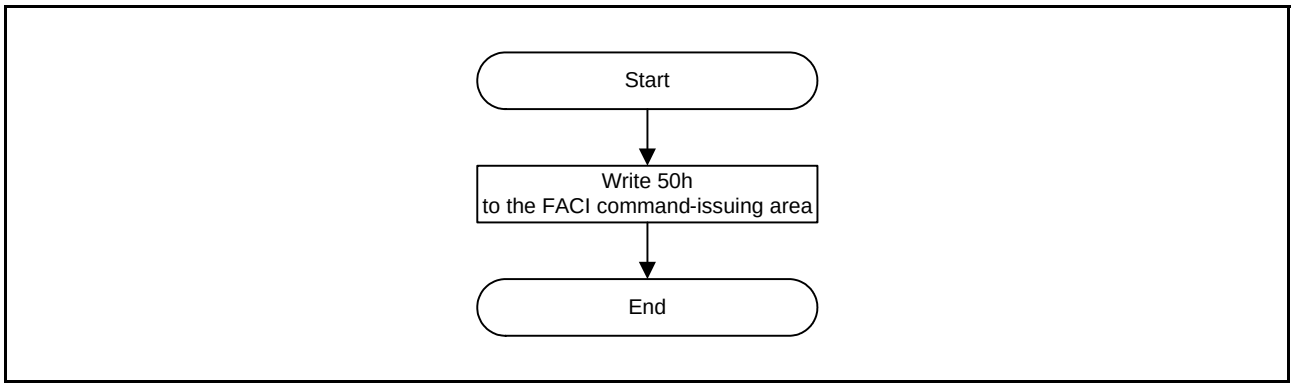


Figure 6.16 Usage of the Status Clear Command

6.3.13 Forced Stop Command

The forced stop command forcibly terminates command processing by the flash sequencer. Although this command halts command processing faster than the P/E suspend command, values of the area being programmed or erased are not guaranteed. Furthermore, resumption of processing is not possible. Processing of programming or erasure terminated by the forced stop command is also defined as one program/erase cycle.
Executing a forced stop command also initializes the entire FCU and part of the FACI, and the FSTATR register. Accordingly, this command can be used in the procedure for recovery from the command-locked state and in processing in response to a time-out of the flash sequencer (see section 6.3.7, Recovery from the Command-Locked State).
All processing of a forced stop command can be executed by hardware without intervention by the FCU firmware.

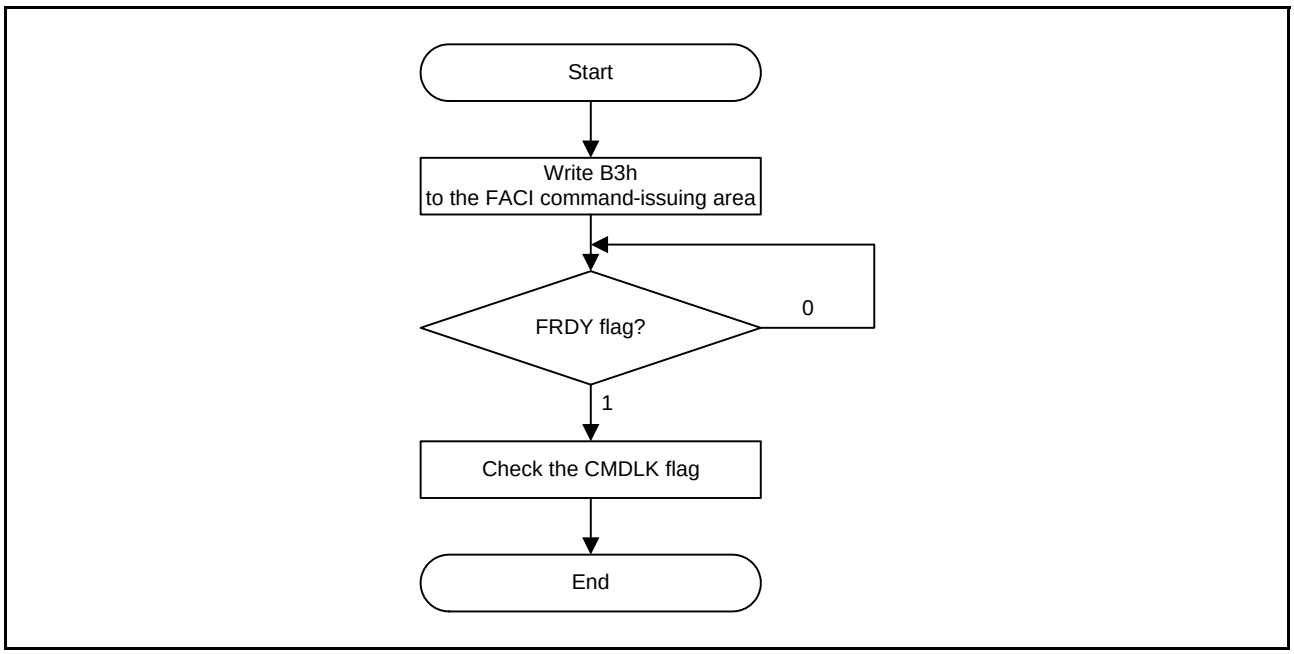


Figure 6.17 Usage of the Forced Stop Command

6.3.14 Blank Check Command

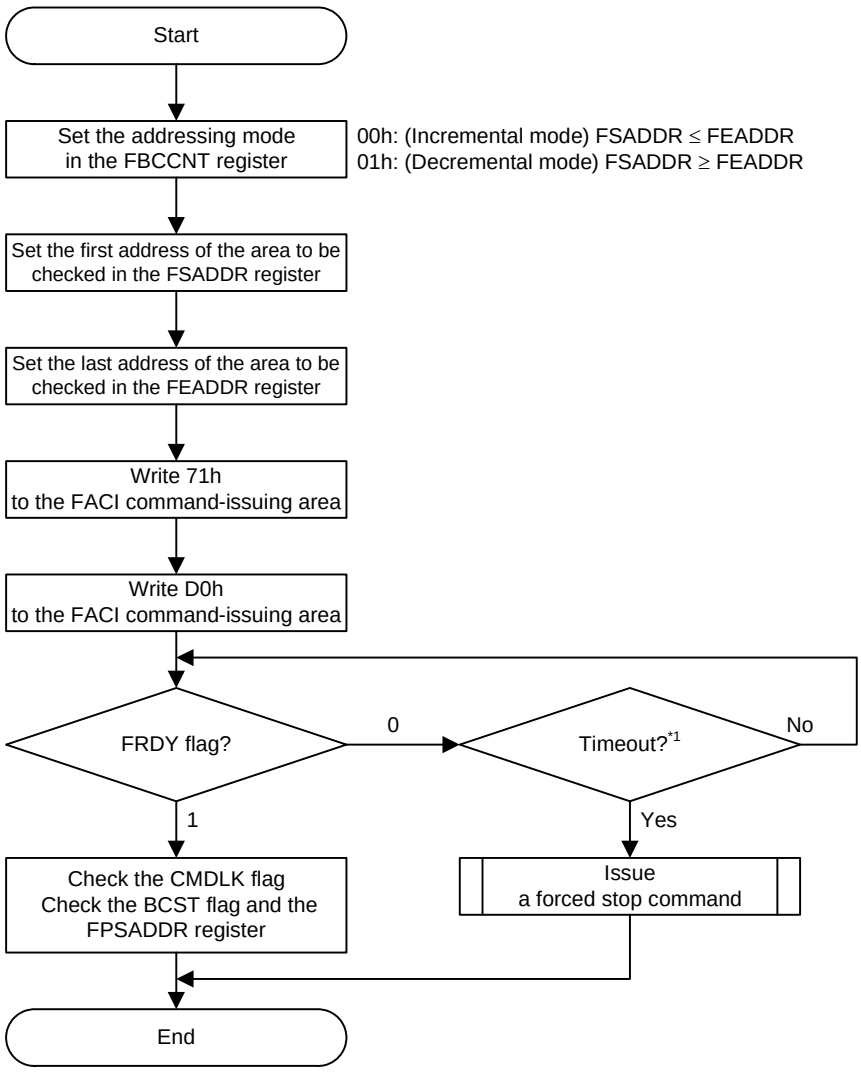
Values read from data flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state) are undefined. Use the blank check command when you need to confirm that an area is in the non-programmed state.

Before issuing a blank check command, set addressing mode, start and end addresses of the target area for blank checking to the FBCCNT, FSADDR, and FEADDR registers. When blank checking addressing mode is set to decremental mode (i.e. the FBCCNT.BCDIR bit is 1), the value specified in the FSADDR register must be set at least the value specified in the FEADDR register.

The value specified in the FSADDR register must be the value specified in the FEADDR register or less when blank check addressing mode is set to incremental mode (i.e. the FBCCNT.BCDIR bit is 0).

When the settings of the FBCCNT.BCDIR bit, FSADDR register, and FEADDR register are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for blank checking is in the range from 4 bytes to 64 Kbytes and is set in units of 4 bytes.

Write 71h and D0h to the FACI command-issuing area to start blank checking. Completion of processing can be confirmed by the FSTATR.FRDY flag. At the end of processing, the result of blank checking is stored in the FBCSTAT.BCST flag. If the target area for blank checking includes areas where programming has been completed, the flash sequencer stores the address of the programmed data that it first detected in the FPSADDR register.

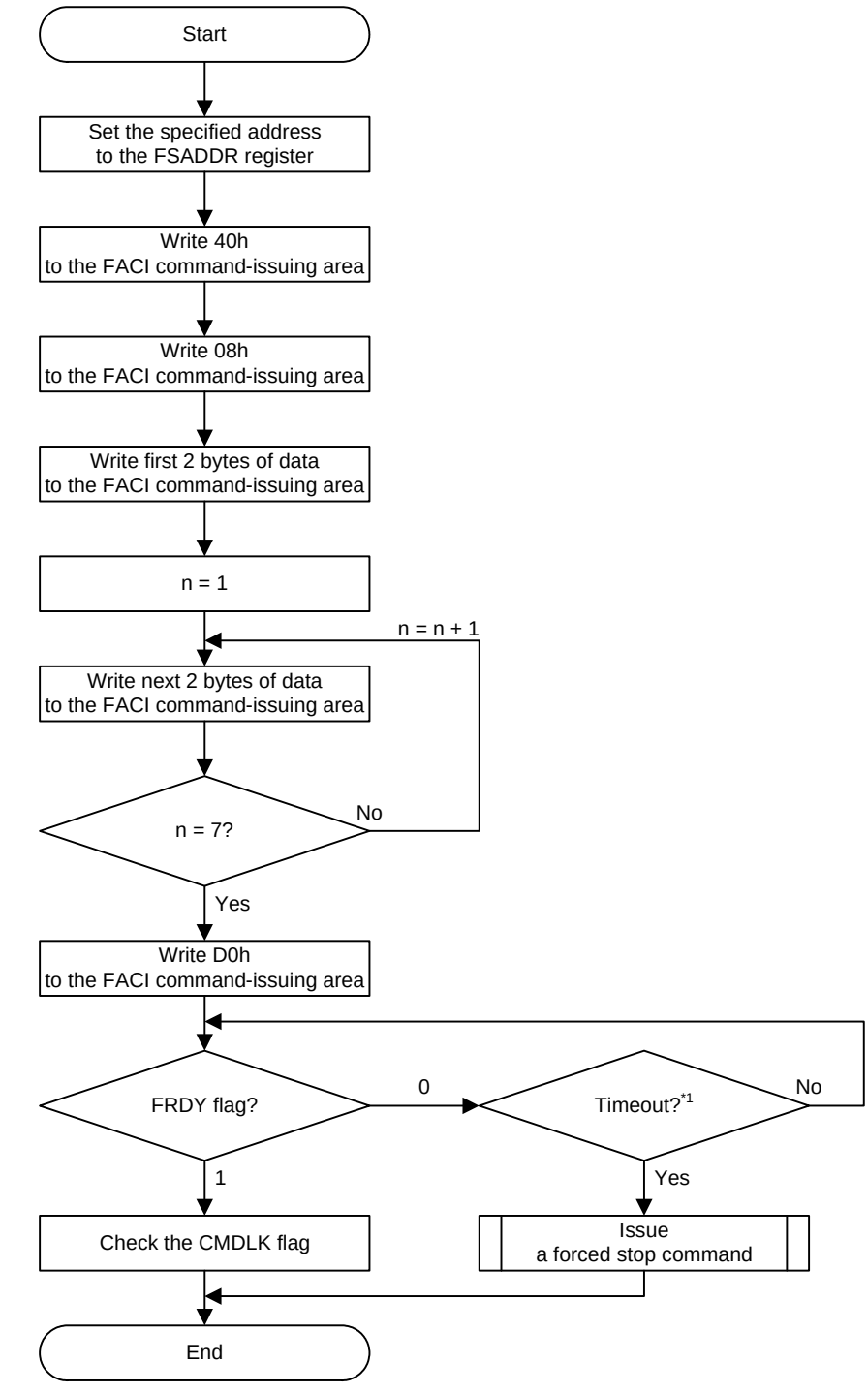


Note 1. Judgment of the timeout is based on 1.1 times the blank checking time (max.) for the entire target area. For the blank checking time, see the User's Manual: Hardware.

Figure 6.18 Usage of the Blank Check Command

6.3.15 Configuration Set Command

The configuration set command is used to set the ID, security function, option-setting memory, and TM function. Before issuing a configuration set command, set the specified address (shown in Table 6.5) in the FSADDR register. Writing D0h to the FACI command-issuing area in the final access for issuing the FACI command starts processing of the configuration set command.



Note 1. Judgment of the timeout is based on 70 ms elapsing (when 20 MHz ≤ FCLK ≤ 60 MHz), 140 ms elapsing (when FCLK = 4 MHz)

Figure 6.19 Usage of the Configuration Set Command

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in Table 6.5. Data in other areas can be changed to any value each time the configuration set command is executed.

Table 6.5 Address Used by Configuration Set Command

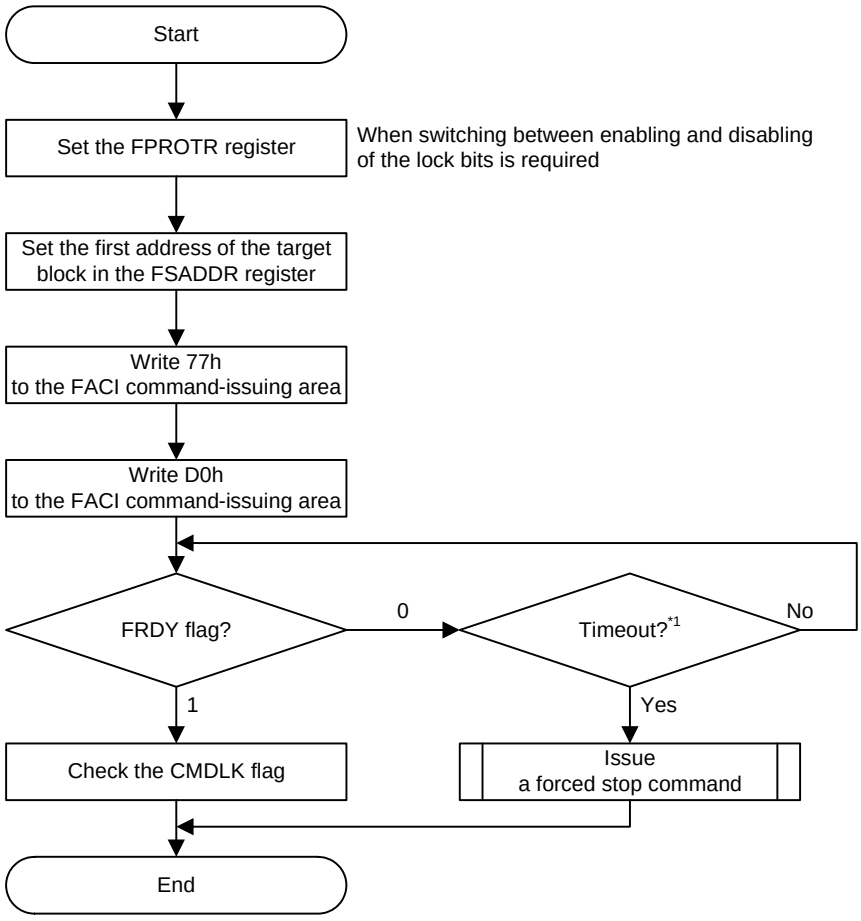
Address	FSADDR Register Value	Setting Data
0012 0040h	0000 0040h	Serial programmer command control register (SPCC), TM enable flag register (TMEF)
0012 0050h	0000 0050h	ID for authentication (OSIS)
0012 0060h	0000 0060h	TM identification data register (TMINF), option function selection (OFS0, OFS1), endian selection (MDE)

6.3.16 Lock-Bit Program Command

The lock-bit program command is used to write to a lock bit. The block erase command is used to erase a lock bit (see section 6.3.9, Block Erase Command).

Before issuing a lock-bit program command, set the first address of the target block in the FSADDR register. Writing 77h and D0h to the FACI command-issuing area starts processing of a lock-bit program command.

The FPROTR register must be set before issuing a lock-bit program command. To switch between enabling and disabling of the lock bits, the setting of the FPROTR register must be changed.

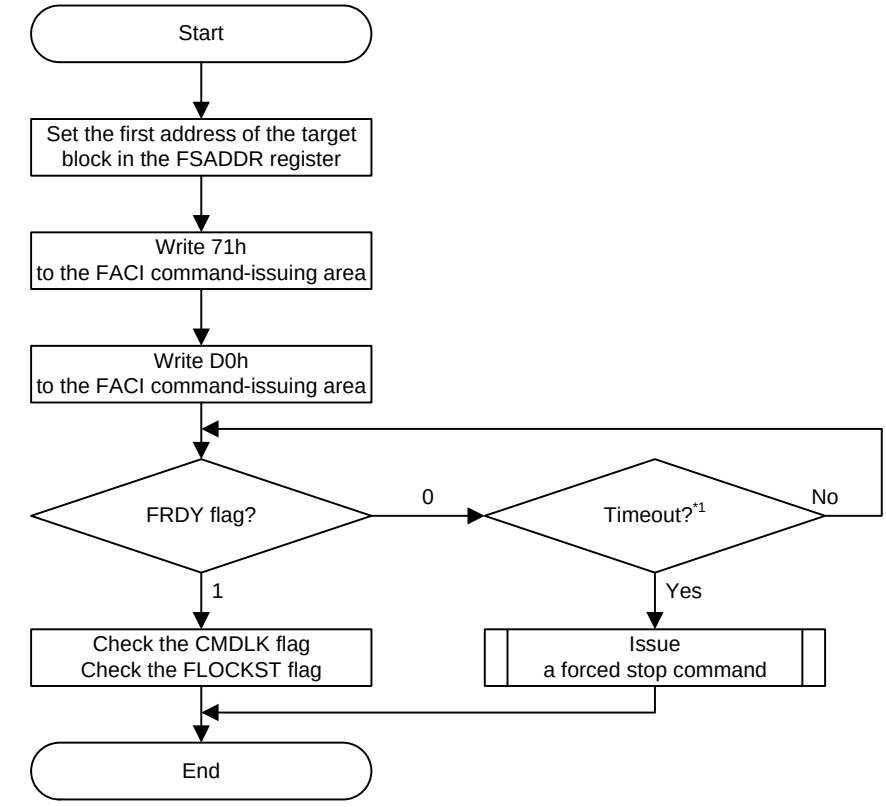


Note 1. Judgment of the timeout is based on 25 ms elapsing (when 20 MHz ≤ FCLK ≤ 60 MHz), 50 ms elapsing (when FCLK = 4 MHz)

Figure 6.20 Usage of the Lock-Bit Program Command

6.3.17 Lock-Bit Read Command

The lock-bit read command is used to read a lock bit.
Before issuing a lock-bit read command, set the first address of the target block in the FSADDR register. Writing 71h and D0h to the FACI command-issuing area starts processing of a lock-bit read command.
Completion of command processing can be confirmed with the FSTATR.FRDY flag. After command processing is completed, the result of reading the lock bit is stored in the FLKSTAT.FLOCKST flag.



Note 1. Judgment of the timeout is based on 10 µs elapsing (when 20 MHz ≤ FCLK ≤ 60 MHz), 20 µs elapsing (when FCLK = 4 MHz)

Figure 6.21 Usage of the Lock-Bit Read Command

7. Safety Function

7.1 Software Protection

Software protection disables programming and erasure for the code flash memory through the settings of control registers and lock bit settings in the user area. If an attempt is made to issue an FACI command against software protection, the flash sequencer enters the command-locked state.

7.1.1 Protection through FWEPROR

Programming cannot proceed in any mode unless the FWEPROR.FLWE[1:0] bits are set to 01b.

7.1.2 Protection through FENTRYR

When the FENTRYR register is set to 0000h, the flash sequencer enters read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

7.1.3 Protection through Lock Bit

Each block in the user area includes a lock bit. When the FPROTR.FPROTCN bit is 0, blocks whose lock bit is set to 0 are disabled from being programmed/erased. To program or erase blocks whose lock bit is set to 0, set the FPROTR.FPROTCN bit to 1. When the lock bit protection is violated and a code flash memory programming, block erase or lock-bit program command is issued, the flash sequencer enters the command-locked state.

7.2 Error Protection

Error protection detects erroneous issuance of FACI commands, unauthorized access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue a status clear or forced stop command while the CFAE and DFAE flags in the FASTAT register are 0. The status clear command can only be used while the FSTATR.FRDY flag is 1. The forced stop command can be used regardless of the value of the FSTATR.FRDY flag. When one of the ILGLERR, ERSERR, PRGERR, FRDTCT, FLWEERR, FCUERR, CFAE, and DFAE flags in the FSTATR register is set to 1, the value of the FASTAT.CMDLK flag becomes 1. When the flash sequencer enters the command-locked state (the FASTAT.CMDLK flag is 1) while the FAEINT.CMDLKIE bit is 1, a flash access error (FIFERR) interrupt is generated.
When the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during program or erase processing, the flash sequencer continues the processing for programming or erasure. In this state, the P/E suspend command cannot be used to suspend the processing for programming or erasure. If a command is issued in the command-locked state, the ILGLERR flag in the FSTATR register becomes 1 and the other flags retain the values set due to previous error detection.
Table 7.1 shows error protection types and status bit values after error detection.

Table 7.1 Error Protection Type

Error Type	Description	ILGLERR	ERSERR	PRGERR	FCUERR	FLWEERR	CFGDTCT	TBLDTCT	FRDTCT	CFAE	DFAE
FENTRYR setting error	AA81h was written to the FENTRYR register.	1	0	0	0	0	0	0	0	0	0
	The FENTRYR setting at suspension disagrees with that at resumption.	1	0	0	0	0	0	0	0	0	0
Illegal command error	An undefined code is written on the first access of an FACI command.	1	0	0	0	0	0	0	0	0	0
	A value other than D0h was written on the last access of an FACI command with multiple access cycles.	1	0	0	0	0	0	0	0	0	0
	The value “N” (refer to Table 6.2) specified in the second access of the FACI command in the program or configuration set command is illegal.	1	0	0	0	0	0	0	0	0	0
	The settings of the FBCCNT.BCDIR bit, FSADDR register, and FEADDR register are inconsistent when a blank check command was issued (see section 4.6, FACI Command End Address Register (FEADDR)).	1	0	0	0	0	0	0	0	0	0
	An FACI command not acceptable in each mode was issued (see Table 6.3).	1	0	0	0	0	0	0	0	0	0
	An FACI command was issued when command acceptance conditions are not satisfied (see Table 6.4).	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Erase error	An error occurs during erasure.	0	1	0	0	0	0	0	0	0	0
	A block erase command has been issued to an area protected by the lock bit.	0	1	0	0	0	0	0	0	0	0
Program error	An error occurs during programming.	0	0	1	0	0	0	0	0	0	0
	A program or lock-bit program command was issued to an area protected by the lock bit.	0	0	1	0	0	0	0	0	0	0
FCU error	An error occurs during CPU processing in FCU.	0	0	0	1	0	0	0	0	0	0
FCURAM ECC error	A 2-bit error was detected when FCURAM is read.	0	0	0	0	0	0	0	1	0	0
Code flash memory access violation	An FACI command was issued to the reserved area of the user area in code flash memory P/E mode (see section 4.2, Flash Access Status Register (FASTAT)).	1	0	0	0	0	0	0	0	1	0
Data flash memory access violation	An FACI command was issued to the reserved area of the data area in data flash memory P/E mode (see section 4.2, Flash Access Status Register (FASTAT)).	1	0	0	0	0	0	0	0	0	1
	A configuration set command was issued to the reserved area (see section 4.2, Flash Access Status Register (FASTAT)).	1	0	0	0	0	0	0	0	0	1
Others	The FACI command-issuing area was accessed in read mode.	1	0	0	0	0	0	0	0	0	0
	The FACI command-issuing area was read in code flash memory P/E mode or data flash memory P/E mode.	1	0	0	0	0	0	0	0	0	0
Flash P/E protection error	A flash memory program/erase protection error for the setting of the FWEPROR register was detected during command processing by the flash sequencer.	0	0/1	0/1	0	1	0	0	0	0	0
Configuration set ECC error	A 2-bit error was detected when the configuration setting value is read.	0	0	0	0	0	1	0	0	0	0
Programming parameter ECC error	A 2-bit error was detected when the overwrite parameter table is read.	0	0	0	0	0	0	1	0	0	0

7.3 Boot Program Protection

7.3.1 User Boot Protection

The user boot area can only be written in boot mode (for the SCI or USB interface). Since this area is usually write-protected in normal operating mode and user boot mode, it can be used for the safe storage of programs such as a boot program.

8. Usage Notes

(1) Reading Area Where Programming/Erasure was Aborted or Suspended

The data stored in the area where programming/erasure has been aborted or suspended are undefined. To avoid mulfunctions caused by reading undefined data, take care not to fetch instructions or read data from the area where programming/erasure was aborted or suspended.

(2) Suspension During Programming/Erasure

When processing of programming/erasure is interrupted by issuing the P/E suspend command, the programming/erasure processing can be resumed by issuing the P/E resume command. If the flash sequencer enters the command-locked state for any reason and issues the forced stop command after the suspended processing is normally completed and the ERSSPD flag or PRGSPD flag is set to 1, the suspended processing cannot be resumed. In addition, the values in the area where the processing was suspended are not guaranteed. Erase that area.

(3) Prohibition of Additional Programming

Programming a given area twice is not possible. Erase the area first before programming an area of flash memory after programming to the area has been completed.

(4) Resets During Programming/Erasure or Black Checking

In the case of a reset due to the signal on the RES# pin during programming/erasure or black checking, wait for at least t_{RESWF} (see the User's Manual: Hardware for details) of the reset input period once the operating voltage is within the range stipulated in the electrical characteristics after assertion of the reset signal, and then release the device from the reset state.

(5) Allocation of Vectors for Interrupts and Other Exceptions During Programming/Erasure

Generation of an interrupt or other exception during programming/erasure may lead to fetching of the vector from the code flash memory. If the conditions for using the background operation (BGO) are not satisfied, set the address for vector to an address that is not in the code flash memory.

(6) Abnormal Termination During Programming/Erasure or Blank Checking

Even if programming/erasure ends abnormally due to the generation of a reset by the RES# pin, the programming/erasure state of the flash memory with undefined data cannot be verified or checked. For the area where programming/erasure ends abnormally, the blank check function cannot judge whether the area is erased successfully or not. Erase the area again and confirm that the corresponding area is completely erased before using.
When programming/erasure or blank checking is not completed successfully due to a voltage change that exceeds the operational voltage range, a reset on the RES# pin, the command-locked state in response to error detection, or prohibited actions described in (7), the lock bit may be enabled.
In this case, erase the target block while the lock bit is disabled to erase the lock bit.

(7) Items Prohibited During Programming/Erasure or Blank Checking

High voltage is applied to the flash memory during programming/erasure or blank checking. To prevent damage to the flash memory, do not perform the following operations.

- Have the operating voltage from the power supply go beyond the permitted range.
- Change the FWEPROR.FLWE[1:0] bits.
- Change the SYSCR0.ROME bit.
- Change the OPCCR.OPCM[2:0] bits.
- Change the SCKCR.FCK[3:0] and PCLKB[3:0] bits.
- Change the SCKCR3.CKSEL[2:0] bits.
- Change the RSTCKCR.RSTCKEN bit.

- Transition to the all module clock stop mode, software standby mode, or deep software standby mode.

9. Electrical Characteristics

9.1 AC Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
FCURAM data transfer time	t_{FFRT}	—	220	—	µs	FCLK = 60 MHz and the FCURAME.FRAMTRAN bit is 0
		—	110	—	µs	FCLK = 60 MHz and the FCURAME.FRAMTRAN bit is 1
FACI command setup time	t_{FACS}	—	—	100	µs	20 MHz ≤ FCLK ≤ 60 MHz
		—	—	200	µs	FCLK = 4 MHz
FACI command processing time	t_{FACE}	—	—	2	t_{Fcyc}	For other than program of code flash memory
		—	—	92	t_{Fcyc}	For program of code flash memory
Forced stop command	t_{FD}	—	—	20	µs	20MHz ≤ FCLK ≤ 60 MHz
		—	—	32	µs	FCLK = 4 MHz

Note: t_{Fcyc}: FCLK cycle

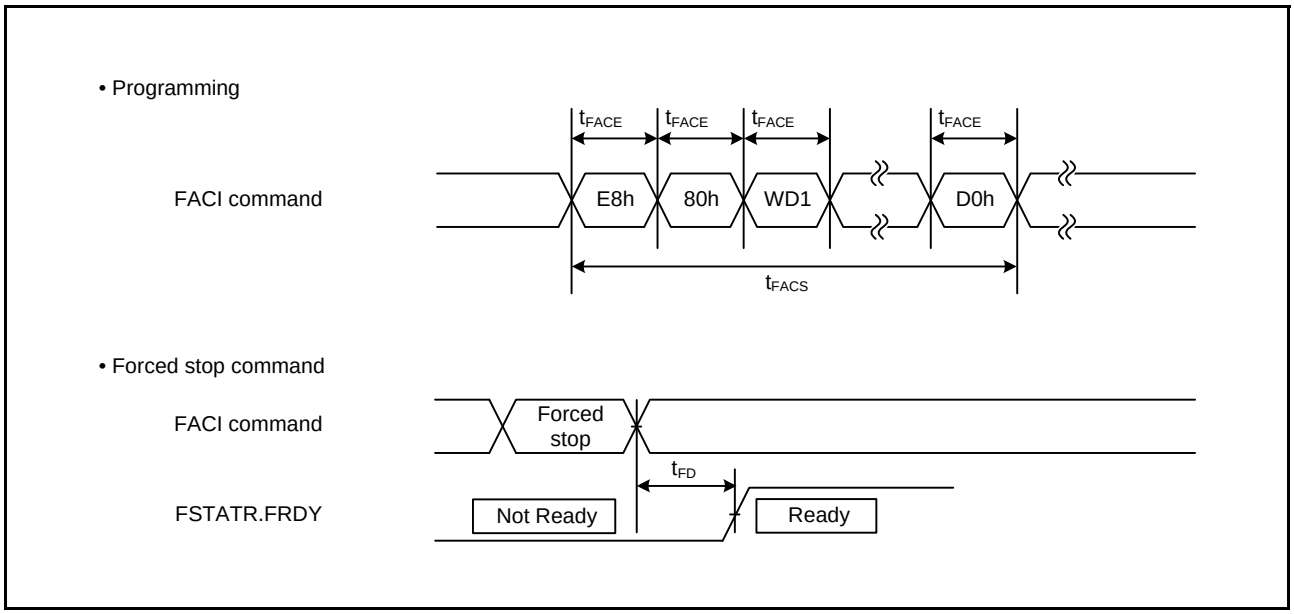


Figure 9.1 Timing of FACI Command

REVISION HISTORY	RX64M Group, RX71M Group Flash Memory User's Manual: Hardware Interface

Rev.	Date	Description	
		Page	Summary
0.90	May 30, 2014	—	First edition, issued
1.00	Jul 31, 2014	6. FACI Commands	
		8	Table 3.1 Information on the Hardware Interface Area, changed
		32	Table 6.1 List of FACI Commands, changed
		55	6.3.15 Configuration Set Command, changed
		56	Table 6.5 Address Used by Configuration Set Command, changed
		60	Table 7.1 Error Protection Type, changed
1.10	Nov 05, 2014	—	RX71M group, added
		All	Terms unified: RX64M User's Manual: Hardware or RX71M User's Manual: Hardware → User's Manual: Hardware
		1. Features	
		6	Body text changed
		2. Module Configuration	
		7	Body text changed
		4. Registers	
		10	4.1 Flash P/E Protect Register (FWEPROR), changed
		11	4.2 Flash Access Status Register (FASTAT), changed
		13	4.3 Flash Access Error Interrupt Enable Register (FAEINT)
		15	4.5 FACI Command Start Address Register (FSADDR), changed
		16	4.6 FACI Command End Address Register (FEADDR), changed
		17	4.7 FCURAM Enable Register (FCURAME), changed
		22	4.9 Flash P/E Mode Entry Register (FENTRYR), changed
		23	4.10 Flash Protection Register (FPROTR), changed
		24	4.11 Flash Sequencer Set-Up Initialization Register (FSUINITR), changed
		27	4.14 Flash P/E Status Register (FPESTAT), changed
		30	4.19 Flash Sequencer Processing Clock Notification Register (FPCKAR), changed
		6. FACI Commands	
		32	Table 6.1 List of FACI Commands, changed
		33	6.2 Relationship between the Flash Sequencer State and FACI Commands, changed
		35	Figure 6.1 Overview of Command Usage in Code Flash Memory P/E Mode (for products in which BGO is possible), changed
		36	Figure 6.2 Overview of Command Usage in Code Flash Memory P/E Mode (for products in which BGO is not possible), changed
		37	Figure 6.3 Overview of Command Usage in Data Flash Memory P/E Mode, changed
		40	Figure 6.7 Procedure for Transition to Read Mode, changed
		44	Figure 6.9 Usage of the Programming Command, changed
		46	6.3.10 P/E Suspend Command, changed
		48	Figure 6.12 Suspension during Programming, changed
		54	Figure 6.18 Usage of the Blank Check Command, changed
		55, 56	6.3.15 Configuration Set Command, changed Table 6.5 Address Used by Configuration Set Command, changed
		7. Safety Function	
		59	7.1.3 Protection through Lock Bit, changed
		60	Table 7.1 Error Protection Type, changed
		8. Usage Notes	
		62	(3) Resets during programming and erasure, changed

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.20	Dec 25, 2019	1. Features		
		6	Body text changed	
		2. Module Configuration		
		7	Body text changed	
		4. Registers		
		11, 12	4.2 Flash Access Status Register (FASTAT), changed	
		19 to 21	4.8 Flash Status Register (FSTATR), changed	
		22	4.9 Flash P/E Mode Entry Register (FENTRYR), changed	
		28	4.16 Data Flash Blank Check Status Register (FBCSTAT), changed	
		30	4.19 Flash Sequencer Processing Clock Frequency Notification Register (FPCKAR), changed	
		6. FACI Commands		
		33	6.2 Relationship between the Flash Sequencer State and FACI Commands, changed	
		34	Table 6.4 Acceptable FACI Commands and the State of the Flash Sequencer: Note 5 added	
		35	Figure 6.1 Overview of Command Usage in Code Flash Memory P/E Mode (for products in which BGO is possible), changed	
		42	Figure 6.8 Recovery from the Command-Locked State, changed	
		43	6.3.8 Programming Command, changed	
		46	6.3.10 P/E Suspend Command, changed	
		47	Figure 6.11 Usage of the P/E Suspend Command, changed	TN-RX*-A187A/E
		56	Figure 6.19 Usage of the Configuration Set Command: Note 1 changed	
		58	Figure 6.20 Usage of the Lock-Bit Programming Command: Note 1 changed	
		59	Figure 6.21 Usage of the Lock-Bit Read Command: Note 1 changed	
		7. Safety Function		
		60	7.2 Error Protection, changed	
		61	Table 7.1 Error Protection Type, changed	
		62	7.3.1 User Boot Protection, changed	
		8. Usage Notes		
		63	(1)(4)(5)(6)(7), changed (2), added	
		9. Electrical Characteristics		
		65	9.1 AC Characteristics, changed Figure 9.1 Timing of FACI Command, added	
1.21	Oct 28, 2022	3. Address Space		
		8	Table 3.1 Information on the Hardware Interface Area, changed	
		6. FACI Commands		
		45	Figure 6.10 Usage of the Block Erase Command, changed	

RX64M Group, RX71M Group Flash Memory
User's Manual: Hardware Interface

Publication Date: Rev.0.90 May 30, 2014
Rev.1.21 Oct 28, 2022

Published by: Renesas Electronics Corporation

RX64M Group, RX71M Group
Flash Memory

Renesas Electronics Corporation

R01UH0435EJ0121