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Renesas Starter Kit+ for SH7203

User's Manual

RENEASAS SINGLE-CHIP MICROCOMPUTER
SuperH™RISC engine

Table of Contents

Chapter 1. Preface	1
Chapter 2. Purpose	2
Chapter 3. Power Supply	3
3.1. Requirements	3
3.2. Power – Up Behaviour	3
Chapter 4. Board Layout	4
4.1. Component Layout	4
4.2. Board Dimensions	5
Chapter 5. Block Diagram	6
Chapter 6. User Circuitry	7
6.1. Switches	7
6.2. LEDs	7
6.3. Potentiometer	7
6.4. Serial port	8
6.5. Debug LCD Module	8
6.6. RCAN	8
6.7. USB	9
6.8. ETHERNET	9
6.9. LCD Interface	9
6.10. SSI	11
6.11. Option Links	12
6.12. DIP Switch Settings	12
6.13. Oscillator Sources	17
6.14. Reset Circuit	17
Chapter 7. Modes	18
Chapter 8. Programming Methods	19
8.1. H-UDI Header for E10A	19
8.2. AUD Header for E10A	19
Chapter 9. Headers	20
9.1. Application Headers	20
Chapter 10. Code Development	23
10.1. Overview	23
10.2. Compiler Restrictions	23
10.3. Breakpoint Support	23
10.4. Memory Map	24
Chapter 11. Component Placement	25
Chapter 12. Additional Information	27

Chapter 1. Preface

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Glossary

RSK	Renesas Starter Kit	RSK+	Renesas Starter Kit plus
LCD	Liquid Crystal Display	ADC	Analog to Digital Converter
CPU	Central Processing Unit	LED	Light Emitting Diode
E10A	'E10A for Starter Kits' Debugger	AUD	Advanced User Debugger
H-UDI	Hitachi - User Debug Interface	USB	Universal Serial Bus
SSI	Serial sound Interface	RCAN	Renesas Controller Area Network
DIP	Dual-In-Line package		

Chapter 2. Purpose

This RSK+ is an evaluation tool for Renesas microcontrollers.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as switches, LEDs and potentiometer(s).
- Sample Application.
- Sample peripheral device initialisation code.

The CPU board contains all the circuitry required for microcontroller operation.

This manual describes the technical details of the RSK+SH7203 hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Chapter 3. Power Supply

3.1. Requirements

This CPU board can operate from either a 5V power supply or an 8V to 15V supply.

Please refer to the following table while selecting the power supply voltage range -

	Jumpers SEL_5VA and SEL_5VB Fitted	Jumpers SEL_5VA and SEL_5VB Removed
Power Supply	5V only	8V to 15V (Default setting)*

* - 12V power supply is included with the RSK+ board.

Table 3-1 Power Supply Options

Warning - Care must be taken to ensure that an appropriate supply is used. Failing to do this may cause permanent damage to the board.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All CPU boards have a centre positive supply connector using a 2.0mm barrel power jack.

Warning - The CPU board is not over voltage protected. Use a centre positive supply for this board.

3.2. Power – Up Behaviour

When the RSK+ is purchased the CPU board has the 'Release' or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. Pressing any switch will cause the LEDs to flash at a rate controlled by the potentiometer.

Chapter 4. Board Layout

4.1. Component Layout

The following diagram shows top layer component layout of the board.

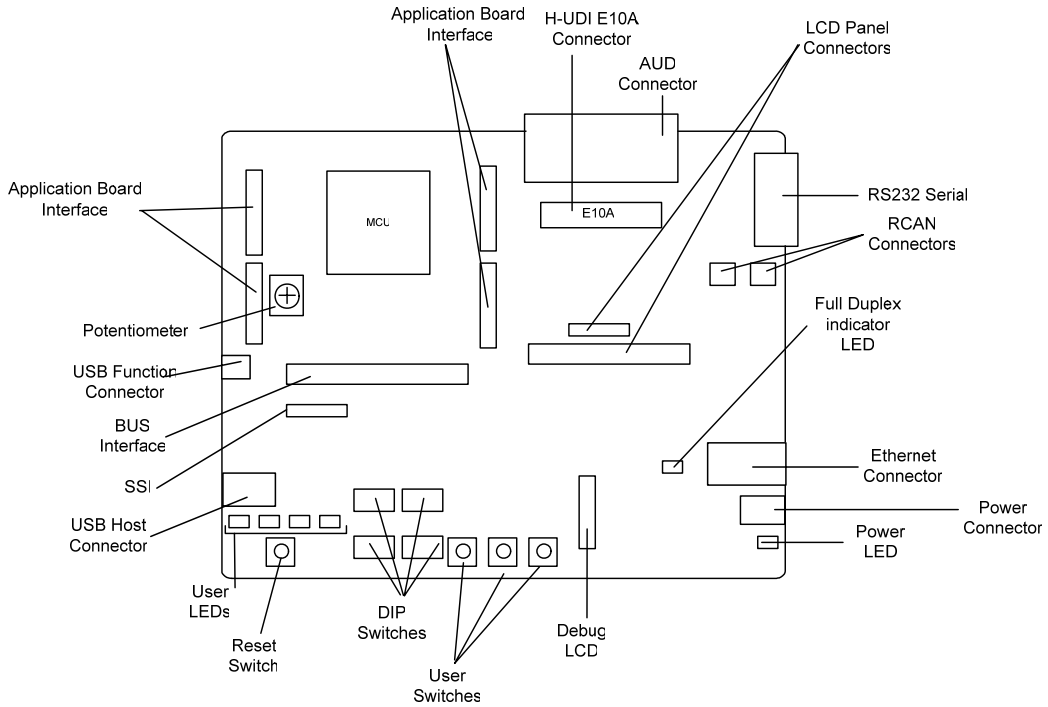


Figure 4-1: Board Layout

4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

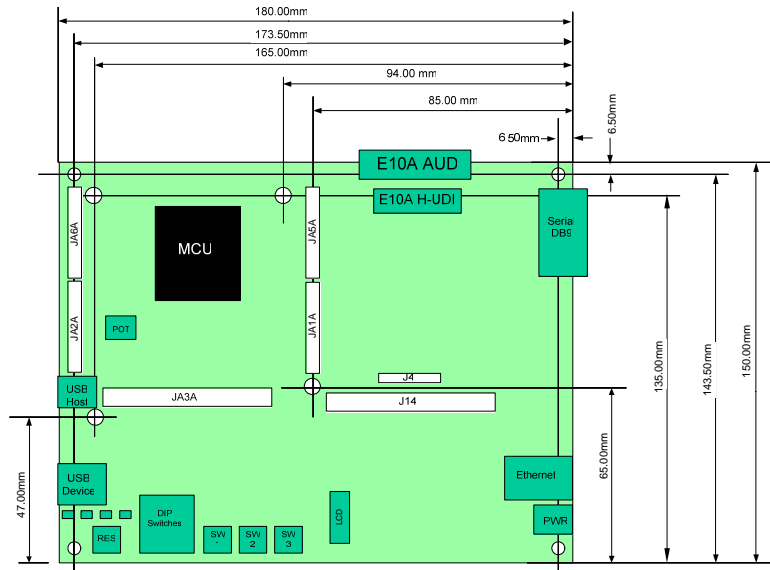


Figure 4-2 : Board Dimensions

Chapter 5. Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.

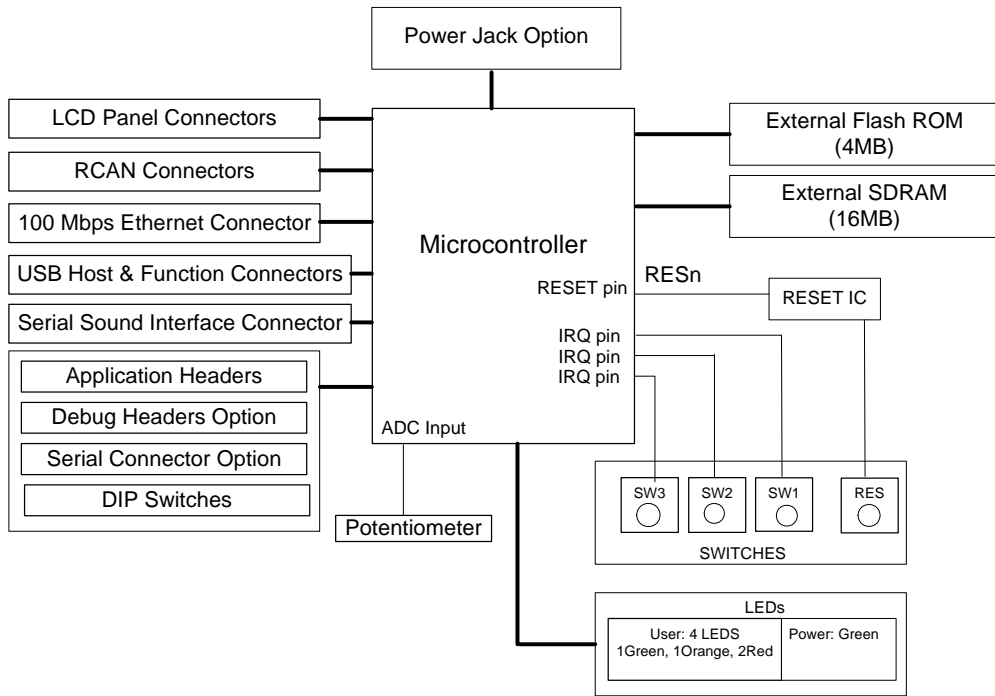


Figure 5-1: Block Diagram

Figure 5-2 shows the connections to the RSK+ board.

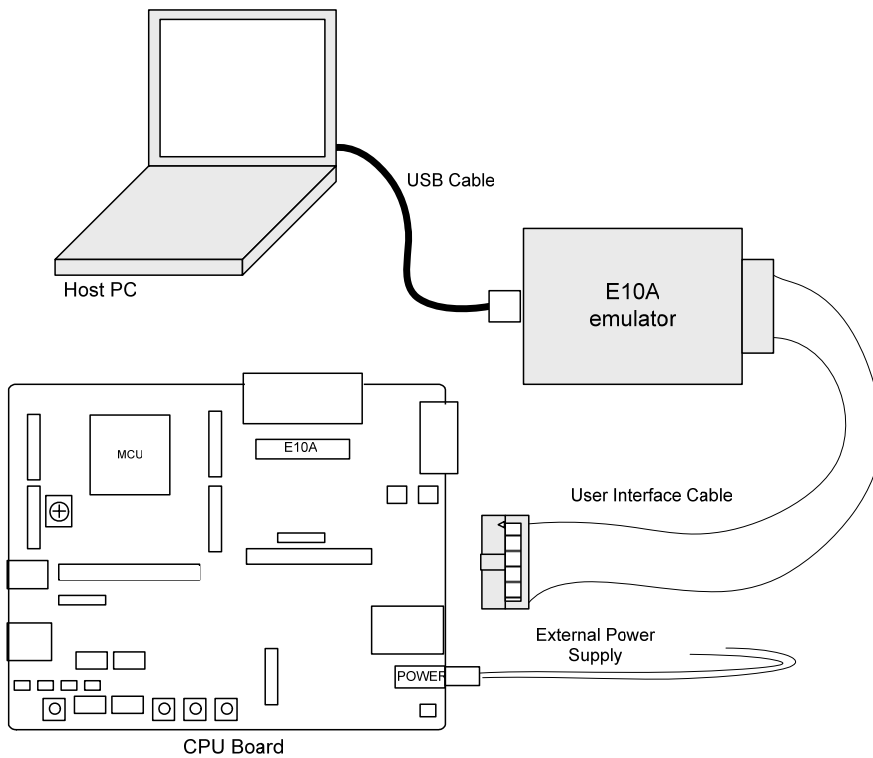


Figure 5-2 : RSK+ Connections

Chapter 6. User Circuitry

6.1. Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in **Table 6-1**.

Switch	Function	Microcontroller
RES	When pressed; the CPU board microcontroller is reset.	RESn , Pin 59
SW1*	Connects to an IRQ input for user controls. SW6-8 needs to be ON.	IRQ0 , Pin 179 (Port B, bit 0)
SW2*	Connects to an IRQ line for user controls. SW6-5 needs to be ON.	IRQ1 , Pin 180 (Port B, bit 1)
SW3*	Connects to an IRQ line for user controls. SW6-3 needs to be ON.	IRQ2 , Pin 181 (Port B, bit 2)

* - Please refer to **Table 6-25** to **Table 6-27** for details on DIP switch settings.

Table 6-1 Switch Functions

6.2. LEDs

There are 6 LEDs on the CPU board. The green 'POWER' LED lights when the board is powered. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low. An Orange LED "LED4" will lit when the Ethernet link operates in Full Duplex mode.

Table 6-2 below, shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Microcontroller Port Pin function	Microcontroller Pin Number	Polarity
LED0	Port E bit 10	71	Active Low
LED1*	Port E bit 12	73	Active Low
LED2*	Port C bit 14	75	Active Low
LED3*	Port E bit 11	72	Active Low

* - Please refer to **Table 6-13**, **Table 6-20** and **Table 6-21** for details on DIP switch settings.

Table 6-2 LED Ports

6.3. Potentiometer

A single turn potentiometer is connected to AN0 of the microcontroller via an option resistor 'R67' (which is fitted by default). This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

6.4. Serial port

The microcontroller serial port SCIF0 can be used for RS232 communication. Please refer to **Table 6-3** for the option links related with the serial ports-

Description	Function	Fit for RS232	Remove to use alternate function
TxD0	Serial Port Tx Pin	R103	R103
RxD0	Serial Port Rx Pin	R98	R98

Table 6-3 Serial Option Links

The board is designed to accept a straight through RS232 cable.

6.5. Debug LCD Module

The LCD module supplied with the RSK can be connected to the connector 'LCD' for use with the tutorial code. Any module that conforms to the pin connections and has a KS0066u compatible controller can be used. The LCD module uses a 4bit interface to reduce the pin allocation. No contrast control is provided; this must be set on the display module.

The module supplied with the CPU board only supports 5V operation.

Table 6-4 shows the pin allocation and signal names used on this connector.

LCD					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Ground	-	2	5V Only	-
3	No Connection	-	4	DLCDRS	138
5	R/W (Wired to Write only)	-	6	DLCDE	148
7	No Connection	-	8	No connection	-
9	No Connection	-	10	No connection	-
11	DLCD4	140	12	DLCD5	136
13	DLCD6	135	14	DLCD7	134

Table 6-4 Debug LCD Module Connections

6.6. RCAN

Two RCAN ports are available on this board. The SH7203 on-chip RCAN module offers a flexible and sophisticated way to organise and control CAN frames, providing the compliance to CAN2.0B Active and ISO-11898-1. **Table 6-5** details the CAN connectors available on this RSK+ board -

CAN0			CAN1		
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	CTx0	86*	1	CTx1	88*
2	GROUND	-	2	GROUND	-
3	CRx0	85*	3	CRx1	87*

* - The RCAN transceivers translate the voltage levels on CPU pin to meet RCAN voltage level standards.

Table 6-5 RCAN Connectors

For more details on SH7203 on-chip *RCAN* module, please refer to *SH7203 Group Hardware Manual*.

6.7. USB

The USB 2.0 host/function module (USB) provides capabilities as a USB host and USB function. It supports high-speed and full-speed transfers defined by USB specification 2.0. The Low speed mode is not supported. This module has a USB transceiver and supports all of the transfer types defined by the USB specification. The module has an 8-kbyte on-chip buffer memory for data transfer, providing a maximum of eight pipes. Any endpoint numbers can be assigned to PIPE1 to PIPE7, based on the peripheral devices or user system for communication. Please note that, a 5V power supply needs to be used while connecting a USB powered device (to the USB Host connector of the RSK+SH7203) if more than 25mA current is required to be sourced. See 3.1.

Table 6-6 below details the USB connectors available on this RSK+ board.

USB_H (USB Host)			USB_D (USB Device / Function)		
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	HOST_VBUS	See SW4-2 to SW4-5	1	DEVICE_VBUS*	See SW4-2 to SW4-5
2	USD -	100	2	USD -	100
3	USD +	101	3	USD +	101
4	GROUND	-	4	NC	-
			5	GROUND	-

* - The connection is via SW4-5.

Table 6-6 USB Connectors

For more details on SH7203 on-chip *USB* module, please refer to *SH7203 Group Hardware Manual*.

6.8. ETHERNET

The network functionality is provided by the SMCS LAN9118-MT non-PCI Ethernet controller. The Ethernet controller is configured to use a 16 bit data bus. It uses single 16 bit read and write strobes. Byte or long word accesses are not available for this device. The chip select used for the network controller is CS1n.

Refer to the *SMCS LAN9118-MT datasheet* for more information on this peripheral.

6.9. LCD Interface

Unified memory architecture is adopted for the LCD controller (LCDC) so that the image data for display is stored in system memory. The LCDC module reads data from system memory, uses the palette memory to determine the colours, and then puts the display on the LCD

panel. It is possible to connect the LCDC to the LCD module other than microcomputer bus interface types and NTSC/PAL types and those that apply the LVDS interface.

Two separate headers are provided on the RSK+ boards to support two types of LCDs -

1. Hitachi LCD (J4)
2. Generic LCD (J14)

Table 6-7 and Table 6-8 below details the LCD headers available on this RSK+ board.

J4 (For Hitachi LCD)					
Pin	CPU board Signal Name	Device Pin	Pin	CPU board Signal Name	Device Pin
1	GROUND	---	2	GROUND	---
3	GROUND	---	4	LCD_VCC	---
5	LCD_VCC	---	6	LCD_VCC	---
7	GROUND	---	8	BLCD_DATA0	169*
9	BLCD_DATA1	167*	10	BLCD_DATA2	166*
11	BLCD_DATA3	165*	12	BLCD_DATA4	164*
13	BLCD_DATA5	163*	14	BLCD_DATA6	162*
15	BLCD_DATA7	161*	16	BLCD_DATA8	160*
17	BLCD_DATA9	158*	18	BLCD_DATA10	155*
19	GROUND	---	20	BLCD_DATA11	153*
21	BLCD_DATA12	152*	22	BLCD_DATA13	151*
23	BLCD_DATA14	150*	24	BLCD_DATA15	149*
25	BLCD_DOTCLK	137*	26	BLCD_HSYNC	147*
27	BLCD_VSYNC	139*	28	BSSCS0	210**
29	BSSCK0	213**	30	BSS00	211**
31	SSI0	212***	32	BLCD_RESn	59*
33	GROUND	---	34	VLED +	---
35	VLED +	---	36	VLED -	---
37	VLED -	---	38	GROUND	---
39	GROUND	---			

Table 6-7 LCD Header J4

J14 (For Generic LCD)					
Pin	CPU board Signal Name	Device Pin	Pin	CPU board Signal Name	Device Pin
1	BOARD_5V	---	2	BOARD_5V	---
3	LCD_VCC	---	4	LCD_VCC	---
5	Unregulated_VCC	---	6	Unregulated_VCC	---
7	BLCD_DATA0	169*	8	BLCD_DATA1	167*
9	BLCD_DATA2	166*	10	BLCD_DATA3	165*
11	BLCD_DATA4	164*	12	BLCD_DATA5	163*
13	BLCD_DATA6	162*	14	BLCD_DATA7	161*
15	BLCD_DATA8	160*	16	BLCD_DATA9	158*
17	BLCD_DATA10	155*	18	BLCD_DATA11	153*
19	BLCD_DATA12	152*	20	BLCD_DATA13	151*
21	BLCD_DATA14	150*	22	BLCD_DATA15	149*
23	BLCD_DON	148*	24	BLCD_HSYNC	147*
25	BLCD_DOTCLK	137*	26	BLCD_MDISP	138*
27	BLCD_VSYNC	139*	28	DLCDD4 (LCD CLK)	140
29	BSSCK0	213**	30	SSI0	212***
31	BSS00	211**	32	BSSCS0	210**
33	BLCD_RESn	59*	34	GROUND	---
35	BLCD_VCPWC	142*	36	BLCD_VEPWC	145*
37	GROUND	---	38	GROUND	---
39	GROUND	---	40	GROUND	---

* - These CPU pins are externally buffered (U15 and U16).

** - These CPU pins are externally buffered and multiplexed (Please refer to Table 6-10 for more details).

*** - These pins are externally multiplexed (Please refer to Table 6-10 for more details).

Table 6-8 LCD Header J14

6.10. SSI

The serial sound interface (SSI) is a module designed to send or receive audio data interface with various devices offering Philips format compatibility. It also provides additional modes for other common formats, as well as support for multi-channel mode. Both transmitter and receiver modules are embedded. **Table 6-9** below details the SSI header.

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Unregulated_VCC	-	2	Board_VCC	-
3	SSISCK3	126	4	SSIWS3	125
5	SSIDATA3	124	6	AUDIOCLK*	128
7	GROUND	-			

* - Please refer to Table 6-15 for more details.

Table 6-9 SSI Header

For more details on SH7203 on-chip *Serial Sound Interface* module, please refer to SH7203 Group Hardware Manual.

6.11. Option Links

Table 6-10 to Table 6-12 below describes the function of the option links contained on this CPU board. The default configuration is indicated by **BOLD** text.

Reference	CPU Pin	Fitted	Alternative (Removed)	Related To
R55	PA7, Pin 119	Connects PIN 119 of the CPU to DA1 on JA5A and JA5B.	Disconnects PIN 119 of the CPU from DA1.	R56
R56	PA7, Pin 119	Connects PIN 119 of the CPU to AN7 on JA5A and JA5B.	Disconnects PIN 119 of the CPU from AN7.	R55

Table 6-10 Option Link for ADPOT_AN0

Reference	CPU Pin	Fitted	Alternative (Removed)	Related To
R57	PA6, Pin 118	Connects PIN 118 of the CPU to DA0 on JA1A and JA1B.	Disconnects PIN 118 of the CPU from DA0.	R61
R61	PA6, Pin 118	Connects PIN 118 of the CPU to AN6 on JA5A and JA5B.	Disconnects PIN 118 of the CPU from AN6.	R57

Table 6-11 Option Link for AN6_DA0

Reference	CPU Pin	Fitted	Alternative (Removed)	Related To
R67	PA0, Pin 110	Connects PIN 110 of the CPU to AD_POT.	Disconnects PIN 110 of the CPU from AD_POT.	R72
R72	PA0, Pin 110	Connects PIN 110 of the CPU to AN0 on JA1A and JA1B.	Disconnects PIN 110 of the CPU from AN0.	R67

Table 6-12 Option Link for AN7_DA1

6.12. DIP Switch Settings

The default configuration is indicated by **BOLD** text.

Reference	Function	ON	OFF
SW4-1	User LEDs	Port pin PE12 (CPU PIN 73) drives LED1	LED1 off
SW4-2	USB	Port Pin PE12 of the CPU controls 5V supply to the USB HOST connector.	5V supply to the USB connector is on if by SW4-3 is on, otherwise it is off.
SW4-3	USB	Host_VBUS is 5V.	5V supply to the USB connector is controlled by Port pin PE12 if SW4-2 is on, otherwise it is off

Note: Do not set SW4-2 and SW4-3.

Table 6-13 LED1 and USB power control.

Reference	Function	ON	OFF
SW4-4	USB	VBUS (pin 102) of the CPU monitors Host VBUS.	HOST_VBUS_FLAG is disconnected from VBUS (pin 102) of the CPU.
SW4-5	USB	VBUS (pin 102) of the CPU monitors Device VBUS.	DEVICE_VBUS is disconnected from VBUS (Pin 102) of the CPU.

Please note that only one switch can be set to ON.

Table 6-14 VBUS connection

Reference	Function	ON	OFF
SW4-6	SSI	PF30 (Pin 128) of the CPU can be used as AUDIOCLK signal on J2.	AUDIOCLK signal on J2 is disconnected from Pin 128 of the CPU.
SW4-7	RCAN	PF30 (Pin 128) of the CPU can be used as CAN1_EN.	Pin 128 of the CPU can not be used as CAN1_EN signal.

Please note that only one switch can be set to ON.

Table 6-15 PF30 function select

Reference	Function	ON	OFF
SW4-8	CLOCK Mode	The MD_CLK0 (Pin 97) of the CPU logic 0	The MD_CLK0 (Pin 97) of the CPU logic 1
SW4-9	CLOCK Mode	The MD_CLK1 (Pin 96) of the CPU logic 0	The MD_CLK1 (Pin 96) of the CPU logic 1

Table 6-16 Clock mode settings

Reference	Function	ON	OFF
SW4-10	BUS Interface	16 bit bus interface is selected for SDRAM access. Port functions on upper 16 bits.	32 bit bus interface is selected for SDRAM access.

Table 6-17 32 bit/16 bit select

Reference	Function	ON	OFF
SW5-1	LCD / NAND FLASH	Pin 147 of the CPU is connected to NAND_CS _n pin of NAND Flash.	NAND flash disabled

Table 6-18 NAND Flash enable

Reference	Function	ON	OFF
SW5-2	External ROM	Disables writing to the External Flash memory.	Enables writing to the External Flash memory.

Table 6-19 Flash protection

Reference	Function	ON	OFF
SW5-3	User LEDs	Port pin PC14 (CPU PIN 75) can be used to drive LED2.	LED 2 off
SW5-4	Bus Interface	Pin 75 of the CPU can be used as WAITn input available on JA3A-49.	Pin 75 of the CPU can not be used as WAITn input.

Table 6-20 LED2 / WAITn control

Reference	Function	ON	OFF
SW5-5	User LEDs	Port pin PE11 (CPU PIN 72) can be used to drive LED3.	LED3 off.
SW5-6	Bus Interface	Pin 72 of the CPU can be used as CS6n output.	Pin 72 of the CPU can not be used as CS6n output.

Table 6-21 LED3 / CS6n

Reference	Function	ON	OFF
SW5-7	Bus interface	Pin 17 of the CPU can be used as A0 address output.	Pin 17 of the CPU can not be used as A0 address output.
SW5-8	AUD interface	Pin 17 of the CPU can be used as AUDSYCNn output.	Pin 17 of the CPU can not be used as AUDSYCNn output.

Please note that only one switch can be set to ON.

Table 6-22 A0/AUDSYCNn selection

Reference	Function	ON	OFF
SW5-9	Application Headers	Pin 192 of the CPU (ADTRGn) is connected to user switch SW3.	Pin 192 of the CPU (ADTRGn) is disconnected from user switch SW3.
SW5-10	Application Headers	Pin 192 of the CPU is connected to EXT_ADTRG available on JA1A-8.	Pin 192 of the CPU is disconnected from EXT_ADTRG.

Please note that SW4-10 must be off (16 Bit mode) to enable ADTRGn

Table 6-23 ADTRGn selection

Reference	Function	ON	OFF
SW6-1	Ethernet	Pin 182 of the CPU is connected to ETH_PME pin of Ethernet controller.	Pin 182 of the CPU is disconnected from ETH_PME.
SW6-2	Application Header	Pin 182 of the CPU is connected to EXT_IRQ3n on JA1A-23.	Pin 182 of the CPU is disconnected from EXT_IRQ3n.

Please note that only one switch can be set to ON.

Table 6-24 ETH_PME /EXT_IRQ3 select

Reference	Function	ON	OFF
SW6-3	User Switches	Pin 181 of the CPU is connected to User switch SW3.	Pin 181 of the CPU is connected to User switch SW3.
SW6-4	Application Header	Pin 181 of the CPU is connected to EXT_IRQ2n on JA2A-23.	Pin 181 of the CPU is disconnected from EXT_IRQ2n.

Table 6-25 SW3/EXT_IRQ2 select

Reference	Function	ON	OFF
SW6-5	User Switches	Pin 180 of the CPU is connected to User switch SW2.	Pin 180 of the CPU is connected to User switch SW2.
SW6-6	Application Header	Pin 180 of the CPU is connected to EXT_IRQ1n on JA2A-23.	Pin 180 of the CPU is disconnected from EXT_IRQ1n.
SW6-7	Bus interface	Pin 180 of the CPU is connected to RDYBYn of Flash memory.	Pin 180 of the CPU is disconnected from RDYBYn.

Table 6-26 EXT_IRQ1n/RDYBYn/SW2 select

Reference	Function	ON	OFF
SW6-8	User Switches	Pin 179 of the CPU is connected to User switch SW1.	Pin 179 of the CPU is connected to User switch SW1.
SW6-9	Application Header	Pin 179 of the CPU is connected to EXT_IRQ0n on JA2A-23.	Pin 179 of the CPU is disconnected from EXT_IRQ0n.
SW6-10	Bus interface	Pin 179 of the CPU is connected to ETH_IRQn of Ethernet controller.	Pin 179 of the CPU is disconnected from ETH_IRQn.

Table 6-27 EXT_IRQ0n/ETH_IRQ/SW1 select

Reference	Function	ON	OFF
SW7-1	Application Header	Pin 213 of the CPU is connected to TRISTn on JA2A-24.	Pin 213 of the CPU is disconnected from TRISTn.
SW7-2	SSU	Pin 213 of the CPU is connected to SSCK0.	Pin 213 of the CPU is disconnected from SSCK0.

Please note that SW4-10 must be off (16 Bit mode) to enable Port functions on this pin

Table 6-28 TRISTn/SSCK0 select

Reference	Function	ON	OFF
SW7-3	Application Header	Pin 212 of the CPU is connected to MO_UD on JA2A-11.	Pin 212 of the CPU is disconnected from MO_UD.
SW7-4	SSU	Pin 212 of the CPU is connected to SSIO.	Pin 212 of the CPU is disconnected from SSIO.

Please note that SW4-10 must be off (16 Bit mode) to enable Port functions on this pin

Table 6-29 MO_UD/SSIO select

Reference	Function	ON	OFF
SW7-5	Application Header	Pin 211 of the CPU is connected to TMR1 on JA2A-20.	Pin 211 of the CPU is disconnected from TMR1.
SW7-6	SSU	Pin 211 of the CPU is connected to SS00.	Pin 211 of the CPU is disconnected from SS00.

Please note that SW4-10 must be off (16 Bit mode) to enable Port functions on this pin

Table 6-30 TMR1/SS00 select

Reference	Function	ON	OFF
SW7-7	Application Header	Pin 210 of the CPU is connected to TMR0 on JA2A-19.	Pin 210 of the CPU is disconnected from TMR0.
SW7-8	SSU	Pin 210 of the CPU is connected to SSCS0.	Pin 210 of the CPU is disconnected from SSCS0.

Please note that SW4-10 must be off (16 Bit mode) to enable Port functions on this pin

Table 6-31 TMR1/SSCS0 select

Reference	Function	ON	OFF
SW7-9	RCAN	Pin 209 of the CPU is connected to CAN1_STBn of the RCAN transceiver.	Pin 209 of the CPU is disconnected from CAN1_STBn.
SW7-10	Application Header	Pin 209 of the CPU is connected to SCK2 on JA6A-11.	Pin 209 of the CPU is disconnected from SCK2.

Please note that SW4-10 must be off (16 Bit mode) to enable ADTRGn

Table 6-32 CAN1_STBn/Serial clock2 select

6.13. Oscillator Sources

A crystal oscillator is fitted on the CPU board and used to supply various clock inputs to the Renesas microcontroller. **Table 6-33** details the oscillators that are fitted and alternative footprints provided on this CPU board:

Reference		Component
Crystal (X1)	Fitted	16.6675 MHz (HC49/4H package)
Crystal (X2)	Fitted	32.768 kHz (90SMX package)
Crystal (X3)	Fitted	24.576 MHz (HC49/4H)
Crystal (X4)	Fitted	48 MHz (HC49/4H package)

Table 6-33 Crystal Oscillators

6.14. Reset Circuit

The CPU Board includes a Reset IC MAX6863 (U3) to meet the minimum reset period of 10ms. Please refer to the hardware manual for more information on the requirements of the reset circuit. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7. Modes

This CPU board supports four clock modes. Please refer to Table 7-1 for clock mode selection.

SW4-9 (CPU Pin 96, MD_CLK1)	SW4-8 (CPU Pin 97, MD_CLK0)	Clock Mode
ON	ON	0
ON	OFF	1
OFF	ON	2
OFF	OFF	3

Table 7-1 Clock Mode Selection

- a. **Clock Mode 0** – This is the default mode on RSK+SH7203. In mode 0, clock is input from the EXTAL pin or the crystal oscillator. The PLL circuit shapes waveforms and the frequency is multiplied according to the frequency control register setting before the clock is supplied to the LSI. The oscillating frequency for the crystal resonator and EXTAL pin input clock ranges from 10 to 16.67 MHz. The frequency range of CKIO is from 40 to 66.67 MHz.
- b. **Clock Mode 1** - In mode 1, clock is input from the EXTAL pin or the crystal oscillator. The PLL circuit shapes waveform and the frequency is multiplied according to the frequency control register setting before the clock is supplied to the LSI. The oscillating frequency for the crystal resonator and EXTAL pin input clock ranges from 20 to 33.33 MHz. The frequency range of CKIO is from 40 to 66.67 MHz.
- c. **Clock Mode 2** - In mode 2, the CKIO pin functions as an input pin and draws an external clock signal. The PLL circuit shapes waveform and the frequency is multiplied according to the frequency control register setting before the clock is supplied to the LSI. The frequency range of CKIO is from 40 to 66.67 MHz.
- d. **Clock Mode 3** - In mode 3, clock is input from the USB_X1 pin or the crystal oscillator. The external clock is input through this pin and waveform is shaped in the PLL circuit. Then the frequency is multiplied according to the frequency control register setting before the clock is supplied to the LSI. The frequency of CKIO is the same as that of the input clock (USB_X1/crystal resonator) (48 MHz).

Warning - While changing the clock mode please ensure that correct Frequency Multiplication/division Ratios are set in the FROCR register. Permanent damage may occur to the CPU due to overheat if incorrect clock is selected.

Chapter 8. Programming Methods

The RSK+SH7203 board can be programmed using E10A-lite supplied with the kit. Following headers are provided to download and debug the user code – H-UDI and AUD.

8.1. H-UDI Header for E10A

This is a 14 pin header used to download and debug the user program. This header provides H-UDI interface for user debugging. Limited Event conditions in ROM and unlimited Breakpoints in RAM are supported. The AUD trace function is not supported. Since the 14-pin type connector is smaller than the 36-pin type (1/2.5), the area where the connector is installed on the user system can be reduced.

8.2. AUD Header for E10A

This is a 36 pin header used to download and debug the user program. This header provides additional AUD trace functions for user debugging. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing. Limited Event conditions in ROM and unlimited Breakpoints in RAM are supported.

User system interface cable for AUD header is not provided with this CPU board. This can be purchased at additional cost from the local Renesas distributor. A list of worldwide Renesas distributors is available on the Renesas website - www.renesas.com

Chapter 9. Headers

9.1. Application Headers

Table 9-1 to Table 9-5 below show the standard application header connections.

Note: Switch ID is specified in brackets where the connection is via a DIP switch.

Note: Asterisk indications apply to all tables in this section

* marks pins where a link to the microcontroller pin is via an option link

** marks pins where the signal is only valid in 16 bit SDRAM mode

*** marks pins where a link to the microcontroller pin is via a 100R resistor and to BOARD VCC via a 4k7 resistor (100R ID & 4k7 ID)

JA1A and JA1B							
Pin	Header Name	CPU board Signal Name	Device Pin / DIP S/W	Pin	Header Name	CPU board Signal Name	Device Pin / DIP S/W
1	5V	CON_5V	---	2	0V (5V)	GROUND	---
3	3V3	CON_3V3	---	4	0V (3V3)	GROUND	---
5	AVcc	AVCC	114	6	AVss	AVSS	120
7	AVref	AVREF	116	8	ADTRG	EXT_ADTRG	192 (SW5-10)
9	ADC0	AN0*	110	10	ADC1	AN1	111
11	ADC2	AN2	112	12	ADC3	AN3	113
13	DAC0	DA0*	118	14	DAC1	DA1*	119
15	IO Port0	LCD_DATA0_IO0	169	16	IO Port1	LCD_DATA1_IO1	167
17	IO Port2	LCD_DATA2_IO2	166	18	IO Port3	LCD_DATA3_IO3	165
19	IO Port4	LCD_DATA4_IO4	164	20	IO Port5	LCD_DATA5_IO5	163
21	IO Port8	LCD_DATA6_IO6	162	22	IO Port7	LCD_DATA7_IO7	161
23	IRQ3	EXT_IRQ3n	182 (SW6-2)	24	I ² C Bus (3 rd pin)	JA1_PIN24	---
25	IIC_SDA	SDA2***	186	26	IIC_SCL	SCL2***	185

Table 9-1: JA1A / JA1B Standard Generic Header

JA2A and JA2B							
Pin	Header Name	CPU board Signal Name	Device Pin / DIP S/W	Pin	Header Name	CPU board Signal Name	Device Pin / DIP S/W
1	RESn	RESn	59	2	EXTAL	CON_EXTAL	
3	NMI	NMIIn	57	4	VSS1	VSS1 (GND)	---
5	WDT Overflow	---	---	6	SCl _a TX	TxD0	63
7	IRQ0	EXT_IRQ0	179 (SW6-9)	8	SCl _a Rx	RxD0	49
9	IRQ1	EXT_IRQ1	180 (SW6-6)	10	SCl _a CK	JA2_PIN10	---
11	UD	MO_UD**	212 (SW7-3)	12	CTSRTS	JA2_PIN12	---
13	Up	MO_Up**	193	14	Un	MO_Un**	194

15	Vp	MO_Vp**	195	16	Vn	MO_Vn**	197
17	Wp	MO_Wp**	202	18	Wn	MO_Wn**	203
19	TMR0	TMR0**	51 (SW7-7)	20	TMR1	TMR1**	211 (SW7-5)
21	TRIGa	TRIGa**	31	22	TRIGb	TRIGb**	208
23	IRQ2	EXT_IRQ2n	181 (SW6-4)	24	TRISTn	TRISTn**	213 (SW7-1)
25	SPARE PIN	---	---	26	SPARE PIN	---	---

Table 9-2: JA2A / JA2B Standard Generic Header

JA3A and JA3B							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	A0	BA(0)	-	2	A1	BA(1)	-
3	A2	BA(2)	-	4	A3	BA(3)	-
5	A4	BA(4)	-	6	A5	BA(5)	-
7	A6	BA(6)	-	8	A7	BA(7)	-
9	A8	BA(8)	-	10	A9	BA(9)	-
11	A10	BA(10)	-	12	A11	BA(11)	-
13	A12	BA(12)	-	14	A13	BA(13)	-
15	A14	BA(14)	-	16	A15	BA(15)	-
17	D0	BD(0)	-	18	D1	BD(1)	-
19	D2	BD(2)	-	20	D3	BD(3)	-
21	D4	BD(4)	-	22	D5	BD(5)	-
23	D6	BD(6)	-	24	D7	BD(7)	-
25	RDn	BRDn	-	26	WRn	BWRn	-
27	CS1n	BCS2n	-	28	CS2n	BCS5n	-
29	D8	BD(8)	-	30	D9	BD(9)	-
31	D10	BD(10)	-	32	D11	BD(11)	-
33	D12	BD(12)	-	34	D13	BD(13)	-
35	D14	BD(14)	-	36	D15	BD(15)	-
37	D16	BD(16)	-	38	D17	BD(17)	-
39	D18	BD(18)	-	40	D19	BD(19)	-
41	D20	BD(20)	-	42	D21	BD(21)	-
43	D22	BD(22)	-	44	SDCLK	BCLKIO	-
45	CS2n	BCS6n	-	46	ALE	JA3_PIN46	-
47	WRHn	BWR1n	-	48	WRLn	BWR0n	-
49	WAITn	WAIT	-	50	Reserved	JA3_PIN50	---

Table 9-3: JA3A / JA3B Standard Generic Header

JA5A and JA5B							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	AD4	AN4	115	2	AD5	AN5	116
3	AD6	AN6*	118	4	AD7	AN7*	119
5	CAN1TX	CTx0	86	6	CAN1RX	CRx0	85
7	CAN2TX	CTx1	88	8	CAN2RX	CRx1	87
9	AD8	JA5_PIN9	---	10	AD9	JA5_PIN10	---
11	AD10	JA5_PIN11	---	12	AD11	JA5_PIN12	---
13	TIOC0A	JA5_PIN13	---	14	TIOC0B	JA5_PIN14	---
15	TIOC0C	JA5_PIN15	---	16	M2_TRISTn	JA5_PIN16	---
17	TCLKC	JA5_PIN17	---	18	TCLKD	JA5_PIN18	---
19	M2_Up	JA5_PIN19	---	20	M2_Un	JA5_PIN20	---
21	M2_Vp	JA5_PIN21	---	22	M2_Vn	JA5_PIN22	---
23	M2_Wp	JA5_PIN23	---	24	M2_Wn	JA5_PIN24	---

Table 9-4: JA5A / JA5B Standard Generic Header

JA6A and JA6B							
Pin	Header Name	CPU board Signal Name	Device Pin	Pin	Header Name	CPU board Signal Name	Device Pin
1	DREQ	DREQ0	201	2	DACK	DACK0	200
3	TEND	TEND0	199	4	STBYn	JA6_PIN4	---
5	RS232TX	RS232TX	---	6	RS232RX	RS232RX	---
7	SClBRx	RxD1	64	8	SClBTX	TxD1	66
9	SClCTx	TxD2	69	45	SClBCK	JA6_PIN10	---
11	SClCCK	SCK2	62 (SW7-10)	73	SClCRX	RxD2	68
13	Reserved	JA6_PIN13	---	14	Reserved	JA6_PIN14	---
15	Reserved	JA6_PIN15	---	16	Reserved	JA6_PIN16	---
17	Reserved	JA6_PIN17	---	18	Reserved	JA6_PIN18	---
19	Reserved	JA6_PIN19	---	20	Reserved	JA6_PIN20	---
21	Reserved	JA6_PIN21	---	22	Reserved	JA6_PIN22	---
23	Reserved	JA6_PIN23	---	24	Reserved	JA6_PIN24	---

Table 9-5: JA6A / JA6B Standard Generic Header

Chapter 10. Code Development

10.1. Overview

Note: For all code debugging using Renesas software tools, the CPU board must be connected to a PC USB port via an E10A lite. An E10A lite is supplied with the RSK product.

This RSK+ board supports both H-UDI and AUD interface. E10A lite supplied with the kit is an on-chip debugging emulator which supports only H-UDI interface of the target device. The H-UDI uses a 14-pin interface and marked as *E10A* on the RSK+SH7203 board. The E10A lite debugger does not support AUD - Advance User Debugging (36 pin) functionality. The E10A debugger (HS0005KCU02H) supporting AUD function can be purchased separately at additional cost.

For more information on E10A lite debugger please refer to the E10A lite.

Due to the continuous process of improvements undertaken by Renesas the user is recommended to review the information provided on the Renesas website at www.renesas.com to check for the latest updates to the Compiler and Debugger manuals.

10.2. Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 256k code and data. To use the compiler with programs greater than this size you will need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3. Breakpoint Support

Limited Event Conditions can be located in ROM code which is directly supported by E10A emulator. To enable breakpoints in RAM following command needs to be included in the script –

```
> SH2A_SBSTK enable
```

For more information on this, please refer to the *SuperH™ Family E10A-USB Emulator Additional Document for User's Manual* for SH7201/ SH7203.

10.4. Memory Map

The memory map shown in this section visually describes the memory areas of RSK+SH7203.

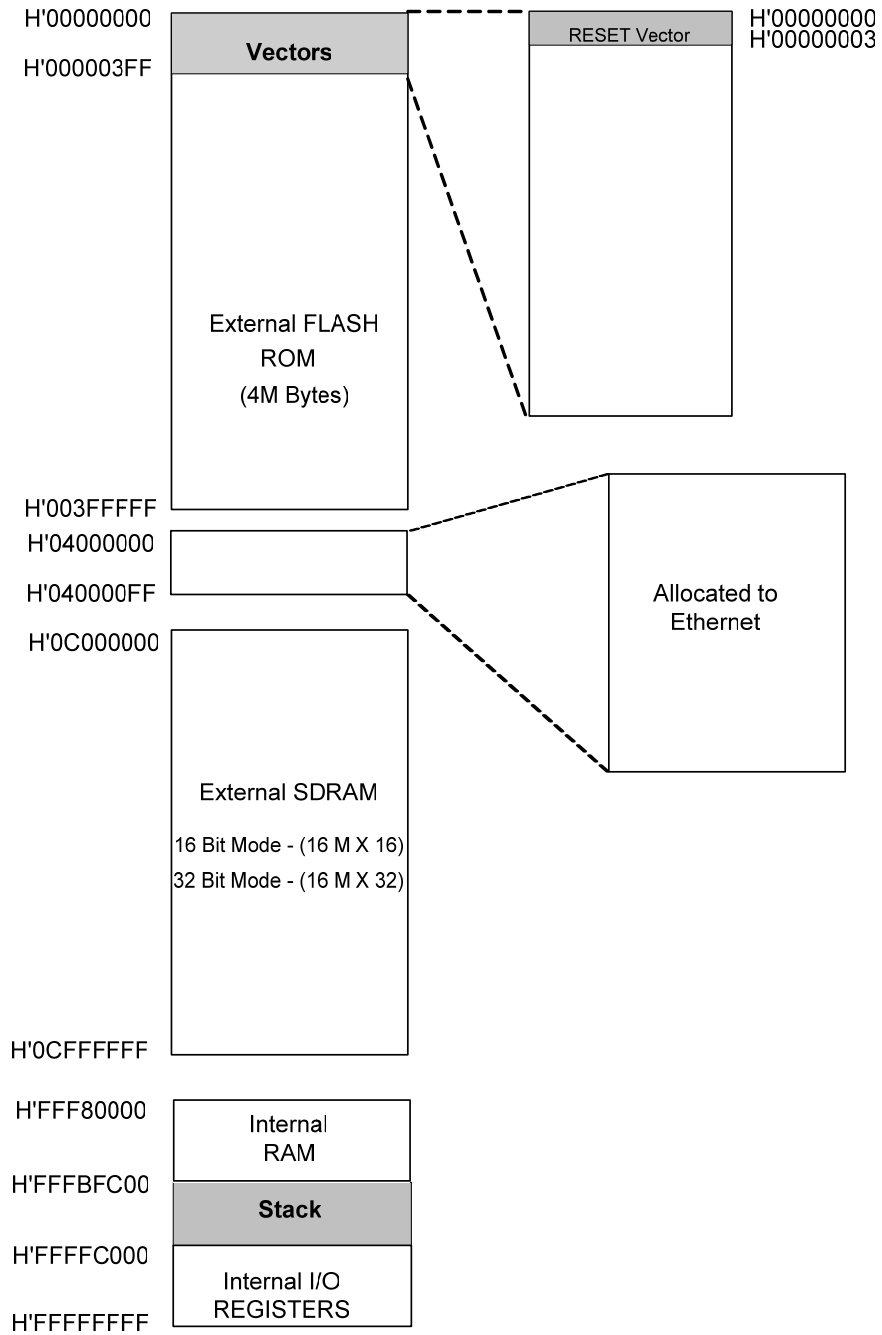


Figure 10-1: Memory Map

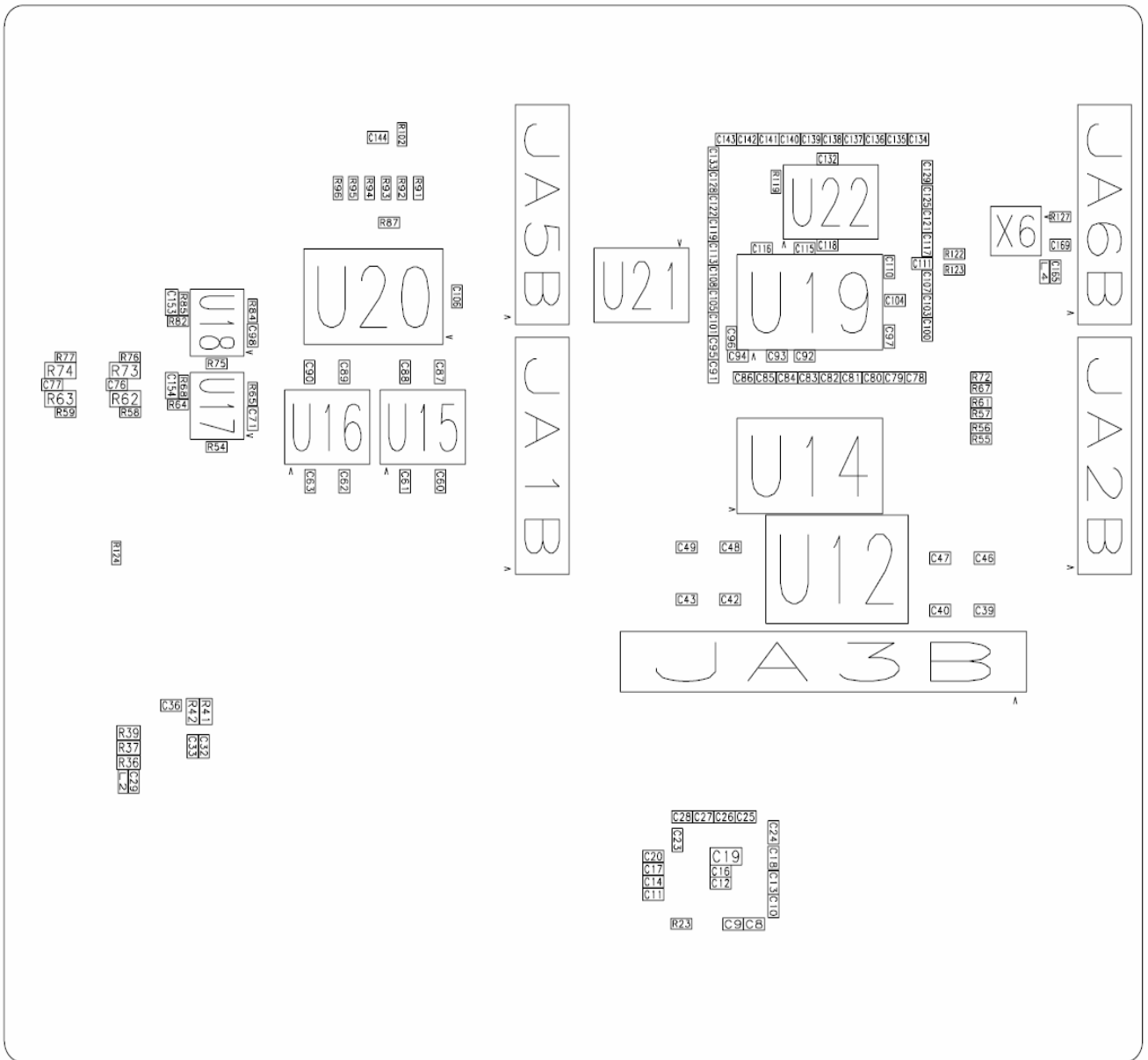


Figure 11-2: Component Placement (Bottom Layer)

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or installed in the Manual Navigator.

For information about the SH7203 microcontrollers refer to the SH7203 Group *Hardware Manual*

For information about the SH7203 assembly language, refer to the SH2A, SH2A-FPU *Software Manual*

Online technical support and information is available at: http://www.renesas.com/renesas_starter_kits

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