User's Manual

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RZ/A1H Group

Renesas Starter Kit+ User's Manual For DS-5

(ASSAM)

RENESAS MCU
Family / RZ/A1H Series

Renesas Electronics
www.renesas.com

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Precautions

The following precautions should be observed when operating any RSK product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   - The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the RSK+ hardware functionality, and electrical characteristics. It is intended for users designing sample code on the RSK+ platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product, but does not intend to be a guide to embedded programming or hardware design. Further details regarding setting up the RSK+ and development environment can found in the tutorial manual.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RZ/A1H Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK hardware.	RSK+RZA1H User's Manual	R20UT2587EG
Quick Start Guide	Provides simple instructions to setup the RSK and run the first sample, on a single A4 sheet.	RSK+RZA1H Quick Start Guide	R20UT2588EG
Schematics	Full detail circuit schematics of the RSK.	RSK+RZA1H Schematics	R20UT2586EG
Hardware Manual	Provides technical details of the RZ/A1 microcontroller.	RZ/A1H Group User's Manual: Hardware	R01UH0403EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
SEGGER JLink-Lite	On-chip Debugger
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
I^2C, IIC	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
KR	Key Return
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MCU	Micro-controller Unit
n/a	Not applicable
n/c	Not connected
PC	Personal Computer
QSPI	Quad Serial Peripheral Interface
RSK	Renesas Starter Kit
RSK+	Renesas Starter Kit Plus
SAU	Serial Array Unit
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microcontrollers. This manual describes the technical details of the RSK+ hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microcontroller programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample application
- Sample peripheral device initialisation code

The RSK+ board contains all the circuitry required for microcontroller operation.

2. Power Supply

2.1 Requirements

This RSK+ is supplied with a SEGGER JLink-Lite debugger. This board is supplied with a 5Vdc supply using a 5.0mm barrel power jack. The board can operate with a supply of up to 12Vdc if required, with appropriate changes to jumper settings as detailed in Table 2.1.

Ensure to check the three pin PWR_SEL jumper settings prior to connecting the power supply.

Details of the power supply requirements for the RSK+, and configuration are shown in Table 2-1 below. The default RSK+ power configuration is shown in **bold, blue text.**

It is essential that if a 12V supply is used that PWR_SEL is ***NOT*** linked on pins 2-3 or an overvoltage will be applied to the MCU and associated devices, resulting in likely destruction of the whole board

CN5 Setting	PWR_SEL Setting		Regulator IC Output		
			IC	Voltage	Power Name
12V	Pin1-2 shorted		IC5	5V	BOARD_5V
			IC4	3.3V	BOARD_VCC
			IC21	1.18V	CORE_VCC
5V	**Pin2-3 shorted**		IC36	3.3V	AVREF

Table 2.1: Main Power Supply Requirements

The main power supply connected to PWR1 should supply a minimum of 5W to ensure full functionality.

When designing an RZ/A1H MCU into a new board, it should be noted that if the 3.3V supply is valid and the 1.18V core supply is not, then MCU input and output ports will be in an undefined state until the 1.18V core supply is valid. When designing the MCU power sequencing during board hardware design it is strongly advised to ensure that the 1.18V supply is valid before the 3.3V.

The 1.18V core supply on the RSK+RZA1H board is valid before the 3.3V supply, so on the RSK+RZA1H the input/output ports remain in a defined state during the power up period.

2.2 Power-Up Behaviour

When the RSK+ is purchased, the RSK+ board has the 'Release' or stand-alone code from the example tutorial software pre-programmed into the Renesas microcontroller. On powering up the board the LEDs will start to flash. After 200 flashes or after pressing any switch, the text on the LCD display will change and the LED's will begin to flash at a rate controlled by the potentiometer.

3. Board Layout

3.1 Component Layout

Figure 3-1 below shows the top component layout of the board.

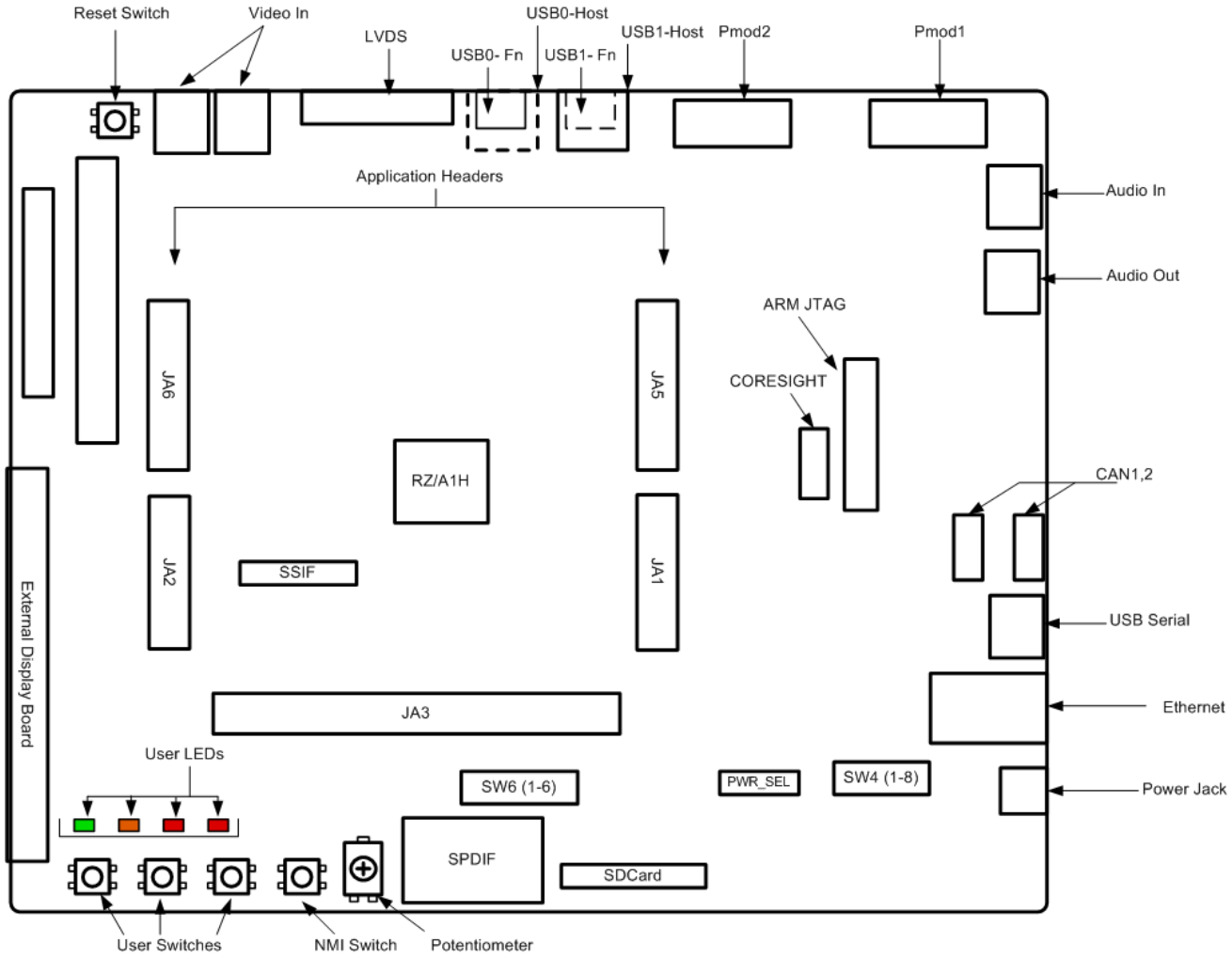


Figure 3.1: Board Layout

3.2 Board Dimensions

Figure 3-2 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 0.1 inch grid for easy interfacing.

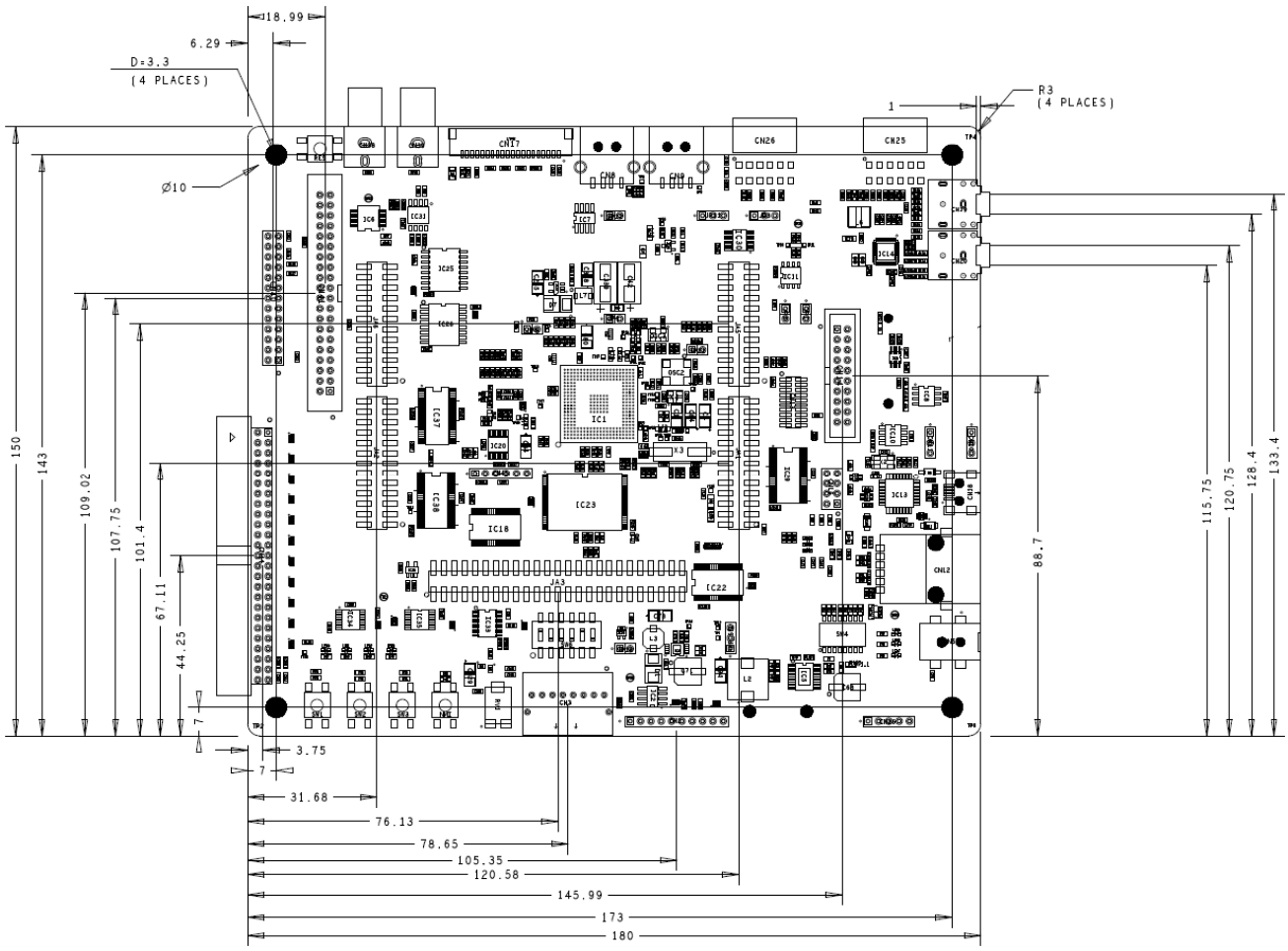


Figure 3.2: Board Dimensions

3.3 Component Placement

Figure 3-3 below shows placement of individual components on the top-side PCB. Figure 3.4 shows placement of individual components on the underside of the PCB. Component types and values can be looked up using the board schematics.

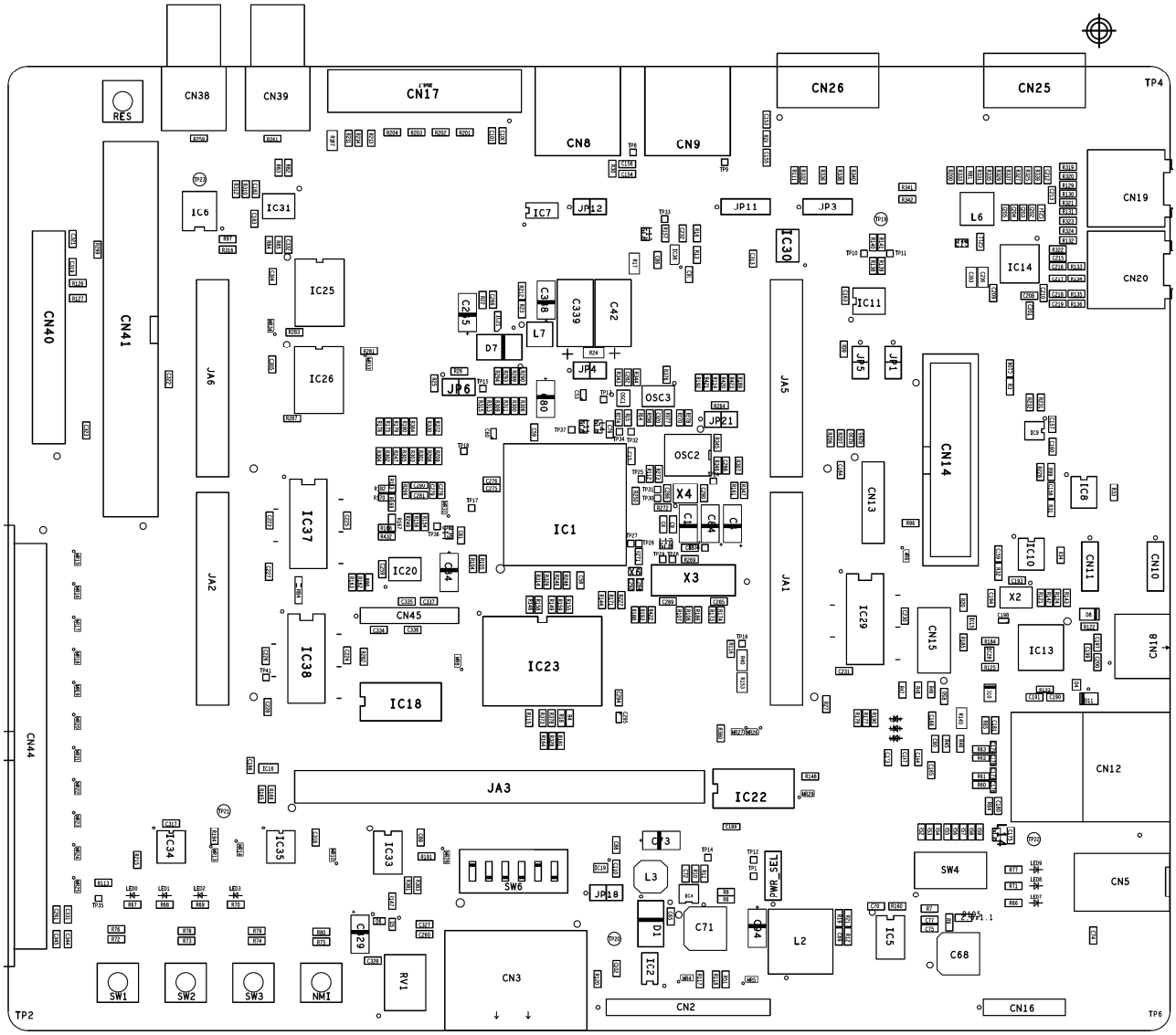


Figure 3.3: Top-Side Component Placement

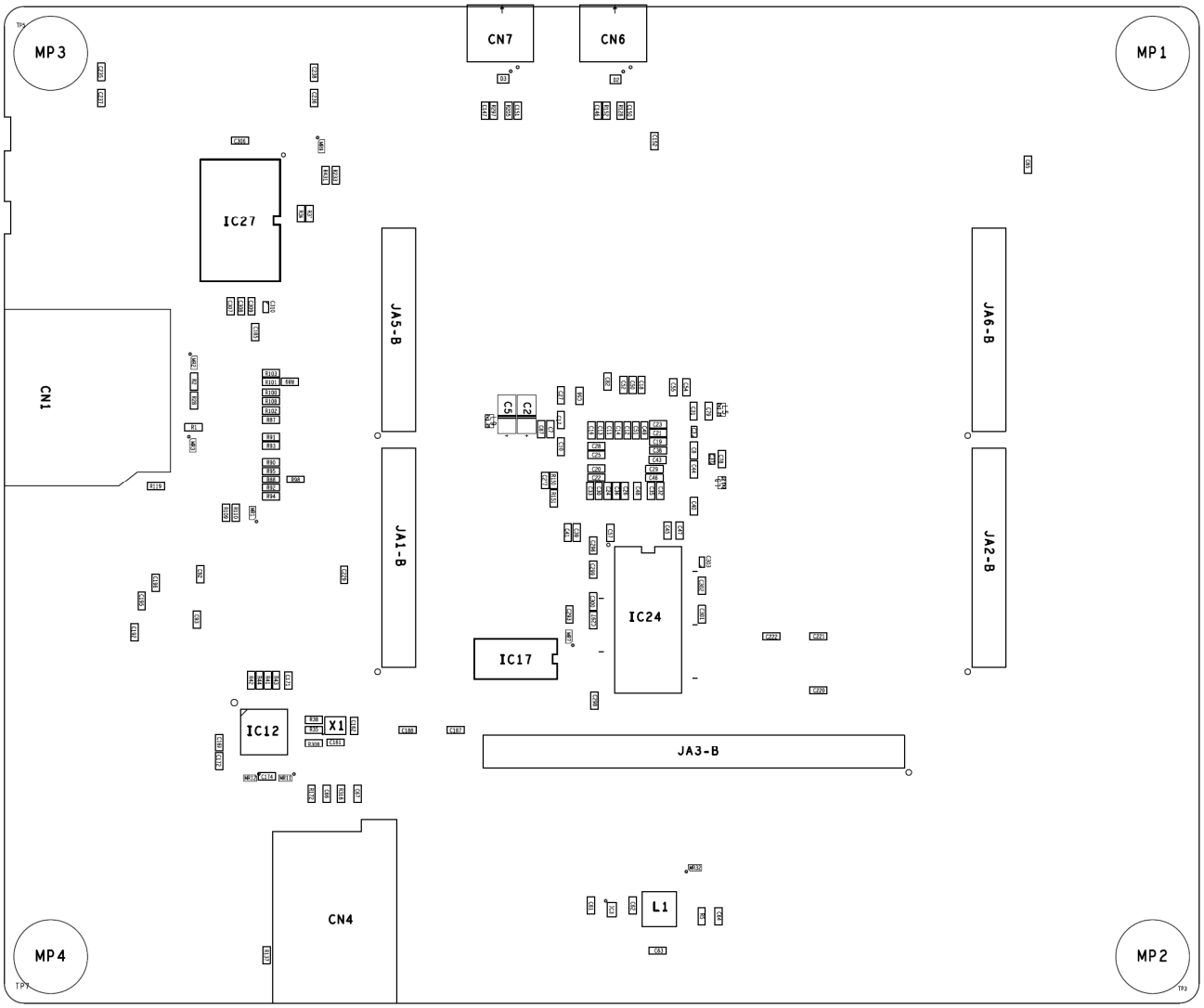


Figure 3.4: Bottom-Side Component Placement

4. Connectivity

4.1 Internal RSK Connections

The diagram below shows the RSK board components and their connectivity to the MCU.

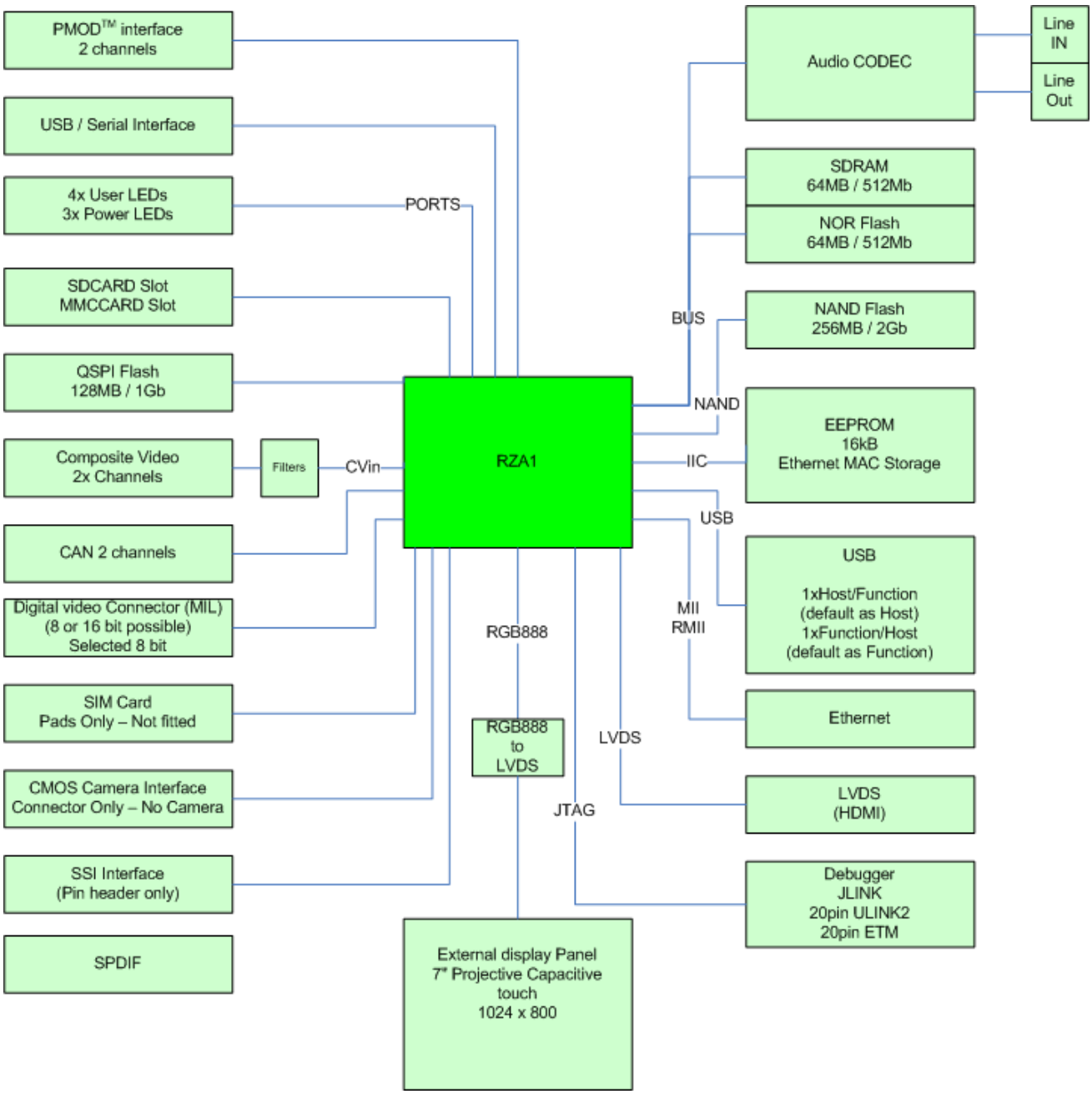


Figure 4.1: Internal RSK Block Diagram

4.2 Debugger Connections

The diagram below shows the connections between the RSK, SEGGER JLink-Lite debugger and the host PC.

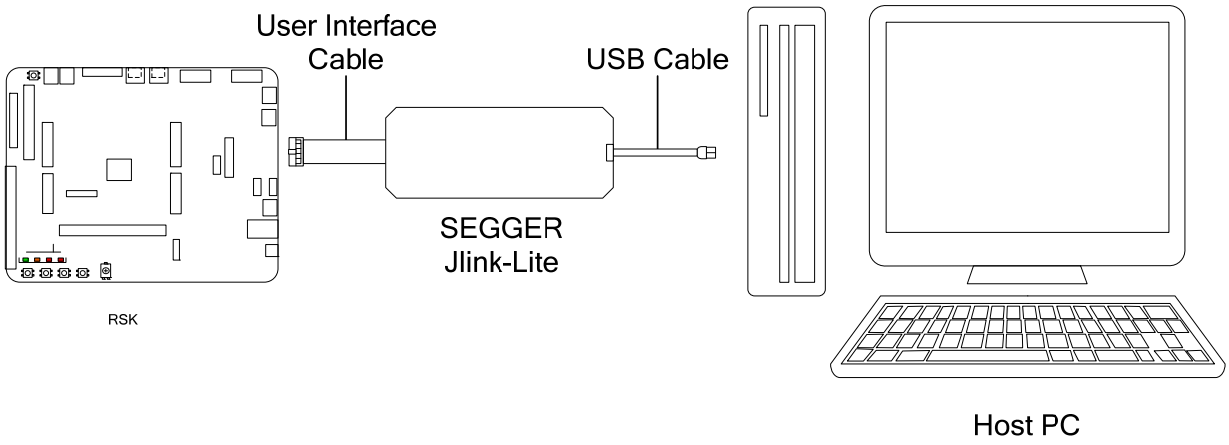


Figure 4.2: Debugger Connection Diagram

5. User Circuitry

5.1 Potentiometer

A single-turn potentiometer, RV1, is connected as a potential divider to analogue input AN7, P1_15, pin Y19. The potentiometer can be used to create a voltage between AVCC and AD_Ground.

The potentiometer is fitted to offer an easy method of supplying a variable analogue input to the microcontroller. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RZ/A1H Group Hardware Manual for further details.

5.2 Clock Circuit

Clock circuits are fitted to the RSK+ to generate the required clock signals to drive the MCU, and associated peripherals. Refer to the RZ/A1H Group Hardware Manual for details regarding the clock signal requirements, and the RSK+RZA1H board schematics for information regarding the clock circuitry in use on the RSK+. Details of the oscillators fitted to the board are listed in Table 5-1 below.

Crystal/Oscillator	Function	Default Placement	Frequency	Device Package
OSC2	Main MCU oscillator.	Fitted	13.333MHz	SOJ 4Pin
OSC1	Audio oscillator.	Fitted	22.5792MHz	TXC_TD_2P5X2
OSC3	Video oscillator.	Fitted	27.000MHz	QFN4
X6	RTC 1 clock	Fitted	32.768kHz	ABS06
X3	RTC 2 clock	Fitted	4.000MHz	HC-49
X4	USB Clock	Fitted	48.000MHz	FA-238

Table 5.1: Oscillators

5.3 RCA Video Input

The RSK+ board provides two channels of RCA video input to the RZ/A1H MCU, on connectors CN38 and CN39. These connect to the RSK+RZA1H MCU on pins VIN1A, B15 and VIN2A, A15 respectively, via 100nF decoupling capacitors. Refer to the RSK+RZA1H board schematics for further information.

5.4 Switches

There are five switches located on the RSK+ board. The function of each switch and its connection is shown in Table 5-2. For further information regarding switch connectivity, refer to the RSK+RZA1H schematics.

Switch	Function	MCU	
		Port	Pin
RES	When pressed, the microcontroller is reset.	RES#	Y8
SW1	Connects to an IRQ input for user controls.	IRQ3 (P1_9)	AB18
SW2	Connects to an IRQ input for user controls.	IRQ2 (P1_8)	AA17
SW3	Connects to an IRQ input for user controls.	IRQ5 (P1_11)	AA18
NMI	Connects to the non-maskable input for user controls.	NMI	Y9

Table 5.2: Switch Connections

5.5 Port Expander

The RSK+ board utilises two port expander ICs, IC34 and IC35 in order to provide more I/O signals. These devices are the CAT9554 from On Semiconductor. For further information on these devices visit the On Semiconductor website at www.onsemi.com.
The port expanders provide 8 parallel I/O lines each, which can be accessed via an I^2C/SMBus serial connection. On the RSK+ board, they are able to be accessed at different addresses on I^2C channel 3 on the MCU. The I^2C logical address for IC34 is 0x40 and IC35 is 0x41. Table 5.3 details the signal connections to IC34 and Table 5.4 details the signal connections to IC35.

Port Number	Signal name	Function
0	LED1	LED output control. Output low = ON, output high = OFF
1	LED2	LED output control. Output low = ON, output high = OFF
2	LED3	LED output control. Output low = ON, output high = OFF
3	NOR_A25	Bit #25 of NOR Flash Addressing
4	PMOD1_RST	Reset line for PMOD Channel 1
5	PMOD2_RST	Reset line for PMOD Channel 2
6	SD_CONN_PWR_EN	Power supply enable for external SD card connection
7	SD_MMC_PWR_EN	Power supply enable for MMC card connection

Table 5.3: Port Expander IC34 Connection Details

Port Number	Signal name	Function
0	PX1_EN0	Multiplex control for LCD/DV Data Lines. Low = LCD, High = DV
1	PX1_EN1	Multiplex control for Ethernet/general Data Lines. Low = general, High = Ethernet.
2	TFT_CS	Chip select for TFT
3	PX1_EN3	Multiplex control for PWM timer channels and audio codec IC14 serial ADC/DAC I/O lines.
4	USB_OVR_CURRENT	Signal from USB power controller indicating overcurrent condition.
5	USB_PWR_ENA	Enable USB power supply for channel 0
6	USB_PWR_ENB	Enable USB power supply for channel 1
7	PX1_EN7	Multiplex control for Address bus line A18-A21 and sound generator outputs SGOUT0-4.

Table 5.4: Port Expander IC35 Connection Details

5.6 CAN

There are two CAN channels which connect to the MCU as listed in Table 5.5.

CAN Signal	Function	MCU	
		Port	Pin
CAN_CTX1	CAN Channel 1 Transmit	P5_10	B7
CAN_CRX1	CAN Channel 1 Receive	P5_9	A7
CAN_CTX2	CAN Channel 2 Transmit	P7_3	J3
CAN_CRX2	CAN Channel 2 Receive	P7_2	H1

Table 5.5: CAN Connection

5.7 SD/MMC

The RSK+ board provides an SD/MMC card socket, CN1. The connections are detailed in Table 5.6.

Signal	Function	MCU	
		Port	Pin
NAF1_TRACED1_SMWP1	Write Protect	P3_9	W20
NAF0_TRACED0_SMCD	Card Detect	P3_8	V19
NAF5_SMCMD	Command I/O	P3_13	R22
NAF4_SMCLK	Clock	P3_12	T22
NAF3_TRACED3_SMD0	Data 0	P3_11	T21
NAF2_TRACED2_SMD1	Data 1	P3_10	T20
NAF7_SMD2	Data 2	P3_15	R20
NAF6_TRACECLK_SMD3	Data 3	P3_14	R21
P4_0_FRE_MMCD4	Data 4	P4_0	P20
P4_1_FCLE_MMCD5	Data 5	P4_1	P22
P4_2_FALE_MMCD6	Data 6	P4_2	P21
P4_3_FWE_MMCD7	Data 7	P4_3	N22

Table 5.6: SD/MMC Connection

Note that it is not possible to boot from an SD card that is connected to the SD/MMC connector CN1. This is because the connector utilises channel 1 of the SD controller integrated in the RZ/A1 MCU. For further information, refer to the hardware manual, table 3.1.

5.8 SDRAM / NOR Flash

The RSK+ board provides 32MByte SDRAM, IC24 and 16MByte NOR Flash, IC23 connected to the address / data buses.

Note that the SDRAM as fitted on the RSK+ board is configured in hardware to use the Chip Select line CS2. The BSC module within the RZ/A1 MCU assumes a second SDRAM device will be connected also to CS3. As such it is necessary that the BSC within the RZ/A1 MCU is configured to use both CS2 and CS3 as SDRAM, even though a second SDRAM is not present on CS3, and that CS3 is not used on the expansion headers. As such option link R164 must NOT be fitted, to prevent bus conflicts. By default this link is not fitted, as this port pin is configured for LED0. For other external memory mapped devices, chip select CS1 remains available for use.
This is a known limitation of the RSK+ board. For new applications with only one SDRAM it is recommended to connect the SDRAM to CS3, which will allow single SDRAM use without issue.
See the hardware manual Bus State Controller section 8.4.3 CS2WCR(SDRAM) , p171 for further details.

Note that the NOR Flash is configured to operate on the bus control line CS0. In order for this to operate Jumper link JP18 and resistor link R314 (fitted as default) must be connected. Refer to the RSK+RZA1H board schematics for further information.

5.9 NAND Flash

The connections of the NAND FLASH are detailed in Table 5.7.

Signal	Function	MCU	
		Port	Pin
NAF0_TRACED0_SMCD	IO line 0	P3_8	V19
NAF1_TRACED1_SMWP1	IO line 1	P3_9	W20
NAF2_TRACED2_SMD1	IO line 2	P3_10	T20
NAF3_TRACED3_SMD0	IO line 3	P3_11	T21
NAF4_SMCLK	IO line 4	P3_12	T22
NAF5_SMCMD	IO line 5	P3_13	R22
NAF6_TRACECLK_SMD3	IO line 6	P3_14	R21
NAF7_SMD2	IO line 7	P3_15	R20
P4_3_FWE_MMCD7	Write Enable	P4_3	N22
P4_2_FALE_MMCD6	Address latch Enable	P4_2	P21
P4_1_FCLE_MMCD5	Command Latch Enable	P4_1	P22
P4_0_FRE_MMCD4	Read Enable	P4_0	P20
P1_2_FRB	Ready Busy	P1_2	B18
FCE_NAND	Chip Enable	P5_5	C10
RESET2_N	Write Protect	Connected to reset circuit	

Table 5.7: NAND Flash Connection

To enable boot for the NAND FLASH, set SW6 pins 1/2/3 to OFF. The NAND device is 256MByte in size, however, it should be noted however, that only 64MByte is addressable. Refer to section 6.1.5 for further details.

5.10 Dual QSPI Flash

The RSK+ board provides two 64MByte Serial Flash memory ICs, IC25 and IC26, which connect to the RZ/A1 MCU via the SPI Multi I/O Bus Controller. Signal Connections are detailed in Table 5.8 below.

Signal	Function	MCU	
		Port	Pin
SPBCLK_0	Serial Clock (Common)	P9_2	C8
P9_3_SPBSSL_0	Chip Select (Common)	P9_3	A6
RESET_N	Device Reset (Common)	Connected to reset circuit	
P9_4_SPBIO00_0	Serial Input / IO_0 (IC26 Device 0)	P9_4	B6
P9_5_SPBIO10_0	Serial Output / IO_1 (IC26 Device 0)	P9_5	C7
P9_6_SPBIO20_0	Write Protect / IO_2 (IC26 Device 0)	P9_6	A5
P9_7_SPBIO30_0	Hold / IO_3 (IC26 Device 0)	P9_7	B5
P2_12_SPBIO01_0	Serial Input / IO_0 (IC25 Device 1)	P2_12	A21
P2_13_SPBIO11_0	Serial Output / IO_1 (IC25 Device 1)	P2_13	A20
P2_14_SPBIO21_0	Write Protect / IO_2 (IC25 Device 1)	P2_14	C18
P2_15_SPBIO31_0_IRQ1	Hold / IO_3 (IC25 Device 1)	P2_15	B19

Table 5.8: SPI Flash Connection

5.10.1 QSPI Modes of Operation

There are several modes of operation of the QSPI memory in conjunction with the serial memory controller in the RZ/A1H MCU. On the RSK+ board, there are two QSPI memory devices, attached to ports 0 and 1, of the Multi I/O SPI controller's channel 0. Channel 1 is used for other functions.

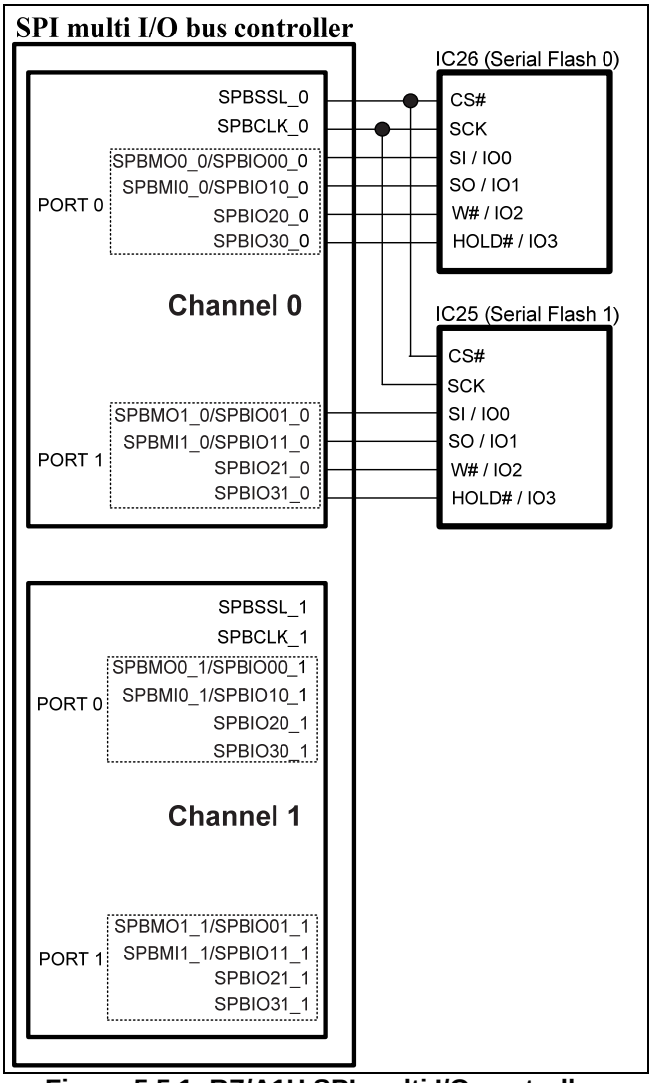


Figure 5.5.1: RZ/A1H SPI multi I/O controller.

Each QSPI memory device can support one, two or four simultaneous serial lines of I/O. Furthermore, the controller allows each channel's ports to work in parallel, providing up to eight simultaneous serial lines of I/O in dual QSPI mode. During the QSPI boot mode Port 0 is used and is accessed using only the clock, SPBMO0 and SPBMI0 signals (Single bit Single channel).

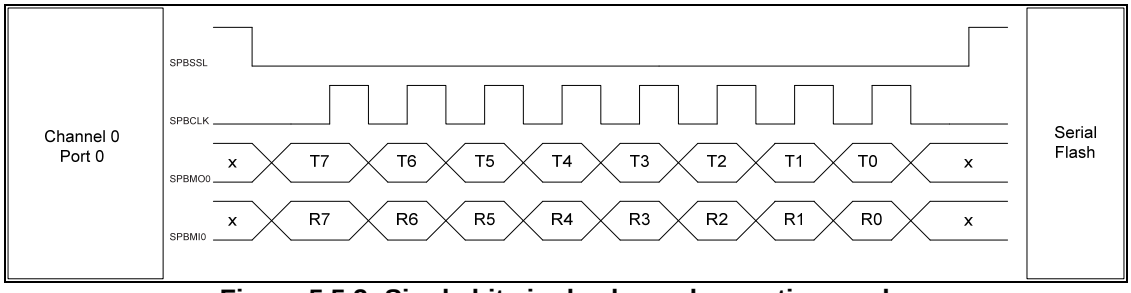


Figure 5.5.2: Single bit single channel operation mode.

It is important to recognise that these eight lines are serial inputs, and are not operating on the same byte, but successive bytes. When operating over the two ports it should be noted that the memory structure is fundamentally different from single channel operation, as lines 1-4 are working with the memory on Port 0 and 5-8 are working with Port 1. Figure 5.3 attempts to show this visually.

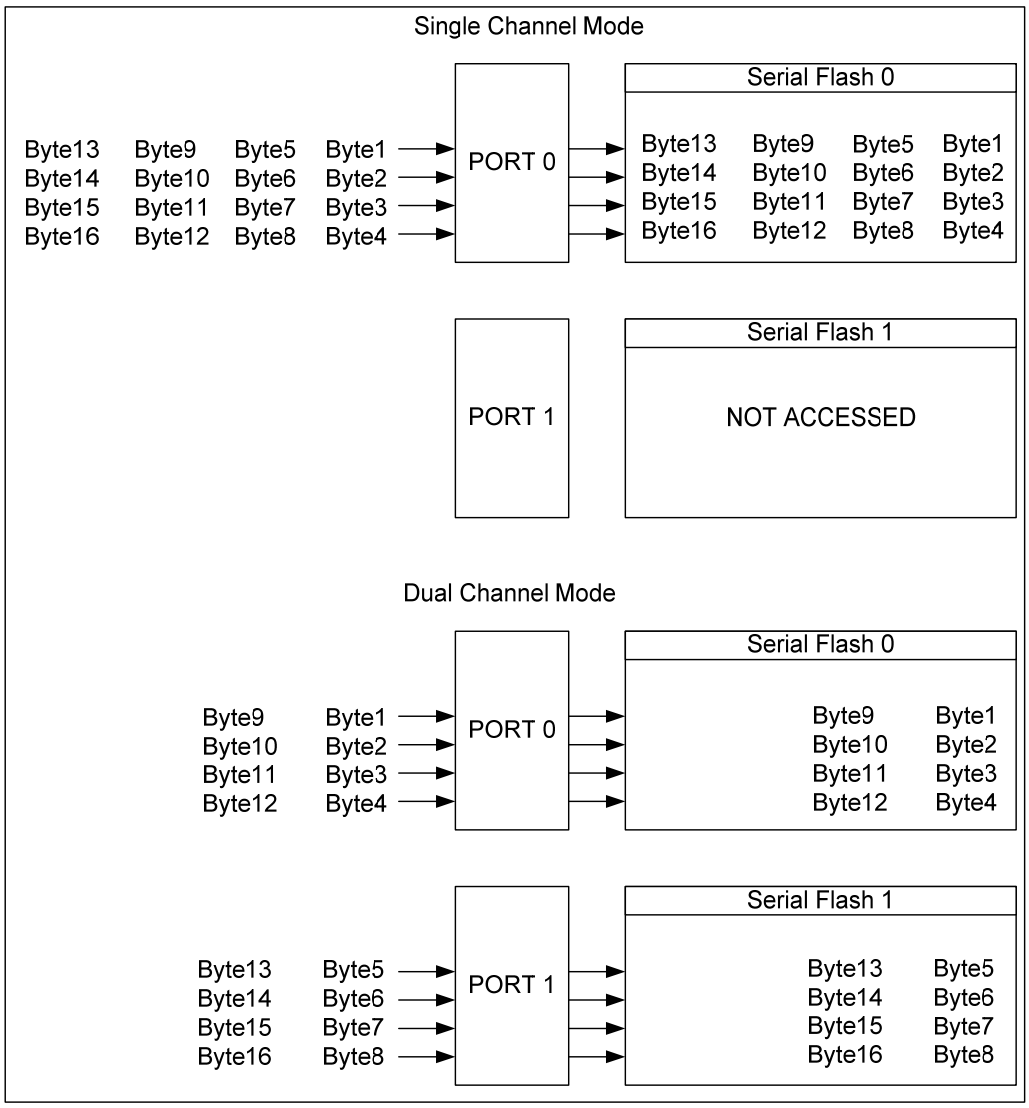


Figure 5.3: Memory access of Single and Dual Mode QSPI Operation.

The consequence of this is that data stored in QSPI FLASH needs to be accessed in the same manner as it has been programmed in. If data is accessed in Single QSPI mode when it has been programmed in Dual QSPI mode, then every fourth group of four bytes will be missing. Conversely data accessed in Dual Channel mode when it has been programmed in Single Channel mode will have blocks of four bytes from the other port inserted between every fourth byte of correct data.

5.11 Universal Serial Bus (USB)

This RSK+ board is fitted with two channels of USB. Each channel can operate as either a host or as a function device. Channel 0 is by default configured as USB Function and the connector and jumper link settings for the channel 0 power supply are shown in Table 5.10. Channel 1 is by default configured as USB Host and the connector and jumper link settings for the Channel 1 power supply are shown in Table 5.12. The signal connections to the MCU for Channel 0 and Channel 1 are detailed in Table 5.9 and Table 5.11 respectively.

Note: Default settings are shown in **bold, blue** text

USB Signal	Function	MCU	
		Port	Pin
DP0	Positive differential data signal.	DP0	AA12
DM0	Negative differential data signal.	DM0	AB12
VBUS0	Cable monitor pin.	VBUSIN0	Y12
USB_PWR_ENA	VBUS power supply enable.	Port Expander 2 IO[5] – See Table 5.4	
USB_OVR_CURRENT	Over-current detection signal	Port Expander 2 IO[4] – See Table 5.4	

Table 5.9: USB0 Module MCU Connections

Operation as USB Function	**Fit Connector CN6**	**Do Not Fit Connector CN8**
	Power from Connector CN6	**Link JP11 pins 2 and 3**
Operation as USB Host	Fit Connector CN8	Do Not Fit Connector CN6
	Power from RSK	Link JP11 pins 1 and 2

Table 5.10: USB0 Module Connector and Power Settings

USB Signal	Function	MCU	
		Port	Pin
DP1	Positive differential data signal.	DP1	AB11
DM1	Negative differential data signal.	DM1	AA11
VBUS1	Cable monitor pin.	VBUSIN1	Y11
USB_PWR_ENB	VBUS power supply enable.	Port Expander 2 IO[6] – See Table 5.4	
USB_OVR_CURRENT	Over-current detection signal	Port Expander 2 IO[4] – See Table 5.4	

Table 5.11: USB1 Module MCU Connections

Operation as USB Host	**Fit Connector CN8**	**Do Not Fit Connector CN6**
	Power from RSK	**Link JP11 pins 1 and 2**
Operation as USB Function	Fit Connector CN6	Do Not Fit Connector CN8
	Power from Connector CN6	Link JP11 pins 2 and 3

Table 5.12: USB1 Module Connector and Power Settings

Note:
- When evaluating OTG, ensure to replace the default USB connector (USB0_D) with a USB Micro-AB connector.
- Connectors such as the one manufactured by Hirose Electric with part number ZX62R-AB-5P, can be used.

5.12 Ethernet & EEPROM

This RSK+ board is fitted with an Ethernet connection. The connections from the Ethernet driver IC, IC12, are detailed in Table 5.13. Refer to the RZ/A1 board schematics for further information.

Signal	MCU	
	Port	Pin
ET_MDC	P5_9*	A7
ET_MDIO	P3_3 (**Multiplexed)	AA6
ET_IRQ	P4_14 IRQ6	G19
ET_RXCLK	P3_4 (**Multiplexed)	Y5
ET_RXD3	P2_11 (**Multiplexed)	E19
ET_RXD2	P2_10 (**Multiplexed)	B22
ET_RXD1	P2_9 (**Multiplexed)	C21
ET_RXD0	P2_8 (**Multiplexed)	D20
ET_RXDV	P3_6 (**Multiplexed)	AB3
ET_RXER	P3_5 (**Multiplexed)	AA4
ET_TXEN	P2_2 (**Multiplexed)	F21
ET_TXD0	P2_4 (**Multiplexed)	F19
ET_TXD1	P2_5 (**Multiplexed)	E22
ET_TXD2	P2_6 (**Multiplexed)	E20
ET_TXD3	P2_7 (**Multiplexed)	C22
ET_TXCLK	P2_0 (**Multiplexed)	L21
ET_TXER	P2_1 (**Multiplexed)	K22
ET_CRS	P2_3 (**Multiplexed)	G20
RESET2_N	Connected to reset circuit	
ET_COL	P1_14	AA19

*This pin is connected to the MCU via link R105 and is not fitted as default. Refer to section 6.1.8 for further details.

**These pins are connected to the MCU via a multiplexer IC IC29. Set Signal PX1_EN1 High to connect these signals to the MCU.
See section 5.20 for further details of the multiplexing on the RSK+ board.

Table 5.13: Ethernet Connection

A 2KByte EEPROM is fitted in order to store the MAC address for the Ethernet connection. This can be accessed via I^2C channel 3, with address 0xA0. Connection details are described in Table 5.14 below.

I^2C Signal	Function	MCU	
		Port	Pin
SDA3	Serial Data Line	P1_7	B16
SCL3	Clock Line	P1_6	A17

Table 5.14: EEPROM Connection on I^2C Channel 3

There is an eight-way configuration DIP switch, SW4, which is used to determine Ethernet settings on the RSK+ board. Refer to section 6.3 for further details.

5.13 LEDs

There are ten LEDs on the RSK. The function of each LED, its colour and connection are shown in Table 5.15.

LED	Colour	Function	MCU	
			Port	Pin
POWER_IN	Green	Indicates the status of the power connected to CN4.	-	-
POWER	Green	Indicates the status of the BOARD_5V (5V) power rail.	-	-
POWER	Green	Indicates the status of the BOARD_VCC (3.3V) power rail.	-	-
LED0	Green	User operated LED.	P7_1	H2
LED1	Orange	User operated LED.	*	*
LED2	Red	User operated LED.	*	*
LED3	Red	User operated LED.	*	*
LED4	Yellow	Ethernet Indication	-	-
LED5	Green	Ethernet Indication	-	-
LED6	Green	Ethernet Indication	-	-

*These LEDs are connected to port expander IC34's I/O pin. See section 5.5 for further details.

Table 5.15: LED Connections

5.14 Reset Circuit

A reset control circuit is fitted to the RSK+ to generate the required reset signal, and is triggered from the RES switch, power supply monitor and debugger connection. Refer to the RZ/A1 hardware manual for details regarding the reset signal timing requirements and the RSK+ schematics for information regarding the reset circuitry in use on the board.

5.15 Audio

The RSK+ board provides audio input via a 3.5mm Stereo jack, CN19 and audio output via 3.5mm stereo jack CN20. It also incorporates an audio codec device, IC14 which is linked to the MCU via the signals described in Table 5.16

Signal	Function	MCU	
		Port	Pin
SCL3	Clock Line	P1_6	A17
SDA3	Serial Data Line	P1_7	B16
IRQ_AUDIO	Hardware IRQ	P3_1	AA7
SSIWS0	Digital Audio Left-Right Clock IO	P4_5*	M20
SSISCK0	Digital Audio Bit Clock	P4_4*	M21
SSIRXD0	Digital Audio Serial Data ADC Output	P4_6*	L22
SSITXD0	Digital Audio Serial Data DAC Input	P4_7*	L20

*Connection to ports via multiplexer IC30. See section 5.20 for more details.

Table 5.16: Audio Codec Connections

5.16 USB Serial Port

A USB serial port implemented in another Renesas low power microcontroller (RL78/G1C) is fitted on the RSK+ to the microcontroller Serial Communications Interface (SCI) module. Multiple options are provided to allow re-use of the serial interface.
Connections between the USB to Serial converter and the microcontroller are listed in Table 5.17 below.

Signal Name	Function	MCU	
		Port	Pin
P3_0_TXD2	External SCI Transmit Signal	P3_0	AB6
P3_2_RXD2	External SCI Receive Signal.	P3_2	Y7
G1C_CTS	Clear To Send	P1_8	AA17
G1C_RTS	Request to Send	P4_14	G19

Table 5.17: Serial Port Connections

When the RSK+ is first connected to a PC running Windows with the USB/Serial connection, the PC will look for a driver. This driver is installed during the installation process, so the PC should be able to find it. The PC will report that it is installing for a driver and then report that a driver has been installed successfully, as shown in Figure 5.4. The exact messages may vary depending upon operating system.

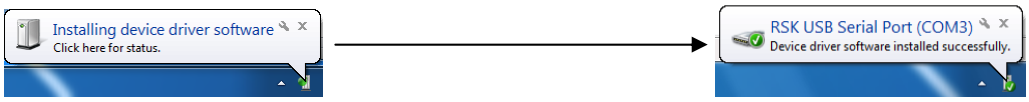
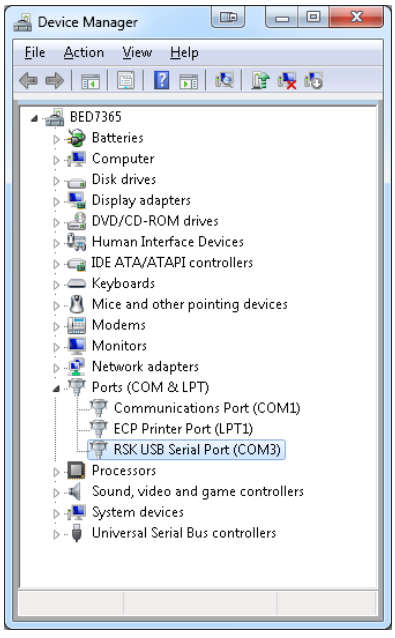


Figure 5.4 USB-Serial Windows Installation message

5.16.1 Reading the Virtual COM Port Number

In order for the PC to be able to communicate with the RSK+ board via the USB virtual COM port, the correct COM port number must be determined. If the COM port number is not known, follow this process:

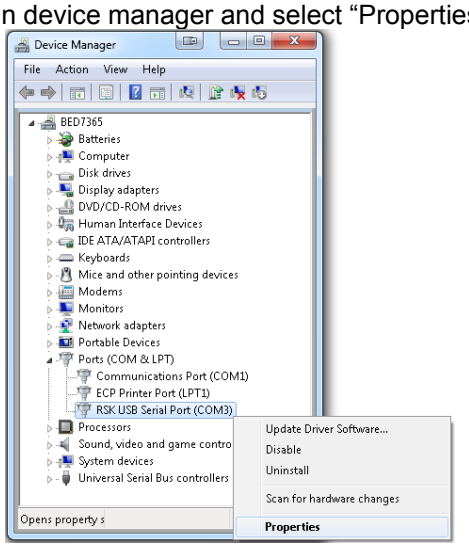
1. Connect the PC to the serial/USB port.
2. On the PC, go to Start→Control Panel→Device Manager. Go to the “Ports (COM & LPT)” section and the COM port should be listed there. To verify the correct port, the USB cable can be disconnected and re-connected to show the COM port appearing and disappearing.



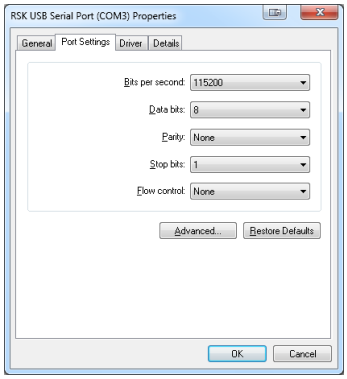
5.16.2 Changing the Virtual COM Port Number

Some PC applications will only work with particular COM port numbers. COM port numbers for the RSK+ serial/USB are assigned automatically at the time of first connection to the PC. It is possible to assign a different value manually. The procedure to do this is as follows:

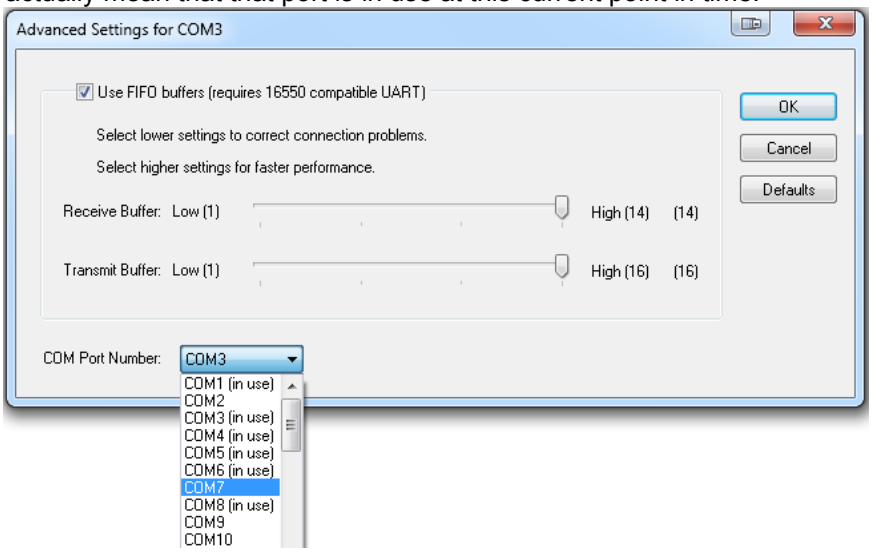
1. Right-click the USB-Serial port in device manager and select “Properties”



2. Select the “Port Settings” tab and click “Advanced…”



3. Select the new COM port from the drop down list. Bear in mind that the “in use” label on various ports listed may not actually mean that that port is in use at this current point in time.



Click OK to complete the process.

5.17 Pmod™ Module Connectors

A Pmod™ Compatible debug LCD module is supplied with the RSK+, and should be connected to the PMOD1 header.

Care should be taken when installing the LCD module to ensure pins are not bent or damaged. The LCD module is vulnerable to electrostatic discharge (ESD); therefore appropriate ESD protection should be used.

The Digilent Pmod™ Compatible header uses a SPI interface. Some RSKs will be provided with a monochrome display, others will have a colour display. Code for the appropriate display will be included in the product software support. Connection information for the Digilent Pmod™ Compatible header is provided in Table 5.18 for Pmod™ connector 1 and Table 5.19 for Pmod™ connector 2.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK designs. Details can be found in the Digilent Pmod™ Interface Specification Revision: November 20, 2011.

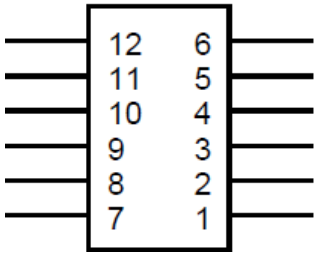


Figure 5.5: Digilent Pmod™ Compatible Header Pin Numbering

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD1_CS	P1_4	B17	7	PMOD_INT	P1_3	A18
2	P11_14_MOSI1	P11_14	H3	8	PMOD1_RST	Port Expander 1 IO[4] – See section 5.5	
3	P11_15_MISO1	P11_15	J4	9	PMOD_PIN9	P4_15	F22
4	P11_12_RSPCK1	P11_12	G2	10	PMOD_PIN10	P3_7	Y4
5	GROUND	-	-	11	GROUND	-	-
6	Board_Vcc	-	-	12	Board_Vcc	-	-

Table 5.18: PMOD1 Header Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MCU		Pin	Circuit Net Name	MCU	
		Port	Pin			Port	Pin
1	PMOD2_CS	P1_5	C16	7	PMOD_INT	P1_3	A18
2	P11_14_MOSI1	P11_14	H3	8	PMOD2_RST	Port Expander 1 IO[5] – See section 5.5	
3	P11_15_MISO1	P11_15	J4	9	PMOD_PIN9	P4_15	F22
4	P11_12_RSPCK1	P11_12	G2	10	PMOD_PIN10	P3_7	Y4
5	GROUND	-	-	11	GROUND	-	-
6	Board_Vcc	-	-	12	Board_Vcc	-	-

Table 5.19: PMOD2 Header Connections

5.18 TFT LCD Panel Connector

A TFT display can connect to the RSK+ board, via connector CN44. The signals route to the MCU via multiplexers IC37 and IC38 as described by
Table **5.20**.Refer to the schematic for further information.

Connector CN44 Pin	Signal	MCU	
		Port	Pin
1	P11_7_LCD0DATA0	P11_7	M3
2	P11_6_LCD0DATA1	P11_6	M2
3	P11_5_LCD0DATA2	P11_5	L1
4	P11_4_LCD0DATA3	P11_4	L4
5	P11_3_LCD0DATA4	P11_3	C5
6	P11_2_LCD0DATA5	P11_2	B4
7	P11_1_LCD0DATA6	P11_1	C6
8	P11_0_LCD0DATA7	P11_0	A4
9	P10_15_LCD0DATA8	P10_15	D21
10	P10_14_LCD0DATA9	P10_14	D22
11	P10_13_LCD0DATA10	P10_13	F20
12	P10_12_LCD0DATA11	P10_12	E21
13	P10_11_LCD0DATA12	P10_11	H20
14	P10_10_LCD0DATA13	P10_10	H21
15	P10_9_LCD0DATA14	P10_9	J20
16	P10_8_LCD0DATA15	P10_8	J21
17	P10_7_LCD0DATA16	P10_7	M22
18	P10_6_LCD0DATA17	P10_6	N21
19	P10_5_LCD0DATA18	P10_5	N20
20	P10_4_LCD0DATA19	P10_4	N19
21	P10_3_LCD0DATA20	P10_3	AB5
22	P10_2_LCD0DATA21	P10_2	Y6
23	P10_1_LCD0DATA22	P10_1	AA5
24	P10_0_LCD0DATA23	P10_0	AB4
26	P11_15_LCD0CLK	P11_15	J4
25	RESET2_N	Connected to reset circuit	
27	P11_12_LCD0TCON2	P11_12	G2
28	P11_11_LCD0TCON3	P11_11	U3
29	P11_10_LCD0TCON4	P11_10	T3
30	P11_13_LCD0TCON1	P11_13	G1
31	P11_14_LCD0TCON0	P11_14	H3
32	P11_9_LCD0TCON5	P11_9	T2
33	P11_8_LCD0TCON6	P11_8	T1
34	BL_PWM_CTRL	P3_1 (IRQ6)	AA7

Table 5.20: TFT Signal Connections

Connector CN44 Pin	Signal	MCU	
		Port	Pin
35	SDA0	P1_1	C17
36	SCL0	P1_0	A19
37	TP_INT	P4_9	K21
38	P11_12_RSPCK1	P11_12	G2
39	P11_14_MOSI1	P11_14	H3
40	P11_15_MISO1	P11_15	J4
41	TFT_CS	Port Expander 2 [2] – See section 5.5	N/A

Table 5.20: TFT Signal Connections (continued)

5.19 LVDS

The RSK+ board provides an LVDS interface, from connector CN17. Connection details to the MCU are described in Table 5.21.

Connector CN17 Pin	Signal	Function	MCU	
			Port	Pin
5	P5_7_TXOUT0M	LVDS Channel 0 Minus Line	P5_7	B9
6	P5_6_TXOUT0P	LVDS Channel 0 Positive Line	P5_6	A9
8	P5_5_TXOUT1M	LVDS Channel 1 Minus Line	P5_5	C10
9	P5_4_TXOUT1P_X	LVDS Channel 1 Positive Line	P5_4	C11
11	P5_3_TXOUT2M	LVDS Channel 2 Minus Line	P5_3	B10
12	P5_2_TXOUT2P	LVDS Channel 2 Positive Line	P5_2	A10
14	P5_0_TXCLKOUTP	LVDS Clock Positive Line	P5_0	A11
15	P5_1_TXCLKOUTM	LVDS Clock negative Line	P5_1	B11

Table 5.21: LVDS Connections

5.20 Pin Multiplexing

The RSK+ uses multiplexing on various channels, in order to increase the amount of available I/O. Table 5.22, Table 5.23 and Table 5.24 describe the signals being multiplexed and the signals that control them.

MCU			Signal Routed to MCU	
Port	**Pin**	**Signal**	**PX1_EN1* = High**	**PX1_EN1* = Low**
P2_0	L21	P2_0_ETTXCLK	ET_TXCLK	P2_0_IO0
P2_1	K22	P2_1_ETTXER	ET_TXER	P2_1_IO1
P2_2	F21	P2_2_ETTXEN	ET_TXEN	P2_1_IO2
P2_3	G20	P2_3_ETCRS	ET_CRS	P2_1_IO3
P2_4	F19	P2_4_ETTXD0	ET_TXD0	P2_1_IO4
P2_5	E22	P2_5_ETTXD1	ET_TXD1	P2_1_IO5
P2_6	E20	P2_6_ETTXD2	ET_TXD2	P2_1_IO6
P2_7	C22	P2_7_ETTXD3	ET_TXD3	P2_1_IO7
P2_8	D20	P2_8_ETTRXD0_RSPCK4	ET_RXD0	RSPCK4
P2_9	C21	P2_9_ETRXD1_SSL40	ET_RXD1	SSL40
P2_10	B22	P2_10_ETRXD2_MOSI4	ET_RXD2	MOSI4
P2_11	E19	P2_11_ETRXD3_MISO4	ET_RXD3	MISO4
P3_3	AA6	P3_3_ETMDIO_SCICTS1	ET_MDIO	SIM_RESET
P3_4	Y5	P3_4_ETRXCLK_SCISCK0	ET_RXCLK	SIM_CLK
P3_5	AA4	P3_5_ETRXER_SCITXD0	ET_RXER	SIM_TXD
P3_6	AB3	P3_6_ETRXDV_SCIRXD0	ET_RXDV	SIM_RXD
***PX1_EN1 is connected to the MCU via port expander IC35. See section 5.5 for further details.**				

Table 5.22: Multiplexing for Signal PX1_EN1, IC29

MCU			Signal Routed to MCU	
Port	**Pin**	**Signal**	**PX1_EN3* = High**	**PX1_EN3* = Low**
P4_4	M21	P4_4_SSISCK0_PWM2E	PWM2E	SSISCK0
P4_5	M20	P4_5_SSIWS0_PWM2F	PWM2F	SSIWS0
P4_6	L22	P4_6_SSIRXD0_PWM2G	PWM2G	SSIRXD0
P4_7	L20	P4_7_SSITXD0_PWM2H	PWM2H	SSITXD0
***PX1_EN3 is connected to the MCU via port expander IC35. See section 5.5 for further details.**				

Table 5.23: Multiplexing for Signal PX1_EN3, IC30

MCU			Signal Routed to MCU	
Port	**Pin**	**Signal**	**PX1_EN7* = High**	**PX1_EN7* = Low**
P8_10	W2	P8_10_A18_SGOUT0	SGOUT0	A18
P8_11	W3	P8_11_A19_SGOUT1	SGOUT1	A19
P8_12	Y1	P8_12_A20_SGOUT2	SGOUT2	A20
P8_13	V4	P8_13_A21_SGOUT3	SGOUT3	A21
***PX1_EN7 is connected to the MCU via port expander IC35. See section 5.5 for further details.**				

Table 5.24: Multiplexing for Signal PX1_EN7, IC20

6. Configuration

6.1 Modifying the RSK

This section lists the option links that are used to modify the way RSK+ operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers.

Table 6-1 below shows the RSKRZ/A1 default configuration with respect to the peripheral functionality. **Bold, blue text** indicates the default configuration that the RSK is supplied with. It is noted that certain peripheral functions are disabled by default, as shown in Table 6.1 in the column entitled **Secondary Function**. It is possible to activate these disabled peripherals, but at the expense of the default peripheral functions as shown in the Table. Refer to the sections cited in the Table in order to perform any required modifications.

When removing soldered components, always ensure that the RSK is not exposed to a soldering iron for intervals greater than **five** seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MCU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to RZ/A1H Group Hardware Manual and RSK+RZA1H schematics for further information.

Primary Function	Secondary Function	See Section(s)
Switches	Various IRQ, Analogue lines on Application headers	6.1.1
LEDs	Timer channel TIOC0B, external bus chip select CS3	6.1.1
Various SD, switch and IRQ functions	USB / Serial RTS & CTS handshaking	6.1.9
SP/DIF	LVDS Channel 0	6.1.2
SDRAM	CAN Channel 2, timer channel TIOC1B	6.1.3
NOR FLASH	Timer channel TIOC3A	6.1.4
NAND FLASH	LVDS Channel 1	6.1.5
QSPI FLASH	Bus Address Line A0	6.1.6
CAN Channel 1	Some Ethernet lines, Misc. Connector CN15	6.1.7
Ethernet	ADC Line for App header, CAN channel 1	6.1.8
Audio Codec	IRQ for port expander / TFT PWM control	6.1.11
LVDS	SP/DIF	6.1.12
PMOD Interfaces	Various SD / Timer and Application Header signals	6.1.13
Various Comms lines on Application Headers, TFT I^2C Interrupt line	SD card interface	6.1.14
TFT I^2C Connection	Various IRQ lines to Application Headers	6.1.10

Table 6.1: RSK Default Configuration by Function

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. Refer to the component placement diagram (Figure 3.3, Figure 3.4) to locate the option links and jumpers. **Bold, blue text** indicates the default configuration that the RSK is supplied with.

6.1.1 Switches, Potentiometer and LED

Table 6.2 details the option links associated with the user switches, pot and LEDs.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
SW1	1_9	AB18	SW1	R192	R114 R421	JA1 Pin23	R114	---
						JA1 Pin10	R421	---
SW2	1_8	AA17	SW2	R162	R163 R86	JA2 Pin23 JA2-B Pin23	R163	--- ---
SW3	1_11	AA18	SW3	R420	R189 R423	JA5 Pin10	R189	---
						JA1 Pin12	R423	---
POT	1_15	Y19	ADPOT	R161	R347	JA1 Pin9	R347	---
LED0	7_1	H2	LED0	R328	R181 R164	JA5 Pin14	R181	---

Table 6.2: Option Link configuration for user switches, pot and LEDs

Switch bank SW4 is used to control the functionality of the Ethernet connection. Please refer to section 6.3 Ethernet Configuration on page 38 for further information.

Switch bank SW6 is used to control the boot options. Please refer to section 6.5 MCU Boot and Oscillator Configuration on page 40 for further information.

6.1.2 SP/DIF

Table 6.3 details the option links associated with SP/DIF.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
SP/DIF	5_6	A9	SPDIF_IN	CN3 R169	R170	---	---	---
	5_7	B9	SPDIF_OUT	R183	R182	---	---	---

Table 6.3: Option Link configuration for SP/DIF

6.1.3 SDRAM

Table 6.4 details the option links associated with the SDRAM.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
SDRAM	7_3	J3	CAS_SDRAM	R173	R174	---	---	---
	7_2	H1	RAS_SDRAM	R4	R18	---	---	---
	7_5	J1	WR_SDRAM	R146	R158	---	---	---
	7_4	J2	CKE_SDRAM	R115	---	---	---	---

Table 6.4: Option Link configuration for SDRAM

6.1.4 NOR FLASH

Table 6.5 details the option links associated with the NOR FLASH.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
NOR FLASH	7_8	K4	RD_NOR	R155	R159	JA2 Pin20	R159	---

Table 6.5: Option Link configuration for NOR FLASH

6.1.5 NAND FLASH

Table 6.6 details the option links associated with the NAND FLASH.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
NAND FLASH	5_5	C10	FCE_NAND	R167	R168	---	---	---

Table 6.6: Option Link configuration for NAND FLASH

6.1.6 QSPI FLASH

Table 6.7 details the option links associated with the QSPI FLASH.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
QSPI FLASH	9_2	C8	SPBCLK_0	R373	R378	---	---	---

Table 6.7: Option Link configuration for QSPI FLASH

6.1.7 CAN Channels

Table 6.8 details the option links associated with the CAN interface.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
CAN CHANNEL 1	5_10	B7	CAN_CTX1	R206	R207	JA5 Pin5	---	---
	5_9	A7	CAN_CRX1	R104	R105	JA5 Pin6	---	---
CAN CHANNEL 2	7_3	J3	CAN_CTX2	R174	R173	JA5 Pin7	---	---
	7_2	H1	CAN_CRX2	R18	R4	JA5 Pin8	---	---

Table 6.8: Option Link configuration for CAN

6.1.8 Ethernet

Table 6.9 details the option links associated with the Ethernet Functionality.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
Ethernet	1_14	AA19	ET_COL	R270	R278	JA5 Pin3	R278	---
	5_9	A7	ET_MDC	R105	R104	JA5 Pin6	R104 R105	---

Table 6.9: Option Link configuration for Ethernet

6.1.9 USB/Serial

Table 6.10 details the option links associated with the USB/Serial Interface.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
USB/Serial	4_14	G19	G1C_RTS	R190	R177 R178	---	---	---
	1_8	AA17	G1C_CTS	R86	R162 R163	JA2 Pin23 JA2-B Pin23	R163 R86	---

Table 6.10: Option Link configuration for USB/Serial

6.1.10 TFT

Table 6.11 details the option links associated with the TFT display connection.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
TFT	4_9	K21	TP_INT	R384	R289 R290	---	---	---
	1_1	C17	SDA0	R302	R304	---	---	---

Table 6.11: Option Link configuration for TFT

6.1.11 Audio Codec

Table 6.12 details the option links associated with the Audio Codec.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
Audio	3_1	AA7	IRQ_AUDIO	R106	**R107** R186	---	---	---
Audio – Line In	---	---	**LINEIN1**	**R129**	R130	CN19 Pin2 *1	---	---
	---	---	**LINEIN2**	**R131**	R132	CN19Pin3 *1	---	---
	---	---	**JACKSNS**	**R323**	R324	---	---	---
Audio – Mic In	---	---	MICL	R130	**R129**	CN19 Pin2 *1	---	---
	---	---	MICR	R132	**R131**	CN19Pin3 *1	---	---
	---	---	JACKSNS	R324	**R323**	---	---	---
Audio - Headphone o/p	---	---	**HPR**	**R133**	R134	CN20 Pin3 *1	---	---
	---	---	**HPL**	**R135**	R136	CN20 Pin2 *1	---	---
Audio – Line Out	---	---	LOUTR	R134	**R133**	CN20 Pin3 *1	---	---
	---	---	LOUTL	R136	**R135**	CN20 Pin2 *1	---	---
Audio Input Gnd	---	---	MICGND	R319	**R320**	CN20 Pin1	R319	**R320**
	---	---	AUDIO_GND	**R320**	R319	CN20 Pin1	**R320**	R319

*1 Via 1uF Decoupling Capacitor

Table 6.12: Option Link configuration for the Audio Codec

6.1.12 LVDS

Table 6.13 details the option links associated with the LVDS functionality.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
LVDS - Channel 0	5_6	A9	P5_6_TXOUT0P	R170	**R169**	CN17 Pin6	R170	**R169**
	5_7	B9	**P5_7_TXOUT0M**	**R182**	R183	CN17 Pin5	**R182**	R183
LVDS - Channel 1	5_4	C11	P5_4_TXOUT1P_X	R432	---	CN17 Pin9	R432	---
	5_5	C10	P5_5_TXOUT1M	R168	**R167**	CN17 Pin8	R168	**R167**

Table 6.13: Option Link configuration for LVDS

6.1.13 Pmod™ Interfaces

Table 6.14 details the option links associated with the Pmod™ Interfaces.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
PMOD1	3_7	Y4	PMOD_PIN10	R171	R227 R144	CN25 Pin10 CN26 Pin10	R171	---
	1_4	B17	PMOD1_CS	R301	---	CN25 Pin1	R301	---
	4_15	F22	PMOD_PIN9	R175	R176	CN25 Pin9 CN26 Pin9	R175	---
	1_3	A18	PMOD_INT	R305	R247	CN25 Pin7 CN26 Pin7	R305	---
PMOD2	3_7	Y4	PMOD_PIN10	R171	R227 R144	CN25 Pin10 CN26 Pin10	R171	---
	1_5	C16	PMOD2_CS	R303	---	CN26 Pin1	R303	---
	4_15	F22	PMOD_PIN9	R175	R176	CN25 Pin9 CN26 Pin9	R175	---
	1_3	A18	PMOD_INT	R305	R247	CN25 Pin7 CN26 Pin7	R305	---

Table 6.14: Option Link configuration for PMOD

6.1.14 SD Card

Table 6.11 details the option links associated with SD card connector CN2. Note that the SD card connector CN2 is not fitted as standard.

Function	MCU		Exclusive Function			Header Connection		
	Port	Pin	Signal	Fit	Remove	Header Pin	Fit	Remove
SD Card	4_9	K21	SD_WP_EXT	R290	R384 R289	CN2 Pin2	R290	---
	4_8	K20	SD_CD_EXT	R306	R300	CN2 Pin3	R306	---
	4_13	G21	SD_CMD_EXT	R180	R179	CN2 Pin4	R180	---
	4_12	H22	SD_CLK_EXT	R311	R309	CN2 Pin5	R311	---
	4_11	H19	SD_D0_EXT	R315	R313	CN2 Pin6	R315	---
	4_10	J22	SD_D1_EXT	R294	R293	CN2 Pin7	R294	---
	4_15	F22	SD_D2_EXT	R176	R175	CN2 Pin8	R176	---
	4_14	G19	SD_D3_EXT	R178	R177 R190	CN2 Pin9	R178	---

Table 6.15: Option Link configuration for SD Card CN2

6.2 Power Supply Configuration

Power to the RSK+RZA1H board should be applied to connector CN5, from a 5mm diameter centre positive plug, at either 5Vdc or 12Vdc.

The header PWR_SEL is used to select operation from a 12V or 5V supply.

It is essential that if a 12V supply is used that PWR_SEL is ***NOT*** linked on pins 2-3 or an overvoltage will be applied to the MCU and associated devices, resulting in likely destruction of the whole board.

Table 6.16 describes the jumper settings for the PWR_SEL header

PWR_SEL	Select Input power voltage setting
Link 1-2	Link 2-3**
12V supply	5V supply
** Do NOT connect a 12V input source to the RSK+ when PWR_SEL jumper is set to link pins 2-3	

Table 6.16: PWR_SEL Header Configuration

There are 2 headers available that can be used to measure the current taken by the MCU during operation. JP4 can be used to measure the MCU core current and JP6 can be used to measure current drawn by the MCU port pins, by shorting them via a current meter. In order to use these functions, it is necessary to remove links R24 and R26 respectively. Table 6.17 provides a summary.

JP4	MCU Core Current Measurement
Remove R24 and short JP4 with meter to measure MCU core current.	
JP6	**MCU Port Pins Current Measurement**
Remove R26 and short JP6 with meter to measure MCU port pin current.	

Table 6.17: MCU Current Measurement Headers

6.3 Ethernet Configuration

Table 6.18 below details the options configurable for the Ethernet function via the 8-way DIP switch SW4.

SW4	LAN Strap Option	Off	On	Signal name
1	Auto MDI-X Enable	1	0	ET_CRS
2	Q-Autoneg Enable	1	0	ET_RXCLK
3	Phy Adr0	0	1	ET_RXD0
4	Phy Adr1	0	1	ET_RXD1
5	Full/Half #	1	0	ET_RXD2
6	Autoneg EN	1	0	ET_RXD3
7	MII/RMII #	1	0	ET_RXER
8	Fast (J) / Std (JK)	1	0	ET_TXCLK

Table 6.18: Ethernet configuration via SW4

6.4 Jumper Link Configuration

Table 6.19 describes the jumper link option configurations available on the RSK+RZA1H board.

JP1	**Enable SIM card 2 way communication (or TX only)**		
Link			**Open**
2 way communication enabled TXD and RXD connected to SIM			**TXD to SIM only**
JP3	**Write protect NAND FLASH IC27**		
Jumper Position			
Link 1-2			Link 2-3 (R233 Not Fitted)**
NAND FLASH IC27 not write protected			NAND FLASH IC27 write protected
** Do NOT short pins 2 and 3 of JP3 when R233 is fitted (which is default configuration)			
JP4	**MCU Core Current Measurement**		
Remove R24 and short JP4 with meter to measure MCU core current.			
JP5	**Disable Ethernet MAC EEPROM write protection IC11**		
Link			**open**
EEPROM IC11 write unprotected			**EEPROM IC11 write protected**
JP6	**MCU Port Pins Current Measurement**		
Remove R26 and short JP6 with meter to measure MCU port pin current.			
JP11	**USB VBUS power select**		
Link 1-2			Link 2-3
BOARD_5V			VBUS
JP12	**USB VBUS1 power select**		
Link 1-2			Link 2-3
BOARD_5V			Power from connector, CN9 pin1 (VBUS1)
JP18	**NOR Flash Chip Enable**		
Link			Open
NOR Flash active on CS0			NOR Flash inactive
JP21	**Defining Function of BSCANP pin on RZ/A1H MCU**		
MCU		Jumper Position	
Port	Pin	**linked**	open
BSCANP	AA22	**Normal Operation (Pin held low)**	Boundary Scan (Pin pulled up to BOARD_VCC via R264 22K resistor)
PWR_SEL	**Select Input power voltage setting**		
Link 1-2			Link 2-3**
12V			5V
** Do NOT connect a 12V input source to the RSK+ when PWR_SEL jumper is set to link pins 2-3			

Table 6.19: Jumper Option descriptions

6.5 MCU Boot and Oscillator Configuration

The six-way DIP switch, SW6 provides some configuration options for the RZ/A1H MCU. Switches 1, 2 and 3 are used to set the boot mode of the RZ/A1H. Table 6.20 provides details of the available modes and the corresponding switch settings. Due to pull-up resistors in the circuit, a “1” is produced when the corresponding switch position is OFF, and a “0” is produced when it is ON.

MD_BOOT0 SW6-1	MD_BOOT1 SW6-2	MD_BOOT2 SW6-3	JP18	Boot Mode
0 ON	0 ON	*	SHORT	Boot mode 0 (CS0-space 16-bit booting) Boots the LSI from memory (bus width: 16 bits) connected to the CS0 space. Uses NOR flash (IC23).
0 ON	1 OFF	*	SHORT	Boot mode 1 (CS0-space 32-bit booting) Boots the LSI from memory (bus width: 32 bits) connected to the CS0 space. Not supported on RSK+.
1 OFF	**0 ON**	**1 OFF**	*	Boot mode 3 (serial flash booting) Boots the LSI from the serial flash memory connected to the SPI multi I/O bus space. The only way of booting this LSI chip is from channel 0 (P9_2 to P9_5) in this mode. Uses QSPI flash (IC26 only).
1 OFF	1 OFF	0 ON	*	Boot mode 4 (eSD booting) Boots the LSI from the NAND flash memory with the SD controller. The only way of booting this LSI chip is from channel 0 (P4_10 to P4_15) in this mode. Not supported on RSK+.
1 OFF	1 OFF	1 OFF	*	Boot mode 5 (eMMC booting) Boots the LSI from the NAND flash memory with the MMC controller. The only way of booting this LSI chip is from channel 0 (P3_10 to P3_15) in this mode. Uses NAND flash (IC27).

Table 6.20: MCU Boot Modes

Note that it is not possible to boot from an SD card that is connected to the SD/MMC connector CN1. This is because the connector utilises channel 1 of the SD controller, which can only boot from channel 0. For further information, refer to the hardware manual, Table 3.1 (note column order is transposed *cf*. Table 6.20).

SW6-4	Clock Signal Source
ON	EXTAL (Uses OSC2, 13.33MHz.)
OFF	USB_X1 (Uses X4, 48MHz.)

Table 6.21: Clock Signal Source

SW6-5	Spread Spectrum Clock Generator (SSCG) Mode
ON	Enables the SSCG function of the MCU’s internal PLL circuit. This function attempts to reduce EMI peak levels by slightly modulating the output frequency.
OFF	Disables the SSCG function.

Table 6.22: Spread Spectrum Clock Generator (SSCG) Mode

SW6-6 is for test purposes only (default is ON).

7. Headers

7.1 Application Headers

This RSK+ is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MCU pins.
The following tables provide details of the pin connections of these headers. Some pins will require link resistors to be fitted in order to make the connection to the specified MCU pin. These resistors are also documented in the tables, highlighted in **bold, blue** if they are fitted by default, or normal text if they are not fitted as standard.

Table 7.1 below lists the connections of the application header, JA1.

Application Header JA1, JA1-B							
Pin	**Header Name**	**MCU Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Pin**	**Link Required**
1	CON_5V	---	R27	2	0V	---	---
3	CON_3V3	---	R25	4	0V	---	---
5	CON_AVCC	---	R116	6	CON_AVSS	---	R153
7	CON_AVREF	---	R13	8	ADTRG	P1_3, A18	R247
9	ADPOT_CN	P1_15, Y19	R347	10	AN1	P1_9, AB18	R421
11	AN2	P1_10, Y17	R422	12	AN3	P1_11, AA18	R423
13	OPEN			14	OPEN		
15	P2_0_IO0	P2_0, L21 (Set PX1_EN1 = 1)	---	16	P2_1_IO1	P2_1, K22 (Set PX1_EN1 = 1)	---
17	P2_2_IO2	P2_2, F21 (Set PX1_EN1 = 1)	---	18	P2_3_IO3	P2_3, G20 (Set PX1_EN1 = 1)	---
19	P2_4_IO4	P2_4, F19 (Set PX1_EN1 = 1)	---	20	P2_5_IO5	P2_5, E22 (Set PX1_EN1 = 1)	---
21	P2_6_IO6	P2_6, E20 (Set PX1_EN1 = 1)	---	22	P2_7_IO7	P2_7, C22 (Set PX1_EN1 = 1)	---
23	IRQ3	P1_9, AB18	R114	24	OPEN		
25	JA1_SDA3	P1_7, B16	**R141 R209**	26	JA1_SCL3	P1_6, A17	**R140 R208**

Table 7.1: Application Header JA1 Connections

Table 7.2 below lists the connections of the application header, JA2.

Application Header JA2, JA2-B							
Pin	Header Name	MCU Port, Pin	Link Required	Pin	Header Name	MCU Port, Pin	Link Required
1	RESET2_N	---	---	2	CON_EXTAL	AB16	R112
3	NMI	Y9	---	4	0V	---	---
5	IRQ0	P1_0, A19	R372	6	TXD0	P4_9, K21	R289
7	OPEN			8	RXD0	P4_10, J22	R293
9	IRQ1	P1_1, C17	R304	10	SCK0	P4_8, K20	R300
11	OPEN			12	OPEN		
13	OPEN			14	OPEN		
15	OPEN			16	OPEN		
17	OPEN			18	OPEN		
19	OPEN			20	TIOC3A	P7_8, K4	R159
21	TCLKB	P1_10, Y17	R188	22	TIOC3D	P3_7, Y4	R144
23	IRQ2	P1_8, AA17	R163	24	OPEN		
25	OPEN			26	OPEN		

Table 7.2: Application Header JA2 Connections

Table 7.3 below lists the connections of the application header, JA3. Note that address lines BA23-BA25 are manifested on Connector CN15, as detailed in Table 7.4.

Application Header JA3, JA3-B							
Pin	Header Name	MCU Port, Pin	Link Required	Pin	Header Name	MCU Port, Pin	Link Required
1	BA0	P9_2, C8	R378	2	BA1	P7_9, K1	---
3	BA2	P7-10, L3	---	4	BA3	P7_11, L2	---
5	BA4	P7_12, M1	---	6	BA5	P7_13, N1	---
7	BA6	P7_14, N2	---	8	BA7	P7_15, N3	---
9	BA8	P8_0, P1	---	10	BA9	P8_1, P2	---
11	BA10	P8_2, P3	---	12	BA11	P8_3, R1	---
13	BA12	P8_4, R2	---	14	BA13	P8_5, R3	---
15	BA14	P8_6, U2	---	16	BA15	P8_7, U4	---
17	BD0	P6_0, B3	---	18	BD1	P6_1, D6	---
19	BD2	P6_2, C4	---	20	BD3	P6_3, D5	---
21	BD4	P6_4, A2	---	22	BD5	P6_5, C1	---
23	BD6	P6_6, D2	---	24	BD7	P6_7, D1	---
25	BRD	P7_8, K4	R155	26	BWR	P7_5, J1	R146
27	BCS1	P3_7, Y4	R227	28	BCS3	P7_1, H2	R164
29	BD8	P6_8, E3	---	30	BD9	P6_9, E2	---
31	BD10	P6_10, E1	---	32	BD11	P6_11, F3	---
33	BD12	P6_12, G4	---	34	BD13	P6_13, F2	---
35	BD14	P6_14, F1	---	36	BD15	P6_15, G3	---
37	BA16	P8_8, V2	---	38	BA17	P8_9, V3	---
39	BA18	P8_10, W2	---	40	BA19	P8_11, W3	---
41	BA20	P8_12, Y1	---	42	BA21	P8_13, V4	---
43	BA22	P8_14, Y2	---	44	BCKIO	CKIO, V1	---
45	BWAIT	P1_13, Y18	---	46	BCKE	P7_4, J2	R115
47	BWE1_DQMLU	P7_7, K2	---	48	BWE0_DQMLL	P7_6, K3	---
49	BCAS	P7_3, J3	R173	50	BRAS	P7_2, H1	---

Table 7.3: Application Header JA3 Connections

Table 7.4 below lists the connections of the Misc. Connector CN15.

Misc. Connector CN15							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	MISO4	P2_11, E19 (Set PX1_EN1 = 1)	---	2	BA23	P8_15, AA1	---
3	MOSI4	P2_10, B22 (Set PX1_EN1 = 1)	---	4	BA24	P9_0, AB2	---
5	RSPCK4	P2_8, D20 (Set PX1_EN1 = 1)	---	6	BA25	P9_1, AA3	---
7	SSL40	P2_9, C21 (Set PX1_EN1 = 1)	---	8	P5B_10	P5_10, B7	R207

Table 7.4: Connector CN15 Connections

Table 7.5 below lists the connections of the application header, JA5.

Application Header JA5, JA5-B							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	AN4	P1_12, AB19	**R307**	2	OPEN		
3	AN6	P1_14, AA19	R278	4	OPEN		
5	CAN_CTX1	P5-10, B7	**R206**	6	CAN_CRX1	P5_9, A7	**R104**
7	CAN_CTX2	P7_3, J3	R174	8	CAN_CRX2	P7_2, H1	R18
9	IRQ4	P1_10, Y17	**R193**	10	IRQ5	P1_11, AA18	R189
11	OPEN			12	OPEN		
13	TIOC0A	P7_0, H4	R326	14	TIOC0B	P7_1, H2	R181
15	OPEN			16	OPEN		
17	OPEN			18	OPEN		
19	PWM2E	P4_4, M21 (Mux on IC30)	---	20	PWM2F	P4_5, M20 (Mux on IC30)	---
21	PWM2G	P4_6, L22 (Mux on IC30)	---	22	PWM2H	P4_7, L20 (Mux on IC30)	---
23	OPEN			24	OPEN		

Table 7.5: Application Header JA5 Connections

Table 7.6 below lists the connections of the application header, JA6.

Application Header JA6, JA6-B							
Pin	**Header Name**	**MCU Port, Pin**	**Link Required**	**Pin**	**Header Name**	**MCU Port, Pin**	**Link Required**
1	OPEN			2	OPEN		
3	OPEN			4	OPEN		
5	OPEN			6	OPEN		
7	OPEN			8	OPEN		
9	TXD1	P4_12, H22	R309	10	OPEN		
11	SCK1	P4_11, H19	R313	12	RXD1	P4_13, G21	R179
13	OPEN			14	OPEN		
15	OPEN			16	OPEN		
17	OPEN			18	OPEN		
19	OPEN			20	OPEN		
21	OPEN			22	OPEN		
23	OPEN			24	OPEN		

Table 7.6: Application Header JA6 Connections

8. Code Development

8.1 Overview

For all code debugging using Renesas software tools, the RSK+ board must be connected to a PC via a Segger JLink-Lite debugger, which is supplied with this RSK+ product.

8.2 Mode Support

The RZ/A1 microcontroller supports five boot modes which includes booting from memory connected to the CS0 space, serial flash memory, the NAND flash memory with an SD controller, and the NAND flash memory with an MMC controller.

8.3 Compiler Restrictions

The version of the compiler provided with this RSK is a fully functional GNU compiler, used in RSK+RZA1H sample projects.

Additionally, the ‘DS-5 Starter Kit for Renesas RZ’ edition provides the ARM compiler with a 32KB limit for instructions and unlimited for data. This can be found on the ARM website at the following link and requires activation:

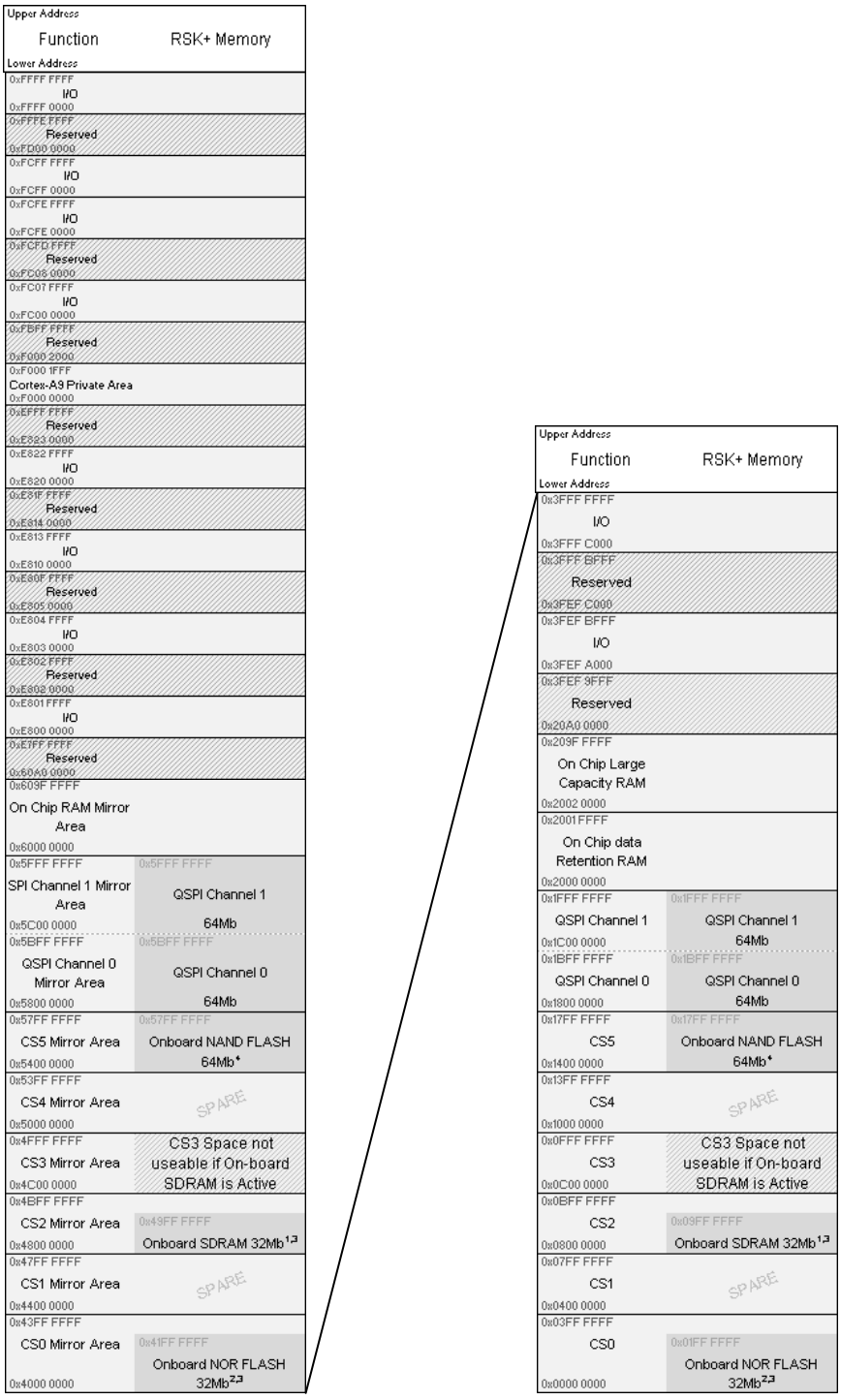
http://ds.arm.com/renesas/rza-starter-kit/

8.4 Debugger Support

The RSK+ board is supplied with a Segger JLink-Lite Debugger. Please refer to the Segger website for further information www.segger.com.

8.5 Address Space

Figure 8.1 below details the address space of the MCU. This diagram is based on the Hardware Manual version 0.6. For further details, refer to the RZ/A1H Group Hardware Manual.



1. **To enable SDRAM, JP18 must be open and SW6 #3 must be in the ON position (CS0_MBOOT2 low)**
2. **To enable NOR FLASH, JP18 must be shorted and SW6 #3 must be in the ON position (CS0_MBBOOT2 low)**
3. **To enable QSPI, JP18 must be shorted and SW6's switches (SW6.1 – SW6.6) need to be set to: OFF, ON, OFF, ON, ON, ON.**
4. **Note that SDRAM and NOR FLASH cannot be enabled at the same time.**
5. **Device is 256MByte, but only 64MByte is addressable.**

Figure 8.1: RZ/A1H Address Map On RSK+ Board

8.6 Boot Modes

A boot-loader is the first program executed in the microcontroller following a system reset. It is used to configure the device to a known state; load a new boot program and, if necessary, copy the main program to the allocated program memory (RAM) of the microcontroller.

The RZ/A1 supports five boot modes (see section 6.5):

Boot mode 0: Boots the LSI from the memory (bus width: 16 bits) connected to the CS0 space
Boot mode 1: Boots the LSI from the memory (bus width: 32 bits) connected to the CS0 space
Boot mode 3: Boots the LSI from the serial flash memory connected to the SPI multi I/O bus space
Boot mode 4: Boots the LSI from the NAND flash memory with the SD controller enabled
Boot mode 5: Boots the LSI from the NAND flash memory with the MMC controller enabled

The requirements for booting from QSPI on the RSK+RZA1H are as follows:

SW6					
SW6.1	SW6.2	SW6.3	SW6.4	SW6.5	SW6.6
OFF	ON	OFF	ON	ON	ON

Table 8.1: SW6 configuration.

Channel	QSPI Signal Name	RSK+RZA1H Signal Name	Function	Comment
0	SPBSSL	P9_3_SPBSSL_0	Slave Select	Common to both QSPI devices. (IC25 and IC26)
	SPBCLK	SPBCLK_0	Clock	Common to both QSPI devices. (IC25 and IC26)
	SPBIO00	P9_4_SPBIO00_0	Data	IC26 Pin Enabled
	SPBIO10	P9_5_SPBIO10_0	Data	Not configured
	SPBIO20	P9_6_SPBIO20_0	Data	Not configured
	SPBIO30	P9_7_SPBIO30_0	Data	Not configured
	SPBIO01	P2_12_SPBIO01_0	Data	Not configured
	SPBIO11	P2_13_SPBIO11_0	Data	Not configured
	SPBIO21	P2_14_SPBIO21_0	Data	Not configured
	SPBIO31	P2_15_SPBIO31_0	Data	Not configured
1	SPBSSL	N/A	Slave Select	These signals are have been used for other functions.
	SPBCLK	N/A	Clock	
	SPBIO0x	N/A	Data	
	SPBIO1x	N/A	Data	
	SPBIO2x	N/A	Data	
	SPBIO3x	N/A	Data	

Table 8.2: QSPI communication pins at boot.

The RZ/A1 has two QSPI channels (0 and 1), and allows for one or two serial flash memories to be directly connected per channel. The number of connected memories is specified by writing to the BSZ bits of register CMNCR of the QSPI bus controller. Booting from QSPI is only possible on channel 0, using Single Channel Single Bit SPI mode. On the RSK+RZA1H, the two QSPI flash devices are connected to channel 0.

Figure 8.2 is a graphical representation of the boot sequence between the RZ/A1 and the QSPI.

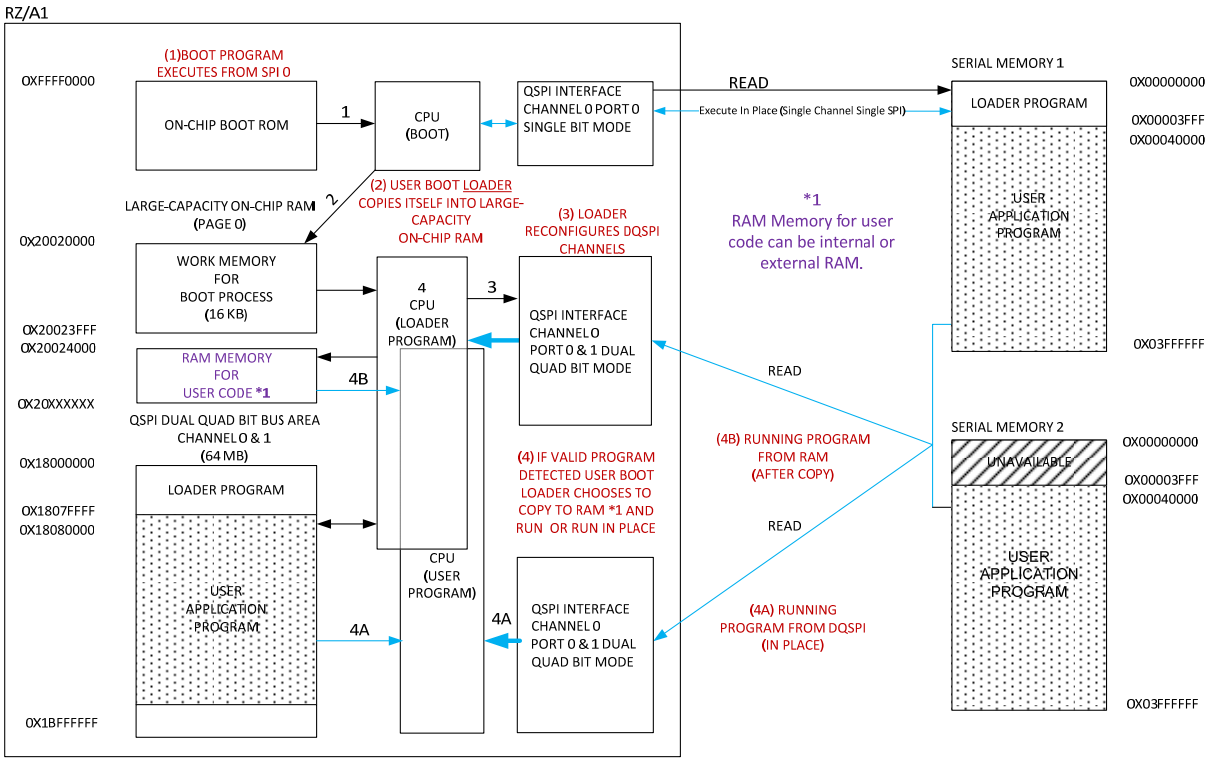


Figure 8.2: Boot process of user code stored in QSPI devices.

QSPI Boot Process:

(1) Initiation of the QSPI Interface Channel 0 in Single Bit mode.

Following a reset, the RZ/A1 executes the Boot Program located in the high exception vector address 0xFFFF0000; which then configures the QSPI bus Channel 0 Port 0 only in Single Bit mode and external address space read mode, ready to read directly from the connected serial flash memory.

Execution of user code in this configuration is possible, but will be slower than necessary. Therefore a small User Boot Loader is provided

(2) Transfer of the Loader Program.

The User Boot Loader Program copies itself to internal RAM and executes here. The Loader program can then disable the QSPI channel, reconfigure it to the Dual port Quad Bit SPI mode for maximum speed and look for a User Application Program.

Note: The external address space for channel 0 is mapped internally to the address range 0x18000000 to 0x1BFFFFFF, giving a total of four gigabytes of address space, when one memory device is connected. With two devices connected, as in the case of the RSK+RZA1H, the internal address space is doubled to eight gigabytes. The RZ/A1H Boot Program uses 16KB of work RAM memory (0x20020000 to 0x20023FFF).

(3) Transfer of a User Application Program (as Desired).

After configuring the external address space, the User boot Loader Program inspects the User Application Program to validate its configuration. Four items inspected in the user application program are the start and end addresses of the user application program, the execution address and a boot load string. These can be found in the start.S file of the user's DS-5 project. A snippet of the contents of start.S file is shown below:

```
        .global start
        .func   start
    start:
        LDR pc, =reset_handler
        LDR pc, =undefined_handler
        LDR pc, =svc_handler
        LDR pc, =prefetch_handler
        LDR pc, =abort_handler
        LDR pc, =reserved_handler
        LDR pc, =irq_handler
        LDR pc, =fiq_handler
    code_start:
        .word    start
    code_end:
        .word    end
    code_execute:
        .word    execute
        .string ".BootLoad_ValidProgramTest."
```

The 'start' is a function/label for loading the user application code's vector table. The 'code_start' and 'code_end' labels contain variable specifying the start and end address of the entire user application code, including the vector addresses.

The 'code_execute' label contains the 'execute' variable used to indicate the execution start address.

The '.string' variable is a signature marker used by the Load Program to validate the user application code, whether to load the code or not.

If the location constants and .string variable in the start.S file is not found immediately after the vector table as shown above, the configuration is deemed invalid and LED0 will be used to flash in the sequence of one long (2 second) followed by one short (0.5 second) pulse so that the error can be recognised. If valid, the User Boot Loader Program checks the start address. If this matches the current location, the execute address is used and the program is launched and executes from QSPI.

Otherwise the start and end addresses are used to copy the program to the required destination using the DMA controller. On completion the program is launched at the provided execute address.

8.7 QSPI Data Reading

Reading of QSPI data can be configured for single or dual device read, depending on the number of serial memories connected to a channel. Differences between the two modes are clearly explained in the next two diagrams. From the diagrams it is clear to see the advantages of dual read mode over single read. With two devices connected, using dual mode doubles the storage space and reduces the number cycles taken to read the same amount of data in single mode.

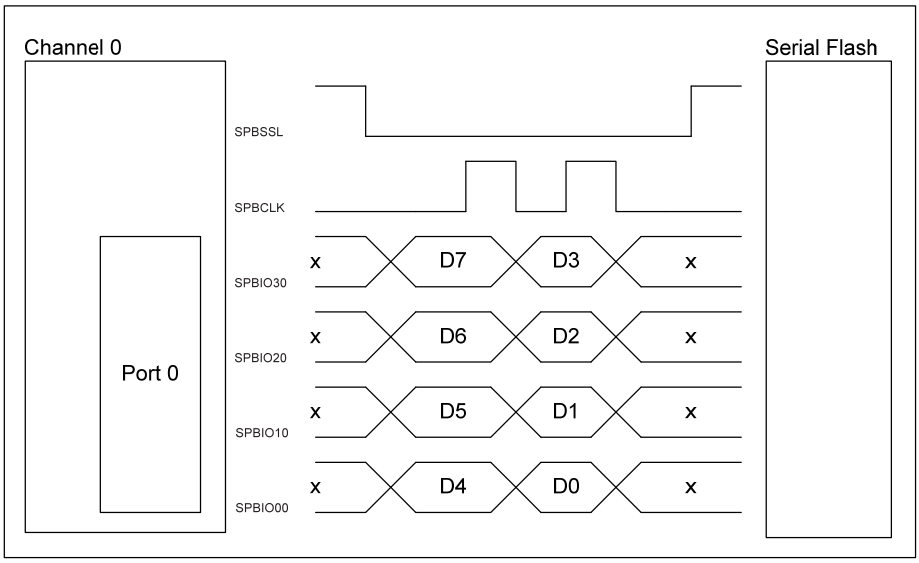


Figure 8.3: Example of a 4-bit data size using one serial flash memory.

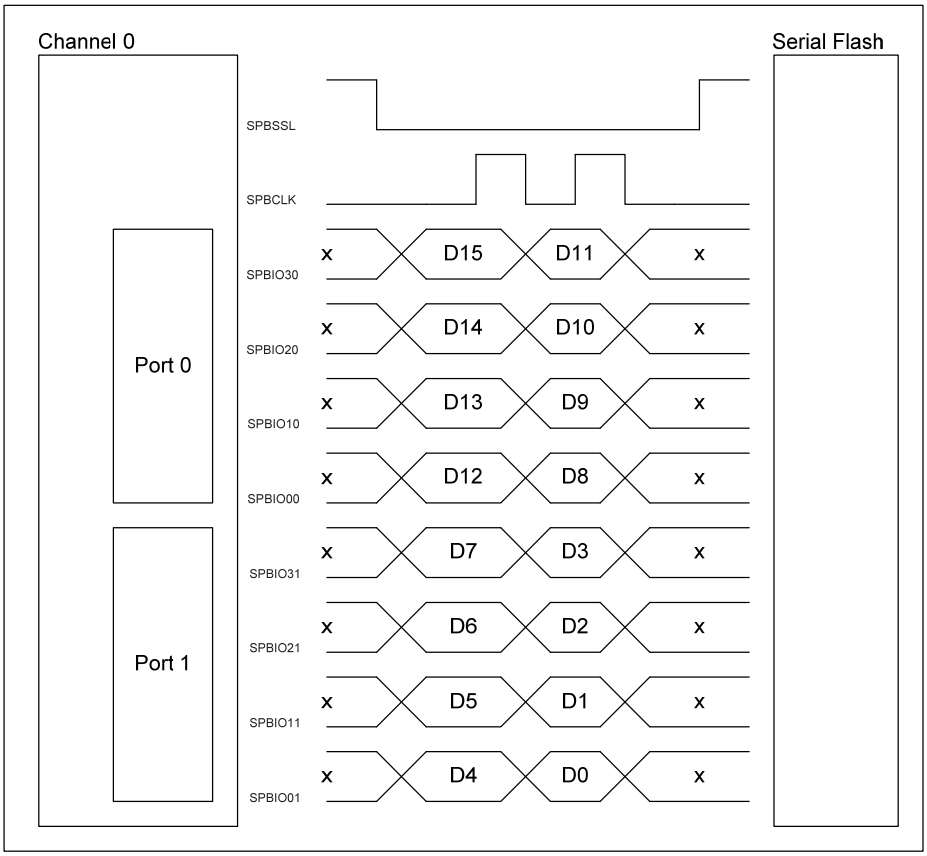
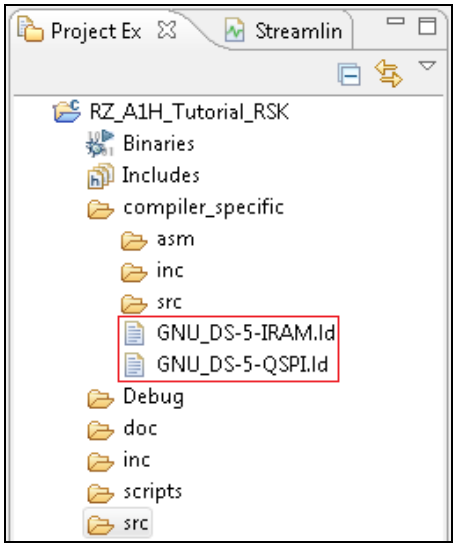


Figure 8.4: Example of a 4-bit data size using two serial flash memories.

8.8 Load Files

The Tutorial sample project provides two load files (.ld) used to specify where the user code is to be located and executed. Execution is either directly from RAM when debugging in RAM, in this case the RAM is initialised by the debugger. Alternatively the program is loaded into QSPI and then is copied at start-up by the User Boot Loader and runs from RAM. The load files can be found in the project folder under the project Explorer view.



The RAM load file contains the following two lines:

```
EXEC_BASE              = 0x20040000;
MIRRORED_VECTOR_TABLE = 0x60040000;
```

The EXEC_BASE variable specifies where in memory the user application code resides and executed from.

The QSPI load file uses the following variables:

```
EXEC_BASE              = 0x18080000;
MIRRORED_VECTOR_TABLE = 0x60040000;
LOAD_BASE              = 0x20040000;
```

As for the QSPI loadfile, the user application resides in the EXEC_BASE address. It is mapped by the Load Program to the LOAD_BASE address (RAM), to be executed from there. An example of a mapping instruction to copy the user application code stored in the serial flash device to the RAM, is shown below.

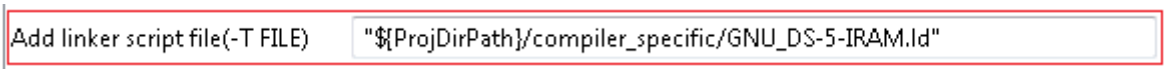
```
.reset EXEC_BASE  : AT ( LOAD_BASE )
```

The NOR load file does not include a load base address. It has an execution address set to 0x00000000.

```
EXEC_BASE              = 0x00000000;
```

To change between the load files, click on the project folder (RZ_A1H_spibsc_boot_init_RSK) in the Project Explorer view.

Select File > Properties > C/C++ Build > Settings > GCC Linker > General.



The RAM load file is configured by default in all samples other than the RZ_A1H_Tutorial_RSK. Change GNU_DS5-5IRAM.ld to GNU_DS-5-QSPI.ld to use the QSPI load file.

8.9 Dual QSPI Debugger (Programming) Settings

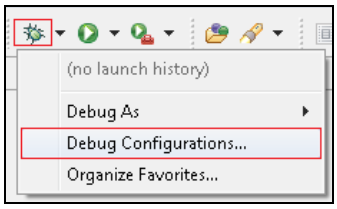
Additional steps are required for connecting to the RSK+RZA1H with a DS-5 project configured to run from QSPI. The following steps assume the user has gone through the RSK+RZA1H's Quick Start Guide.

These steps also assume that the User Boot Loader is still resident on your board. If you have re-programmed the Channel 0 Port 0 QSPI flash device, this loader may not be resident. In this case we provide the source project for the User Boot Loader in the sample set, and a simple batch file to re-flash the User Boot Loader. Please refer to the description.txt file in this project for details.

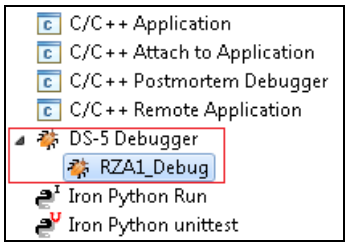
Append the following string to the debugger's serial number in the debug configurations settings of the DS-5 user application sample project "`:device R7S721001_DualSPI`", without the quote marks.

Note: This must not be used when using the User Boot Loader Program sample project in DS-5.

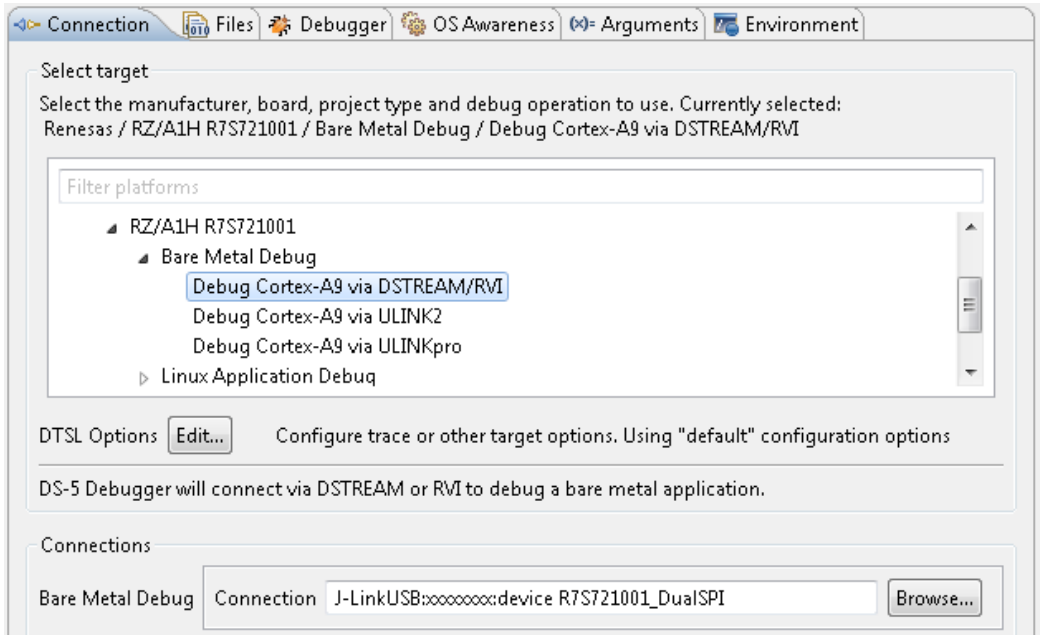
To open the debug configurations settings in DS-5, click on the small triangle to the right of the Debug icon and select Debug Configurations… from the menu bar as shown below.



Expand the DS-5 Debugger entry to reveal the debug configuration as shown in the following example.



Click on the desired configuration; e.g. RZA1_Debug, to open the Files tabs. Under the Connection tab, append the string to the detected J-Link debugger's serial number (highlighted in the example below).



Please refer to the RSK+RZA1H's Quick Start Guide for detailed instructions on how to create and setup the debug configurations.

With this configuration, on connecting to the target board with the User Application, the application will be automatically programmed into the flash.

8.10 NOR Flash Boot Loader

The RZ/A1 device is designed to boot from the memory device connected to address space CS0. Booting from this address space has two modes, Mode 1 and Mode 2. Boot Mode 1 uses 16-bit bus addressing and Boot Mode 2 uses 32-bit bus addressing. The NOR flash memory on the RSK+ZA1H has a 16-bit bus. To configure the RZ/A1 to boot from this memory, set the all switches on SW6 to the ON position. In this mode, following cancelation of the power-on reset, the RZ/A1begins program execution from address 0x00000000.

The NOR flash is connected to CS0 address space. The RZ_A1H_NOR_INIT_Sample project is a boot loader. Two methods for programming the NOR flash memory device on the RSK+RZA1H are provided in the software package that is copied to the user PC after running the installer. The methods are:

- Sample code
  - Allows the user to program and debug the Boot Loader using the DS-5.
  - User application code to be programmed into the NOR flash is also provided.
  - Requires modification to the script file to enable write access to the NOR flash region.

- Batch Files
  - Allows programming the user application code into the NOR flash.
  - This is independent of the IDE.

The user application code provided (RZ_A1H_Display_Board_RSK) is built in RAM and loaded into the NOR flash using the Boot Loader.

The NOR Boot Loader, similar to the QSPI Boot Loader, checks for the signature string

```
".BootLoad_ValidProgramTest."
```

This signals the Loader to load the user application code into the NOR flash device.

Please ensure to modify the J-Link connection string to allow read and write access to the NOR flash.

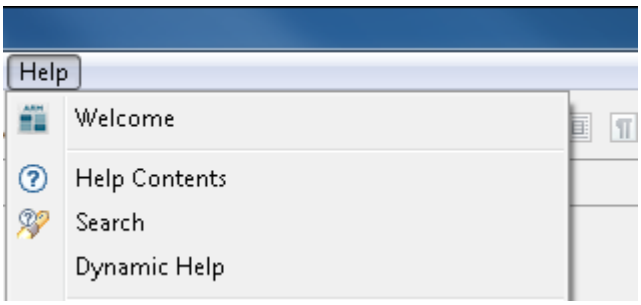
- In DS-5, select the project under the Project Tree view.
- Open the Debug Configurations
- Append the string shown below, taking care to add the space between the J-Link serial and the colon.

J-LinkUSB:xxxxxxxx**:SetCFIFlash 0x00000000-0x03FFFFFF:SetWorkRAM 0x20020000-0x20021FFF**

Please refer to the RZ/A1H device group's hardware manual for more information on boot modes.

9. Additional Information

Technical Support
For details on how to use DS-5, refer to the help file by opening DS-5, then selecting Help > Help Contents from the menu bar.



For information about the RZ/A1H series microcontrollers refer to the RZ/A1H Group Hardware Manual.

For information about the RZ assembly language, refer to the RZ Series Software Manual.

Technical Contact Details

Please refer to the contact details listed in section 10 of the "Quick Start Guide"

General information on Renesas Microcontrollers can be found on the Renesas website at:
http://www.renesas.com/

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