

ISL78205EVAL1Z Evaluation Board Setup Procedure

The ISL78205EVAL1Z board demonstrates the synchronous/asynchronous buck operation of the ISL78205. The board input voltage range is 3V to 40V.

The output voltage is set to 5V and can be changed by altering the feedback resistors R3 and R4. Note that to increase the output voltage, the output capacitors' voltage rating needs to be checked.

The board's output current is 2A typical. The board is set with default 3.6A OC threshold. The OC threshold can be programmed by R15 placed at the ILIMIT pin.

The ISL78205EVAL1Z board is configured as a synchronous buck and can be configured to an asynchronous buck. The board is set to a default switch frequency of 500kHz. The frequency can be programmed by R8 at the FS pin.

The board can be synchronized with an external clock. Multiple ISL78205EVAL1Z boards can be synchronized simply by connecting their SYNC pins together.

Recommended Equipment

- 0V to 40V power supply with 3A source current
- Load capable of sinking 3A current
- Multimeters
- Oscilloscope

Quick Start-up

Figure 1 shows the board image. Note N/A section shows unused circuits. The useful buck section is noted inside the block.

1. Connect the power source to inputs J1 (VIN+) and J2 (GND). Connect the load terminals to buck outputs J3 (VOUT+) and J4 (GND). Make sure the setup is correct prior to applying any power or load to the board.
2. Adjust the power source to 12V and turn it on.
3. Verify the output voltage is 5V and use oscilloscope to monitor the phase node waveforms through J28.

Asynchronous Buck Configuration

To configure the board to asynchronous buck, remove R19 and change R20 (on bottom of the board) to 0Ω to ensure Q6 is securely off.

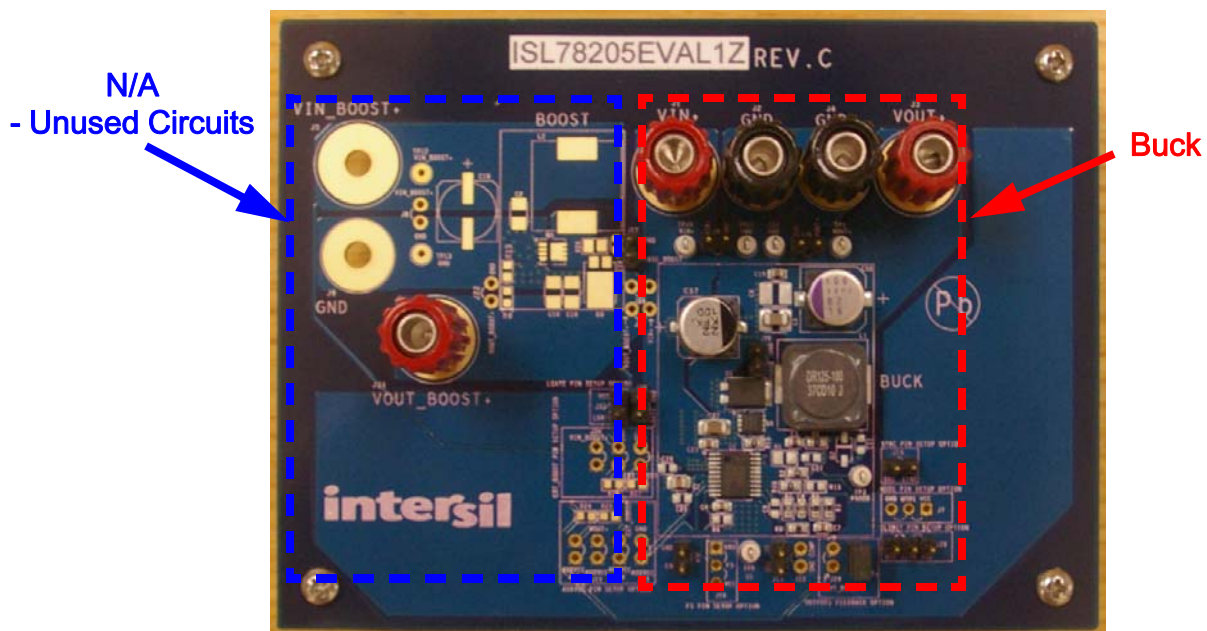


FIGURE 1. ISL78205EVAL1Z BOARD IMAGE

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TABLE 1. CONNECTORS/TEST POINTS DESCRIPTIONS

J1	VIN+, positive terminal of buck inputs.
J2	GND, ground terminal of buck inputs.
J3	VOUT+, positive terminal of buck outputs.
J4	GND, ground terminal of buck outputs.
J5	N/A. Left open.
J6	N/A. Left open.
J7	N/A. Left open.
J8	N/A. Left open.
J9	Test points to monitor buck input. Monitoring purpose only and don't short it with jumper.
J10	N/A. Left open.
J11	N/A. Left open.
J12	N/A. Left open.
J13	N/A. Left open.
J14	Use this connector to control IC ON/OFF.
J15	Test points to monitor the FB pin. Monitoring purpose only and don't short it with jumper.
J16	Use it to set up switching frequency. With FS pin connected to VCC or GND, or left open, the IC has default 500kHz frequency. R8 is a placeholder for a resistor to program frequency.
J17	N/A. Left open.
J18	Use it to configure synchronization. Option 1: to apply external clock for the IC to be synchronized with. Option 2: to synchronize multiple ISL78205, simply connect those SYNC pins together.
J22	N/A. Left open.
J23	Test points to monitor the COMP pin. Monitoring purpose only and don't short it with jumper.
J24	N/A. Left open.
J25	Must short it with jumper to provide output feedback connection.
J26, J27	N/A. Left open.
J28	Test points to monitor the buck PHASE node waveforms. For monitoring purposes only. Do Not short with jumper.
J29	Use it to set up the overcurrent limit threshold. With ILIMIT pin connected to VCC or GND or left open, the IC has default of 3.6A OC threshold. R15 is a placeholder for a resistor to program the OC threshold.
J30, J34	N/A. Left open.
J31	N/A. Left open.
J32	Test points to monitor the LGATE. For monitoring purposes only. Do Not short with jumper.
J33	For asynchronous buck configuration, short with jumper before IC startup will disable the low-side driver after IC startup.
J35	N/A. Left open.
J36	Test points to monitor the buck output voltage. For monitoring purposes only. Do Not short with jumper.

ISL78205EVAL1Z Schematic

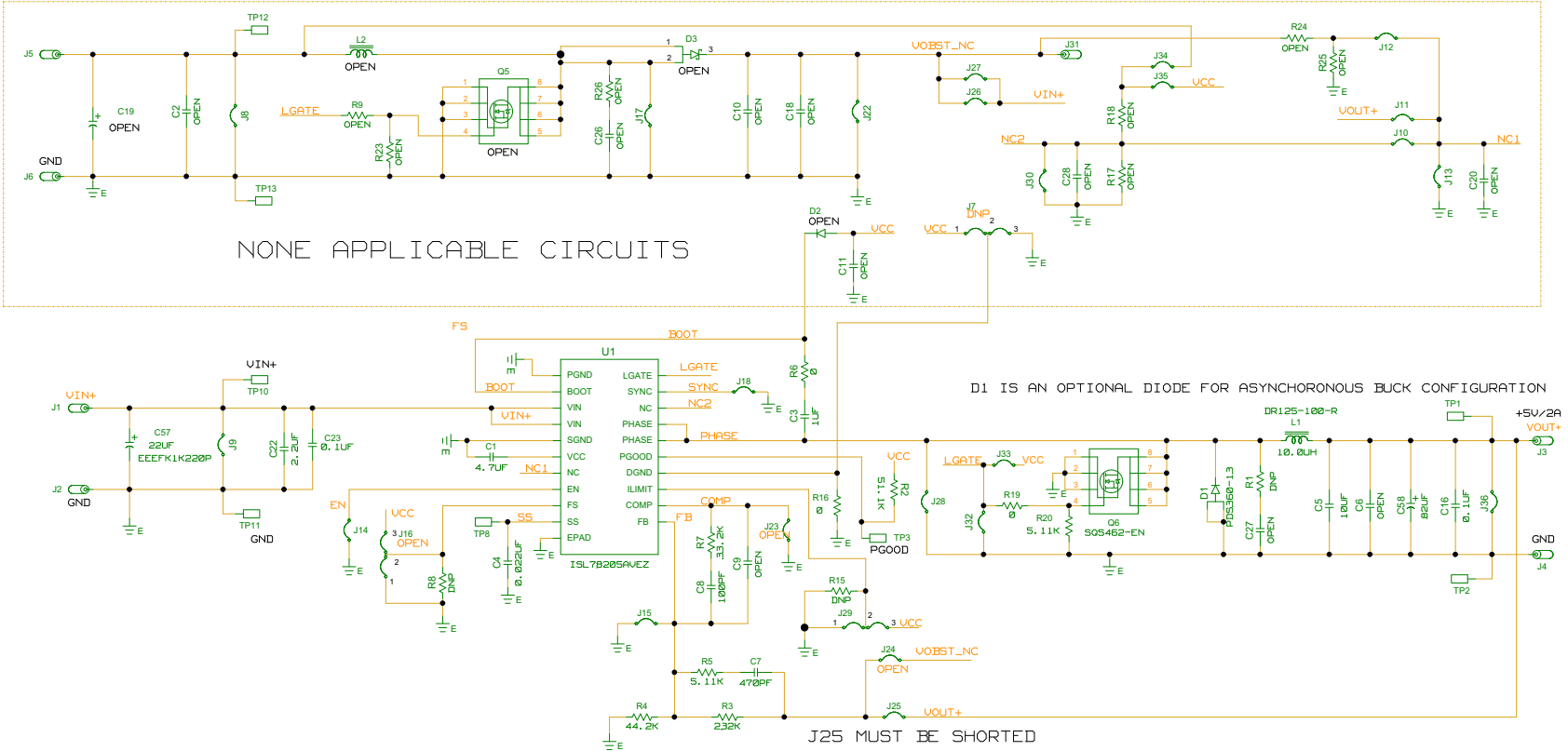


FIGURE 2. ISL78205EVAL1Z BOARD SCHEMATIC

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TABLE 1. BILL OF MATERIALS

REF DES	PART NUMBER	QTY	DESCRIPTION	MANUFACTURER
C3	C1608X7R1C105K	1	CAP, SMD, 0603, 1.0µF, 16V, 10%, X7R, ROHS	TDK
C57	EEE-FK1K220P	1	CAP, SMD, 8X10.2, 22µF, 80V, 20%, ALUM.ELEC., ROHS	PANASONIC
C1	GRM21BR71A475KA 73L	1	CAP, SMD, 0805, 4.7µF, 10V, 10%, X7R, ROHS	MURATA
C18, C22	GRM31CR71H225KA 88L	2	CAP, SMD, 1206, 2.2µF, 50V, 10%, X7R, ROHS	MURATA
C8	VARIOUS	1	CAP, SMD, 0603, 100pF, 50V, 5%, COG, ROHS	VARIOUS
C16, C23	VARIOUS	2	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	VARIOUS
C4	VARIOUS	1	CAP, SMD, 0603, 0.022µF, 16V, 10%, X7R, ROHS	VARIOUS
C7	C0603X7R500- 471KNE	1	CAP, SMD, 0603, 470pF, 50V, 10%, X7R, ROHS	VENKEL
C2, C9, C11, C18, C19, C20, C26, C27, C28	N/A	0	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	N/A
C5	VARIOUS	1	CAP, SMD, 1206, 10µF, 16V, 10%, X5R, ROHS	VENKEL
C10	N/A	0	CAP, SMD, 1206, DNP-PLACE HOLDER, ROHS	N/A
C6	N/A	0	CAP, SMD, 1210, DNP-PLACE HOLDER, ROHS	N/A
C58	16SVPD82M	1	CAP-OSCON, SMD, 6.9x8.3, 82µF, 16V, 20%, 40mΩ, ROHS	SANYO
L1	DR125-100-R	1	COIL-PWR INDUCTOR, SMD, 12.5mm, 10µH, 20%, 5.35A, ROHS	COOPER/COILTRONICS
D1	PDS360	1	DIODE-SCHOTTKY RECTIFIER, SMD, SMPC, 50V, 3A, ROHS	DIODES
U1	ISL78205AVEZ	1	IC-2.5A BUCK CONTROLLER, 20P, HTSSOP, ROHS	INTERSIL
Q6	SQS462EN-T1-GE3	1	TRANSISTOR-MOS, N-CHANNEL, 8P, PWRPAK, 60V, 8A, ROHS	VISHAY
R6, R16, R19	VARIOUS	3	RES, SMD, 0603, 0Ω, 1/10W, ROHS	VARIOUS
R3	VARIOUS	1	RES, SMD, 0603, 232k, 1/10W, 1%, ROHS	VARIOUS
R7	VARIOUS	1	RES, SMD, 0603, 33.2k, 1/10W, 1%, ROHS	VARIOUS
R4	VARIOUS	1	RES, SMD, 0603, 44.2k, 1/10W, 1%, ROHS	VARIOUS
R5, R20	VARIOUS	2	RES, SMD, 0603, 5.11k, 1/10W, 1%, ROHS	VARIOUS
R2	VARIOUS	1	RES, SMD, 0603, 51.1k, 1/10W, 1%, ROHS	VARIOUS
R8, R9, R15, R17, R18, R23, R24, R25	N/A	0	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS	N/A
R1, R26	N/A	0	RES, SMD, 0805, DNP-PLACE HOLDER, ROHS	N/A
D2, D3	N/A	0	DO NOT POPULATE OR PURCHASE	N/A
L2	N/A	0	DO NOT POPULATE OR PURCHASE	N/A
Q5	N/A	0	DO NOT POPULATE OR PURCHASE	N/A
C3	C1608X7R1C105K	1	CAP, SMD, 0603, 1.0µF, 16V, 10%, X7R, ROHS	TDK
C57	EEE-FK1K220P	1	CAP, SMD, 8X10.2, 22µF, 80V, 20%, ALUM.ELEC., ROHS	PANASONIC
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C18, C22	GRM31CR71H225KA 88L	2	CAP, SMD, 1206, 2.2µF, 50V, 10%, X7R, ROHS	MURATA

ISL78205EVAL1Z Board Layout

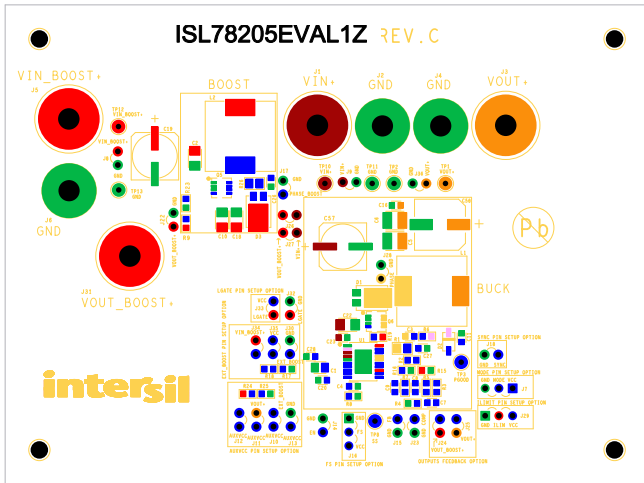


FIGURE 1. TOP COMPONENTS SILKSCREEN

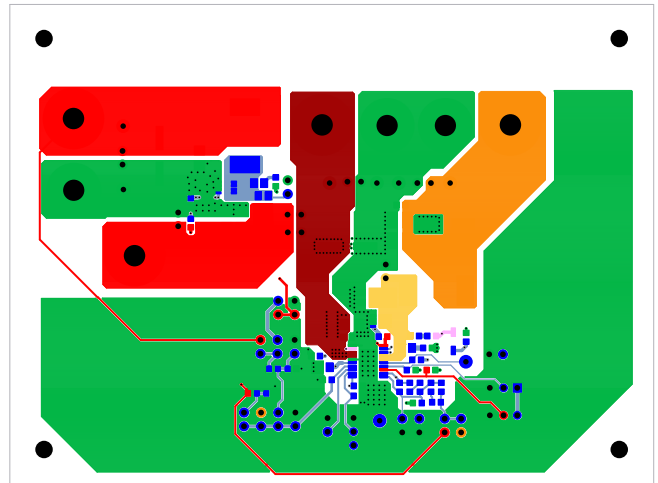


FIGURE 2. TOP LAYER

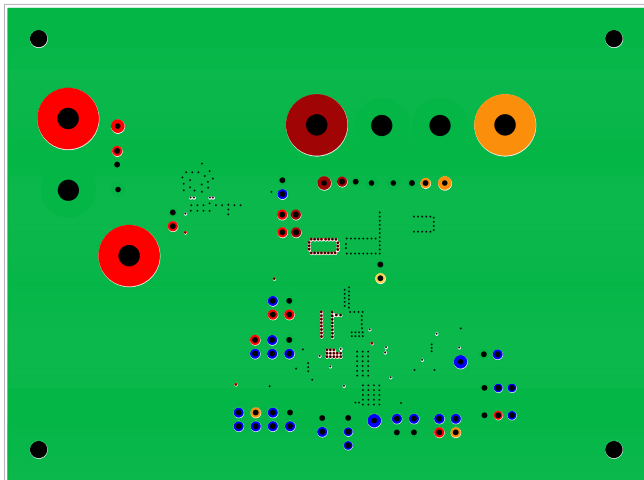


FIGURE 3. 2nd LAYER

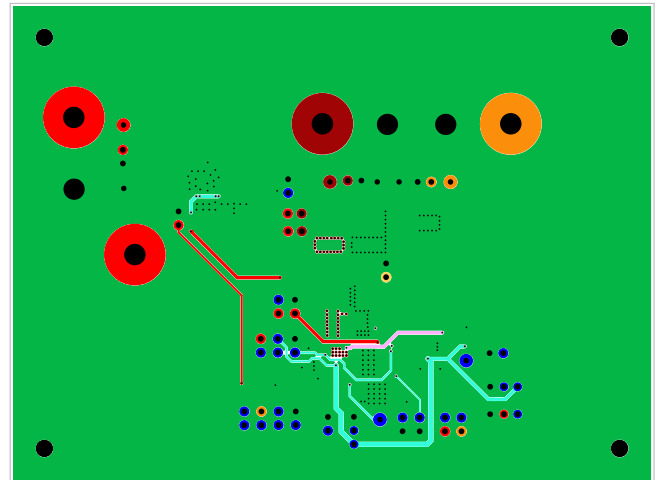


FIGURE 4. 3rd LAYER

ISL78205EVAL1Z Board Layout (Continued)

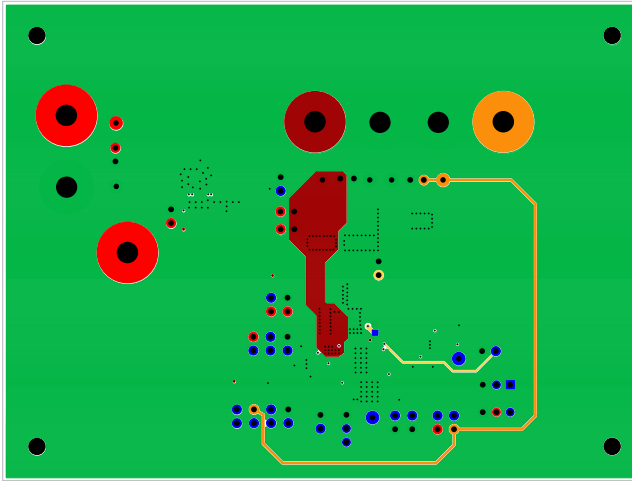


FIGURE 5. BOTTOM LAYER

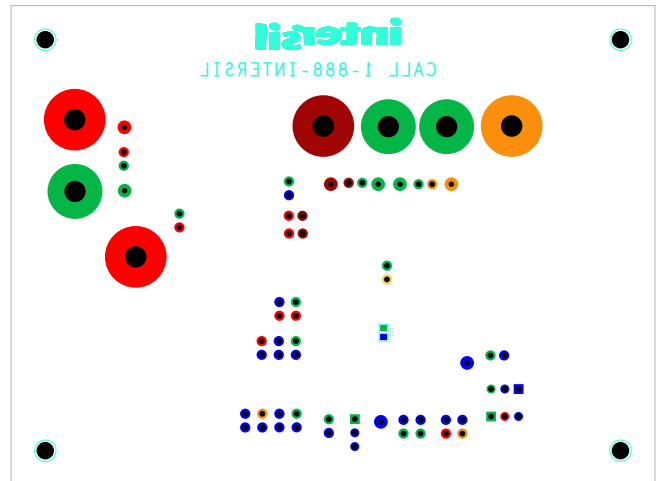


FIGURE 6. BOTTOM COMPONENTS SILKSCREEN

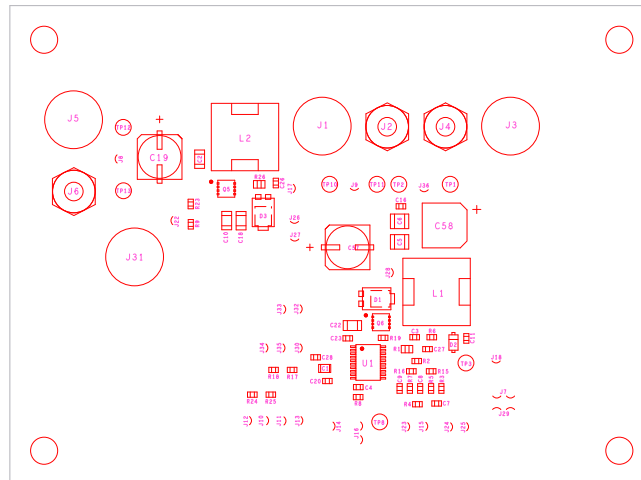


FIGURE 7. TOP COMPONENT ASSEMBLY

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