User's Manual

ISL70321SEHDEMO1Z

User's Manual: Demonstration Board

High Reliability

Rev 0.00 Jul 2017

ISL70321SEHDEMO1Z

Demonstration Board

UG124
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1. Overview

The ISL70321SEHDEMO1Z is a Small Form Factor (SFF) board suitable for integrating onto an existing circuit board or onto a prototype system circuit. The demonstration board provides up to four sequencing events for Point-of-Load (POL) regulators powering multi-rail loads.

The ISL70321SEHDEMO1Z provides access to the IC pins for integration along with a minimum of external passives to provide decoupling, a 2:1 resistive divider on the four VM inputs, pull-ups, and the timers set to 2ms and 4ms for the delay and power-good durations, respectively.

1.1 Key Features

- Small, compact design
- Easy to integrate into an existing circuit
- Highly customizable

1.2 Specifications

This board provides for the following operating conditions:

- Nominal V_{IN} = 3.3V to 12V
- Sequence up and down in reverse order
- 1.5% accuracy voltage monitoring
- Adjustable voltage monitoring thresholds
- Adjustable delay between sequenced events
- Adjustable power-good delay

1.3 Ordering Information

Part Number	Description
ISL70321SEHDEMO1Z	ISL70321SEH Mini Demonstration Board

1.4 Related Literature

- For a full list of related documents please visit our website
  - ISL70321SEH product page

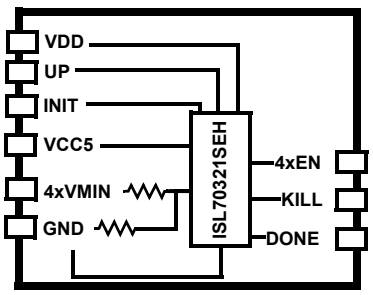

Figure 1. Block Diagram

2. Board Functional Description

The ISL70321SEHDEMO1Z demonstration board provides a simple platform with which to drop in an integrated circuit solution to sequence up to four events into an existing or a prototype multi power supply system circuit.

After it is connected into the circuit and properly addressed using the UP and INIT inputs, the ISL70321DEMO1Z starts sequencing the ENABLE outputs from low to high, EN1 through EN4 order. The DONE output is released to pull high after sequencing is completed.

After the UP input is pulled low, the ISL70321SEHDEMO1Z starts sequencing the ENABLE outputs from high to low, EN4 through EN1 order. The DONE output is pulled low when the down sequencing is completed.

The ISL70321SEHDEMO1Z is shown in Figures 8 through 10 in photographic and schematic forms.

2.1 Operating Range

The ISL70321SEHDEMO1Z is configured for the operating conditions of V_{DD} from 3V to 13.2V, with the ENx outputs resistively connected to the VCC5 5V pull-up supply. The VMx, UP, and INIT inputs are limited to a maximum of 5V.

2.2 Default Configuration Settings

All functional and performance configuration settings for this demonstration board will be set by the circuit design requirements. However, a default set of conditions for the VM input threshold and the delay timing have been configured for building familiarity with its functions before system integration.

The default configuration is set as follows:

- The VMx inputs all have 2:1 resistor dividers from the VMx_IN connection points to the VM1 to VM4 inputs. This sets the nominal VM rising input voltage threshold to be ~1.2V.
- The ENx, DONE, and $\overline{KILL}$ outputs all have 10kΩ pull-up resistors to VCC5.
- The Power-Good Timer (PGTMR) and the Time Delay (TDLY) pins both have 10kΩ resistors to ground providing a nominal 4ms for the monitored voltage to be ‘GOOD’ and a nominal 2ms for the delay between sequenced enable outputs.

2.3 Quick Start Guide

With the default or user intended configuration components in place, ensure that the board is properly connected to the appropriate supplies and loads before applying any power.

(1) Change the delay and power-good timer resistors on the board as necessary to achieve the desired timing of sequenced events using the provided resistor positions.
(2) Connect the appropriate bias supply to VDD and GND.
(3) Connect the enabling input of the POLs to be sequenced to the appropriate ISL70321SEH ENx outputs in order of desired turn-on sequence
(4) Connect the POL outputs to the appropriate ISL70321SEH VMx inputs.
(5) Connect UP to the appropriate signaling input.
(6) Use oscilloscopes and DVMs to monitor signals and voltages.
(7) Turn system input power supply ON.
(8) Signal the UP input.
(9) Observe sequencing function and adjust timing and threshold voltages as desired.

3. Application Considerations

3.1 Connecting Unused Rails

The simplified schematic in Figure 2 highlights the necessary connections for unused EN_X and VM_{Xun} pins. The unused VM_X and EN_X must be shorted together in pairs and each pair pulled up to VCC5 with an external resistor. An unused ENx/VMx pair can be used to establish a delayed active high output for down stream signaling. Figures 4 and 5 illustrate three POLs being turned on and off respectively.

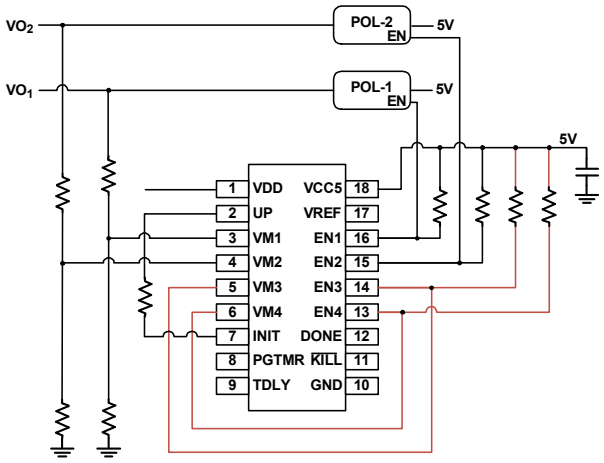

Figure 2. Connecting Unused Rails

3.2 Automatic Fault Clearing Reset and Restart Configuration

There is an auto restart configuration in case the ISL70321SEH is set up to be self starting upon bias without signaling. When the ISL70321SEH restarts, it will sequence up all of its ENABLE outputs without intervention. The EN output delays can be programmed to allow for the down stream sequenced circuits to be ready before being enabled. Faults resulting in an immediate $\overline{KILL}$ will then make the ISL70321SEH cycle through an infinite number of attempts at restarting and $\overline{KILL}$ shut down until the fault is cleared. Figure 3 shows the auto restart connection. When $\overline{KILL}$ is invoked, it is used to automatically clear and reset the sequencer. This results in the ISL70321SEH attempting to restart the entire sequence up progression. Figure 6 shows the details of a low VM input (to invoke a $\overline{KILL}$), the $\overline{KILL}$ output pulling low with both the UP and INIT pins low as well. Figure 7 shows the resulting restart with EN1, EN, DONE, and $\overline{KILL}$ signals.

This configuration can be used if required criteria must be met before turn-on by continuously checking for those requirements while attempting turn-on.

In this configuration, the sequence down can be invoked through a pull down on UP/INIT with isolation to $\overline{KILL}$ input. Using $\overline{KILL}$ as an input will produce a simultaneous shutdown of the EN outputs.

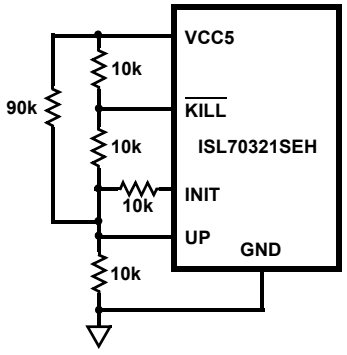

Figure 3. Auto Fault Clear and Reset Configuration

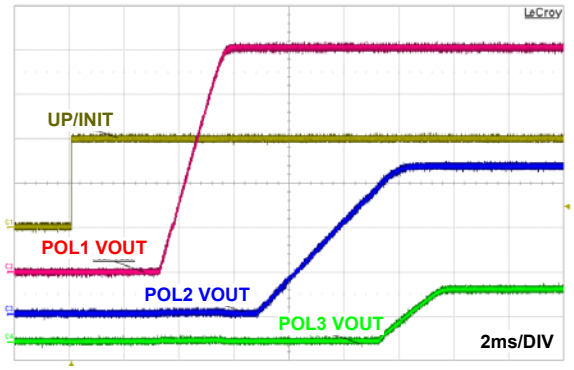

Figure 4. Sequencing On 3 POLs, RTDLY = 2ms

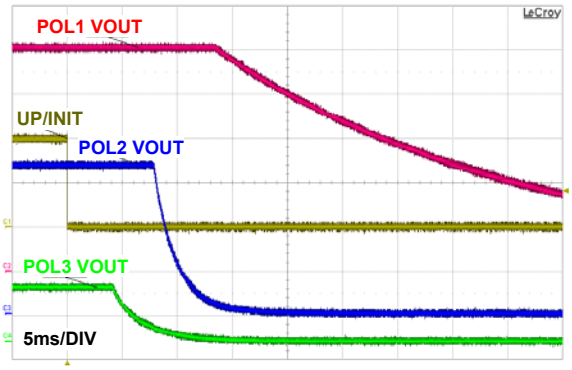

Figure 5. Sequencing Off 3 POLs, RTDLY = 2ms

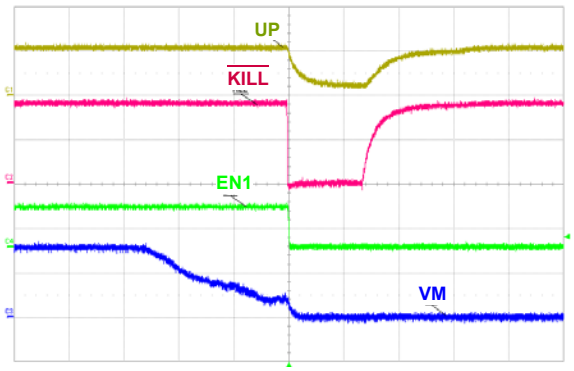

Figure 6. VM Low to KILL, UP, and EN1

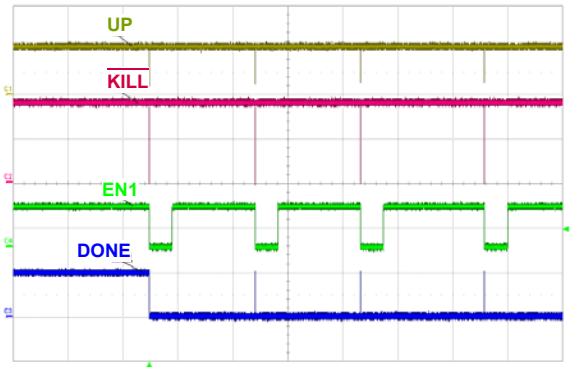

Figure 7. Auto Fault Clear and Reset Waveform

4. PCB Layout Guidelines

The ISL70321SEHDEMO1Z PCB layout has been optimized for size and ease of use.

The following key features are:

• The small 2” x 1” size allows easy drop-in placement in system

• Connection posts allow for quick wire-in to circuitry

• 0402 components provide easy handling and customization.

4.1 ISL70321SEHDEMO1Z Evaluation Board

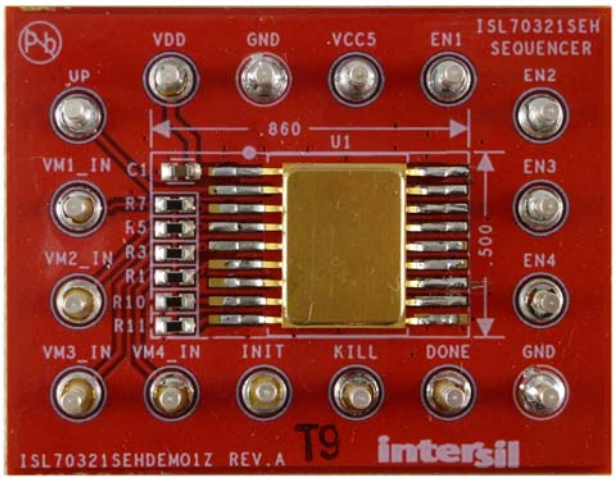

Figure 8. Top of Board

Figure 9. Bottom of Board

4.2 ISL70321SEHDEMO1Z Schematic

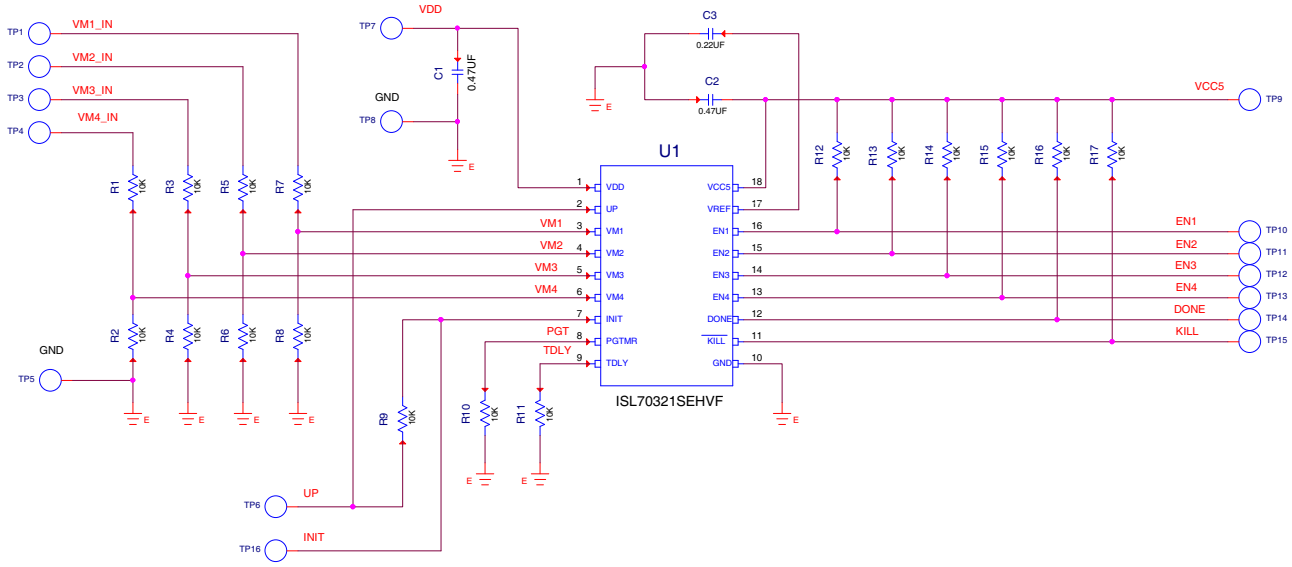

Figure 10. ISL70321SEHDEMO1Z Schematic

4.3 Bill of Materials

Item	Qty	Reference Designator	Value	Tol (%)	Rating	Type	PCB Footprint	Manufacturer	Manufacturer Part Number
1	1	U1						Intersil	ISL70321SEH/PROTO
2	2	C1, C2	0.47µF	10	16V	X7R	SM0603	Various	Generic
3	1	C3,	0.22µF	10	16V	X7R	SM0402	Various	Generic
4	17	R1 - R17	10kΩ	1	1/16W	CHIP	SM0402	Various	Generic

4.4 Board Layout

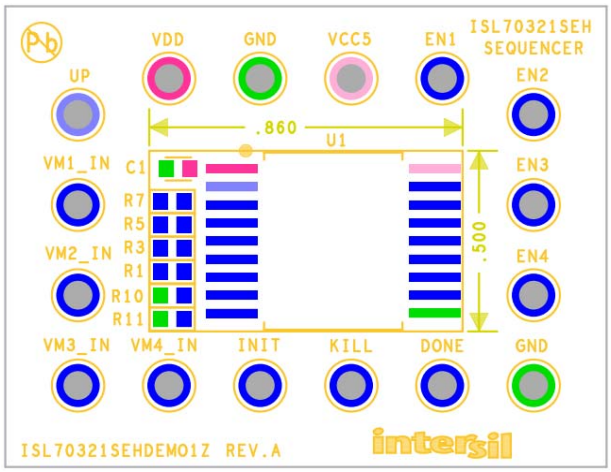

Figure 11. Top Silkscreen

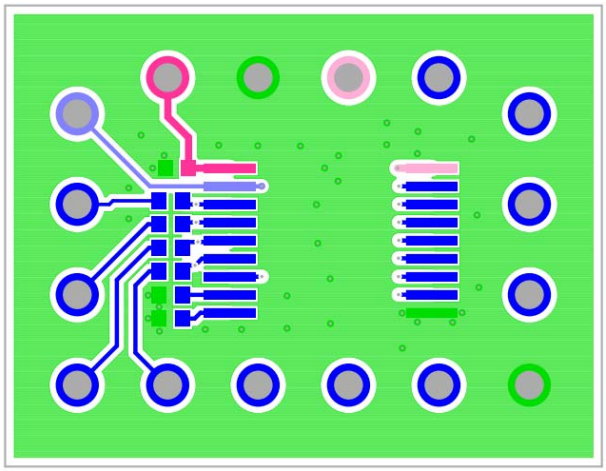

Figure 12. Top Layer

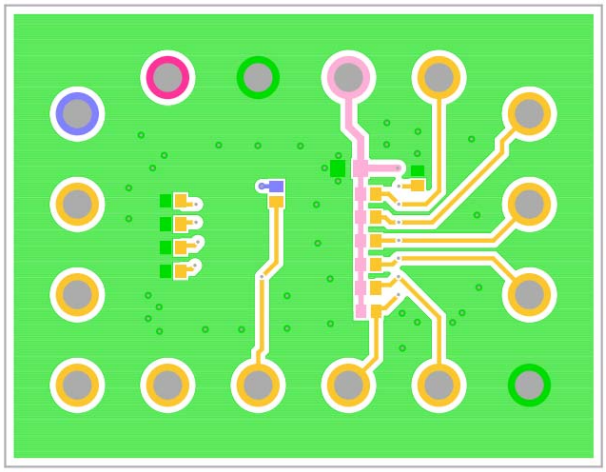

Figure 13. Bottom Trace Layers

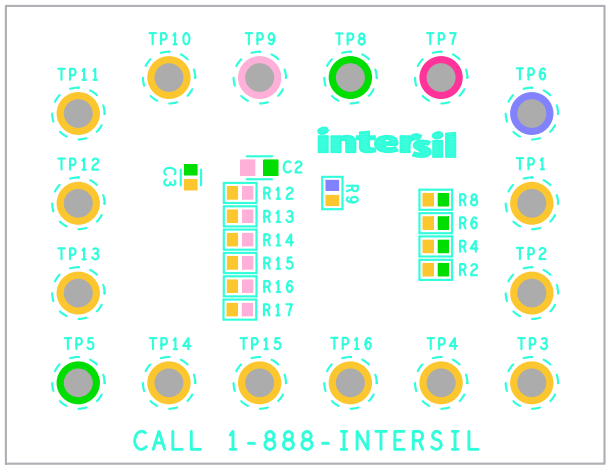

Figure 14. Bottom Silkscreen

5. Revision History

Rev.	Date	Description
0.00	Jul 24, 2017	Initial release

ISL70321SEHDEMO1Z

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