User's Manual

Development Kit S7G2 (DK-S7G2)

User's Manual

Renesas Synergy™ Platform
Synergy Tools & Kits
Kits: DK-S7G2 v4.1

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This Renesas Synergy™ Development Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Renesas Synergy™ Development Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

Renesas Synergy™ Platform

Development Kit S7G2 (DK-S7G2) v4.1

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1. Overview

The Development Kit S7G2 (DK-S7G2) provides easy-to-access interfaces to the peripherals of the S7G2 microcontroller for application development. The kit includes breakout pin headers for direct access to the S7G2 microcontroller I/O pins. DIP configuration switches allow easy transition between different board configurations and ensure that the signal lines are always properly connected.

- Renesas Synergy™ S7G2 Microcontroller Group
  - R7FS7G27H2A01CBD
  - 224-pin Ball Grid Array package
  - 240 MHz Arm® Cortex® M4 core with FPU
  - 640 KB on-chip SRAM
  - 4 MB on-chip code flash memory
  - 64 KB on-chip data flash memory
- Connectivity
  - One HS Host USB and one FS Device USB connector for the Main MCU
  - SEGGER J-Link® On-board (OB) interface for debugging and programming of the S7G2 MCU. A 20-pin JTAG/SWD interface is also provided for connecting optional external debuggers and programmers.
  - Four PMOD connectors, allowing use of appropriate PMOD compliant peripheral plug-in modules for rapid prototyping
  - Pin headers for access to power and signals for the Main MCU
  - Terminal block connector for access to RS233/485 and CAN interfaces
  - 3.5 mm analog audio output jack
  - Right-angle socket for connecting an optional external LCD display
- Multiple clock sources
  - Main MCU oscillator crystals, providing precision 24.000 MHz and 32,768 Hz reference clocks
  - Additional low-precision clocks are available internal to the Main MCU
- MCU reset push button switch

- Operating voltage
  - External 5 V input through a 5 mm barrel jack connector supplies the on-board power regulator to power the Development Kit logic and interfaces.
  - Button cell battery holder for on-board battery backup
  - Current sense resistors and power measurement test points for precision current consumption measurement.
- A green LED indicating availability of regulated power
- Two green and two red User LEDs, controlled by the Main MCU firmware
- Three User push-button switches and a User Potentiometer, all of which are monitored by the Main MCU firmware
- MCU boot configuration jumper
- 256 Mb SDRAM
- 256 Mb QSPI Serial Flash
- 4-GB e.MMC
- SD Card socket
- On-board 4.3” 480x272 RGB Graphic TFT LCD module with Resistive Touch overlay
- Parallel Data Capture (PDC) Camera Module
- Configuration DIP switches with LED indicators for each functional block

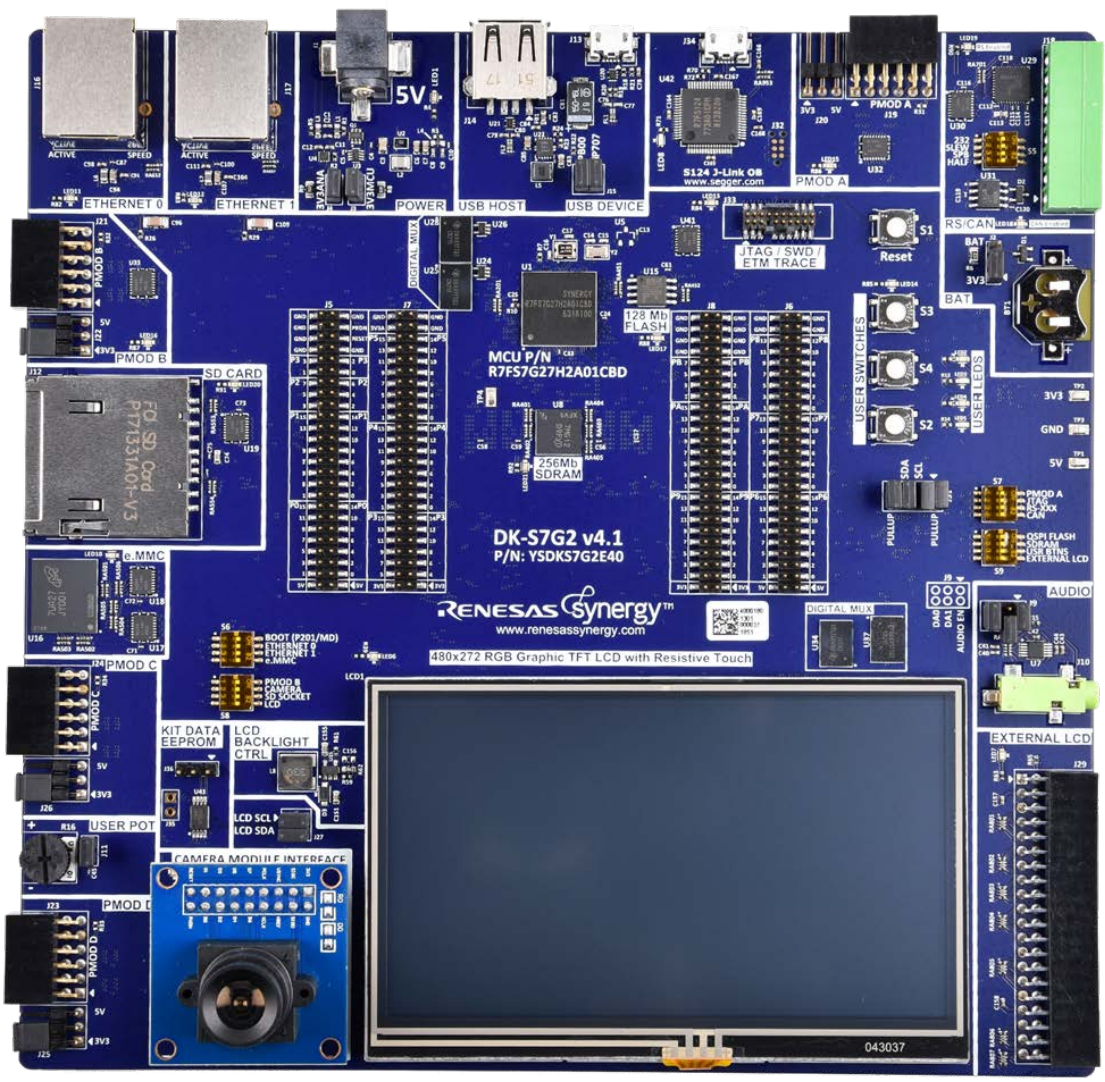


Figure 1. DK-S7G2 Top Side

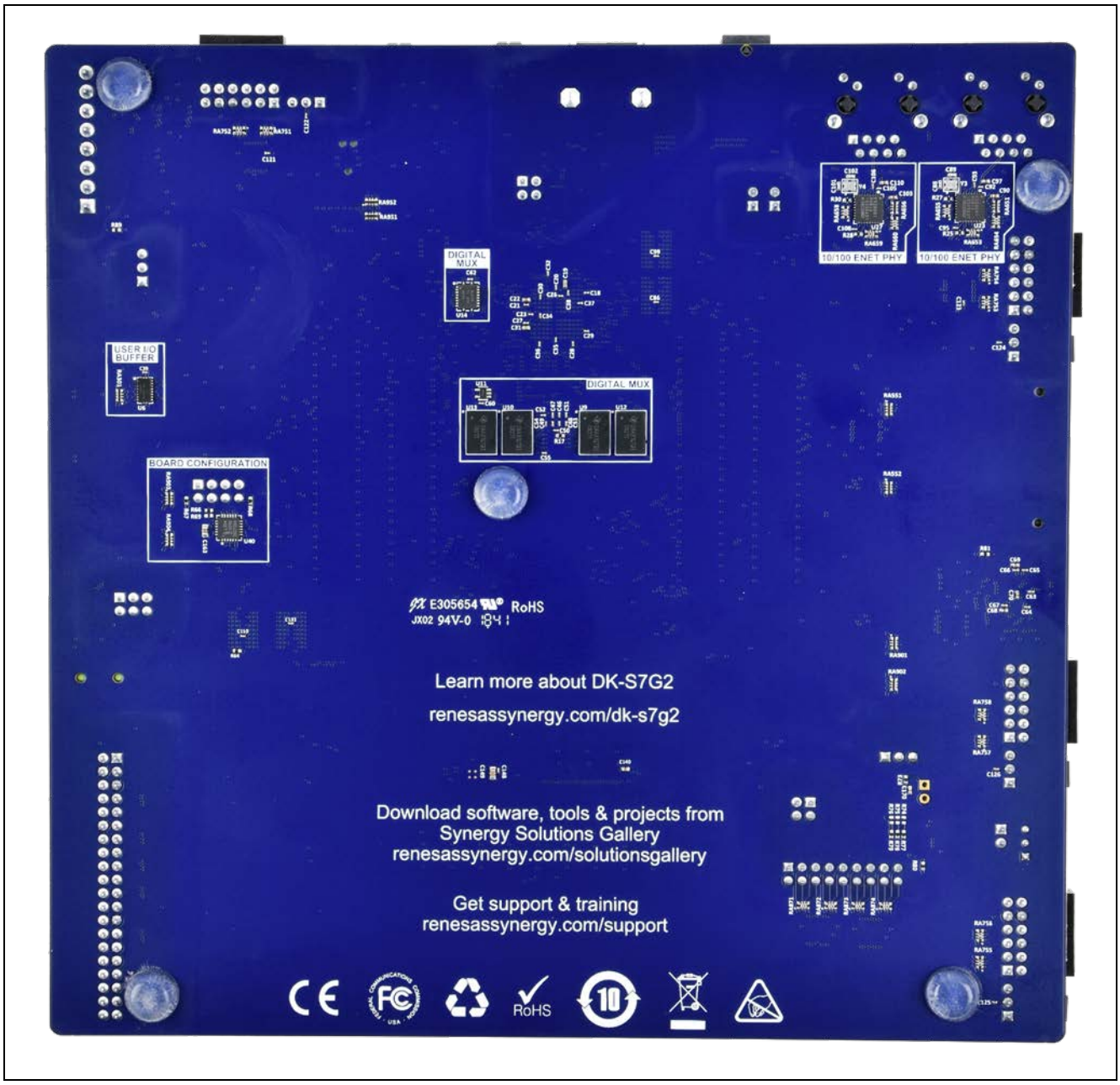


Figure 2. DK-S7G2 Bottom Side

2. Kit Contents

The following components are included in the Development Kit S7G2 (DK-S7G2):

- 1x DK-S7G2 board
- Detachable CMOS VGA camera module
- 1x USB Type-A to Micro-B cable
- 1x Ethernet patch cable
- UART and CAN adapter block
- Multi-region 5 V power supply

3. Getting Started with Embedded Application Development on DK-S7G2

To develop and execute embedded applications on the DK-S7G2 using the Synergy Platform, Synergy Software Package and development tools are required to be installed on your computer.

Step 1: Create My Renesas Account (if you do not have one already)

You need a **My Renesas** account to download software, development tools, and application projects. Log in to or Sign up for a **My Renesas** account at www.update.renesas.com/SSO/login.

Step 2: Download and Install Synergy Software Package and Development Tools

The Synergy Software Package, J-Link USB drivers, and one of the two supported tool chains are bundled and available as single downloadable file as follows:

A. **IAR Platform Installer** installs Synergy Software Package and IAR Embedded Workbench® for Renesas Synergy™ IDE with IAR complier and J-Link USB drivers.
Download from www.renesas.com/synergy/ewsynergy.

B. **e² studio Platform Installer** installs Synergy Software Package and e² studio for Synergy IDE with IAR complier and J-Link USB drivers.
Download from www.renesas.com/synergy/e2studio.

Note: The DK-S7G2 uses J-Link® On-board (OB) debug interface. While J-Link drivers are necessary to establish debug connection between the host PC and the DK-S7G2, they are not required to run the Out-of-Box (OoB) Demonstration Application that the DK-S7G2 comes pre-programmed with. Refer to the *DK-S7G2 Quick Start Guide* for more details.

Step 3: Explore Existing Application Projects for the DK-S7G2

Renesas provides several application projects to demonstrate different capabilities of the S7G2 MCU Group. These application projects can also serve as a good starting point for you to develop your custom applications. Application projects available for the DK-S7G2 are listed at www.renesas.com/synergy/dk-s7g2.

Notes: 1. Every application project includes the project files, an application note, and instructions to import the application project.
2. On downloading the application project from the website to your computer, the application projects have to be built using one of the two supported tool chains before they can be downloaded on to the DK-S7G2 board.

4. DK-S7G2 Hardware Details

4.1 Jumpers and DIP Switch Settings

4.1.1 Default Board Configuration

The Circuit Group for each jumper is the designation found in the board schematic. See Section 6, Electrical Schematics. Functional details for many of the listed jumpers may be found in Section 5.4, Connectivity and Settings. The following table describes the default settings for each jumper on the DK-S7G2.

Table 1. Default Jumper Settings

Location	Circuit Group	Default Open/Closed	Function
J2	Power	Jumper on pins 1-2	MCU VBAT source
J3	Power	Open	MCU main 3.3 V current measurement
J4	Power	Open	MCU analog 3.3 V current measurement
J9	Audio	All open	Connects audio amplifier to MCU
J11	User	Jumper on pins 1-2	Connects user potentiometer to MCU
J15	USB	Jumper on pins 1-2 and on pins 3-4	Connects USBH_OC (P707) and USBH_VBUSEN (PB00) to USB power regulator
J20	PMOD	Jumper on pins 1-2	Configures PMOD A for 3.3 V operation
J22	PMOD	Jumper on pins 1-2	Configures PMOD B for 3.3 V operation
J26	PMOD	Jumper on pins 1-2	Configures PMOD C for 3.3 V operation
J25	PMOD	Jumper on pins 1-2	Configures PMOD D for 3.3 V operation
J27	LCD	Jumper on pins 1-2 and on pins 3-4	Connects LCD I2C to system I2C
J31	Configuration	Jumpers on pins 1-2, pins 3-4, pins 5-6, and pins 7-8	Connects configuration I/O expander I2C to system I2C and connects pullup resistors to the system I2C signals.
J35	Kit Data	Not Populated	For factory use only

The following table describes the default settings for each DIP switch on the DK-S7G2.

Note: An ON setting means that the switch is closed, and an OFF setting means that the switch is open.

Table 2. Default Jumper Settings

Location	Circuit Group	Default Open/Closed	Function
S5-1	RS Config	ON	Sets the transceiver to RS-232 mode
S5-2	RS Config	OFF	Sets the RS Slew Rate (N/A for RS-232 mode)
S5-3	RS Config	OFF	Sets the RS SPB (N/A for RS-232 mode)
S5-4	RS Config	OFF	Enables the RX output
S6-1	Peripheral Config	OFF	Sets Boot mode (MD) to normal boot
S6-2	Peripheral Config	OFF	Disables Ethernet 0
S6-3	Peripheral Config	OFF	Disables Ethernet 1
S6-4	Peripheral Config	OFF	Disables the e.MMC
S7-1	Peripheral Config	OFF	Disables PMOD A
S7-2	Peripheral Config	ON	Enables the JTAG interface
S7-3	Peripheral Config	OFF	Disables the Serial Port (RS232/485) interface
S7-4	Peripheral Config	OFF	Disables the CAN interface
S8-1	Peripheral Config	OFF	Disables PMOD B
S8-2	Peripheral Config	OFF	Disables the Camera Module
S8-3	Peripheral Config	OFF	Disables the SD Card
S8-4	Peripheral Config	ON	Enables the on-board LCD
S9-1	Peripheral Config	OFF	Disables the QSPI Flash
S9-2	Peripheral Config	OFF	Disables the SDRAM
S9-3	Peripheral Config	OFF	Disables the User Pushbuttons
S9-4	Peripheral Config	OFF	Disables the External LCD interface

5. Hardware Layout

5.1 System Block Diagram

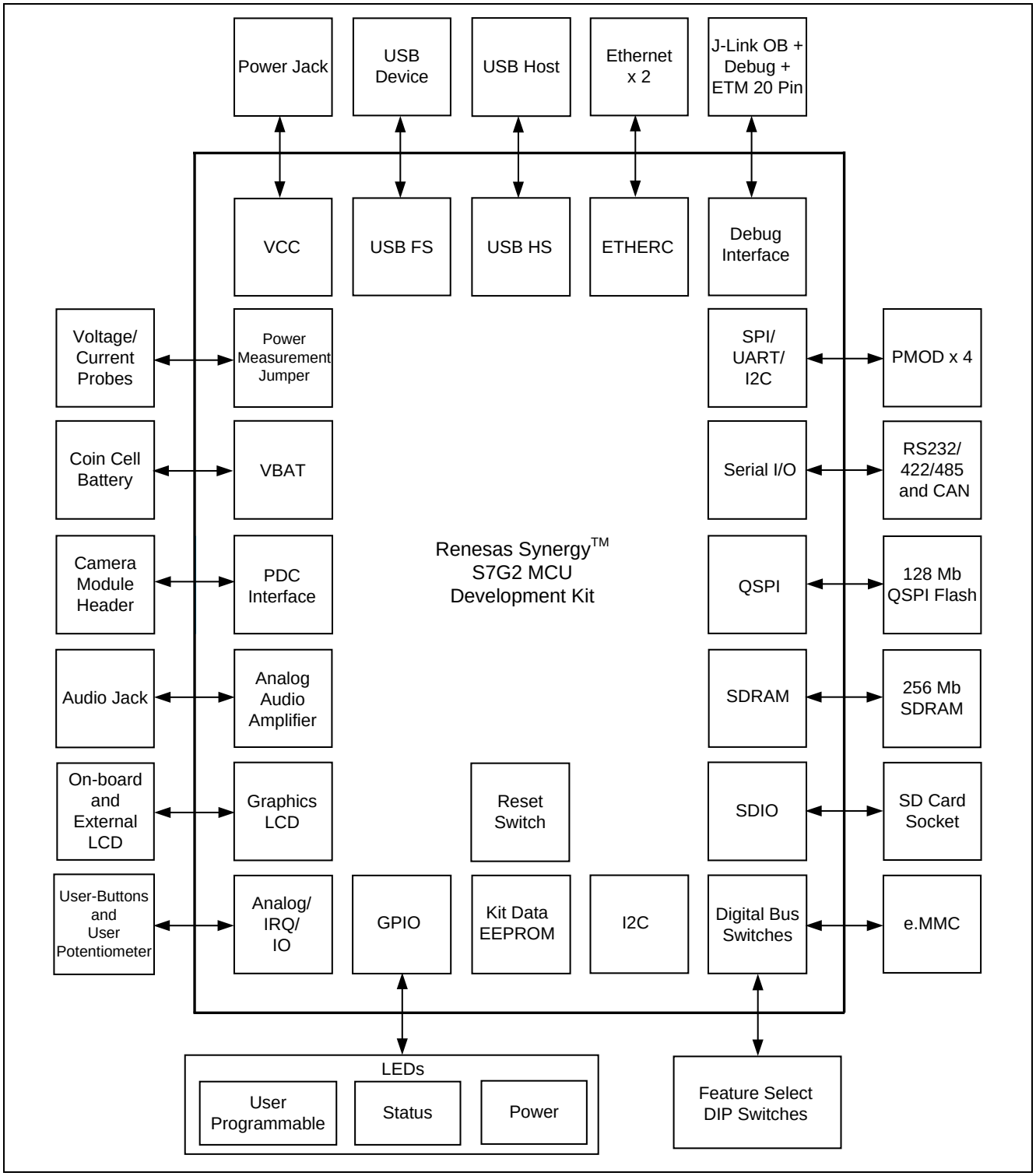


Figure 3. DK-S7G2 Block Diagram

5.2 Power Requirements

DK-S7G2 is designed for +5 V operation. A 5 V, 2.5 A wall-mounted power supply provides power through a barrel jack connector (J1) on DK-S7G2. The input power jack J1 supplies the main 5 V power to the system. This input supplies power to a +3.3 V regulator (U2), which supplies power to most of the digital devices on the board. DK-S7G2 cannot be powered using any of the USB connectors on the board.

5.2.1 Power-up Behavior

When powered, the green LED in the POWER section (LED1) lights up. See the *DK-S7G2 Quick Start Guide (QSG)* for details on the default power-on behavior of the DK-S7G2.

Figure 4. Input Power section

5.2.2 Battery Supply Configuration

An external battery may be installed in the CR1220 coin cell battery holder. This battery is connected only to VBAT on the S7G2 MCU and is used for backup power. The VBAT voltage powers the Realtime Clock (RTC) power domain of the S7G2 microcontroller, and keeps this domain powered even when the main power is removed.

J2 configures the source for VBAT. Place a jumper on pins 1-2 to connect the battery to VBAT. Place a jumper on pins 2-3 to connect the main +3.3 V power to VBAT.

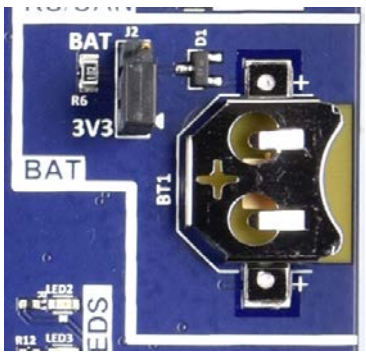


Figure 5. Battery Holder

5.2.3 Measuring Current Consumption

DK-S7G2 provides precision 50 mΩ resistors (Bourns, part number CRM0805-FW-R050ELF) for current measurement of the main 3.3 V MCU power, and the 3.3 V analog MCU power. Measure the voltage drop across these resistors and use Ohm's Law to calculate the current. For convenience, J3 is provided to measure the main 3.3 V MCU power, and J4 is provided to measure the 3.3 V analog MCU power. See Figure 4 for the location of J3 and J4.

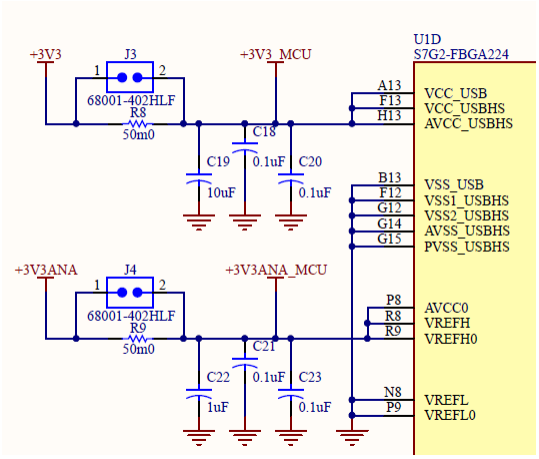


Figure 6. MCU Current Measurement Circuit

5.3 Main Components

- Main MCU
  - Renesas Synergy™ S7G2 MCU device, part number R7FS7G27C3A01CFB#AA0 (U1)
    - Main MCU
- J-Link MCU
  - Renesas Synergy™ S124 MCU device, part number R7FS124773A01CFM#AA0 (U42)
    - J-Link MCU
- USB Connectors
  - FCI, part number 10118192-0001LF (J13, J34)
    - Micro USB 2.0 Female connector
    - Primary communication with Main MCU and J-Link MCU
  - FCI, part number 87583-3010RPALF (J15)
    - USB Type-A Female connector for Host USB
- Ethernet
  - Abracon, part number ARJC02-111009D (J16, J17)
    - Ethernet 10/100 Base-TX RJ45 connector with integrated magnetics
  - Microchip/Micrel, part number KSZ8091RNBIA (U23, U27)
    - Ethernet 10/100 Base-TX PHY controller
- RS232/485 and CAN
  - Amphenol FCI, part number 20020110-C081A01LF (J18)
    - 3.5 mm pitch terminal block for RS232/485 and CAN signals
  - Renesas Intersil, part number ISL41387IRZ (U29)
    - RS232/485 transceiver
  - Infineon, part number IFX1050GVIO (U31)
    - CAN transceiver, 1M Baud
- Push-Buttons
  - C&K, part number KSC222J LFS (S1, S2, S3, S4)
    - Momentary push-button switch
    - Used for system reset and user-defined functions

- DC-DC Buck-Boost Switching Regulator
  - Renesas Intersil, part number ISL91107IINZ (U2)
    - Generates system 3.3 V from main 5 V input
- LDO Regulator
  - Texas Instruments, part number TLV70033DSE (U4)
    - Low-dropout linear regulator
    - Generates analog 3.3 V from main 5 V input
- PMOD Connectors
  - Sullins, part number PPPC062LJBN-RC (J19, J21, J23, J24)
    - 12-pin right angle connector for PMOD
- Pin Headers
  - Amphenol ICC / FCI, part number 57202-G52-25LF (J4, J6, J7, J8)
    - 50 position pin header, 2 mm pitch
    - Provides signal breakout and access for Main MCU signals
- LCD
  - LXD, part number M1790C (LCD1)
    - 480 x 272 RGB Graphic TFT LCD with Resistive Touch
  - FCI, part number 62684-401100ALF (J28)
    - 40 position FPC connector
  - Semtech, part number SX8676IWLTRT (U36)
    - Touchscreen controller for Resistive Touch
- SDRAM
  - Micron, part number MT48LC16M16A2B4-7E IT:G (U8)
    - 256 Mb 16M x 16, 3.3 V
- e.MMC
  - Micron, part number MTFC4GACAJCN-4M IT (U16)
    - 4 GB, 3.3 V
- QSPI Flash
  - Macronix, part number MX25L12835FM2I-10G (U15)
    - 256 Mb QSPI serial flash

5.4 Connectivity and Settings

5.4.1 Device USB

The DEVICE USB Micro-B connection jack (J13) connects the Main MCU to an external USB Host, FS capable, allowing communications for testing and use of the Main MCU firmware. Power for the DK-S7G2 cannot be received from this connector. The DEVICE USB interface can detect the presence of power from the USB Host PC. USB Host power received at the DEVICE USB interface is not connected to the DK-S7G2 5 V power bus.

Table 3. Device USB Connector (J13)

USB Device Connector		**DK-S7G2**
Pin	**Description**	**Signal/Bus**
1	+5VDC, connected to a sense voltage 2/3 divider to allow Main MCU sensing of Host presence	+5VUSB P407/USB_VBUS = 2/3(5VUSB)
2	Data-	USB_DM
3	Data+	USB_DP
4	USB ID, jack internal switch, cable inserted	N.C.
5	Ground	GND

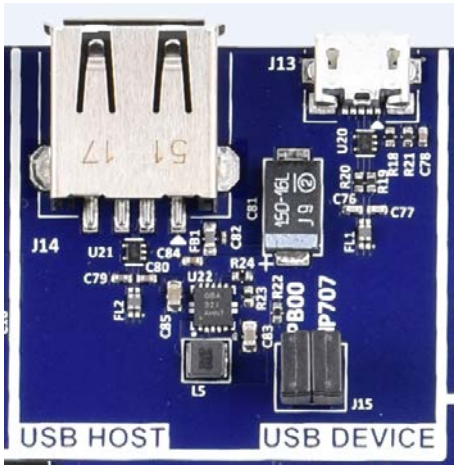


Figure 7. USB Connectors

5.4.2 Host USB

The Host USB Type-A connection jack (J14) connects the Main MCU to external USB devices, HS capable, allowing communications for testing and use of the Main MCU firmware. The USB Host connection includes a TBS2501 USB Power Switch (U22) to provide regulated 5 V USB power to connected devices. The Power Switch provides a nominal 500 mA, and maximum of 720 mA to connected USB devices.

The USB Power Switch is controlled by the S7G2 MCU using P707 (USBHS Overcurrent) and PB00 (USBHS VBUS Enable). To use these ports for other DK-S7G2 functions, these signals may be disconnected from the USB Power Switch by removing the jumpers from J15.

Table 4. Device USB Connector (J14)

USB Device Connector		**DK-S7G2**
Pin	**Description**	**Signal/Bus**
1	+5VDC	+5VUSB Host Power, from U22
2	Data-	USBHS_DM
3	Data+	USBHS_DP
4	Ground	GND

5.4.3 Debug USB

The J-Link OB USB Micro-B connection jack (J34) connects the S124 J-Link MCU to an external USB Host, FS capable, allowing re-programming and debugging of the Main MCU firmware. Power for the DK-S7G2 can NOT be received from this connector.

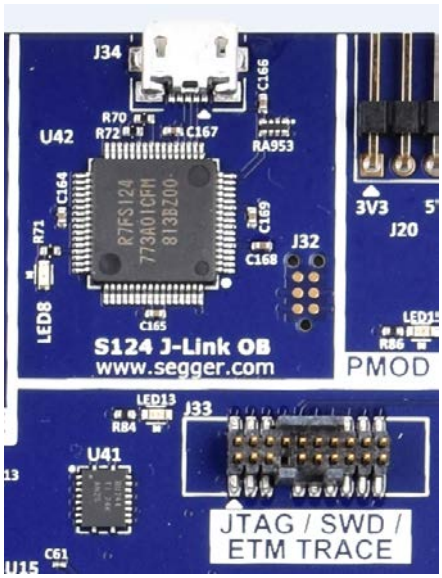


Figure 8. S124 J-Link OB and JTAG

The J-Link OB interface is multiplexed with the JTAG interface and can collectively be referred to as the Programming Interface.

Table 5. Debug USB Connector (J34)

Debug USB Connector		**DK-S7G2**
Pin	**Description**	**Signal/Bus**
1	+5VDC	+5V_JUSB
2	Data-	U2 USB_DM (U2-18)
3	Data+	U2 USB_DP (U2-19)
4	USB ID, jack internal switch, cable inserted	N.C.
5	Ground	GND

5.4.4 JTAG/SWD/TRACE

A 20-pin Cortex® Debug Connector is provided at J33. See Figure 8.

A digital bus switch (U41) is provided to isolate the JTAG signals from the rest of the system. To enable the JTAG header (J33), set DIP Switch S7-2 to ON. When the JTAG interface is enabled, LED13 is illuminated.

Table 6. JTAG/SWD/TRACE Connector (J33)

JTAG Connector				DK-S7G2
Pin	**JTAG Pin Name**	**SWD Pin Name**	**ETM Pin Name**	**Signal/Bus**
1	VTref	VTref	VTref	+3V3
2	TMS	SWDIO	N/A	P108/SWDIO (U1-51)
3	GND	GND	GND	GND
4	TCK	SWCLK	N/A	P300/SWCLK (U1-50)
5	GND	GND	GND	GND
6	TDO	SWO	N/A	P109 (U1-52)
7	Key	Key	Key	N.C.
8	TDI	NC/EXTb	N/A	P110 (U1-53)
9	GNDDetect	GNDDetect	GNDDetect	N.C. (short E31 to connect to GND)
10	nSRST	nSRST	nSRST	RESET# (U1-38)
11	N/A	N/A	N/A	N.C.
12	N/A	N/A	TCLK	PA12
13	N/A	N/A	N/A	N.C.
14	N/A	N/A	TDATA0	PA13
15	N/A	N/A	GND	GND
16	N/A	N/A	TDATA1	PA14
17	N/A	N/A	GND	GND
18	N/A	N/A	TDATA2	PA15
19	N/A	N/A	GND	GND
20	N/A	N/A	TDATA3	P813

The Cortex® Debug Connector is fully described in the Arm® CoreSight™ Architecture Specification.

5.4.5 LEDs

There are 21 LEDs provided on the DK-S7G2. In addition, each Ethernet connector has built-in link status and link speed LEDs.

The behavior of the LEDs on the DK-S7G2 is described in the following table.

Table 7. DK-S7G2 LED Functions

Designator	Color	Function	MCU Control Port	MCU Pin
LED1	Green	Main Power Indicator	N/A	N/A
LED2	Green	User LED	P807	U1-P12
LED3	Red	User LED	P808	U1-K7
LED4	Green	User LED	P809	U1-K8
LED5	Red	User LED	P810	U1-P3
LED6	Green	LCD Enabled	N/A	N/A
LED7	Green	External LCD Enabled	N/A	N/A
LED8	Red	J-Link connect status	S124 P103	S124 pin 45
LED9	Green	Camera Module Enabled	N/A	N/A
LED10	Green	e.MMC Enabled	N/A	N/A
LED11	Green	Ethernet 0 Enabled	N/A	N/A
LED12	Green	Ethernet 1 Enabled	N/A	N/A
LED13	Green	JTAG Enabled	N/A	N/A
LED14	Green	User Buttons and LEDs Enabled	N/A	N/A

LED15	Green	PMOD A Enabled	N/A	N/A
LED16	Green	PMOD B Enabled	N/A	N/A
LED17	Green	QSPI Enabled	N/A	N/A
LED18	Green	CAN Enabled	N/A	N/A
LED19	Green	RS-232/485 Enabled	N/A	N/A
LED20	Green	SD Card Enabled	N/A	N/A
LED21	Green	SDRAM Enabled	N/A	N/A

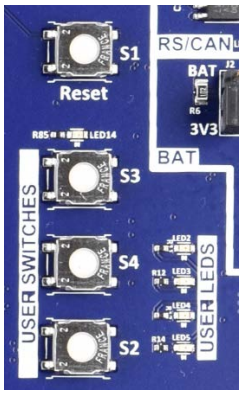


Figure 9. Reset Switch, User Switches, and User LEDs

5.4.6 Switches

Four miniature, momentary, mechanical push-button type SMT switches are mounted on DK-S7G2.

Pressing the Reset switch (S1) generates a reset signal to restart the Main MCU.

Table 8. DK-S7G2 Switches

Designator	Function	MCU Control Port	MCU Pin
S1	MCU Reset Switch	RESET#	U1-F8
S2	User Switch	P006 (AN102)	U1-P10
S3	User Switch	P010 (AN103)	U1-M10
S4	User Switch	P011 (AN104)	U1-N10

A digital bus switch (U6) is provided to isolate the User Switch signals from the rest of the system. To enable the User Switches, set DIP Switch S9-3 to ON. When the User Switches are enabled, LED14 is illuminated.

5.4.7 PMOD A

A 12-pin PMOD Type-2A connector is provided at PMOD A. The Main MCU acts as the SPI master, and the connected module acts as an SPI slave device. This interface may additionally be re-configured in firmware as several other PMOD types.

This PMOD interface may supply either 5 V or 3.3 V to the PMOD device. This can be selected by placing a jumper on the appropriate pins of J20. For 3.3 V operation, place a jumper on pins 1-2, or place a jumper on pins 2-3 for 5 V operation.

A digital bus switch (U32) is provided to isolate the PMOD A signals from the rest of the system. To enable PMOD A, set DIP Switch S7-1 to ON. When the PMOD A is enabled, LED15 is illuminated.

Table 9. PMOD A Connector (J19)

PMOD A Connector		DK-S7G2
Pin	**Description**	**Signal/Bus**
1	SS/CTS_RTS	PB02, U1-J11
2	MOSI/TXD	PB04, U1-H10
3	MISO/RXD	PB05, U1-J12
4	SCK	PB03, U1-K12
5	GND	GND

6	VCC	Select using J20
7	INT (slave to master)	P004 (IRQ9), U1-M11
8	RESET (master to slave)	P911, U1-A7
9	Not Specified (GPIO)	P912, U1-B7
10	Not Specified (GPIO)	P913, U1-H8
11	GND	GND
12	VCC	Select using J20

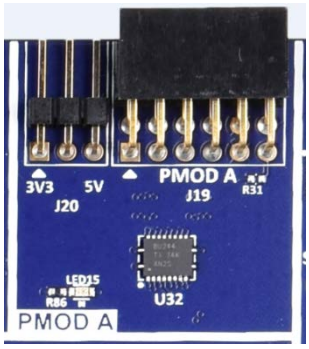


Figure 10. PMOD A

5.4.8 PMOD B

A 12-pin PMOD Type-2A connector is provided at PMOD B. The Main MCU acts as the SPI master, and the connected module acts as an SPI slave device. This interface may additionally be re-configured in firmware as several other PMOD types.

This PMOD interface may supply either 5 V or 3.3 V to the PMOD device. This can be selected by placing a jumper on the appropriate pins of J22. For 3.3 V operation, place a jumper on pins 1-2, or place a jumper on pins 2-3 for 5 V operation.

A digital bus switch (U33) is provided to isolate the PMOD B signals from the rest of the system. To enable PMOD B, set DIP switch S8-1 to ON. When the PMOD B is enabled, LED16 is illuminated.

Table 10: PMOD B Connector (J21)

PMOD B Connector		**DK-S7G2**
Pin	**Description**	**Signal/Bus**
1	SS/CTS_RTS	P507, U1-N6
2	MOSI/TXD	P509, U1-P6
3	MISO/RXD	P510, U1-N7
4	SCK	P508, U1-M7
5	GND	GND
6	VCC	Select using J22
7	INT (slave to master)	P005 (IRQ10), U1-R11
8	RESET (master to slave)	PA05, U1-J3
9	Not Specified (GPIO)	PA06, U1-J2
10	Not Specified (GPIO)	PA07, U1-J1
11	GND	GND
12	VCC	Select using J22

Figure 11. PMOD B

5.4.9 PMOD C

A 12-pin PMOD Type-2A connector is provided at PMOD C. The Main MCU acts as the SPI master, and the connected module acts as an SPI slave device. This interface may additionally be re-configured in firmware as several other PMOD types.

This PMOD interface may supply either 5 V or 3.3 V to the PMOD device. This can be selected by placing a jumper on the appropriate pins of J26. For 3.3 V operation, place a jumper on pins 1-2, or place a jumper on pins 2-3 for 5 V operation.

The ports used for PMOD C are also used for the SDRAM interface. A set of digital bus switches is provided to isolate the SDRAM signals from the rest of the system. To enable PMOD C, the SDRAM must be disabled. To disable the SDRAM, and enable other functions including PMOD C, set DIP switch S9-2 to OFF.

Table 11. PMOD C Connector (J24)

PMOD C Connector		**DK-S7G2**
Pin	**Description**	**Signal/Bus**
1	SS/CTS_RTS	P103, U1-N2
2	MOSI/TXD	P101, U1-P1
3	MISO/RXD	P100, U1-R1
4	SCK	P102, U1-N1
5	GND	GND
6	VCC	Select using J26
7	INT (slave to master)	P008 (IRQ12), U1-N11
8	RESET (master to slave)	P600, U1-L3
9	Not Specified (GPIO)	P601, U1-L2
10	Not Specified (GPIO)	P602, U1-L1
11	GND	GND
12	VCC	Select using J26

Figure 12. PMOD C

5.4.10 PMOD D

A 12-pin PMOD Type-2A connector is provided at PMOD D. The Main MCU acts as the SPI master, and the connected module acts as an SPI slave device. This interface may additionally be re-configured in firmware as several other PMOD types.

This PMOD interface may supply either 5 V or 3.3 V to the PMOD device. This can be selected by placing a jumper on the appropriate pins of J25. For 3.3 V operation, place a jumper on pins 1-2, or place a jumper on pins 2-3 for 5 V operation.

The ports used for PMOD D are also used for the SDRAM interface. A set of digital bus switches is provided to isolate the SDRAM signals from the rest of the system. To enable PMOD D, the SDRAM must be disabled. To disable the SDRAM, and enable other functions including PMOD D, set DIP switch S9-2 to OFF.

Table 12. PMOD D Connector (J23)

PMOD D Connector		DK-S7G2
Pin	**Description**	**Signal/Bus**
1	SS/CTS_RTS	P307, U1-D6
2	MOSI/TXD	P305, U1-D4
3	MISO/RXD	P304, U1-C4
4	SCK	P306, U1-D5
5	GND	GND
6	VCC	Select using J25
7	INT (slave to master)	P009 (IRQ13), U1-R10
8	RESET (master to slave)	P603, U1-K3
9	Not Specified (GPIO)	P604, U1-K2
10	Not Specified (GPIO)	P605, U1-K1
11	GND	GND
12	VCC	Select using J25

Figure 13. PMOD D

5.4.11 Ethernet 0

The Ethernet 0 interface uses an RMII Ethernet Physical Layer Transceiver (PHY) (U23), connected to an RJ45 standard Ethernet connector (J16) with integrated magnetics and status indicators. The Ethernet clock is sourced from a precision 25 MHz clock crystal connected directly to the Ethernet PHY.

A digital bus switch (U25) is provided to isolate the Ethernet 0 signals from the rest of the system. To enable Ethernet 0, set DIP switch S6-2 to ON. When Ethernet 0 is enabled, LED11 is illuminated.

Table 13. Ethernet 0 Port Assignments

Ethernet 0 Signal Description	DK-S7G2 Port
IRQ	P015
RESET#	P903
MDC	P401
MDIO	P402
CRS_DV	P408
TXD_EN	P415
TXD0	P413
TXD1	P414
RXD1	P410
RXD0	P411
RX_ER	P409
REF50CK	P412

Table 14. Ethernet 0 Components

Component	Manufacturer	Manufacturer Part Number
Ethernet PHY	Microchip	KSZ8091RBN
RJ-45 Connector	Abracon	ARJC02-111009D
25 MHz Oscillator	TXC	8Y-25.000MEEQ-T

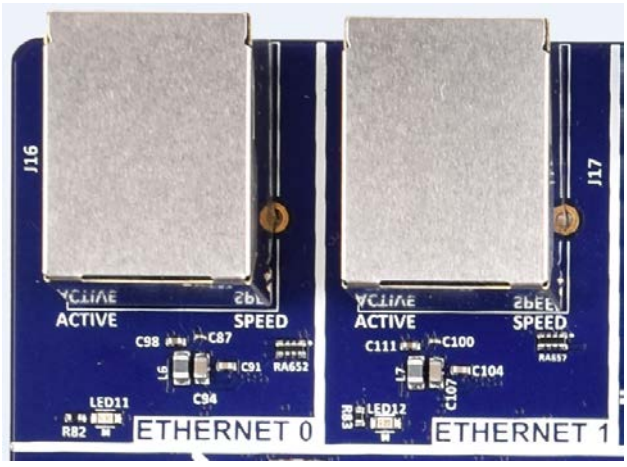


Figure 14. Ethernet Connectors

5.4.12 Ethernet 1

The Ethernet 1 interface uses an RMII Ethernet Physical Layer Transceiver (PHY) (U27), connected to an RJ45 standard Ethernet connector (J17) with integrated magnetics and status indicators. The Ethernet clock is sourced from a precision 25 MHz clock crystal connected directly to the Ethernet PHY.

A digital bus switch (U28) is provided to isolate the Ethernet 1 signals from the rest of the system. To enable Ethernet 1, set DIP switch S6-3 to ON. When Ethernet 1 is enabled, LED12 is illuminated.

Table 15. Ethernet 1 Port Assignments

Ethernet 1 Signal Description	DK-S7G2 Port
IRQ	P002
RESET#	P706
MDC	P403
MDIO	P404
CRS_DV	P705
TXD_EN	P405
TXD0	P700
TXD1	P406
RXD1	P703
RXD0	P702
RX_ER	P704
REF50CK	P701

Table 16. Ethernet 1 Components

Component	Manufacturer	Manufacturer Part Number
Ethernet PHY	Microchip	KSZ8091RBN
RJ-45 Connector	Abracon	ARJC02-111009D
25 MHz Oscillator	TXC	8Y-25.000MEEQ-T

5.4.13 RS232/485 Transceiver

DK-S7G2 includes an Intersil ISL41387 dual-protocol RS-232/485 Transceiver (U29) with loop-back mode and shutdown functions. The shutdown mode disables the receive and transmit outputs of the transceiver, disables the charge pump in RS-232 mode, and places the transceiver in low-current (35 µA) mode.

In RS-232 mode, the on-board charge pump generates RS-232 compliant +/- 5 V Tx output levels. The transceiver supports Rx input levels of +/- 25 V and Tx output levels of +/- 12 V with data rates of up to 650 kbps.

In RS-485 mode, the charge pump is disabled to save power and minimize noise. The RS-485 receiver supports full fail-safe operation that keeps the Rx output in a high state if the inputs are opened or shorted together. The RS-485 transmitter supports three data rates: up to 20 Mbps, 460 kbps, and 115 kbps. Data rates of 460 kbps and 115 kbps in RS-485 mode are slew-rate limited for problem-free communication.

The transceiver can be configured for either RS-232 or RS-485, and for various data rates using DIP switches 1 through 3 on S5, as shown in the following table.

DIP switch S5-4 (HALF) can be used to disable the receiver output and set up the UART in half-duplex mode by controlling the direction through a GPIO pin.

A digital bus switch (U30) is provided to isolate the RS232/485 signals from the rest of the system. To enable the RS232/485 interface, set DIP switch S7-3 to ON. When RS232/485 interface is enabled, LED19 is illuminated.

Table 17. RS232/485 Configuration using DIP Switch S5

Switch 1 (232)	Switch 2 (SLEW)	Switch 3 (SPB)	Data rate	Mode
OFF	ON	ON	115 kbps	485
OFF	ON	OFF	460 kbps	485
OFF	OFF	X	20 Mbps	485
ON	X	X	460 kbps	232

Table 18. RS232/485 Port Assignments

RS232/485 Signal Description	DK-S7G2 Port
RX	P708
DEN	P914
TX	P709
ON	P915

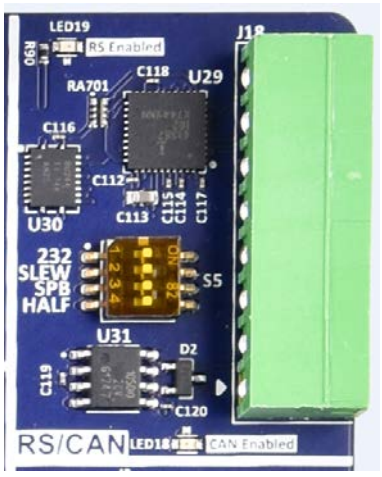


Figure 15. RS232/485 and CAN Interfaces

5.4.14 CAN Transceiver

The Infineon IFX1050GVIO CAN Transceiver (U31) supports transmission rates from 1 kbaud to 1 Mbaud. An On Semiconductor NUP2105 Bus Protector protects the CAN transceiver.

The CAN transceiver is connected to CAN channel 0 on the S7G2 microcontroller and to connector J18.

A digital bus switch (U30) is provided to isolate the CAN signals from the rest of the system. To enable the CAN interface, set DIP switch S7-4 to ON. When the CAN interface is enabled, LED18 is illuminated.

Table 19. CAN Port Assignments

CAN Signal Description	DK-S7G2 Port
TX	P811
RX	P812

5.4.15 QSPI Flash

Included on DK-S7G2 is a Macronix 128 Mb serial flash QSPI memory (MX25L12835FM). The QSPI serial flash device (U15) connects to the QSPI peripheral on the S7G2 MCU and defaults to standard SPI mode initially. The flash memory is enabled for XIP (Execute-in-place) mode directly after power-on.

A digital bus switch (U14) is provided to isolate the QSPI signals from the rest of the system. To enable the QSPI Flash, set DIP switch S9-1 to ON. When the QSPI Flash is enabled, LED17 is illuminated.

Table 20. QSPI Flash Port Assignments

QSPI Signal Description	DK-S7G2 Port
QSPI CS#	P501
QSPI CLK	P500
QSPI DQ0	P502
QSPI DQ1	P503
QSPI DQ2	P504
QSPI DQ3	P505

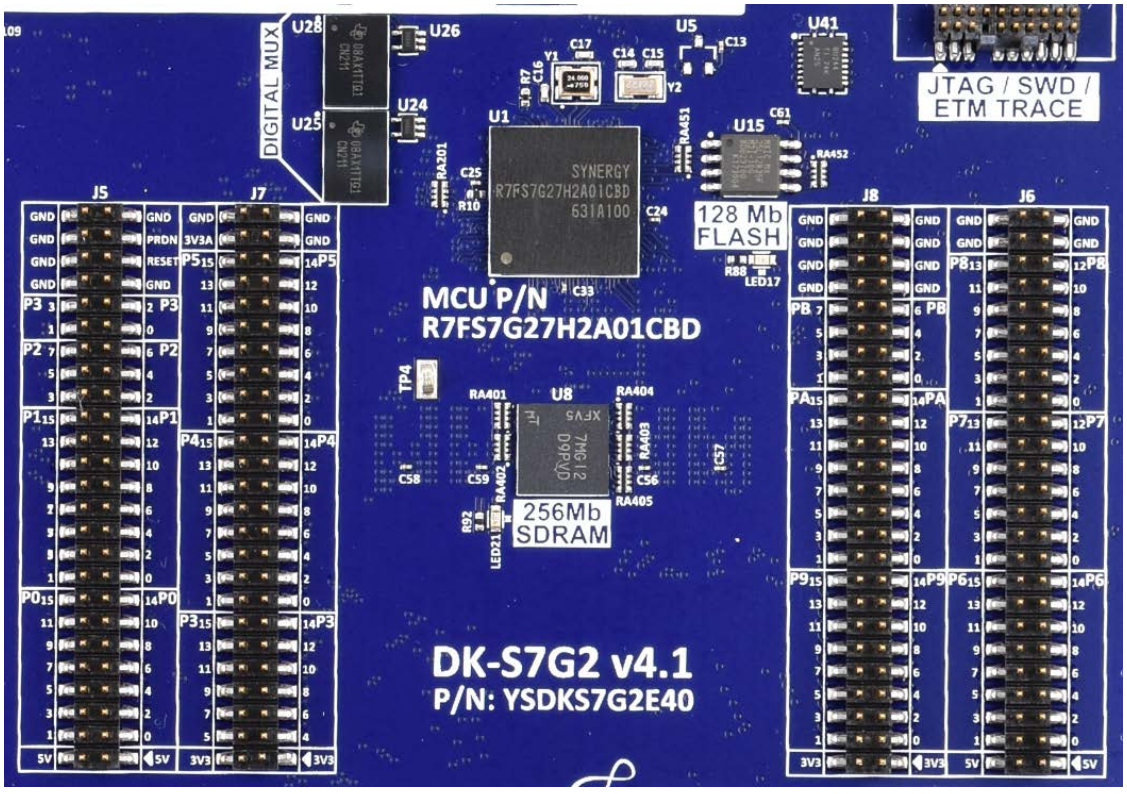


Figure 16. Main MCU, SDRAM, QSPI Flash, and Breakout Pin Headers

5.4.16 SDRAM

Included on DK-S7G2 is a Micron 256 Mb automotive grade SDR SDRAM (U8) in a 4M x 16 x 4 bank configuration (MT48LC16M16A2).

Because the S7G2 MCU ports are highly multiplexed, some of the ports used for SDRAM signals are also used for PMOD C and PMOD D signals. A set of digital bus switches is provided to isolate the SDRAM signals from the rest of the system. To enable the SDRAM, set DIP switch S9-2 to ON. This is done to preserve SDRAM signal integrity. When the SDRAM is enabled, LED21 is illuminated. When the SDRAM is enabled, PMOD C, PMOD D, and the breakout pin headers are not available for the ports used by the SDRAM. To use PMOD C, PMOD D, or access the ports used by the SDRAM at the breakout pin headers, the SDRAM must be disabled.

Table 21. SDRAM Port Assignments

SDRAM Device Signal Description	DK-S7G2 SDRAM Signal Description	DK-S7G2 Port
DQ15	SDRAM DQ15	P801
DQ14	SDRAM DQ14	P800
DQ13	SDRAM DQ13	P603
DQ12	SDRAM DQ12	P604
DQ11	SDRAM DQ11	P605
DQ10	SDRAM DQ10	P614
DQ9	SDRAM DQ9	P613
DQ8	SDRAM DQ8	P612
DQ7	SDRAM DQ7	P107
DQ6	SDRAM DQ6	P106
DQ5	SDRAM DQ5	P105
DQ4	SDRAM DQ4	P104
DQ3	SDRAM DQ3	P103
DQ2	SDRAM DQ2	P102
DQ1	SDRAM DQ1	P101
DQ0	SDRAM DQ0	P100
A12	SDRAM A15	P310
BA1	SDRAM A14	P309
BA0	SDRAM A13	P308
A11	SDRAM A12	P307
A10	SDRAM A11	P306
A9	SDRAM A10	P305
A8	SDRAM A9	P304
A7	SDRAM A8	P303
A6	SDRAM A7	P302
A5	SDRAM A6	P301
A4	SDRAM A5	P111
A3	SDRAM A4	P112
A2	SDRAM A3	P113
A1	SDRAM A2	P114
A0	SDRAM A1	P115
UDQM	SDRAM DQM1	P608
LDQM	SDRAM DQM0	P601
CLK	SDRAM SDCLK	P602
CKE	SDRAM CKE	P609
RAS#	SDRAM RAS#	P311
CAS#	SDRAM CAS#	P312
WE#	SDRAM WE#	P610
CS#	SDRAM SDCS#	P611

5.4.17 SD Card Socket

Included on DK-S7G2 is an SD/MMC card socket (J12) with a four-bit data bus, plus card detect and write protect functions. The SD card socket is connected to channel 0 of the SD/MMC controller on the S7G2 MCU.

A digital bus switch (U19) is provided to isolate the SD card signals from the rest of the system. To enable the SD card socket, set DIP switch S8-3 to ON. When SD Card socket is enabled, LED20 is illuminated.

The SD Card socket conflicts with the e.MMC. To use the SD card, disable the e.MMC by setting S6-4 to OFF.

Table 22. SD Card Port Assignments

SD Card Signal Description	DK-S7G2 Port
CMD	P412
CLK	P413
CD	P903
WP	P414
D0	P411
D1	P410
D2	P206
D3	P205

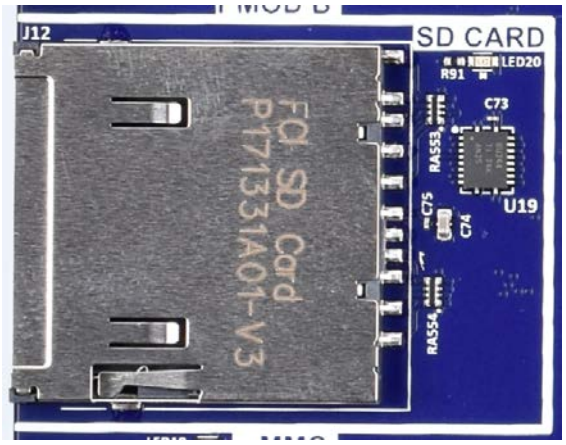


Figure 17. SD Card Socket

5.4.18 e.MMC

Included on DK-S7G2 is a Micron 4 GB e.MMC memory device with an eight-bit data bus (MTFC4GACAJCN-4M IT). The e.MMC memory is connected to channel 0 of the SD/MMC controller on the S7G2 MCU.

Digital bus switches (U17 and U18) are provided to isolate the SD card signals from the rest of the system. To enable the SD card socket, set DIP switch S6-4 to ON. When the e.MMC is enabled, LED10 is illuminated.

Since this is an embedded device, the CD and WP signals are not used by the e.MMC. When the e.MMC is enabled, these two signals are pulled high so the S7G2 MCU SD/MMC peripheral functions correctly.

The e.MMC conflicts with the SD Card socket. To use the e.MMC, disable the SD Card Socket by setting S8-3 to OFF.

Table 23 e.MMC Port Assignments

e.MMC Signal Description	DK-S7G2 Port
CMD	P412
CLK	P413
CD	P903
WP	P414
D0	P411
D1	P410
D2	P206
D3	P205
D4	P204
D5	P203
D6	P202
D7	P313

Figure 18. e.MMC

5.4.19 Camera Interface

The DK-S7G2 Camera Module includes an Omnivision OV7670 image sensor with adjustable lens. The image sensor combines a VGA camera with an image processor and can be controlled through an I²C bus interface connected to the Serial Communications Interface (SCI) peripheral on the S7G2 microcontroller.

The 8-bit data bus supports data formats YUV/YCbCr 4:2:2, RGB565/555, GRB 4:2:2, or Raw RGB Data.

The sensor has an image array operating at up to 30 frames per second in VGA. Image quality, image format, and output data transfer are user programmable. The sensor supports image processing such as exposure control, gamma correction, and adjustment of white balance, color saturation, and hue.

The Camera Module can be installed on J30 of the DK-S7G2.

Digital bus switches (U38 and U39) are provided to isolate the Camera signals from the rest of the system. To enable the Camera Module interface, set DIP switch S8-2 to ON. When the Camera Module interface is enabled, LED9 is illuminated.

The camera module conflicts with Ethernet 1. Ethernet 1 must be disabled for the Camera interface to function correctly. To disable Ethernet 1, set DIP switch S6-3 to OFF.

Table 24. Camera Interface Port Assignments

Camera Interface Signal Description	J30 Pin Number	DK-S7G2 Port
+3.3 V	1	N/A
GND	2	N/A
I2C SCL	3	PA03
I2C SDA	4	PA02
VSYNC	5	P512
HSYNC	6	P704
PIXCLK	7	P705
PCKO	8	P511
PXD7	9	P403
PXD6	10	P404
PXD5	11	P405
PXD4	12	P406
PXD3	13	P700
PXD2	14	P701
PXD1	15	P702
PXD0	16	P703
RESET#	17	PB06
PWDN#	18	PB07

Figure 19. Camera Module

5.4.20 Audio Jack

DK-S7G2 contains an On Semiconductor 135 mW stereo headphone power amplifier (NCP2809BDMR2G). The output signals are generated by the Digital-to-Analog peripheral signals DA0 and DA1 on the S7G2 microcontroller.

The audio interface also uses P902 as a GPIO signal that drives the shutdown signal on the amplifier. Port P015 (DA1) is shared with Ethernet 0. Ethernet 0 must be enabled to use Audio Jack. To enable Ethernet 0, set DIP switch S6-2 to ON.

Note: Ethernet 0 and Audio Jack cannot be used at the same time.

To isolate Audio Jack and prevent interference with Ethernet 0, remove the jumpers from J9. Silkscreen next to J9 shows the related jumper positions for each signal in the audio interface.

Table 25. Audio Jack Port Assignments

Audio Jack Signal Description	DK-S7G2 Port	Jumper J9 Connections
Amp SHDN#	P902	Pins 1-2
OUT-Left	P014 (DA0)	Pins 5-6
OUT-Right	P015 (DA1)	Pins 3-4

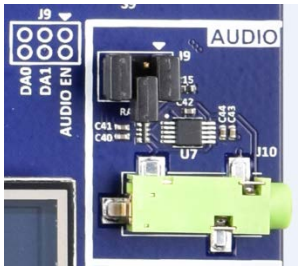


Figure 20. Audio Jack

5.4.21 LCD

DK-S7G2 includes an LXD M7190C 4.3” TFT RGB 480x272 LCD panel with Resistive Touch screen. The LCD interface supports a 16-bit LCD data bus and includes a resistive touch controller and LED backlight driver.

The resistive touch interface uses a Semtech SX8676IWLTRT touch controller, driven by the MCU I^2C bus. The resistive touch controller may be isolated from the system I^2C signals by removing the jumpers from header J27.

The LED backlight controller is an On Semiconductor CAT4237TD LED driver.

Some LCD modules produce excessive Electromagnetic Interference (EMI), which can cause undesirable performance. To compensate for this potential EMI radiation, DK-S7G2 provides footprints for optional Pi filters on each of the LCD data and control lines. By default, these Pi filters are not installed, but zero-ohm bridge resistors are installed. DK-S7G2 is designed to use Murata NFL21SP506X1C3D filters components, in a 4-pin 0805 surface mount package. Be sure to remove the respective bridge resistor when installing a Pi filter for the desired signal.

A digital bus switch (U34) is provided to isolate the LCD signals from the rest of the system. To enable the on-board LCD, set DIP switch S8-4 to ON. When the on-board LCD is enabled, LED6 is illuminated.

Table 26. LCD Control Signal Port Assignments

LCD Control Signal Description	DK-S7G2 Port
LCD SCL (I2C)	PA03
LCD SDA (I2C)	PA02
TOUCH RESET#	P711
TOUCH IRQ	P001
LCD Backlight Enable	P712

Table 27. LCD Port Assignments

LCD Signal Description	LCD ZIF Connector (J28) Pin	LCD ZIF Connector Pin Name	DK-S7G2 Port	Pi Filter	Bridge Resistor
LEDK	1	LEDK	-	-	-
LEDA	2	LEDA	-	-	-
GND	3	GND	-	-	-
+3.3 V	4	VCC	-	-	-
DATA13	5	R0	P907	FL7	R40
DATA14	6	R1	P908	FL9	R42
DATA15	7	R2	P901	FL11	R44
DATA11	8	R3	P905	FL3	R35
DATA12	9	R4	P906	FL5	R37
DATA13	10	R5	P907	FL7	R40
DATA14	11	R6	P908	FL9	R42
DATA15	12	R7	P901	FL11	R44
DATA9	13	G0	PA08	FL6	R38
DATA10	14	G1	P615	FL8	R41
DATA5	15	G2	PA00	FL13	R46
DATA6	16	G3	PA01	FL15	R48
DATA7	17	G4	PA10	FL17	R50
DATA8	18	G5	PA09	FL4	R36
DATA9	19	G6	PA08	FL6	R38
DATA10	20	G7	P615	FL8	R41
DATA2	21	B0	P802	FL14	R47
DATA3	22	B1	P606	FL16	R49
DATA4	23	B2	P607	FL18	R51
DATA0	24	B3	P804	FL10	R43
DATA1	25	B4	P803	FL12	R45
DATA2	26	B5	P802	FL14	R47
DATA3	27	B6	P606	FL16	R49
DATA4	28	B7	P607	FL18	R51
GND	29	GND	-	-	-
CLK	30	CLK	P900	FL19	R52
ON	31	DISP	P710	FL20	R53
HSYNC	32	HS	P314	FL21	R54
VSYNC	33	VS	P313	FL22	R55
DE	34	DEN	P315	FL23	R57
N.C.	35	N.C.	-	-	-
GND	36	GND	-	-	-
TOUCH XR	37	XR	-	-	-
TOUCH YB	38	YB	-	-	-
TOUCH XL	39	XL	-	-	-
TOUCH YT	40	YT	-	-	-

Figure 21. On-board LCD Module

5.4.22 External LCD Connector

In addition to the on-board LCD, DK-S7G2 provides an expansion connector for the use of an external LCD module. The External LCD interface supports a 16-bit LCD data bus, control signals, and I^2C bus to interface with a touch controller. The external LCD interface uses the same MCU ports for the LCD data bus as the on-board LCD.

A digital bus switch (U37) is provided to isolate the LCD signals from the rest of the system. To enable the external LCD, set DIP switch S9-4 to ON. When the external LCD is enabled, LED7 is illuminated.

The connector interface includes an LCD_PRESENT signal (J29 pin 2), which has a weak pull-down on DK-S7G2. The LCD_PRESENT signal is connected to the Board Configuration I2C Bus Expander (U40) and indicates to the MCU that an external LCD is installed. This signal should be pulled high (+3.3 V) by the external LCD module.

Figure 22. External LCD Connector

Table 28. External LCD Connector Port Assignments

LCD Signal Description	External LCD Connector (J29) Pin	DK-S7G2 Port
+3.3V	1	-
LCD Present	2	-
+3.3V	3	-
GND	4	-
GND	5	-
DATA0	6	P804
DATA1	7	P803
DATA2	8	P802
DATA3	9	P606
DATA4	10	P607
DATA5	11	PA00
GND	12	-
DATA6	13	PA01
DATA7	14	PA10
DATA8	15	PA09
DATA9	16	PA08
DATA10	17	P615
DATA11	18	P905
DATA12	19	P906
DATA13	20	P907
DATA14	21	P908
DATA15	22	P901
TOUCH RESET#	23	P711
NC	24	-
GND	25	-
DE	26	P315
HSYNC	27	P314
VSYNC	28	P313
GND	29	-
CLK	30	P900
GND	31	-
+5V	32	-
+5V	33	-
+5V	34	-
ON	35	P710
I2C SDA	36	PA02
I2C SCL	37	PA03
IRQ	38	P001
Backlight Enable	39	P712
LCD RESET#	40	P713

5.4.23 User Potentiometer

DK-S7G2 includes a 10 kΩ single-turn potentiometer (R16) connected to the Analog-to-Digital Converter (ADC) peripheral on the S7G2 MCU. This device is connected to P000 using the AN000 function assignment.

To isolate the User Potentiometer from P000, remove the jumper from J11.

Figure 23. User Potentiometer

5.4.24 Kit Data Serial EEPROM

DK-S7G2 includes a 64 Kb I²C serial EEPROM (U43), which stores basic information about the DK-S7G2. This device is programmed at the factory and is write protected. This device may be accessed either through the MCU or through the breakout pin headers to retrieve the basic kit information. The 7-bit I²C address is 0x50 for this device.

Figure 24. Kit Data Serial EEPROM

5.5 Breakout Pin Headers

The DK-S7G2 pin headers, J5, J6, J7 and J8, provide access to all Main MCU interface signals, and to voltages for all Main MCU power ports as seen in Figure 16. Each pin is labeled with the voltage or port connected to that pin.

5.6 Configuration

5.6.1 Function select DIP switches

Most pins of the Synergy S7G2 microcontroller support multiple functions and can therefore be connected to more than one device or connector on the DK-S7G2 board. To make it easy and safe to connect important functions, especially those with wide data bus connections, the DK-S7G2 provides banks of DIP switches S6, S7, S8, and S9.

Each DIP switch controls a high-speed buffer which, when the switch is in the ON position, connects the signal lines between the microcontroller and the on-board device or connector. When the switch is in the OFF position, the microcontroller pins are isolated from the respective connector or device and can be used for another board function.

When the DIP switches are in the OFF position, software can dynamically enable the respective peripherals at system initialization through an I/O expander. The I/O expander is controlled through software through an I^2C port connected to the SCI channel 7 on the S7G2 microcontroller and performs the following functions:

- Sense the position of the DIP switch.
- Generate the enable signal for the buffer.
- Control an LED.

Through the I/O expander's I^2C port, software can read the position of the DIP switch and, if the DIP switch is open, enable the buffers to connect the device to the microcontroller pins.

The selection DIP switches enable peripheral functions as shown in the following table.

Table 29. Selection DIP Switch Functions

Location	Default Setting	Function	Notes
S6-1	OFF	Boot Mode (MD) Select	OFF = Normal Boot mode ON = Serial Boot mode
S6-2	OFF	Ethernet 0 Enable	
S6-3	OFF	Ethernet 1 Enable	
S6-4	OFF	e.MMC Enable	
S7-1	OFF	PMOD A Enable	
S7-2	ON	JTAG Enable	
S7-3	OFF	Serial Port (RS232/485) Enable	
S7-4	OFF	CAN Enable	
S8-1	OFF	PMOD B Enable	
S8-2	OFF	Camera Module Enable	
S8-3	OFF	SD Card Enable	
S8-4	ON	On-board LCD Enable	
S9-1	OFF	QSPI Flash Enable	
S9-2	OFF	SDRAM Enable	
S9-3	OFF	User Push-buttons Enable	
S9-4	OFF	External LCD Enable	

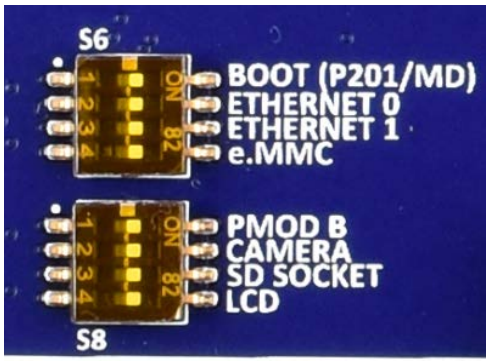


Figure 25. Function Select DIP Switches S6 and S8

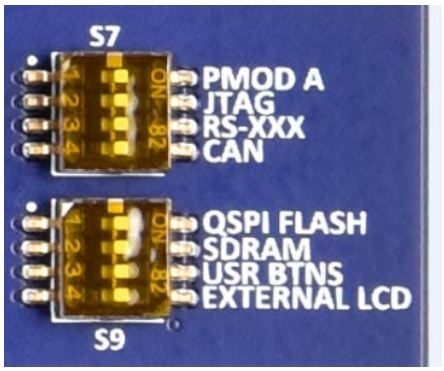


Figure 26. Function Select DIP Switches S7 and S9

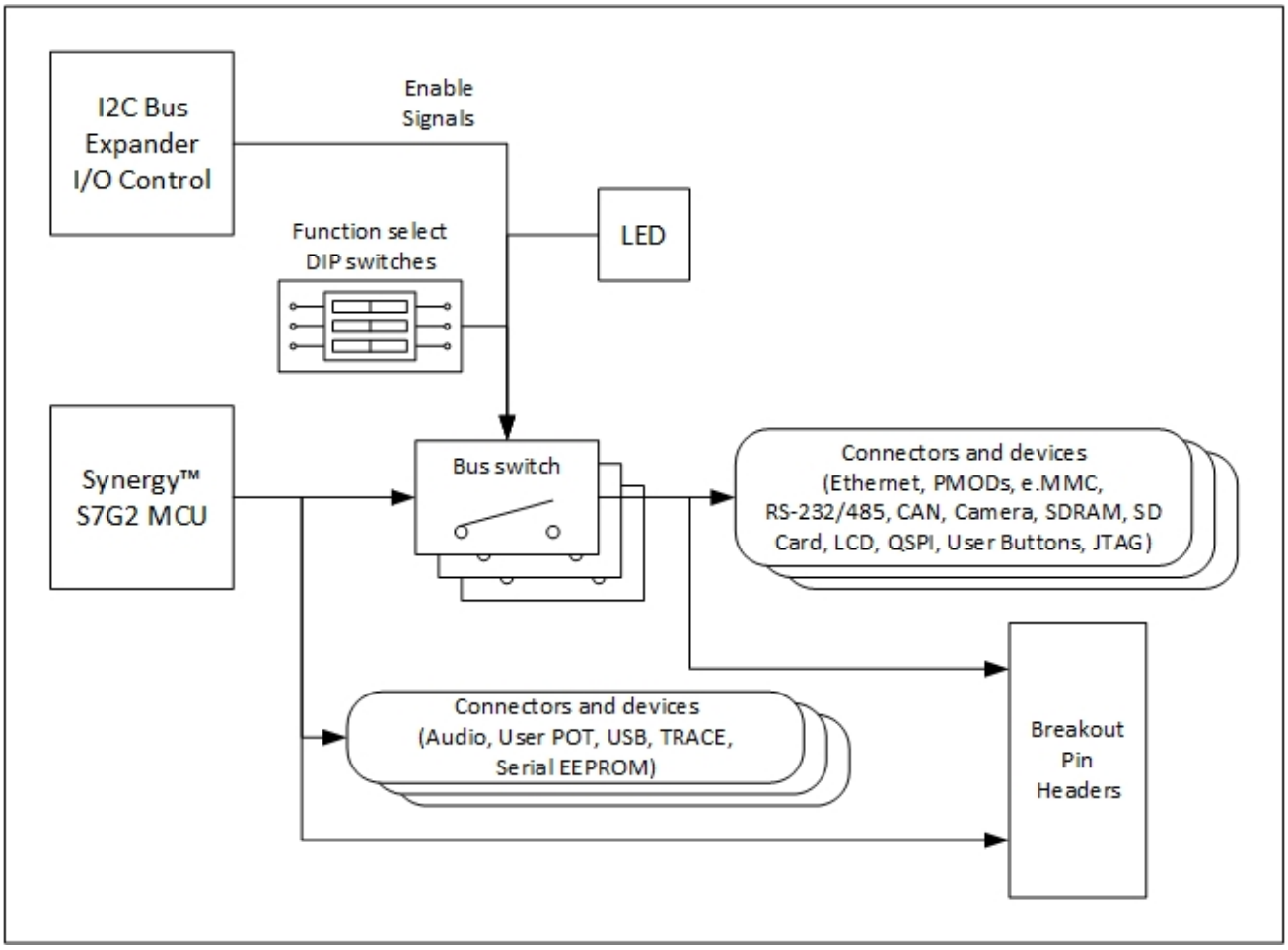


Figure 27. Function Selection

5.6.2 Ethernet 0 Multiplexing

Ethernet 0 is multiplexed with Audio Jack, SD Card, e.MMC, and Breakout Pin Headers.

To enable Ethernet 0, set S6-2 to ON. The selection DIP switches for the SD Card and e.MMC do not matter when Ethernet 0 is enabled. With Ethernet 0 enabled, the other multiplexed functions are not available.

To disable Ethernet 0 and enable the other multiplexed functions, set S6-2 to OFF. To enable the SD Card, set S8-3 to ON. To enable the e.MMC, set S6-4 to ON. With Ethernet 0 disabled, Audio Jack is automatically enabled, and the multiplexed ports are available at the Breakout Pin Headers.

Note: SD Card and e.MMC use the same MCU ports. SD Card and e.MMC cannot be used at the same time.

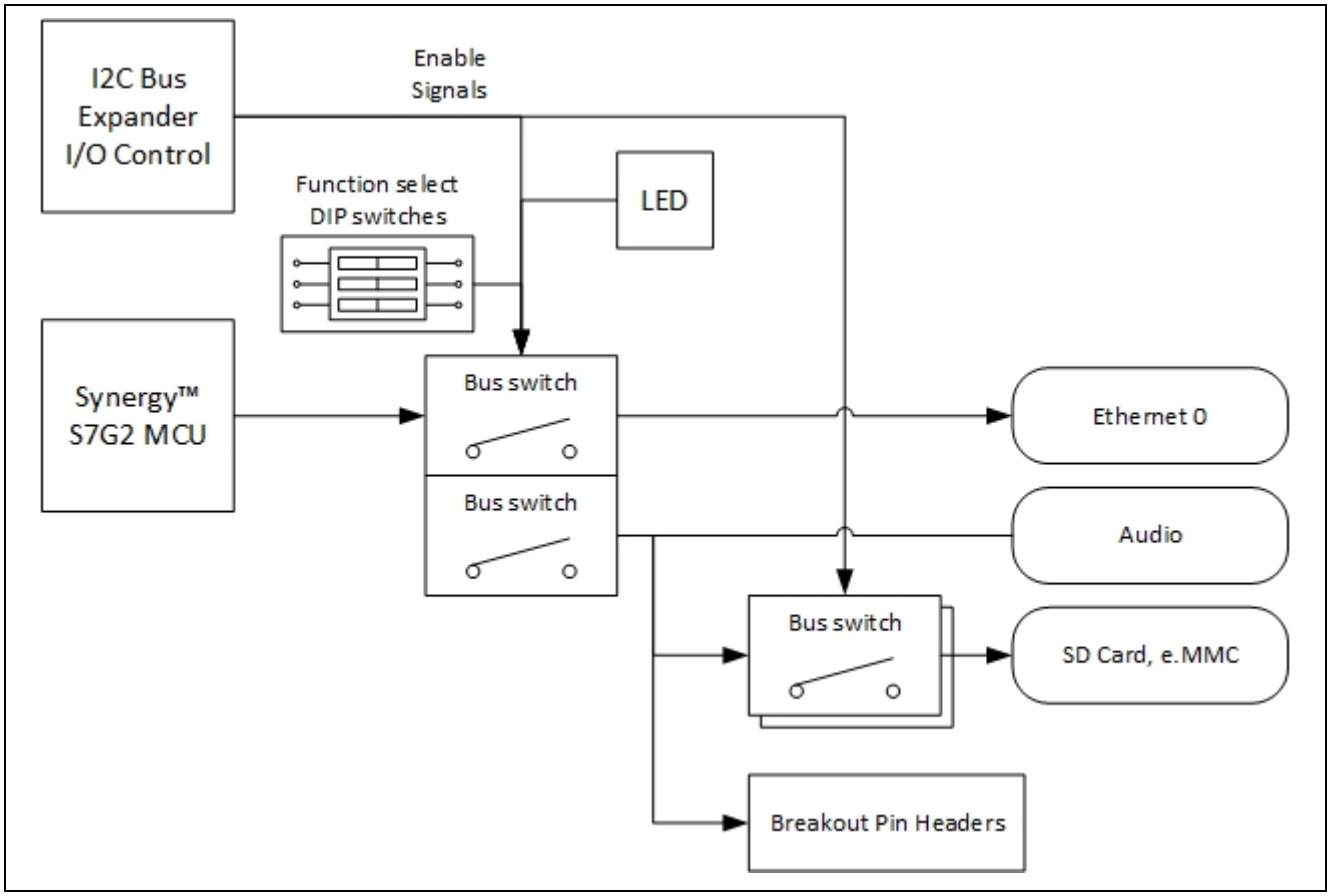


Figure 28. Ethernet 0 Multiplexing

5.6.3 Ethernet 1 Multiplexing

Ethernet 1 is multiplexed with the Camera Module and some ports on the Breakout Pin Headers.

To enable Ethernet 1, set S6-3 to ON and S8-2 to OFF. This also enables the multiplexed ports that are routed to the Breakout Pin Headers.

To enable the Camera Module, Ethernet 1 must be enabled. Set S6-3 to ON and S8-2 to ON. To avoid signal conflicts, do not use Ethernet 1 and the Camera Module at the same time.

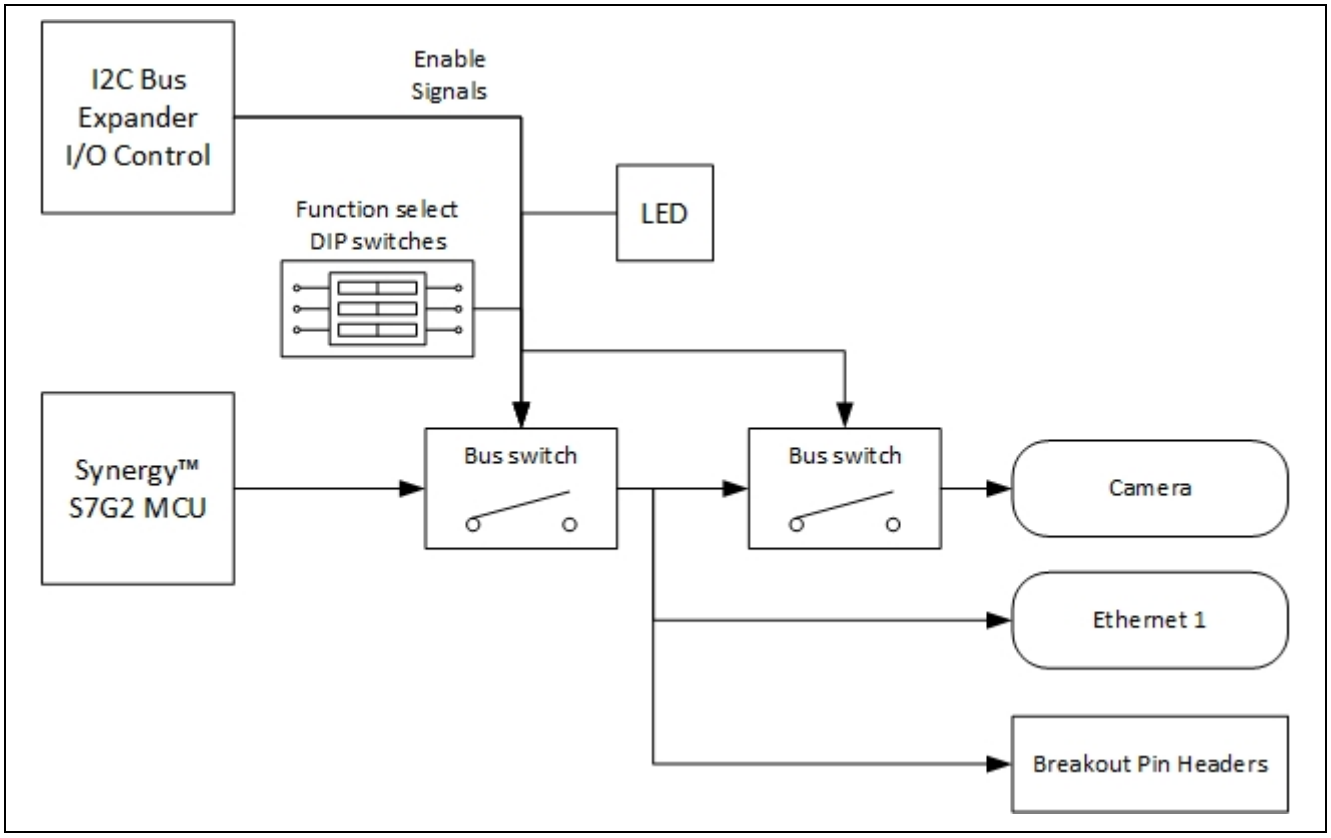


Figure 29. Ethernet 1 Multiplexing

5.6.4 LCD Multiplexing

Ports used for the on-board LCD are shared with the external LCD, and some LCD ports are multiplexed with the e.MMC. These shared and multiplexed signals are always available at the Breakout Pin Headers.

To enable the on-board LCD, set S8-4 to ON, S9-4 to OFF, and S6-4 to OFF.

To enable the external LCD, set S8-4 to OFF, S9-4 to ON, and S6-4 to OFF.

To enable the e.MMC, set S8-4 to OFF, S9-4 to OFF, and S6-4 to ON.

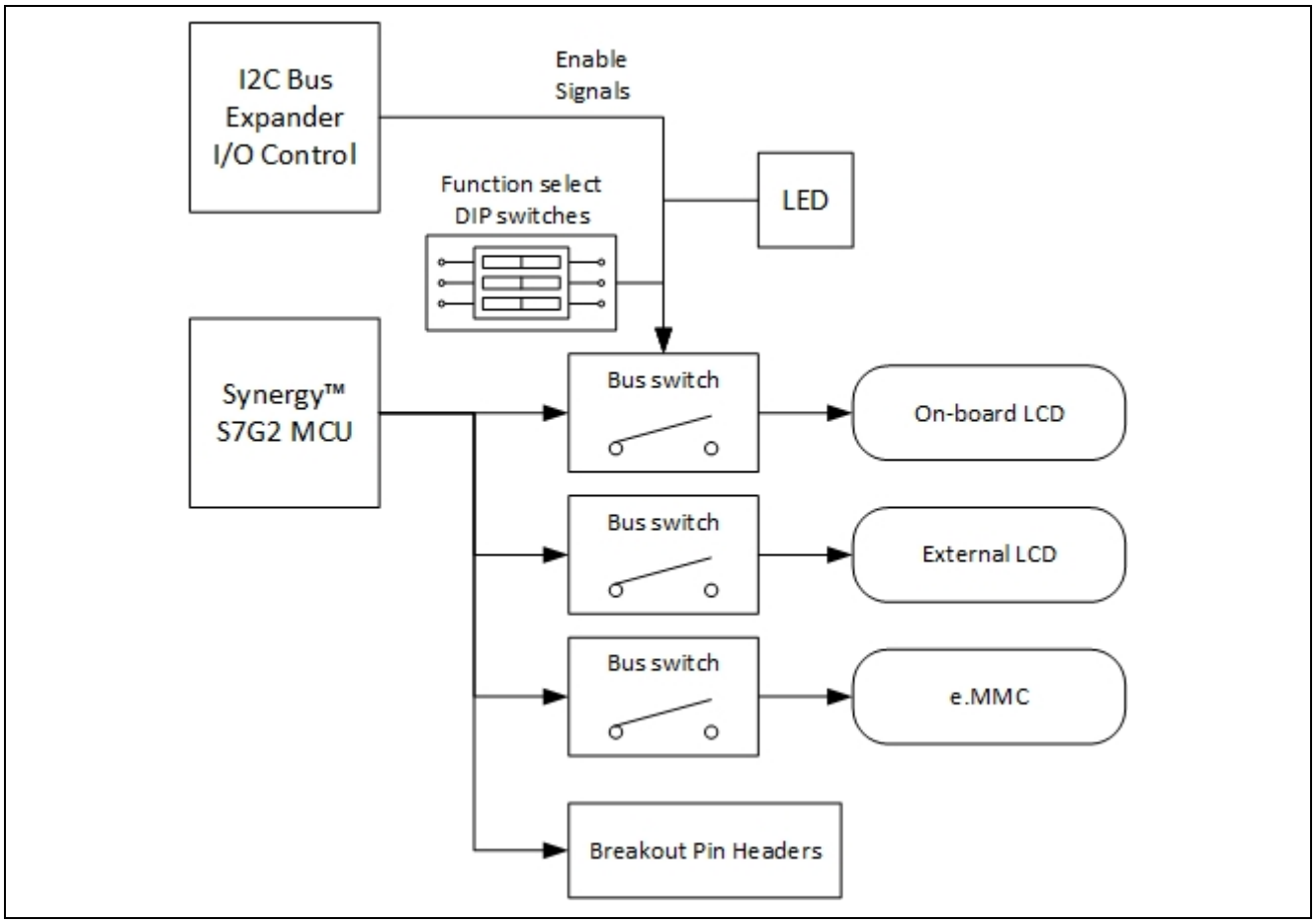


Figure 30. LCD Multiplexing

5.6.5 SDRAM Multiplexing

Ports used for the SDRAM are multiplexed with PMOD C, PMOD D, and some ports on the Breakout Pin Headers.

To enable the SDRAM and disable the other multiplexed functions, set S9-2 to ON.

To enable PMOD C, PMOD D, and the multiplexed ports on the Breakout Pin Headers, first disable the SDRAM. To disable the SDRAM, set S9-2 to OFF. PMOD C, PMOD D, and the multiplexed ports on the Breakout Pin Headers will be available.

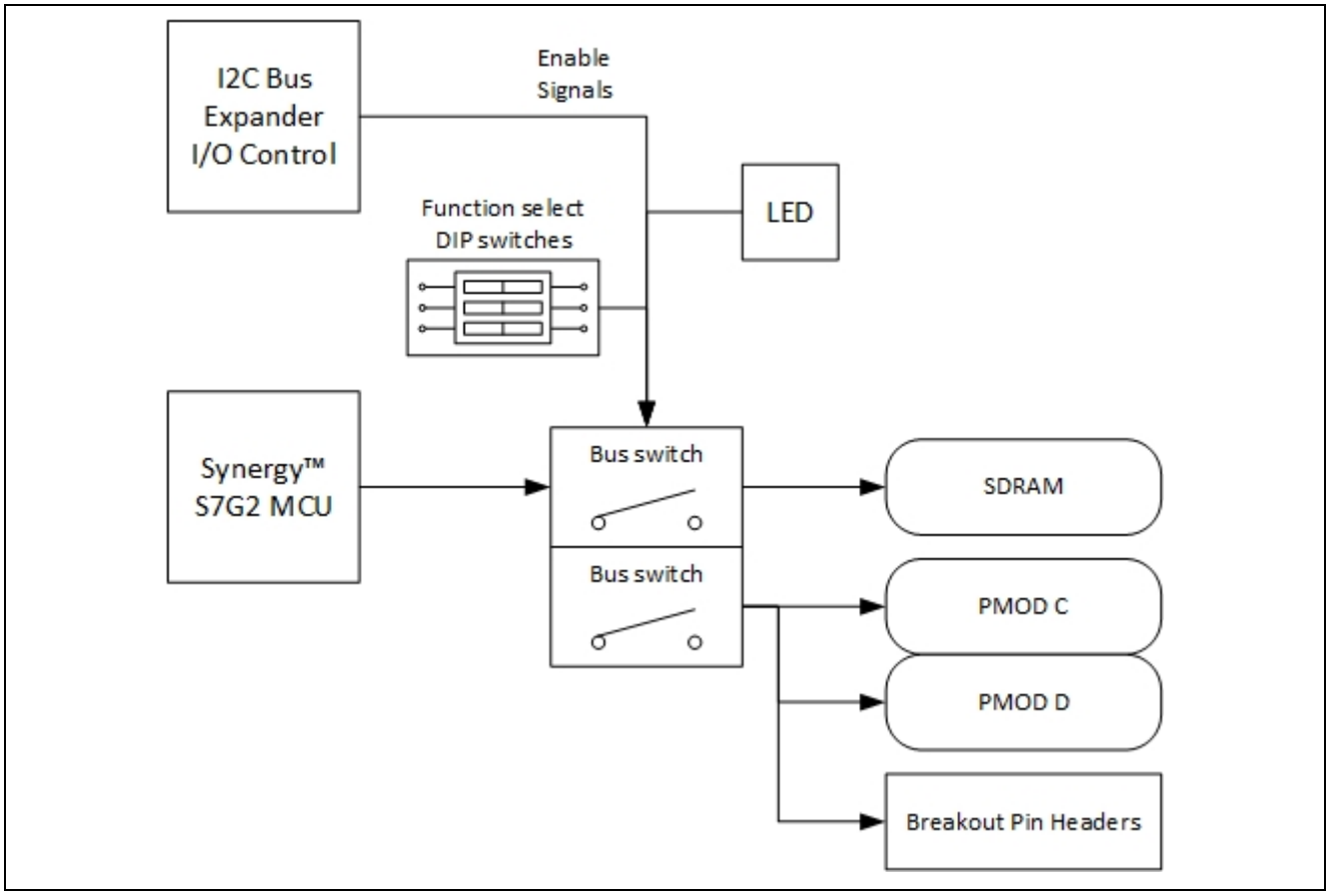
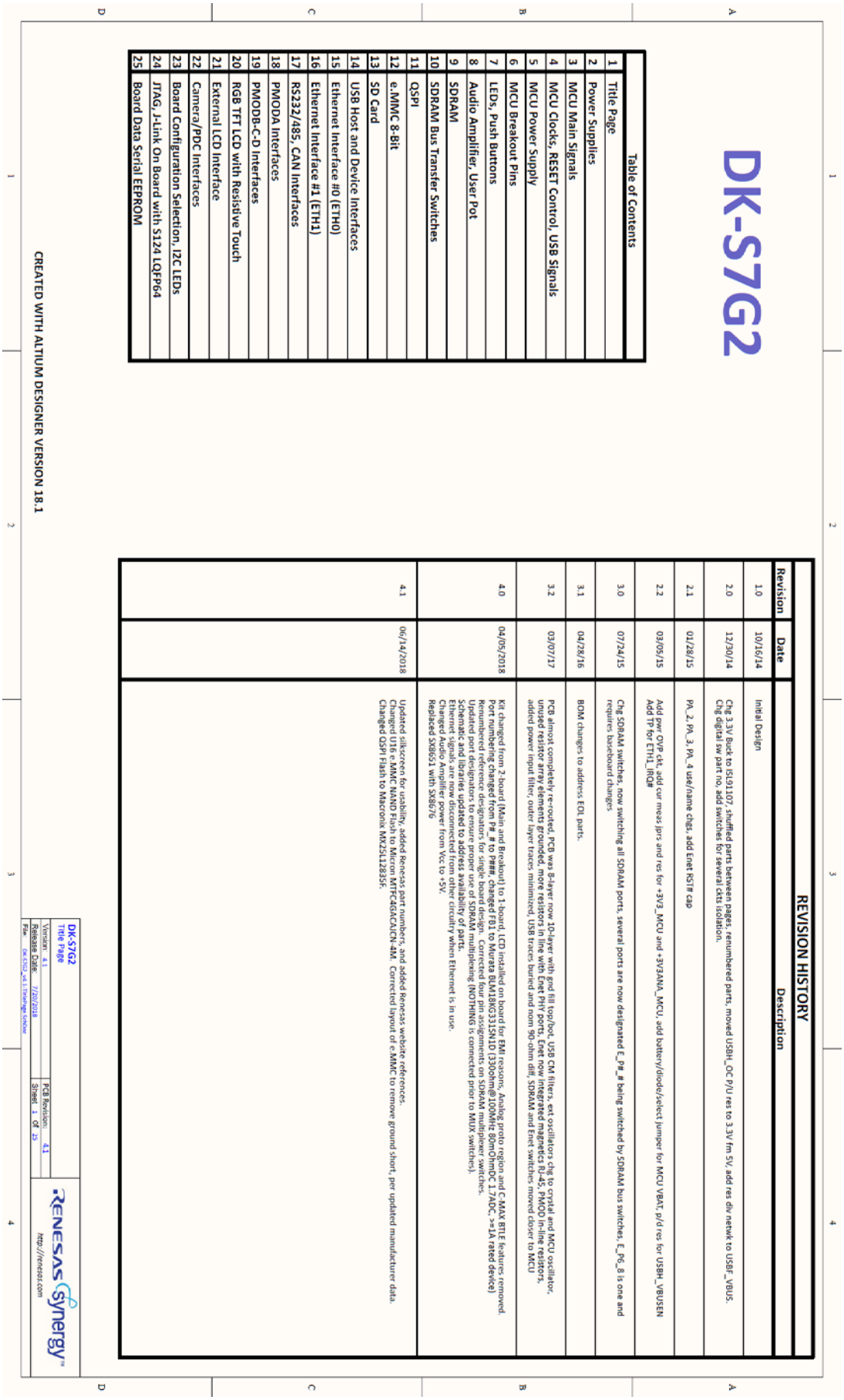
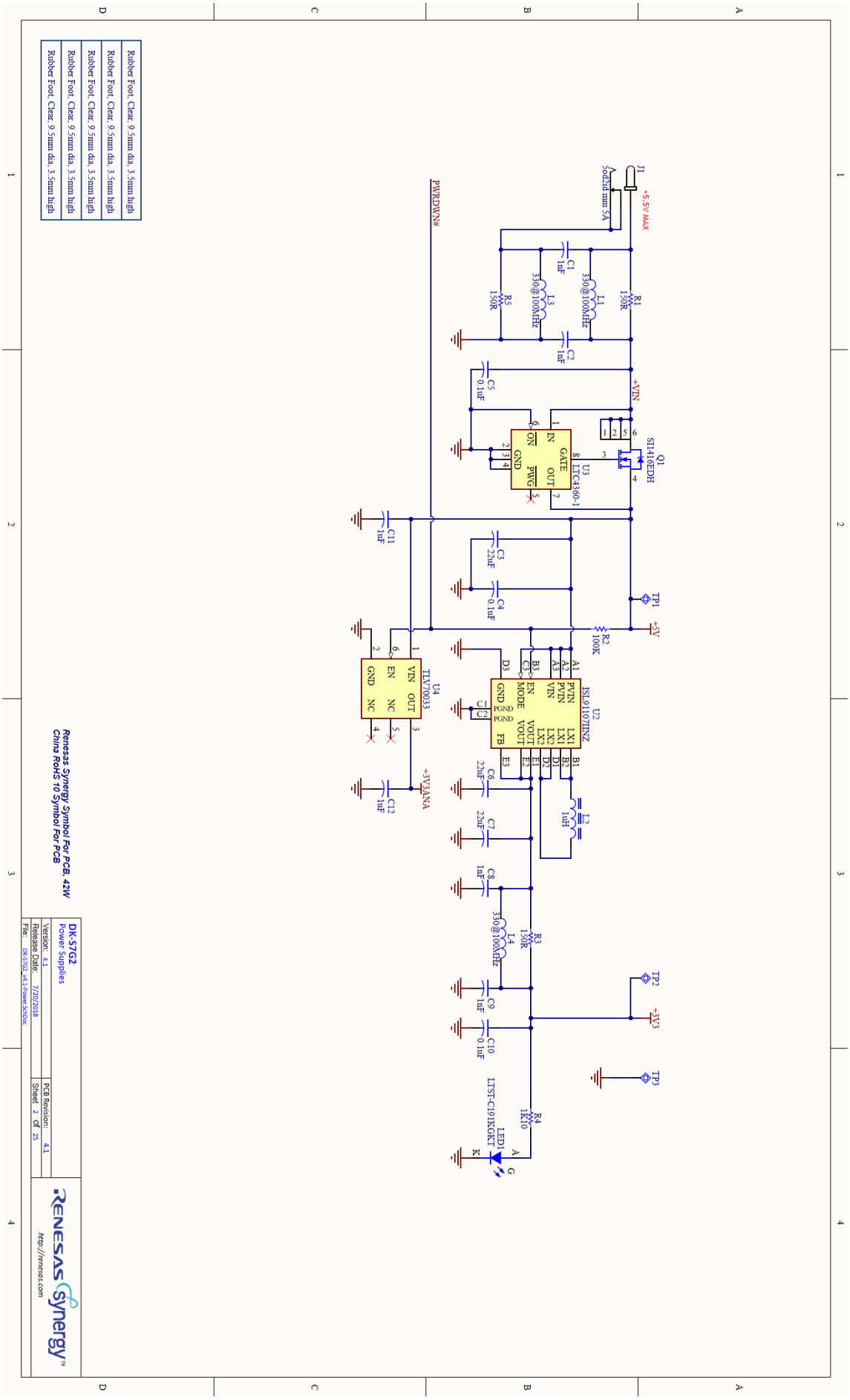


Figure 31. SDRAM Multiplexing

6. Electrical Schematics

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Rubber Foot, Clear, 9.5mm dia, 3.5mm high
Rubber Foot, Clear, 9.5mm dia, 3.5mm high
Rubber Foot, Clear, 9.5mm dia, 3.5mm high
Rubber Foot, Clear, 9.5mm dia, 3.5mm high
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+VIN
+5V
+3V3
+3V3ANA
Renesas Synergy Symbol For PCB, 42W
China RoHS 10 Symbol For PCB
DK-S7G2
Power Supplies
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Release Date: 7/30/2018
PCB Revision: 4.1
Sheet 2 of 25
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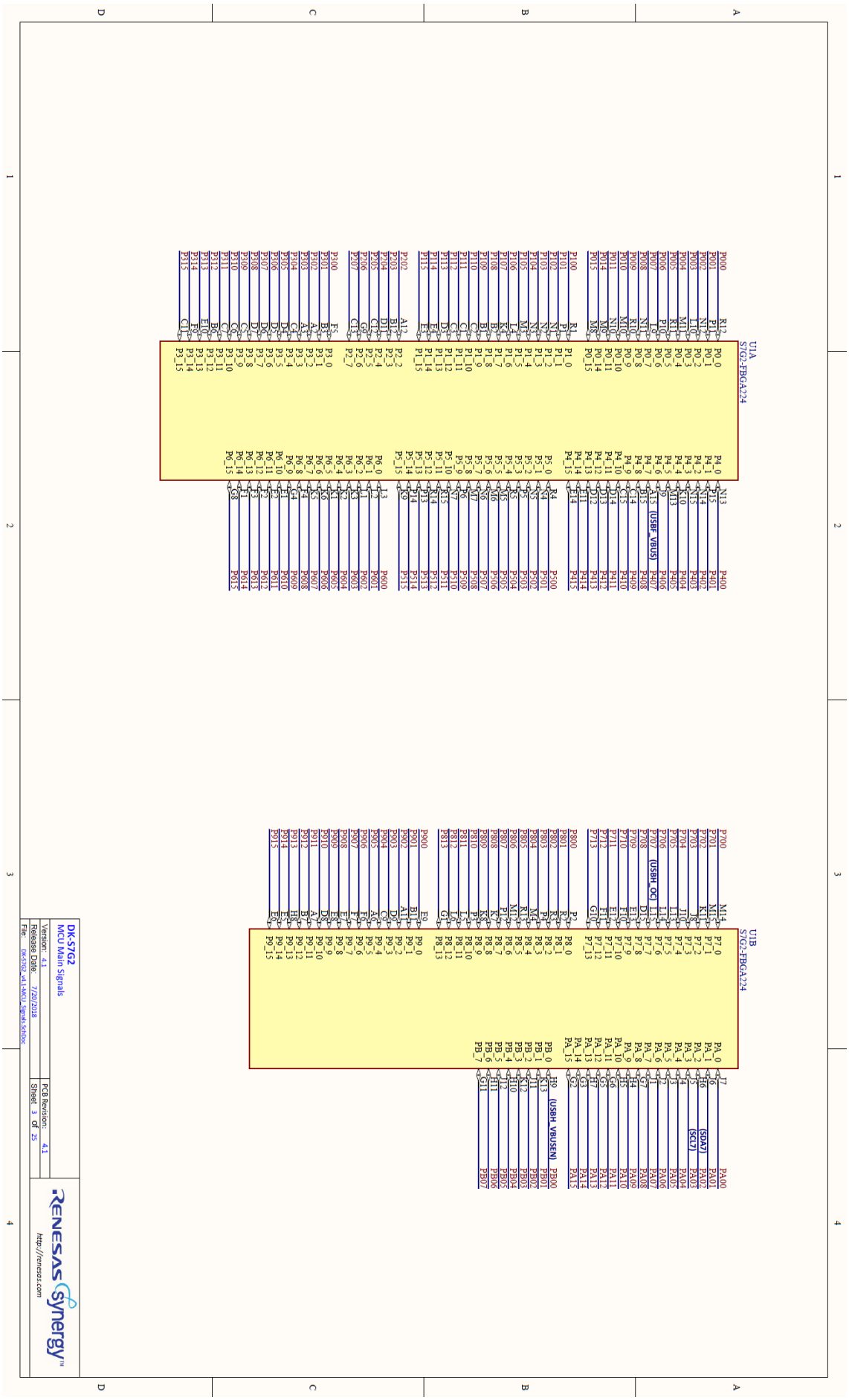
http://renesas.com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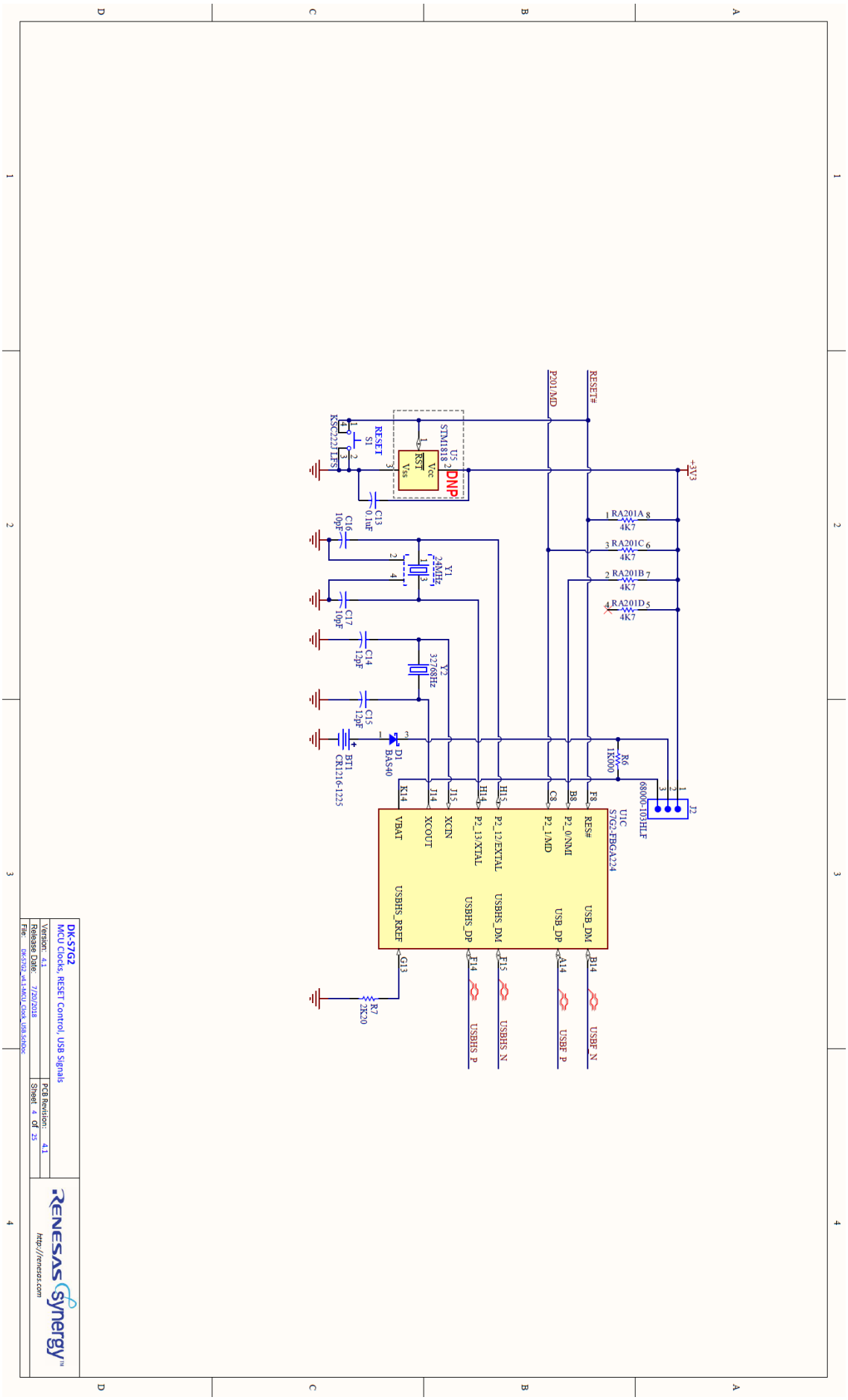
PCB Revision: 4.1
Sheet 3 of 25
RENESAS synergy™
http://renesas.com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MCU Clocks, RESET Control, USB Signals
Version: 4.1
Release Date: 7/20/2018
PCB Revision: 4.1
Sheet 4 of 25
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http://renesas.com
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KSC223J LFS
U5
STM1818
DNP
C13
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C16
10pF
C17
10pF
C14
12pF
C15
12pF
Y1
24MHz
Y2
32768Hz
BT1
CR1216-1225
D1
BAS40
RA201A 8
4K7
RA201C 6
4K7
RA201B 7
4K7
RA201D 5
4K7
R6
10K00
J2
68000-103HLF
U1C
S7G2-FBGA224
VBAT
XCOUT
XCIN
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P2_12/EXTAL
P2_1/MD
P2_0/NMI
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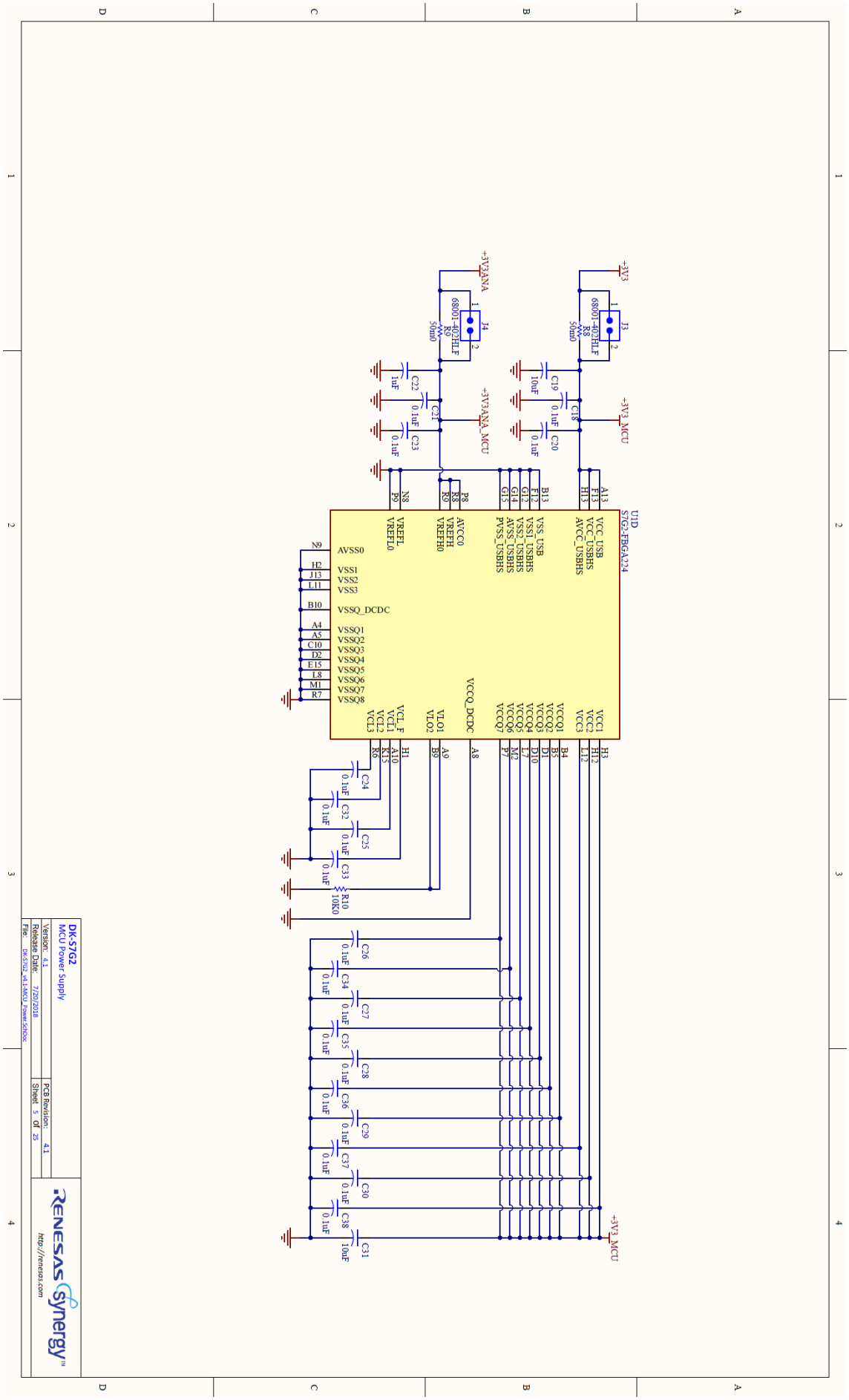
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MCU Power Supply
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PCB Revision: 4.1
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RENESAS Synergy
http://renesas.com
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+3V3ANA
+3V3_MCU
+3V3ANA_MCU
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J4
U1D
S7G2-FBGA224
AVSS0
VSS1
VSS2
VSS3
VSSQ_DCDC
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VREFL
VREFL0
AVCC0
VREFH
VREFH0
AVSS_USBHS
PVSS_USBHS
VSS_USB
VSS1_USBHS
VSS2_USBHS
VCC_USB
VCC_USBHS
AVCC_USBHS
VCL
VCL1
VCL2
VCL3
VCL_F
VLO1
VLO2
VCCQ_DCDC
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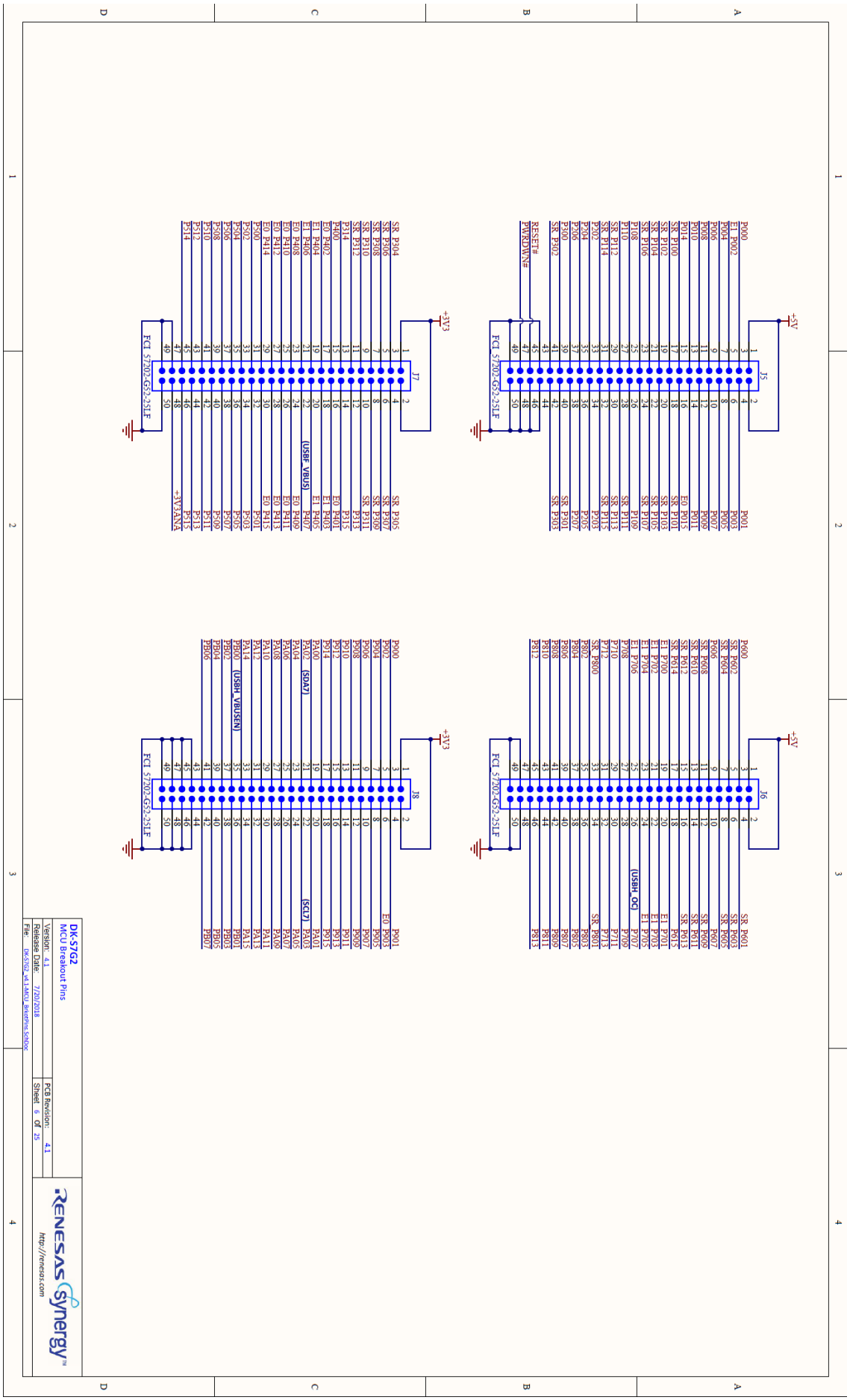
10KΩ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MCU Breakout Pins
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Release Date: 7/20/2018
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http://renesas.com
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J6
J7
J8
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+3V3
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PWRDWN#
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(USBH_VBUSEN)
(SDA7)
(SCL7)
-3V3ANA
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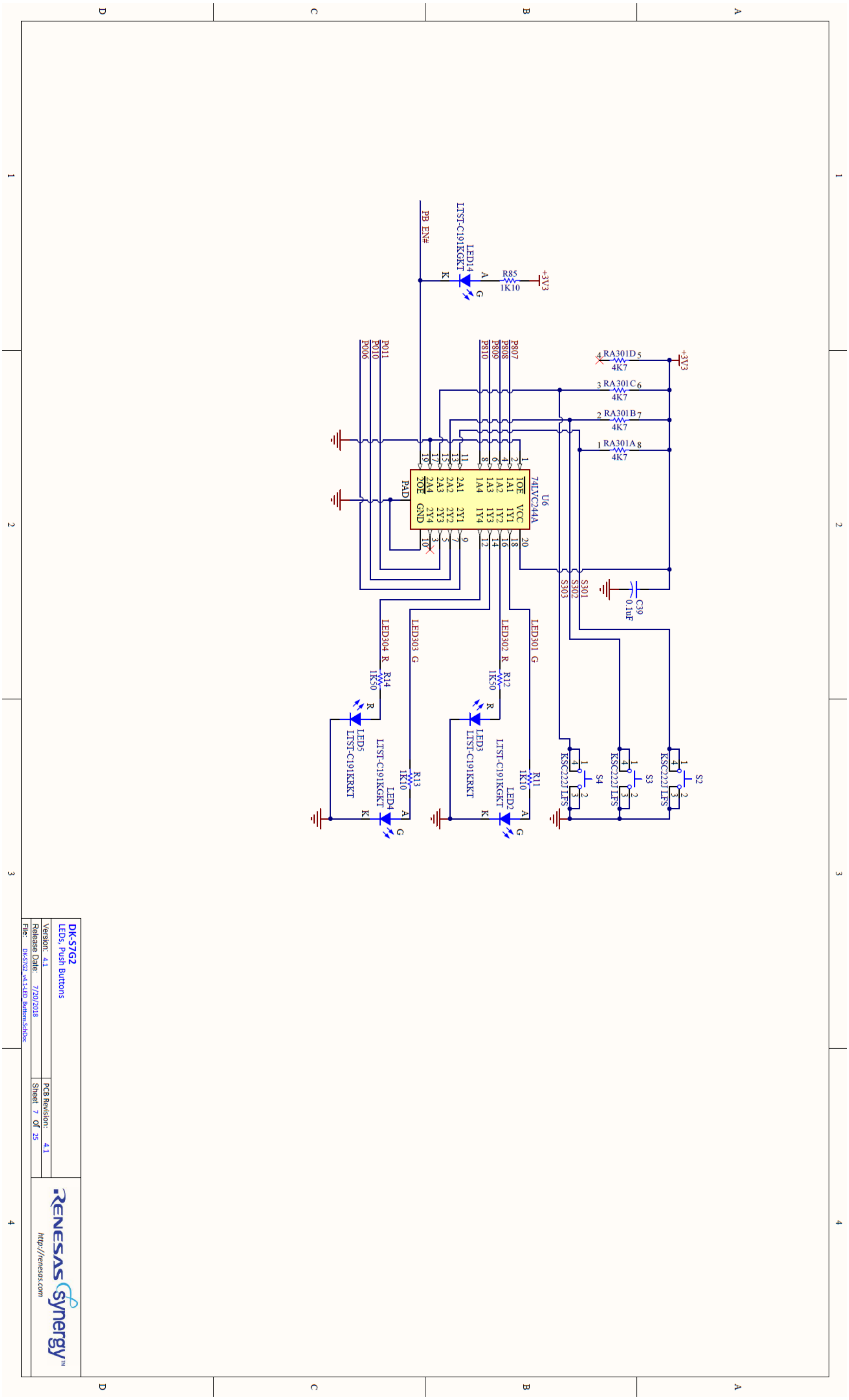
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LEDs, Push Buttons
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PCB Revision: 4.1
Release Date: 7/20/2018
Sheet 7 of 25
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http://renesas.com
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+3V3
RA301A
RA301B
RA301C
RA301D
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C39
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S301
S302
S303
LED301 G
LED302 R
LED303 G
LED304 R
R11
R12
R13
R14
1K50
LED2
LED3
LED4
LED5
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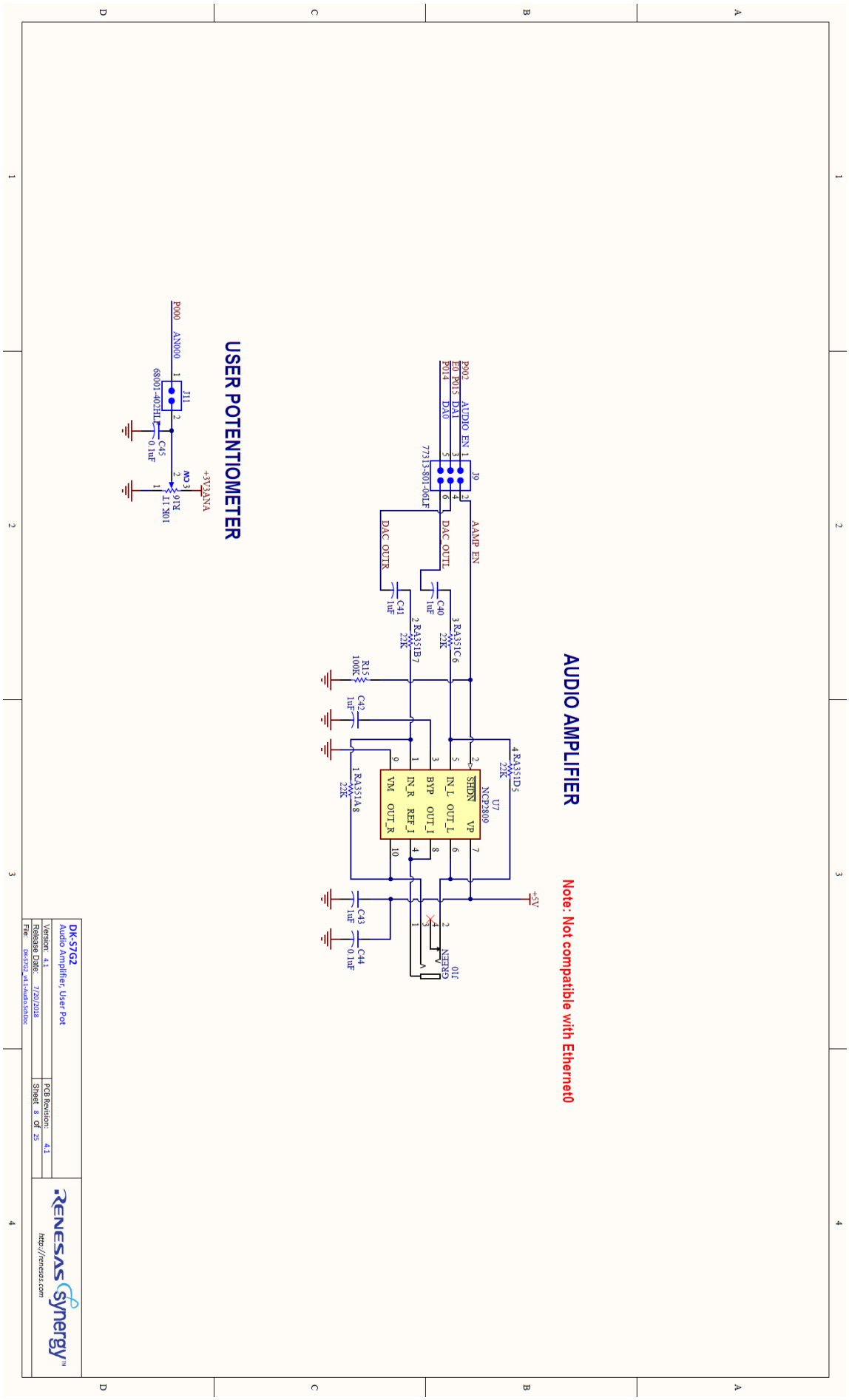
AUDIO AMPLIFIER
Note: Not compatible with Ethernet0
USER POTENTIOMETER
DK-S7G2
Audio Amplifier, User Pot
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Release Date: 7/20/2018
File: dk-s7g2_v4.1-audio.SchDoc
PCB Revision: 4.1
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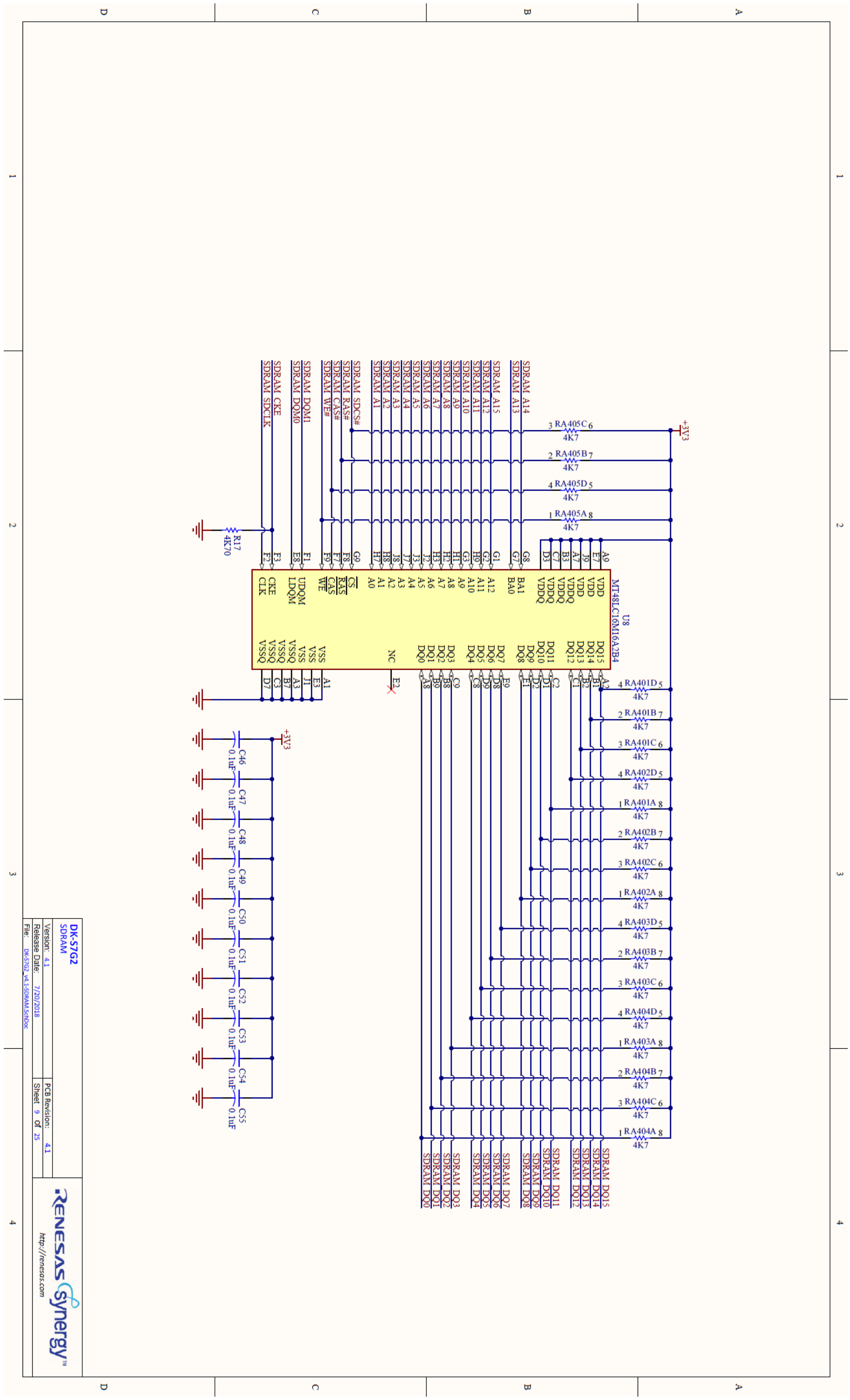
http://renesas.com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SDRAM
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PCB Revision: 4.1
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MT48LC16M16A2B4
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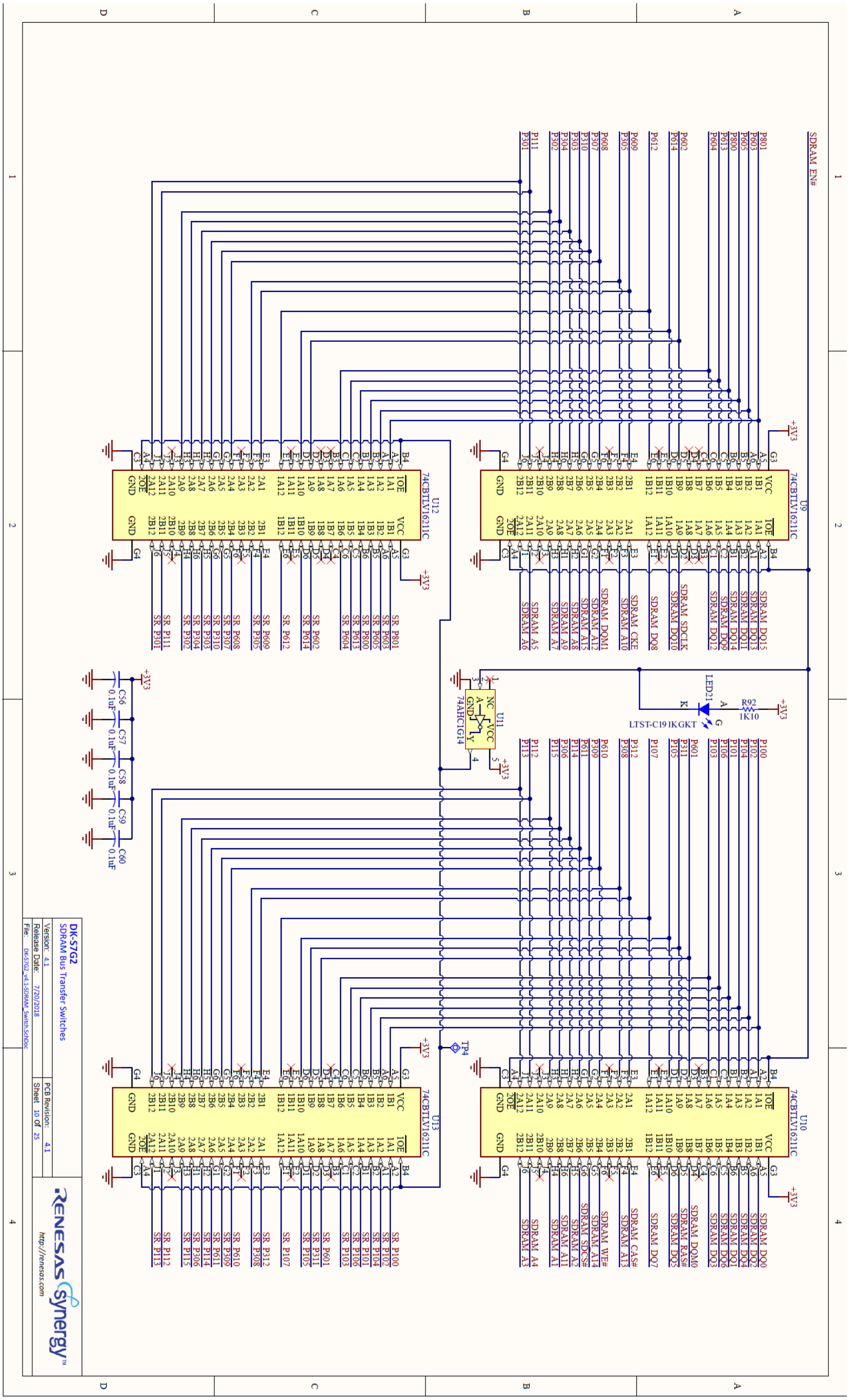
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PCB Revision: 4.1
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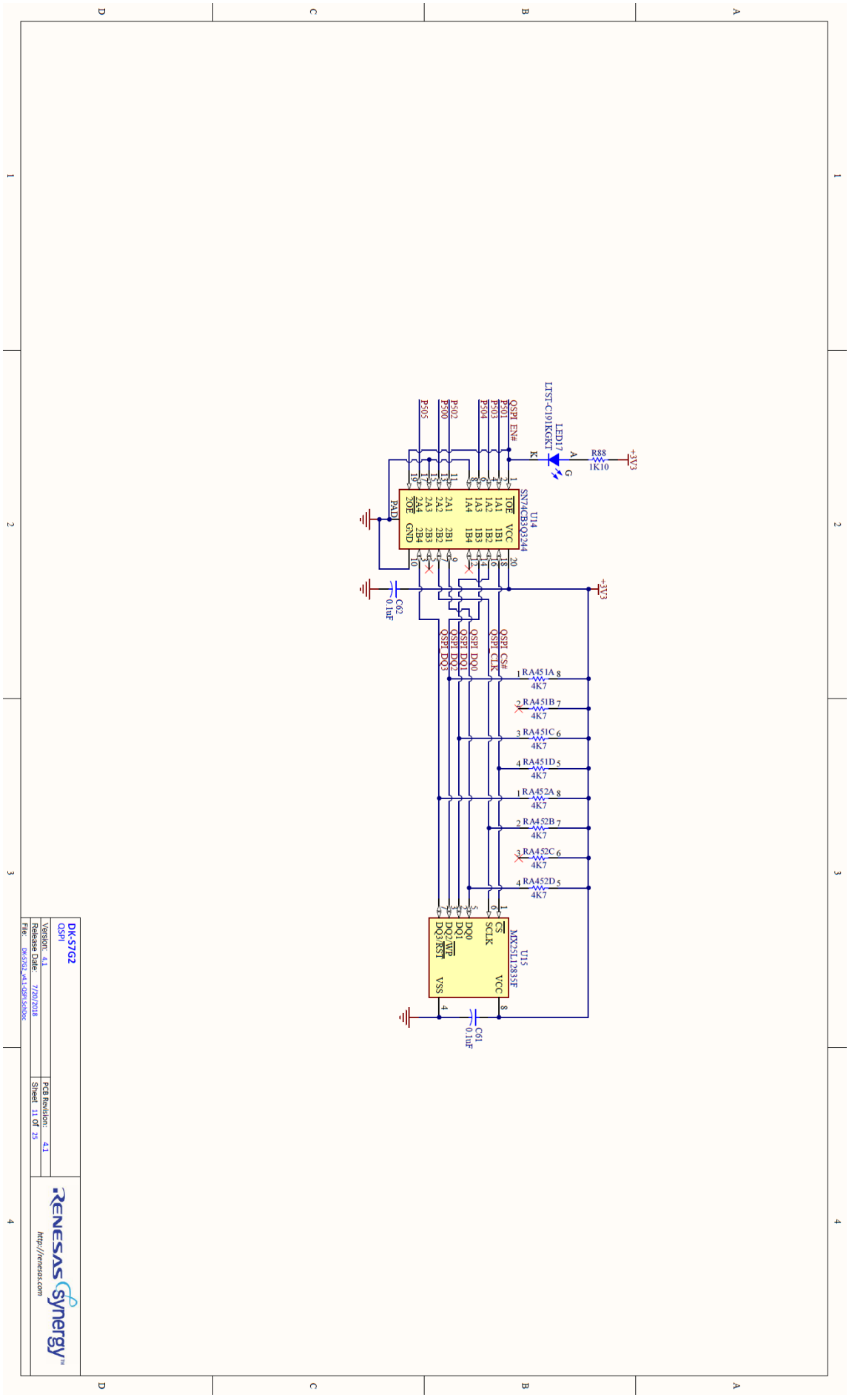
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P500
P506
P504
P503
P501
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U14
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C62
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QSPI_DQ2
QSPI_DQ1
QSPI_DQ0
QSPI_CS#
QSPI_CLK
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RA451B
RA451C
RA451D
RA452A
RA452B
RA452C
RA452D
4K7
MX25L12835F
U15
SCLK
VSS
C61
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Version: 4.1
Release Date: 7/20/2018
PCB Revision: 4.1
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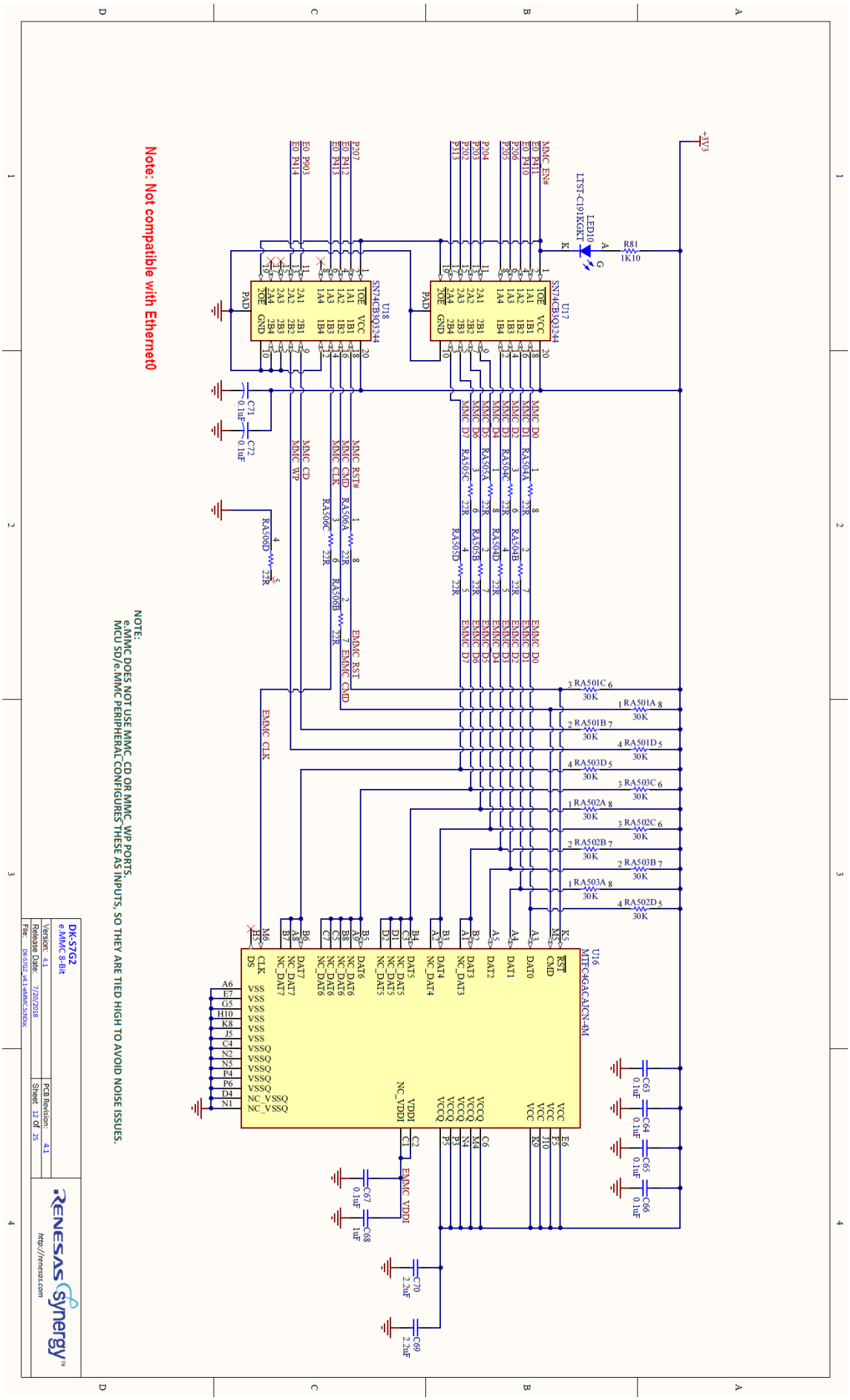
RENESAS synergy
http://renesas.com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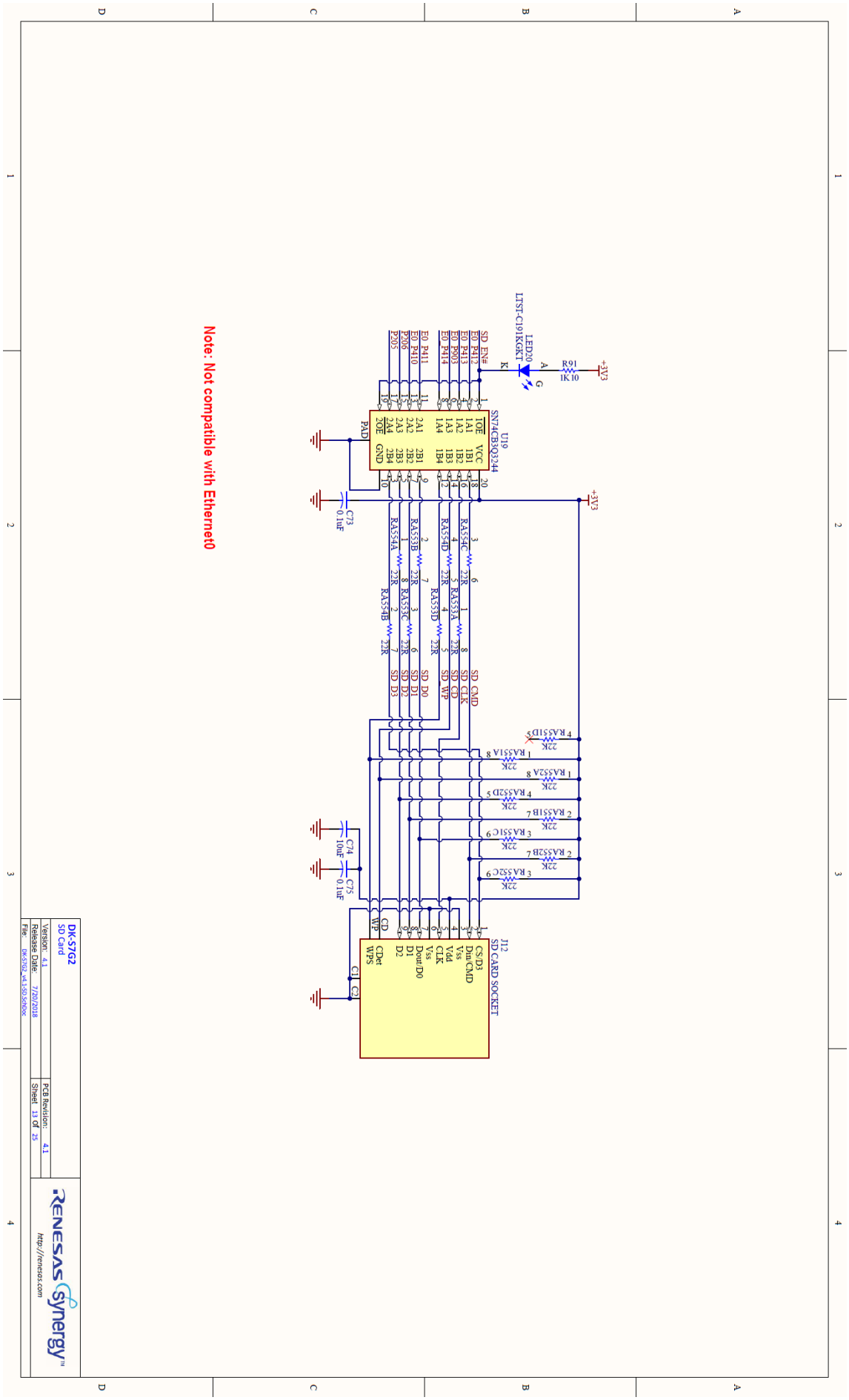
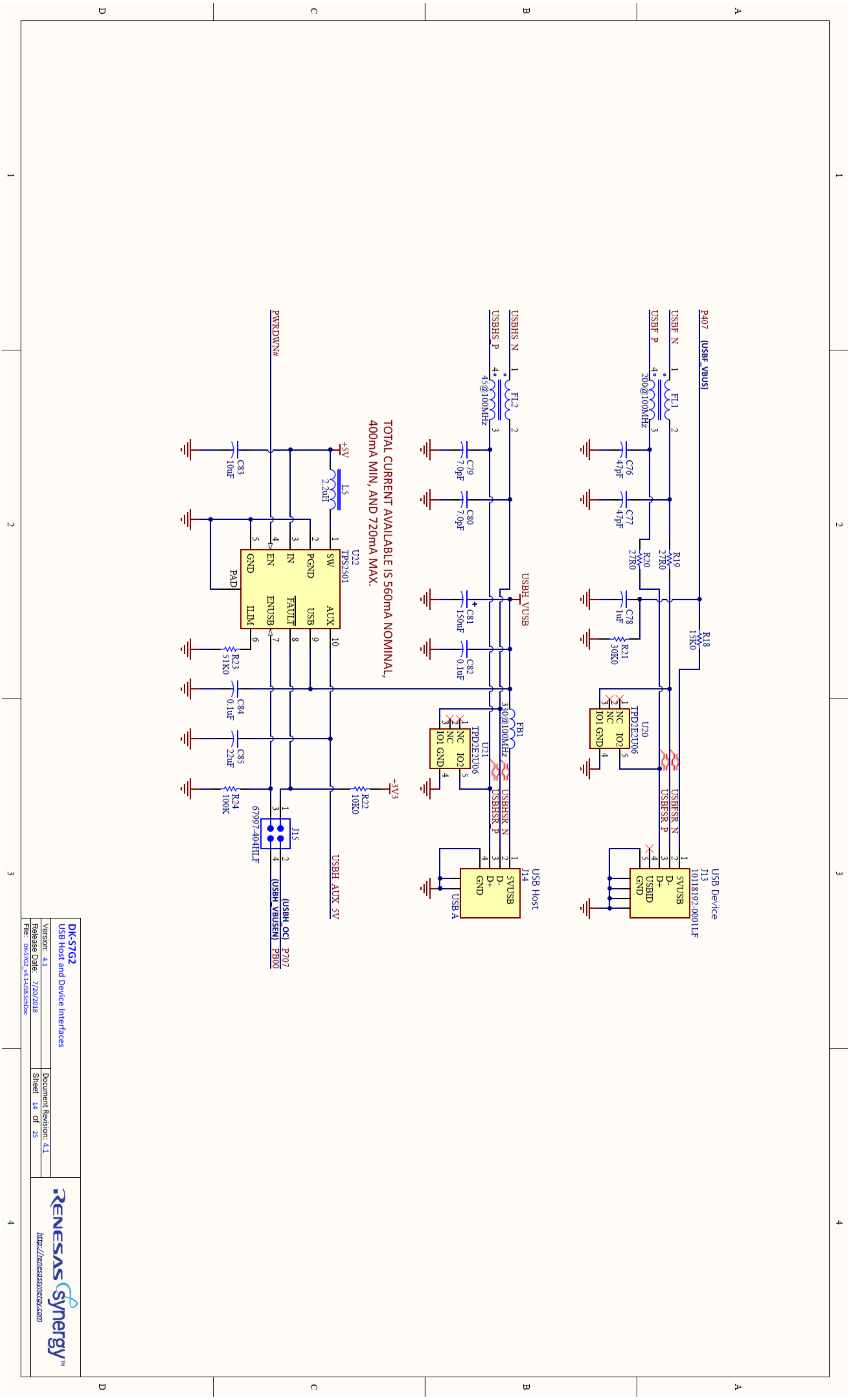
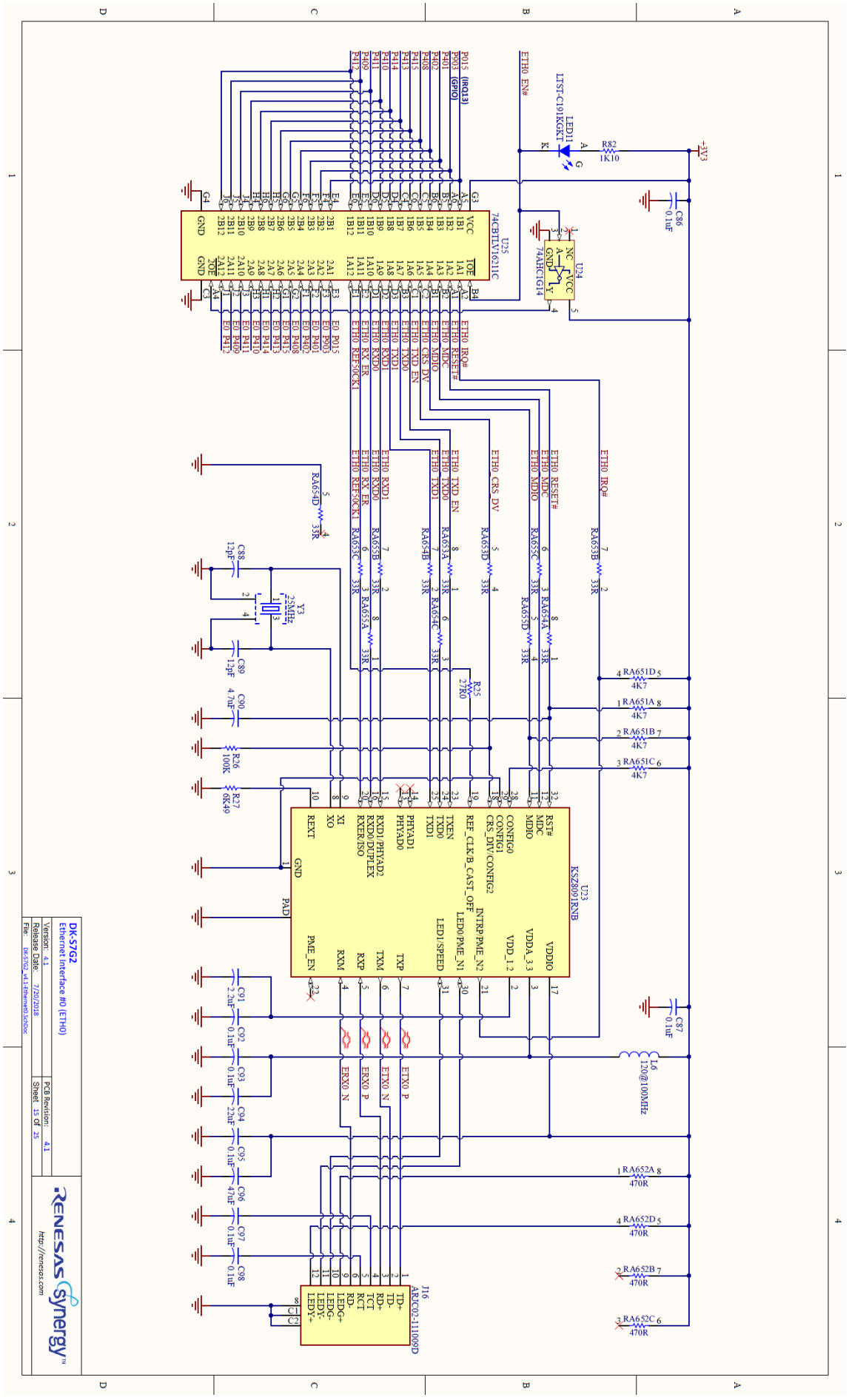
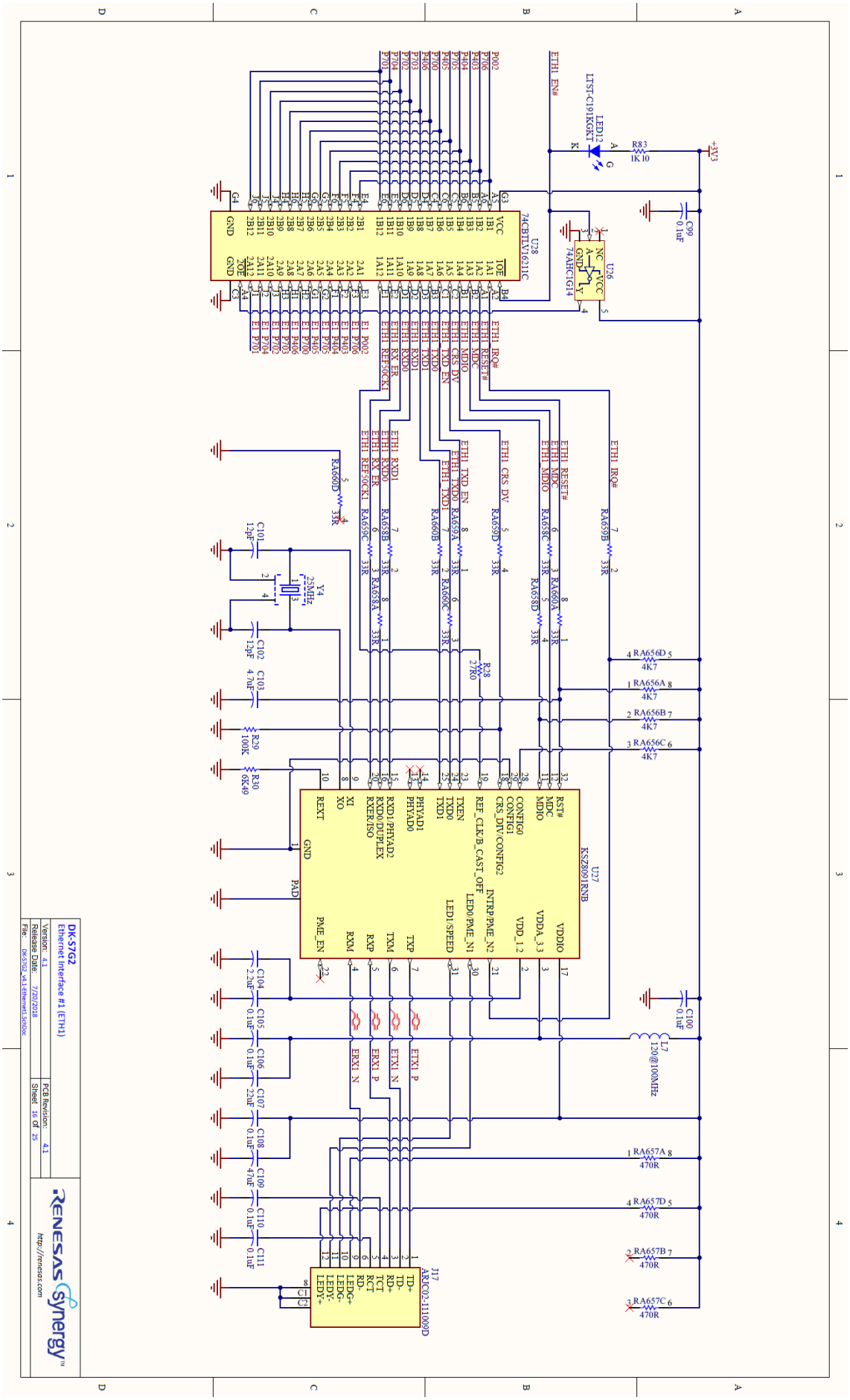
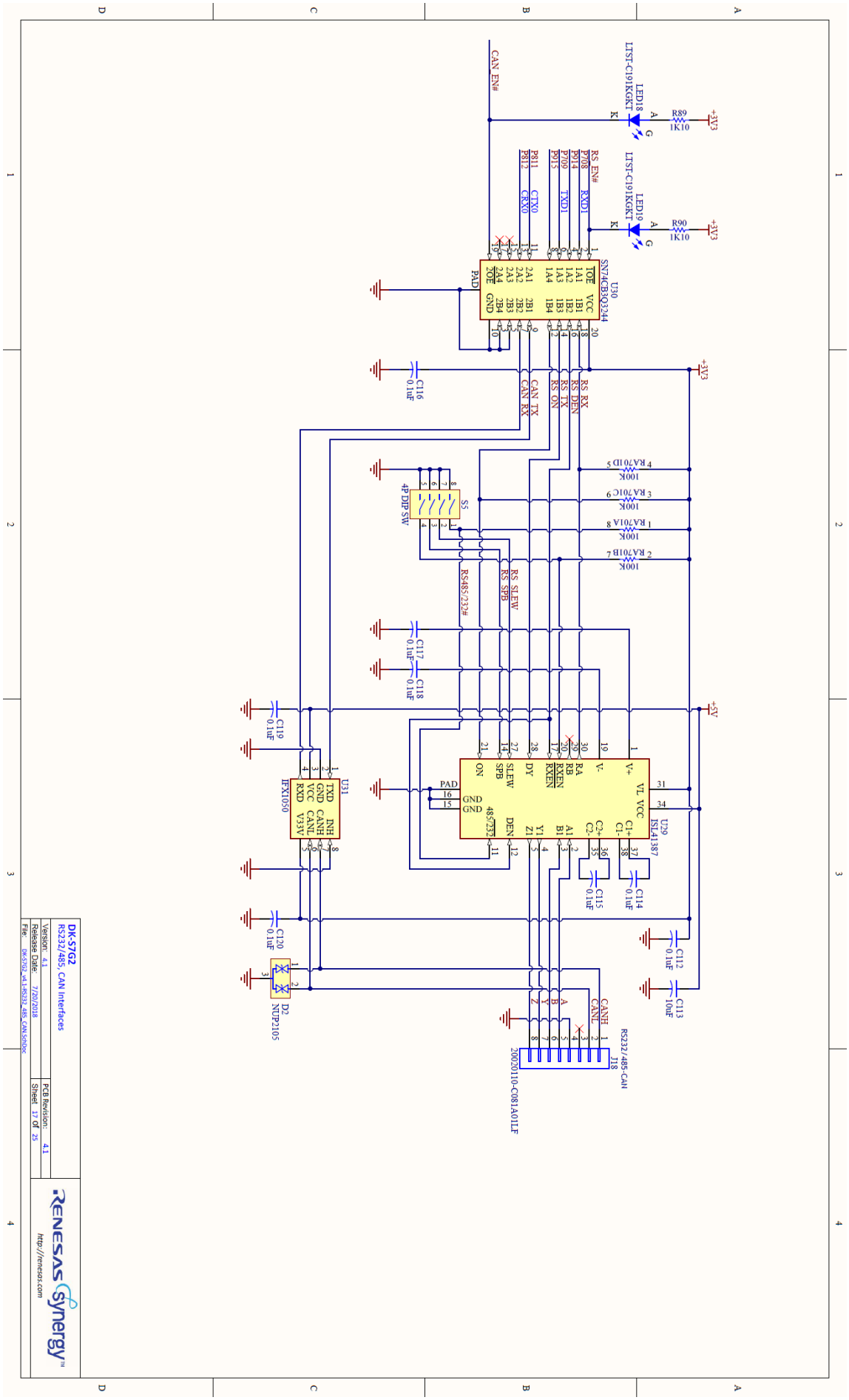
NOTE:
e.MMC DOES NOT USE MMC_CD OR MMC_WP PORTS.
MCU SD/e.MMC PERIPHERAL CONFIGURES THESE AS INPUTS, SO THEY ARE TIED HIGH TO AVOID NOISE ISSUES.
DK-S7G2
e.MMC 8-Bit
Version: 4.1
Release Date: 7/30/2018
PCB Revision: 4.1
Sheet 12 Of 25
http://renesas.com

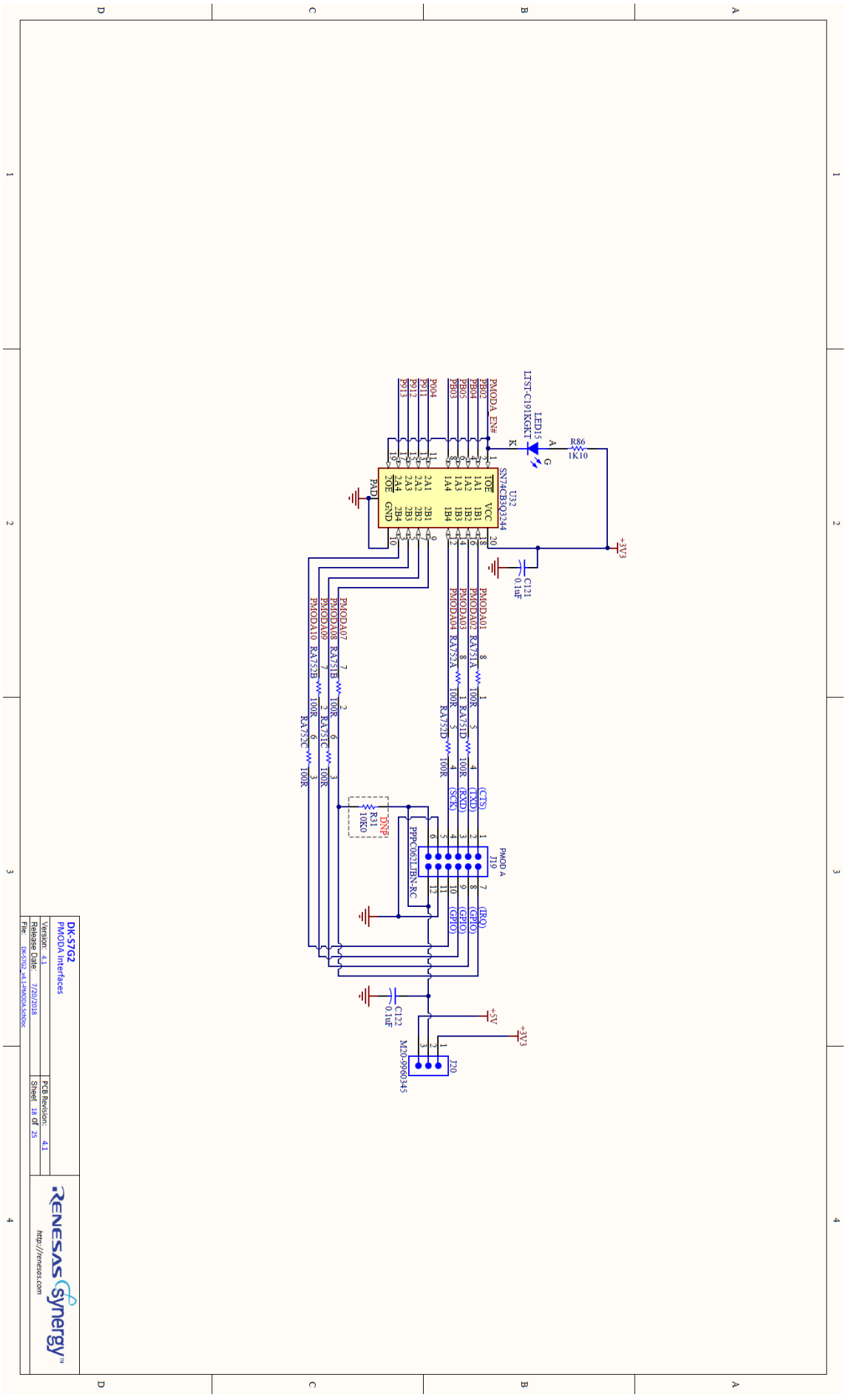

Note: Not compatible with Ethernet0
LED20
LTST-C191KGKT
R91
1K10
+3V3
U19
SN74CB3Q3244
SD_EN#
P412
P413
P903
P414
P411
P410
P206
P205
PAD
GND
VCC
C73
0.1uF
RA554A
RA553B
RA554D
RA554C
RA553A
RA554B
RA553C
RA553D
22R
SD CMD
SD CLK
SD CD
SD WP
SD D0
SD D1
SD D2
SD D3
RA551D
RA551A
RA552A
RA552D
RA551B
RA551C
RA552B
RA552C
22K
C74
10uF
C75
0.1uF
C1
C2
J12
SD CARD SOCKET
CS/D3
Din/CMD
Vss
Vdd
CLK
Vss
Dout/D0
D1
D2
CDet
WPS
CD
WP
DK-S7G2
SD Card
Version: 4.1
Release Date: 7/20/2018
File: DK-S7G2_v4.1-SD.SchDoc
PCB Revision: 4.1
Sheet 13 of 25
RENESAS synergy™
http://renesas.com

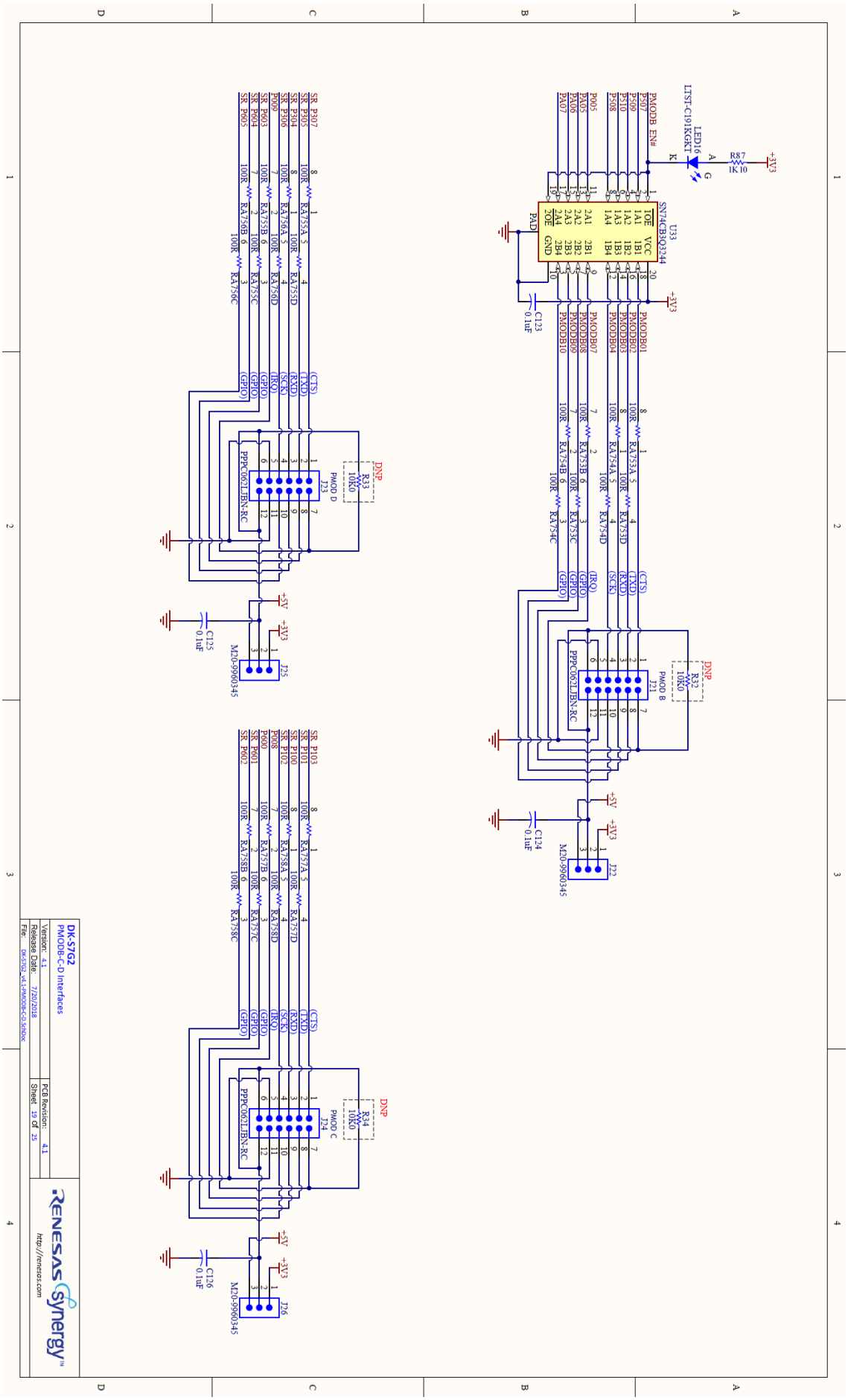

TOTAL CURRENT AVAILABLE IS 560mA NOMINAL, 400mA MIN, AND 720mA MAX.
USB Device
USB Host
DK-S7G2
USB Host and Device Interfaces

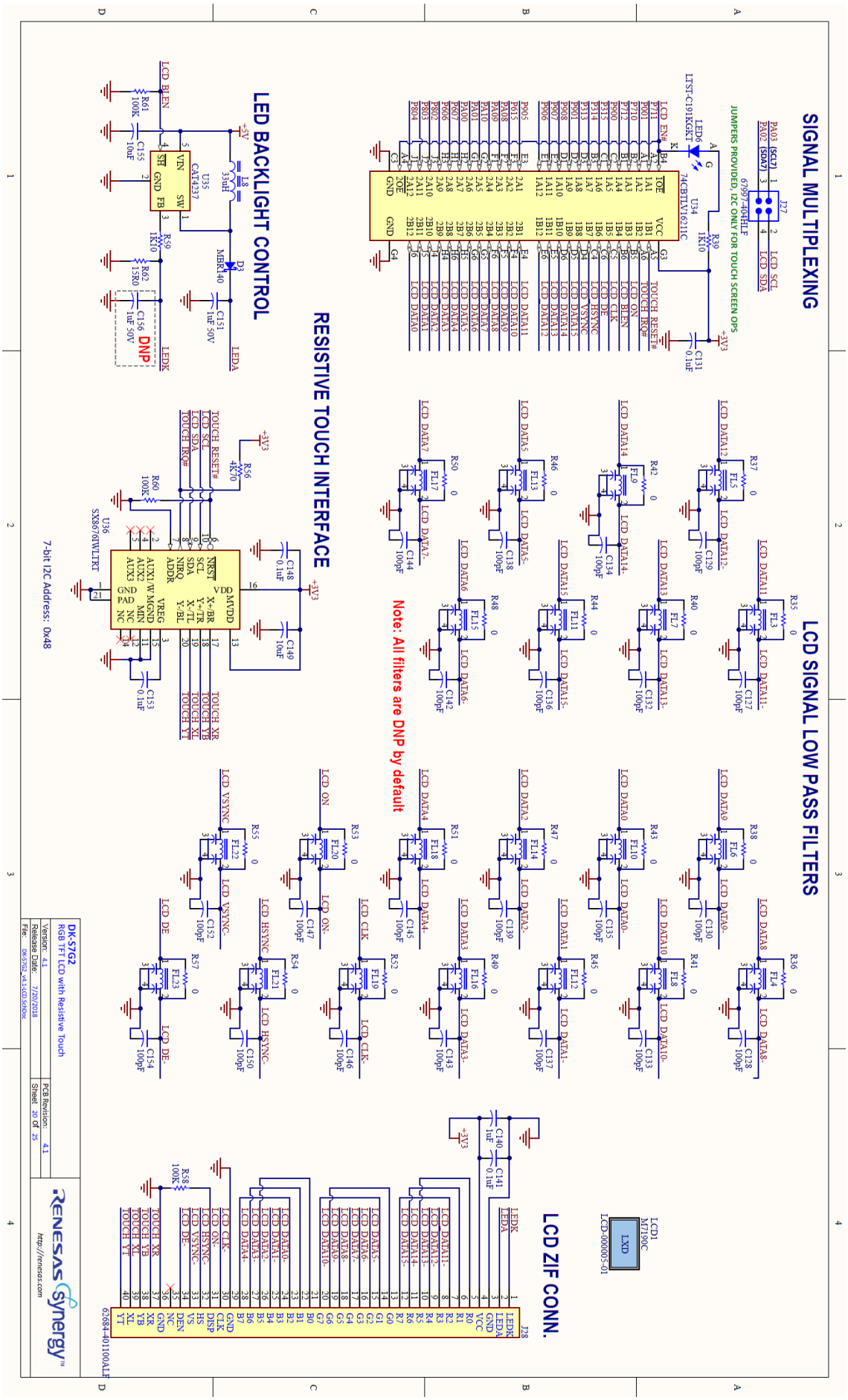

DK-S7G2
Ethernet Interface #0 (ETH0)
Version: 4.1
Release Date: 7/20/2018
File: DK-S7G2_v4.1-Ethernet0.SchDoc
PCB Revision: 4.1
Sheet 15 Of 25
RENESAS Synergy™
http://renesas.com
U25
74CBTLV16211C
U24
74AHC1G14
LED11
LTST-C191KGKT
U23
KSZ8091RNB
J16
ARJC02-11000D
Y3
25MHz
ETH0 EN#
ETH0 IRQ#
ETH0 RESET#
ETH0 MDIO
ETH0 MDC
ETH0 CRS_DV
ETH0 TXD EN
ETH0 TXD0
ETH0 TXD1
ETH0 RXD1
ETH0 RXD0
ETH0 RX_ER
ETH0 REFSOCK1
ETX0 P
ETX0 N
ERX0 P
ERX0 N
+3V3
GND

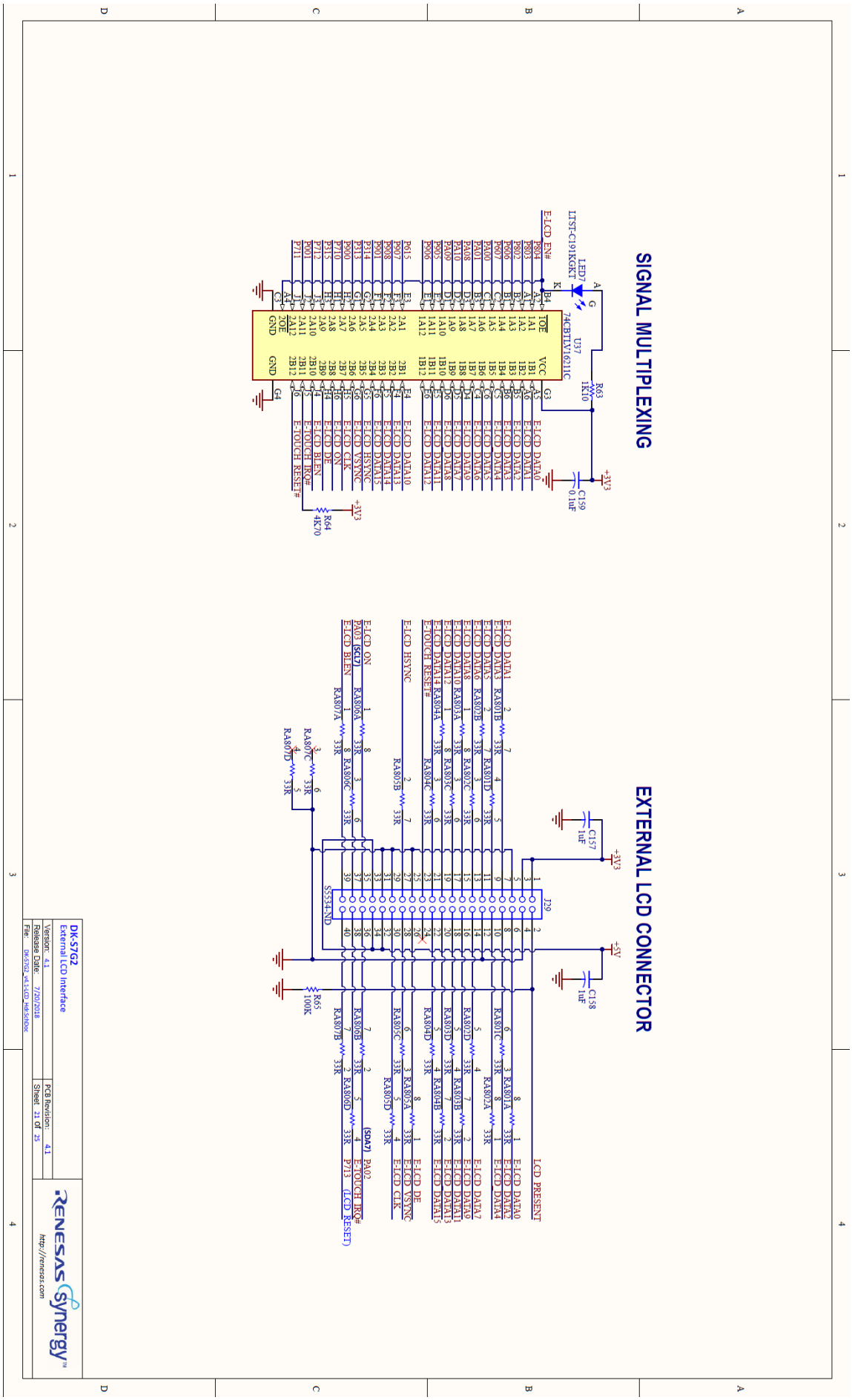

DK-S7G2
Ethernet Interface #1 (ETH1)
Version: 4.1
Release Date: 7/20/2018
PCB Revision: 4.1
Sheet 16 of 25
RENESAS synergy
http://renesas.com
U27
KSZ8091RNB
U28
74CBTLV16211C
U26
74AHC1G14
J17
ARJC02-111009D
LED12
LTST-C191KGKT
Y4
25MHz
L7
120@100MHz
ETH1 EN#
ETH1 IRQ#
ETH1 RESET#
ETH1 MDC
ETH1 MDIO
ETH1 CRS_DV
ETH1 TXD1
ETH1 TXD0
ETH1 TXD_EN
ETH1 RXD1
ETH1 RXD0
ETH1 RX_ER
ETH1 REFSOCK1
ETH1 TXN
ETH1 TXP
ETH1 RXN
ETH1 RXP
ETH1 ETXI_N
ETH1 ETXI_P
ETH1 ERXI_N
ETH1 ERXI_P
+3V3
R83 1K10
C99 0.1uF
C100 0.1uF
C101 12pF
C102 12pF
C103 4.7uF
C104 2.2uF
C105 0.1uF
C106 0.1uF
C107 2.2uF
C108 0.1uF
C109 4.7uF
C110 0.1uF
C111 0.1uF
R28 27K0
R29 100K
R30 6K49
RA656D 5 4K7
RA656A 8 4K7
RA656B 7 4K7
RA656C 6 4K7
RA657A 8 470R
RA657D 5 470R
RA657B 7 470R
RA657C 6 470R
RA660D 33R
RA659C 33R
RA658B 33R
RA659A 33R
RA660B 33R
RA658C 33R
RA659D 33R
RA660A 33R
RA658D 33R
RA658A 33R
RA660C 33R

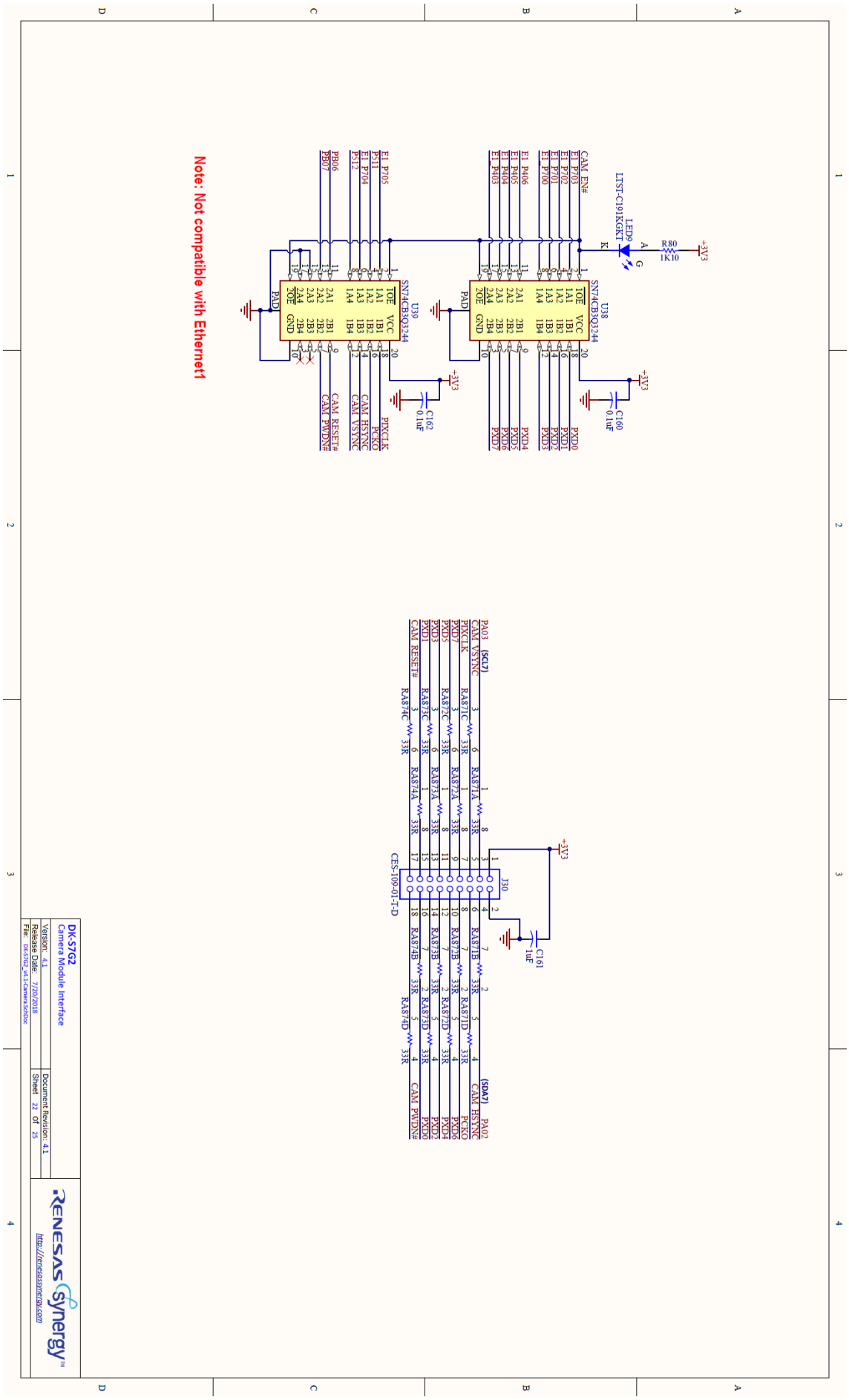

DK-S7G2
RS232/485, CAN Interfaces
Version: 4.1
Release Date: 7/20/2018
File: DK-S7G2_v4.1-RS232_485_CAN.SchDoc
PCB Revision: 4.1
Sheet 17 of 25
RENESAS synergy
http://renesas.com
CAN_EN#
LED18
LED19
LTST-C191KGKT
R89
R90
1K10
+3V3
+5V
U30
SN74CBTQ3244
U31
IFX1050
U29
ISL41387
D2
NTP2105
S5
4P DIP SW
RA701A
RA701B
RA701C
RA701D
100K
C116
C117
C118
C119
C120
C112
C113
C114
C115
0.1uF
10nF
RS485/232#
RS_SLEW
RS_SPB
RS_ON
RS_DEN
RS_RX
CAN_TX
CAN_RX
RS_EN#
CRXD
CTXD
RXD1
TXD1
RS232/485-CAN
J18
20020110-C081A01LF

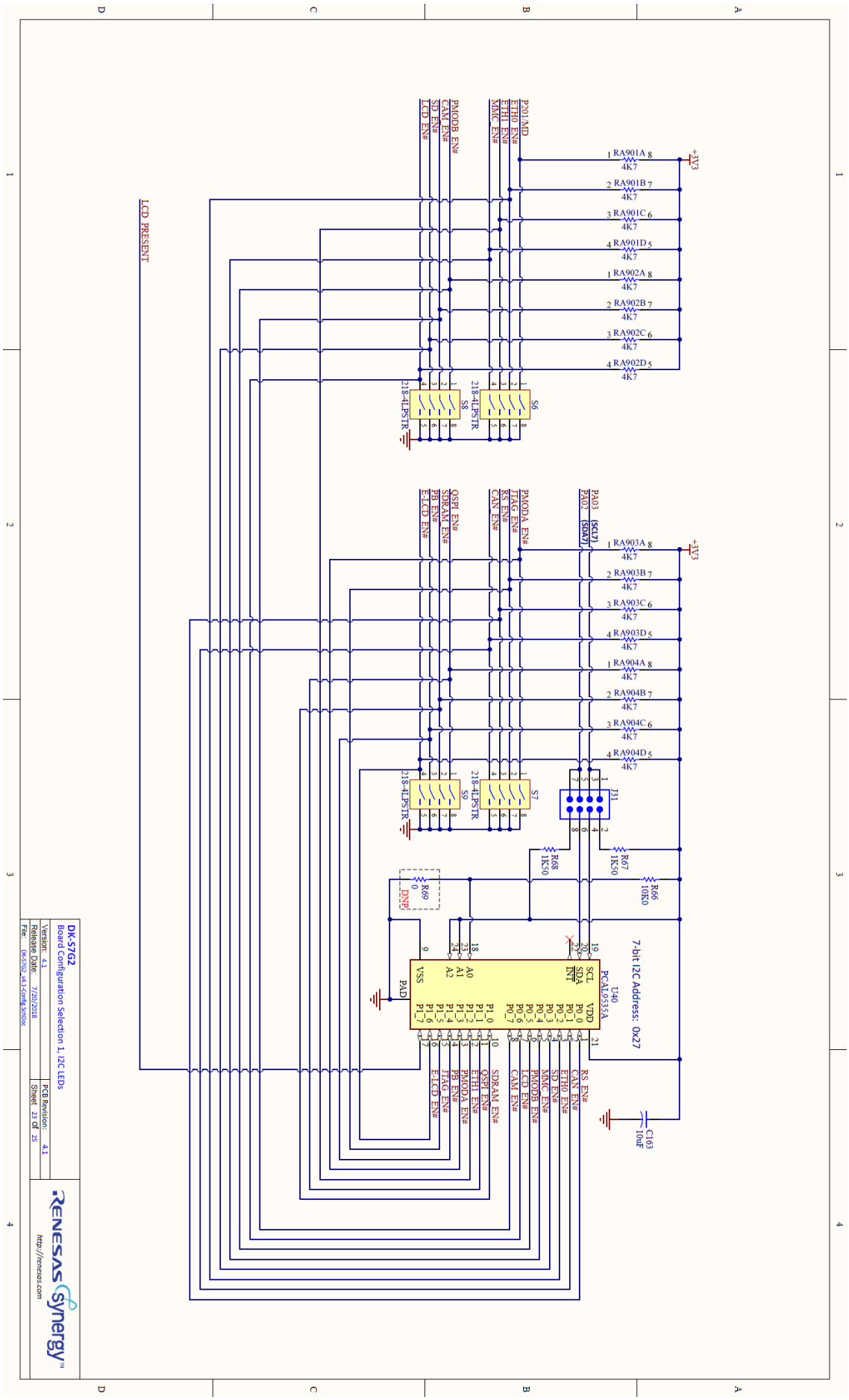

DK-S7G2
PMODA Interfaces
Version 4.1
Release Date 7/20/2018
PCB Revision 4.1
Sheet 18 of 25
RENESAS Synergy
http://renesas.com
LED15
LTST-C191KGKT
R86
1K10
SN74CB3Q3244
U33
C121
0.1uF
+3V3
PMODA_EN#
PMODA01
PMODA02
PMODA03
PMODA04
PMODA07
PMODA08
PMODA09
PMODA10
RA751A
RA751B
RA751C
RA751D
RA752A
RA752B
RA752C
RA752D
100R
R31
10KΩ
DNP
PPPC062LJBN-RC
PMOD A
J19
(CTS)
(TXD)
(RXD)
(SCK)
(GPIO)
(IRQ)
C122
0.1uF
+5V
J20
M20-9900345

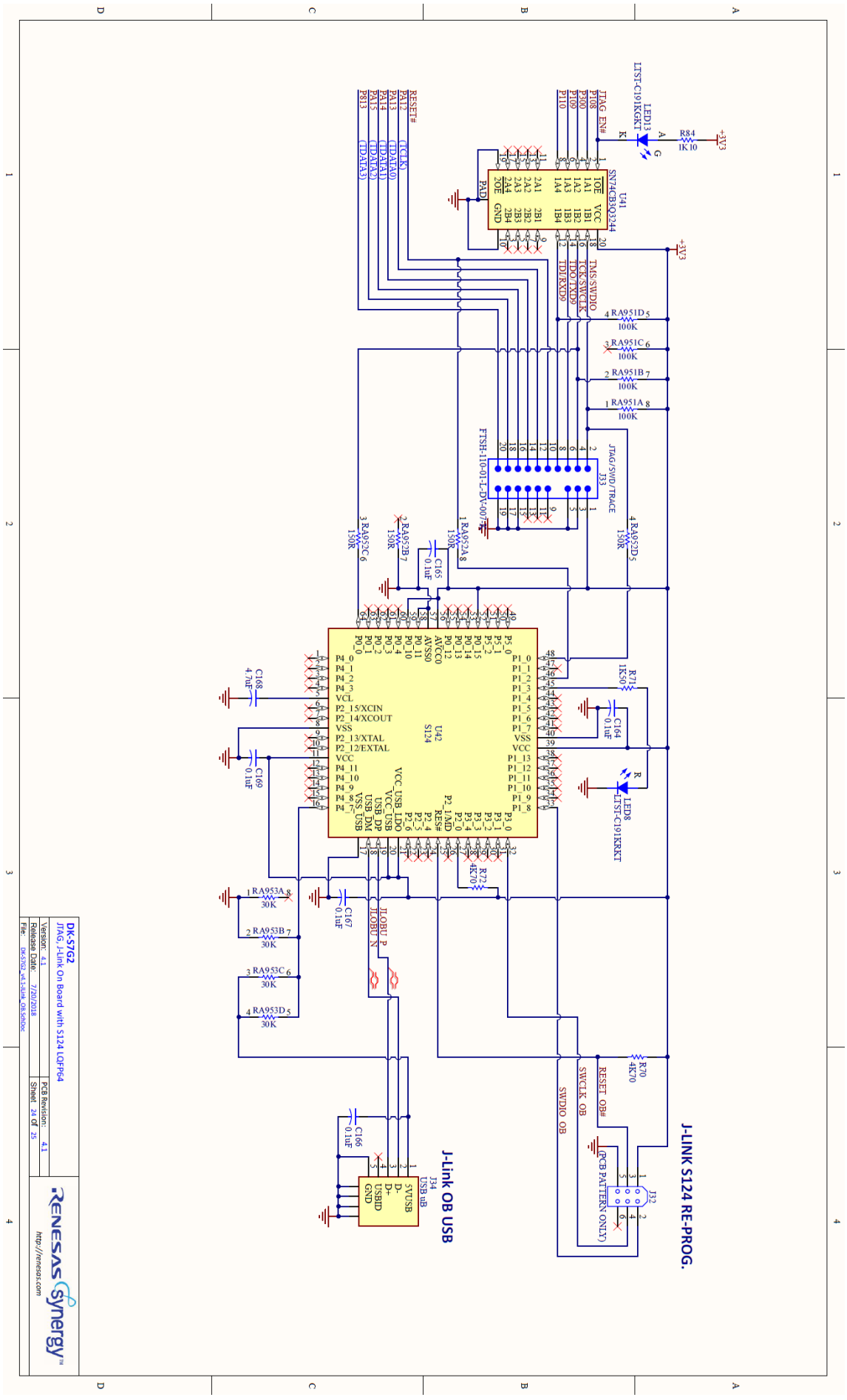

DK-S7G2
PMODB-C-D Interfaces
Version: 4.1
Release Date: 7/20/2018
PCB Revision: 4.1
Sheet 19 Of 25
RENESAS synergy
http://renesas.com
PMOD B
PMOD C
PMOD D
SN74CBQ3244
LED16
LTST-C191KGKT
R87
1K 10
C123
C124
C125
C126
0.1uF
M20-9960345
PPPC062LJBN-RC
DNP
R32
R33
R34
10K0
+3V3
+5V

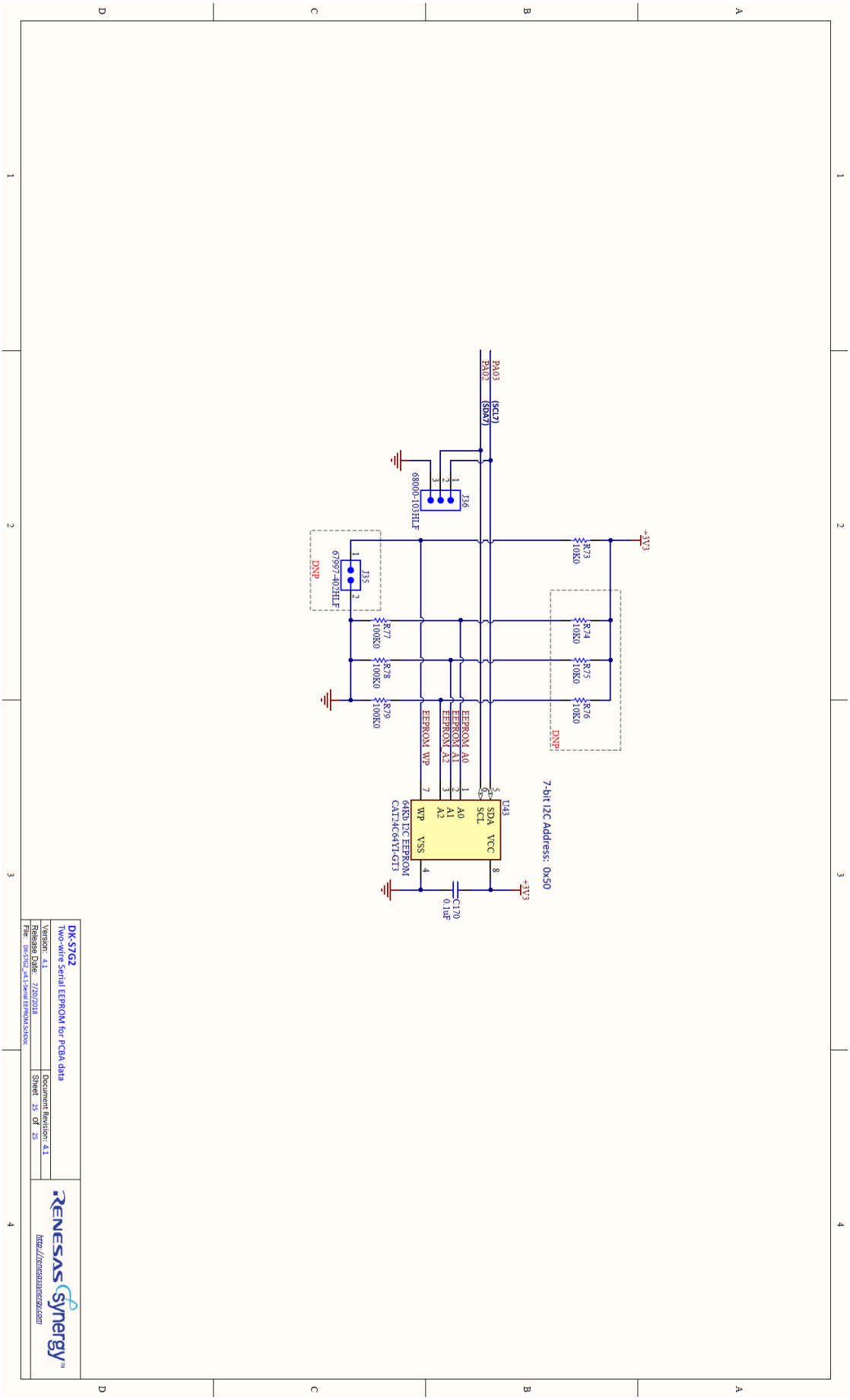

SIGNAL MULTIPLEXING
LCD SIGNAL LOW PASS FILTERS
LED BACKLIGHT CONTROL
RESISTIVE TOUCH INTERFACE
LCD ZIF CONN.
Note: All filters are DNP by default
7-bit I2C Address: 0x48
DK-S7G2
RGB TFT LCD with Resistive Touch
Version: 4.1
Release Date: 7/20/2018
PCB Revision: 4.1
Sheet 20 Of 25
RENESAS synergy
http://renesas.com


SIGNAL MULTIPLEXING
EXTERNAL LCD CONNECTOR
LED7
LTST-C191KGKT
74CBTLV16211C
U37
R63
1K10
C159
0.1uF
R64
4K70
J29
C157
1uF
C158
1uF
R65
100K
LCD PRESENT
DK-S7G2
External LCD Interface
Version: 4.1
Release Date: 7/30/2018
PCB Revision: 4.1
Sheet 21 of 25
RENESAS synergy™
http://renesas.com

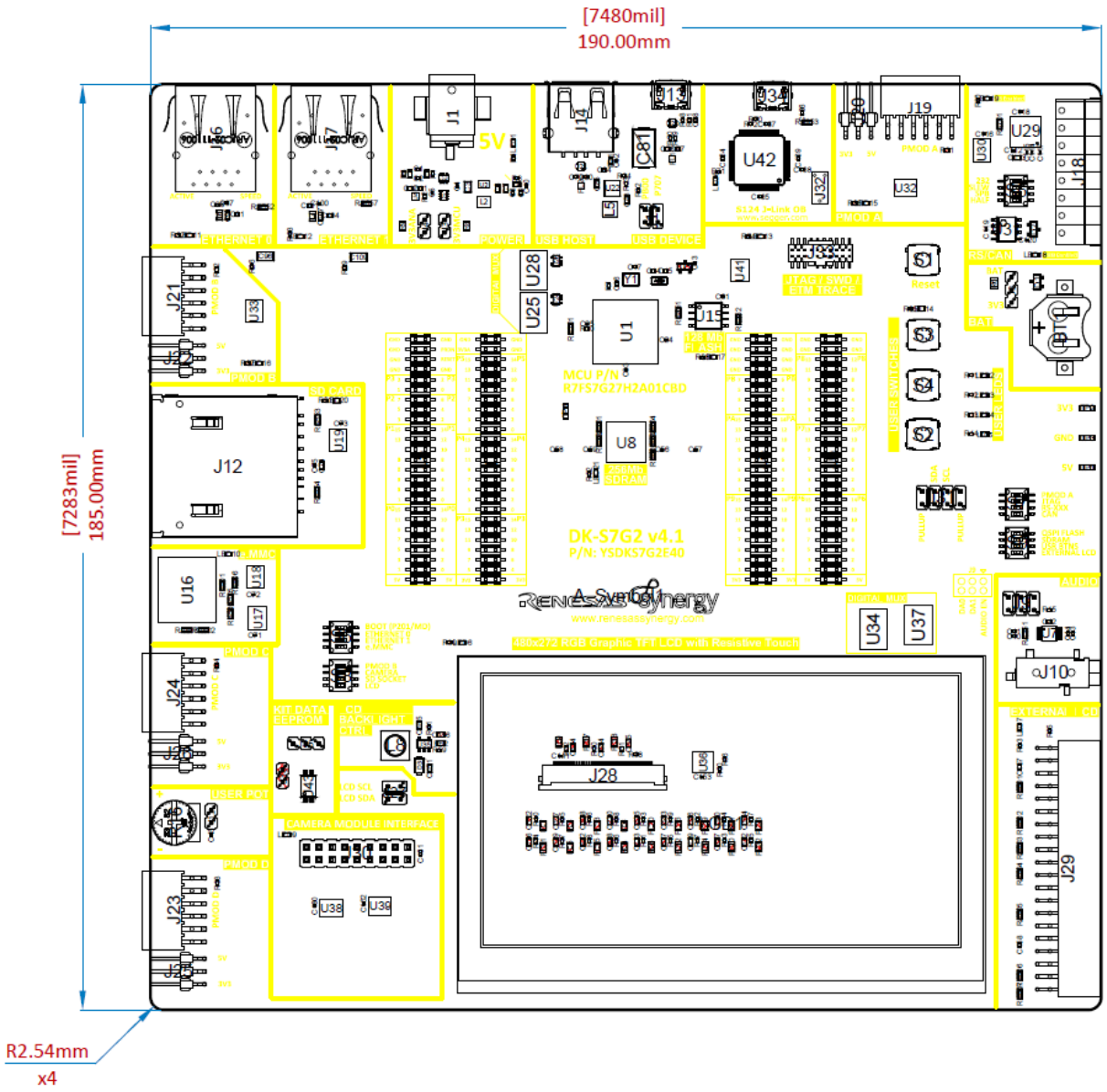

Note: Not compatible with Ethernet1
DK-S7G2
Camera Module Interface
Version: 4.1
Release Date: 7/20/2018
File: DK-S7G2_v4.1-Camera.SchDoc
Document Revision: 4.1
Sheet 21 of 25
RENESAS Synergy
http://renesassynergy.com
U38
SN74CBTQ3244
U39
SN74CBTQ3244
J30
CES-109-01-T-D
LED9
LTST-C191KGKT
R80
1K10
C160
0.1uF
C162
0.1uF
C161
1uF
+3V3
CAM_EN#
PXD0
PXD1
PXD2
PXD3
PXD4
PXD5
PXD6
PXD7
PCKO
CAM_HSYNC
CAM_VSYNC
PIXCLK
CAM_RESET#
CAM_PWDN#
(SCL7)
(SDA7)


LCD PRESENT
PMODB_EN#
CAM_EN#
SD_EN#
LCD_EN#
P201AD
ETH0_EN#
ETH1_EN#
MMC_EN#
RA901A 8
RA901B 7
RA901C 6
RA901D 5
RA902A 8
RA902B 7
RA902C 6
RA902D 5
4K7
+3V3
218-4LPSTR
S8
S6
QSPI_EN#
SDRAM_EN#
PB_EN#
E-LCD_EN#
PMODA_EN#
JTAG_EN#
RS_EN#
CAN_EN#
PA03 (SCL7)
PA02 (SDA7)
RA903A 8
RA903B 7
RA903C 6
RA903D 5
RA904A 8
RA904B 7
RA904C 6
RA904D 5
S9
S7
J31
R68 1K50
R67 1K50
R66 10K0
R69 0 -DNP
U40
PCAL9535A
7-bit I2C Address: 0x27
SCL
SDA
INT
VDD
VSS
A0
A1
A2
P0_0
P0_1
P0_2
P0_3
P0_4
P0_5
P0_6
P0_7
P1_0
P1_1
P1_2
P1_3
P1_4
P1_5
P1_6
P1_7
PAD
C163 10uF
SDRAM_EN#
QSPI_EN#
PB_EN#
PMODA_EN#
JTAG_EN#
E-LCD_EN#
LCD_EN#
CAM_EN#
PMODB_EN#
MMC_EN#
SD_EN#
ETH0_EN#
ETH1_EN#
CAN_EN#
RS_EN#
DK-S7G2
Board Configuration Selection 1, I2C LEDs
Version: 4.1
Release Date: 7/20/2018
File: DK-S7G2_v4.1-Config.SchDoc
PCB Revision: 4.1
Sheet 23 of 25
RENESAS synergy
http://renesas.com


DK-S7G2
JTAG J-Link On Board with S124 LQFP64
Version: 4.1
Release Date: 7/20/2018
File: DK-S7G2 v4.1-sink OB.SchDoc
PCB Revision: 4.1
Sheet 24 of 25
RENESAS synergy™
http://renesas.com
J-LINK S124 RE-PROG.
J-Link OB USB
JTAG/SWD/TRACE
U42
S124
U41
SN74CB3Q3244
LED13
LTST-C191KGKT
LED8
LTST-C191KRKT
FTSH-110-01-L-DV-007
J34
USB uB
J32
(PCB PATTERN ONLY)
RESET OB#
SWCLK OB
SWDIO OB
JLOBU P
JLOBU N
TMS SWDIO
TCK SWCLK
TDO TXD9
TDI RXD9
RESET#
(TCLK)
(TDATA0)
(TDATA1)
(TDATA2)
(TDATA3)
JTAG EN#
+3V3
5VUSB
USBID
D-
D+
GND


PA03 (SCL7)
PA02 (SDA7)
J36
68000-103HLF
J35
67997-403HLF
DNP
+3V3
R73 10KΩ
R74 10KΩ
R75 10KΩ
R76 10KΩ
DNP
R77 100KΩ
R78 100KΩ
R79 100KΩ
EEPROM WP
EEPROM A0
EEPROM A1
EEPROM A2
U43
SDA
SCL
A0
A1
A2
WP
VSS
VCC
64Kb I2C EEPROM
CAT24C64YI-GT3
C170 0.1uF
7-bit I2C Address: 0x50
DK-S7G2
Two-wire Serial EEPROM for PCBA data
Version: 4.1
Release Date: 7/20/2018
Document Revision: 4.1
Sheet 25 of 25
RENESAS Synergy
http://renesassynergy.com

7. Mechanical Drawing



8. Certifications

FCC Compliance

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Japanese VCCI Normative Annex 1 and Normative Annex 1-1, Class B ITE

This is a Class B product based on the standard of the VCCI Council. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

China SJ/T 113642014, 10 year environmental protection use period.

Chinese National Standard 13438, C6357 compliance, Class B limits

Australia/New Zealand AS/NZS CISPR 32:2015, Class B

EU RoHS

EU EMI/EMC compliance

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

Synergy Software	www.renesas.com/synergy/software
Synergy Software Package	www.renesas.com/synergy/ssp
Software add-ons	www.renesas.com/synergy/addons
Software glossary	www.renesas.com/synergy/softwareglossary
Development tools	www.renesas.com/synergy/tools
Synergy Hardware	www.renesas.com/synergy/hardware
Microcontrollers	www.renesas.com/synergy/mcus
MCU glossary	www.renesas.com/synergy/mcuglossary
Parametric search	www.renesas.com/synergy/parametric
Kits	www.renesas.com/synergy/kits
Synergy Solutions Gallery	www.renesas.com/synergy/solutionsgallery
Partner projects	www.renesas.com/synergy/partnerprojects
Application projects	www.renesas.com/synergy/applicationprojects
Self-service support resources:	
Documentation	www.renesas.com/synergy/docs
Knowledgebase	www.renesas.com/synergy/knowledgebase
Forums	www.renesas.com/synergy/forum
Training	www.renesas.com/synergy/training
Videos	www.renesas.com/synergy/videos
Chat and web ticket	www.renesas.com/synergy/resourcelibrary

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.15.19	-	First release document

Development Kit S7G2 (DK-S7G2) User's Manual

Publication Date: Apr.15.19

Published by: Renesas Electronics Corporation

Renesas Synergy™ Platform
Development Kit S7G2 (DK-S7G2)

Renesas Electronics Corporation

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