Contents

List of Figures

List of Tables

1 Control Logic

1.1. General Description

The control logic of the ZSC31150 consists of the calibration microcontroller (CMC) and the control logic modules of the analog-to-digital (A/D) converter and serial digital interface. The configuration of the various modes of the device is done by programming an EEPROM.

The CMC controls the measurement cycle and performs the calculations for sensor signal conditioning. This eliminates the gain deviation, the offset, the temperature deviation, and the non-linearity of the pre-amplified and A/D-converted sensor signal.

Communication between the ZSC31150 and an external microcontroller, especially for calibration purposes, is done via a serial digital interface. Communication protocols according to the I^2C standard are supported. A one-wire interface called OWI with the brand name ZACwire™ is also implemented. These serial interfaces are used for calibration of the sensor system consisting of a sensor transducer and the ZSC31150. The serial interface provides the read-out of the results of sensor signal conditioning as digital values during the calibration. The internal processing of received interface commands is done by the CMC. Therefore, the measurement cycle is interrupted if a command is received. Only the read-out of data is controlled by the serial interface itself and does not interrupt the CMC.

The controller of the A/D conversion is started by the CMC and executed as a continuous measurement cycle. The conditioning calculation by the CMC works in parallel to the A/D conversion.

1.2. CMC Description

The CMC is especially adapted to the tasks connected with the signal conditioning.

The main features are

- 16-bit processing width and programming via ROM.
- Constants/coefficients for the conditioning calculation stored in the EEPROM. After power-on or after re-initialization from EEPROM by sending a specific command to the serial interface, the EEPROM is mirrored to the RAM.
- Continuous parity checking during every read from RAM. If incorrect data is detected, the diagnostic mode (DM) is activated (an error code is written to the serial digital output; the analog out is set to the diagnostic level).

1.3. General Working Modes

The ZSC31150 supports three different working modes:

- Normal Operation Mode (NOM)
- Command Mode (CM)
- Diagnostic Mode (DM)

The command set includes commands for changing the working mode. Refer to section 4 for a detailed description of these commands.

1.3.1. Normal Operation Mode (NOM)

The NOM is the recommended working mode for applications. After power-on, the ZSC31150 starts with an initialization routine, and the NOM will be activated after this.

During the initialization routine, first the EEPROM is mirrored to the RAM, which checks the EEPROM content. If an error is detected, the DM is activated. The configuration of the ZSC31150, which is stored in the EEPROM, is consecutively set.

Next, the continuous measurement cycle and the conditioning calculation start. The signal conditioning result is refreshed with each cycle time period. This generates the analog output at the AOUT pin, and it can be read via the serial digital Interface (SIF) as a digital output.

Provided that the EEPROM is programmed correctly, the NOM works without the microcontroller sending any command to the digital serial interface. Read-out of the conditioning result via the SIF is possible; this does not interrupt continuous processing of the signal conditioning routine.

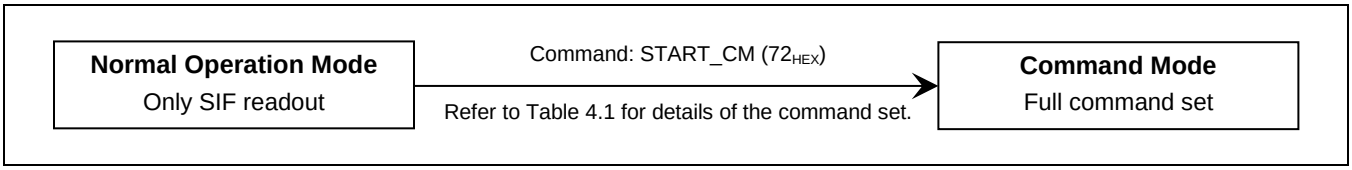
1.3.2. Command Mode (CM)

The CM is the working mode that is used for calibration data acquisition and access to the internal RAM and EEPROM of the ZSC31150. The CM start command START_CM aborts the running NOM, so the measurement cycle is stopped. The ZSC31150 changes to CM only after receiving the START_CM command via the digital serial interface. This protects the ZSC31150 against interruption of processing during the NOM (= continuous signal conditioning) and/or unintentional changes of configuration. In CM, the full set of commands is supported.

If the ZSC31150 receives a command other than START_CM in NOM, it is not valid. It will be ignored, and no interrupt to the continuous measurement cycle will be generated. Refer to section 4.5.1 for a detailed description of the START_CM command.

In CM, the full command set is enabled for processing. During processing of a received command, the serial interface is disabled, and no further commands are recognized. After finishing the routine, the CMC waits for further commands or the process loops continuously (e.g., after measurement commands).

Figure 1.1 Modes of Digital Serial Communication



EEPROM programming is only enabled after receiving the EEP_WRITE_EN command.

Starting CM via I^2C communication (SCL and SDA pins) is possible at any time. For communication via the one-wire interface (AOUT pin), several modes can be activated in the configuration setup, e.g., the start window.

1.3.3. Diagnostic Mode (DM), Failsafe Tasks, and Error Codes

The ZSC31150 detects various possible failures, in which case the DM is activated. The DM is indicated by the ZSC31150 setting the output pin AOUT in the lower diagnostic range (LDR) and the output registers of the digital serial interface are set to a defined error code. In this case, independent from configuration, the OWI and I^2C communication is enabled, and an error code can be read out.

Because the analog output AOUT is driven LOW, the AOUT pin must be overwritten (AOUT current limitation: < 20mA) for starting digital communication using the OWI interface. Therefore the communication master must provide driving capability for doing this.

Note that the error detection functionality can be partly enabled/disabled by configuration words (e.g., sensor connection check, sensor aging (CMV) limits, ROM check, etc.).

The failure counting sequence/procedure is called the “Temporary DM.” The DM (LDR) will be activated after two sequential detected failure events and will be deactivated after counting down the failure counter if the failure condition is no longer given.

1.3.3.1. Power and Ground Loss

Power and ground loss cases are indicated by pulling the AOUT pin into the lower or upper diagnostic range (LDR/UDR) in the event of a lost node or load connection to ground or the supply. The ZSC31150 is inactive in this case, and the specified leakage current in combination with the load resistor guarantees reaching the LDR or UDR.

1.3.3.2. Temperature Sensor Check *

The temperature sensor check monitors whether the ADC exceeds lower or upper temperature limits.
Possible causes of failure are

- The external temperature sensor is unconnected.
- The offset of the temperature measurement (ADJREF:TOFFS) is not sufficiently adjusted; signal is out of the ADC range.

The temperature raw value (T) is checked to determine if it is equal 0 or if it is greater or equal to ($2^{RESOLUTION}$ - 1).

16/15 bit raw values are shifted to 14/13 bits before the check. The temperature sensor (TS) check uses the failure counter sequence (i.e., temporary DM).

* **Note:** The Temperature Sensor Check is only available for ZSC31150Dxx and subsequent versions.

Table 1.1 Error Codes

Note: In the case of detection of different failures with the code "C0xx$_{HEX}$," the codes are "OR" combined. If any signature or configuration error occurs, it is overwritten if there is a watchdog error at the watchdog timeout.

Failsafe Task	Description	Messaging Time	Error Code	Deactivation	Action
Oscillator Fail (OFC)	Detects faulty oscillator operation	< 200µs	-	No	Temporary DM
Watchdog Timeout (WDG)	Detection of watchdog timeout of start routine (69632 clocks) or measurement cycle (2 x conversion cycle time)	Always	C008$_{HEX}$	No	DM or Reset
RAM Parity (RAP)	Parity check at every RAM access	Without Delay	C001$_{HEX}$	No	DM or Reset
Register Parity (RGP)	Permanent parity check of configuration registers	Without Delay	C002$_{HEX}$	No	DM or Reset
EEPROM Multi-bit (EMC)	Detection of non-correctable multi-bit error per 16-bit word	Start Up	C004$_{HEX}$	No	DM
EEPROM Signature (ECS)	Signature check during read out of EEPROM after power-on or after START_CYC_EEP* command	Start Up	C0AA$_{HEX}$	No	DM
ROM Signature (RSC)	ROM signature check at power-on (enabled by CFGAPP:CHKROM; needs approximately 10ms additional startup time)	Start Up	C0CC$_{HEX}$	Yes	DM
Only for product codes ZSC31150Ex and earlier: Inconsistent Configuration (ICC)	Detects digital averaging filter coefficients failure, analog output limits out of addressable range, or undefined command in CM	Start Up / Command Received	C0FF$_{HEX}$	No	DM
Arithmetic Check (ACC)	Functional check of arithmetic unit during measurement cycle		C010$_{HEX}$	No	DM or Reset
SCC	Sensor connection check (enabled by CFGAPP:CHKSENS)	Processed once per cycle, so message time is a minimum of 2 cycles.	C010$_{HEX}$	Yes	Temporary DM (temporary diagnostic mode)
Temperature Sensor (TS) Check	Temperature sensor AD conversion result check = 0_{HEX} or ($2^{RESOLUTION} - 1$)		C010$_{HEX}$	Yes	
SSC (P/N)	Sensor short check positive/negative biased (enabled by CFGAPP:CHKSENS)		C010$_{HEX}$	Yes	
Sensor Aging (CMV)	Compares sensor bridge common mode voltage to programmed limits Disabled by register A_{HEX} = FF00$_{HEX}$		C010$_{HEX}$	Yes	
Power & Ground Loss (PGL)	Power and ground loss detection; in the event of PGL, the output is pulled into the LDR or UDR by an external pull-up resistor	<5ms	-	No	Reset

2 Signal Conditioning

2.1. AD Conversion

During NOM, the analog preconditioned sensor signal is continuously converted by the ADC. The A/D conversion is configurable for resolution r_{ADC} and the inherent range shift RS_{ADC} by the configuration word CFGAFE (see Table 5.3).The one or two step conversion mode is selectable. The two-step mode is faster; the one-step mode is more accurate because of the longer integration time. The selected resolution for the A/D conversion is equal for all measurements in the measurement cycle (e.g., input voltage, temperature, auto-zero, etc.). The resulting digital raw values for the measured value (e.g., pressure) and temperature are determined by the following equations:

⇒ **Analog differential input voltage to A/D conversion**

Measured value V_{IN_DIFF} to be conditioned:

$$V_{ADC\_DIFF} = a_{IN} * V_{IN\_DIFF} + a_{XZC} * V_{XZC}$$

⇒ **Digital raw A/D conversion result:**

$$Z_{ADC} = 2^{r_{ADC}} \left(\frac{V_{ADC\_DIFF} + V_{OFF}}{V_{ADC\_REF}} + 1 - RS_{ADC} \right)$$

⇒ **Auto-zero value:**

$$Z_{AZ} = 2^{r_{ADC}} \left(\frac{V_{OFF}}{V_{ADC\_REF}} + 1 - RS_{ADC} \right)$$

⇒ **Auto-zero corrected raw A/D conversion result:**

$$Z_{CORR} = Z_{ADC} - Z_{AZ} = 2^{r_{ADC}} \left(\frac{V_{ADC\_DIFF}}{V_{ADC\_REF}} \right)$$

V_{IN_DIFF}	Differential voltage input to analog front-end
V_{OFF}	Residual offset voltage of analog front-end (which is eliminated by $Z_{ADC} – Z_{AZ}$ difference calculation)
V_{XZC}	Extended zero compensation voltage (refer to the *ZSC31150 Data Sheet* for details): $V_{XZC} = V_{ADC\_REF} * PXZC\left(\frac{\left(3^{PXZCPOL} - 2\right)}{48}\right)$ (PXZC and PXZCPOL are bit fields in register CFGAFE.)
a_{IN}	Gain of analog front-end for differential input voltage (see Table 5.3)
a_{XZC}	Gain of extended zero compensation voltage (refer to the *ZSC31150 Data Sheet* for details)
V_{ADC_DIFF}	Differential input voltage to A/D converter
V_{ADC_REF}	ADC reference voltage (ratiometric reference for measurement)
r_{ADC}	Resolution of A/D conversion
RS_{ADC}	Range shift of A/D conversion: Bridge Sensor Measurement: ½, ¾, $^7/_8$, $^{15}/_{16}$ Temperature Measurement: ½ (see section 6)

2.2. AD Conversion Result Segmentation

The result of the AD conversion Z_{CORR}, which is the input value for the signal conditioning formula, depends on the resolution adjustment r_{ADC} ranging from 13 to 16 bit resolution. Raw values acquired with resolutions of 15 and 16 bits must be mapped to the 13 or 14 bit resolution range for further calculations. This is done by different methods depending on the data to be measured:

- CMV, SSC+, and SSC- measurements for diagnostic checks are always shifted to 13 bits.
- The temperature measurement data (Z_{CORR_T}) are divided by 4.
- The bridge sensor (BR) measurement auto-zero corrected data (Z_{CORR}) must be moved in the +/- 2^{15} range (see Table 2.1) by subtraction of the offset determined in configuration register CFGAPP:POFFS (see Table 5.4). Minimum and maximum input data (span of Z_{CORR} raw data) should have 14-bit or slightly higher resolution (16384 ADC counts) for proper calibration coefficients calculation.

AD conversion result segmentation calculation (only if r_{ADC} = 15 or 16 bit)

$$Z_{CORR\_OUT} = Z_{CORR} - POFFS * 2^{13}$$

with POFFS $\in$ [0; 7]

$$Z_{CORR\_TOUT} = \frac{Z_{CORR\_T}}{4}$$

r_{ADC}	Resolution of AD conversion in bits
Z_{CORR}	Raw input main channel A/D result for measured value (auto-zero compensated; $D8_{HEX}$ and $D9_{HEX}$ commands)
Z_{CORR_OUT}	Raw main channel A/D result for measured value (auto-zero compensated), mapped in range given in Table 2.1
Z_{CORR_T}	Raw temperature input A/D result for measured value (auto-zero compensated)
Z_{CORR_TOUT}	Raw temperature A/D result for measured value (auto-zero compensated), mapped in range [-2^{14}; 2^{14})

Note: All raw data acquiring commands (Dx commands listed in Table 4.1) do not process the shifting procedure, and therefore 15 and 16 bit results are read out. Therefore the acquired data must be processed according to the Z_{CORR_OUT} and Z_{CORR_TOUT} formulas above in the following sequence before calculation of the calibration coefficients:

1. Raw calibration data acquisition
2. Z_{CORR_OUT} calculation for the main channel data and the Z_{CORR_T} calculation for temperature data
3. Calibration coefficients calculation using calculated corrected raw data

Important: Results of the ADC conversion Z_{CORR_OUT} greater than +32767 counts (15 bits) will result in negative read-out values and a wrong analog output voltage for AOUT. In this case, a greater offset POFFS, adjusted ADC Range Shift, or lower gain should be used.

Table 2.1 Valid Data Ranges for 15-bit and 16-bit ADC Resolution

ADC Resolution	Range Shift	1/2		3/4		7/8		15/16	
	Data	Min	Max	Min	Max	Min	Max	Min	Max
16 bits	Z_{CORR_IN} ($D8_{HEX}$ & $D9_{HEX}$ commands)	-32768	32767	-16384	49151	-8192	57343	-4096	61439
15 bits		-16384	16383	-8192	24575	-4096	28671	-2048	30719
16 bits	Z_{CORR_OUT}	-32768	32767	-16384	32767	-8192	32767	-4096	32767
15 bits		-16384	16383	-8192	24575	-4096	28671	-2048	30719

Recommendation: To avoid possible ADC saturation, perform a check on the ADC raw data ($D0_{HEX}$ and $D1_{HEX}$ commands). For results close to the limits [0-2^{res}), a lower gain or adjusted RangeShift should be used.

2.3. Signal Conditioning Formula

The digital raw value Z_{CORR} for the measured value to be conditioned is further processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to 3rd order. The signal conditioning equation is computed by the CMC and is defined as follows:

⇒ **Range definition of inputs**

$$Z_{CORR} \in \left[-2^{r_{ADC}}; 2^{r_{ADC}} \right)$$

$$Z_{CORR\_T} \in \left[-2^{r_{ADC}-1}; 2^{r_{ADC}-1} \right)$$

⇒ **Conditioning equations (P = Bridge Sensor Measurand)**

$$Y = \frac{Z_{CORR} + c_0 + 2^{-(r_{ADC}-1)} * c_4 * Z_{CORR\_T} + 2^{-2(r_{ADC}-1)} * c_5 * Z_{CORR\_T}^2}{c_1 + 2^{-(r_{ADC}-1)} * c_6 * Z_{CORR\_T} + 2^{-2(r_{ADC}-1)} * c_7 * Z_{CORR\_T}^2}$$

$$Y \in [0;1)$$

$$P = Y\left(1 - 2^{-15} * c_2 - 2^{-15} * c_3\right) + 2^{-15} * c_2 * Y^2 + 2^{-15} * c_3 * Y^3$$

$$P \in [0;1)$$

r_{ADC} Resolution of AD conversion (13 or 14 bit)

Z_{CORR} Raw A/D result for measured bridge sensor value (auto-zero compensated)

Z_{CORR_T} Raw A/D result for temperature (auto-zero compensated)

Conditioning coefficients stored in EEPROM registers 0 to 7

$c_i \in [-2^{15}; 2^{15})$, two's complement

c_0 … Bridge offset

c_1 … Gain

c_2 … Non-linearity 2nd order

c_3 … Non-linearity 3rd order

c_4 … Temperature coefficient offset 1st order

c_5 … Temperature coefficient offset 2nd order

c_6 … Temperature coefficient gain 1st order

c_7 … Temperature coefficient gain 2nd order

The first equation calculates the intermediate result Y for compensating the offset and fitting the gain including its temperature dependence. The non-linearity is corrected in the next equation, which calculates the non-negative value P for the measured bridge sensor value in the range [0;1). This value P is continuously written to the output register of the digital serial interface during the measurement cycle.

Note: The conditioning coefficients c_i are positive or negative values in two's complement format.

2.4. Analog and Digital Output

The DAC used for generation of the analog output has 5632 levels.

Important: To fit the normalized conditioning result P [0;1) to the DAC ranges, the targets for calibration must be multiplied by 0.6875 = $\left(5632/2^{13}\right)$.

If using the calibration library *RBIC1.DLL*: Note that this multiplication is done in the ZSC31150 Evaluation Kit Software and is not contained in *RBIC1.DLL*. Refer to the *Calibration DLL Description* (*RBIC_DLL_description.txt*) for a description of stand-alone usage of the DLL. *RBIC1.DLL* and *RBIC_DLL_description.txt* can be found in the in the program folder on the user's PC after installation of the ZSC31150 Evaluation Software.

The digital output, i.e., the conditioning result readable via the SIF, is calculated with 15-bit resolution/accuracy (maximum). The MSB is used as the error identifier – if the MSB is set, an error is indicated. In normal cases, this means that if the targets are adjusted for using analog output, the digital output is weighted with factor 0.6875.

If only digital output is used, targets can be calculated using the full 15-bit resolution/accuracy range. The ZSC31150 Evaluation Kit Software offers the option for doing this.

2.5. Digital Filter Function

The ZSC31150 offers a digital (averaging) filter function for calculating the output result in NOM. These filters can also be used for acquiring data in calibration procedures using the START_AD_CNT command "62."

The filter can be parameterized using two programmable coefficients stored in EEPROM: an integrating coefficient PAVG and a differential coefficient PDIFF. (See Table 5.1.) The output $Pout_i$ is set to P_i for the first calculation of an output result for a (new) sent command (e.g., starting NOM or "62").

Set PDIFF and PAVG to 0 to disable the filter function. Default settings for the ZSC31150 disable the filter function. With this function it is possible to build up a low-pass filter.

Important: Ensure that the coefficient $\frac{\text{PDIFF}+1}{2^{\text{PAVG}}}$ never exceeds 1.

If this coefficient exceeds 1, the filter function can oscillate and the system gets a flywheel effect. The filter function can be described as follows:

⇒ **Digital filter function**

$$Pout_i = Pout_{i-1} + \left(P_i - Pout_{i-1}\right)\left(\frac{PDIFF+1}{2^{PAVG}}\right) : i>0$$

with PAVG, PDIFF ∈ [0; 7]

P_i	Conditioning equation result for bridge sensor signal (refer to section 2.2)
$Pout_i$	Output result to be calculated
PAVG	Averaging filter coefficient (EEPROM register 08_{HEX}, [2:0])
PDIFF	Differential filter coefficient (EEPROM register 09_{HEX}, [2:0])

2.6. Output Signal Range and Limitation

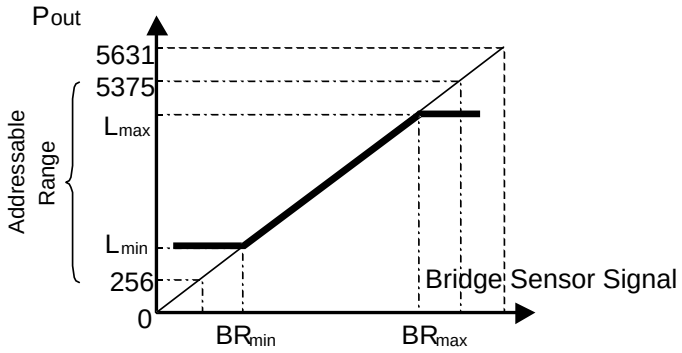
The bridge sensor measurand conditioning result P for the measured value is output at the analog output pin and SIF with >12-bit resolution. The DAC used for generation of the analog output has 5632 levels, where 5120 levels (from 256 to 5375) can be addressed or voltage output from 4.55% to 95.44% of the supply voltage.

$$V_{OUT\_MIN} = (V_{VDDE} - V_{VSSE})\frac{256}{5632} \qquad V_{OUT\_MAX} = (V_{VDDE} - V_{VSSE})\frac{5375}{5632}$$

As a result, an adjustable range from 5% to 95% of the supply including all possible tolerances is guaranteed. Setting the analog output outside the allowed range (for example via the Set_DAC command) will result in entering the diagnostic mode (DM) and setting the output to LDR (Lower Diagnostic Range).

Note that the limit setting registers 08_{HEX} and 09_{HEX} (see Table 5.1) are shared with the digital filter configuration (the 3 LSBs).

Figure 2.1 Accessible Output Signal Range and Limitation



ZSC31150 offers an output limitation function ***for the analog output AOUT***, which clips the output signal if the calculated result is outside of the defined limits. These output minimum and maximum limits (13-bit accuracy) are defined in EEPROM.

⇒ **Limitation**

$$P_{out}(P > L_{max}) = L_{max}$$
$$P_{out}(P < L_{min}) = L_{min} \qquad P_{out} \in [L_{min}; L_{max}]$$

Limits stored in bits [15:3] of EEPROM registers 08_{HEX} and 09_{HEX}:

L_{min}	Lower output limit,
L_{max}	Upper output limit
$L_{min/max} \in$	[100_{HEX}; $14FF_{HEX}$] or [256_{DEC}; 5375_{DEC}]

The output signal V_{OUT} is ratiometric to the power supply (V_{VDDE} - V_{VSSE}) and can be calculated via this equation:

$$V_{OUT} = (V_{VDDE} - V_{VSSE})\frac{P_{OUT}}{5632}$$

P_{OUT}	Calculated digital output value for bridge sensor
V_{OUT}	Output voltage
V_{VDDE}, V_{VSSE}	Potential at pins VDDE and VSSE

The digital output signal, which is calculated with 14-bit resolution, can be read out using digital serial interface communication. Refer to section 4.3 for a detailed description of the SIF output registers.

3 Serial Digital Interface (SIF)

3.1. General Description

The ZSC31150 includes a serial digital interface (SIF), which is able to communicate using two communication protocols: I^2C and ZACwire™ one-wire communication (OWI). The SIF allows programming the EEPROM to configure the application mode of the ZSC31150 and to calibrate the conditioning equations. It provides the read out of the conditioning result of the measured value as a digital value. The ZSC31150 always works as a slave.

The communication protocol used is selectable. In Command Mode (CM) both communication protocols are always available. The access mode for OWI communication is programmable in EEPROM (ADJREF: IFOWIM; see Table 5.5). There are two start window modes and a mode with continuous OWI access. OWI access can also be locked so that communication is only possible via the I^2C protocol.

An unconfigured ZSC31150, identified by a non-consistent EEPROM signature, always starts in diagnostic mode (DM). The output is driven LOW in this case so that the lower diagnostic range can be detected. Independent from the configuration, OWI and I^2C communication is enabled, any error codes can be read out, and access to the EEPROM content for rewriting is possible.

A command consists of an address byte and a command byte. Some commands (e.g., writing data into EEPROM) also include two data bytes. This is independent of the communication protocol used. Refer to section 1.3 for details about working modes and section 4 for command descriptions.

There are two general types of requests to read data via the SIF from the ZSC31150:

- Continuously reading the conditioning result in NOM
  ➔ Digital data read out
- Reading of internal data (e.g., RAM/EEPROM content) or acquired measurement data in CM
  ➔ Calibration and/or configuration tasks

To read internal and/or measurement data from the ZSC31150 in CM, normally a specific command must be sent to transfer this data into the output register of the SIF. Thereafter the READ command consisting of the address byte with the read bit set is used to retrieve this data. The data transmission is continuously repeated until the master sends a stop condition. Again this is independent of the communication protocol used. During the measurement cycle (NOM), the ZSC31150 transfers the conditioning result into the output register of the SIF. These data will be sent if the master generates a read-request. The active measurement cycle is not interrupted by this.

3.1.1. Addressing

Addressing is supported by the I^2C and ZACwire™ interface. Every slave connected to the master responds to a specific address. After generating the start condition, the master sends the address byte containing a 7-bit address followed by a data direction bit (R/W). A ‘0’ indicates a transmission from master to slave (WRITE); a ‘1’ indicates a data request (READ).

The general ZSC31150 slave address is 78_{HEX} (7-bit). The addressed slave answers with an acknowledge (only I^2C). All other slaves connected to the master ignore this communication. Via EEPROM programming, it is possible to allocate and activate an additional available slave address within the range 70_{HEX} to $7F_{HEX}$ to a single device. In this case, the device recognizes communication on both addresses, on the general one and on the additional one.

3.1.2. Communication Verification

A read request is answered by the data present in the SIF output registers (2 bytes). A check sum is also sent (1 byte) followed by the command that is being answered. The check sum and the returned command allow the verification of received data by the master. For details and exceptions, also see section 4.3.

3.1.3. Communication Protocol Selection

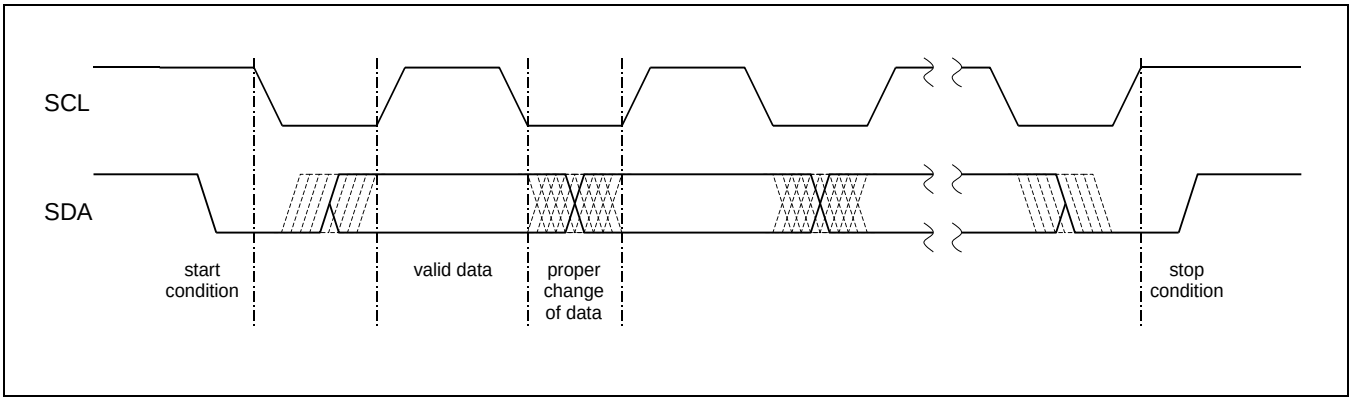
Both available protocols, I^2C and OWI, are active in parallel, but only one interface can be used at a time.

OWI communication access is also possible if OWI communication is enabled and the analog output is active (OWIANA and OWIWIN after start window; see section 3.3). For this option, the active output AOUT must be overwritten by the communication master, so it is recommended that a stop condition be generated before starting the communication to guarantee a defined start of communication (refer to section 3.3).

3.2. I^2C Protocol

For I^2C communication, a data line (SDA) and a clock line (SCL) are required.

Figure 3.1 I^2C – Principles of Protocol



The I^2C communication and protocol used is defined as follows:

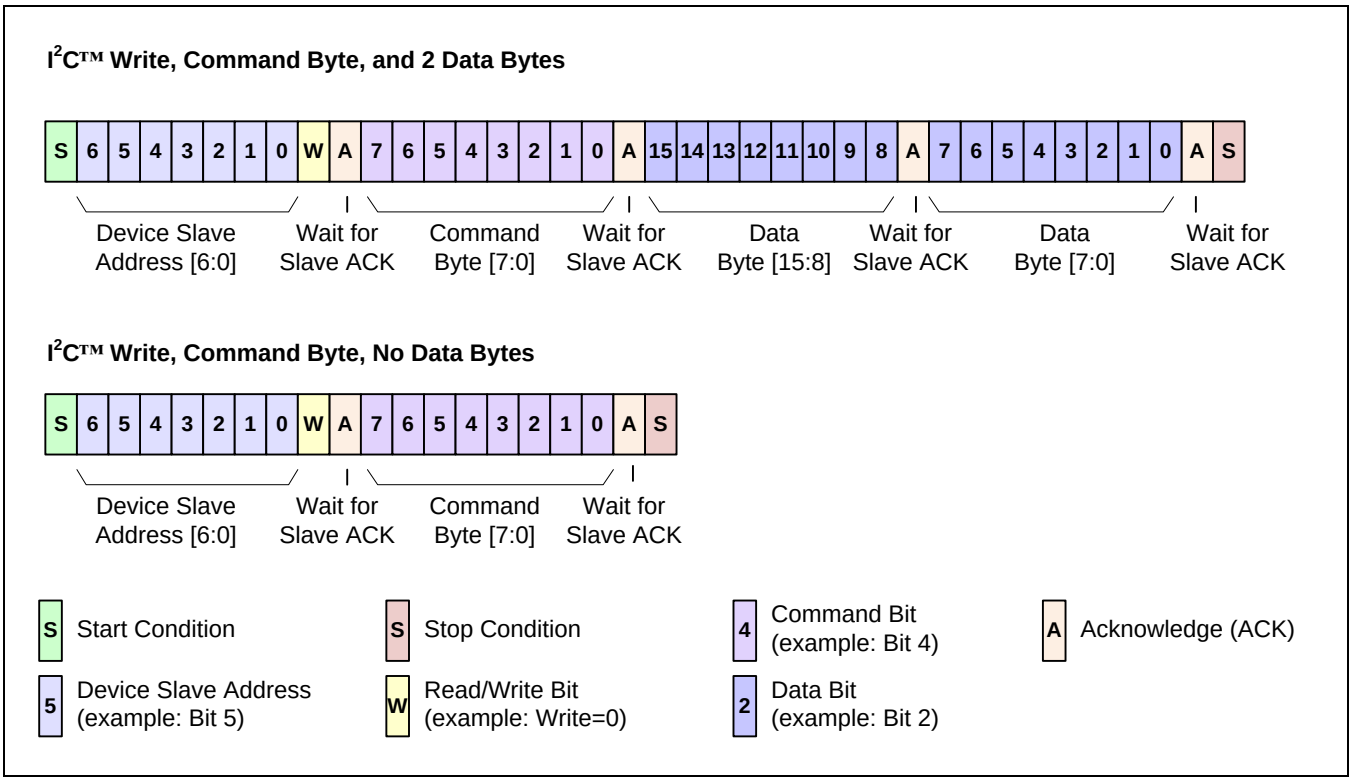
- **Idle Period**
  During inactivity of the bus, SDA and SCL are pulled-up to the supply voltage VDDA.
- **Start Condition**
  A high-to-low transition on SDA while SCL is at the high level indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can always generate a start condition.
- **Stop Condition**
  A low-to-high transition on SDA while SCL is at the high level indicates a stop condition. A command must be closed by a stop condition to start processing the command routine in the ZSC31150.
- **Valid Data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Each byte transmitted is followed by an acknowledge bit. Transmitted bits are valid if after a start condition, SDA remains at a constant level during the high period of SCL. The SDA level must change only when the clock signal at SCL is low.
- **Acknowledge**
  An acknowledge after a transmitted byte is obligatory. The master must generate an acknowledge-related clock pulse. The receiver (slave or master) pulls-down the SDA line during the acknowledge clock pulse. If no acknowledge is generated by the receiver, a transmitting slave will become inactive. A transmitting master can abort the transmission by generating a stop condition and can repeat the command.

  A receiving master must signal the end of the transfer to the transmitting slave by not generating an acknowledge-related clock pulse at SCL.

  The ZSC31150 as a slave changes to inactive interface mode during processing internal command routines started by a previously sent command.

- **Write Operation**
  An I²C™ WRITE operation is initiated by the master sending the slave an address byte including a data direction bit set to '0' (WRITE). The address byte is followed by a command byte and depending on the transmitted command, an additional two data bytes (optional). The ZSC31150 internal microcontroller evaluates the received command and processes the related routine. The following figure illustrates a write command with two data bytes and without data bytes. A detailed description of the command set is given in section 4.1.

Figure 3.2 I²C™ – Write Operation

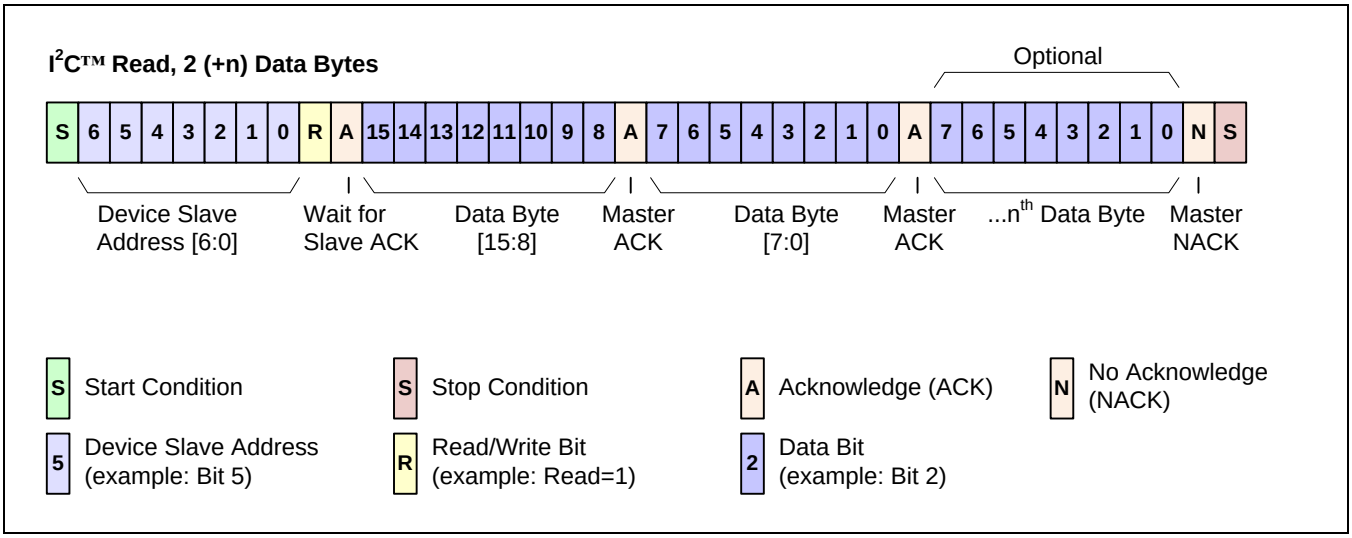


- **Read Operation**
  After a data request from master to slave by sending an address byte including a data direction bit set to '1' (READ), the slave answers by sending data from the interface output registers. The master must generate the transmission clock on SCL, the acknowledges after each data byte (except after the last one), and the stop condition at the end.

  A data request is answered by the ZSC31150's interface module and consequently does not interrupt the current process of the internal microcontroller.

  Note: The data in the activated registers is sent continuously until a stop condition is detected; after transmitting all available data, the slave starts repeating the data.

Figure 3.3 I²C™ – Read Operation – Data Request



During an active measurement cycle, data is constantly updated with conditioning results. To get other data from the slave (e.g., EEPROM content) typically a specific command must be sent before the data request to initiate the transfer of this data to the interface output registers. This command does interrupt the current process of the internal microprocessor and consequently also interrupts an active measurement cycle.

Figure 3.4 I²C™ – Timing Protocol

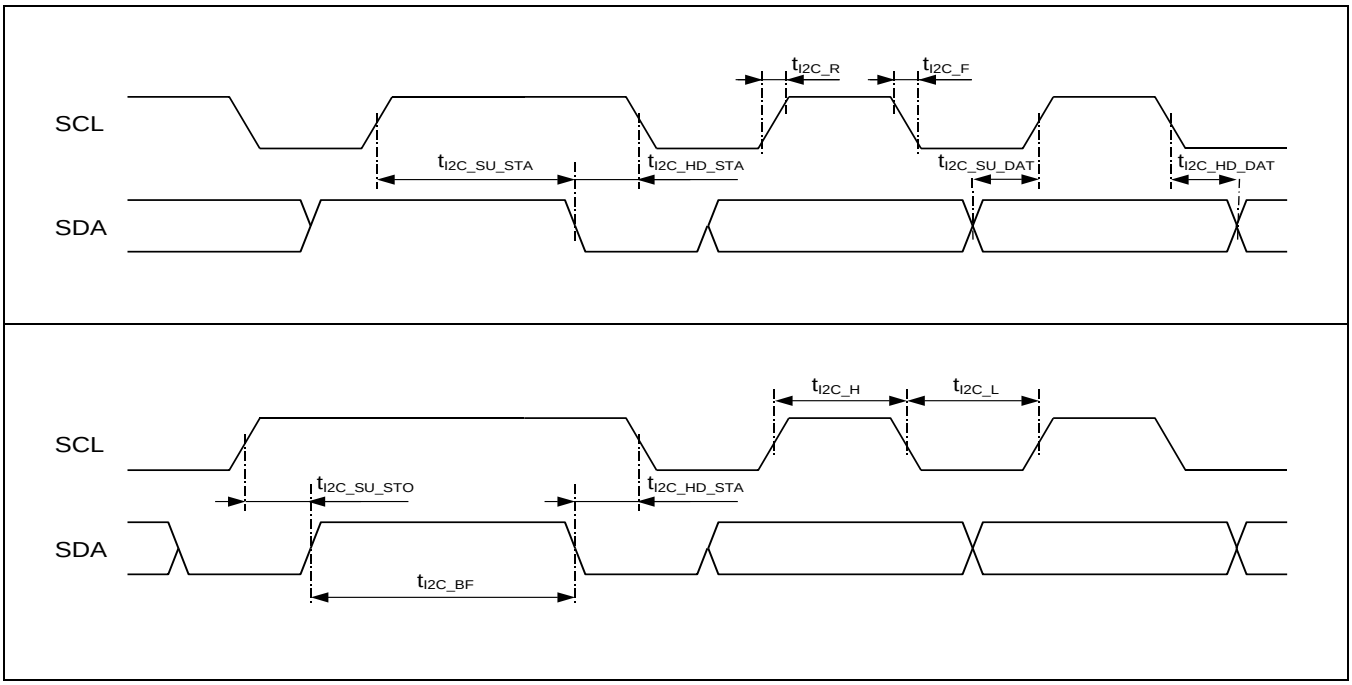


Table 3.1 Timing I²C Protocol

Nr.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1	SCL clock frequency	f_{SCL}	f_{OSC} ≥ 2MHz			400	kHz
2	Bus free time between start and stop condition	t_{I2C_BF}		1.3			µs
3	Hold time start condition	$t_{I2C\_HD\_STA}$		0.6			µs
4	Setup time repeated start condition	$t_{I2C\_SU\_STA}$		0.6			µs
5	Low period SCL/SDA	t_{I2C_L}		1.3			µs
6	High period SCL/SDA	t_{I2C_H}		0.6			µs
7	Data hold time	$t_{I2C\_HD\_DAT}$		0			µs
8	Data setup time	$t_{I2C\_SU\_DAT}$		0.1			µs
9	Rise time SCL/SDA	t_{I2C_R}				0.3	µs
10	Fall time SCL/SDA	t_{I2C_F}				0.3	µs
11	Setup time stop condition	$t_{I2C\_SU\_STO}$		0.6			µs
12	Noise interception SDA/SCL	t_{I2C_NI}	Spike suppression			50	ns

Note: See section 1.4 of the ZSC31150 for additional specifications related to the I²C interface.

3.3. Digital One-Wire Interface (OWI)

The ZSC31150 employs IDT's ZACwire™, a one-wire digital interface concept (OWI). It combines a simple and easy protocol adaptation with a cost-saving pin sharing. The communication principle of the OWI interface is derived from the I²C protocol. Becoming familiar with the I²C protocol is recommended for an understanding of OWI communication.

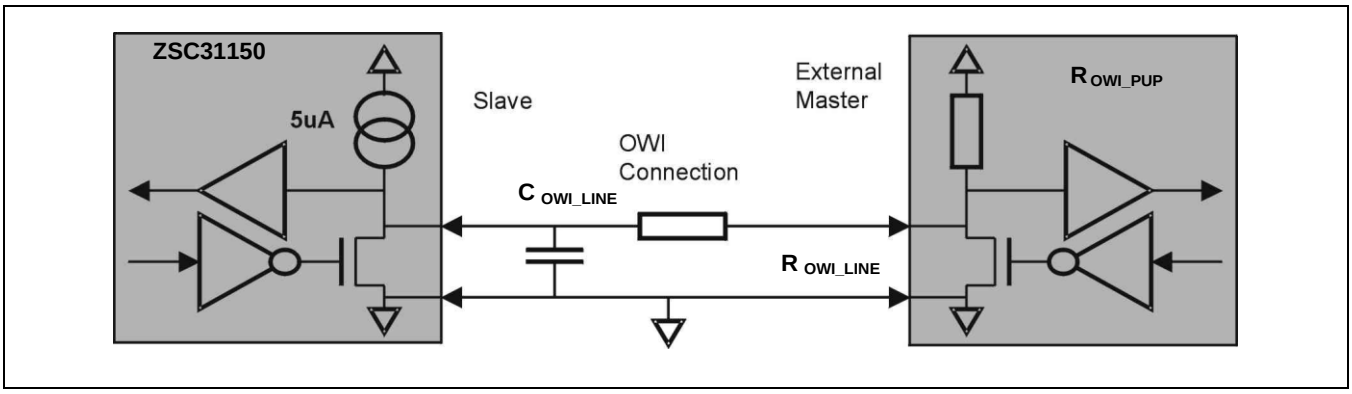
Both the analog voltage output and the digital interface (calibration and/or digital output value) use the same pin, AOUT. An advantage of OWI output signal capability is that it enables “end of line” calibration – no additional pins are required to digitally calibrate a finished assembly. However, although the OWI was designed mainly for calibration, it can also be used to digitally read out the calibrated sensor signal continuously.

These two communication tasks are supported by different configurations of the interface. Depending on the EEPROM configuration (ADJREF:IFOWIM, see Table 5.5), there are 4 different modes for OWI:

- **OWIENA → OWI enabled**
  OWI remains active at the AOUT pin; analog output is disabled.
  (Note: no internal pull-up resistor is implemented.)
- **OWIWIN → OWI startup window**
  OWI is enabled during the startup window (~100ms minimum) and is disabled if the startup window times out without receiving a valid START_CM command [$72D1_{HEX}$]. Analog voltage output is activated after the startup window elapses. (Note: no internal pull-up resistor is implemented).
- **OWIANA → OWI startup window with Analog Out**
  Analog voltage output is activated after startup time (maximum 5ms). OWI is enabled during the startup window (~100ms minimum) and is disabled if the startup window times out without receiving a valid START_CM command [$72D1_{HEX}$]. When sending the START_CM command, the master must overwrite the active analog voltage output (I_{OUT} max = 20mA).
- **OWIDIS → OWI disabled**
  OWI communication is not possible. Access to the ZSC31150 is only available via the I^2C interface.

Figure 3.5 Block Diagram of the OWI Connection

Note: An external pull-up must be provided; no guarantee for usage of the ZSC31150 internal pull-up.



In Command Mode (CM), communication via OWI is possible if OWI is enabled. Typically the ZSC31150 is in the OWIENA mode. After specific commands requesting an analog output at the AOUT pin, the mode is comparable to OWIANA but without a timeout.

Both devices are peers; however only the external device starts communication and requests data. In this sense, it is referred to as the master and the ZSC31150 as slave.

In the case of an invalid EEPROM signature, the lower diagnostic range (LDR) driven at the analog output AOUT pin must be overwritten (I_{OUT} max=20mA) for sending the START_CM command. A push-pull driver is necessary for this. It is possible to overwrite the driven analog output AOUT by a communication sequence if OWI is enabled (refer to the OWI modes described above).

3.3.1.1. Properties and Parameters

Although the OWI is designed as a bilateral connection, for reasons of compatibility, the protocol used is equivalent to I^2C communication. This means a command always includes an address byte with a read/write bit. OWI communication is self-locking (synchronizing) on the master's communication speed within the range specified for OWI bit time, which is guaranteed for ZSC31150's clock frequency in the range of 2 to 4 MHz.

The OWI communication start window in OWIANA and OWIWIN mode is 52700 internal frequency clocks long (~100ms minimum). To initiate OWI communication and enter the Command Mode, the START_CM command must be sent during this period.

Table 3.2 OWI Interface Parameters

Nr.	Parameter	Symbol	Conditions	Min	Max	Unit
1	OWI bit time [1)]	t_{OWI_BIT}	$t_{BIT} = 10 * R_{OWI\_PUP} * C_{OWI\_LOAD}$	0.04	4	ms
2	Pull-up resistance – master	R_{OWI_PUP}		0.3	3.30	kΩ
3	OWI line resistance	R_{OWI_LINE}	$R_{OWI\_LINE} < R_{OWI\_PUP}/100$	20	33	Ω
4	OWI load capacitance	C_{OWI_LOAD}	Total OWI line load		50	nF
5	Voltage level low	$V_{OWI\_IN\_L}$	Minimum VDDA is 4.2V @ 4.5V VDDE		0.2	VDDA
6	Voltage level high	$V_{OWI\_IN\_H}$	Maximum VDDA is 5.5V @ 5.5V VDDE	0.75		VDDA

1) Range is guaranteed independent of the clock frequency adjustment. Also see Table 3.3 for more details.

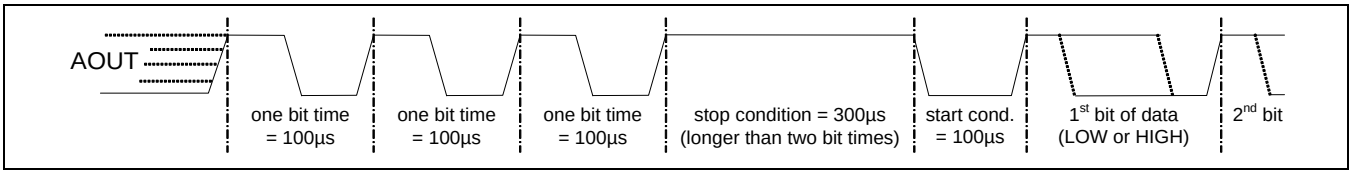
The OWI communication and protocol used is defined as follows:

- **Idle Period**
  During inactivity of the bus, the OWI communication line is pulled-up to the supply voltage VDDA.
- **Start Condition**
  When the OWI communication line is in idle mode, a low pulse (return to one) with a minimum t_{OWI_STA} width of 25µs indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in the idle mode.
- **Stop Condition**
  The master finishes a transmission by changing back to the high level (idle mode). Every command (see the following "Write Operation" section for details) must be closed by a stop condition in order to start processing the command. The master can interrupt a transmitting slave after a data request (refer to "Read Operation" below) by clamping the OWI line to the low level for generating a stop condition.

  A stop condition is indicated by no transition from low to high or from high to low (constant level) at the OWI line for at least twice the period of the last transmitted valid bit or more than the doubled bit time. A stop condition without regard to the last bit-time (secure stop condition) is generated by a constant level at the OWI line for more than 32766 clocks of the internal clock oscillator. A secure stop condition is also generated at bit times less than 80 clocks of the clock oscillator.

  In the case of overwriting an active AOUT (e.g., upon starting communication in OWIANA mode), a stop condition must be generated independently from the current AOUT potential, which can be LOW or HIGH. The timing patterns shown in Figure 3.6 ensure proper generation of the stop condition:

Figure 3.6 OWI – Stop Condition for Active Driven AOUT

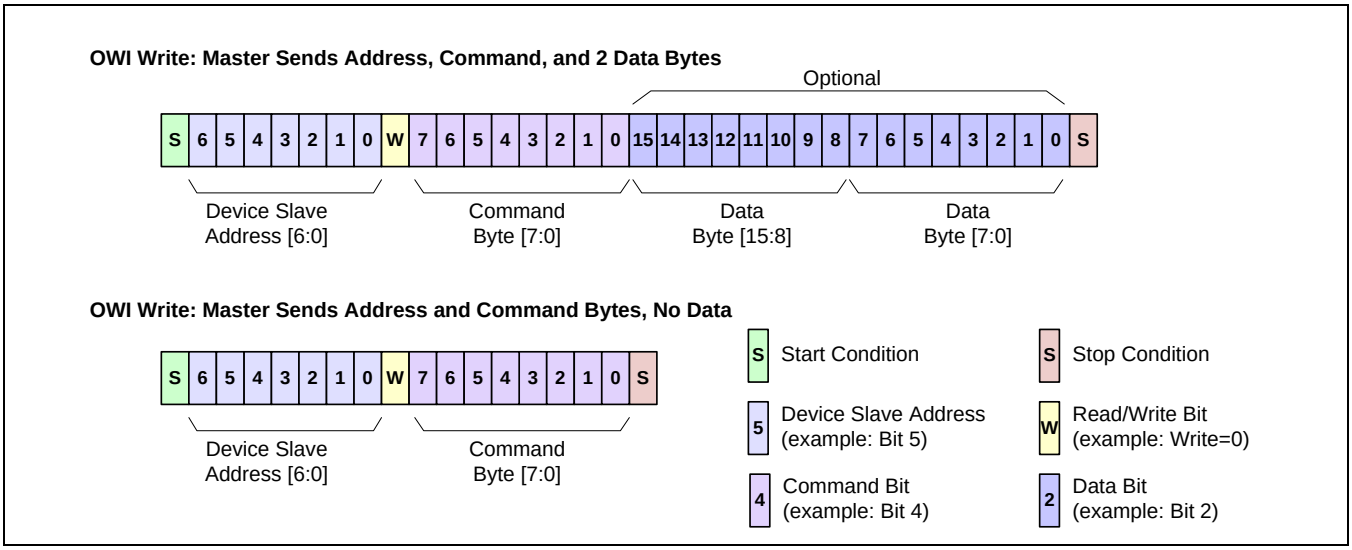


- **Valid Data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high on the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, t_{OWI_BIT}; see Table 3.3). A duty ratio greater than 1/8 and less than 3/8 is detected as a 0; a duty ratio greater than 5/8 and less than 7/8 is detected as a 1.

  The bit period of consecutive bits must not change by more than a factor of 2 because a stop condition is detected in this case.

- **Write Operation**
  An OWI WRITE operation is initiated by the master sending the slave an address byte including a data direction bit set to 0 (WRITE). The address byte is followed by a command byte and depending on the transmitted command, an additional two data bytes (optional). The ZSC31150 internal microcontroller evaluates the command received and processes the related routine. Figure 3.7 illustrates the write of a command with two data bytes and without data bytes. A detailed description of the command set is given in section 4.1.

Figure 3.7 OWI – Write Operation



- **Read Operation**
  After a data request from the master to a slave by sending an address byte including a data direction bit set to 1 (READ), the slave answers by sending data from the interface output registers. The slave generates the data bits with a bit period equal to the last received bit (R/W bit). The master must generate a stop condition after receiving the requested data.

  A data request is answered by the ZSC31150's interface module, so it does not interrupt the current process of the internal microcontroller.

  The data in the output registers is sent continuously until a stop condition is detected; after transmitting all available data, the slave starts repeating the data.

  During the active measurement cycle, data is constantly updated with conditioning results. To get other data from the slave (e.g., EEPROM content) normally a specific command must be sent before the data request to initiate the transfer of this data to the interface output registers. This command does interrupt the present operation of the internal microcontroller and consequently also interrupts any active measurement cycle.

Figure 3.8 OWI – Read Operation – Data Request

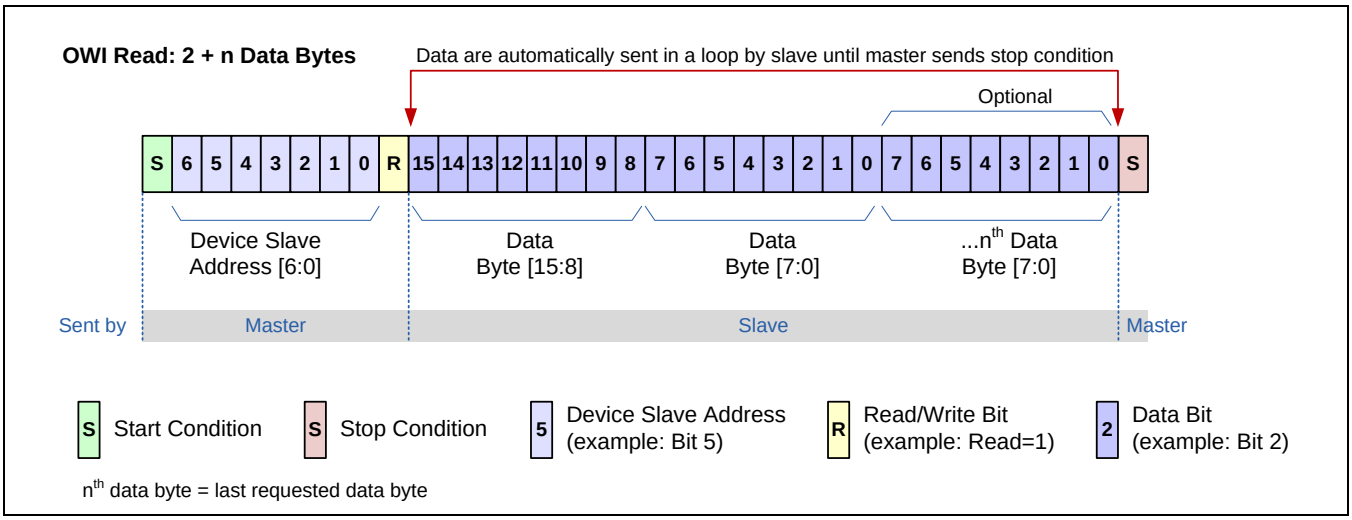


Figure 3.9 OWI – Timing Protocol

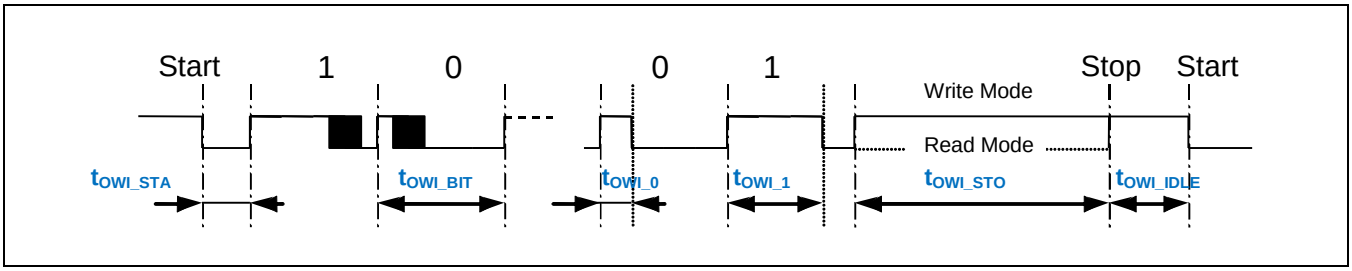


Table 3.3 OWI Timing Protocol

Nr.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1	Bus free time	t_{OWI_IDLE}	Between start and stop	25			µs
2	Hold time start condition [1)]	t_{OWI_STA}		25			µs
3	Bit period range [2)]	t_{OWI_BIT}	f_{OSC} = 4MHz (min.); 2MHz (max.)	20		8000	µs
4	Duty ratio bit ‘0’	t_{OWI_0}		0.125	0.25	0.375	t_{OWI_BIT}
5	Duty ratio bit ‘1’	t_{OWI_1}		0.625	0.75	0.875	t_{OWI_BIT}
6	Hold time stop condition	t_{OWI_STO}	Minimum t_{OWI_BIT} (20ms) to bit period of last valid bit (Also see “Stop Condition” on page 19 for further details.)	2.0			$t_{OWI\_BIT\_L}$
7	Bit period deviation	$t_{OWI\_BIT\_DEV}$	Current bit to next bit	0.55	1.0	1.5	t_{OWI_BIT}

1) This hold time is valid for all frequency adjustments for the ZSC31150.
2) This bit period range is achievable with different frequency adjustments. OWI communication is always possible in the OWI bit time specified in Table 3.2.

4 Interface Commands

4.1. Command Set

All commands are only available in Command Mode (CM) (see section 1.3.2) and for I^2C and OWI communication. CM is initiated by sending the START_CM command [$72D1_{HEX}$]. See Table 4.1 for command descriptions and processing time.

In CM, every command received is answered. The response consists of the two bytes of requested data or validation code, 1 byte for the check sum, and the 1-byte command reply. For more details about responses, see sections 4.3 and 4.4.

Important: Before sending commands that write to EEPROM registers, EEPROM programming must be enabled by sending the EEP_WRITE_EN command $6CF742_{HEX}$.

A read command can be sent during an active measurement cycle (i.e., the processing time has not yet elapsed after sending one of the STRT_CYC_x or START_AD_x commands indicated by gray shading in Table 4.1). For example, the SIF can be read during the START_AD_CNT command. If any of the other commands is to be sent during an active measurement cycle, the measurement command must first be aborted. Typically an active measurement cycle is aborted if a non-read command is received, but in special cases, the command might not be received correctly and the active measurement is not aborted. Therefore, for safe communication during an active measurement cycle, IDT recommends sending the START_CM command [$72D1_{HEX}$] first for non-read commands.

Table 4.1 Command Set

Command (HEX)	Data	Command	Notes	Processing Time @ f_{CLK}=3MHz
01 / 02		STRT_CYC_EEPOWI / STRT_CYC_RAMOWI	Start measurement cycle including initialization from EEPROM/RAM for digital output with activation of OWI mode OWIENA.	350µs / 220µs
03 / 04		STRT_CYC_EEPANA / STRT_CYC_RAMANA	Start measurement cycle including initialization from EEPROM/RAM for analog output with activation of OWI mode OWIANA.	350µs / 220µs
05 / 06		STRT_CYC_EEPOWIDIS / STRT_CYC_RAMOWIDIS	Start measurement cycle including initialization from EEPROM/RAM for digital output with OWI mode disabled (OWIDIS mode).	350µs / 220µs
07 / 08		STRT_CYC_EEP / STRT_CYC_RAM †	Start measurement cycle including initialization from EEPROM/RAM. **Note for OWIWIN and OWIANA:** OWI communication is disabled after the startup window).	350µs / 220µs
10 to 1E		READ_RAM	Read data from RAM address 00_{HEX} to $0E_{HEX}$.	50µs
30 to 43		READ_EEP	Read data from EEPROM address 00_{HEX} to 13_{HEX}.	50µs
50		ADJ_OSC_ACQ	Acquire frequency ratio of internal oscillator to communication frequency (f_{OSC} / f_{OWI}) for adjusting internal oscillator frequency by ADJREF:OSCADJ. **Important:** Use this command only with OWI communication.	50µs
60	2 Bytes	SET_DAC	Set analog output (DAC) to value defined by data bytes. Important note: If the data byte is outside the allowed range of 0100_{HEX} to $14FF_{HEX}$, the ZSC31150 will enter DM and output the LDR (lower diagnostic range). The AOUT pin goes into tri-state during processing.	40µs

† Note: For product versions ZSC31150Exx and earlier, the commands STRT_CYC_EEP and STRT_CYC_RAM are not available.

Command (HEX)	Data	Command	Notes	Processing Time @ f_{CLK}=3MHz
62	2 Bytes	START_AD_CNT	Process an A/D conversion <n> (= data) times for input voltage and temperature, auto-zero corrected. Result is updated continuously in digital output registers (4 data bytes), last values remain after processing. See 4.5.1 for details.	<n>∗ (D8+D9) commands
65	2 Bytes	ADJ_OSC_WRI	Write and activate oscillator adjust value to RAM ADJREF:OSCADJ, returns compete configuration word ADJREF. **Important:** Use this command only with OWI communication	50µs
6C	2 Bytes	EEP_WRITE_EN	Enable data write to EEPROM when sent with data $F742_{HEX}$; sending any other data disables EEPROM writing.	50µs
72	1 Byte	START_CM	Start Command Mode (CM); always send with data $D1_{HEX}$.	50µs
80 to 8E	2 Bytes	WRITE_RAM	Write data to RAM addresses 00_{HEX} to $0E_{HEX}$ respectively.	50µs
A0 to B2	2 Bytes	WRITE_EEP	Write data to EEPROM addresses 00_{HEX} to 12_{HEX} respectively.	12.5ms
C0		COPY_EEP2RAM	Copy the content of EEPROM addresses 00_{HEX} to $0E_{HEX}$ to RAM; restores EEPROM configuration in RAM.	130µs
C3		COPY_RAM2EEP	Copy the content of RAM addresses 00_{HEX} to $0E_{HEX}$ to EEPROM; generates the EEPROM signature and writes it to address $0F_{HEX}$, returns the EEPROM signature.	200ms
C8		GET_EEP_SIGN	Calculates EEPROM signature and writes the result to SIF output register 1 (SIF1; see Table 4.2).	150µs
C9		GEN_EEP_SIGN	Calculates EEPROM signature and writes it to EEPROM address $0F_{HEX}$ and writes the result to SIF1.	12.6ms
CA		GET_RAM_SIGN	Calculates RAM signature and writes the result to SIF1.	150µs
CF		ROM_VERSION	Get hardware and ROM version: • ROM version is defined by the low byte “CF” command answer. • Design version is defined by the high byte “CF” command answer. ZSC31150Axx = $0Axx_{HEX}$ ZSC31150Exx = $0Exx_{HEX}$ ZSC31150Cxx = $0Cxx_{HEX}$ ZSC31150Fxx = $0Fxx_{HEX}$ ZSC31150Dxx = $0Dxx_{HEX}$ ZSC31150Gxx = $19xx_{HEX}$	50µs

Note: All Dx commands are used for the calibration process, write raw conversion result to SIF output registers, and do not generate analog output. Processing time with f_{CLK}=3MHz for D0-D6 commands is 150 clock cycles (approximately 50µs) + A/D conversion time. The processing time is 2 times this value for the D8 to DB commands.

Note: Enabling the A/D converter clock divider (i.e., bit CFGAFE:ADCSLOW is set to 1) doubles only the A/D conversion time.

Command (HEX)	Command	Notes
D0	START_AD_BR	Start cyclic A/D conversion at bridge sensor channel (BR); e.g., pressure measurement.
D1	START_AD_T	Start cyclic A/D conversion at temperature channel (T).
D2	START_AD_SSCP	Start cyclic A/D conversion for positive-biased Sensor Short Check and Sensor Connection Check.
D3	START_AD_CMV	Start cyclic A/D conversion for common mode voltage measurement for Sensor Aging Check.
D4	START_AD_BR_AZ	Start cyclic A/D conversion auto-zero (AZ) at bridge sensor channel (BR); e.g., pressure
D5	START_AD_TAZ	Start cyclic A/D conversion auto-zero at temperature channel (TAZ).

Command (HEX)	Command	Notes
D6	START_AD_SSCN	Start cyclic A/D conversion for negative-biased Sensor Short Check and Sensor Connection Check.
D8	START_AD_BR_AZC	Start cyclic A/D conversion at bridge sensor channel (BR) including auto-zero.
D9	START_AD_T_AZC	Start cyclic A/D conversion at temperature channel (T) including auto-zero.
DA	START_AD_SSCP-SSCN	Start cyclic A/D conversion for positive and negative biased Sensor Short Check and Sensor Connection Check.
DB	START_AD_CMV_AZC	Start cyclic A/D conversion for common mode voltage measurement (for Sensor Aging Check) including auto-zero.

4.2. Command Processing

All commands are available for both I^2C and OWI protocols (except ADJ_OSC_ACQ and ADJ_OSC_WRI). If CM is active, reception of a valid command interrupts the internal microcontroller (CMC) and starts a routine processing the received command. The processing time depends on the internal system clock frequency (minimum: ~2MHz; adjustable by EEPROM programming). For a data read from the ZSC31150, the requested data (e.g., register content or acquired measurements) is written to the SIF output register and can be read out by a read request.

Commands sent while a previously sent command has not yet executed completely will be ignored. The ZSC31150 releases the interface while a running and valid I²C™ communication takes place (i.e., a start condition of an I²C™ communication has already occurred). If the ZSC31150 does not detect a start condition, it will not provide the ACK to the address byte.

4.3. SIF Output Registers

The serial interface (SIF) contains two 16-bit output registers that can be read out by a read request. Depending on the configuration of ADJREF:IFOWIM, access to the one-wire interface (OWI) can be limited during NOM. Depending on the present operation mode of ZSC31150 (NOM, CM or DM; refer to section 1.3), different data are written to SIF output registers. The output registers SIF1 and SIF2 are continuously updated.

Note: If the update rate is high, a check sum error might occur if data is read out in NOM during an active measurement cycle or during CM for all calibration commands (e.g., the START_AD_CNT command). Refer to the *ZSC31150 Data Sheet* and the *ZSC31150 Bandwidth Calculation Spreadsheet* for more details about the update rate. The data readout occurs word-by-word. Therefore it is possible that during reading the first word (SIF1), the output register is updated with a new conditioned value and thus the check sum is also updated. The check sum value for the new conditioned value is read out within the next word (SIF2). The new conditioned value could have a different check sum value than was read out as the first word and so an apparent check sum error is detected.

Recommendation: To prevent such misinterpretation in these cases, read at least 6 bytes as shown below in Figure 4.1. If an invalid check sum is detected in the first four bytes, the second SIF1 reading can be used to check whether a misinterpretation of the check sum has occurred or a check sum error occurred. The reading of the 6 bytes must be faster than the update rate of the measurand data at SIF1.

Figure 4.1 Preventing Misinterpretation of Check Sum

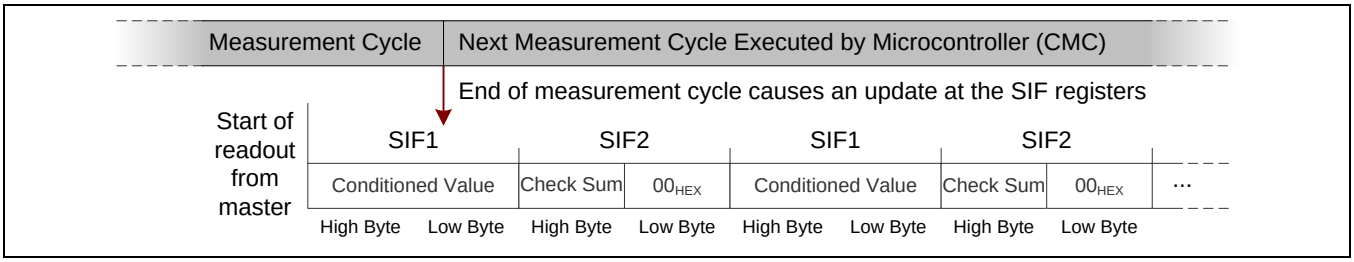


Table 4.2 Output Register Contents of Serial Digital Interface (SIF) When Processing Commands

Mode/ Commands	Output Register 1 (SIF1)		Output Register 2 (SIF2)	
	High Byte	**Low Byte**	**High Byte**	**Low Byte**
Normal Operation Mode (NOM)				
	Conditioned value: <error flag(MSB)> <15-bit data>		Check sum	00_{HEX}
Command Mode (CM)				
Read RAM or EEP (Commands 10_{HEX} to $1E_{HEX}$ and 30_{HEX} to 43_{HEX}).	Requested RAM or EEP data		Check sum	Processed command
START_AD_xx (Dx_{HEX} commands)	Measured raw value		Check sum	Processed command ‡
START_AD_CNT (Command 62_{HEX})	Measured raw value (e.g., pressure)		Measured raw value temperature	
STRT_CYC_xx (01_{HEX} to 08_{HEX})	Conditioned value => refer to NOM			
Commands without output	Success code $C3xx_{HEX}$; see Table 4.3		Check sum	Processed command
SET_DAC (Command 60_{HEX})	DAC adjustment data		Check sum	60_{HEX}
ADJ_OSC_ACQ (Command 50_{HEX})	Oscillator adjustment count		Check sum	50_{HEX}
ADJ_OSC_WRI (Command 65_{HEX})	The new configuration word ADJREF		Check sum	65_{HEX}
Diagnostic Mode (DM)				
	Error code $C0xx_{HEX;}$ MSB = error flag = 1		Check sum	00_{HEX}

The check sum is calculated using the following formula: check sum = FF_{HEX} – (high byte + low byte).

‡ For product versions ZSC31150Dxx and earlier, the value 00_{HEX} was sent in place of the processed command.

4.4. Command Response Codes

In CM, every command received is answered with either data or a success/failure code. Table 4.3 gives the codes for the first word of the response to commands. The high byte of the second word contains the check sum and the low byte repeats the processed command.

Table 4.3 Command Response: First Readout Word (SIF Output Register 1)

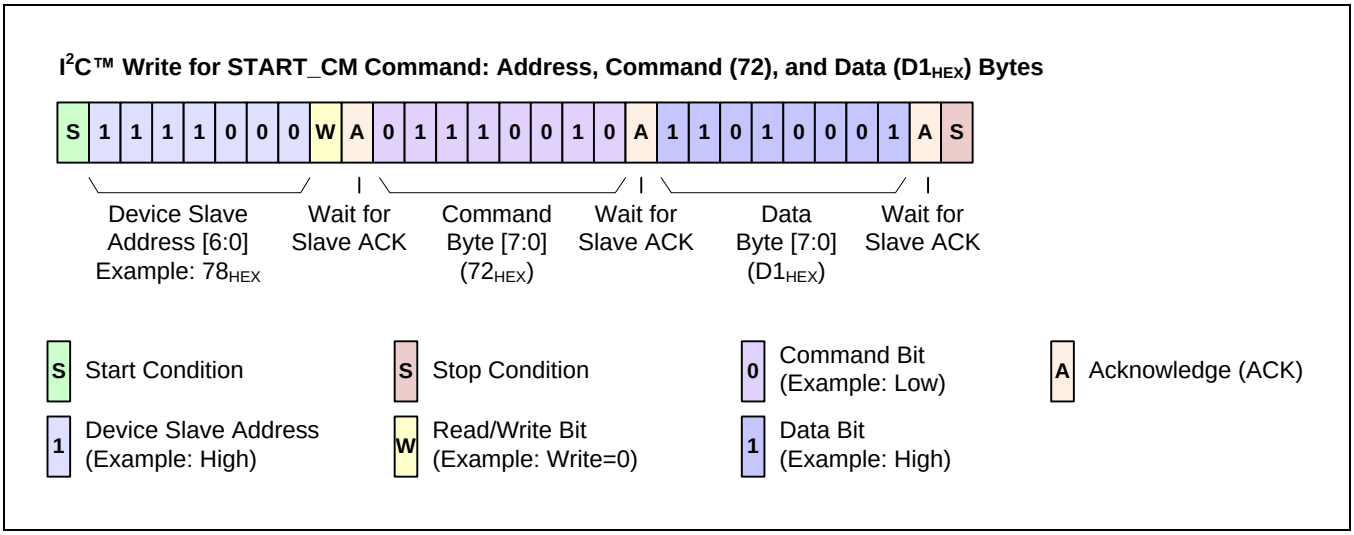
Command	Success Code	Failure Detected Code	Notes
6C $F742_{HEX}$	$C36C_{HEX}$	$CF6C_{HEX}$	Charge pump enable in order to write data to EEPROM
72 $D1_{HEX}$	$C372_{HEX}$		Start Command Mode
$C0_{HEX}$	$C3C0_{HEX}$		Copy EEP to RAM
$C3_{HEX}$	$C3C3_{HEX}$	$CFC3_{HEX}$	Copy RAM to EEP
xy	-	$CF00_{HEX}$	Wrong command or data missing
xy	-	$C000_{HEX}$	Command processing error or undefined internal error
Commands that initiate NOM		$C0xx_{HEX}$ where $xx \neq 00$	$C0xx_{HEX}$ indicates the Diagnostic Mode; see Table 1.1 (if the DM is “temporary,” then the measurement cycle continues)

4.5. Detailed Description for Specific Commands

4.5.1. START_CM ($72D1_{HEX}$)

As described in section 1.3.1, the ZSC31150 starts in NOM. In this mode, it continuously measures the input signal and refreshes the SIF. To start the Command Mode, a START_CM command via I²C™ must be transmitted to the ZSC31150. This command is shown in Figure 4.2.

Figure 4.2 START_CM Command



When sending the START_CM command to abort the NOM or a raw data acquisition command (Dx_{HEX}), the command execution can be affected by the internal asynchronous processed update of the SIF output register. In this case, the received command could be overwritten and therefore the Command Mode would not be entered. This event can only happen between two clock cycles of the ZSC31150 oscillator. Checking the response to the START_CM command to ensure that CM was started is recommended. If the ZSC31150 answers with $C372_{HEX}$, entering CM was successful; otherwise, send the START_CM command again. Timing between sending the first and second Start_CM should not be equal to the ADC conversation time (refer to the *ZSC31150 Bandwidth Calculation Spreadsheet)*. A timing of half of the known ADC conversion time can be used when tolerances of the oscillator should be taken in account or the oscillator calibration procedure has been performed (described in section 4.5.3).

Depending on internal conditions, if the secondary SIF address is used for communication, it is possible that the ZSC31150 will not answer communication requests from that point forward. If this occurs, use the primary I^2C address (78_{HEX}) for restarting the ZSC31150 with a START_CM command and then the secondary address will be functional again.

4.5.2. START_AD_CNT (62_{HEX})

The START_AD_CNT command is used for synchronized bridge sensor (the measurand; e.g., pressure) and temperature raw calibration data acquisition during the calibration process. The possible synchronization enables a raw data acquisition (snapshot) for all attached devices under test (DUTs) under temperature drift and measurand leakage conditions, which is especially useful for mass calibration.

Two data inputs are evaluated and required for processing of the START_AD_CNT command:

- Average count (cavg) for calibration based on the PAVG bits [2:0] in register 08_{HEX}: $\langle cavg \rangle = 2^{\langle PAVG \rangle}$
- Conversion cycle count <cccnt> to be processed (recommendation: $\langle cccnt \rangle = 2^{\langle PAVG \rangle} + 8$)

All necessary A/D conversions (measurand, temperature, auto-zero) are cyclic. For the A/D conversions, the START_AD_CNT command implements the following Dx commands in this sequence:

- D5, D1 (for temperature measurand), which is equivalent to the $D9_{HEX}$ command (T_AZC = T - TAZ)
- D4, D0 (for bridge sensor measurand), which is equivalent to the $D8_{HEX}$ command (BR_AZC = BR - BR_AZ).

The two data bytes attached to the START_AD_CNT command define the count of conversion cycles <cccnt>. The A/D conversion is stopped after processing the required count of conversion cycles.

Table 4.4 START_AD_CNT – Data Word Description

Bit#	data <15:0>
Description	Conversion cycle count <cccnt> to be processed

During A/D conversion, the SIF output registers are continuously updated, so temporary results can be read out during processing the command and the result is valid after processing the last conversion. The time needed for this can be estimated by following formula:

$$\text{readout\_delay} = \langle \text{AD conversion time} \rangle * \left[\left(4.1 * \langle \text{cccnt} \rangle \right) + 1 \right]$$

After the command is processed, the last or averaged result is readable in the SIF output registers until the next command. The averaged value is calculated using the filter formula (refer to section 2.5) with PDIFF = 0 and PAVG = $\log_2$ <cavg> and $Pout_{n-1} = Pout_n$.

Table 4.5 START_AD_CNT – Command Response Description

Command	SIF1	SIF2
START_AD_CNT	Bridge Sensor Measurand BR_AZC	Temperature T_AZC

4.5.3. ADJ_OSC_ACQ (50_{HEX}) and ADJ_OSC_WRI ($65xxxx_{HEX}$)

The ADJ_OSC_xxx commands are used to adjust the frequency of the internal oscillator. This frequency is adjustable in the range of 2 to 4 MHz and has a directly proportional effect on the A/D conversion time. The internal oscillator frequency can be adjusted by ADJREF:OSCADJ (see section 5.2). The default value 12_{HEX} corresponds to a frequency of 3MHz. The frequency is changed per count by a step of approximately **-**125kHz (frequency is decreased if OSCADJ is increased).

The ADJ_OSC_ACQ command is sent first. Note: This command works ***only with ZACwire™ communication*** (OWI). It returns the ratio of the internal oscillator frequency to the communication frequency f_{OSC}/f_{OWI}. Since the communication frequency f_{OWI} is known, the current internal oscillator frequency f_{OSC} can be calculated. Note that the resolution of the frequency measurement improves as the communication frequency decreases.

The change in ADJREF:OSCADJ needed to reach the target frequency can be calculated from the ratio f_{OSC}/f_{OWI} and the adjustment of -125kHz/step. The ADJ_OSC_WRI command is used to write the ADJREF:OSCADJ to RAM and to activate the new adjustment. The command returns the complete configuration word ADJREF (all other configuration bits keep their value).

This sequence allows an easy and accurate adjustment of the internal frequency during end-of-line calibration.

Table 4.6 Oscillator Frequency Adjustment Sequence / Tasks (OWI Only)

Communication	Command Description	Comment
Task: Measure and adjust the internal frequency		
[72 D1]	START_CM	Start command mode
[1D]	READ_RAM 0xD	Read RAM ADJREF
[SIF-READ]	READ ADJREF	Read ADJREF; OSCADJ = ADJREF[4:0]
[50]	ADJ_OSC_ACQ	Acquire frequency ratio of internal oscillator to communication frequency
[SIF-READ]	READ F_RATIO	Read F_RATIO = f_{OSC}/f_{OWI} or f_{OSC} = F_RATIO*f_{OWI} $D\_OSCADJ = \frac{f_{OSC,new} - F\_RATIO * f_{OWI}}{-125kHz}$ OSCADJnew = OSCADJ + D_OSCADJ
[65 OSCADJnew]	ADJ_OSC_WRI	Write ADJREF:OSCADJ
[SIF-READ]	READ ADJREF	Read ADJREFnew
Task: Check the resulting internal frequency (optional)		
[50]	ADJ_OSC_ACQ	Acquire frequency ratio of internal oscillator to communication frequency
[SIF-READ]	READ F_RATIO	Read F_RATIO
Task: Write the new frequency adjustment to EEPROM		
[6C F742]	EEP_WRITE_EN	Enable data write to EEPROM
[AD ADJREFnew]	WRITE_EEP	Write EEPROM ADJREFnew
[C9]	GEN_EEP_SIGN	Generate and write EEPROM signature

5 EEPROM and RAM

5.1. Programming the EEPROM

Programming the EEPROM is done using an internal charge pump to generate the required programming voltage. The timing of the programming pulses is controlled internally. The programming time for a write operation is typically 12.5ms independent of the programmed clock frequency (ADJREF:OSCADJ). Recommendation: Wait at least 15ms per write operation before starting the next communication.

To program the EEPROM, it is necessary to set the ZSC31150 in Command Mode via the START_CM command (72 $D1_{HEX}$) and to enable EEPROM programming via the EEP_WRITE_EN command (6C F7 42_{HEX}). Writing data to the EEPROM is done via the serial digital interface by sending specific commands (refer to section 4). The WRITE_EEP command includes the address of the targeted EEPROM word and is followed by two data bytes. During EEPROM programming, the serial digital interface is disabled so that no further commands can be recognized.

The COPY_RAM2EEP command writes the content of the RAM mirror area to the EEPROM. This is to simplify the calibration process when the ZSC31150 is configured iteratively. The EEPROM signature, which is not mirrored in RAM is generated, written to EEPROM, and returned to the SIF output register. This copy operation includes 16 EEPROM write operations and therefore typically requires 200ms (recommended wait time: 250ms).

5.2. EEPROM and RAM Content

The configuration of the ZSC31150 is stored in 20 EEPROM 16-bit words.

Calibration constants for conditioning the sensor signal by the conditioning calculation and analog output limits are stored in 11 words. There are three words for setting the configuration of the ZSC31150 regarding the application. One register is used for storing the EEPROM signature, which is used in NOM to check the validity of the EEPROM content after power-on. Three additional 16-bit words are for arbitrary free user data.

After every power-on, the EEPROM content is mirrored to RAM. During this readout, the content of the EEPROM is checked by calculating the signature and comparing it with the stored one. If a signature error is detected, the ZSC31150 starts in DM. In this case, the LDR is driven at the analog output and the OWI interface is activated. The error code is send to the SIF output register.

The configuration of the device is done from the mirrored area in RAM. Therefore the configuration words are transferred to the internal registers. The calibration constants for the conditioning calculation are also read from RAM. Thus every change to the RAM mirror area impacts the configuration and functioning of the device after the next start of cyclic measurement.

After power-on, the content of the RAM mirror area is determined by the EEPROM content and can then be changed by specific commands writing to RAM. A new configuration can be activated by the STRT_CYC_RAMx commands or START_AD_x commands. See Table 5.1 for the EEPROM and RAM contents.

Note: The ZSC31150 is delivered with default contents in the registers. The specified default configuration can be changed. Registers' content must be rewritten completely during the calibration procedure. At delivery, registers 10_{HEX}, 11_{HEX}, and 12_{HEX} contain traceability data (lot#, wafer#, and device#; refer to section 5.2.1 for details). Register 13_{HEX} contains variable IDT internal data at delivery. IDT recommends logging of registers 10_{HEX} to 13_{HEX} data in the calibration log.

Table 5.1 EEPROM and RAM Content

EEPROM/RAM Address	Write Command RAM/EEP	Default Configuration	Description (Note: when bits are divided, the description begins with MSB and ends with LSB)
Conditioning Coefficients – Correction formula for bridge sensor measurand (see section 2.2)			
00_{HEX}	$80/A0_{HEX}$	1000_{HEX}	**c0** - Offset
01_{HEX}	$81/A1_{HEX}$	4000_{HEX}	**c1** - Gain
02_{HEX}	$82/A2_{HEX}$	0000_{HEX}	**c2** - Non-linearity, 2nd order
03_{HEX}	$83/A3_{HEX}$	0000_{HEX}	**c3** - Non-linearity, 3rd order
04_{HEX}	$84/A4_{HEX}$	0000_{HEX}	**c4** - Temperature coefficient offset, 1st order
05_{HEX}	$85/A5_{HEX}$	0000_{HEX}	**c5** - Temperature coefficient offset, 2nd order
06_{HEX}	$86/A6_{HEX}$	0000_{HEX}	**c6** - Temperature coefficient gain, 1st order
07_{HEX}	$87/A7_{HEX}$	0000_{HEX}	**c7** - Temperature coefficient gain, 2nd order
Conditioning Coefficients – Limit and/or filter the analog output at pin AOUT (see section 2.5 and 2.6)			
08_{HEX}	$88/A8_{HEX}$	0800_{HEX}	13 bits: **Lmin** - Lower limit for analog output via pin AOUT 3 bits (LSB): **PAVG** - Output low-pass filter (LPF) averaging coefficient PAVG
09_{HEX}	$89/A9_{HEX}$	$A7F8_{HEX}$	13 bits: **Lmax** - Upper limit for analog output via pin AOUT 3 bits (LSB): **PDIFF** - Output LPF differential coefficient PDIFF
Common Mode Voltage Measurement (CMV) Limits			
$0A_{HEX}$	$8A/AA_{HEX}$	$FF00_{HEX}$	8 bits: **CMVmax** – Upper limit common mode voltage 8 bits (LSB): **CMVmin** – Lower limit common mode voltage
Configuration Words (see section 5.2.2)			
$0B_{HEX}$	$8B/AB_{HEX}$	0013_{HEX}	CFGAFE: Configuration of analog front-end
$0C_{HEX}$	$8C/AC_{HEX}$	0458_{HEX}	CFGAPP: Configuration of target application
$0D_{HEX}$	$8D/AD_{HEX}$	2112_{HEX}	ADJREF: Adjustment of system, communication settings, etc.
$0E_{HEX}$	$8E/AE_{HEX}$	0000_{HEX}	RSVD: Reserved
Calculated Signature based on register 00_{HEX} to $0E_{HEX}$ data			
$0F_{HEX}$	$- /AF_{HEX}$	$6F8C_{HEX}$	Signature
Application Free Memory *(not included in signature)*			
10_{HEX}	$- /B0_{HEX}$	xxx	Free user memory, not included in signature
11_{HEX}	$- /B1_{HEX}$	xxx	Free user memory, not included in signature
12_{HEX}	$- /B2_{HEX}$	xxx	Free user memory, not included in signature
13_{HEX}	$- /B3_{HEX}$	xxx	No customer access; IDT restricted use

5.2.1. Traceability

IDT can guarantee the EEPROM contents for packaged parts only; at delivery of bare dice, the EEPROM content might be changed by flipped bits because of electrostatic effects, which could occur during the wafer sawing.

The ZSC31150 contains three 16-bit registers reserved for user data; e.g., for an ID number. There are no restrictions for the content of these registers 10_{HEX} / 11_{HEX} / 12_{HEX}; they can be read via I^2C at any time.

When using ZACwire™ communication (OWI),

- READ is possible if ZACwire™ communication is enabled
- WRITE is possible if the EEPROM lock is disabled
- WRITE is possible if an EEPROM error (wrong signature or multi-bit error) is detected

During final test, IDT writes the following manufacturing data to these registers:

- **Register 10_{HEX}:** bits 15:0 = lot number part 1 (MSB section
- **Register 11_{HEX}:** bits 15:5 = lot number part 2 (LSB section) / bits 4:0 = wafer number
- **Register 12_{HEX}** bits 15:8 = wafer x-position / bits 7:0 = wafer y-position

Table 5.2 Lot, Wafer, x-Position, and y-Position Number Calculation Procedure

```
temp      = reg0x10 * 2048 + (reg0x11&0xFFE0)/32;
lotNbr    = NumberConvert(temp, BASE); // BASE = 36
waferNbr  = reg0x11&0x1F;
xpos      = reg0x12&0xFF00)/256;
ypos      = reg0x12&0x00FF;
```

IDT recommends saving these data in the calibration log to identify the device in the event that RMA processing is needed.

Register 13_{HEX} is used by IDT to store logistic data and internal information. It can be written by IDT via test equipment only; the user cannot write data to this register.

5.2.1.1. EEPROM Error Correction

The EEPROM data are stored with HAMMING DISTANCE = 3, which means

- 100% detection and correction of 1-bit errors
- 100% detection of 2-bit errors

The detection of multi-bit errors (>2 bit) is processed at a lower detection rate.

5.2.2. Configuration Words

The data stored in RAM and EEPROM in the registers at addresses $0B_{HEX}$ to $0E_{HEX}$ determine the configuration of the ZSC31150 as described in the following tables.

Table 5.3 Configuration Word CFGAFE

Bit	Default at Delivery	CFGAFE - Configuration of analog front-end	EEPROM/RAM Address $0B_{HEX}$
15	0_{BIN}	Bridge sensor (e.g., **P**ressure) channel e**X**tended **Z**ero **C**ompensation **POL**arity (offset compensation by analog front-end; refer to section 2.1) 0: negative – compensates positive offsets 1: positive – compensates negative offsets	PXZCPOL
14:10	$0\ 0000_{BIN}$	Bridge sensor (e.g., **P**ressure) channel e**X**tended **Z**ero **C**ompensation value (offset compensation by analog front-end; refer to section 2.1) Offset compensation is only active if PXZC ≠ 0. The value of one compensation step depends on the selected input span.	PXZC
9:6	0000_{BIN}	Bridge sensor (e.g., **P**ressure) channel **GAIN** (a_{IN}; refer to section 2.1) 0000: 420 0101: 70 1001: 14 0001: 280 0110: 52.5 1010: 9.3 0010: 210 0111: 35 1011: 7 0011: 140 1000: 26.25 11dd: 2.8 0100: 105	PGAIN
5	0_{BIN}	Enable **AD C**onverter clock divider Influences only the internal frequency of the A/D conversion. Integration time is doubled to enhance the conversion result quality (less noise, better linearity). 0: $f_{ADC} = f_{CLK}$ 1: $f_{ADC} = f_{CLK} / 2$	ADCSLOW
4:3	10_{BIN}	**AD C**onversion input **R**ange **S**hift for measured signal (RS_{ADC}; see section 2.1) 00: $^{15}/_{16} \Rightarrow$ ADC range = [(–1/16 V_{ADC_REF}) to (+15/16 V_{ADC_REF})] 01: $^{7}/_{8} \Rightarrow$ ADC range = [(–1/8 V_{ADC_REF}) to (+7/8 V_{ADC_REF})] 10: ¾ ⇒ ADC range = [(–1/4 V_{ADC_REF}) to (+3/4 V_{ADC_REF})] 11: ½ ⇒ ADC range = [(–1/2 V_{ADC_REF}) to (+1/2 V_{ADC_REF})]	ADCRS
2:1	01_{BIN}	**AD C**onversion **RES**olution (r_{ADC}; refer to section 2.1) Valid for both bridge sensor and temperature measurement. 00: 13 bits 10: 15 bits 01: 14 bits 11: 16 bits If 15 bits or 16 bits are activated, use CFGAPP:POFFS to select the segment used for the bridge sensor signal. Conditioning calculation is done with a 13-bit or 14-bit input value respectively.	ADCRES
0	1v	**AD C**onversion **ORD**er 0: 1-step conversion 1: 2-step conversion	ADCORD

Table 5.4 Configuration Word CFGAPP

Bit	Default	CFGAPP - Configuration of target application EEPROM/RAM Address $0C_{HEX}$	
15:13	000_{BIN}	Bridge sensor (e.g., **P**ressure) measurement segment. Digital offset to raw bridge sensor measurand value	POFFS
12	0_{BIN}	Ratio of bridge sensor (e.g., **P**ressure) measurements to special measurements in cycle: 0: 1 bridge sensor and 1 special 1: 30 bridge sensor and 1 special	PCNT
11	0_{BIN}	Enable ROM check at power-on. Start-up time is increased by approximately 10ms. 0: disabled 1: enabled	CHKROM
10	1_{BIN}	Enable lower limit for sensor short check. 0: limit = 1750 counts 1: limit = 1500 counts	CHKSSCL
9	0_{BIN}	Enable sensor connection and short check. 0: disabled 1: enabled	CHKSENS
8	0_{BIN}	Enable **T**emperature sensor check. § 0: disabled 1: enabled	CHKTS
7:6	01_{BIN}	**T**emperature measurement **GAIN** (refer to section 6). 00: GT1 01: GT2 10: GT3 11: GT4	TGAIN
5	0_{BIN}	**T**emperature **M**easurement **M**ode At sensor voltage excitation (CSBE=0) ***AND*** with external temperature measurement (TINT=0), determination of temperature measurement mode for external TS. 0: diode 1: external voltage **Otherwise** *at sensor bridge current excitation (CSBE=1)* ***OR*** *at internal temperature measurement (TINT=1),* adjust temperature measurement zero point ZCT; adjustment correlates with ADJREF:TOFFS. 0: zero point TOFFS=0 1: zero point TOFFS=2	TMM
4	1_{BIN}	Temperature measurement internal 0: external (diode or voltage) 1: on-chip diode	TINT
3	1_{BIN}	**Bridge current excitation (CSBE=1):** enable common mode regulation **Bridge voltage excitation (CSBE=0):** Connect internal VSSA to VBR_B and VDDA to VBR_T 0: disabled/disconnected 1: enabled/connected	CMSHE
2	0_{BIN}	Sensor bridge excitation mode: 0: voltage excitation 1: current excitation	CSBE
1	0_{BIN}	ADC and XZC reference voltage (V_{ADC_REF}; refer to section 2.1): 0: $V_{ADC\_REF} = V_{VBR\_T} – V_{VBR\_B}$ 1: $V_{ADC\_REF} = V_{VDDA} – V_{VSSA}$	BREF
0	0_{BIN}	Bridge signal polarity (differential voltage at pins VBP and VBN): 0: positive ($V_{IN\_DIFF} = V_{VBP} – V_{VBN}$) 1: negative ($V_{IN\_DIFF} = V_{VBN} – V_{VBP}$)	BPOL

§ **Note:** For product versions ZSC31150Cxx and earlier, bit 8 is CHKAGE, which is the enable bit for the Sensor Aging Check (CMV). Set to 1 to enable. The default is 0. For product versions ZSC31150Dxx and subsequent versions, the CMV check is controlled by the limits.

Table 5.5 Configuration Word ADJREF

<table>
<tr><th>Bit</th><th>Default</th><th colspan="2">ADJREF - Adjustment of internal references
EEPROM/RAM Address $0D_{HEX}$</th></tr>
<tr><td>15:14</td><td>00_{BIN}</td><td>One-Wire Interface Mode (refer to section 3.3 for details)
<table>
<tr><th rowspan="2">Bits 15:14</th><th rowspan="2">OWI Mode</th><th colspan="2">Pin AOUT</th></tr>
<tr><th>OWI</th><th>Analog Output</th></tr>
<tr><td>00</td><td>OWIWIN</td><td>Start-up window</td><td>After start-up window</td></tr>
<tr><td>01</td><td>OWIANA</td><td>Start-up window</td><td>Enabled</td></tr>
<tr><td>10</td><td>OWIENA</td><td>Enabled</td><td>Disabled</td></tr>
<tr><td>11</td><td>OWIDIS</td><td>Disabled</td><td>Enabled</td></tr>
</table></td><td>IFOWIM</td></tr>
<tr><td>13:10</td><td>1000_{BIN}</td><td>Additional alternative SIF slave address for I^2C and OWI.
3 MSB bits (70_{HEX}) are added to 4 programmable LSB bits (resulting range 70_{HEX} to $7F_{HEX}$, default address 78_{HEX} is also valid).</td><td>IFADDR</td></tr>
<tr><td>9</td><td>0_{BIN}</td><td>Enable reset in case of Diagnostic Mode (executed after time-out of the watchdog timer)
0: stop, hold in DM 1: reset, start-up again</td><td>DMRES</td></tr>
<tr><td rowspan="2">8:6</td><td rowspan="2">100_{BIN}</td><td>ZCT adjustment value
Sensor bridge voltage excitation (CFGAPP:CSBE=0)
→ Adjustment for zero point of temperature measurement ZCT
(refer to section 6.1 for details).</td><td>TOFFS</td></tr>
<tr><td>Sensor bridge current excitation (CFGAPP:CSBE=1)
→ Adjustment for sensor bridge current.
Supply current depends on external reference resistor R_{IBR}.
$I_{BR,nom} = V_{VDDA} / (16\ R_{IBR})$.
I_{BR} is adjustable in $0.125 * I_{BR,nom}$ units in the range of 0.5 to $1.375 * I_{BR,nom}$.
Default value causes factor 1 ($I_{BR,nom}$).</td><td>CSBADJ</td></tr>
<tr><td>5</td><td>1_{BIN}</td><td>Enables bias current boost for analog front-end (recommended f_{CLK} > 3MHz)
0: disabled 1: enabled</td><td>BBOOST</td></tr>
<tr><td>4:0</td><td>10010_{BIN}</td><td>Adjusts frequency f_{OSC}, of internal oscillator.
Adjustment of f_{CLK} in the range of 2 to 4MHz. (Only applicable for OWI communication.)</td><td>OSCADJ</td></tr>
</table>

Table 5.6 Configuration Word RESERVED

Bit	Default at delivery	RSVD – Additional adjustments EEPROM/RAM Address $0E_{HEX}$	
15:2	0000 0000 0000 00_{BIN}	Do not use	
1	0_{BIN}	Enables enhanced bridge-settling mode. During NOM, one more bridge measurement is included after a special measurement (e.g., auto-zero, temperature, CMV, Sensor Connection Check, or Sensor Short Check), where the first measurement is discarded. It allows charging external capacitors at the sensor inputs. 0: disabled 1: enabled	BSETTL
0	0_{BIN}	Enables EEPROM lock for OWI communication 0: disabled 1: enabled	EEPLOCK

5.3. EEPROM Signature

The EEPROM signature (address F_{HEX}) is used to check the validity of EEPROM contents. The signature is built using a polynomial arithmetic modulo 2. The following source code generates the signature if the field ***eepcont[ ]*** is allocated by the EEPROM contents (addresses 00_{HEX} to $0E_{HEX}$). The parameter is the count of addresses included in the signature and must be set to N=15 for the ZSC31150.

Figure 5.1 Source-Code Signature Generation

```
#define POLYNOM 0xA005
unsigned short signature(eepcont, N)
  unsigned short eepcont[], N;
  {
   unsigned short sign, poly, p, x, i, j;
   sign = 0; poly = POLYNOM;
   for (i=0; i<N; i++) {
     sign^=eepcont[i];
     p=0; x=sign&poly;
     for (j=0; j<16; j++, p^=x, x>>=1);
     sign<<=1; sign+=(p&1);
   }
   return(~sign);
  }
```

5.4. EEPROM Write Locking

Product versions ZSC31150Dxx and later support EEPROM write locking. If the mode is active (RSVD:EEPLOCK=1), it is not possible to overwrite the current EEPROM content using the OWI interface and the ZSC31150 responds with error code $CF6C_{HEX}$. An activated EEPROM lock (RSVD:EEPLOCK=1) can be always overwritten using I^2C communication.

An EEPROM lock programmed in EEPROM is activated by

1) New power-on
2) Sending the EEP_WRITE_EN command
3) Start measurement cycle by a STRT_CYC_xxx command

The following write sequence is possible:

1) Write calibration data including EEPLOCK to RAM mirror
2) Copy RAM mirror to EEPROM
3) Write EEPROM signature directly to EEPROM

In the case of a wrong EEPROM signature, the EEPROM lock is always deactivated.

6 Temperature Sensor Adaption and CMV Measurement

Temperature measurement data can be acquired from different temperature sensors (TS), which are adjusted by configuration registers CFGAPP and ADJREF. CFGAPP:TMM and CFGAPP:TINT define the temperature sensor to be used for acquiring temperature data. CFGAPP:TGAIN, ADJREF:TOFFS, and CFGAPP:TMM are used to adapt/fit the signal range of the sensor to the input properties and operation temperature range. The range shift for the A/D conversion is always set to ½ (refer to section 2.1). Table 6.1 shows recommended and possible configurations for different types of temperature sensors.

Table 6.1 Configuration Temperature Measurement

Temperature Sensor	Gain TGAIN	Zero Point Adjustment ZCT	Sensor Connected to/between Pin(s)	Notes
Internal Diode	GT1 – GT4	0 or 2 (TMM)		Recommended: GT2 and ZCT=0 TS zero point is adjusted by CFGAPP:TMM
External Diode	GT1 – GT4	0 to 7 (TOFFS)	VBR_T, IRTEMP	$V_{TEMP} = V_{IRTEMP} - V_{VBR\_T}$ TS zero point is adjusted by CFGAPP:TOFFS
External Resistor	GT1 – GT4	0 to 7 (TOFFS)	IRTEMP	Half bridge: VDDA to VSSA TS zero point is adjusted by CFGAPP:TOFFS
Bridge TC	No adjustment	5 or 7 (TMM)		TS zero point is adjusted by CFGAPP:TMM

Note: The temperature sensor must be adjusted to ensure that at minimum and maximum temperature, the temperature sensor output voltage (including tolerances!) is inside the specified input signal and ADC range. Adjust the gain and offset within the temperature range so that the output of the ADC (START_AD_T_AZC, command D9) is in the range of 10% to 90% of the minimum to maximum digital conversion result.

6.1. Temperature Measurement when Sensor Bridge is in Voltage Excitation Mode

6.1.1. Internal PN-Junction TS

Table 6.2 Sensitivity Internal Temperature Sensor

CFGAPP:TGAIN	Sensitivity ppm FS / K		
	Minimum	Typical	Maximum
GT1 (00)	1333	1466	1629
GT2 (01)	3332	3665	4072
GT3 (10)	3665	4032	4479
GT4 (11)	3998	4398	4887

The input range is typically shifted by 1/8 full scale higher for adjusting CFGAPP:TMM=1.

6.1.2. External PN-Junction TS

Adaptation of an external diode for temperature measurement is described in this section. The values given in Table 6.3 are recommended for typical diodes within the temperature range. Measure the diode's forward voltage (V_F) for the external pn-junction to make an adjustment; normally 650mV is expected. Typically V_F changes depending on the temperature by –2mV/K.

Figure 6.1 External PN-Junction Temperature Sensor

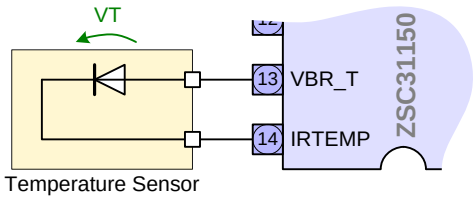


Table 6.3 Sensitivity and IRTEMP Input Signal Range in mV/V using External PN-Junction Mode

TGAIN	Sensitivity (S_{ED}) ppm FS / K		
	Minimum	Typical	Maximum
GT1	606	667	741
GT2	1515	1667	1852
GT3	1667	1833	2037
GT4	1818	2000	2222

Table 6.4 Temperature Measurement Input Range Midpoint in mV (RM_{ED})

Zero Point Adjustment (ZCT)	VT Input Range Midpoint in mV (RM_{ED})							
	0	1	2	3	4	5	6	7
Minimum	533	500	467	433	400	367	333	300
Typical	667	625	583	542	500	458	417	375
Maximum	800	750	700	650	600	550	500	450

Calculation of input range for a given adjustment configuration (see Table 6.3 for S_{EDxxx}):

Input range minimum: $IR_{min} = RM_{EDmin} +/- 0.45/ S_{EDmax}$

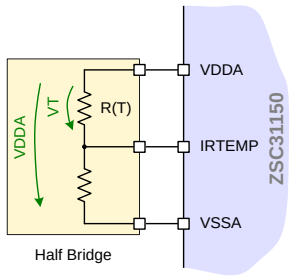
Input range typical value: $IR_{typ} = RM_{EDtyp} +/- 0.45/ S_{EDtyp}$

Input range maximum: $IR_{max} = RM_{EDmax} +/- 0.45/ S_{EDmin}$

Input signal ranges are roughly estimated and must be verified in the application in the full application temperature range.

6.1.3. External Resistor

Figure 6.2 Temperature Measurement with External Resistor



The ZSC31150's external resistor mode supports using an external half bridge for temperature measurement, which is connected between VDDA and VSSA. Input signal range is asymmetric and begins at a maximum of approximately 30%∗VDDA less than VDDA (asymmetric input range, approximately 0.7 VDDA to 1 VDDA).

Table 6.5 explains the resulting input range for using an external resistor for temperature measurement in detail. Because temperature measurement via an external resistor delivers a ratiometric result, the voltage VT is displayed as a ratio to VDDA.

Table 6.5 ZSC31150 Input Signal Range for External Resistor Mode (Voltages referenced to VDDA)

TGAIN	Sensitivity ppm FS / [mV/V]	VT / VDDA [mV/V]	Temperature Zero Point Adjustment (register ADJREG:TOFFS)							
			0	1	2	3	4	5	6	7
GT1	2666	min	20	20	20	20	20	20	20	20
		max	350	340	330	320	310	300	290	280
GT2	6666	min	95	85	70	60	50	40	30	20
		max	240	230	220	210	200	190	180	166
GT3	7333	min	100	90	80	70	60	50	40	30
		max	230	220	210	200	190	180	170	160
GT4	8000	min	105	95	85	75	65	55	45	35
		max	225	215	205	195	185	175	165	155

Hint: IRTEMP input signal ranges are roughly estimated and must be verified in the application.

6.1.4. Result and Sensitivity Calculation

Temperature gain (TGAIN) and offset (ADJREF:TOFFS) are programmable for temperature acquisition; V_{OFFS} is the resulting shift potential of the offset adjustment. The temperature measurement result is compared to V_{T_REF} (depending on input mode) and can be calculated and verified by using the following gain coefficients (voltages referenced to VSS):

Table 6.6 Temperature Gain Coefficients

Gain Identifier	GT1	GT2	GT3	GT4
GAIN	2.66	4.0	6.6	7.33

6.2. Temperature Measurement when Sensor Bridge in Current Excitation Mode

Bridge current excitation enables temperature measurements using the temperature coefficient of bridge resistors, so no additional temperature sensor is needed. For temperature data acquisition, the common mode voltage of the bridge inputs (VBP and VBN) is measured.

The bridge current must be adjusted with restricted voltage over the bridge V_{Bridge} and the input signal V_{VBN} and V_{VBP} must be in the allowed range, which can be secured by an internal control circuit. The bridge current can be coarsely tuned by adding an external resistor from the VBR_T pin to the top of the bridge and finely adjusted by changing the configuration register ADJREF:CSBADJ to ensure that the common mode range is not exceeded when considering the full temperature behavior and measured rejection limits.

Figure 6.3 Bridge Current Mode Application

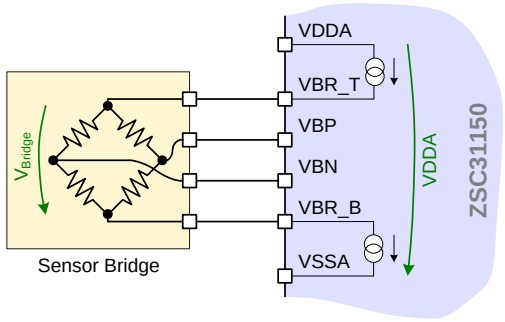


Table 6.7 gives the input sensitivity and range with respect to V_{Bridge}/VDDA for bridge signal measurements in Bridge Current Excitation Mode for temperature measurements.

Table 6.7 Temperature Measurement in Bridge Current Excitation Mode (CFGAPP:CSBE=1)

TGAIN	Sensitivity ppm FS / [mV/V]	V_{Bridge} / VDDA [mVV]	Temperature Zero Point Adjustment (register CFGAPP:TMM)	
			TMM=0	TMM=1
GT1	444	Min	0	0
		Max	1000	1000
GT2	889	Min	163	319
		Max	1000	1000
GT3	1067	Min	195	338
		Max	1000	1000
GT4	1333	Min	203	328
		Max	923	1000

6.3. CMV Measurement

ZSC31150 offers a special method for sensor aging detection. The common mode voltage (CMV) of the sensor bridge is periodically measured during NOM and compared with limits that are defined during calibration for this function. Limits are stored in register $0A_{HEX}$. The 16 bits of this register are divided into two sections. The lower limit is stored at bits [7:0] and the upper limit is stored at bits [15:8] of register $0A_{HEX}$. A CMV error is indicated if the current CMV measurement result is lower than the lower limit or higher than the upper limit.

The CMV limits can be expressed as percentages of the CMV measurement result (START_AD_CMV_AZC, command DB) or calculated directly with the following CMV_AZC formula. When defining CMV limits, note that the CMV measurement result can drift in the temperature range depending on the temperature behavior of the sensor bridge. The CMV measurement acquires the common mode voltage of bridge (V_{IN_CM}) and can be approximated using following formulas:

⇒ **Approximated CMV measurement**

$$CMV = 2^{RES}\left(\frac{8}{3}\right)\left(\frac{V_{IN\_CM}}{VBR}\right) - 2^{RES}\left(\frac{5}{6}\right)$$

$$CMV\_AZC = 2^{RES}\left(\frac{8}{3}\right)\left(\frac{V_{IN\_CM}}{VBR}\right) - T1AZ - 2^{RES}\left(\frac{5}{6}\right)$$

⇒ **Ideal Case** $\left(T1AZ = 2^{RES-1}\right)$

$$CMV\_AZC = 2^{RES}\left(\frac{4}{3}\right)\left(2\frac{V_{IN\_CM}}{VBR} - 1\right)$$

RES	ADC resolution in bits (RES =[13|14|15|16])
T1AZ	AZ readout of T1 measurement (Command D5)
V_{IN_CM}	Common mode voltage at input (shorted VBP and VBN)
VBR	VBR_T – VBR_B = bridge (supply) voltage

The EEPROM register content for upper and lower limits can be calculated using the following equations:

⇒ **Upper Limit**

$$CMV_{bits[15:8]} = Hex\left[\left(\frac{CMV\_AZC}{2^{RES-13}} + 4096 + \frac{8196 * CMV_{limit\_high}}{100}\right) \div 32 + 1\right]$$

⇒ **Upper Limit**

$$CMV_{bits[7:0]} = Hex\left[\left(\frac{CMV\_AZC}{2^{RES-13}} + 4096 - \frac{8196 * CMV_{limit\_low}}{100}\right) \div 32\right]$$

RES	ADC resolution in bits (RES = [13|14|15|16])
CMV_{limit_high}	Percentage value for upper CMV limit range = [0 to 25] %
CMV_{limit_low}	Percentage value for lower CMV limit range = [0 to 25] %

The factor of 2^{RES-13} is used to shift the result of the CMV_AZC measurement to the internal 13-bit domain that is used for comparison with predefined CMV limits.

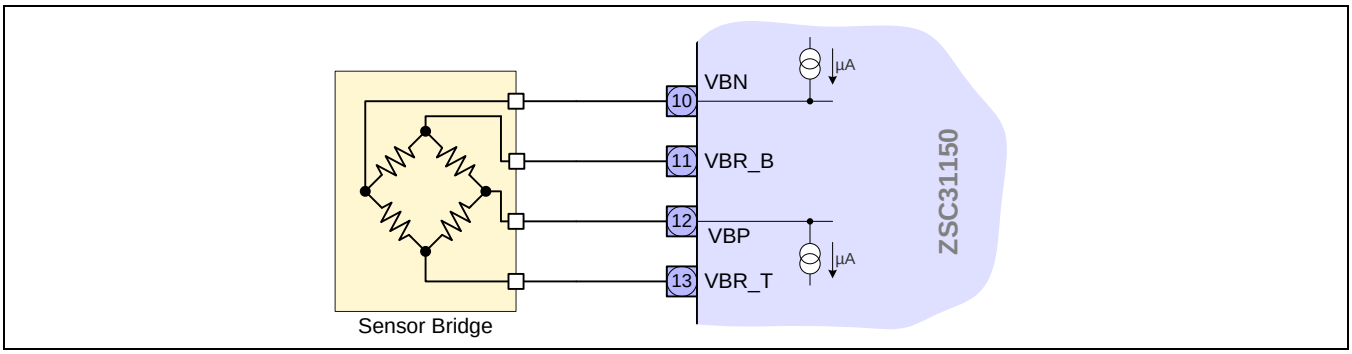
6.4. Sensor Check

The sensor check consists of two parts: the Sensor Connection Check (SCC) and Sensor Short Check (SSC). These two options can only be enabled or disabled together because both options are controlled via CFGAPP:CHKSENS (refer to Table 5.4). Both options will directly influence the response time of the whole system. For details about response time, refer to the *ZSC31150 Bandwidth Calculation Spreadsheet.*

The Sensor Connection Check will check if one of the four connection wires of the sensor bridge is broken. This option enables additional comparators that will monitor both differential inputs of the sensor bridge. An internal current supply will bring the VBR_T line to a defined voltage level to avoid misinterpretations if the VBR_T line is not connected.

Figure 6.4 illustrates the principle of Sensor Short Check. If SSC is enabled, two additional measurement tasks (SSC+ and SSC-) are added into the measurement cycle, which are described in the *ZSC31150 Data Sheet*. During the measurement, a current is forced into the bridge by internal current sources. The voltage difference between VBP and VBN is measured. If voltage difference is too small, then a shorted sensor is detected. In order to avoid misinterpretations during measuring, which could be caused by the voltage difference of the sensor bridge, the SSC measurement with same current level is repeated but with a reverse sign.

Figure 6.4 Principle of Sensor Short Check



7 Related Documents

Document
ZSC31150 Data Sheet
ZSC31150 Evaluation Kit Description
ZSC31150/ZSSC3138 Application Note – Range Zooming
SSC Application Note – RBIC1 Calibration DLL Description
ZSC31150 Bandwidth Calculation Spreadsheet
ZSC31150 Calibration Calculation
SSC Temperature Profile Calculation Spreadsheet
ZSC31150 Technical Note – SSOP14 and DFN14 Package Description
IDT Wafer Dicing Guidelines
SSC Application Note - Single Ended Input
ZSC31150 Technical Note – Traceability
ZSC31150 Traceability Calculation Spreadsheet
*SSC Command Syntax Spreadsheet**

Visit the ZSC31150 product page www.idt.com/zsc31150 on IDT's website www.idt.com or contact your nearest sales office for the latest version of these documents.

Note: Documents marked with an asterisk are available on the product page for the SSC Communication Board for the Evaluation Kit: www.idt.com/ssc-cb.

8 Glossary

Term	Description
ADC	Analog-to-Digital Converter
AOUT	Analog Output
BR	Bridge Sensor Signal Measurand (e.g., Pressure)
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
DAC	Digital-to-Analog Converter
DM	Diagnostic Mode
EEPROM	Electrically Erasable Programmable Read Only Memory
LDR	Lower Diagnostic Range
LPF	Low-Pass Filter
MSB	Most Significant Bit
NOM	Normal Operation Mode
OWI	One-Wire Interface
RAM	Random-Access Memory
ROM	Read Only Memory
SCC	Sensor Connection Check
SED	Sensitivity External Diode
SIF	Serial Interface
SSC	Sensor Short Check or Sensor Signal Conditioner (depending on context)
SSC+	Positive-Biased Sensor Short Check
SSC-	Negative-Biased Sensor Short Check
TS	Temperature Sensor
UDR	Upper Diagnostic Range
XZC	eXtended Zero Compensation

9 Document Revision History

Revision	Date	Description
1.00	September 25, 2009	First release of document.
1.01-1.02	October 2, 2009	Change to ZMDI denotation.
1.03	July 29, 2010	Table 5.4: TMM explained more in detail. Table 4.2: Low byte of SIF2 at START_AD_xx command changed to processed command. Rearrangement of formulas in section 6.3 → renamed common mode voltage. Section 2.5: Added a more detailed description. Section 4.5.1: Added a more detailed description of START_CM command. Inserted new drawings for Figure 1.1, Figure 3.2, Figure 3.3, Figure 3.7, Figure 3.8. Corrected default value in Table 5.6 for bits 15:4 to “000HEX.” Section 8: extended glossary. Applied new ZMDI template. Renamed RREF in section 6.2 and RBR_REF in Table 5.5 into RIBR as in DS. Renamed the ZMD31150 as the ZSC31150.
1.04	May 16, 2011	Corrected CMV equation for ideal case in section 6.3. Corrected measurement tasks to SSC+ and SSC- in section 6.4. Extended working mode description (1.3) and START_CM description (4.5.1). Corrected Figure 6.2 and redrew Figure 6.1 and Figure 6.3. Added more detailed description for OWI bit time (tOWI_Bit) and OWI hold time start condition (tOWI_STA).
1.05	May 26, 2011	Add detailed description for CMV limit calculation and EEPROM registers 8HEX/9HEX.
1.06	August 7, 2013	Sed_DAC command behavior and formulas added. Added detailed description for CMV limit calculation and EEPROM registers 8HEX/9HEX. Added extend description of AD segmentation. Revision to Table 6.3. Added definition of SED to glossary. Added range shift definition for temperature measurement.
1.07	June 30, 2014	Segmentation section updated. Correction for Range Shift values in calculation formulas. OWI interface parameters extended. Updates for Table 3.2 and text below. Update for specification for tOWI_STO in Table 3.3. Contact phone numbers and related documents section updated. Minor edits for clarity.
1.10	November 9, 2015	CRC references changed to check sum. Conversion time for D8 to DB commands updated. Configuration words ADJREF and RESERVED updated. Command START_AD_CNT updated in Table 4.1. Updates for section 4.5.1 OWI bit time formula updated in Table 3.2. Error codes in Table 1.1 updated. Contact information updated. Updates for related documents.
1.11	December 3, 2015	Update for Table 5.4 for the definition of CHKSSCL.
1.12	April 16, 2016	Conditioning equations corrected. Update for contact information and related documents.
160527	May 27, 2016	Changed to IDT branding.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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