

# M16C/5L Group, M16C/56 Group

## User's Manual: Hardware

RENESAS MCU

M16C Family / M16C/50 Series

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

# About This Manual

## 1. Purpose and Target User

This manual is designed to be read primarily by application developers who have an understanding of this microcomputer (MCU) including its hardware functions and electrical characteristics. The user should have a basic understanding of electric circuits, logic circuits and, MCUs.

This manual consists of six main categories: Overview, CPU, System Control, Peripherals, Electrical Characteristics, and Usage Notes.

Carefully read all notes in this document prior to use. Notes are found throughout each chapter, at the end of each chapter, and in the dedicated Usage Notes chapter.

The Revision History at the end of this manual summarizes primary modifications and additions to the previous versions. For details, please refer to the relative chapters or sections of this manual.

The M16C/5L Group, M16C/56 Group includes the documents listed below. Verify this manual is the latest version by visiting the Renesas Electronics website.

Type of Document	Contents	Document Name	Document Number
Datasheet	Overview of Hardware and Electrical Characteristics	M16C/5L Group, M16C/56 Group Datasheet	R01DS0035EJ0110
User's Manual: Hardware	Specifications and detailed descriptions of: -pin layout -memory map -peripherals -electrical characteristics -timing characteristics Refer to the Application Manual for peripheral usage.	M16C/5L Group, M16C/56 Group User's Manual: Hardware	This publication
User's Manual: Software/Software Manual	Descriptions of instruction set	M16C/60, M16C/20, M16C/Tiny Series Software Manual	REJ09B0137
Application Note	-Usages -Applications -Sample programs -Programming technics using Assembly language or C programming language	Available on the Renesas Electronics website.	
Renesas Technical Update	Bulletins on product specifications, documents, etc.		

## 2. Numbers and Symbols

The following explains the denotations used in this manual for registers, bits, pins and various numbers.

(1) Registers, bits, and pins

Registers, bits, and pins are indicated by symbols. Each symbol has a register/bit/pin identifier after the symbol.

Example: PM03 bit in the PM0 register

P3\_5 pin, VCC pin

(2) Numbers

A binary number has the suffix "b" except for a 1-bit value.

A hexadecimal number has the suffix "h".

A decimal number has no suffix.

Example: Binary notation: 11b

Hexadecimal notation: EFA0h

Decimal notation: 1234

### 3. Registers

The following illustration describes registers used throughout this manual.

**Example Register**

Symbol  
EXAMPLE

Address  
9999h

Reset Value  
000X 1X00b

See Note 1

See Note 2

Bit Symbol	Bit Name	Description	RW
AAAA0	Example bit 0	b2 b1 0 0 : XX function 0 1 : YY function 1 0 : Do not set this value. 1 1 : ZZ function	RW
AAAA1			RW
— (b2)	No register bit. If necessary, set this bit to 0. The read value is undefined.		—
— (b3)	Reserved	Set this bit to 1.	RW
— (b4)	Reserved	Set this bit to 0. The read value is undefined.	RW
AAAA5	Example bit 1	Functions vary with operating modes	WO
AAAA6			WO
AAAA7	Example flag	0: Example detected 1: Example not detected	RO

Notes:

1. Blank box: Set this bit to 0 or 1 according to the function.  
 0: Set this bit to 0.  
 1: Set this bit to 1.  
 X: Nothing is assigned to this bit.
2. RW: Read and write  
 RO: Read only  
 WO: Write only (the read value is undefined)  
 —: Not applicable
3. Reserved bit: This bit field is reserved. Set this bit to a specified value. For RW bits, the written value is read unless otherwise noted.
4.
  - No register bit(s): No register bit(s) is/are assigned to this field. If necessary, set to 0 for possible future implementation.
  - Do not use this combination: Proper operation is not guaranteed when this value is set.
  - Functions vary with operating modes: Functions vary with peripheral operating modes. Refer to register illustrations of the respective mode.

## 4. Abbreviations and Acronyms

The following acronyms and terms are used throughout this manual.

Abbreviation/Acronym	Meaning
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

# Table of Contents

Quick Reference .....	B-1
<b>1. Overview .....</b>	<b>1</b>
1.1 Features.....	1
1.1.1 Applications .....	1
1.2 Specifications.....	2
1.3 Product List.....	6
1.4 Block Diagram .....	8
1.5 Pin Assignments .....	10
1.6 Pin Functions.....	16
<b>2. Central Processing Unit (CPU).....</b>	<b>19</b>
2.1 Data Registers (R0, R1, R2, and R3) .....	20
2.2 Address Registers (A0 and A1) .....	20
2.3 Frame Base Register (FB).....	20
2.4 Interrupt Table Register (INTB).....	20
2.5 Program Counter (PC).....	20
2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP) .....	20
2.7 Static Base Register (SB) .....	20
2.8 Flag Register (FLG) .....	20
2.8.1 Carry Flag (C Flag) .....	20
2.8.2 Debug Flag (D Flag) .....	20
2.8.3 Zero Flag (Z Flag) .....	20
2.8.4 Sign Flag (S Flag) .....	20
2.8.5 Register Bank Select Flag (B Flag) .....	20
2.8.6 Overflow Flag (O Flag) .....	20
2.8.7 Interrupt Enable Flag (I Flag) .....	21
2.8.8 Stack Pointer Select Flag (U Flag) .....	21
2.8.9 Processor Interrupt Priority Level (IPL) .....	21
2.8.10 Reserved Areas .....	21
<b>3. Memory .....</b>	<b>22</b>
<b>4. Special Function Registers (SFRs) .....</b>	<b>24</b>
4.1 SFRs.....	24
4.2 Notes on SFRs .....	55
4.2.1 Register Settings .....	55
<b>5. Protection .....</b>	<b>57</b>
5.1 Introduction.....	57
5.2 Register .....	57



5.2.1	Protect Register (PRCR) .....	57
5.3	Notes on Protection .....	59
<b>6.</b>	<b>Resets .....</b>	<b>60</b>
6.1	Introduction .....	60
6.2	Registers.....	62
6.2.1	Processor Mode Register 0 (PM0) .....	62
6.2.2	Reset Source Determine Register (RSTFR) .....	63
6.3	Optional Function Select Area.....	64
6.3.1	Optional Function Select Address 1 (OFS1) .....	64
6.4	Operations .....	66
6.4.1	Status after Reset .....	66
6.4.2	Hardware Reset .....	68
6.4.3	Power-On Reset Function .....	69
6.4.4	Voltage Monitor 0 Reset .....	70
6.4.5	Voltage Monitor 2 Reset .....	70
6.4.6	Oscillator Stop Detect Reset .....	70
6.4.7	Watchdog Timer Reset .....	70
6.4.8	Software Reset .....	71
6.5	Notes on Resets .....	72
6.5.1	Power Supply Rising Gradient .....	72
6.5.2	Power-On Reset .....	72
6.5.3	OSDR Bit (Oscillation Stop Detect Reset Detect Flag) .....	72
6.5.4	Hardware Reset When VCC < Vdet0 .....	72
<b>7.</b>	<b>Voltage Detector .....</b>	<b>73</b>
7.1	Introduction .....	73
7.2	Registers.....	74
7.2.1	Voltage Detector 2 Flag Register (VCR1) .....	75
7.2.2	Voltage Detector Operation Enable Register (VCR2) .....	76
7.2.3	Voltage Monitor Function Select Register (VWCE) .....	77
7.2.4	Voltage Detector 2 Level Select Register (VD2LS) .....	78
7.2.5	Voltage Monitor 0 Control Register (VW0C) .....	79
7.2.6	Voltage Monitor 2 Control Register (VW2C) .....	80
7.3	Optional Function Select Area.....	82
7.3.1	Optional Function Select Address 1 (OFS1) .....	82
7.4	Operations .....	83
7.4.1	Digital Filter .....	83
7.4.2	Voltage Detector 0 .....	84
7.4.3	Voltage Detector 2 .....	86
7.5	Interrupts.....	89

<b>8.</b>	<b>Clock Generator .....</b>	<b>90</b>
8.1	Introduction .....	90
8.2	Registers.....	92
8.2.1	System Clock Control Register 0 (CM0) .....	93
8.2.2	System Clock Control Register 1 (CM1) .....	95
8.2.3	Oscillation Stop Detection Register (CM2) .....	97
8.2.4	Peripheral Clock Select Register (PCLKR) .....	99
8.2.5	PLL Control Register 0 (PLC0) .....	100
8.2.6	Processor Mode Register 2 (PM2) .....	101
8.2.7	40 MHz On-Chip Oscillator Control Register 0 (FRA0) .....	102
8.2.8	40 MHz On-Chip Oscillator Control Register 2 (FRA2) .....	103
8.3	Clocks Generated by Clock Generators .....	104
8.3.1	Main Clock .....	104
8.3.2	PLL Clock .....	105
8.3.3	fOCO40M .....	106
8.3.4	fOCO-F .....	106
8.3.5	125 kHz On-Chip Oscillator Clock (fOCO-S) .....	106
8.3.6	Sub Clock (fC) .....	107
8.4	CPU Clock and Peripheral Function Clocks .....	108
8.4.1	CPU Clock and BCLK .....	108
8.4.2	Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC, Main Clock) .....	108
8.5	Clock Output Function .....	110
8.6	System Clock Protection Function.....	110
8.7	Oscillator Stop/Restart Detect Function.....	111
8.7.1	Operation When CM27 Bit is 0 (Oscillator Stop Detect Reset) .....	111
8.7.2	Operation When CM27 Bit is 1 (Oscillator Stop/Restart Detect Interrupt) .....	112
8.7.3	Using the Oscillator Stop/Restart Detect Function .....	113
8.8	Interrupt .....	113
8.9	Notes on Clock Generator .....	114
8.9.1	Oscillator Using a Crystal or a Ceramic Resonator .....	114
8.9.2	Noise Countermeasure .....	115
8.9.3	CPU Clock .....	116
8.9.4	Oscillator Stop/Restart Detect Function .....	116
8.9.5	PLL Frequency Synthesizer .....	117
<b>9.</b>	<b>Power Control.....</b>	<b>118</b>
9.1	Introduction .....	118
9.2	Registers.....	118
9.2.1	Flash Memory Control Register 0 (FMR0) .....	119
9.2.2	Flash Memory Control Register 2 (FMR2) .....	120
9.3	Clock.....	122

9.3.1	Normal Operating Mode .....	122
9.3.2	Clock Mode Transition Procedure .....	126
9.3.3	Wait Mode .....	129
9.3.4	Stop Mode .....	131
9.4	Power Control in Flash Memory .....	133
9.4.1	Stopping Flash Memory .....	133
9.4.2	Reading Flash Memory .....	134
9.5	Reducing Power Consumption .....	136
9.5.1	Ports .....	136
9.5.2	A/D Converter .....	136
9.5.3	Stopping Peripheral Functions .....	136
9.5.4	Switching the Oscillation-Driving Capacity .....	136
9.6	Notes on Power Control.....	137
9.6.1	CPU Clock .....	137
9.6.2	Wait Mode .....	137
9.6.3	Stop Mode .....	137
9.6.4	Low Current Consumption Read Mode .....	138
9.6.5	Slow Read Mode .....	138
<b>10.</b>	<b>Processor Mode .....</b>	<b>139</b>
10.1	Introduction .....	139
10.2	Registers.....	140
10.2.1	Processor Mode Register 1 (PM1) .....	140
10.2.2	Program 2 Area Control Register (PRG2C) .....	141
10.2.3	Flash Memory Control Register 1 (FMR1) .....	142
10.3	Software Wait.....	143
10.4	Bus Hold .....	143
<b>11.</b>	<b>Programmable I/O Ports.....</b>	<b>144</b>
11.1	Introduction .....	144
11.2	I/O Ports and Pins.....	145
11.3	Registers.....	152
11.3.1	NMI Digital Debounce Register (NDDR) .....	153
11.3.2	P1_7 Digital Debounce Register (P17DDR) .....	153
11.3.3	Pull-Up Control Register 0 (PUR0) .....	154
11.3.4	Pull-Up Control Register 1 (PUR1) .....	154
11.3.5	Pull-Up Control Register 2 (PUR2) .....	155
11.3.6	Port Control Register (PCR) .....	156
11.3.7	Input Threshold Select Register 0 (VLT0) .....	157
11.3.8	Input Threshold Select Register 1 (VLT1) .....	158
11.3.9	Input Threshold Select Register 2 (VLT2) .....	158

11.3.10	Pin Assignment Control Register (PACR) .....	159
11.3.11	Port Pi Register (Pi) (i = 0 to 3, 6 to 10) .....	160
11.3.12	Port Pi Direction Register (PDi) (i = 0 to 3, 6 to 10) .....	161
11.4	Peripheral Function I/O .....	162
11.4.1	Peripheral Function I/O and Port Direction Bits .....	162
11.4.2	Priority Level of Peripheral Function I/O .....	162
11.4.3	Digital Debounce Filters .....	163
11.5	Unassigned Pin Handling .....	165
11.6	Notes on Programmable I/O Ports .....	166
11.6.1	Pin Assignment Control .....	166
11.6.2	Influence of $\overline{SD}$ .....	166
11.6.3	Input Voltage Threshold .....	166
<b>12.</b>	<b>Interrupts .....</b>	<b>167</b>
12.1	Introduction .....	167
12.2	Registers .....	168
12.2.1	Processor Mode Register 2 (PM2) .....	170
12.2.2	Interrupt Control Register 1 (BCNIC/TMOSIC, DM0IC to DM3IC, KUPIC, ADIC, S0TIC to S2TIC, S0RIC to S3RIC, TA0IC to TA4IC, TB0IC to TB2IC, S4TIC/RTCCIC, S4RIC, C0WIC, S3TIC/C0EIC, RTCTIC C0RIC, C0TIC, C0FRIC, C0FTIC, ICOC0IC, ICOCH0IC, ICOC1IC/IICIC, ICOCH1IC/SCLDAIC, ICOCH2IC to ICOCH3IC, BTIC) .....	171
12.2.3	Interrupt Control Register 2 (INT3IC, INT5IC, INT4IC, INT0IC to INT2IC) .....	172
12.2.4	Interrupt Source Select Register 3 (IFSR3A) .....	173
12.2.5	Interrupt Source Select Register 2 (IFSR2A) .....	174
12.2.6	Interrupt Source Select Register (IFSR) .....	175
12.2.7	Address Match Interrupt Enable Register (AIER) .....	176
12.2.8	Address Match Interrupt Enable Register 2 (AIER2) .....	176
12.2.9	Address Match Interrupt Register i (RMADi) (i = 0 to 3) .....	177
12.2.10	NMI Digital Debounce Register (NDDR) .....	178
12.2.11	P1_7 Digital Debounce Register (P17DDR) .....	178
12.3	Types of Interrupts .....	179
12.4	Software Interrupts .....	180
12.4.1	Undefined Instruction Interrupt .....	180
12.4.2	Overflow Interrupt .....	180
12.4.3	BRK Interrupt .....	180
12.4.4	INT Instruction Interrupt .....	180
12.5	Hardware Interrupts .....	181
12.5.1	Special Interrupts .....	181
12.5.2	Peripheral Function Interrupts .....	181
12.6	Interrupts and Interrupt Vectors .....	182
12.6.1	Fixed Vector Tables .....	182

12.6.2	Relocatable Vector Tables .....	183
12.7	Interrupt Control.....	185
12.7.1	Maskable Interrupt Control .....	185
12.7.2	Interrupt Sequence .....	186
12.7.3	Interrupt Response Time .....	187
12.7.4	Variation of IPL When Interrupt Request is Accepted .....	187
12.7.5	Saving Registers .....	188
12.7.6	Returning from an Interrupt Routine .....	189
12.7.7	Interrupt Priority .....	189
12.7.8	Interrupt Priority Level Select Circuit .....	189
12.7.9	Multiple Interrupts .....	191
12.8	$\overline{\text{INT}}$ Interrupt.....	191
12.9	$\overline{\text{NMI}}$ Interrupt.....	192
12.10	Key Input Interrupt.....	192
12.11	Address Match Interrupt .....	193
12.12	Non-Maskable Interrupt Source Discrimination .....	194
12.13	Notes on Interrupts .....	195
12.13.1	Reading Address 00000h .....	195
12.13.2	SP Setting .....	195
12.13.3	$\overline{\text{NMI}}$ Interrupt .....	195
12.13.4	Changing an Interrupt Source .....	196
12.13.5	Rewriting the Interrupt Control Register .....	197
12.13.6	Instruction to Rewrite the Interrupt Control Register .....	197
12.13.7	$\overline{\text{INT}}$ Interrupt .....	198
<b>13.</b>	<b>Watchdog Timer .....</b>	<b>199</b>
13.1	Introduction.....	199
13.2	Registers.....	201
13.2.1	Voltage Monitor 2 Control Register (VW2C) .....	202
13.2.2	Count Source Protection Mode Register (CSPR) .....	203
13.2.3	Watchdog Timer Refresh Register (WDTR) .....	203
13.2.4	Watchdog Timer Start Register (WDTS) .....	204
13.2.5	Watchdog Timer Control Register (WDC) .....	204
13.3	Optional Function Select Area.....	205
13.3.1	Optional Function Select Address 1 (OFS1) .....	205
13.3.2	Optional Function Select Address 2 (OFS2) .....	206
13.4	Operations.....	207
13.4.1	Refresh Operation Period .....	207
13.4.2	Count Source Protection Mode Disabled .....	208
13.4.3	Count Source Protection Mode Enabled .....	209
13.5	Interrupts.....	210

13.6	Notes on the Watchdog Timer .....	211
<b>14.</b>	<b>DMAC.....</b>	<b>212</b>
14.1	Introduction .....	212
14.2	Registers.....	214
14.2.1	DMAi Source Pointer (SARi) (i = 0 to 3) .....	215
14.2.2	DMAi Destination Pointer (DARi) (i = 0 to 3) .....	215
14.2.3	DMAi Transfer Counter (TCRi) (i = 0 to 3) .....	216
14.2.4	DMAi Control Register (DMiCON) (i = 0 to 3) .....	217
14.2.5	DMAi Source Select Register (DMiSL) (i = 0 to 3) .....	218
14.3	Operations .....	221
14.3.1	DMA Enabled .....	221
14.3.2	DMA Request .....	221
14.3.3	Transfer Cycles .....	222
14.3.4	DMAC Transfer Cycles .....	224
14.3.5	Single Transfer Mode .....	225
14.3.6	Repeat Transfer Mode .....	226
14.3.7	Channel Priority and DMA Transfer Timing .....	227
14.4	Interrupts.....	228
14.5	Notes on DMAC.....	229
14.5.1	Write to the DMAE Bit in the DMiCON Register (i = 0 to 3) .....	229
14.5.2	Changing the DMA Request Source .....	229
<b>15.</b>	<b>Timer A.....</b>	<b>230</b>
15.1	Introduction .....	230
15.2	Registers.....	233
15.2.1	Peripheral Clock Select Register (PCLKR) .....	234
15.2.2	Clock Prescaler Reset Flag (CPSRF) .....	234
15.2.3	Timer AB Division Control Register 0 (TCKDIVC0) .....	235
15.2.4	Timer A Count Source Select Register i (TACSi) (i = 0 to 2) .....	236
15.2.5	16-bit Pulse Width Modulation Mode Function Select Register (PWMFS) .....	237
15.2.6	Timer A Waveform Output Function Select Register (TAPOFS) .....	238
15.2.7	Timer A Output Waveform Change Enable Register (TAOW) .....	239
15.2.8	Timer Ai Register (TAi) (i = 0 to 4) .....	240
15.2.9	Timer Ai-1 Register (TAi1) (i = 1, 2, 4) .....	241
15.2.10	Count Start Flag (TABSR) .....	241
15.2.11	One-Shot Start Flag (ONSF) .....	242
15.2.12	Trigger Select Register (TRGSR) .....	243
15.2.13	Increment/Decrement Flag (UDF) .....	244
15.2.14	Timer Ai Mode Register (TAiMR) (i = 0 to 4) .....	245
15.3	Operations .....	246

15.3.1	Common Operations .....	246
15.3.2	Timer Mode .....	248
15.3.3	Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing) .....	252
15.3.4	Event Counter Mode (When Processing Two-Phase Pulse Signal) .....	256
15.3.5	One-Shot Timer Mode .....	261
15.3.6	Pulse Width Modulation (PWM) Mode .....	265
15.3.7	Programmable Output Mode (Timers A1, A2, and A4) .....	270
15.4	Interrupts.....	274
15.5	Notes on Timer A.....	275
15.5.1	Common Notes on Multiple Modes .....	275
15.5.2	Timer A (Timer Mode) .....	276
15.5.3	Timer A (Event Counter Mode) .....	276
15.5.4	Timer A (One-Shot Timer Mode) .....	276
15.5.5	Timer A (Pulse Width Modulation Mode) .....	277
15.5.6	Timer A (Programmable Output Mode) .....	278
<b>16.</b>	<b>Timer B.....</b>	<b>279</b>
16.1	Introduction.....	279
16.2	Registers.....	282
16.2.1	Peripheral Clock Select Register (PCLKR) .....	283
16.2.2	Clock Prescaler Reset Flag (CPSRF) .....	283
16.2.3	Timer Bi Register (TBi) (i = 0 to 2) .....	284
16.2.4	Timer Bi-1 Register (TBi1) (i = 0 to 2) .....	285
16.2.5	Pulse Period/Pulse Width Measurement Mode Function Select Register 1 (PPWFS1) ..	285
16.2.6	Timer B Count Source Select Register i (TBCSi) (i = 0 to 1) .....	286
16.2.7	Timer AB Division Control Register 0 (TCKDIVC0) .....	287
16.2.8	Count Start Flag (TABSR) .....	287
16.2.9	Timer Bi Mode Register (TBiMR) (i = 0 to 2) .....	288
16.3	Operations.....	289
16.3.1	Common Operations .....	289
16.3.2	Timer Mode .....	291
16.3.3	Event Counter Mode .....	293
16.3.4	Pulse Period/Pulse Width Measurement Modes .....	296
16.4	Interrupts.....	301
16.5	Notes on Timer B.....	302
16.5.1	Common Notes on Multiple Modes .....	302
16.5.2	Timer B (Timer Mode) .....	302
16.5.3	Timer B (Event Counter Mode) .....	302
16.5.4	Timer B (Pulse Period/Pulse Width Measurement Modes) .....	303

<b>17. Three-Phase Motor Control Timer Function .....</b>	<b>304</b>
17.1 Introduction .....	304
17.2 Registers.....	308
17.2.1 Timer B2 Register (TB2) .....	309
17.2.2 Timer Ai, Ai-1 Register (TAi, TAI1) (i = 1, 2, 4) .....	309
17.2.3 Three-Phase PWM Control Register 0 (INVC0) .....	310
17.2.4 Three-Phase PWM Control Register 1 (INVC1) .....	312
17.2.5 Three-Phase Output Buffer Register i (IDBi) (i = 0, 1) .....	314
17.2.6 Dead Time Timer (DTT) .....	314
17.2.7 Timer B2 Interrupt Generation Frequency Set Counter (ICTB2) .....	315
17.2.8 Timer B2 Special Mode Register (TB2SC) .....	316
17.2.9 Position-Data-Retain Function Control Register (PDRF) .....	317
17.2.10 Port Function Control Register (PFCR) .....	318
17.2.11 Three-Phase Protect Control Register (TPRC) .....	318
17.3 Operations .....	319
17.3.1 Common Operations in Multiple Modes .....	319
17.3.2 Triangular Wave Modulation Three-Phase Mode 0 .....	325
17.3.3 Triangular Wave Modulation Three-Phase Mode 1 .....	330
17.3.4 Sawtooth Wave Modulation Mode .....	337
17.4 Interrupts.....	342
17.4.1 Timer B2 Interrupt .....	342
17.4.2 Timer A1, A2, and A4 Interrupts .....	342
17.5 Notes on Three-Phase Motor Control Timer Function.....	343
17.5.1 Timer A and Timer B .....	343
17.5.2 Influence of $\overline{SD}$ .....	343
<b>18. Timer S.....</b>	<b>344</b>
18.1 Introduction .....	344
18.2 Registers.....	348
18.2.1 Time Measurement Register j (G1TMj) (j = 0 to 7) .....	350
18.2.2 Waveform Generation Register j (G1POj) (j = 0 to 7) .....	351
18.2.3 Waveform Generation Control Register j (G1POCRj) (j = 0 to 7) .....	352
18.2.4 Time Measurement Control Register j (G1TMCRj) (j = 0 to 7) .....	354
18.2.5 Base Timer Register (G1BT) .....	356
18.2.6 Base Timer Control Register 0 (G1BCR0) .....	357
18.2.7 Base Timer Control Register 1 (G1BCR1) .....	358
18.2.8 Time Measurement Prescaler Register j (G1TPRj) (j = 6 and 7) .....	359
18.2.9 Function Enable Register (G1FE) .....	359
18.2.10 Function Select Register (G1FS) .....	360
18.2.11 Base Timer Reset Register (G1BTRR) .....	361
18.2.12 Count Source Divide Register (G1DV) .....	361



18.2.13	Waveform Output Master Enable Register (G1OER) .....	362
18.2.14	Timer S I/O Control Register 0 (G1IOR0) .....	363
18.2.15	Timer S I/O Control Register 1 (G1IOR1) .....	364
18.2.16	Interrupt Request Register (G1IR) .....	365
18.2.17	Interrupt Enable Register 0 (G1IE0) .....	366
18.2.18	Interrupt Enable Register 1 (G1IE1) .....	367
18.3	Operations .....	368
18.3.1	Base Timer .....	368
18.3.2	Time Measurement Function .....	376
18.3.3	Waveform Generation Function .....	380
18.3.4	I/O Port Select Function .....	392
18.4	Interrupts.....	393
18.4.1	IC/OC Base Timer Interrupt .....	394
18.4.2	IC/OC Channel 0 Interrupt to IC/OC Channel 3 Interrupt .....	394
18.4.3	IC/OC Interrupt 0 and IC/OC Interrupt 1 .....	394
18.5	Notes on Timer S.....	395
18.5.1	Register Access .....	395
18.5.2	Changing the G1IR Register .....	395
18.5.3	Changing Registers ICOCiIC (i = 0, 1) .....	397
18.5.4	Output Waveform During the Base Timer Reset with the BTS bit .....	397
18.5.5	OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register .....	397
18.5.6	Interrupt Request When Selecting Time Measurement Function .....	397
<b>19.</b>	<b>Task Monitor Timer .....</b>	<b>398</b>
19.1	Introduction .....	398
19.2	Registers.....	399
19.2.1	Task Monitor Timer Register (TMOS) .....	399
19.2.2	Task Monitor Timer Count Start Flag (TMOSSR) .....	399
19.2.3	Task Monitor Timer Count Source Select Register (TMOSCS) .....	400
19.2.4	Task Monitor Timer Protect Register (TMOSPR) .....	400
19.3	Operation .....	401
19.4	Interrupt .....	402
19.5	Notes on Task Monitor Timer.....	403
19.5.1	Register Settings .....	403
19.5.2	Reading the Timer .....	403
<b>20.</b>	<b>Real-Time Clock .....</b>	<b>404</b>
20.1	Introduction .....	404
20.2	Registers.....	406
20.2.1	Real-Time Clock Second Data Register (RTCSEC) .....	407
20.2.2	Real-Time Clock Minute Data Register (RTCMIN) .....	408

20.2.3	Real-Time Clock Hour Data Register (RTCHR) .....	409
20.2.4	Real-Time Clock Day Data Register (RTCWK) .....	410
20.2.5	Real-Time Clock Control Register 1 (RTCCR1) .....	411
20.2.6	Real-Time Clock Control Register 2 (RTCCR2) .....	413
20.2.7	Real-Time Clock Count Source Select Register (RTCCSR) .....	415
20.2.8	Real-Time Clock Second Compare Data Register (RTCCSEC) .....	416
20.2.9	Real-Time Clock Minute Compare Data Register (RTCCMIN) .....	417
20.2.10	Real-Time Clock Hour Compare Data Register (RTCCHR) .....	418
20.3	Operations .....	419
20.3.1	Basic Operation .....	419
20.3.2	Compare Mode .....	422
20.4	Interrupts.....	428
20.5	Notes on Real-Time Clock.....	429
20.5.1	Starting and Stopping the Count .....	429
20.5.2	Register Settings (Time Data, etc.) .....	429
20.5.3	Register Settings (Compare Data) .....	429
20.5.4	Time Reading Procedure in Real-Time Clock Mode .....	430
<b>21.</b>	<b>Serial Interface UART<sub>i</sub> (i = 0 to 4) .....</b>	<b>431</b>
21.1	Introduction.....	431
21.2	Registers.....	434
21.2.1	UART Clock Select Register (UCLKSEL0) .....	436
21.2.2	Peripheral Clock Select Register (PCLKR) .....	436
21.2.3	UART <sub>i</sub> Transmit/Receive Mode Register (UiMR) (i = 0 to 4) .....	437
21.2.4	UART <sub>i</sub> Bit Rate Register (UiBRG) (i = 0 to 4) .....	438
21.2.5	UART <sub>i</sub> Transmit Buffer Register (UiTB) (i = 0 to 4) .....	438
21.2.6	UART <sub>i</sub> Transmit/Receive Control Register 0 (UiC0) (i = 0 to 4) .....	439
21.2.7	UART <sub>i</sub> Transmit/Receive Control Register 1 (UiC1) (i = 0 to 4) .....	441
21.2.8	UART <sub>i</sub> Receive Buffer Register (UiRB) (i = 0 to 4) .....	442
21.2.9	UART2 Special Mode Register 4 (U2SMR4) .....	444
21.2.10	UART2 Special Mode Register 3 (U2SMR3) .....	446
21.2.11	UART2 Special Mode Register 2 (U2SMR2) .....	447
21.2.12	UART2 Special Mode Register (U2SMR) .....	448
21.2.13	Pin Assignment Control Register (PACR) .....	449
21.3	Operations.....	450
21.3.1	Clock Synchronous Serial I/O Mode .....	450
21.3.2	Clock Asynchronous Serial I/O (UART) Mode .....	458
21.3.3	Special Mode 1 (I <sup>2</sup> C Mode) (UART2) .....	467
21.3.4	Special Mode 2 (UART2) .....	482
21.3.5	Special Mode 3 (IE Mode) (UART2) .....	486
21.3.6	Special Mode 4 (SIM Mode) (UART2) .....	488

21.4	Interrupts.....	493
21.4.1	Interrupt Related Registers .....	493
21.4.2	Reception Interrupt .....	494
21.5	Notes on Serial Interface UARTi (i = 0 to 4) .....	495
21.5.1	Common Notes on Multiple Modes .....	495
21.5.2	Clock Synchronous Serial I/O Mode .....	495
21.5.3	Special Mode 1 (I <sup>2</sup> C Mode) .....	496
21.5.4	Special Mode 4 (SIM Mode) .....	498
<b>22.</b>	<b>Multi-master I<sup>2</sup>C-bus Interface .....</b>	<b>499</b>
22.1	Introduction .....	499
22.2	Registers Descriptions.....	502
22.2.1	I2C0 Data Shift Register (S00) .....	503
22.2.2	I2C0 Address Register i (S0Di) (i = 0 to 2) .....	504
22.2.3	I2C0 Control Register 0 (S1D0) .....	505
22.2.4	I2C0 Clock Control Register (S20) .....	507
22.2.5	I2C0 Start/Stop Condition Control Register (S2D0) .....	509
22.2.6	I2C0 Control Register 1 (S3D0) .....	510
22.2.7	I2C0 Control Register 2 (S4D0) .....	514
22.2.8	I2C0 Status Register 0 (S10) .....	516
22.2.9	I2C0 Status Register 1 (S11) .....	521
22.3	Operations .....	522
22.3.1	Clock .....	522
22.3.2	Generating a Start Condition .....	525
22.3.3	Generating a Stop Condition .....	527
22.3.4	Generating a Restart Condition .....	528
22.3.5	Start Condition Overlap Protect .....	529
22.3.6	Arbitration Lost .....	531
22.3.7	Detecting Start/Stop Conditions .....	533
22.3.8	Operation after Transmitting/Receiving a Slave Address or Data .....	535
22.3.9	Timeout Detection .....	536
22.3.10	Data Transmit/Receive Examples .....	537
22.4	Interrupts.....	542
22.5	Notes on Multi-master I <sup>2</sup> C-bus Interface .....	545
22.5.1	Limitation on CPU Clock .....	545
22.5.2	Register Access .....	545
<b>23.</b>	<b>CAN Module .....</b>	<b>546</b>
23.1	CAN SFRs .....	549
23.1.1	CAN0 Control Register (C0CTRL) .....	550
23.1.2	CAN0 Clock Select Register (C0CLKR) .....	554

23.1.3	CAN0 Bit Configuration Register (C0BCR) .....	555
23.1.4	CAN0 Mask Register k (C0MKRk) (k = 0 to 7) .....	557
23.1.5	CAN0 FIFO Received ID Compare Register n (C0FIDCR0 to C0FIDCR1) (n = 0, 1) .....	558
23.1.6	CAN0 Mask Invalid Register (C0MKIVLR) .....	560
23.1.7	CAN0 Mailbox Register j (C0MBj) (j = 0 to 31) .....	561
23.1.8	CAN0 Mailbox Interrupt Enable Register (C0MIER) .....	565
23.1.9	CAN0 Message Control Register (C0MCTLj) (j = 0 to 31) .....	566
23.1.10	CAN0 Receive FIFO Control Register (C0RFCR) .....	570
23.1.11	CAN0 Receive FIFO Pointer Control Register (C0RFPCR) .....	573
23.1.12	CAN0 Transmit FIFO Control Register (C0TFCR) .....	574
23.1.13	CAN0 Transmit FIFO Pointer Control Register (C0TFPCR) .....	576
23.1.14	CAN0 Status Register (C0STR) .....	577
23.1.15	CAN0 Mailbox Search Mode Register (C0MSMR) .....	580
23.1.16	CAN0 Mailbox Search Status Register (C0MSSR) .....	581
23.1.17	CAN0 Channel Search Support Register (C0CSSR) .....	583
23.1.18	CAN0 Acceptance Filter Support Register (C0AFSR) .....	584
23.1.19	CAN0 Error Interrupt Enable Register (C0EIER) .....	585
23.1.20	CAN0 Error Interrupt Factor Judge Register (C0EIFR) .....	587
23.1.21	CAN0 Receive Error Count Register (C0RECR) .....	590
23.1.22	CAN0 Transmit Error Count Register (C0TECR) .....	591
23.1.23	CAN0 Error Code Store Register (C0ECSR) .....	592
23.1.24	CAN0 Time Stamp Register (C0TSR) .....	594
23.1.25	CAN0 Test Control Register (C0TCR) .....	595
23.2	Operating Mode .....	598
23.2.1	CAN Reset Mode .....	599
23.2.2	CAN Halt Mode .....	600
23.2.3	CAN Sleep Mode .....	601
23.2.4	CAN Operation Mode (Excluding Bus-Off State) .....	602
23.2.5	CAN Operation Mode (Bus-Off State) .....	603
23.3	CAN Communication Speed Configuration .....	604
23.3.1	CAN Clock Configuration .....	604
23.3.2	Bit Timing Configuration .....	604
23.3.3	Bit rate .....	605
23.4	Mailbox and Mask Register Structure .....	606
23.5	Acceptance Filtering and Masking Function .....	608
23.6	Reception and Transmission .....	611
23.6.1	Reception .....	612
23.6.2	Transmission .....	614
23.7	CAN Interrupt .....	615

<b>24. A/D Converter</b> .....	<b>616</b>
24.1 Introduction.....	616
24.2 Registers.....	618
24.2.1 Open-Circuit Detection Assist Function Register (AINRST) .....	619
24.2.2 A/D Register i (ADi) (i = 0 to 7) .....	620
24.2.3 A/D Control Register 2 (ADCON2) .....	621
24.2.4 A/D Control Register 0 (ADCON0) .....	622
24.2.5 A/D Control Register 1 (ADCON1) .....	624
24.3 Operations .....	625
24.3.1 A/D Conversion Cycle .....	625
24.3.2 A/D Conversion Start Conditions .....	627
24.3.3 A/D Conversion Result .....	628
24.3.4 Current Consumption Reduce Function .....	628
24.3.5 Open-Circuit Detection Assist Function .....	628
24.4 Operational Modes .....	630
24.4.1 One-Shot Mode .....	630
24.4.2 Repeat Mode .....	632
24.4.3 Single Sweep Mode .....	634
24.4.4 Repeat Sweep Mode 0 .....	636
24.5 External Sensor .....	638
24.6 Interrupt .....	639
24.7 Notes on A/D Converter.....	640
24.7.1 Analog Input Pin .....	640
24.7.2 Pin Configuration .....	640
24.7.3 Register Access .....	640
24.7.4 A/D Conversion Start .....	640
24.7.5 A/D Operation Mode Change .....	640
24.7.6 State When Forcibly Terminated .....	640
24.7.7 A/D Open-Circuit Detection Assist Function .....	641
24.7.8 Detecting Completion of A/D Conversion .....	641
24.7.9 $\phi$ AD .....	641
<b>25. CRC Calculator</b> .....	<b>642</b>
25.1 Introduction.....	642
25.2 Registers.....	643
25.2.1 SFR Snoop Address Register (CRCSAR) .....	643
25.2.2 CRC Mode Register (CRCMR) .....	644
25.2.3 CRC Data Register (CRCD) .....	644
25.2.4 CRC Input Register (CRCIN) .....	644
25.3 Operations .....	645
25.3.1 Basic Operation .....	645

25.3.2	CRC Snoop .....	645
<b>26.</b>	<b>Flash Memory.....</b>	<b>648</b>
26.1	Introduction .....	648
26.2	Memory Map.....	650
26.3	Registers.....	651
26.3.1	Flash Memory Control Register 0 (FMR0) .....	651
26.3.2	Flash Memory Control Register 1 (FMR1) .....	654
26.3.3	Flash Memory Control Register 2 (FMR2) .....	655
26.3.4	Flash Memory Control Register 3 (FMR3) .....	656
26.3.5	Flash Memory Control Register 6 (FMR6) .....	657
26.4	Optional Function Select Area.....	658
26.4.1	Optional Function Select Address 1 (OFS1) .....	659
26.4.2	Optional Function Select Address 2 (OFS2) .....	660
26.5	Flash Memory Rewrite Disable Function .....	661
26.6	Boot Mode .....	661
26.7	User Boot Mode.....	661
26.7.1	User Boot Function .....	661
26.8	CPU Rewrite Mode.....	665
26.8.1	EW0 Mode .....	666
26.8.2	EW1 Mode .....	672
26.8.3	Operating Speed .....	678
26.8.4	Data Protect Function .....	678
26.8.5	Suspend Function .....	679
26.8.6	Software Commands .....	681
26.8.7	Status Register .....	688
26.9	Standard Serial I/O Mode .....	691
26.9.1	ID Code Check Function .....	692
26.9.2	Forced Erase Function .....	693
26.9.3	Standard Serial I/O Mode Disable Function .....	693
26.9.4	Standard Serial I/O Mode 1 .....	694
26.9.5	Standard Serial I/O Mode 2 .....	696
26.10	Parallel I/O Mode.....	697
26.10.1	ROM Code Protect Function .....	697
26.11	Notes on Flash Memory.....	698
26.11.1	OFS1 Address, OFS2 Address, and ID Code Storage Address .....	698
26.11.2	Reading Data Flash .....	698
26.11.3	CPU Rewrite Mode .....	699
26.11.4	User Boot .....	701

<b>27. Electrical Characteristics</b> .....	<b>702</b>
27.1 Electrical Characteristics (J-Version, Common to 3 V and 5 V).....	702
27.1.1 Absolute Maximum Rating .....	702
27.1.2 Recommended Operating Conditions .....	703
27.1.3 A/D Conversion Characteristics .....	705
27.1.4 Flash Memory Electrical Characteristics .....	706
27.1.5 Voltage Detector and Power Supply Circuit Electrical Characteristics .....	709
27.1.6 Oscillator Electrical Characteristics .....	711
27.2 Electrical Characteristics (J-Version, $V_{CC} = 5\text{ V}$ ) .....	712
27.2.1 Electrical Characteristics .....	712
27.2.2 Timing Requirements (Peripheral Functions and Others) .....	714
27.3 Electrical Characteristics (J-Version, $V_{CC} = 3\text{ V}$ ) .....	721
27.3.1 Electrical Characteristics .....	721
27.3.2 Timing Requirements (Peripheral Functions and Others) .....	723
27.4 Electrical Characteristics (K-Version, Common to 3 V and 5 V).....	730
27.4.1 Absolute Maximum Rating .....	730
27.4.2 Recommended Operating Conditions .....	731
27.4.3 A/D Conversion Characteristics .....	733
27.4.4 Flash Memory Electrical Characteristics .....	734
27.4.5 Voltage Detector and Power Supply Circuit Electrical Characteristics .....	737
27.4.6 Oscillator Electrical Characteristics .....	739
27.5 Electrical Characteristics (K-Version, $V_{CC} = 5\text{ V}$ ) .....	740
27.5.1 Electrical Characteristics .....	740
27.5.2 Timing Requirements (Peripheral Functions and Others) .....	742
27.6 Electrical Characteristics (K-Version, $V_{CC} = 3\text{ V}$ ) .....	749
27.6.1 Electrical Characteristics .....	749
27.6.2 Timing Requirements (Peripheral Functions and Others) .....	751
<b>28. Usage Notes</b> .....	<b>758</b>
28.1 Notes on Noise .....	758
28.2 Notes on SFRs .....	759
28.2.1 Register Settings .....	759
28.3 Notes on Protection .....	761
28.4 Notes on Resets .....	762
28.4.1 Power Supply Rising Gradient .....	762
28.4.2 Power-On Reset .....	762
28.4.3 OSDR Bit (Oscillation Stop Detect Reset Detect Flag) .....	762
28.4.4 Hardware Reset When $V_{CC} < V_{det0}$ .....	762
28.5 Notes on Clock Generator .....	763
28.5.1 Oscillator Using a Crystal or a Ceramic Resonator .....	763
28.5.2 Noise Countermeasure .....	764

28.5.3	CPU Clock .....	765
28.5.4	Oscillator Stop/Restart Detect Function .....	765
28.5.5	PLL Frequency Synthesizer .....	766
28.6	Notes on Power Control.....	767
28.6.1	CPU Clock .....	767
28.6.2	Wait Mode .....	767
28.6.3	Stop Mode .....	767
28.6.4	Low Current Consumption Read Mode .....	768
28.6.5	Slow Read Mode .....	768
28.7	Notes on Programmable I/O Ports.....	769
28.7.1	Pin Assignment Control .....	769
28.7.2	Influence of $\overline{SD}$ .....	769
28.7.3	Input Voltage Threshold .....	769
28.8	Notes on Interrupts .....	770
28.8.1	Reading Address 00000h .....	770
28.8.2	SP Setting .....	770
28.8.3	$\overline{NMI}$ Interrupt .....	770
28.8.4	Changing an Interrupt Source .....	771
28.8.5	Rewriting the Interrupt Control Register .....	772
28.8.6	Instruction to Rewrite the Interrupt Control Register .....	772
28.8.7	$\overline{INT}$ Interrupt .....	773
28.9	Notes on the Watchdog Timer .....	774
28.10	Notes on DMAC.....	775
28.10.1	Write to the DMAE Bit in the DMiCON Register (i = 0 to 3) .....	775
28.10.2	Changing the DMA Request Source .....	775
28.11	Notes on Timer A.....	776
28.11.1	Common Notes on Multiple Modes .....	776
28.11.2	Timer A (Timer Mode) .....	777
28.11.3	Timer A (Event Counter Mode) .....	777
28.11.4	Timer A (One-Shot Timer Mode) .....	777
28.11.5	Timer A (Pulse Width Modulation Mode) .....	778
28.11.6	Timer A (Programmable Output Mode) .....	779
28.12	Notes on Timer B.....	780
28.12.1	Common Notes on Multiple Modes .....	780
28.12.2	Timer B (Timer Mode) .....	780
28.12.3	Timer B (Event Counter Mode) .....	780
28.12.4	Timer B (Pulse Period/Pulse Width Measurement Modes) .....	781
28.13	Notes on Three-Phase Motor Control Timer Function.....	782
28.13.1	Timer A and Timer B .....	782
28.13.2	Influence of $\overline{SD}$ .....	782
28.14	Notes on Timer S.....	783



28.14.1	Register Access .....	783
28.14.2	Changing the G1IR Register .....	783
28.14.3	Changing Registers ICOCiIC (i = 0, 1) .....	785
28.14.4	Output Waveform During the Base Timer Reset with the BTS bit .....	785
28.14.5	OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register .....	785
28.14.6	Interrupt Request When Selecting Time Measurement Function .....	785
28.15	Notes on Task Monitor Timer.....	786
28.15.1	Register Settings .....	786
28.15.2	Reading the Timer .....	786
28.16	Notes on Real-Time Clock.....	787
28.16.1	Starting and Stopping the Count .....	787
28.16.2	Register Settings (Time Data, etc.) .....	787
28.16.3	Register Settings (Compare Data) .....	787
28.16.4	Time Reading Procedure in Real-Time Clock Mode .....	788
28.17	Notes on Serial Interface UARTi (i = 0 to 4) .....	789
28.17.1	Common Notes on Multiple Modes .....	789
28.17.2	Clock Synchronous Serial I/O Mode .....	789
28.17.3	Special Mode 1 (I <sup>2</sup> C Mode) .....	790
28.17.4	Special Mode 4 (SIM Mode) .....	792
28.18	Notes on Multi-master I <sup>2</sup> C-bus Interface .....	793
28.18.1	Limitation on CPU Clock .....	793
28.18.2	Register Access .....	793
28.19	Notes on CAN Module.....	794
28.20	Notes on A/D Converter.....	795
28.20.1	Analog Input Pin .....	795
28.20.2	Pin Configuration .....	795
28.20.3	Register Access .....	795
28.20.4	A/D Conversion Start .....	796
28.20.5	A/D Operation Mode Change .....	796
28.20.6	State When Forcibly Terminated .....	796
28.20.7	A/D Open-Circuit Detection Assist Function .....	796
28.20.8	Detecting Completion of A/D Conversion .....	796
28.20.9	φAD .....	796
28.21	Notes on Flash Memory.....	797
28.21.1	OFS1 Address, OFS2 Address, and ID Code Storage Address .....	797
28.21.2	Reading Data Flash .....	797
28.21.3	CPU Rewrite Mode .....	798
28.21.4	User Boot .....	800
<b>REGISTER INDEX</b>	<b>.....</b>	<b>801</b>

# Quick Reference

Only one page number is listed for each register. Refer to the REGISTER INDEX for more details.

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	62
0005h	Processor Mode Register 1	PM1	140
0006h	System Clock Control Register 0	CM0	93
0007h	System Clock Control Register 1	CM1	95
0008h			
0009h			
000Ah	Protect Register	PRCR	57
000Bh			
000Ch	Oscillation Stop Detection Register	CM2	97
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	141
0011h			
0012h	Peripheral Clock Select Register	PCLKR	99
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	234
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	63
0019h	Voltage Detector 2 Flag Register	VCR1	75
001Ah	Voltage Detector Operation Enable Register	VCR2	76
001Bh			
001Ch	PLL Control Register 0	PLC0	100
001Dh			
001Eh	Processor Mode Register 2	PM2	101
001Fh			
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	102
0023h			
0024h	40 MHz On-Chip Oscillator Control Register 2	FRA2	103
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	77
0027h			
0028h	Voltage Detector 2 Level Select Register	VD2LS	78
0029h			
002Ah	Voltage Monitor 0 Control Register	VW0C	79
002Bh			
002Ch	Voltage Monitor 2 Control Register	VW2C	80
002Dh			
002Eh			
002Fh			
0030h to 003Fh			
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	172
0045h			
0046h			
0047h			
0048h	INT5 Interrupt Control Register	INT5IC	172

Address	Register	Symbol	Page
0049h	INT4 Interrupt Control Register	INT4IC	172
004Ah	UART2 Bus Collision Detection Interrupt Control Register, Task Monitoring Timer Interrupt Control Register	BCNIC, TMOSIC	171
004Bh	DMA0 Interrupt Control Register	DM0IC	171
004Ch	DMA1 Interrupt Control Register	DM1IC	171
004Dh	Key Input Interrupt Control Register	KUPIC	171
004Eh	A/D Conversion Interrupt Control Register	ADIC	172
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	171
0050h	UART2 Receive Interrupt Control Register	S2RIC	171
0051h	UART0 Transmit Interrupt Control Register	S0TIC	171
0052h	UART0 Receive Interrupt Control Register	S0RIC	171
0053h	UART1 Transmit Interrupt Control Register	S1TIC	171
0054h	UART1 Receive Interrupt Control Register	S1RIC	171
0055h	Timer A0 Interrupt Control Register	TA0IC	171
0056h	Timer A1 Interrupt Control Register	TA1IC	171
0057h	Timer A2 Interrupt Control Register	TA2IC	171
0058h	Timer A3 Interrupt Control Register	TA3IC	171
0059h	Timer A4 Interrupt Control Register	TA4IC	171
005Ah	Timer B0 Interrupt Control Register	TB0IC	171
005Bh	Timer B1 Interrupt Control Register	TB1IC	171
005Ch	Timer B2 Interrupt Control Register	TB2IC	171
005Dh	INT0 Interrupt Control Register	INT0IC	172
005Eh	INT1 Interrupt Control Register	INT1IC	172
005Fh	INT2 Interrupt Control Register	INT2IC	172
0060h to 0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	171
006Ah	DMA3 Interrupt Control Register	DM3IC	171
006Bh			
006Ch			
006Dh			
006Eh			
006Fh	UART4 Transmit Interrupt Control Register, Real-Time Clock Compare Interrupt Control Register	S4TIC, RTCCIC	171
0070h	UART4 Receive Interrupt Control Register	S4RIC	171
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	171
0072h	UART3 Transmit Interrupt Control Register, CAN0 Error Interrupt Control Register	S3TIC, C0EIC	171
0073h	UART3 Receive Interrupt Control Register	S3RIC	171
0074h	Real-Time Clock Cycle Interrupt Control Register	RTCTIC	171
0075h	CAN0 Reception Complete Interrupt Control Register	C0RIC	171
0076h	CAN0 Transmission Complete Interrupt Control Register	C0TIC	171
0077h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	171
0078h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	171
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	171
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOC0IC	171
007Bh	IC/OC Interrupt 1 Control Register, I2C-bus Interface Interrupt Control Register	ICOC1IC, IICIC	171
007Ch	SCL/SDA Interrupt Control Register, IC/OC Channel 1 Interrupt Control Register	SCLDAIC, ICOC1IC	171
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOC2IC	171
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOC3IC	171
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	171

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
0180h	DMA0 Source Pointer	SAR0	215
0181h			
0182h			
0183h			
0184h	DMA0 Destination Pointer	DAR0	215
0185h			
0186h			
0187h			
0188h	DMA0 Transfer Counter	TCR0	216
0189h			
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	217
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	215
0191h			
0192h			
0193h			
0194h	DMA1 Destination Pointer	DAR1	215
0195h			
0196h			
0197h			
0198h	DMA1 Transfer Counter	TCR1	216
0199h			
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	217
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	215
01A1h			
01A2h			
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	215
01A5h			
01A6h			
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	216
01A9h			
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	217
01ADh			
01AEh			
01AFh			
01B0h	DMA3 Source Pointer	SAR3	215
01B1h			
01B2h			
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	215
01B5h			
01B6h			
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	216
01B9h			
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	217
01BDh			
01BEh			
01BFh			

Address	Register	Symbol	Page
01C0h	Timer B0-1 Register	TB01	285
01C1h			
01C2h			
01C3h	Timer B1-1 Register	TB11	285
01C4h			
01C5h			
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	285
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	286
01C9h	Timer B Count Source Select Register 1	TBCS1	286
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	235
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	236
01D1h	Timer A Count Source Select Register 1	TACS1	236
01D2h	Timer A Count Source Select Register 2	TACS2	236
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	237
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	238
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	239
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	318
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Task Monitor Timer Register	TMOS	399
01F1h			
01F2h	Task Monitor Timer Count Start Flag	TMOSSR	399
01F3h	Task Monitor Timer Count Source Select Register	TMOSCS	400
01F4h	Task Monitor Timer Protect Register	TMOSPR	400
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	173
0206h	Interrupt Source Select Register 2	IFSR2A	174
0207h	Interrupt Source Select Register	IFSR	175
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	176
020Fh	Address Match Interrupt Enable Register 2	AIER2	176
0210h			
0211h	Address Match Interrupt Register 0	RMAD0	177
0212h			
0213h			
0214h			
0215h	Address Match Interrupt Register 1	RMAD1	177
0216h			
0217h			
0218h			
0219h	Address Match Interrupt Register 2	RMAD2	177
021Ah			
021Bh			
021Ch			
021Dh	Address Match Interrupt Register 3	RMAD3	177
021Eh			
021Fh			
0220h	Flash Memory Control Register 0	FMR0	651
0221h	Flash Memory Control Register 1	FMR1	654
0222h	Flash Memory Control Register 2	FMR2	120
0223h	Flash Memory Control Register 3	FMR3	656
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	657
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			
0240h			
0241h			
0242h			
0243h			

Address	Register	Symbol	Page
0244h			
0245h			
0246h			
0247h			
0248h	UART0 Transmit/Receive Mode Register	U0MR	437
0249h	UART0 Bit Rate Register	U0BRG	438
024Ah	UART0 Transmit Buffer Register	U0TB	438
024Bh			
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	439
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	441
024Eh	UART0 Receive Buffer Register	U0RB	442
024Fh			
0250h			
0251h			
0252h	UART Clock Select Register	UCLKSEL0	436
0253h			
0254h			
0255h			
0256h			
0257h			
0258h	UART1 Transmit/Receive Mode Register	U1MR	437
0259h	UART1 Bit Rate Register	U1BRG	438
025Ah	UART1 Transmit Buffer Register	U1TB	438
025Bh			
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	439
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	441
025Eh	UART1 Receive Buffer Register	U1RB	442
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	
0265h	UART2 Special Mode Register 3	U2SMR3	
0266h	UART2 Special Mode Register 2	U2SMR2	
0267h	UART2 Special Mode Register	U2SMR	
0268h	UART2 Transmit/Receive Mode Register	U2MR	437
0269h	UART2 Bit Rate Register	U2BRG	438
026Ah	UART2 Transmit Buffer Register	U2TB	438
026Bh			
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	439
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	441
026Eh	UART2 Receive Buffer Register	U2RB	442
026Fh			
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h			
0291h			
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h	UART4 Transmit/Receive Mode Register	U4MR	437
0299h	UART4 Bit Rate Register	U4BRG	438
029Ah	UART4 Transmit Buffer Register	U4TB	438
029Bh			
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	439
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	441
029Eh	UART4 Receive Buffer Register	U4RB	442
029Fh			
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h	UART3 Transmit/Receive Mode Register	U3MR	437
02A9h	UART3 Bit Rate Register	U3BRG	438
02AAh	UART3 Transmit Buffer Register	U3TB	438
02ABh			
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	439
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	441
02AEh	UART3 Receive Buffer Register	U3RB	442
02AFh			
02B0h	I2C0 Data Shift Register	S00	503
02B1h			
02B2h	I2C0 Address Register 0	S0D0	504
02B3h	I2C0 Control Register 0	S1D0	505
02B4h	I2C0 Clock Control Register	S20	507
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	509
02B6h	I2C0 Control Register 1	S3D0	510
02B7h	I2C0 Control Register 2	S4D0	514
02B8h	I2C0 Status Register 0	S10	516
02B9h	I2C0 Status Register 1	S11	521
02BAh	I2C0 Address Register 1	S0D1	504
02BBh	I2C0 Address Register 2	S0D2	504
02BCh			
02BDh			
02BEh			
02BFh			

Address	Register	Symbol	Page
02C0h	Time Measurement Register 0, Waveform Generation Register 0	G1TM0, G1PO0	350
02C1h			
02C2h	Time Measurement Register 1, Waveform Generation Register 1	G1TM1, G1PO1	350
02C3h			
02C4h	Time Measurement Register 2, Waveform Generation Register 2	G1TM2, G1PO2	350
02C5h			
02C6h	Time Measurement Register 3, Waveform Generation Register 3	G1TM3, G1PO3	350
02C7h			
02C8h	Time Measurement Register 4, Waveform Generation Register 4	G1TM4, G1PO4	350
02C9h			
02CAh	Time Measurement Register 5, Waveform Generation Register 5	G1TM5, G1PO5	350
02CBh			
02CCh	Time Measurement Register 6, Waveform Generation Register 6	G1TM6, G1PO6	350
02CDh			
02CEh	Time Measurement Register 7, Waveform Generation Register 7	G1TM7, G1PO7	350
02CFh			
02D0h	Waveform Generation Control Register 0	G1POCR0	352
02D1h	Waveform Generation Control Register 1	G1POCR1	352
02D2h	Waveform Generation Control Register 2	G1POCR2	352
02D3h	Waveform Generation Control Register 3	G1POCR3	352
02D4h	Waveform Generation Control Register 4	G1POCR4	352
02D5h	Waveform Generation Control Register 5	G1POCR5	352
02D6h	Waveform Generation Control Register 6	G1POCR6	352
02D7h	Waveform Generation Control Register 7	G1POCR7	352
02D8h	Time Measurement Control Register 0	G1TMCR0	352
02D9h	Time Measurement Control Register 1	G1TMCR1	352
02DAh	Time Measurement Control Register 2	G1TMCR2	352
02DBh	Time Measurement Control Register 3	G1TMCR3	352
02DCh	Time Measurement Control Register 4	G1TMCR4	352
02DDh	Time Measurement Control Register 5	G1TMCR5	352
02DEh	Time Measurement Control Register 6	G1TMCR6	352
02DFh	Time Measurement Control Register 7	G1TMCR7	352
02E0h	Base Timer Register	G1BT	356
02E1h			
02E2h	Base Timer Control Register 0	G1BCR0	357
02E3h	Base Timer Control Register 1	G1BCR1	358
02E4h	Time Measurement Prescaler Register 6	G1TPR6	359
02E5h	Time Measurement Prescaler Register 7	G1TPR7	359
02E6h	Function Enable Register	G1FE	359
02E7h	Function Select Register	G1FS	360
02E8h	Base Timer Reset Register	G1BTRR	361
02E9h			
02EAh	Count Source Divide Register	G1DV	361
02EBh			
02ECh	Waveform Output Master Enable Register	G1OER	362
02EDh			
02EEh	Timer S I/O Control Register 0	G1IOR0	363
02EFh	Timer S I/O Control Register 1	G1IOR1	364
02F0h	Interrupt Request Register	G1IR	365
02F1h	Interrupt Enable Register 0	G1IE0	366
02F2h	Interrupt Enable Register 1	G1IE1	367
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh	NMI Digital Debounce Register	NDDR	153
02FFh	P1_7 Digital Debounce Register	P17DDR	153

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
0300h			
0301h			
0302h	Timer A1-1 Register	TA11	241
0303h			
0304h	Timer A2-1 Register	TA21	241
0305h			
0306h	Timer A4-1 Register	TA41	241
0307h			
0308h	Three-Phase PWM Control Register 0	INVC0	310
0309h	Three-Phase PWM Control Register 1	INVC1	312
030Ah	Three-Phase Output Buffer Register 0	IDB0	314
030Bh	Three-Phase Output Buffer Register 1	IDB1	314
030Ch	Dead Time Timer	DTT	314
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	315
030Eh	Position-Data-Retain Function Control Register	PDRF	317
030Fh			
0310h			
0311h			
0312h			
0313h			
0314h			
0315h			
0316h			
0317h			
0318h	Port Function Control Register	PFCR	318
0319h			
031Ah			
031Bh			
031Ch			
031Dh			
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	241
0321h			
0322h	One-Shot Start Flag	ONSF	242
0323h	Trigger Select Register	TRGSR	243
0324h	Increment/Decrement Flag	UDF	244
0325h			
0326h	Timer A0 Register	TA0	240
0327h			
0328h	Timer A1 Register	TA1	240
0329h			
032Ah	Timer A2 Register	TA2	240
032Bh			
032Ch	Timer A3 Register	TA3	240
032Dh			
032Eh	Timer A4 Register	TA4	240
032Fh			
0330h	Timer B0 Register	TB0	284
0331h			
0332h	Timer B1 Register	TB1	284
0333h			
0334h	Timer B2 Register	TB2	284
0335h			
0336h	Timer A0 Mode Register	TA0MR	245
0337h	Timer A1 Mode Register	TA1MR	245
0338h	Timer A2 Mode Register	TA2MR	245
0339h	Timer A3 Mode Register	TA3MR	245
033Ah	Timer A4 Mode Register	TA4MR	245

Address	Register	Symbol	Page
033Bh	Timer B0 Mode Register	TB0MR	288
033Ch	Timer B1 Mode Register	TB1MR	288
033Dh	Timer B2 Mode Register	TB2MR	288
033Eh	Timer B2 Special Mode Register	TB2SC	316
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	407
0341h	Real-Time Clock Minute Data Register	RTCMIN	408
0342h	Real-Time Clock Hour Data Register	RTCHR	409
0343h	Real-Time Clock Day Data Register	RTCWK	410
0344h	Real-Time Clock Control Register 1	RTCCR1	411
0345h	Real-Time Clock Control Register 2	RTCCR2	413
0346h	Real-Time Clock Count Source Select Register	RTCCSR	415
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	416
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	417
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	418
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			
0360h	Pull-Up Control Register 0	PUR0	154
0361h	Pull-Up Control Register 1	PUR1	154
0362h	Pull-Up Control Register 2	PUR2	155
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	156
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch	Input Threshold Select Register 0	VLT0	157
036Dh	Input Threshold Select Register 1	VLT1	158
036Eh	Input Threshold Select Register 2	VLT2	158
036Fh			
0370h	Pin Assignment Control Register	PACR	159
0371h			
0372h			
0373h			
0374h			
0375h			
0376h			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	203
037Dh	Watchdog Timer Refresh Register	WDTR	203
037Eh	Watchdog Timer Start Register	WDTS	204
037Fh	Watchdog Timer Control Register	WDC	204
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			
0390h	DMA2 Source Select Register	DM2SL	218
0391h			
0392h	DMA3 Source Select Register	DM3SL	218
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	218
0399h			
039Ah	DMA1 Source Select Register	DM1SL	218
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	619
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			

Address	Register	Symbol	Page
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	643
03B5h			
03B6h	CRC Mode Register	CRCMR	644
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	644
03BDh			
03BEh	CRC Input Register	CRCIN	644
03BFh			
03C0h	A/D Register 0	AD0	620
03C1h			
03C2h	A/D Register 1	AD1	620
03C3h			
03C4h	A/D Register 2	AD2	620
03C5h			
03C6h	A/D Register 3	AD3	620
03C7h			
03C8h	A/D Register 4	AD4	620
03C9h			
03CAh	A/D Register 5	AD5	620
03CBh			
03CCh	A/D Register 6	AD6	620
03CDh			
03CEh	A/D Register 7	AD7	620
03CFh			
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	621
03D5h			
03D6h	A/D Control Register 0	ADCON0	622
03D7h	A/D Control Register 1	ADCON1	624
03D8h			
03D9h			
03DAh			
03DBh			
03DCh			
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	160
03E1h	Port P1 Register	P1	160
03E2h	Port P0 Direction Register	PD0	161
03E3h	Port P1 Direction Register	PD1	161
03E4h	Port P2 Register	P2	160
03E5h	Port P3 Register	P3	160
03E6h	Port P2 Direction Register	PD2	161
03E7h	Port P3 Direction Register	PD3	161
03E8h			
03E9h			
03EAh			
03EBh			
03ECh	Port P6 Register	P6	160
03EDh	Port P7 Register	P7	160
03EEh	Port P6 Direction Register	PD6	161
03EFh	Port P7 Direction Register	PD7	161

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Address	Register	Symbol	Page
03F0h	Port P8 Register	P8	160
03F1h	Port P9 Register	P9	160
03F2h	Port P8 Direction Register	PD8	161
03F3h	Port P9 Direction Register	PD9	161
03F4h	Port P10 Register	P10	160
03F5h			
03F6h	Port P10 Direction Register	PD10	161
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			
D000h to D4FFh D			

Address	Register	Symbol	Page
D500h	CAN0 Mailbox 0: Message Identifier	COMB0	562
D501h			
D502h			
D503h			
D504h			
D505h	CAN0 Mailbox 0: Data Length	COMB0	562
D506h	CAN0 Mailbox 0: Data Field		
D507h			
D508h			
D509h			
D50Ah			
D50Bh			
D50Ch			
D50Dh			
D50Eh	CAN0 Mailbox 0: Time Stamp		
D50Fh			
D510h	CAN0 Mailbox 1: Message Identifier	COMB1	562
D511h			
D512h			
D513h			
D514h			
D515h	CAN0 Mailbox 1: Data Length	COMB1	562
D516h	CAN0 Mailbox 1: Data Field		
D517h			
D518h			
D519h			
D51Ah			
D51Bh			
D51Ch			
D51Dh			
D51Eh	CAN0 Mailbox 1: Time Stamp		
D51Fh			
D520h	CAN0 Mailbox 2: Message Identifier	COMB2	562
D521h			
D522h			
D523h			
D524h			
D525h	CAN0 Mailbox 2: Data Length	COMB2	562
D526h	CAN0 Mailbox 2: Data Field		
D527h			
D528h			
D529h			
D52Ah			
D52Bh			
D52Ch			
D52Dh			
D52Eh	CAN0 Mailbox 2: Time Stamp		
D52Fh			
D530h	CAN0 Mailbox 3: Message Identifier	COMB3	562
D531h			
D532h			
D533h			
D534h			
D535h	CAN0 Mailbox 3: Data Length	COMB3	562
D536h	CAN0 Mailbox 3: Data Field		
D537h			
D538h			
D539h			
D53Ah			
D53Bh			
D53Ch			
D53Dh			
D53Eh	CAN0 Mailbox 3: Time Stamp		
D53Fh			

The blank areas are reserved. No access is allowed.



Address	Register	Symbol	Page
D540h	CAN0 Mailbox 4: Message Identifier	COMB4	562
D541h			
D542h			
D543h			
D544h			
D545h	CAN0 Mailbox 4: Data Length		
D546h	CAN0 Mailbox 4: Data Field		
D547h			
D548h			
D549h			
D54Ah			
D54Bh			
D54Ch			
D54Dh	CAN0 Mailbox 4: Time Stamp		
D54Eh			
D54Fh	COMB5		
D550h		CAN0 Mailbox 5: Message Identifier	
D551h			
D552h			
D553h			
D554h			
D555h		CAN0 Mailbox 5: Data Length	
D556h		CAN0 Mailbox 5: Data Field	
D557h			
D558h			
D559h			
D55Ah			
D55Bh			
D55Ch			
D55Dh		CAN0 Mailbox 5: Time Stamp	
D55Eh			
D55Fh	COMB6	562	
D560h			CAN0 Mailbox 6: Message Identifier
D561h			
D562h			
D563h			
D564h			
D565h			CAN0 Mailbox 6: Data Length
D566h			CAN0 Mailbox 6: Data Field
D567h			
D568h			
D569h			
D56Ah			
D56Bh			
D56Ch			
D56Dh			CAN0 Mailbox 6: Time Stamp
D56Eh			
D56Fh	COMB7	562	
D570h			CAN0 Mailbox 7: Message Identifier
D571h			
D572h			
D573h			
D574h			
D575h			CAN0 Mailbox 7: Data Length
D576h			CAN0 Mailbox 7: Data Field
D577h			
D578h			
D579h			
D57Ah			
D57Bh			
D57Ch			
D57Dh			CAN0 Mailbox 7: Time Stamp
D57Eh			
D57Fh			

Address	Register	Symbol	Page
D580h	CAN0 Mailbox 8: Message Identifier	COMB8	562
D581h			
D582h			
D583h			
D584h			
D585h	CAN0 Mailbox 8: Data Length		
D586h	CAN0 Mailbox 8: Data Field		
D587h			
D588h			
D589h			
D58Ah			
D58Bh			
D58Ch			
D58Dh	CAN0 Mailbox 8: Time Stamp		
D58Eh			
D58Fh	COMB9		
D590h		CAN0 Mailbox 9: Message Identifier	
D591h			
D592h			
D593h			
D594h			
D595h		CAN0 Mailbox 9: Data Length	
D596h		CAN0 Mailbox 9: Data Field	
D597h			
D598h			
D599h			
D59Ah			
D59Bh			
D59Ch			
D59Dh		CAN0 Mailbox 9: Time Stamp	
D59Eh			
D59Fh	COMB10	562	
D5A0h			CAN0 Mailbox 10: Message Identifier
D5A1h			
D5A2h			
D5A3h			
D5A4h			
D5A5h			CAN0 Mailbox 10: Data Length
D5A6h			CAN0 Mailbox 10: Data Field
D5A7h			
D5A8h			
D5A9h			
D5AAh			
D5ABh			
D5ACh			
D5ADh			CAN0 Mailbox 10: Time Stamp
D5AEh			
D5AFh	COMB11	562	
D5B0h			CAN0 Mailbox 11: Message Identifier
D5B1h			
D5B2h			
D5B3h			
D5B4h			
D5B5h			CAN0 Mailbox 11: Data Length
D5B6h			CAN0 Mailbox 11: Data Field
D5B7h			
D5B8h			
D5B9h			
D5BAh			
D5BBh			
D5BCh			
D5BDh			CAN0 Mailbox 11: Time Stamp
D5BEh			
D5BFh			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
D5C0h	CAN0 Mailbox 12: Message Identifier	C0MB12	562
D5C1h			
D5C2h			
D5C3h			
D5C4h			
D5C5h	CAN0 Mailbox 12: Data Length		
D5C6h	CAN0 Mailbox 12: Data Field		
D5C7h			
D5C8h			
D5C9h			
D5CAh			
D5CBh			
D5CCh			
D5CDh			
D5CEh	CAN0 Mailbox 12: Time Stamp		
D5CFh			
D5D0h	CAN0 Mailbox 13: Message Identifier	C0MB13	562
D5D1h			
D5D2h			
D5D3h			
D5D4h			
D5D5h	CAN0 Mailbox 13: Data Length		
D5D6h	CAN0 Mailbox 13: Data Field		
D5D7h			
D5D8h			
D5D9h			
D5DAh			
D5DBh			
D5DCh			
D5DDh			
D5DEh	CAN0 Mailbox 13: Time Stamp		
D5DFh			
D5E0h	CAN0 Mailbox 14: Message Identifier	C0MB14	562
D5E1h			
D5E2h			
D5E3h			
D5E4h			
D5E5h	CAN0 Mailbox 14: Data Length		
D5E6h	CAN0 Mailbox 14: Data Field		
D5E7h			
D5E8h			
D5E9h			
D5EAh			
D5EBh			
D5ECh			
D5EDh			
D5EEh	CAN0 Mailbox 14: Time Stamp		
D5EFh			
D5F0h	CAN0 Mailbox 15: Message Identifier	C0MB15	562
D5F1h			
D5F2h			
D5F3h			
D5F4h			
D5F5h	CAN0 Mailbox 15: Data Length		
D5F6h	CAN0 Mailbox 15: Data Field		
D5F7h			
D5F8h			
D5F9h			
D5FAh			
D5FBh			
D5FCh			
D5FDh			
D5FEh	CAN0 Mailbox 15: Time Stamp		
D5FFh			

Address	Register	Symbol	Page
D600h	CAN0 Mailbox 16: Message Identifier	C0MB16	562
D601h			
D602h			
D603h			
D604h			
D605h	CAN0 Mailbox 16: Data Length		
D606h	CAN0 Mailbox 16: Data Field		
D607h			
D608h			
D609h			
D60Ah			
D60Bh			
D60Ch			
D60Dh			
D60Eh	CAN0 Mailbox 16: Time Stamp		
D60Fh			
D610h	CAN0 Mailbox 17: Message Identifier	C0MB17	562
D611h			
D612h			
D613h			
D614h			
D615h	CAN0 Mailbox 17: Data Length		
D616h	CAN0 Mailbox 17: Data Field		
D617h			
D618h			
D619h			
D61Ah			
D61Bh			
D61Ch			
D61Dh			
D61Eh	CAN0 Mailbox 17: Time Stamp		
D61Fh			
D620h	CAN0 Mailbox 18: Message Identifier	C0MB18	562
D621h			
D622h			
D623h			
D624h			
D625h	CAN0 Mailbox 18: Data Length		
D626h	CAN0 Mailbox 18: Data Field		
D627h			
D628h			
D629h			
D62Ah			
D62Bh			
D62Ch			
D62Dh			
D62Eh	CAN0 Mailbox 18: Time Stamp		
D62Fh			
D630h	CAN0 Mailbox 19: Message Identifier	C0MB19	562
D631h			
D632h			
D633h			
D634h			
D635h	CAN0 Mailbox 19: Data Length		
D636h	CAN0 Mailbox 19: Data Field		
D637h			
D638h			
D639h			
D63Ah			
D63Bh			
D63Ch			
D63Dh			
D63Eh	CAN0 Mailbox 19: Time Stamp		
D63Fh			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
D640h	CAN0 Mailbox 20: Message Identifier	C0MB20	562
D641h			
D642h			
D643h			
D644h			
D645h	CAN0 Mailbox 20: Data Length		
D646h	CAN0 Mailbox 20: Data Field		
D647h			
D648h			
D649h			
D64Ah			
D64Bh			
D64Ch			
D64Dh			
D64Eh	CAN0 Mailbox 20: Time Stamp		
D64Fh			
D650h	CAN0 Mailbox 21: Message Identifier	C0MB21	562
D651h			
D652h			
D653h			
D654h			
D655h	CAN0 Mailbox 21: Data Length		
D656h	CAN0 Mailbox 21: Data Field		
D657h			
D658h			
D659h			
D65Ah			
D65Bh			
D65Ch			
D65Dh			
D65Eh	CAN0 Mailbox 21: Time Stamp		
D65Fh			
D660h	CAN0 Mailbox 22: Message Identifier	C0MB22	562
D661h			
D662h			
D663h			
D664h			
D665h	CAN0 Mailbox 22: Data Length		
D666h	CAN0 Mailbox 22: Data Field		
D667h			
D668h			
D669h			
D66Ah			
D66Bh			
D66Ch			
D66Dh			
D66Eh	CAN0 Mailbox 22: Time Stamp		
D66Fh			
D670h	CAN0 Mailbox 23: Message Identifier	C0MB23	562
D671h			
D672h			
D673h			
D674h			
D675h	CAN0 Mailbox 23: Data Length		
D676h	CAN0 Mailbox 23: Data Field		
D677h			
D678h			
D679h			
D67Ah			
D67Bh			
D67Ch			
D67Dh			
D67Eh	CAN0 Mailbox 23: Time Stamp		
D67Fh			

Address	Register	Symbol	Page
D680h	CAN0 Mailbox 24: Message Identifier	C0MB24	562
D681h			
D682h			
D683h			
D684h			
D685h	CAN0 Mailbox 24: Data Length		
D686h	CAN0 Mailbox 24: Data Field		
D687h			
D688h			
D689h			
D68Ah			
D68Bh			
D68Ch			
D68Dh			
D68Eh	CAN0 Mailbox 24: Time Stamp		
D68Fh			
D690h	CAN0 Mailbox 25: Message Identifier	C0MB25	562
D691h			
D692h			
D693h			
D694h			
D695h	CAN0 Mailbox 25: Data Length		
D696h	CAN0 Mailbox 25: Data Field		
D697h			
D698h			
D699h			
D69Ah			
D69Bh			
D69Ch			
D69Dh			
D69Eh	CAN0 Mailbox 25: Time Stamp		
D69Fh			
D6A0h	CAN0 Mailbox 26: Message Identifier	C0MB26	562
D6A1h			
D6A2h			
D6A3h			
D6A4h			
D6A5h	CAN0 Mailbox 26: Data Length		
D6A6h	CAN0 Mailbox 26: Data Field		
D6A7h			
D6A8h			
D6A9h			
D6AAh			
D6ABh			
D6ACh			
D6ADh			
D6AEh	CAN0 Mailbox 26: Time Stamp		
D6AFh			
D6B0h	CAN0 Mailbox 27: Message Identifier	C0MB27	562
D6B1h			
D6B2h			
D6B3h			
D6B4h			
D6B5h	CAN0 Mailbox 27: Data Length		
D6B6h	CAN0 Mailbox 27: Data Field		
D6B7h			
D6B8h			
D6B9h			
D6BAh			
D6BBh			
D6BCh			
D6BDh			
D6BEh	CAN0 Mailbox 27: Time Stamp		
D6BFh			

The blank areas are reserved. No access is allowed.

Address	Register	Symbol	Page
D6C0h	CAN0 Mailbox 28: Message Identifier	COMB28	562
D6C1h			
D6C2h			
D6C3h			
D6C4h			
D6C5h	CAN0 Mailbox 28: Data Length		
D6C6h	CAN0 Mailbox 28: Data Field		
D6C7h			
D6C8h			
D6C9h			
D6CAh			
D6CBh			
D6CCh			
D6CDh	CAN0 Mailbox 28: Time Stamp		
D6CEh			
D6CFh	COMB29	562	
D6D0h			CAN0 Mailbox 29: Message Identifier
D6D1h			
D6D2h			
D6D3h			
D6D4h			CAN0 Mailbox 29: Data Length
D6D5h			
D6D6h			CAN0 Mailbox 29: Data Field
D6D7h			
D6D8h			
D6D9h			
D6DAh			
D6DBh			
D6DCh			
D6DDh			CAN0 Mailbox 29: Time Stamp
D6DEh			
D6DFh	COMB30	562	
D6E0h			CAN0 Mailbox 30: Message Identifier
D6E1h			
D6E2h			
D6E3h			
D6E4h			CAN0 Mailbox 30: Data Length
D6E5h			
D6E6h			CAN0 Mailbox 30: Data Field
D6E7h			
D6E8h			
D6E9h			
D6EAh			
D6EBh			
D6ECh			
D6EDh			CAN0 Mailbox 30: Time Stamp
D6EEh			
D6EFh	COMB31	562	
D6F0h			CAN0 Mailbox 31: Message Identifier
D6F1h			
D6F2h			
D6F3h			
D6F4h			CAN0 Mailbox 31: Data Length
D6F5h			
D6F6h			CAN0 Mailbox 31: Data Field
D6F7h			
D6F8h			
D6F9h			
D6FAh			
D6FBh			
D6FCh			
D6FDh			CAN0 Mailbox 31: Time Stamp
D6FEh			
D6FFh			

Address	Register	Symbol	Page
D700h	CAN0 Mask Register 0	COMKR0	557
D701h			
D702h			
D703h			
D704h	CAN0 Mask Register 1	COMKR1	557
D705h			
D706h			
D707h	CAN0 Mask Register 2	COMKR2	557
D708h			
D709h			
D70Ah			
D70Bh	CAN0 Mask Register 3	COMKR3	557
D70Ch			
D70Dh			
D70Eh	CAN0 Mask Register 4	COMKR4	557
D70Fh			
D710h			
D711h			
D712h	CAN0 Mask Register 5	COMKR5	557
D713h			
D714h			
D715h	CAN0 Mask Register 6	COMKR6	557
D716h			
D717h			
D718h			
D719h	CAN0 Mask Register 7	COMKR7	557
D71Ah			
D71Bh			
D71Ch	CAN0 FIFO Receive ID Compare Register 0	COFIDCR0	558
D71Dh			
D71Eh			
D71Fh			
D720h	CAN0 FIFO Receive ID Compare Register 1	COFIDCR1	558
D721h			
D722h			
D723h	CAN0 Mask Invalid Register	COMKIVLR	560
D724h			
D725h			
D726h			
D727h	CAN0 Mailbox Interrupt Enable Register	COMIER	565
D728h			
D729h			
D72Ah	CAN0 Mailbox Interrupt Enable Register	COMIER	565
D72Bh			
D72Ch	CAN0 Mailbox Interrupt Enable Register	COMIER	565
D72Dh			
D72Eh	CAN0 Mailbox Interrupt Enable Register	COMIER	565
D72Fh			
D730h to D79Fh			
D7A0h	CAN0 Message Control Register 0	COMCTL0	566
D7A1h	CAN0 Message Control Register 1	COMCTL1	566
D7A2h	CAN0 Message Control Register 2	COMCTL2	566
D7A3h	CAN0 Message Control Register 3	COMCTL3	566
D7A4h	CAN0 Message Control Register 4	COMCTL4	566
D7A5h	CAN0 Message Control Register 5	COMCTL5	566
D7A6h	CAN0 Message Control Register 6	COMCTL6	566
D7A7h	CAN0 Message Control Register 7	COMCTL7	566
D7A8h	CAN0 Message Control Register 8	COMCTL8	566
D7A9h	CAN0 Message Control Register 9	COMCTL9	566
D7AAh	CAN0 Message Control Register 10	COMCTL10	566
D7ABh	CAN0 Message Control Register 11	COMCTL11	566
D7ACh	CAN0 Message Control Register 12	COMCTL12	566
D7ADh	CAN0 Message Control Register 13	COMCTL13	566
D7AEh	CAN0 Message Control Register 14	COMCTL14	566
D7AFh	CAN0 Message Control Register 15	COMCTL15	566

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Address	Register	Symbol	Page
D7B0h	CAN0 Message Control Register 16	COMCTL16	566
D7B1h	CAN0 Message Control Register 17	COMCTL17	566
D7B2h	CAN0 Message Control Register 18	COMCTL18	566
D7B3h	CAN0 Message Control Register 19	COMCTL19	566
D7B4h	CAN0 Message Control Register 20	COMCTL20	566
D7B5h	CAN0 Message Control Register 21	COMCTL21	566
D7B6h	CAN0 Message Control Register 22	COMCTL22	566
D7B7h	CAN0 Message Control Register 23	COMCTL23	566
D7B8h	CAN0 Message Control Register 24	COMCTL24	566
D7B9h	CAN0 Message Control Register 25	COMCTL25	566
D7BAh	CAN0 Message Control Register 26	COMCTL26	566
D7BBh	CAN0 Message Control Register 27	COMCTL27	566
D7BCh	CAN0 Message Control Register 28	COMCTL28	566
D7BDh	CAN0 Message Control Register 29	COMCTL29	566
D7BEh	CAN0 Message Control Register 30	COMCTL30	566
D7BFh	CAN0 Message Control Register 31	COMCTL31	566
D7C0h	CAN0 Control Register	C0CTLR	550
D7C1h			
D7C2h	CAN0 Status Register	C0STR	577
D7C3h			
D7C4h			
D7C5h	CAN0 Bit Configuration Register	C0BCR	555
D7C6h			
D7C7h	CAN0 Clock Select Register	C0CLKR	554
D7C8h	CAN0 Receive FIFO Control Register	C0RFCR	570
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	573
D7CAh	CAN0 Transmit FIFO Control Register	C0TFCR	574
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR	576
D7CCh	CAN0 Error Interrupt Enable Register	C0EIER	585
D7CDh	CAN0 Error Interrupt Source Judge Register	C0EIFR	587
D7CEh	CAN0 Receive Error Count Register	C0RECR	590
D7CFh	CAN0 Transmit Error Count Register	C0TECR	591
D7D0h	CAN0 Error Code Store Register	C0ECSR	592
D7D1h	CAN0 Channel Search Support Register	C0CSSR	583
D7D2h	CAN0 Mailbox Search Status Register	C0MSSR	581
D7D3h	CAN0 Mailbox Search Mode Register	C0MSMR	580
D7D4h	CAN0 Time Stamp Register	C0TSR	594
D7D5h			
D7D6h	CAN0 Acceptance Filter Support Register	C0AFSR	584
D7D7h			
D7D8h	CAN0 Test Control Register	C0TCR	595
D7D9h			
D7DAh			
D7DBh			
D7DCh			
D7DDh			
D7DEh			
D7DFh			

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FFFDBh	Optional Function Select Address 2	OFS2	206
FFFFFh	Optional Function Select Address 1	OFS1	205

The OFS1 and OFS2 addresses are not SFRs.

## **1. Overview**

### **1.1 Features**

The M16C/5L and M16C/56 Group's microcomputers (MCUs) are single-chip control units that utilize high-performance silicon gate CMOS technology with the M16C/60 Series CPU core. The M16C/5L Group and M16C/56 Group are available in 64-pin and 80-pin plastic molded LQFP packages. The MCUs employ sophisticated instructions for a high level of efficiency and they are capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier and DMAC for high-speed operation processing which makes it adequate for controlling office equipment, home appliances, and industrial equipment.

The M16C/5L Group has one CAN module, which makes it suitable for automotive control, and factory automation LAN system.

#### **1.1.1 Applications**

Automotive, car audio, factory automation LAN system, etc.

## 1.2 Specifications

Table 1.1 to Table 1.4 list specifications of the M16C/5L Group, M16C/56 Group.

**Table 1.1 Specifications (80-pin Package) (1/2)**

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: $16 \times 16 \rightarrow 32$ bits, Multiply-accumulate unit: $16 \times 16 + 32 \rightarrow 32$ bits) <ul style="list-style-type: none"> <li>Basic instructions: 91</li> <li>Minimum instruction execution time: 31.25 ns (<math>f(\text{BCLK}) = 32</math> MHz, <math>V_{CC} = 3.0</math> to 5.5 V)</li> <li>Operating mode: Single-chip mode</li> </ul>
Memory	ROM, RAM, data flash	See Table 1.5 and Table 1.6.
Voltage Detection	Voltage detector	<ul style="list-style-type: none"> <li>2 voltage detect points</li> </ul>
Clock	Clock generator	<ul style="list-style-type: none"> <li>5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator)</li> <li>Oscillation stop detector: Main clock oscillator stop/restart detection</li> <li>Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable</li> <li>Low-power consumption modes: Wait mode, stop mode</li> <li>Real-time clock</li> </ul>
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> <li>71 CMOS inputs/outputs, a pull-up resistor selectable</li> </ul>
Interrupts		<ul style="list-style-type: none"> <li>Interrupt vectors: 70</li> <li>External interrupt inputs: 11 (<math>\overline{\text{NMI}}</math>, <math>\overline{\text{INT}} \times 6</math>, key input <math>\times 4</math>)</li> <li>Interrupt priority levels: 7</li> </ul>
Watchdog Timer		<ul style="list-style-type: none"> <li>15 bits <math>\times 1</math> (with prescaler)</li> <li>Automatic reset start function selectable</li> <li>Dedicated 125 kHz on-chip oscillator for the watchdog timer contained</li> </ul>
DMA	DMAC	<ul style="list-style-type: none"> <li>4 channels, Cycle-steal transfer mode</li> <li>Trigger sources: 41</li> <li>Transfer modes: 2 (single transfer, repeat transfer)</li> </ul>
Timers	Timer A	16-bit timer $\times 5$ Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) $\times 3$ Programmable output mode $\times 3$
	Timer B	16-bit timer $\times 3$ Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer $\times 1$ (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/output compare)	<ul style="list-style-type: none"> <li>16-bit timer <math>\times 1</math> (base timer)</li> <li>I/O: 8 channels</li> </ul>
	Task monitoring timer	16-bit timer $\times 1$ channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART4	4 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I <sup>2</sup> C-bus, IEBus)
Multi-master I <sup>2</sup> C-bus Interface		1 channel
A/D Converter		10-bit resolution $\times 27$ channels

**Table 1.2 Specifications (80-pin Package) (2/2)**

Item	Function	Specification
CRC Calculator		<ul style="list-style-type: none"> <li>• 1 circuit</li> <li>• CRC-CCITT (<math>X^{16} + X^{12} + X^5 + 1</math>), CRC-16 (<math>X^{16} + X^{15} + X^2 + 1</math>) compliant</li> <li>• MSB/LSB selectable</li> </ul>
CAN Module		32-slot message buffer × 1 channel (M16C/5L Group only)
Flash Memory		<ul style="list-style-type: none"> <li>• Programming and erasure supply voltage: 3.0 to 5.5 V</li> <li>• Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash)</li> <li>• Program security: ROM code protect, ID code check</li> </ul>
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V
Current Consumption		Described in 27. "Electrical Characteristics"
Operating Temperature		-40°C to 85°C -40°C to 125°C (1)
Package		80-pin plastic mold LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

## Note:

1. Refer to Table 1.5 "Product List of M16C/5L Group" and Table 1.6 "Product List of M16C/56 Group" for Operating Temperature.



**Table 1.3 Specifications (64-pin Package) (1/2)**

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits) <ul style="list-style-type: none"> <li>• Basic instructions: 91</li> <li>• Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC = 3.0 to 5.5 V)</li> <li>• Operating mode: Single-chip mode</li> </ul>
Memory	ROM, RAM, data flash	See Table 1.5 and Table 1.6.
Voltage Detection	Voltage detector	<ul style="list-style-type: none"> <li>• 2 voltage detect points</li> </ul>
Clock	Clock generator	<ul style="list-style-type: none"> <li>• 5 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator)</li> <li>• Oscillation stop detector: Main clock oscillator stop/restart detection</li> <li>• Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable</li> <li>• Low-power consumption modes: Wait mode, stop mode</li> <li>• Real-time clock</li> </ul>
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> <li>• 55 CMOS inputs/outputs, a pull-up resistor selectable</li> </ul>
Interrupts		<ul style="list-style-type: none"> <li>• Interrupt vectors: 70</li> <li>• External interrupt inputs: 11 (<math>\overline{\text{NMI}}</math>, <math>\overline{\text{INT}} \times 6</math>, key input <math>\times 4</math>)</li> <li>• Interrupt priority levels: 7</li> </ul>
Watchdog Timer		<ul style="list-style-type: none"> <li>• 15 bits × 1 (with prescaler)</li> <li>• Automatic reset start function selectable</li> <li>• Dedicated 125 kHz on-chip oscillator for the watchdog timer contained</li> </ul>
DMA	DMAC	<ul style="list-style-type: none"> <li>• 4 channels, Cycle-steal transfer mode</li> <li>• Trigger sources: 39</li> <li>• Transfer modes: 2 (single transfer, repeat transfer)</li> </ul>
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/output compare)	<ul style="list-style-type: none"> <li>• 16-bit timer × 1 (base timer)</li> <li>• I/O: 8 channels</li> </ul>
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART3	3 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I <sup>2</sup> C-bus, IEBus)
Multi-master I <sup>2</sup> C-bus Interface		1 channel
A/D Converter		10-bit resolution × 16 channels

**Table 1.4 Specifications (64-pin Package) (2/2)**

Item	Function	Specification
CRC Calculator		<ul style="list-style-type: none"> <li>• 1 circuit</li> <li>• CRC-CCITT (<math>X^{16} + X^{12} + X^5 + 1</math>), CRC-16 (<math>X^{16} + X^{15} + X^2 + 1</math>) compliant</li> <li>• MSB/LSB selectable</li> </ul>
CAN Module		32-slot message buffer × 1 channel (M16C/5L Group only)
Flash Memory		<ul style="list-style-type: none"> <li>• Programming and erasure supply voltage: 3.0 to 5.5 V</li> <li>• Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash)</li> <li>• Program security: ROM code protect, ID code check</li> </ul>
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V
Current Consumption		Described in 27. "Electrical Characteristics"
Operating Temperature		-40°C to 85°C -40°C to 125°C (1)
Package		64-pin plastic mold LQFP: PLQP0064KB-A (Previous package code: 64P6Q-A)

## Note:

1. Refer to Table 1.5 "Product List of M16C/5L Group" and Table 1.6 "Product List of M16C/56 Group" for Operating Temperature.

### 1.3 Product List

Table 1.5 and Table 1.6 list product information on the M16C/5L Group, M16C/56 Group. Figure 1.1 shows part numbers, memory sizes, and packages. Figure 1.2 shows marking drawing (top view).

**Table 1.5 Product List of M16C/5L Group**

As of September 2011

Part Number	ROM Capacity			RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash				
R5F35L30JFF	64 KB	16 KB	4 KB x 2 blocks	4 KB	1 channel	PLQP0064KB-A	Operating Temperature -40°C to 85°C
R5F35L23JFE	96 KB	16 KB	4 KB x 2 blocks	8 KB		PLQP0080KB-A	
R5F35L33JFF						PLQP0064KB-A	
R5F35L26JFE	128 KB	16 KB	4 KB x 2 blocks	12 KB		PLQP0080KB-A	
R5F35L36JFF						PLQP0064KB-A	
R5F35L2EJFE	256 KB	16 KB	4 KB x 2 blocks	20 KB		PLQP0080KB-A	
R5F35L3EJFF						PLQP0064KB-A	
R5F35L30KFF	64 KB	16 KB	4 KB x 2 blocks	4 KB		PLQP0064KB-A	Operating Temperature -40°C to 125°C
R5F35L23KFE	96 KB	16 KB	4 KB x 2 blocks	8 KB		PLQP0080KB-A	
R5F35L33KFF						PLQP0064KB-A	
R5F35L26KFE	128 KB	16 KB	4 KB x 2 blocks	12 KB		PLQP0080KB-A	
R5F35L36KFF						PLQP0064KB-A	
R5F35L2EKFE	256 KB	16 KB	4 KB x 2 blocks	20 KB		PLQP0080KB-A	
R5F35L3EKFF						PLQP0064KB-A	

(D): Under development

(P): Under planning

The old package names are as follows:

PLQP0080KB-A: 80P6Q-A PLQP0064KB-A: 64P6Q-A

**Table 1.6 Product List of M16C/56 Group**

As of September 2011

Part Number	ROM Capacity			RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash				
R5F35630JFF	64 KB	16 KB	4 KB x 2 blocks	4 KB	N/A	PLQP0064KB-A	Operating Temperature -40°C to 85°C
R5F35623JFE	96 KB	16 KB	4 KB x 2 blocks	8 KB		PLQP0080KB-A	
R5F35633JFF						PLQP0064KB-A	
R5F35626JFE	128 KB	16 KB	4 KB x 2 blocks	12 KB		PLQP0080KB-A	
R5F35636JFF						PLQP0064KB-A	
R5F3562EJFE	256 KB	16 KB	4 KB x 2 blocks	20 KB		PLQP0080KB-A	
R5F3563EJFF						PLQP0064KB-A	
R5F35630KFF	64 KB	16 KB	4 KB x 2 blocks	4 KB		PLQP0064KB-A	Operating Temperature -40°C to 125°C
R5F35623KFE	96 KB	16 KB	4 KB x 2 blocks	8 KB		PLQP0080KB-A	
R5F35633KFF						PLQP0064KB-A	
R5F35626KFE	128 KB	16 KB	4 KB x 2 blocks	12 KB		PLQP0080KB-A	
R5F35636KFF						PLQP0064KB-A	
R5F3562EKFE	256 KB	16 KB	4 KB x 2 blocks	20 KB		PLQP0080KB-A	
R5F3563EKFF						PLQP0064KB-A	

(D): Under development

(P): Under planning

The old package names are as follows:

PLQP0080KB-A: 80P6Q-A PLQP0064KB-A: 64P6Q-A

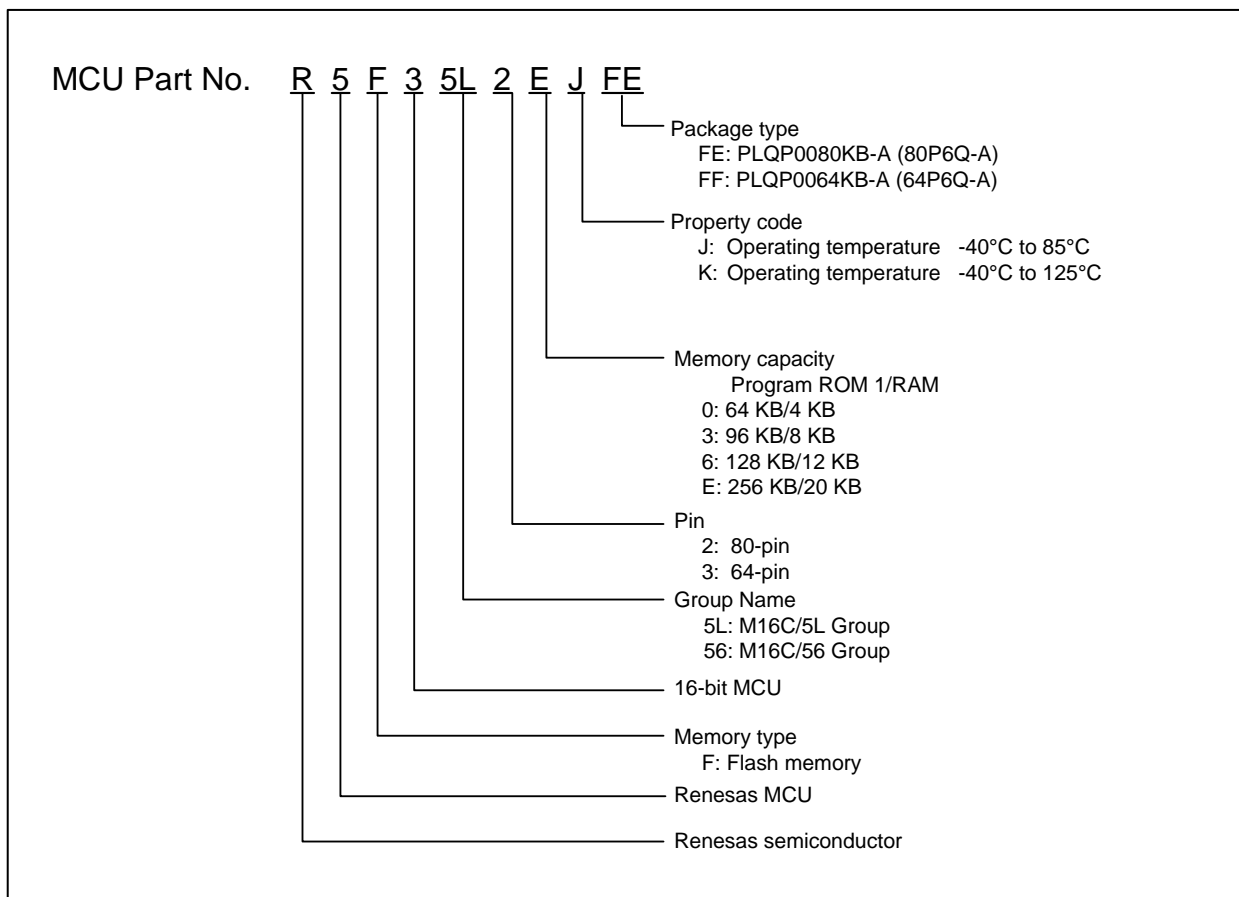


Figure 1.1 Correspondence of Part Number, Memory Size, and Package

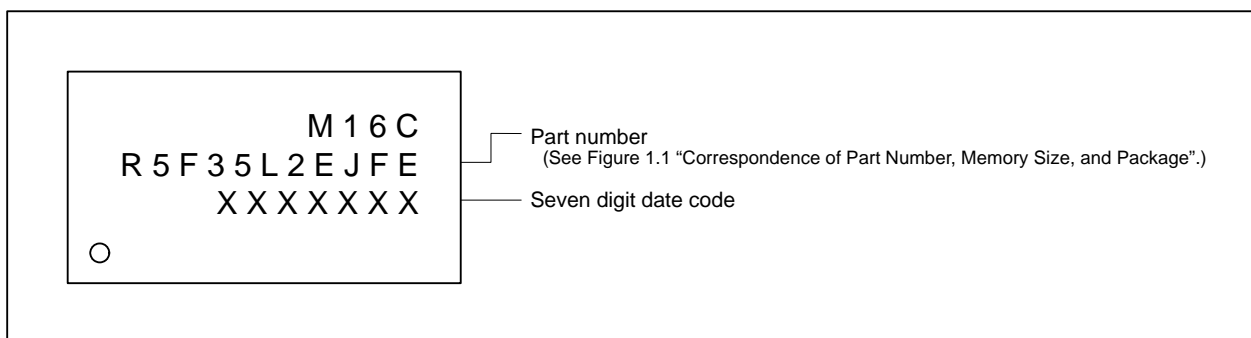


Figure 1.2 Marking Diagram of Flash Memory Version (Top View)

### 1.4 Block Diagram

Figure 1.3 shows a block diagram of M16C/5L Group, M16C/56 Group 80-pin package. Figure 1.4 shows a block diagram of the M16C/5L Group, M16C/56 Group 64-pin package.

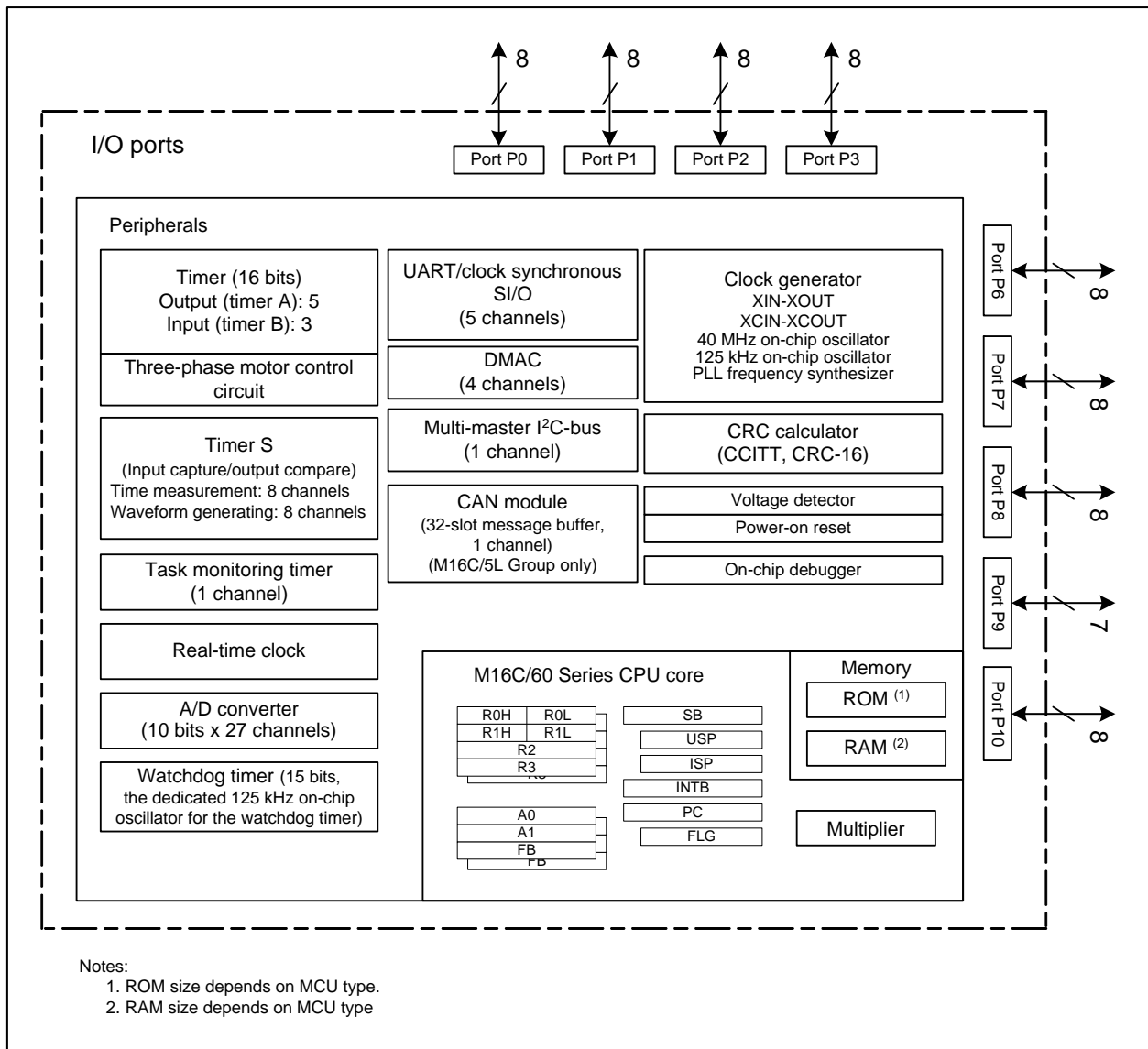


Figure 1.3 80-Pin Block Diagram

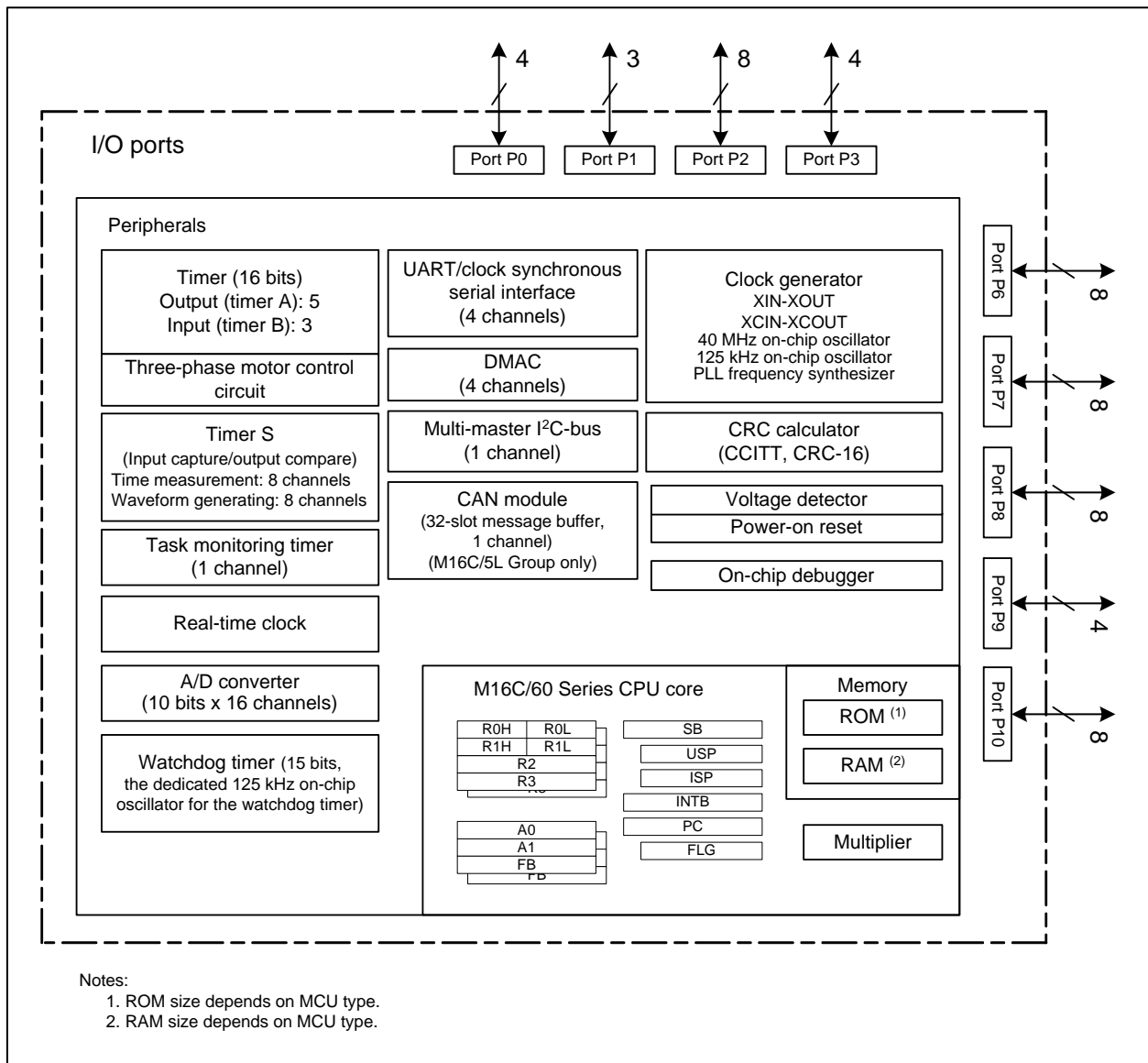
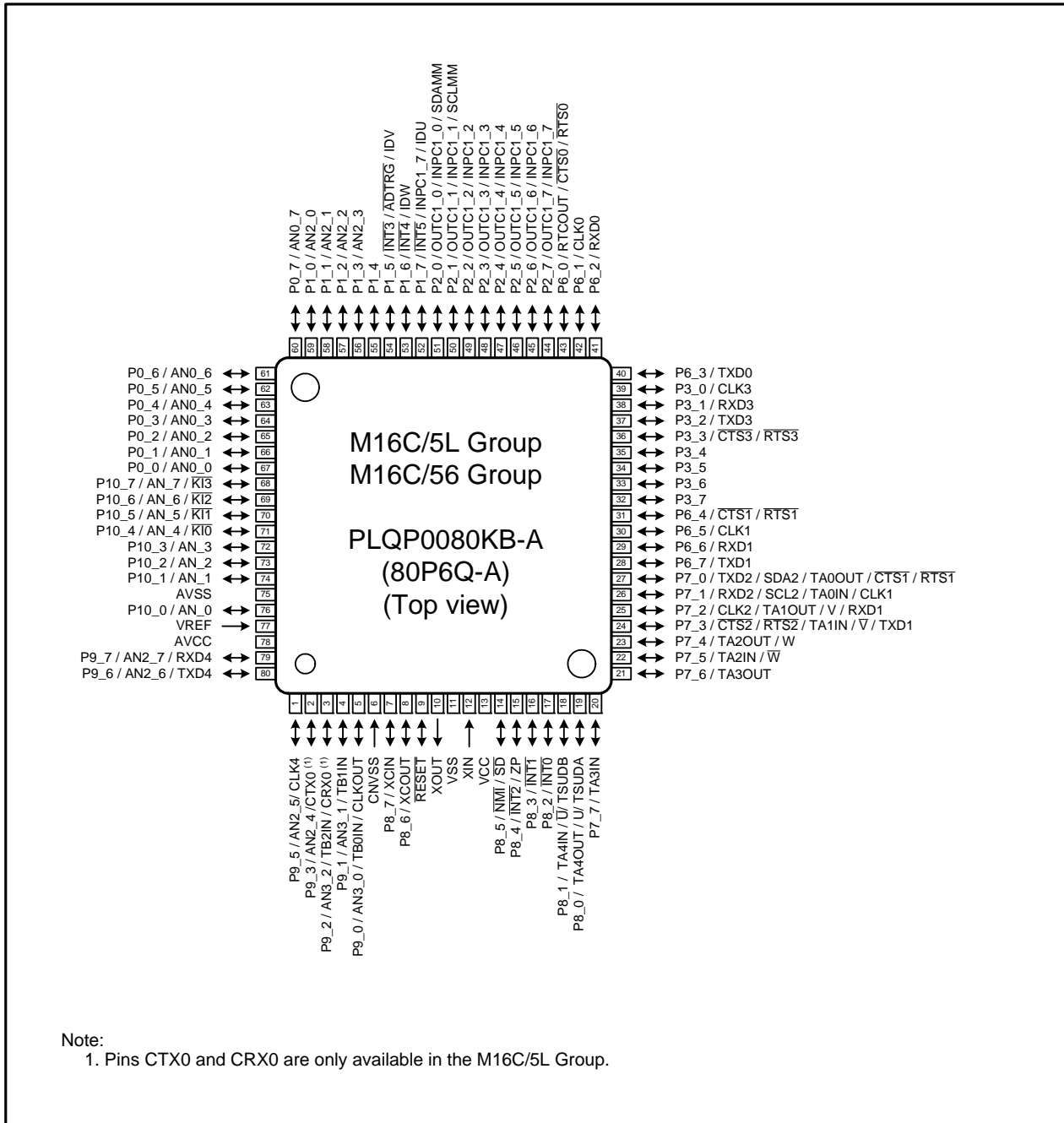


Figure 1.4 64-Pin Block Diagram

### 1.5 Pin Assignments

Figure 1.5 shows the pin assignments for 80-pin package and Figure 1.6 shows the pin assignments for 64-pin package.



**Figure 1.5 Pin Assignment for 80-Pin Package (Top View)**

Set bits PACR2 to PACR0 in the PACR register to 011b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

**Table 1.7 Pin Names, 80-Pin Package (1/2)**

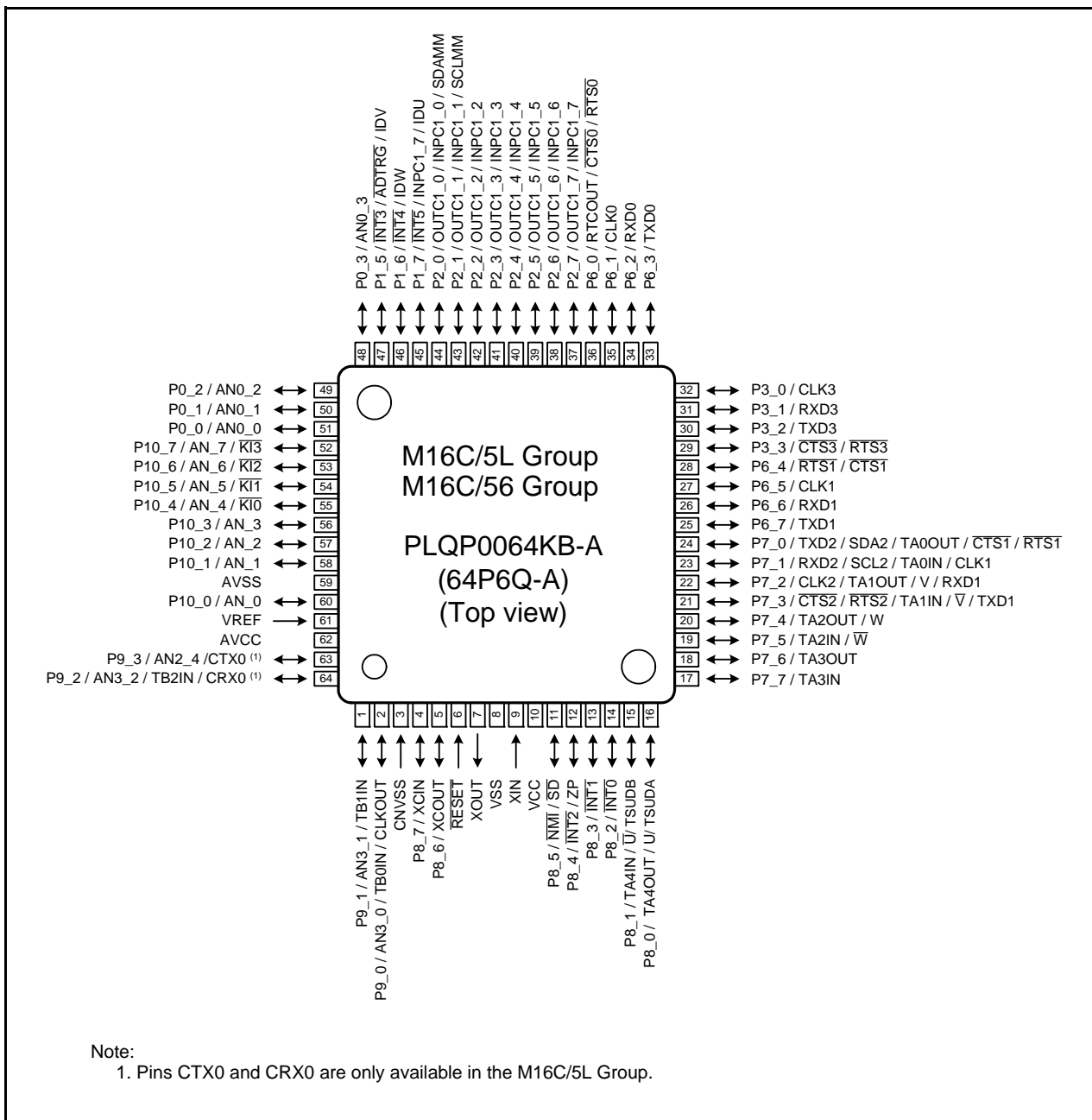
Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I <sup>2</sup> C-bus pin	Analog Pin
1		P9_5				CLK4		AN2_5
2		P9_3				CTX0 (1)		AN2_4
3		P9_2		TB2IN		CRX0 (1)		AN3_2
4		P9_1		TB1IN				AN3_1
5	CLKOUT	P9_0		TB0IN				AN3_0
6	CNVSS							
7	XCIN	P8_7						
8	XCOU	P8_6						
9	RESET							
10	XOUT							
11	VSS							
12	XIN							
13	VCC							
14		P8_5	NMI	SD				
15		P8_4	INT2	ZP				
16		P8_3	INT1					
17		P8_2	INT0					
18		P8_1		TA4IN/U	TSUDB			
19		P8_0		TA4OUT/U	TSUDA			
20		P7_7		TA3IN				
21		P7_6		TA3OUT				
22		P7_5		TA2IN/W				
23		P7_4		TA2OUT/W				
24		P7_3		TA1IN/V		CTS2/RTS2/TXD1		
25		P7_2		TA1OUT/V		CLK2/RXD1		
26		P7_1		TA0IN		RXD2/SCL2/CLK1		
27		P7_0		TA0OUT		TXD2/SDA2/CTS1/RTS1		
28		P6_7				TXD1		
29		P6_6				RXD1		
30		P6_5				CLK1		
31		P6_4				CTS1/RTS1		
32		P3_7						
33		P3_6						
34		P3_5						
35		P3_4						
36		P3_3				CTS3/RTS3		
37		P3_2				TXD3		
38		P3_1				RXD3		
39		P3_0				CLK3		
40		P6_3				TXD0		

Note 1. There are pins CTX0 and CRX0 only in the M16C/5L Group



**Table 1.8 Pin Names, 80-Pin Package (2/2)**

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I <sup>2</sup> C-bus pin	Analog Pin
41		P6_2				RXD0		
42		P6_1				CLK0		
43		P6_0		RTCOUT		CTS0/RTS0		
44		P2_7			OUTC1_7/INPC1_7			
45		P2_6			OUTC1_6/INPC1_6			
46		P2_5			OUTC1_5/INPC1_5			
47		P2_4			OUTC1_4/INPC1_4			
48		P2_3			OUTC1_3/INPC1_3			
49		P2_2			OUTC1_2/INPC1_2			
50		P2_1			OUTC1_1/INPC1_1		SCLMM	
51		P2_0			OUTC1_0/INPC1_0		SDAMM	
52		P1_7	INT5	IDU	INPC1_7			
53		P1_6	INT4	IDW				
54		P1_5	INT3	IDV				ADTRG
55		P1_4						
56		P1_3						AN2_3
57		P1_2						AN2_2
58		P1_1						AN2_1
59		P1_0						AN2_0
60		P0_7						AN0_7
61		P0_6						AN0_6
62		P0_5						AN0_5
63		P0_4						AN0_4
64		P0_3						AN0_3
65		P0_2						AN0_2
66		P0_1						AN0_1
67		P0_0						AN0_0
68		P10_7	KI3					AN_7
69		P10_6	KI2					AN_6
70		P10_5	KI1					AN_5
71		P10_4	KI0					AN_4
72		P10_3						AN_3
73		P10_2						AN_2
74		P10_1						AN_1
75	AVSS							
76		P10_0						AN_0
77	VREF							
78	AVCC							
79		P9_7				RXD4		AN2_7
80		P9_6				TXD4		AN2_6



**Figure 1.6 Pin Assignment for 64-Pin Package (Top View)**

Set bits PACR2 to PACR0 in the PACR register to 010b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

**Table 1.9 Pin Names, 64-Pin Package (1/2)**

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I <sup>2</sup> C-bus pin	Analog Pin
1		P9_1		TB1IN				AN3_1
2	CLKOUT	P9_0		TB0IN				AN3_0
3	CNVSS							
4	XCIN	P8_7						
5	XCOU	P8_6						
6	RESET							
7	XOUT							
8	VSS							
9	XIN							
10	VCC							
11		P8_5	NMI	SD				
12		P8_4	INT2	ZP				
13		P8_3	INT1					
14		P8_2	INT0					
15		P8_1		TA4IN/U	TSUDB			
16		P8_0		TA4OUT/U	TSUDA			
17		P7_7		TA3IN				
18		P7_6		TA3OUT				
19		P7_5		TA2IN/W				
20		P7_4		TA2OUT/W				
21		P7_3		TA1IN/V		CTS2/RTS2/TXD1		
22		P7_2		TA1OUT/V		CLK2/RXD1		
23		P7_1		TA0IN		RXD2/SCL2/CLK1		
24		P7_0		TA0OUT		TXD2/SDA2/CTS1/RTS1		
25		P6_7				TXD1		
26		P6_6				RXD1		
27		P6_5				CLK1		
28		P6_4				CTS1/RTS1		
29		P3_3				CTS3/RTS3		
30		P3_2				TXD3		
31		P3_1				RXD3		
32		P3_0				CLK3		
33		P6_3				TXD0		
34		P6_2				RXD0		
35		P6_1				CLK0		
36		P6_0		RTCOUT		CTS0/RTS0		
37		P2_7			OUTC1_7/INPC1_7			
38		P2_6			OUTC1_6/INPC1_6			
39		P2_5			OUTC1_5/INPC1_5			
40		P2_4			OUTC1_4/INPC1_4			

**Table 1.10 Pin Names, 64-Pin Package (2/2)**

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I <sup>2</sup> C-bus pin	Analog Pin
41		P2_3			OUTC1_3/INPC1_3			
42		P2_2			OUTC1_2/INPC1_2			
43		P2_1			OUTC1_1/INPC1_1		SCLMM	
44		P2_0			OUTC1_0/INPC1_0		SDAMM	
45		P1_7	INT5	IDU	INPC1_7			
46		P1_6	INT4	IDW				
47		P1_5	INT3	IDV				ADTRG
48		P0_3						AN0_3
49		P0_2						AN0_2
50		P0_1						AN0_1
51		P0_0						AN0_0
52		P10_7	KI3					AN_7
53		P10_6	KI2					AN_6
54		P10_5	KI1					AN_5
55		P10_4	KI0					AN_4
56		P10_3						AN_3
57		P10_2						AN_2
58		P10_1						AN_1
59	AVSS							
60		P10_0						AN_0
61	VREF							
62	AVCC							
63		P9_3				CTX0 (1)		AN2_4
64		P9_2		TB2IN		CRX0 (1)		AN3_2

Note 1. There are pins CTX0 and CRX0 only in the M16C/5L Group.

## 1.6 Pin Functions

**Table 1.11 Pin Functions (64-Pin and 80-Pin Packages) (1/2)**

Signal Name	Pin Name	I/O	Description
Power supply	VCC, VSS	I	Apply 3.0 to 5.5 V to VCC pin and 0 V to VSS pin.
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. Pins AVCC and AVSS should be connected to VCC and VSS, respectively.
Reset input	RESET	I	Driving this low resets the MCU.
CNVSS	CNVSS	I	Connect to VSS via a resistor.
Main clock input	XIN	I	Input/output for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. <sup>(1)</sup> To apply an external clock, connect it to XIN and leave XOUT open. When XIN is not used, connect XIN to VCC pin and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. Connect a crystal oscillator between XCIN and XCOU. <sup>(1)</sup>
Sub clock output	XCOU	O	
Clock output	CLKOUT	O	This pin outputs the clock having the same frequency as f <sub>1</sub> , f <sub>8</sub> , f <sub>32</sub> , or f <sub>C</sub> .
INT interrupt input	INT0 to INT5	I	Input for INT interrupt.
NMI input	NMI	I	Input for NMI interrupt.
Key input interrupt	KI0 to KI3	I	Input for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
	ZP	I	Input for Z-phase
Timer B	TB0IN to TB2IN	I	Timers B0 to B2 input
Three-phase motor control timer	U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$	O	Output for three-phase motor control timer
	IDU, IDW, IDV, $\bar{SD}$	I	Input for three-phase motor control timer
Real-time clock	RTCOUT	O	Output for real-time clock
Serial interface UART0 to UART3	$\bar{CTS}0$ to $\bar{CTS}3$	I	Input to control data transmission
	RTS0 to RTS3	O	Output to control data reception
	CLK0 to CLK3	I/O	Transfer clock input/output
	RXD0 to RXD3	I	Serial data input
	TXD0 to TXD3	O	Serial data output
UART2 I <sup>2</sup> C mode	SDA2	I/O	Serial data input/output
	SCL2	I/O	Transfer clock input/output
Multi-master I <sup>2</sup> C-bus	SDAMM	I/O	Serial data input/output
	SCLMM		Transfer clock input/output

Note:

1. Please contact the manufacturer of crystal/ceramic resonator for oscillation characteristic.

**Table 1.12 Pin Functions (64-Pin and 80-Pin Packages) (2/2)**

Signal Name	Pin Name	I/O	Description
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.
A/D converter	AN_0 to AN_7 AN0_0 to AN0_3 AN2_4 AN3_0 to AN3_2	I	Analog input
	ADTRG	I	Input for an external trigger
Timer S	INPC1_0 to INPC1_7	I	Input for time measurement function
	OUTC1_0 to OUTC1_7	O	Output for waveform generating function
	TSUDA, TSUDB	I	Two-phase pulse input
CAN module (1)	CRX0	I	Receive data input for CAN communication
	CTX0	O	Transmit data output for CAN communication
I/O port	P0_0 to P0_3 P1_5 to P1_7 P2_0 to P2_7 P3_0 to P3_3 P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_3 P10_0 to P10_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, a pull-up resistor is selectable for every unit of 4 bits.

Note:

1. The CAN module is only in the M16C/5L Group.

**Table 1.13 Pin Functions (80-Pin Package Only)**

Signal Name	Pin Name	I/O	Description
Serial interface UART4	CLK4	I/O	Transfer clock I/O pin
	RXD4	I	Serial data input pin
	TXD4	O	Serial data output pin
A/D converter	AN0_4 to AN0_7 AN2_0 to AN2_3 AN2_5 to AN2_7	I	Analog input
I/O port	P0_4 to P0_7 P1_0 to P1_4 P3_4 to P3_7 P9_5 to P9_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, Pull-up resistor is selectable for every unit of 4 bits.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.

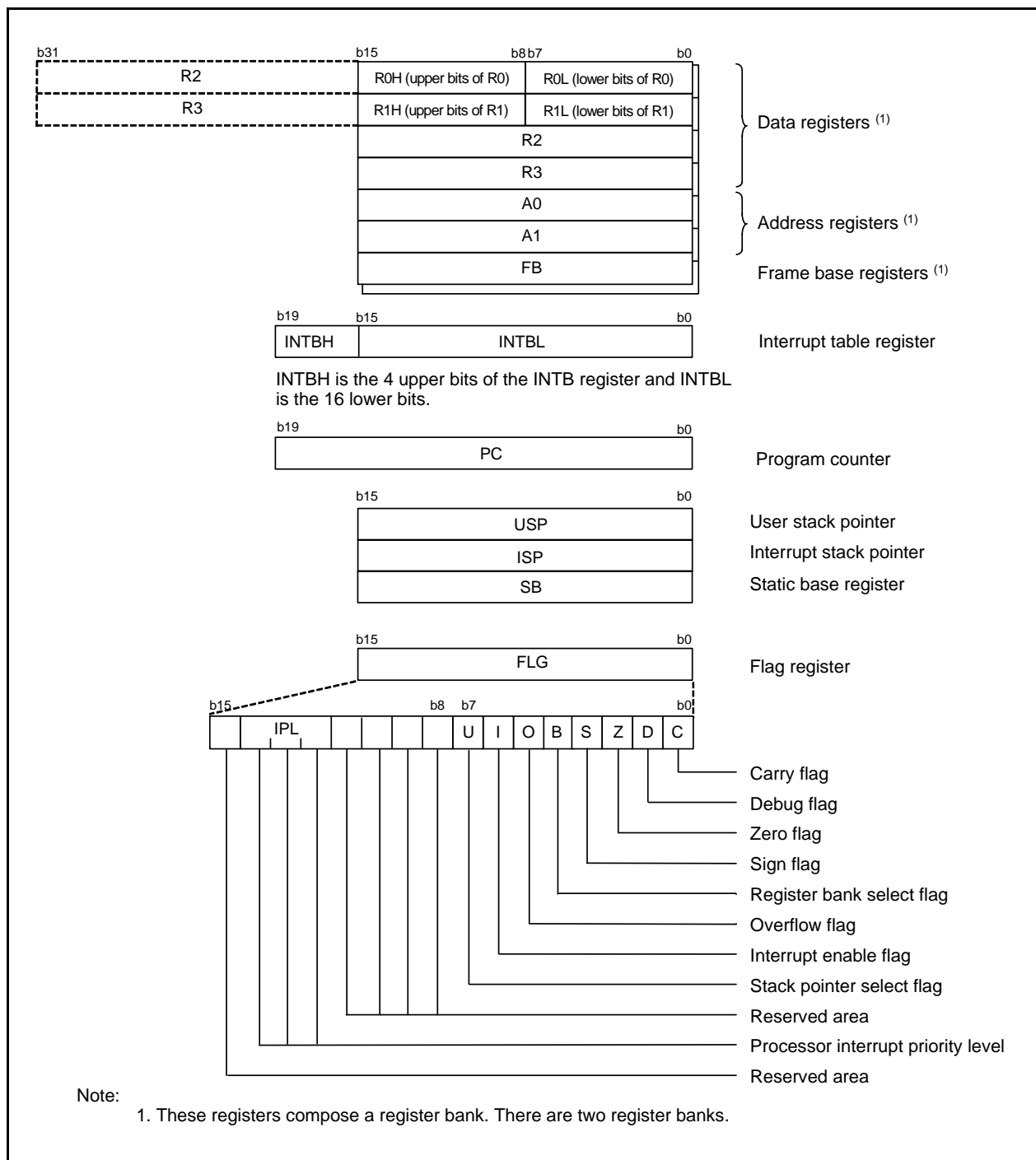


Figure 2.1 CPU Registers



## 2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers.

R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

## 2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

## 2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

### 2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

### 2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

### **2.8.7 Interrupt Enable Flag (I Flag)**

The I flag enables maskable interrupts.

Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

### **2.8.8 Stack Pointer Select Flag (U Flag)**

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.

The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.

If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

### **2.8.10 Reserved Areas**

Only set these bits to 0. The read value is undefined.

### 3. Memory

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank spaces within SFRs are reserved, so do not access any blank spaces.

The internal RAM is allocated from address 00400h to superior direction. For example, a 8 KB internal RAM is addressed from 00400h to 023FFh. The internal RAM is used not only for data storage but also for stack area when subroutines are called or when interrupt request are acknowledged.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is addressed from 0E000h to 0FFFFh. This data flash space is used not only for data storage but also for program storage.

Program ROM 2 is assigned addresses 10000h to 13FFFh. Program ROM 1 is assigned addresses FFFFFh to inferior direction. For example, the 64 KB program ROM 1 space has addresses F0000h to FFFFFh.

The special page vectors are assigned addresses FFE00h to FFFD7h. They are used for the JMPS instruction and JSRS instruction. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts, ID code write address, OFS1 address and OSF2 address are assigned addresses FFFDBh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

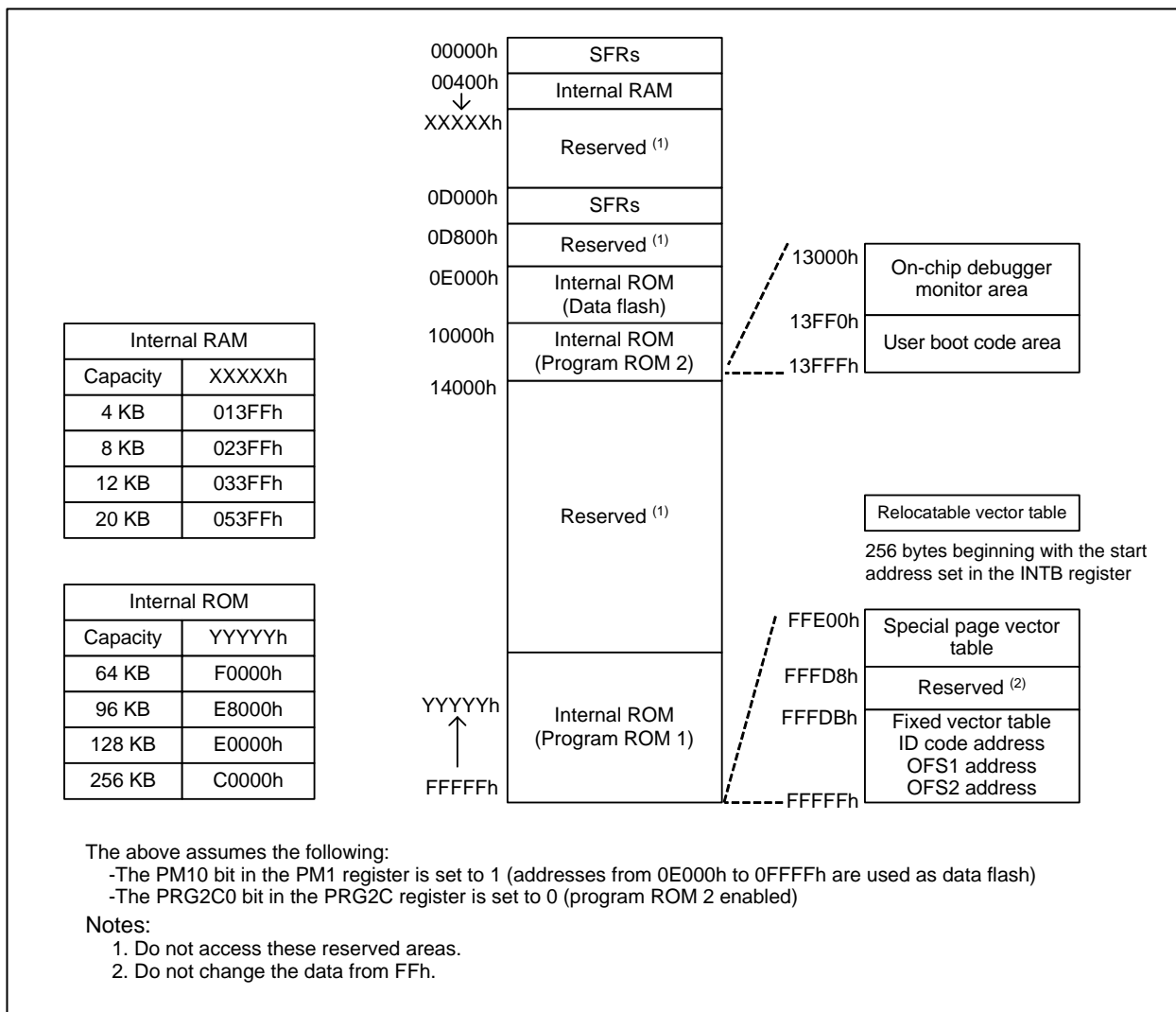


Figure 3.1 Memory Map

## 4. Special Function Registers (SFRs)

### 4.1 SFRs

An SFR is a control register for a peripheral function.

**Table 4.1 SFR Information (1) (1)**

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (3)
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h			
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX0X 001Xb (hardware reset) (4)
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (2)
001Ah	Voltage Detector Operation Enable Register	VCR2	000X 0000b (2, 5) 001X 0000b (2, 6)
001Bh			
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

X: Undefined

**Notes:**

1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, and voltage monitor 2 reset do not affect the following registers: registers VCR1 and VCR2.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value when the LVDAS bit of the OFS1 address is 1 during hardware reset.
6. This is the reset value after voltage monitor 0 reset, power-on reset, or when the LVDAS bit of the OFS1 address is 0 during hardware reset.

**Table 4.2 SFR Information (2) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0023h			
0024h	40 MHz On-Chip Oscillator Control Register 2	FRA2	0XX0 X000b
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	00h
0027h			
0028h	Voltage Detector 2 Level Select Register	VD2LS	0000 0100b <sup>(2)</sup>
0029h			
002Ah	Voltage Monitor 0 Control Register	VW0C	1100 1X10b <sup>(3, 4)</sup> 1100 1X11b <sup>(3, 5)</sup>
002Bh			
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b <sup>(3, 6)</sup>
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

## Notes:

1. The blank areas are reserved. No access is allowed.
2. Hardware reset, power-on reset, voltage monitor 0 reset, or voltage monitor 2 reset.
3. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 0 reset, and voltage monitor 2 reset do not affect the following registers or bit: the VW0C register, and bits VW2C2 and VW2C3 in the VW2C register.
4. This is the reset value when the LVDAS bit of the OFS1 address is 1 during hardware reset
5. This is the reset value after voltage monitor 0 reset, power-on reset, or when the LVDAS bit of the OFS1 address is 0 during hardware reset.
6. This is the reset value after hardware reset, power-on reset, or voltage monitor 0 reset

**Table 4.3 SFR Information (3) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	XX00 X000b
0045h			
0046h			
0047h			
0048h	INT5 Interrupt Control Register	INT5IC	XX00 X000b
0049h	INT4 Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register Task Monitoring Timer Interrupt Control Register	BCNIC TMOSIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

## Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.4 SFR Information (4) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh	UART4 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S4TIC RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register CAN0 Error Interrupt Control Register	S3TIC C0EIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register	RTCTIC	XXXX X000b
0075h	CAN0 Reception Complete Interrupt Control Register	C0RIC	XXXX X000b
0076h	CAN0 Transmission Complete Interrupt Control Register	C0TIC	XXXX X000b
0077h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0078h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I2C-bus Interface Interrupt Control Register	ICOC1IC IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b
0080h to 017Fh			

X: Undefined

## Note:

1. The blank areas are reserved. No access is allowed.



**Table 4.5 SFR Information (5) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.6 SFR Information (6) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:

- The blank areas are reserved. No access is allowed.

**Table 4.7 SFR Information (7) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Task Monitor Timer Register	TMOS	XXh
01F1h			XXh
01F2h	Task Monitor Timer Count Start Flag	TMOSSR	XXXX XXX0b
01F3h	Task Monitor Timer Count Source Select Register	TMOSCS	XXXX 0000b
01F4h	Task Monitor Timer Protect Register	TMOSPR	00h
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.8 SFR Information (8) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.9 SFR Information (9) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h			
0245h			
0246h			
0247h			
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h			
0251h			
0252h	UART Clock Select Register	UCLKSELO	X0h
0253h			
0254h			
0255h			
0256h			
0257h			
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.10 SFR Information (10) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h			
0291h			
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.11 SFR Information (11) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h	Time Measurement Register 0	G1TM0	XXh
02C1h	Waveform Generation Register 0	G1PO0	XXh
02C2h	Time Measurement Register 1	G1TM1	XXh
02C3h	Waveform Generation Register 1	G1PO1	XXh
02C4h	Time Measurement Register 2	G1TM2	XXh
02C5h	Waveform Generation Register 2	G1PO2	XXh
02C6h	Time Measurement Register 3	G1TM3	XXh
02C7h	Waveform Generation Register 3	G1PO3	XXh
02C8h	Time Measurement Register 4	G1TM4	XXh
02C9h	Waveform Generation Register 4	G1PO4	XXh
02CAh	Time Measurement Register 5	G1TM5	XXh
02CBh	Waveform Generation Register 5	G1PO5	XXh
02CCh	Time Measurement Register 6	G1TM6	XXh
02CDh	Waveform Generation Register 6	G1PO6	XXh
02CEh	Time Measurement Register 7	G1TM7	XXh
02CFh	Waveform Generation Register 7	G1PO7	XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.12 SFR Information (12) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
02D0h	Waveform Generation Control Register 0	G1POCR0	0X00 XX00b
02D1h	Waveform Generation Control Register 1	G1POCR1	0X00 XX00b
02D2h	Waveform Generation Control Register 2	G1POCR2	0X00 XX00b
02D3h	Waveform Generation Control Register 3	G1POCR3	0X00 XX00b
02D4h	Waveform Generation Control Register 4	G1POCR4	0X00 XX00b
02D5h	Waveform Generation Control Register 5	G1POCR5	0X00 XX00b
02D6h	Waveform Generation Control Register 6	G1POCR6	0X00 XX00b
02D7h	Waveform Generation Control Register 7	G1POCR7	0X00 XX00b
02D8h	Time Measurement Control Register 0	G1TMCR0	00h
02D9h	Time Measurement Control Register 1	G1TMCR1	00h
02DAh	Time Measurement Control Register 2	G1TMCR2	00h
02DBh	Time Measurement Control Register 3	G1TMCR3	00h
02DCh	Time Measurement Control Register 4	G1TMCR4	00h
02DDh	Time Measurement Control Register 5	G1TMCR5	00h
02DEh	Time Measurement Control Register 6	G1TMCR6	00h
02DFh	Time Measurement Control Register 7	G1TMCR7	00h
02E0h	Base Timer Register	G1BT	XXh
02E1h			XXh
02E2h	Base Timer Control Register 0	G1BCR0	00h
02E3h	Base Timer Control Register 1	G1BCR1	00h
02E4h	Time Measurement Prescaler Register 6	G1TPR6	00h
02E5h	Time Measurement Prescaler Register 7	G1TPR7	00h
02E6h	Function Enable Register	G1FE	00h
02E7h	Function Select Register	G1FS	00h
02E8h	Base Timer Reset Register	G1BTRR	XXh
02E9h			XXh
02EAh	Count Source Divide Register	G1DV	00h
02EBh			
02ECh	Waveform Output Master Enable Register	G1OER	00h
02EDh			
02EEh	Timer S I/O Control Register 0	G1IOR0	00h
02EFh	Timer S I/O Control Register 1	G1IOR1	00h
02F0h	Interrupt Request Register	G1IR	XXh
02F1h	Interrupt Enable Register 0	G1IE0	00h
02F2h	Interrupt Enable Register 1	G1IE1	00h
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh	NMI Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh

X: Undefined

## Note:

1. The blank areas are reserved. No access is allowed.



**Table 4.13 SFR Information (13) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0300h			
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h			
0311h			
0312h			
0313h			
0314h			
0315h			
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh			
031Ch			
031Dh			
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.14 SFR Information (14) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.15 SFR Information (15) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	00h
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	0XX0 0XX0b
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch	Input Threshold Select Register 0	VLT0	00h
036Dh	Input Threshold Select Register 1	VLT1	0000 XXXXb
036Eh	Input Threshold Select Register 2	VLT2	XX00 0000b
036Fh			
0370h	Pin Assignment Control Register	PACR	0XXX X000b
0371h			
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h <sup>(2)</sup>
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			

X: Undefined

## Notes:

1. The blank areas are reserved. No access is allowed.
2. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

**Table 4.16 SFR Information (16) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 XXXXb
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:

- The blank areas are reserved. No access is allowed.

**Table 4.17 SFR Information (17) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h			
03D9h			
03DAh			
03DBh			
03DCh			
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h			
03E9h			
03EAh			
03EBh			
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:

- The blank areas are reserved. No access is allowed.

**Table 4.18 SFR Information (18) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	000X 0000b
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

## Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.19 SFR Information (19) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D500h	CAN0 Mailbox 0: Message Identifier	COMBO	XXh
D501h			XXh
D502h			XXh
D503h			XXh
D504h			
D505h	CAN0 Mailbox 0: Data Length		XXh
D506h	CAN0 Mailbox 0: Data Field		XXh
D507h			XXh
D508h			XXh
D509h			XXh
D50Ah			XXh
D50Bh			XXh
D50Ch			XXh
D50Dh			XXh
D50Eh	CAN0 Mailbox 0: Time Stamp		XXh
D50Fh			XXh
D510h	CAN0 Mailbox 1: Message Identifier	COMB1	XXh
D511h			XXh
D512h			XXh
D513h			XXh
D514h			
D515h	CAN0 Mailbox 1: Data Length		XXh
D516h	CAN0 Mailbox 1: Data Field		XXh
D517h			XXh
D518h			XXh
D519h			XXh
D51Ah			XXh
D51Bh			XXh
D51Ch			XXh
D51Dh			XXh
D51Eh	CAN0 Mailbox 1: Time Stamp		XXh
D51Fh			XXh
D520h	CAN0 Mailbox 2: Message Identifier	COMB2	XXh
D521h			XXh
D522h			XXh
D523h			XXh
D524h			
D525h	CAN0 Mailbox 2: Data Length		XXh
D526h	CAN0 Mailbox 2: Data Field		XXh
D527h			XXh
D528h			XXh
D529h			XXh
D52Ah			XXh
D52Bh			XXh
D52Ch			XXh
D52Dh			XXh
D52Eh	CAN0 Mailbox 2: Time Stamp		XXh
D52Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.20 SFR Information (20) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value	
D530h	CAN0 Mailbox 3: Message Identifier	C0MB3	XXh	
D531h			XXh	
D532h			XXh	
D533h			XXh	
D534h				
D535h	CAN0 Mailbox 3: Data Length		XXh	
D536h	CAN0 Mailbox 3: Data Field		XXh	
D537h			XXh	
D538h			XXh	
D539h			XXh	
D53Ah			XXh	
D53Bh			XXh	
D53Ch			XXh	
D53Dh			XXh	
D53Eh	CAN0 Mailbox 3: Time Stamp		XXh	
D53Fh			XXh	
D540h	CAN0 Mailbox 4: Message Identifier		C0MB4	XXh
D541h				XXh
D542h				XXh
D543h				XXh
D544h				
D545h	CAN0 Mailbox 4: Data Length	XXh		
D546h	CAN0 Mailbox 4: Data Field	XXh		
D547h		XXh		
D548h		XXh		
D549h		XXh		
D54Ah		XXh		
D54Bh		XXh		
D54Ch		XXh		
D54Dh		XXh		
D54Eh	CAN0 Mailbox 4: Time Stamp	XXh		
D54Fh		XXh		
D550h	CAN0 Mailbox 5: Message Identifier	C0MB5		XXh
D551h				XXh
D552h				XXh
D553h				
D554h				
D555h	CAN0 Mailbox 5: Data Length		XXh	
D556h	CAN0 Mailbox 5: Data Field		XXh	
D557h			XXh	
D558h			XXh	
D559h			XXh	
D55Ah			XXh	
D55Bh			XXh	
D55Ch			XXh	
D55Dh			XXh	
D55Eh	CAN0 Mailbox 5: Time Stamp		XXh	
D55Fh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.



**Table 4.21 SFR Information (21) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D560h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXh
D561h			XXh
D562h			XXh
D563h			XXh
D564h			
D565h	CAN0 Mailbox 6: Data Length		XXh
D566h	CAN0 Mailbox 6: Data Field		XXh
D567h			XXh
D568h			XXh
D569h			XXh
D56Ah			XXh
D56Bh			XXh
D56Ch			XXh
D56Dh			XXh
D56Eh	CAN0 Mailbox 6: Time Stamp		XXh
D56Fh			XXh
D570h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXh
D571h			XXh
D572h			XXh
D573h			XXh
D574h			
D575h	CAN0 Mailbox 7: Data Length		XXh
D576h	CAN0 Mailbox 7: Data Field		XXh
D577h			XXh
D578h			XXh
D579h			XXh
D57Ah			XXh
D57Bh			XXh
D57Ch			XXh
D57Dh			XXh
D57Eh	CAN0 Mailbox 7: Time Stamp		XXh
D57Fh			XXh
D580h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXh
D581h			XXh
D582h			XXh
D583h			XXh
D584h			
D585h	CAN0 Mailbox 8: Data Length		XXh
D586h	CAN0 Mailbox 8: Data Field		XXh
D587h			XXh
D588h			XXh
D589h			XXh
D58Ah			XXh
D58Bh			XXh
D58Ch			XXh
D58Dh			XXh
D58Eh	CAN0 Mailbox 8: Time Stamp		XXh
D58Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.22 SFR Information (22) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D590h	CAN0 Mailbox 9: Message Identifier	COMB9	XXh
D591h			XXh
D592h			XXh
D593h			XXh
D594h			
D595h	CAN0 Mailbox 9: Data Length		XXh
D596h	CAN0 Mailbox 9: Data Field		XXh
D597h			XXh
D598h			XXh
D599h			XXh
D59Ah			XXh
D59Bh			XXh
D59Ch			XXh
D59Dh			XXh
D59Eh	CAN0 Mailbox 9: Time Stamp		XXh
D59Fh			XXh
D5A0h	CAN0 Mailbox 10: Message Identifier	COMB10	XXh
D5A1h			XXh
D5A2h			XXh
D5A3h			XXh
D5A4h			
D5A5h	CAN0 Mailbox 10: Data Length		XXh
D5A6h	CAN0 Mailbox 10: Data Field		XXh
D5A7h			XXh
D5A8h			XXh
D5A9h			XXh
D5AAh			XXh
D5ABh			XXh
D5ACh			XXh
D5ADh			XXh
D5AEh	CAN0 Mailbox 10: Time Stamp		XXh
D5AFh			XXh
D5B0h	CAN0 Mailbox 11: Message Identifier	COMB11	XXh
D5B1h			XXh
D5B2h			XXh
D5B3h			XXh
D5B4h			
D5B5h	CAN0 Mailbox 11: Data Length		XXh
D5B6h	CAN0 Mailbox 11: Data Field		XXh
D5B7h			XXh
D5B8h			XXh
D5B9h			XXh
D5BAh			XXh
D5BBh			XXh
D5BCh			XXh
D5BDh			XXh
D5BEh	CAN0 Mailbox 11: Time Stamp		XXh
D5BFh			XXh

X: Undefined

Note:

- The blank areas are reserved. No access is allowed.

**Table 4.23 SFR Information (23) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D5C0h	CAN0 Mailbox 12: Message Identifier	C0MB12	XXh
D5C1h			XXh
D5C2h			XXh
D5C3h			XXh
D5C4h			
D5C5h	CAN0 Mailbox 12: Data Length		XXh
D5C6h	CAN0 Mailbox 12: Data Field		XXh
D5C7h			XXh
D5C8h			XXh
D5C9h			XXh
D5CAh			XXh
D5CBh			XXh
D5CCh			XXh
D5CDh			XXh
D5CEh	CAN0 Mailbox 12: Time Stamp		XXh
D5CFh			XXh
D5D0h	CAN0 Mailbox 13: Message Identifier		C0MB13
D5D1h		XXh	
D5D2h		XXh	
D5D3h		XXh	
D5D4h			
D5D5h	CAN0 Mailbox 13: Data Length	XXh	
D5D6h	CAN0 Mailbox 13: Data Field	XXh	
D5D7h		XXh	
D5D8h		XXh	
D5D9h		XXh	
D5DAh		XXh	
D5DBh		XXh	
D5DCh		XXh	
D5DDh		XXh	
D5DEh	CAN0 Mailbox 13: Time Stamp	XXh	
D5DFh		XXh	
D5E0h	CAN0 Mailbox 14: Message Identifier	C0MB14	
D5E1h			XXh
D5E2h			XXh
D5E3h			XXh
D5E4h			
D5E5h	CAN0 Mailbox 14: Data Length		XXh
D5E6h	CAN0 Mailbox 14: Data Field		XXh
D5E7h			XXh
D5E8h			XXh
D5E9h			XXh
D5EAh			XXh
D5EBh			XXh
D5ECh			XXh
D5EDh			XXh
D5EEh	CAN0 Mailbox 14: Time Stamp		XXh
D5EFh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.24 SFR Information (24) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D5F0h	CAN0 Mailbox 15: Message Identifier	COMB15	XXh
D5F1h			XXh
D5F2h			XXh
D5F3h			XXh
D5F4h			
D5F5h	CAN0 Mailbox 15: Data Length		XXh
D5F6h	CAN0 Mailbox 15: Data Field		XXh
D5F7h			XXh
D5F8h			XXh
D5F9h			XXh
D5FAh			XXh
D5FBh			XXh
D5FCh			XXh
D5FDh			XXh
D5FEh	CAN0 Mailbox 15: Time Stamp		XXh
D5FFh			XXh
D600h	CAN0 Mailbox 16: Message Identifier		COMB16
D601h		XXh	
D602h		XXh	
D603h		XXh	
D604h			
D605h	CAN0 Mailbox 16: Data Length	XXh	
D606h	CAN0 Mailbox 16: Data Field	XXh	
D607h		XXh	
D608h		XXh	
D609h		XXh	
D60Ah		XXh	
D60Bh		XXh	
D60Ch		XXh	
D60Dh		XXh	
D60Eh	CAN0 Mailbox 16: Time Stamp	XXh	
D60Fh		XXh	
D610h	CAN0 Mailbox 17: Message Identifier	COMB17	
D611h			XXh
D612h			XXh
D613h			XXh
D614h			
D615h	CAN0 Mailbox 17: Data Length		XXh
D616h	CAN0 Mailbox 17: Data Field		XXh
D617h			XXh
D618h			XXh
D619h			XXh
D61Ah			XXh
D61Bh			XXh
D61Ch			XXh
D61Dh			XXh
D61Eh	CAN0 Mailbox 17: Time Stamp		XXh
D61Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.25 SFR Information (25) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value	
D620h	CAN0 Mailbox 18: Message Identifier	COMB18	XXh	
D621h			XXh	
D622h			XXh	
D623h			XXh	
D624h				
D625h	CAN0 Mailbox 18: Data Length		XXh	
D626h	CAN0 Mailbox 18: Data Field		XXh	
D627h			XXh	
D628h			XXh	
D629h			XXh	
D62Ah			XXh	
D62Bh			XXh	
D62Ch			XXh	
D62Dh			XXh	
D62Eh	CAN0 Mailbox 18: Time Stamp		XXh	
D62Fh			XXh	
D630h	CAN0 Mailbox 19: Message Identifier		COMB19	XXh
D631h				XXh
D632h		XXh		
D633h		XXh		
D634h				
D635h	CAN0 Mailbox 19: Data Length	XXh		
D636h	CAN0 Mailbox 19: Data Field	XXh		
D637h		XXh		
D638h		XXh		
D639h		XXh		
D63Ah		XXh		
D63Bh		XXh		
D63Ch		XXh		
D63Dh		XXh		
D63Eh	CAN0 Mailbox 19: Time Stamp	XXh		
D63Fh		XXh		
D640h	CAN0 Mailbox 20: Message Identifier	COMB20		XXh
D641h				XXh
D642h			XXh	
D643h			XXh	
D644h				
D645h	CAN0 Mailbox 20: Data Length		XXh	
D646h	CAN0 Mailbox 20: Data Field		XXh	
D647h			XXh	
D648h			XXh	
D649h			XXh	
D64Ah			XXh	
D64Bh			XXh	
D64Ch			XXh	
D64Dh			XXh	
D64Eh	CAN0 Mailbox 20: Time Stamp		XXh	
D64Fh			XXh	

X: Undefined

## Note:

- The blank areas are reserved. No access is allowed.

**Table 4.26 SFR Information (26) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D650h	CAN0 Mailbox 21: Message Identifier	COMB21	XXh
D651h			XXh
D652h			XXh
D653h			XXh
D654h			
D655h	CAN0 Mailbox 21: Data Length		XXh
D656h	CAN0 Mailbox 21: Data Field		XXh
D657h			XXh
D658h			XXh
D659h			XXh
D65Ah			XXh
D65Bh			XXh
D65Ch			XXh
D65Dh			XXh
D65Eh	CAN0 Mailbox 21: Time Stamp		XXh
D65Fh			XXh
D660h	CAN0 Mailbox 22: Message Identifier	COMB22	XXh
D661h			XXh
D662h			XXh
D663h			XXh
D664h			
D665h	CAN0 Mailbox 22: Data Length		XXh
D666h	CAN0 Mailbox 22: Data Field		XXh
D667h			XXh
D668h			XXh
D669h			XXh
D66Ah			XXh
D66Bh			XXh
D66Ch			XXh
D66Dh			XXh
D66Eh	CAN0 Mailbox 22: Time Stamp		XXh
D66Fh			XXh
D670h	CAN0 Mailbox 23: Message Identifier	COMB23	XXh
D671h			XXh
D672h			XXh
D673h			XXh
D674h			
D675h	CAN0 Mailbox 23: Data Length		XXh
D676h	CAN0 Mailbox 23: Data Field		XXh
D677h			XXh
D678h			XXh
D679h			XXh
D67Ah			XXh
D67Bh			XXh
D67Ch			XXh
D67Dh			XXh
D67Eh	CAN0 Mailbox 23: Time Stamp		XXh
D67Fh			XXh

X: Undefined

## Note:

- The blank areas are reserved. No access is allowed.

**Table 4.27 SFR Information (27) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value	
D680h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXh	
D681h			XXh	
D682h			XXh	
D683h			XXh	
D684h				
D685h	CAN0 Mailbox 24: Data Length		XXh	
D686h	CAN0 Mailbox 24: Data Field		XXh	
D687h			XXh	
D688h			XXh	
D689h			XXh	
D68Ah			XXh	
D68Bh			XXh	
D68Ch			XXh	
D68Dh			XXh	
D68Eh	CAN0 Mailbox 24: Time Stamp		XXh	
D68Fh			XXh	
D690h	CAN0 Mailbox 25: Message Identifier		C0MB25	XXh
D691h				XXh
D692h				XXh
D693h				XXh
D694h				
D695h	CAN0 Mailbox 25: Data Length			XXh
D696h	CAN0 Mailbox 25: Data Field			XXh
D697h				XXh
D698h				XXh
D699h				XXh
D69Ah				XXh
D69Bh		XXh		
D69Ch		XXh		
D69Dh		XXh		
D69Eh	CAN0 Mailbox 25: Time Stamp	XXh		
D69Fh		XXh		
D6A0h	CAN0 Mailbox 26: Message Identifier	C0MB26		XXh
D6A1h				XXh
D6A2h				XXh
D6A3h				XXh
D6A4h				
D6A5h	CAN0 Mailbox 26: Data Length			XXh
D6A6h	CAN0 Mailbox 26: Data Field			XXh
D6A7h				XXh
D6A8h				XXh
D6A9h				XXh
D6AAh				XXh
D6ABh			XXh	
D6ACh			XXh	
D6ADh			XXh	
D6AEh	CAN0 Mailbox 26: Time Stamp		XXh	
D6AFh			XXh	

X: Undefined

## Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.28 SFR Information (28) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D6B0h	CAN0 Mailbox 27: Message Identifier	C0MB27	XXh
D6B1h			XXh
D6B2h			XXh
D6B3h			XXh
D6B4h			
D6B5h	CAN0 Mailbox 27: Data Length		XXh
D6B6h	CAN0 Mailbox 27: Data Field		XXh
D6B7h			XXh
D6B8h			XXh
D6B9h			XXh
D6BAh			XXh
D6BBh			XXh
D6BCh			XXh
D6BDh			XXh
D6BEh	CAN0 Mailbox 27: Time Stamp		XXh
D6BFh			XXh
D6C0h	CAN0 Mailbox 28: Message Identifier		C0MB28
D6C1h		XXh	
D6C2h		XXh	
D6C3h		XXh	
D6C4h			
D6C5h	CAN0 Mailbox 28: Data Length	XXh	
D6C6h	CAN0 Mailbox 28: Data Field	XXh	
D6C7h		XXh	
D6C8h		XXh	
D6C9h		XXh	
D6CAh		XXh	
D6CBh		XXh	
D6CCh		XXh	
D6CDh		XXh	
D6CEh	CAN0 Mailbox 28: Time Stamp	XXh	
D6CFh		XXh	
D6D0h	CAN0 Mailbox 29: Message Identifier	C0MB29	
D6D1h			XXh
D6D2h			XXh
D6D3h			XXh
D6D4h			
D6D5h	CAN0 Mailbox 29: Data Length		XXh
D6D6h	CAN0 Mailbox 29: Data Field		XXh
D6D7h			XXh
D6D8h			XXh
D6D9h			XXh
D6DAh			XXh
D6DBh			XXh
D6DCh			XXh
D6DDh			XXh
D6DEh	CAN0 Mailbox 29: Time Stamp		XXh
D6DFh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.



**Table 4.29 SFR Information (29) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D6E0h	CAN0 Mailbox 30: Message Identifier	COMB30	XXh
D6E1h			XXh
D6E2h			XXh
D6E3h			XXh
D6E4h			
D6E5h	CAN0 Mailbox 30: Data Length		XXh
D6E6h	CAN0 Mailbox 30: Data Field		XXh
D6E7h			XXh
D6E8h			XXh
D6E9h			XXh
D6EAh			XXh
D6EBh			XXh
D6ECh			XXh
D6EDh			XXh
D6EEh	CAN0 Mailbox 30: Time Stamp		XXh
D6EFh			XXh
D6F0h	CAN0 Mailbox 31: Message Identifier		COMB31
D6F1h		XXh	
D6F2h		XXh	
D6F3h		XXh	
D6F4h			
D6F5h	CAN0 Mailbox 31: Data Length	XXh	
D6F6h	CAN0 Mailbox 31: Data Field	XXh	
D6F7h		XXh	
D6F8h		XXh	
D6F9h		XXh	
D6FAh		XXh	
D6FBh		XXh	
D6FCh		XXh	
D6FDh		XXh	
D6FEh	CAN0 Mailbox 31: Time Stamp	XXh	
D6FFh		XXh	
D700h	CAN0 Mask Register 0	COMKR0	
D701h			XXh
D702h			XXh
D703h			XXh
D704h	CAN0 Mask Register 1	COMKR1	XXh
D705h			XXh
D706h			XXh
D707h			XXh
D708h	CAN0 Mask Register 2	COMKR2	XXh
D709h			XXh
D70Ah			XXh
D70Bh			XXh
D70Ch	CAN0 Mask Register 3	COMKR3	XXh
D70Dh			XXh
D70Eh			XXh
D70Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

**Table 4.30 SFR Information (30) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D710h	CAN0 Mask Register 4	C0MKR4	XXh
D711h			XXh
D712h			XXh
D713h			XXh
D714h	CAN0 Mask Register 5	C0MKR5	XXh
D715h			XXh
D716h			XXh
D717h			XXh
D718h	CAN0 Mask Register 6	C0MKR6	XXh
D719h			XXh
D71Ah			XXh
D71Bh			XXh
D71Ch	CAN0 Mask Register 7	C0MKR7	XXh
D71Dh			XXh
D71Eh			XXh
D71Fh			XXh
D720h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXh
D721h			XXh
D722h			XXh
D723h			XXh
D724h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXh
D725h			XXh
D726h			XXh
D727h			XXh
D728h	CAN0 Mask Invalid Register	C0MKIVLR	XXh
D729h			XXh
D72Ah			XXh
D72Bh			XXh
D72Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXh
D72Dh			XXh
D72Eh			XXh
D72Fh			XXh
D730h to D79Fh			
D7A0h	CAN0 Message Control Register 0	C0MCTL0	00h
D7A1h	CAN0 Message Control Register 1	C0MCTL1	00h
D7A2h	CAN0 Message Control Register 2	C0MCTL2	00h
D7A3h	CAN0 Message Control Register 3	C0MCTL3	00h
D7A4h	CAN0 Message Control Register 4	C0MCTL4	00h
D7A5h	CAN0 Message Control Register 5	C0MCTL5	00h
D7A6h	CAN0 Message Control Register 6	C0MCTL6	00h
D7A7h	CAN0 Message Control Register 7	C0MCTL7	00h
D7A8h	CAN0 Message Control Register 8	C0MCTL8	00h
D7A9h	CAN0 Message Control Register 9	C0MCTL9	00h
D7AAh	CAN0 Message Control Register 10	C0MCTL10	00h
D7ABh	CAN0 Message Control Register 11	C0MCTL11	00h
D7ACh	CAN0 Message Control Register 12	C0MCTL12	00h
D7ADh	CAN0 Message Control Register 13	C0MCTL13	00h
D7AEh	CAN0 Message Control Register 14	C0MCTL14	00h
D7AFh	CAN0 Message Control Register 15	C0MCTL15	00h

X: Undefined

## Note:

- The blank areas are reserved. No access is allowed.

**Table 4.31 SFR Information (31) <sup>(1)</sup>**

Address	Register	Symbol	Reset Value
D7B0h	CAN0 Message Control Register 16	C0MCTL16	00h
D7B1h	CAN0 Message Control Register 17	C0MCTL17	00h
D7B2h	CAN0 Message Control Register 18	C0MCTL18	00h
D7B3h	CAN0 Message Control Register 19	C0MCTL19	00h
D7B4h	CAN0 Message Control Register 20	C0MCTL20	00h
D7B5h	CAN0 Message Control Register 21	C0MCTL21	00h
D7B6h	CAN0 Message Control Register 22	C0MCTL22	00h
D7B7h	CAN0 Message Control Register 23	C0MCTL23	00h
D7B8h	CAN0 Message Control Register 24	C0MCTL24	00h
D7B9h	CAN0 Message Control Register 25	C0MCTL25	00h
D7BAh	CAN0 Message Control Register 26	C0MCTL26	00h
D7BBh	CAN0 Message Control Register 27	C0MCTL27	00h
D7BCh	CAN0 Message Control Register 28	C0MCTL28	00h
D7BDh	CAN0 Message Control Register 29	C0MCTL29	00h
D7BEh	CAN0 Message Control Register 30	C0MCTL30	00h
D7BFh	CAN0 Message Control Register 31	C0MCTL31	00h
D7C0h	CAN0 Control Register	C0CTLR	0000 0101b
D7C1h			00h
D7C2h	CAN0 Status Register	C0STR	0000 0101b
D7C3h			00h
D7C4h	CAN0 Bit Configuration Register	C0BCR	00h
D7C5h			00h
D7C6h			00h
D7C7h	CAN0 Clock Select Register	C0CLKR	00h
D7C8h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
D7CAh	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR	XXh
D7CCh	CAN0 Error Interrupt Enable Register	C0EIER	00h
D7CDh	CAN0 Error Interrupt Source Judge Register	C0EIFR	00h
D7CEh	CAN0 Receive Error Count Register	C0RECR	00h
D7CFh	CAN0 Transmit Error Count Register	C0TECR	00h
D7D0h	CAN0 Error Code Store Register	C0ECSR	00h
D7D1h	CAN0 Channel Search Support Register	C0CSSR	XXh
D7D2h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
D7D3h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
D7D4h	CAN0 Time Stamp Register	C0TSR	00h
D7D5h			00h
D7D6h	CAN0 Acceptance Filter Support Register	C0AFSR	XXh
D7D7h			XXh
D7D8h	CAN0 Test Control Register	C0TCR	00h
D7D9h			
D7DAh			
D7DBh			
D7DCh			
D7DDh			
D7DEh			
D7DFh			

X: Undefined

## Note:

- The blank areas are reserved. No access is allowed.

## 4.2 Notes on SFRs

### 4.2.1 Register Settings

Table 4.32 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM. Read-modify-write instructions can be used when writing to the no register bits.

**Table 4.32 Registers with Write-Only Bits**

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0299h	UART4 Bit Rate Register	U4BRG
029Bh to 029Ah	UART4 Transmit Buffer Register	U4TB
02A9h	UART3 Bit Rate Register	U3BRG
02ABh to 02AAh	UART3 Transmit Buffer Register	U3TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR

**Table 4.33 Read-Modify-Write Instructions**

Function	Mnemonic
Transfer	<i>MOVDir</i>
Bit processing	BCLR, <i>BMCnd</i> , BNOT, BSET, BTSTC, and BTSTS
Shifting	ROL, ROR, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

## 5. Protection

### 5.1 Introduction

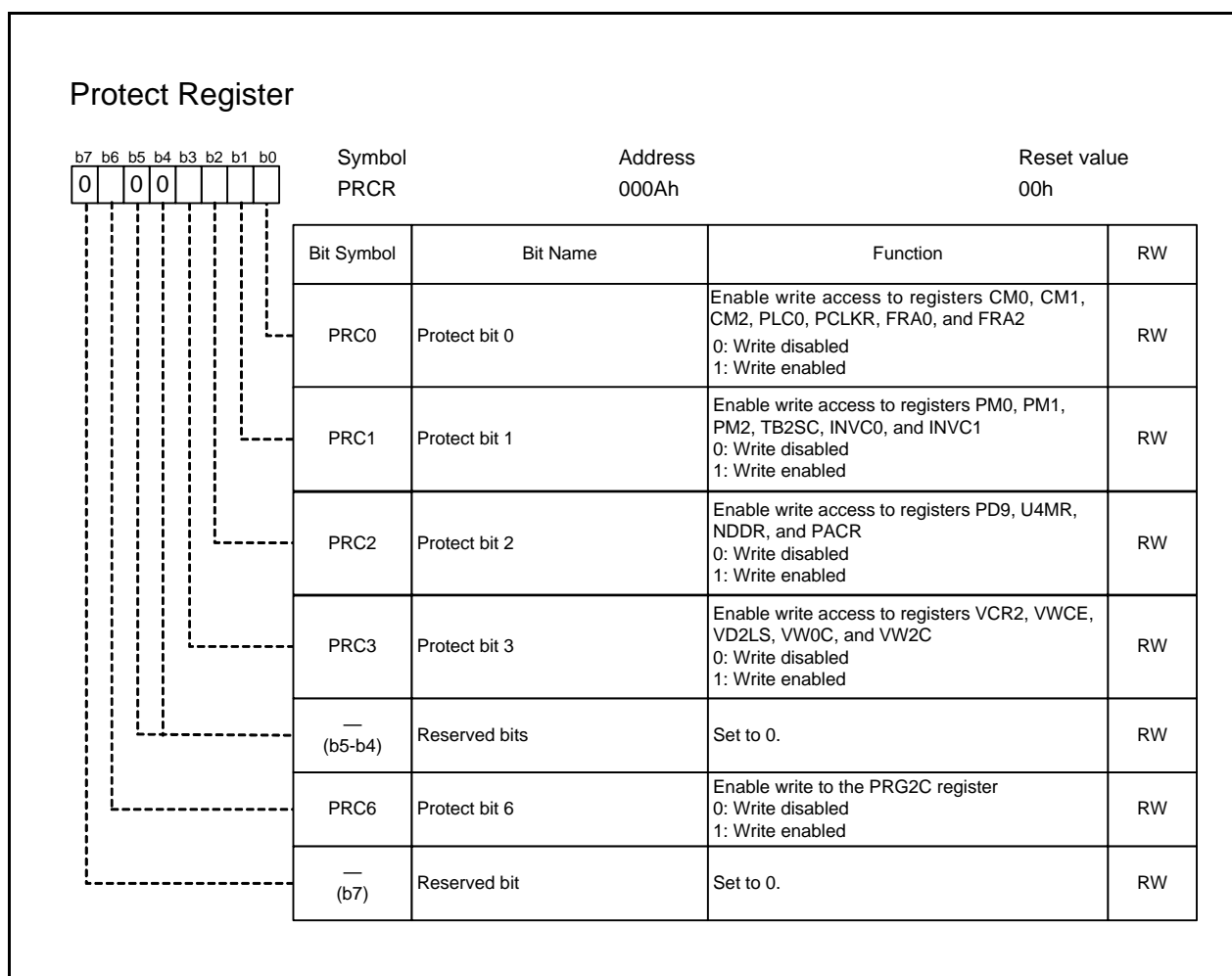
In the event that a program runs out of control, this function protects the important registers so that they will not be rewritten easily.

### 5.2 Register

**Table 5.1 Registers**

Address	Register	Symbol	Reset Value
000Ah	Protect Register	PRCR	00h

#### 5.2.1 Protect Register (PRCR)



**PRC6, PRC3, PRC1, PRC0 (Protect bits 6, 3, 1, 0) (b6, b3, b1, b0)**

When setting bits PRC6, PRC3, PRC1, and PRC0 to 1 (write enabled), these bits remain 1 (write enabled). To change registers protected by these bits, follow these steps:

- (1) Set the PRC<sub>i</sub> bit to 1. (i = 0, 1, 3, 6)
- (2) Write to the register protected by the PRC<sub>i</sub> bit.
- (3) Set the PRC<sub>i</sub> bit to 0 (write protected).

**PRC2 (Protect bit 2) (b2)**

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0. Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. The steps are shown below. Make sure there are no interrupts or DMA transfers between steps (1) and (2).

- (1) Set the PRC2 bit to 1.
- (2) Write to the register protected by the PRC2 bit.

### 5.3 Notes on Protection

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0 (write disabled). Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure there are no interrupts or DMA transfers between the instruction that sets the PRC2 bit to 1 and the next instruction.



## 6. Resets

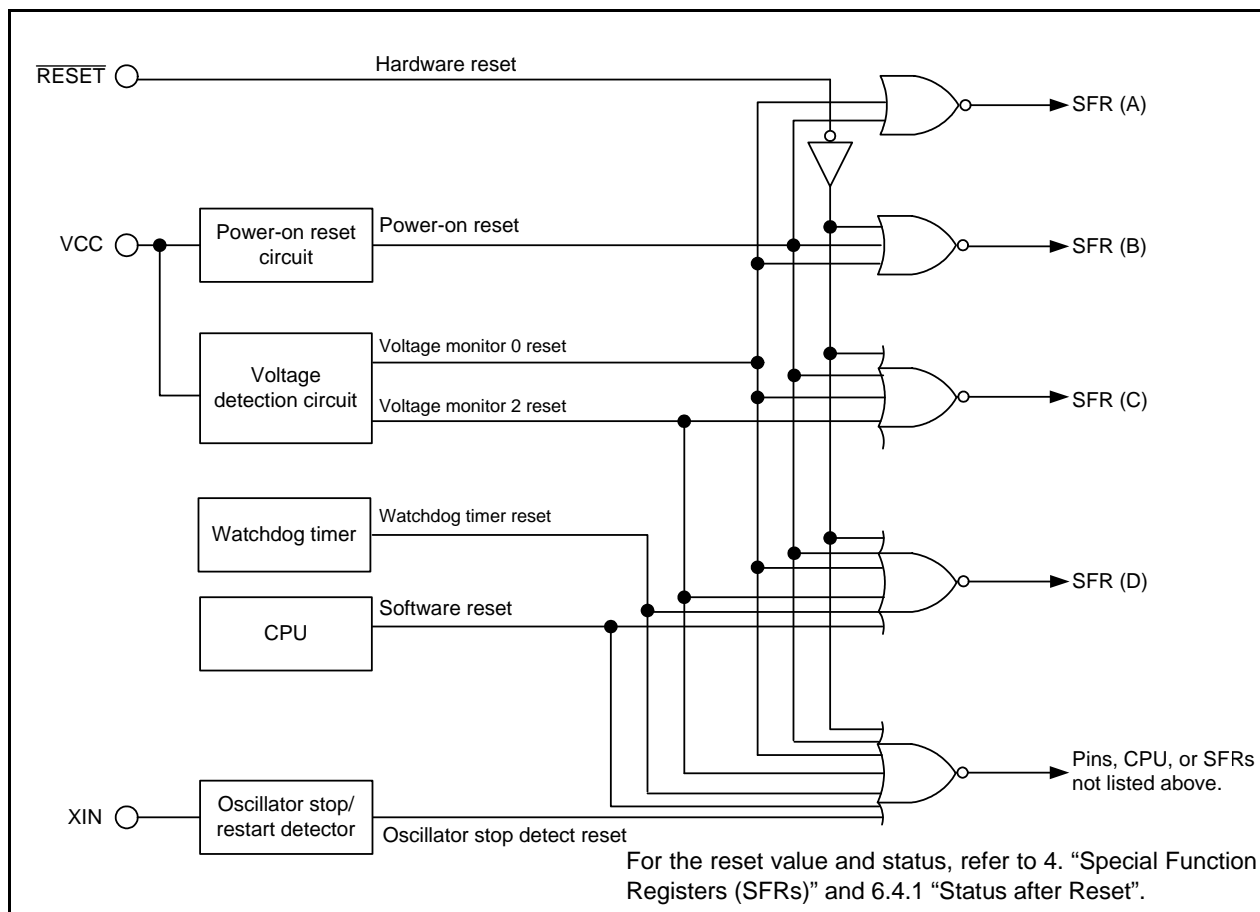
### 6.1 Introduction

The following resets can be used to reset the MCU: hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, and software reset.

Table 6.1 lists the Types of Resets and Figure 6.1 shows the Reset Circuit Block Diagram. Symbols (A) to (D) in the table and figure is explained in Table 6.2. Table 6.3 lists the I/O Pins.

**Table 6.1 Types of Resets**

Reset Name	Trigger	Registers and Bits Not to Reset
Hardware reset	A low-level signal is applied to the $\overline{\text{RESET}}$ pin.	(A)
Power-on reset	A rise in voltage on VCC	N/A
Voltage monitor 0 reset	A drop in voltage on VCC (reference voltage: Vdet0)	N/A
Voltage monitor 2 reset	A drop in voltage on VCC (reference voltage: Vdet2)	(B)
Oscillator stop detect reset	A stop in the main clock oscillator is detected.	(B) (C) (D)
Watchdog timer reset	The watchdog timer underflows.	(B) (C)
Software reset	Setting the PM03 bit in the PM0 register to 1.	(B) (C)



**Figure 6.1 Reset Circuit Block Diagram**

**Table 6.2 Classification of SFRs Which are Reset**

SFR	Register and Bit
SFR (A)	OSDR bit in the RSTFR register
SFR (B)	Registers VCR1, VCR2, and VW0C Bits VW2C2 and VW2C3 in the VW2C register
SFR (C)	VD2LS register
SFR (D)	Bits CM20, CM21, and CM27 in the CM2 register

**Table 6.3 I/O Pins**

Pin	I/O	Function
RESET	Input	Hardware reset input
VCC	Input	Power input. The power-on reset, voltage monitor 0 reset, and voltage monitor 2 reset are generated by monitoring VCC.
XIN	Input	Main clock input. The oscillator stop detect reset is generated by monitoring the main clock.

## 6.2 Registers

Refer to 7. “Voltage Detector” for registers used with the voltage monitor 0 reset, and voltage monitor 2 reset. Refer to 13. “Watchdog Timer” for registers used with the watchdog timer reset. Refer to 8.7 “Oscillator Stop/Restart Detect Function” for registers used with the oscillator stop detect reset.

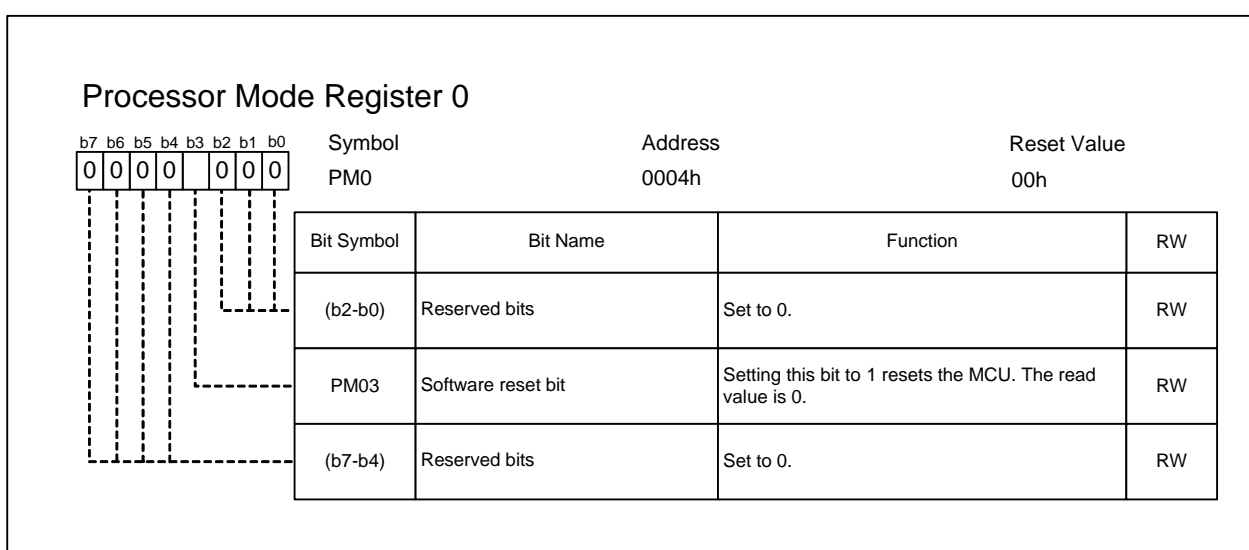
**Table 6.4 Registers**

Address	Register	Symbol	Reset Value
0004h	Processor Mode Register 0	PM0	00h
0018h	Reset Source Determine Register	RSTFR	– (1)

Note:

1. Refer to 6.2.2 “Reset Source Determine Register (RSTFR)”

### 6.2.1 Processor Mode Register 0 (PM0)

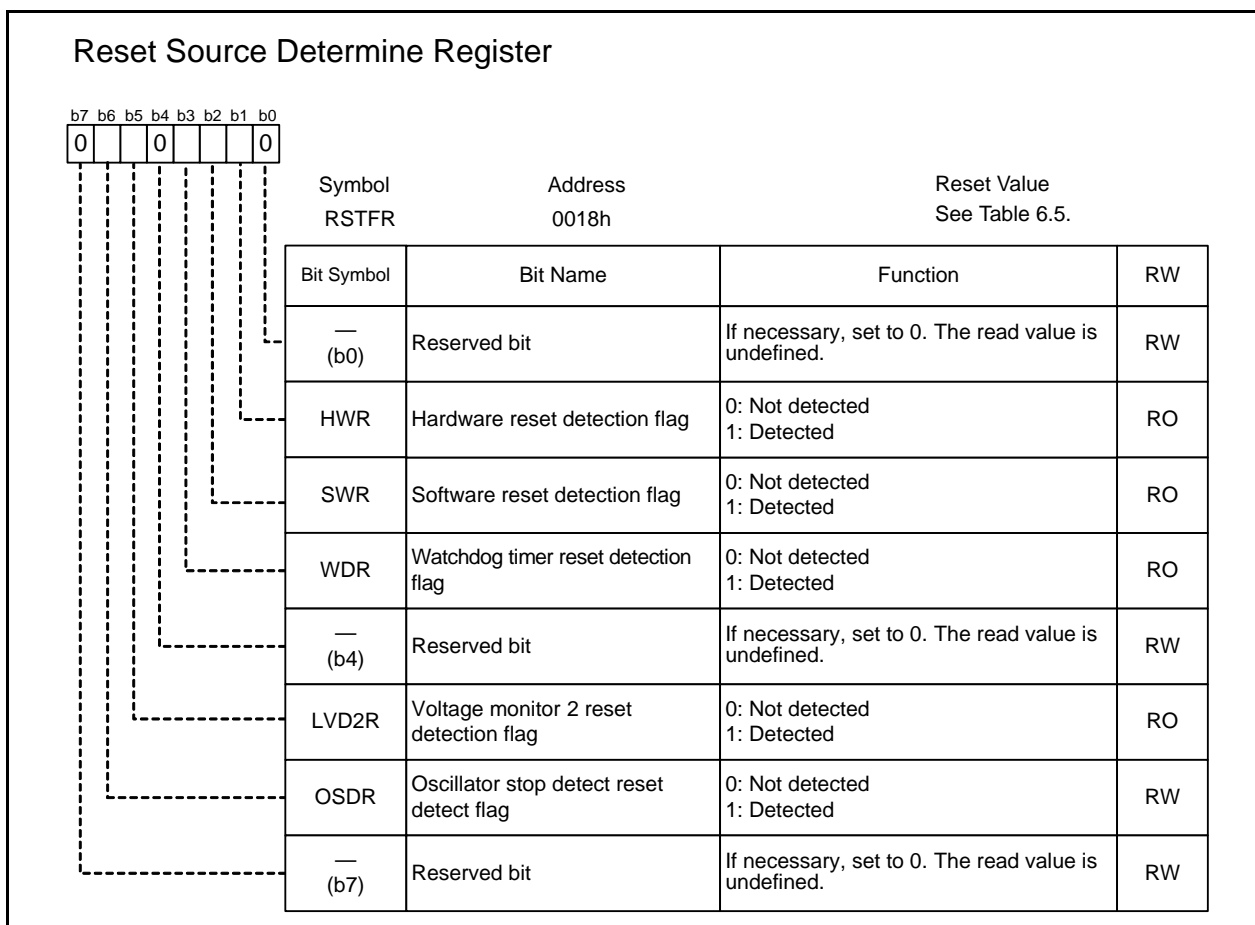


Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).

#### PM03 (Software reset bit) (b3)

A software reset is generated by setting the PM03 bit to 1.

## 6.2.2 Reset Source Determine Register (RSTFR)



**Table 6.5 RSTFR Register Reset Value**

Reset	Bits in the RSTFR Register				
	OSDR	LVD2R	WDR	SWR	HWR
Hardware reset	No change	0	0	0	1
Power-on reset	0	0	0	0	0
Voltage monitor 0 reset	0	0	0	0	0
Voltage monitor 2 reset	0	1	0	0	0
Oscillator stop detect reset	1	0	0	0	0
Watchdog timer reset	0	0	1	0	0
Software reset	0	0	0	1	0

### HWR (Hardware Reset Detect Flag) (b1)

When setting the LVDAS bit in the OFS1 address to 0 (voltage detector 0 reset is enabled after resetting the hardware), or the voltage monitor 0 reset is enabled by a program after reset, the HWR bit after the hardware reset is undefined.

### OSDR (Oscillator stop detect reset detect flag) (b6)

The OSDR bit also changes when following condition is met:

Conditions to become 0:

- Power-on
- Setting this bit to 0

This bit will not become 1 even when written to 1.

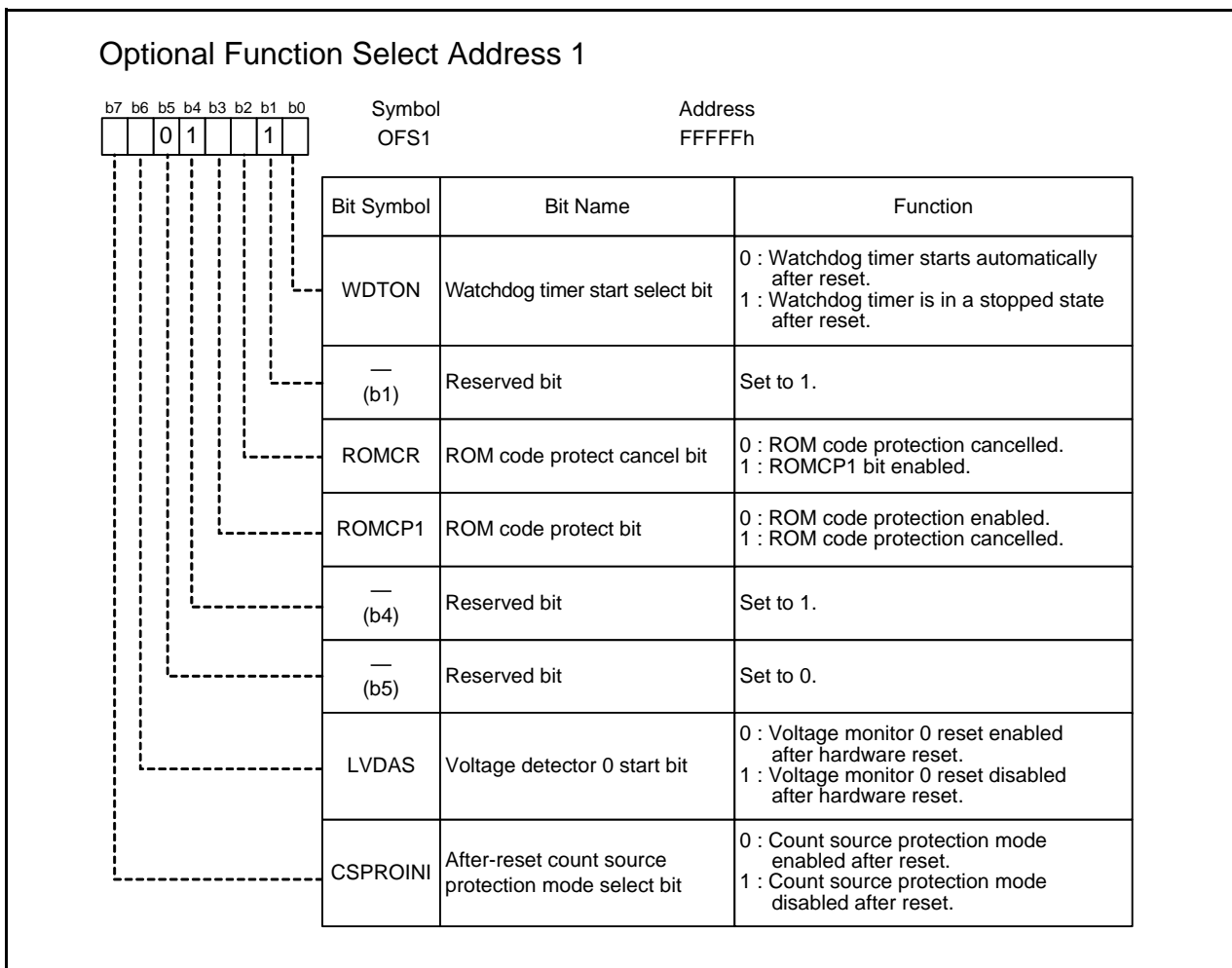
### 6.3 Optional Function Select Area

In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

In blank products, the OFS1 address value is FFh when shipped. After a value is written by the user, this address takes on the written value. In programmed products, the OFS1 address is the value set in the user program prior to shipping.

#### 6.3.1 Optional Function Select Address 1 (OFS1)



WDTON (Watchdog timer start select bit) (b0)

CSPROINI (After-reset count source protection mode select bit) (b7)

These bits select the state of the watchdog timer after reset.

Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).

Refer to 13. "Watchdog Timer" for details on the watchdog timer and count source protection mode.

ROMCR (ROM code protect cancel bit) (b2)

ROMCP1 (ROM code protect bit) (b3)

These bits prevent the flash memory from being read or changed in parallel I/O mode.

**Table 6.6 ROM Code Protection**

Bit Setting		ROM Code Protection
ROMCR bit	ROMCP1 bit	
0	0	Cancelled
0	1	
1	0	Enabled
1	1	Cancelled

Reserved bit (b5)

Set to 0.

LVDAS (Voltage detector 0 start bit) (b6)

Set this bit to 0 (voltage monitor 0 reset enabled after hardware reset) when using the power-on reset.

This bit is enabled in single-chip mode, while disabled in boot mode.

## 6.4 Operations

### 6.4.1 Status after Reset

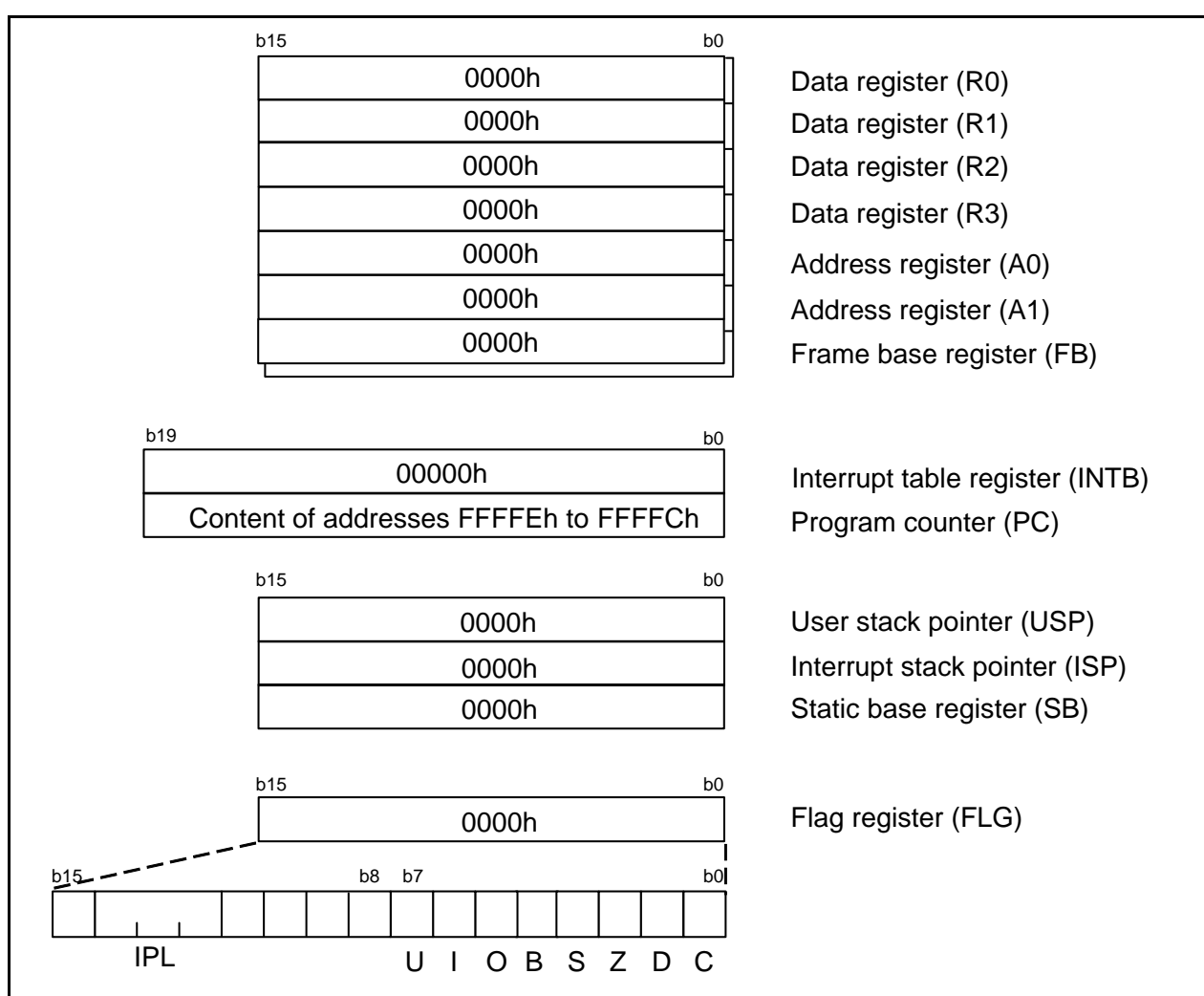
The status of SFRs after reset depends on the reset type. See the Reset Value column in 4. “Special Function Registers (SFRs)”. Table 6.7 lists Pin Status When  $\overline{\text{RESET}}$  Pin Level is Low, Figure 6.2 shows CPU Register Status after Reset, and Figure 6.3 shows Reset Sequence.

**Table 6.7 Pin Status When  $\overline{\text{RESET}}$  Pin Level is Low**

Pin Name	Status (1)
P0 to P3, P6 to P10	Input port (high-impedance)

Note:

- The pin status shown here is when the internal power supply voltage has stabilized after power-on. The pin status is undefined until  $t_d(P-R)$  has elapsed after power-on.



**Figure 6.2 CPU Register Status after Reset**

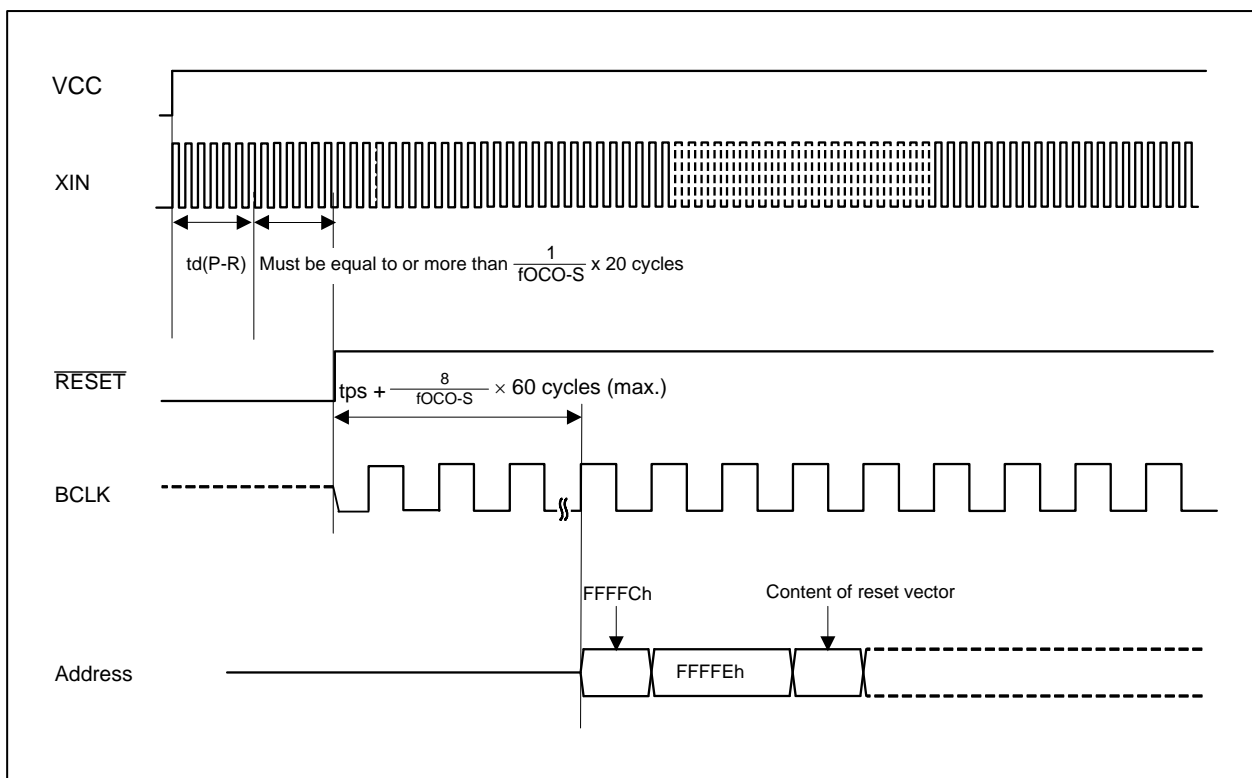


Figure 6.3 Reset Sequence



### 6.4.2 Hardware Reset

This reset is triggered by the  $\overline{\text{RESET}}$  pin. When the power supply voltage meets the recommended operating conditions, the MCU resets the pins, CPU, and SFRs when a low-level signal is applied to the  $\overline{\text{RESET}}$  pin.

When changing the signal applied to the  $\overline{\text{RESET}}$  pin from low to high, the MCU executes the program at the address indicated by the reset vector.  $f_{\text{OCO-S}}$  divided by 8 is automatically selected as the CPU clock after reset.

The HWR bit in the RSTFR register becomes 1 (hardware reset detected) after hardware reset. However, if the LVDAS bit in the OFS1 address is 0 (voltage detector 0 reset is enabled after resetting the hardware), the HWR bit is undefined. Refer to 4. "Special Function Registers (SFRs)" for the remaining SFR states after reset.

The internal RAM is not reset. When a low-level signal is applied to the  $\overline{\text{RESET}}$  pin while writing data to the internal RAM, the internal RAM becomes undefined.

The procedures for generating a hardware reset are as follows:

When the power supply is stable

- (1) Apply a low-level signal to the  $\overline{\text{RESET}}$  pin.
- (2) Wait for  $t_w(\text{RSTL})$ .
- (3) Apply a high-level signal to the  $\overline{\text{RESET}}$  pin.

When the power is turned on

- (1) Apply a low-level signal to the  $\overline{\text{RESET}}$  pin.
- (2) Raise the power supply voltage to the recommended operating level.
- (3) Wait for  $t_d(\text{P-R})$  until the internal voltage stabilizes.
- (4) Wait for  $\frac{1}{f_{\text{OCO-S}}} \times 20$  cycles.
- (5) Apply a high-level signal to the  $\overline{\text{RESET}}$  pin.

Figure 6.4 shows an Reset Circuit Example.

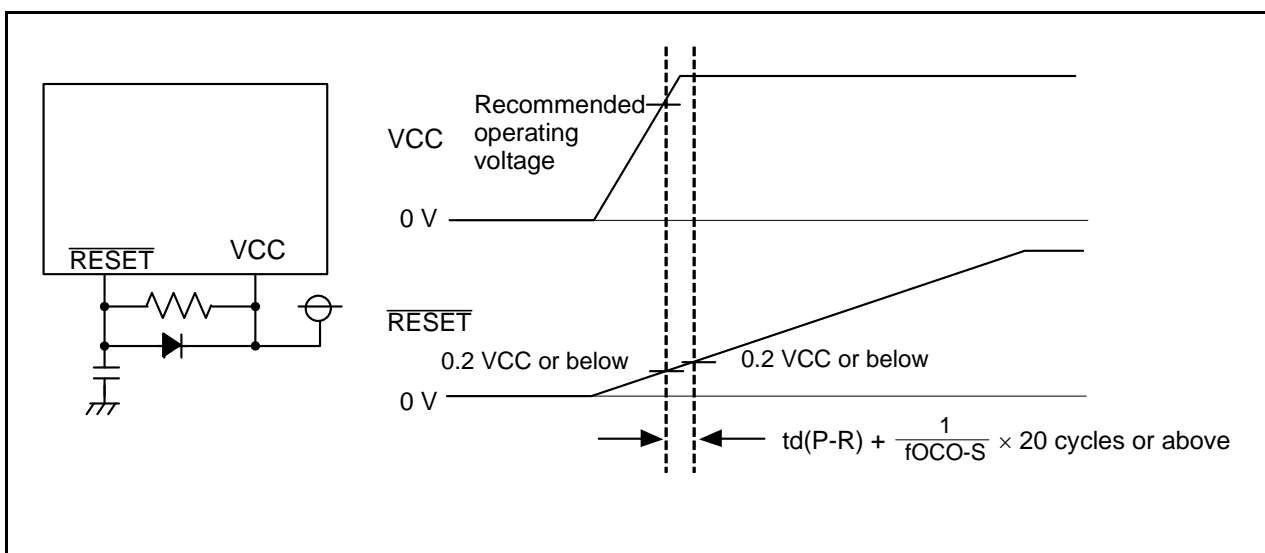


Figure 6.4 Reset Circuit Example

### 6.4.3 Power-On Reset Function

When the  $\overline{\text{RESET}}$  pin is connected to VCC via a pull-up resistor, and the VCC voltage level rises while the rise gradient is  $t_{rth}$  or more, the power-on reset function is enabled and the MCU resets the pins, CPU, and SFRs. Also, when a capacitor is connected to the  $\overline{\text{RESET}}$  pin, always keep the voltage to the  $\overline{\text{RESET}}$  pin in the range of  $V_{IH}$ .

When the input voltage to the VCC pin reaches  $V_{det0}$  or above, the fOCO-S count starts. When the fOCO-S count reaches 128, the internal reset signal becomes high and the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The internal RAM is not reset.

Use the voltage monitor 0 reset together with the power-on reset. Set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset) to use the power-on reset. In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1 and the VC25 bit in the VCR2 register is 1). Do not set these bits to 0 by a program.

Refer to 7. "Voltage Detector" for details of the voltage monitor 0 reset.

Figure 6.5 shows Example of Power-On Reset Operation.

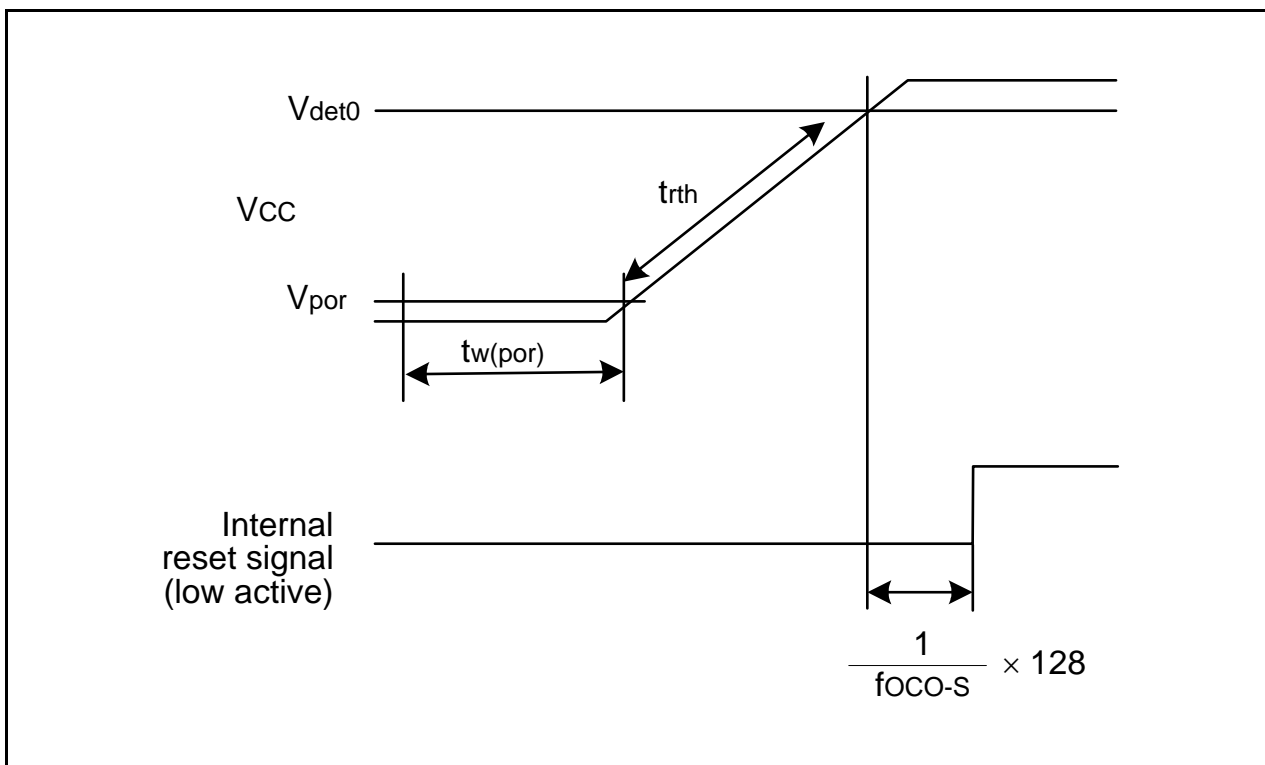


Figure 6.5 Example of Power-On Reset Operation

#### 6.4.4 Voltage Monitor 0 Reset

This reset is triggered by the MCU's on-chip voltage detector 0. The voltage detector 0 monitors the voltage applied to the VCC pin (Vdet0).

The MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC pin drops to Vdet0 or below.

Then, the fOCO-S count starts when the voltage applied to the VCC pin rises to Vdet0 or above. The internal reset signal becomes high after 128 cycles of fOCO-S, and then the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The internal RAM is not reset. When the voltage applied to the VCC pin drops to Vdet0 or below while writing data to the internal RAM, the internal RAM becomes undefined.

Refer to 7. "Voltage Detector" for details of the voltage monitor 0 reset.

#### 6.4.5 Voltage Monitor 2 Reset

This reset is triggered by the MCU's on-chip voltage detector 2. Voltage detector 2 monitors the voltage applied to the VCC pin (Vdet2).

When the VW2C6 bit in the VW2C register is 1 (voltage monitor 2 reset when Vdet2 passage is detected), the MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC pin drops to Vdet2 or below. fOCO-S divided by 8 is automatically selected as the CPU clock after reset. Then, after the set amount of time, the MCU executes the program at the address indicated by the reset vector.

The LVD2R bit in the RSTFR register becomes 1 (voltage monitor 2 reset detected) after voltage monitor 2 reset. Some SFRs are not reset at voltage monitor 2 reset. Refer to 4. "Special Function Registers (SFRs)" for details.

The internal RAM is not reset.

Refer to 7. "Voltage Detector" for details of the voltage monitor 2 reset.

#### 6.4.6 Oscillator Stop Detect Reset

The MCU resets and stops the pins, CPU, and SFRs when the CM27 bit in the CM2 register is 0 (reset when oscillator stop detected), if it detects that the main clock oscillator has stopped.

The OSDR bit in the RSTFR register becomes 1 (oscillator stop detect reset detected) after oscillator stop detect reset.

Some SFRs are not reset at oscillator stop detect reset. Refer to 4. "Special Function Registers (SFRs)" for details. The internal RAM is not reset. When the main clock oscillator stop is detected while writing data to the internal RAM, the internal RAM becomes undefined.

Oscillator stop detect reset is canceled by hardware reset or voltage monitor 0 reset.

Refer to 8.7 "Oscillator Stop/Restart Detect Function" for details.

#### 6.4.7 Watchdog Timer Reset

The MCU resets the pins, CPU, and SFRs when the PM12 bit in the PM1 register is 1 (reset when watchdog timer underflows) and the watchdog timer underflows. Then the MCU executes the program at the address determined by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The WDR bit in the RSTFR register becomes 1 (watchdog timer reset detected) after watchdog timer reset. Some SFRs are not reset at watchdog timer reset. Refer to 4. "Special Function Registers (SFRs)" for details.

The internal RAM is not reset. When the watchdog timer underflows while writing data to the internal RAM, the internal RAM becomes undefined.

Refer to 13. "Watchdog Timer" for details.

### 6.4.8 Software Reset

The MCU resets the pins, CPU, and SFRs when the PM03 bit in the PM0 register is 1 (MCU reset). Then the MCU executes the program at the address determined by the reset vector.  $f_{OCO-S}$  divided by 8 is automatically selected as the CPU clock after reset.

The SWR bit in the RSTFR register becomes 1 (software reset detected) after software reset. Some SFRs are not reset at software reset. Refer to 4. "Special Function Registers (SFRs)" for details. The internal RAM is not reset.

## 6.5 Notes on Resets

### 6.5.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC) (Voltage range: 0 to 2)	0.05			V/ms

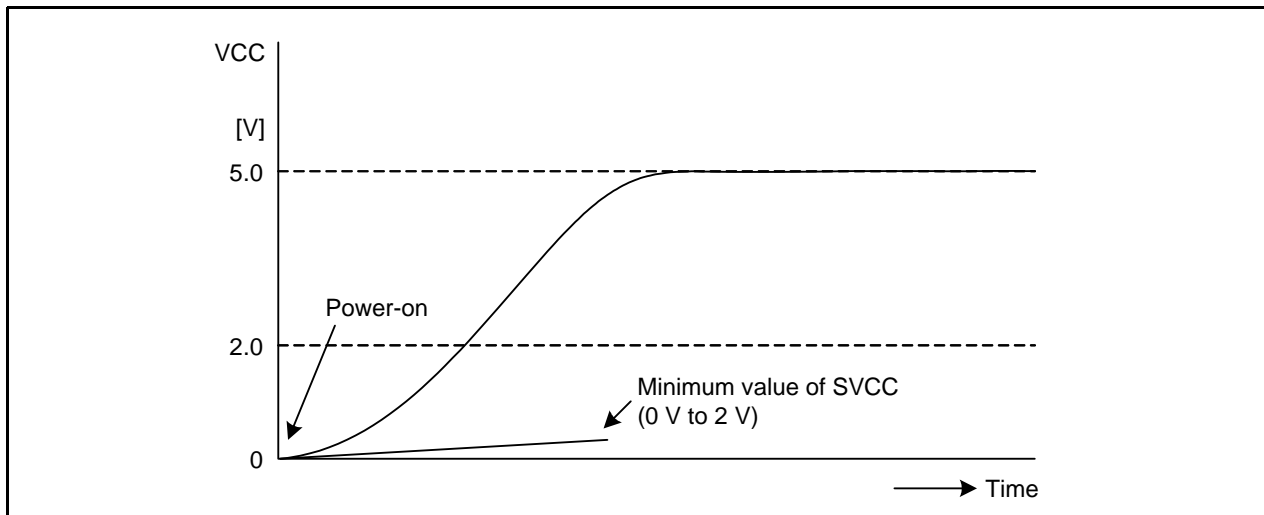


Figure 6.6 SVCC Timing

### 6.5.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use the power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable these bits by a program.

### 6.5.3 OSDR Bit (Oscillation Stop Detect Reset Detect Flag)

When an oscillator stop detect reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit in the RSTFR register is not affected by a hardware reset, but becomes 0 (not detected) from a voltage monitor 0 reset.

### 6.5.4 Hardware Reset When $VCC < V_{det0}$

If a hardware reset is executed when the LVDAS bit in the OFS1 address is 0 (voltage monitor 0 reset enabled after hardware reset) and  $VCC < V_{det0}$ , the MCU executes the program at the address indicated by the reset vector when changing the signal applied to the  $\overline{RESET}$  pin from low to high. A voltage monitor 0 reset is not generated.

## 7. Voltage Detector

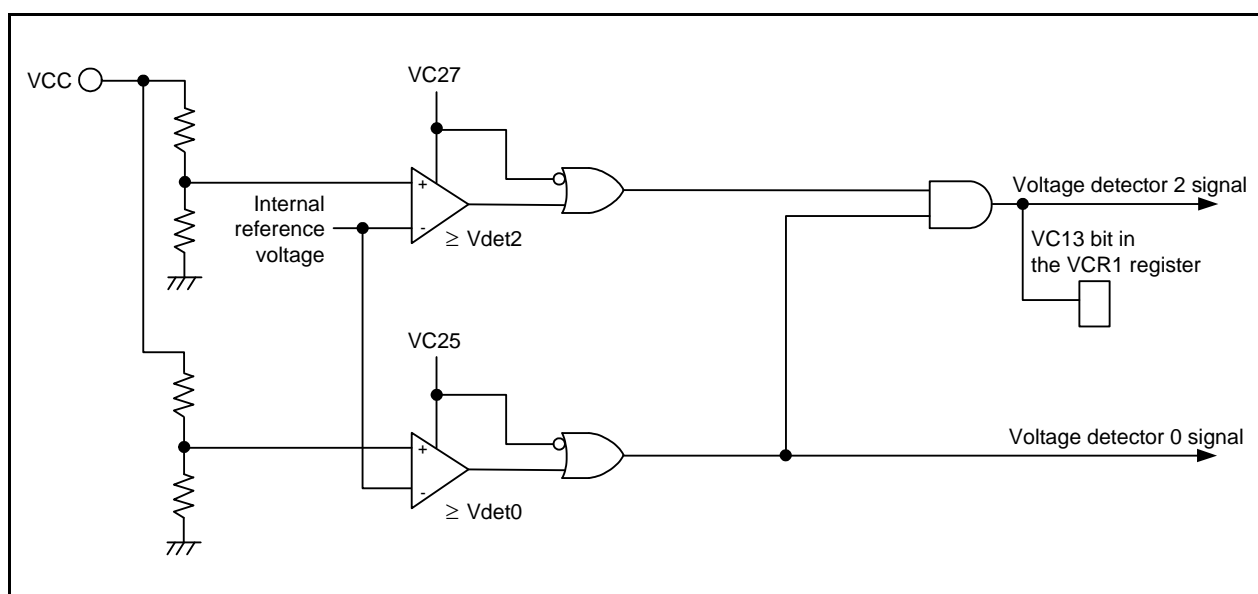
### 7.1 Introduction

The voltage detector monitors the voltage applied to the VCC pin. This circuit can be programmed to monitor the VCC input voltage. Voltage monitor 0 reset, voltage monitor 2 interrupt, and voltage monitor 2 reset can also be used.

Table 7.1 lists the Voltage Detector Specifications and Figure 7.1 shows Voltage Detector Block Diagram.

**Table 7.1 Voltage Detector Specifications**

Item		Voltage Detector 0	Voltage Detector 2
VCC monitor	Voltage to monitor	Vdet0	Vdet2
	Detection target	Whether passing Vdet0 by rising or falling	Whether passing Vdet2 by rising or falling
	Monitor	None	VC13 bit in VCR1 register Whether VCC is higher or lower than Vdet2
Process when voltage is detected	Reset	Voltage monitor 0 reset Reset at $V_{det0} > V_{CC}$ ; restart CPU operation at $V_{CC} > V_{det0}$	Voltage monitor 2 reset Reset at $V_{det2} > V_{CC}$ ; restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 2 interrupt Interrupt request at $V_{det2} > V_{CC}$ and $V_{CC} > V_{det2}$ when digital filter is enabled; interrupt request at $V_{det2} > V_{CC}$ or $V_{CC} > V_{det2}$ when digital filter is disabled
Digital filter	Switch enabled/disabled	None	Available
	Sampling time	None	(Divide-by-n of fOCO-S) × 3 n: 1, 2, 4, 8



**Figure 7.1 Voltage Detector Block Diagram**

## 7.2 Registers

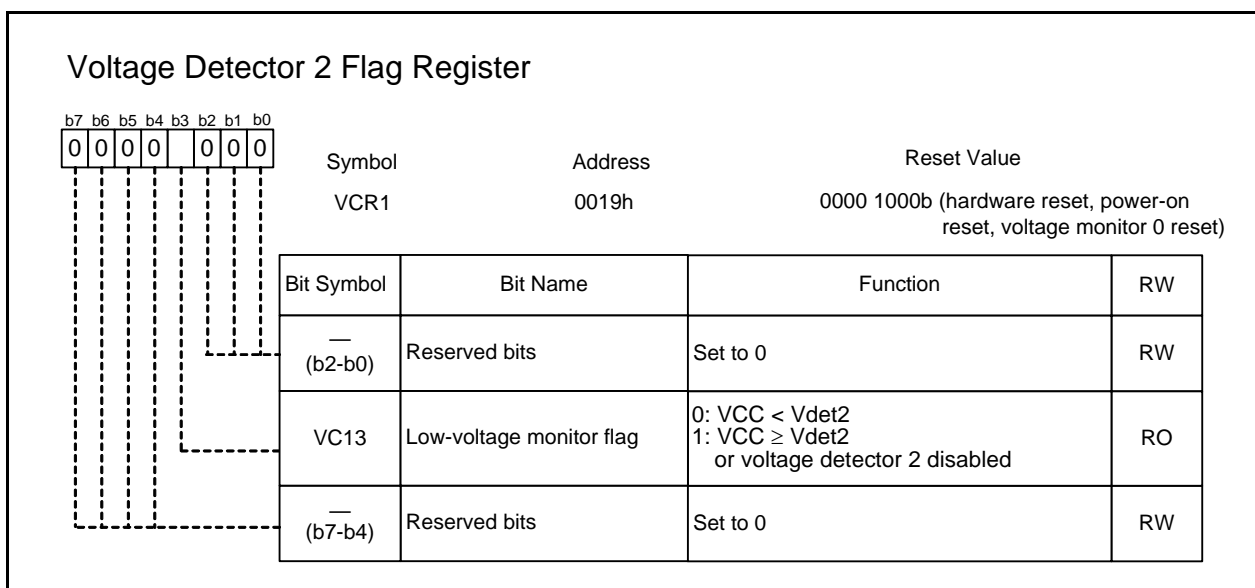
**Table 7.2 Registers**

Address	Register Name	Register Symbol	Reset Value
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (1, 5)
001Ah	Voltage Detector Operation Enable Register	VCR2	000X 0000b (2, 5) 001X 0000b (3, 5)
0026h	Voltage Monitor Function Select Register	VWCE	00h
0028h	Voltage Detector 2 Level Select Register	VD2LS	0000 0100b (4, 6)
002Ah	Voltage Monitor 0 Control Register	VW0C	1100 1X10b (2, 5) 1100 1X11b (3, 5)
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b (1, 7)

**Notes:**

1. Hardware reset, power-on reset, or voltage monitor 0 reset
2. When the LVDAS bit of the OFS1 address is 1 at hardware reset.
3. This value shows the value after any of the following resets.
  - Voltage monitor 0 reset
  - When the LVDAS bit of the OFS1 address is 0 at hardware reset
  - Power-on reset
4. Hardware reset, power-on reset, voltage monitor 0 reset, or voltage monitor 2 reset
5. The value does not change after voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.
6. The value does not change after oscillator stop detect reset, watchdog timer reset, or software reset.
7. Bits VW2C2 and VW2C3 are not changed after voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

### 7.2.1 Voltage Detector 2 Flag Register (VCR1)



This register does not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

#### VC13 (Low-voltage monitor flag) (b3)

The VC13 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled).

Condition to become 0:

- $V_{CC} < V_{det2}$  (when the VW12E bit is 1 and the VC27 bit is 1)

Conditions to become 1:

- $V_{CC} \geq V_{det2}$  (when the VW12E bit is 1 and the VC27 bit is 1)
- The VC27 bit is 0 (voltage detector 2 disabled).



## 7.2.2 Voltage Detector Operation Enable Register (VCR2)

Voltage Detector Operation Enable Register																			
<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px;">b7</td><td style="padding: 2px;">b6</td><td style="padding: 2px;">b5</td><td style="padding: 2px;">b4</td><td style="padding: 2px;">b3</td><td style="padding: 2px;">b2</td><td style="padding: 2px;">b1</td><td style="padding: 2px;">b0</td> </tr> <tr> <td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td> </tr> </table>	b7	b6	b5	b4	b3	b2	b1	b0	0	0	0	0	0	0	0	0	Symbol VCR2	Address 001Ah	Reset Value 000X 0000b <sup>(1)</sup> 001X 0000b <sup>(2)</sup>
b7	b6	b5	b4	b3	b2	b1	b0												
0	0	0	0	0	0	0	0												
— (b3-b0)	Reserved bits	Set to 0	RW																
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—																
VC25	Voltage detector 0 enable bit	0 : Disable voltage detector 0 1 : Enable voltage detector 0	RW																
— (b6)	Reserved bit	Set to 0	RW																
VC27	Voltage detector 2 enable bit	0 : Disable voltage detector 2 1 : Enable voltage detector 2	RW																

Notes:

1. When the LVDAS bit of the OFS1 address is 1 at hardware reset
2. This value shows the value after any of the following resets:
  - Voltage monitor 0 reset
  - When the LVDAS bit of the OFS1 address is 0 at hardware reset
  - Power-on reset

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting this register.

This register does not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

### VC25 (Voltage detector 0 enable bit) (b5)

To use voltage monitor 0 reset, set the VC25 bit to 1 (voltage detector 0 enabled). After changing the VC25 bit to 1, the detector starts operating when the td(E-A) elapses.

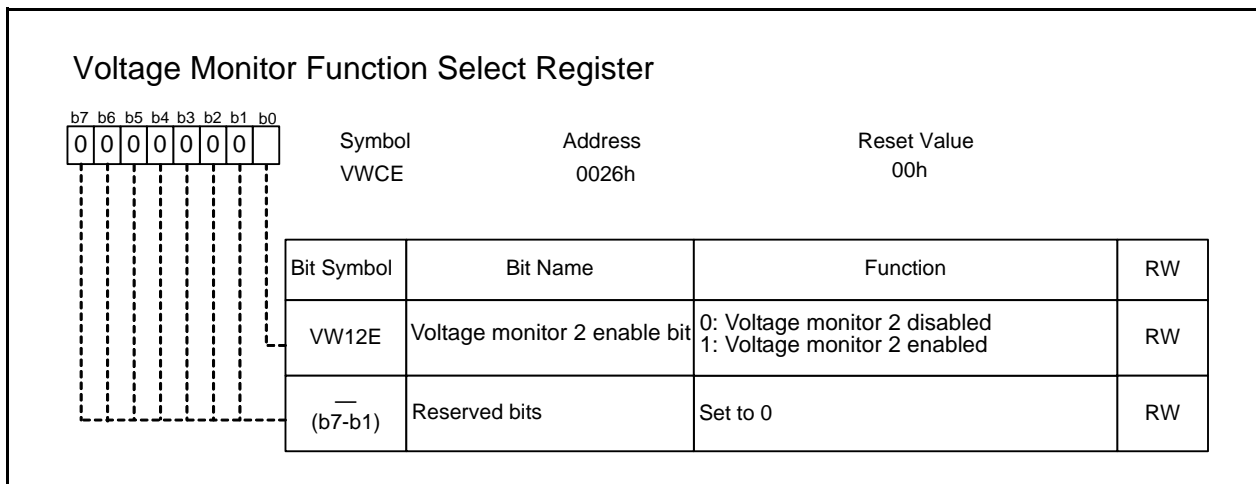
### VC27 (Voltage detector 2 enable bit) (b7)

Voltage detector 2 is enabled when the VW12E bit in the VWCE register is set to 1 (voltage monitor 2 enabled) and the VC27 bit is 1 (voltage detector 2 enabled). Set bits VW12E and VC27 to 1 under the following conditions:

- When using voltage monitor 2 interrupt/reset
- When using the VC13 bit in the VCR1 register
- When using the VW2C2 bit in the VW2C register

After changing this bit from 0 to 1, the detector will start operating after td(E-A) elapses.

### 7.2.3 Voltage Monitor Function Select Register (VWCE)

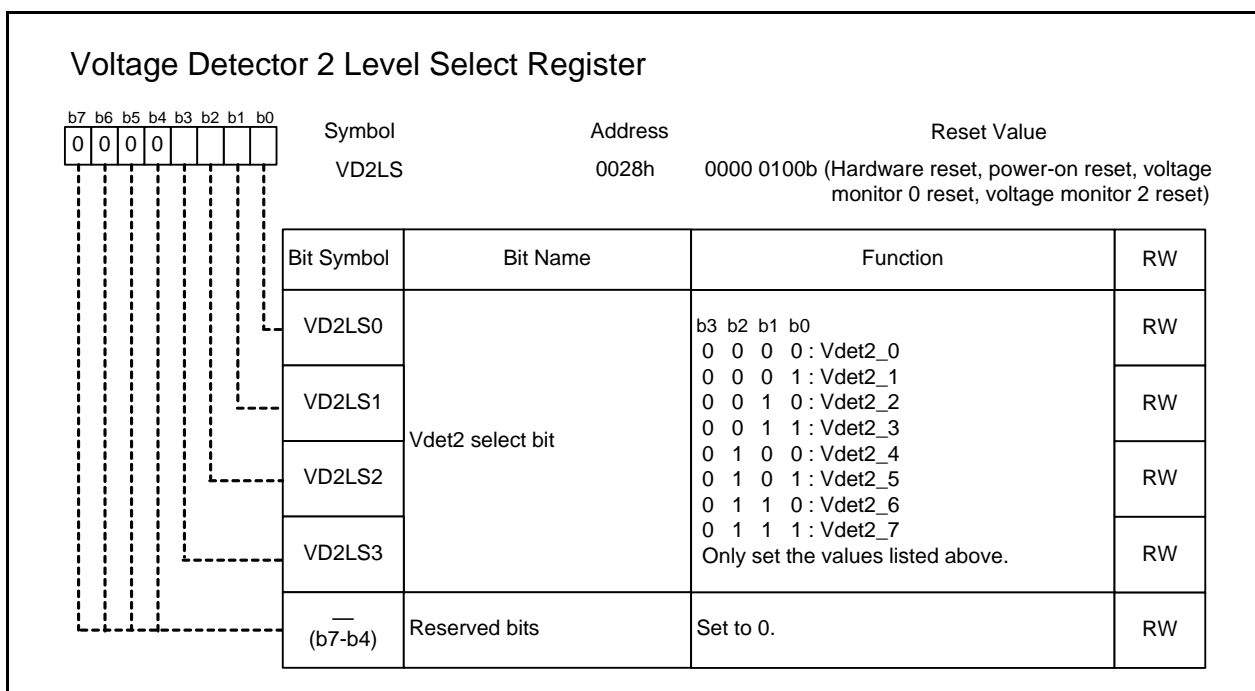


Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting this register.

VW12E (Voltage monitor 2 enable bit) (b0)

Set the VW12E bit to 1 (enabled) when the VC27 bit in the VCR2 register is 1 (enabled).

## 7.2.4 Voltage Detector 2 Level Select Register (VD2LS)



Set the PRC3 bit in the PRCR register to 1 (write enabled) before the VD2LS register is rewritten.

This register does not change at watchdog timer reset, oscillation stop detector reset, or software reset.

The value of the VD2LS register is affected by the VW12E bit in the VWCE register. Table 7.3 lists VD2LS Register Value. When setting the VW12E bit to 0 and then 1 after setting a value to the VD2LS register, the setting value to the VD2LS register is returned.

**Table 7.3 VD2LS Register Value**

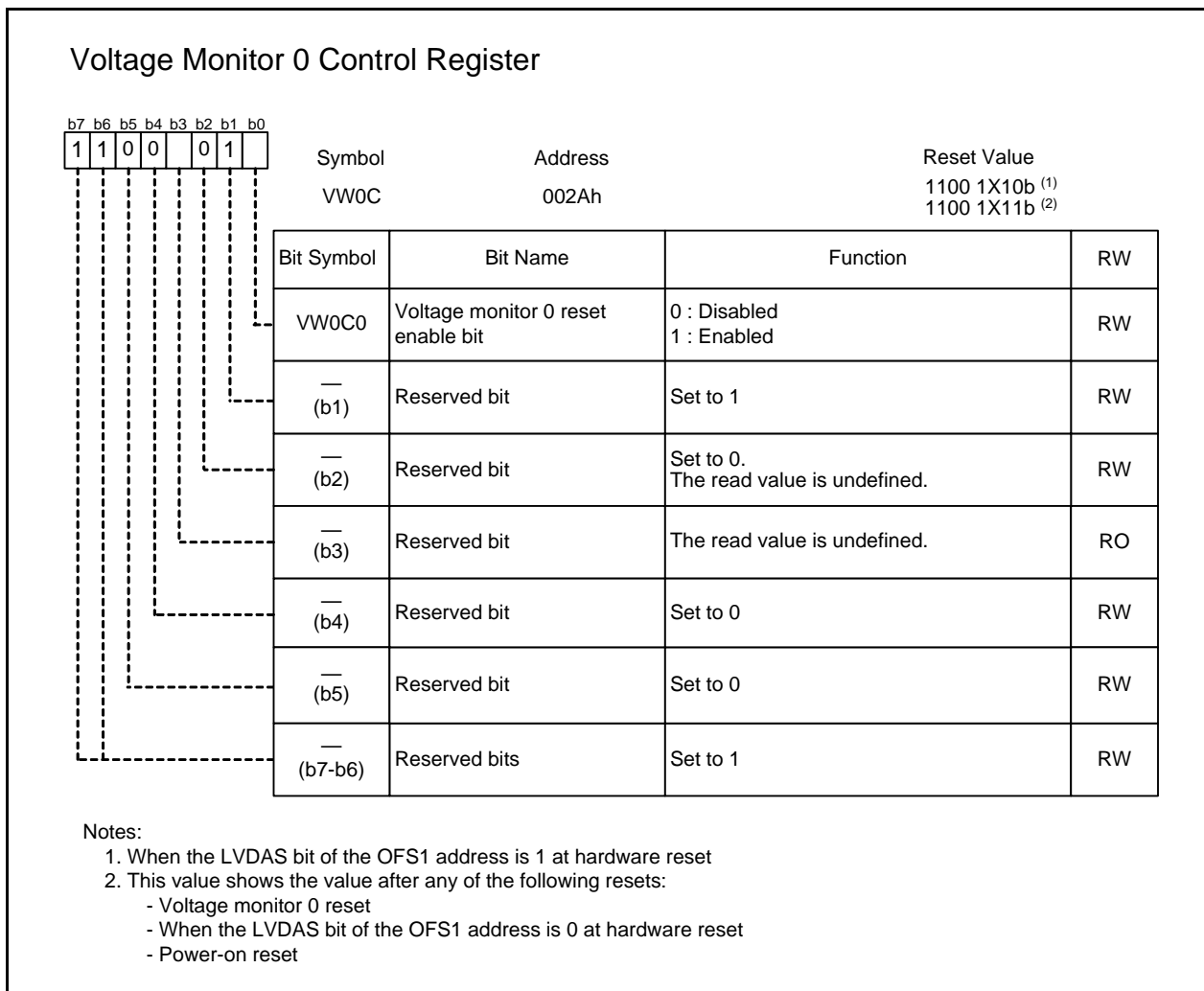
VW12E Bit	Value of the VD2LS Register
0	0000 0100b
1	Value set in the VD2LS register (0000 0111b when no value is set in the VD2LS register)

### VD2LS3-VD2LS0 (Vdet2 select bit) (b3-b0)

When using voltage detector 2, set the values shown in the VD2LS register diagram.

When not using voltage detector 2, the reset values can remain as is.

### 7.2.5 Voltage Monitor 0 Control Register (VW0C)



Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to this register.

This register does not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

#### VW0C0 (Voltage monitor 0 reset enable bit) (b0)

The VW0C0 bit is enabled when the VC25 bit in the VCR2 register is 1 (voltage detector 0 enabled). Set the VW0C0 bit to 0 (disabled) when the VC25 bit is 0 (voltage detector 0 disabled). Set bit 6 in the VW0C register, as well, when setting the VW0C0 bit to 1 (enabled).

## 7.2.6 Voltage Monitor 2 Control Register (VW2C)

Voltage Monitor 2 Control Register				
		Symbol VW2C	Address 002Ch	Reset Value 1000 0X10b (hardware reset, power-on reset, voltage monitor 0 reset)
Bit Symbol	Bit Name	Function	RW	
VW2C0	Voltage monitor 2 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW	
VW2C1	Voltage monitor 2 digital filter disable mode select bit	0 : Digital filter enabled 1 : Digital filter disabled	RW	
VW2C2	Voltage change detection flag	0 : Not detected 1 : Vdet2 passage detected	RW	
VW2C3	Watchdog timer detection flag	0 : Not detected 1 : Watchdog timer underflow detected	RW	
VW2F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW	
VW2F1				
VW2C6	Voltage monitor 2 mode select bit	0 : Voltage monitor 2 interrupt at Vdet2 passage 1 : Voltage monitor 2 reset at Vdet2 passage	RW	
VW2C7	Voltage monitor 2 interrupt/ reset generation condition select bit	0: When VCC reaches or goes above Vdet2 1: When VCC reaches or goes below Vdet2	RW	

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.

Bits VW2C2 and VW2C3 do not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

When rewriting the VW2C register (excluding the VW2C3 bit), the VW2C2 bit may become 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.

### VW2C0 (Voltage monitor 2 interrupt/reset enable bit) (b0)

The VW2C0 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled). Set the VW2C0 bit to 0 (disabled) when the VC27 bit is 0 (voltage detector 2 disabled).

### VW2C1 (Voltage monitor 2 digital filter disable mode select bit) (b1)

After using the voltage monitor 2 interrupt to exit stop mode, to use it again to exit stop mode, set the VW2C1 bit to 0 first and then to 1.

**VW2C2 (Voltage change detection flag) (b2)**

The VW2C2 bit is enabled when the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled). This bit does not change even if set to 1.

Condition to become 0:

- Writing this bit to 0

Condition to become 1:

- Refer to the following table.

**Table 7.4 Conditions Under Which the VW2C2 Bit Becomes 1**

Bit Setting (1)			Conditions under Which the VW2C2 Bit Becomes 1
VW2C1	VW2C6	VW2C7	
0	0	0 or 1	The VC13 bit changes from 0 to 1 or from 1 to 0.
	1	1	The VC13 bit changes from 1 to 0.
1	0	0	The VC13 bit changes from 0 to 1.
		1	The VC13 bit changes from 1 to 0.
	1	1	The VC13 bit changes from 1 to 0.

VC13 bit: Bit in the VCR1 register

Note:

1. Only set the values listed above.

**VW2C6 (Voltage monitor 2 mode select bit) (b6)**

The VW2C6 bit is enabled when the VW2C0 bit is 1 (voltage monitor 2 interrupt/reset enabled).

**VW2C7 (Voltage monitor 2 interrupt/reset generation condition select bit) (b7)**

The voltage monitor 2 interrupt/reset generation condition can be selected by the VW2C7 bit when the VW2C6 bit is 0 (voltage monitor 2 interrupt at Vdet2 passage) and the VW2C1 bit is 1 (digital filter disabled).

When the VW2C6 bit is 1 (voltage monitor 2 reset at Vdet2 passage), set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below). (Do not set the VW2C7 bit to 0.)

When the VW2C1 bit is 0 (digital filter enabled), regardless of the VW2C7 bit setting, the voltage monitor 2 interrupt is generated when VCC reaches Vdet2 or above, and also when VCC reaches Vdet2 or below.

### 7.3 Optional Function Select Area

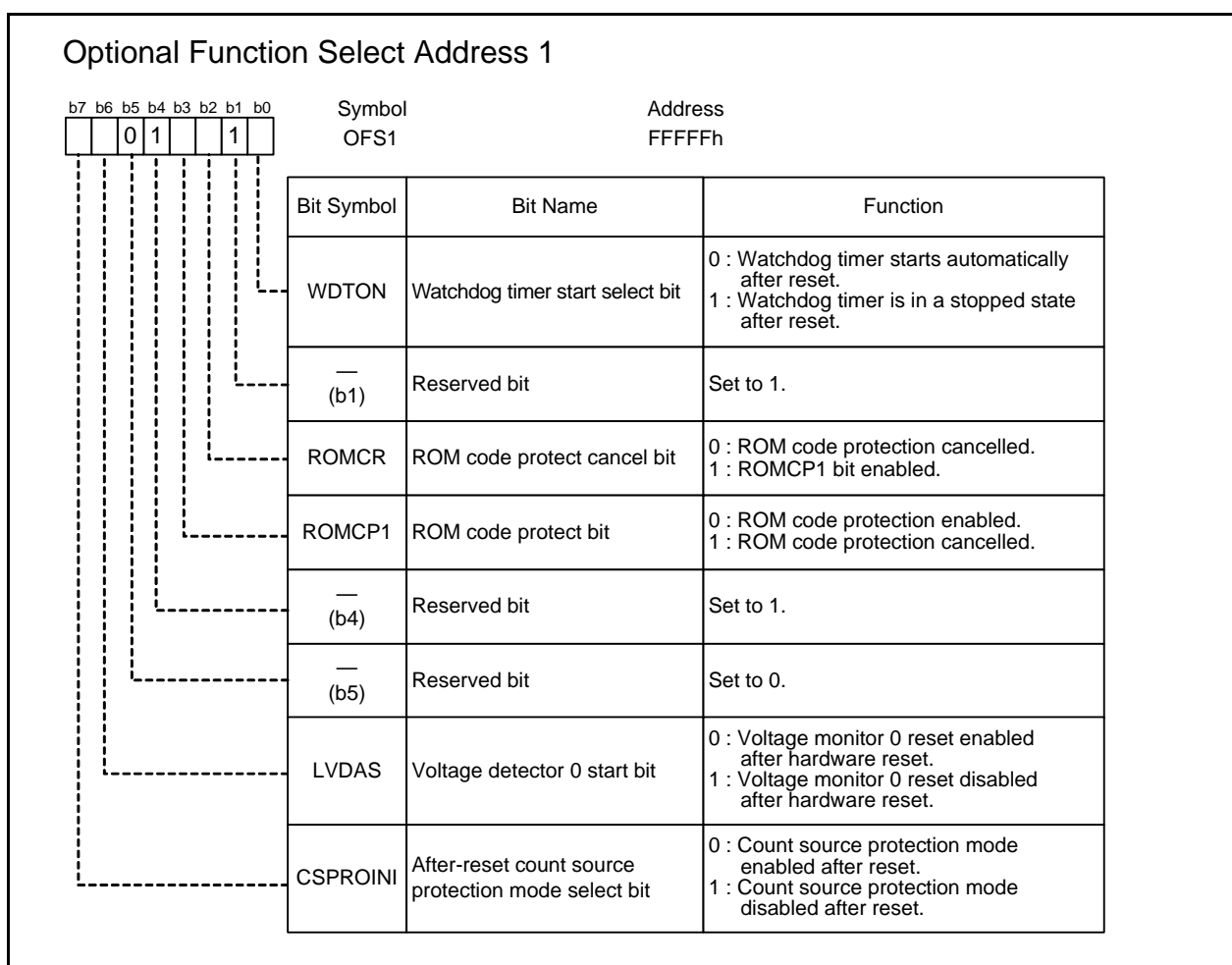
In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

In blank products, the OFS1 address value is FFh when shipped. After a value is written by the user, this address takes on the written value.

In programmed products, the OFS1 address value is the value set in the user program prior to shipping.

#### 7.3.1 Optional Function Select Address 1 (OFS1)



#### LVDAS (Voltage detector 0 start bit) (b6)

When using power-on reset, set this bit to 0 (voltage monitor 0 reset enabled after hardware reset). This bit is enabled in single-chip mode, while disabled in boot mode.

## 7.4 Operations

### 7.4.1 Digital Filter

A digital filter can be used to monitor VCC input voltage. For voltage detector 2, the digital filter is enabled when the VW2C1 bit in the VW2C register is set to 0 (digital filter enabled).

fOCO-S divided by 1, 2, 4, or 8 is selected as a sampling clock. When using the digital filter, set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on).

The VCC input level is sampled by the digital filter for every sampling clock. When the same sampled level is detected three times in a row, at the third sampling timing, the internal reset signal goes low or a voltage monitor 2 interrupt request is generated. Therefore, when the digital filter is used, the time from when the VCC input voltage level passes Vdet2 until when a reset or an interrupt is generated is up to three cycles of the sampling clock.

Since fOCO-S stops in stop mode, the digital filter does not function. When using voltage detector 2 to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Figure 7.2 shows Digital Filter Operation Example.

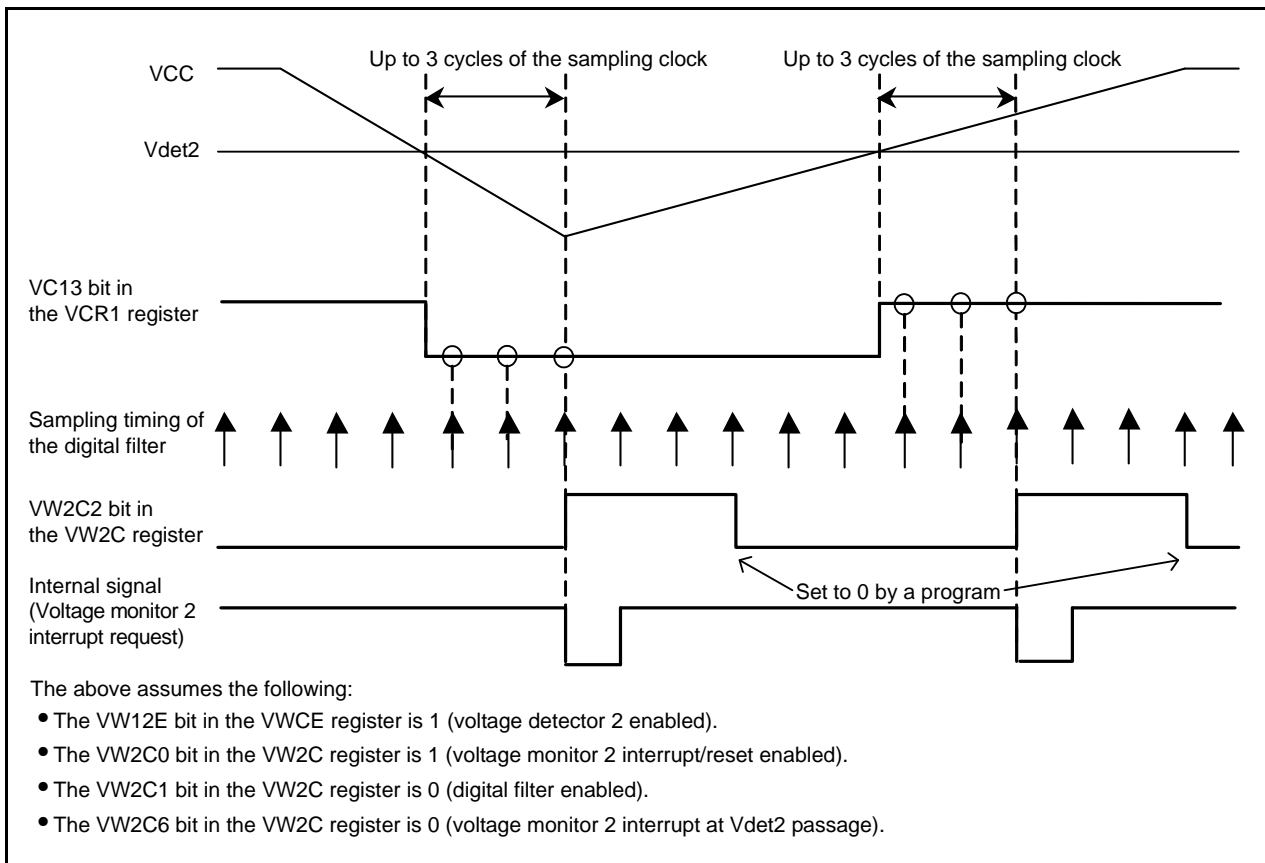
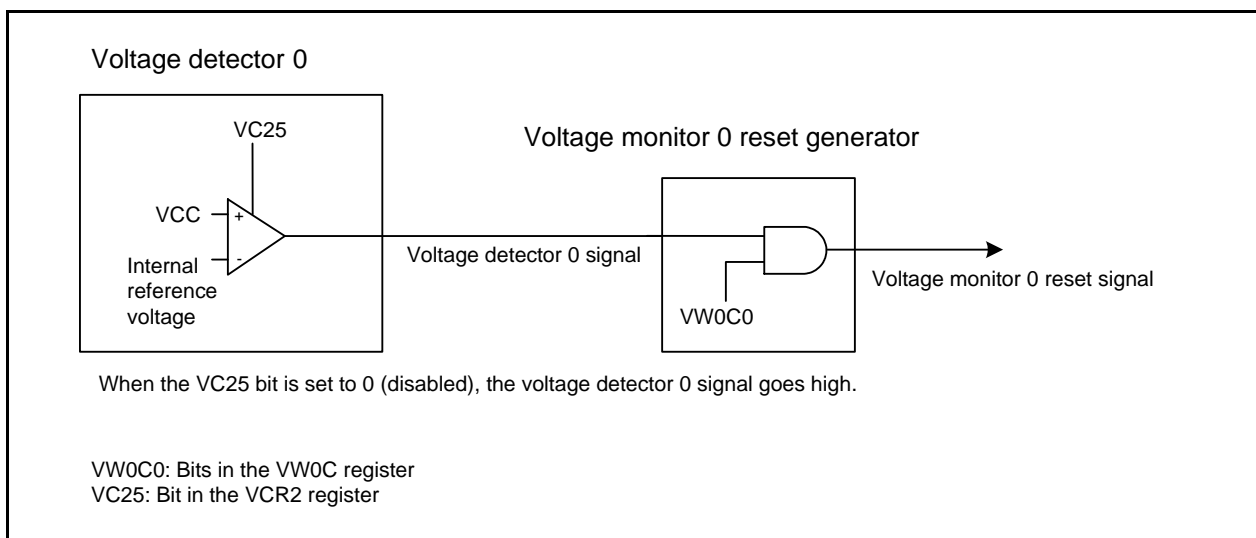


Figure 7.2 Digital Filter Operation Example



### 7.4.2 Voltage Detector 0

When the VC25 bit in the VCR2 register is 1 (voltage detector 0 enabled), voltage detector 0 monitors the voltage applied to the VCC pin and detects whether the voltage rises through or falls through Vdet0.



**Figure 7.3 Voltage Monitor 0 Reset Generator Block Diagram**

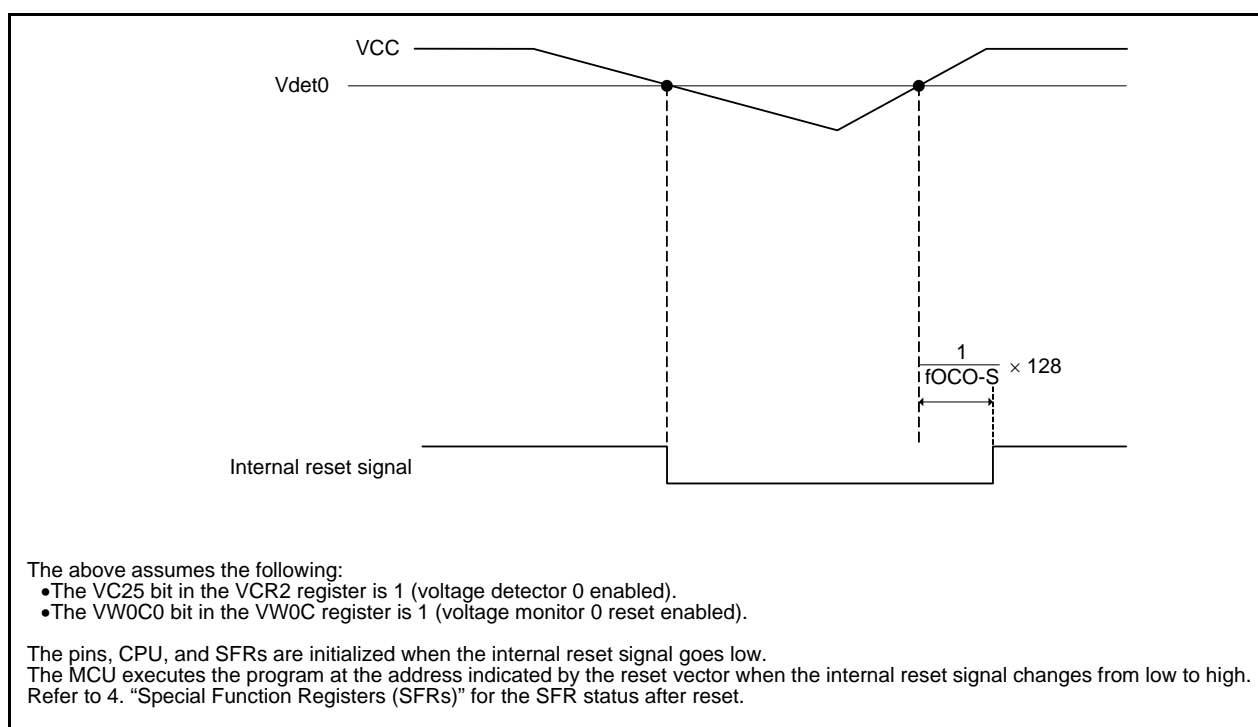
### 7.4.2.1 Voltage Monitor 0 Reset

Table 7.5 lists Steps to Set Voltage Monitor 0 Reset Related Bits.

**Table 7.5 Steps to Set Voltage Monitor 0 Reset Related Bits**

Step	
1	Set the VC25 bit in the VCR2 register to 1 (voltage detector 0 enabled).
2	Wait for $t_d(E-A)$ .
3	Set bits 6 and 7 in the VW0C register to 1.
4	Set bit 2 in the VW0C register to 0 (set this bit to 0 once again after step 3).
5	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).

Figure 7.4 shows Voltage Monitor 0 Reset Operation Example.



**Figure 7.4 Voltage Monitor 0 Reset Operation Example**

### 7.4.3 Voltage Detector 2

When the VW12E bit in the VWCE register is 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register is 1 (voltage detector 2 enabled), voltage detector 2 monitors the voltage applied to the VCC pin and detects whether the voltage rises through or falls through Vdet2.

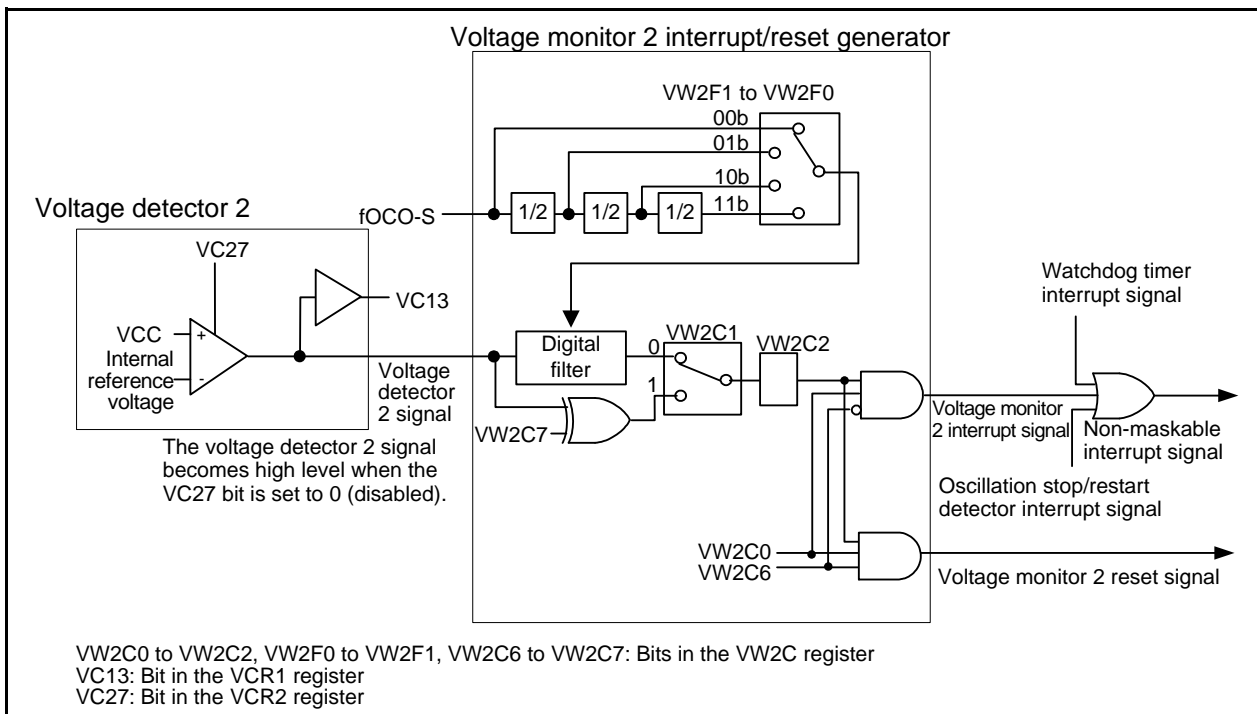


Figure 7.5 Voltage Monitor 2 Interrupt/Reset Generator

#### 7.4.3.1 Monitoring Vdet2

Set the VW12E bit in the VWCE register to 1 (voltage monitor 2 enabled) and the VC27 bit in the VCR2 register to 1 (voltage detector 2 enabled). Vdet2 can be monitored using the VC13 bit in the VCR1 register after td(E-A) elapses.

### 7.4.3.2 Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

Table 7.6 lists Procedure for Setting Voltage Monitor 2 Interrupt/Reset Related Bits.

**Table 7.6 Procedure for Setting Voltage Monitor 2 Interrupt/Reset Related Bits**

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		—	
2	Wait for digital filter sampling clock x 3 cycles.		— (no wait time)	
3	Set the VW12E bit in the VWCE register to 1 (voltage detector enabled).			
4	Use bits VD2LS3 to VD2LS0 in the VD2LS register to select Vdet2.			
5	Set the VC27 bit in the VCR2 register to 1 (voltage detector 2 enabled).			
6	Wait for td(E-A).			
7	Use bits VW2F0 to VW2F1 in the VW2C register to select the digital filter sampling clock.		Use the VW2C7 bit in the VW2C register to select the timing of the interrupt and reset request. <sup>(1)</sup>	
8 <sup>(2)</sup>	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).	
9 <sup>(2)</sup>	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).
10	Set the VW2C2 bit in the VW2C register to 0 (Vdet2 passage not detected).			
11	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled).			

Notes:

1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is 0, steps 7, 8, and 9 can be executed simultaneously (with one instruction).

When using voltage monitor 2 interrupt or voltage monitor 2 reset to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

When voltage monitor 2 reset is generated, the LVD2R bit in the RSTFR register is automatically becomes 1 (voltage monitor 2 reset detected). Refer to 6.4.5 "Voltage Monitor 2 Reset" for status after reset.

Figure 7.6 shows Voltage Monitor 2 Interrupt/Reset Operation Example.

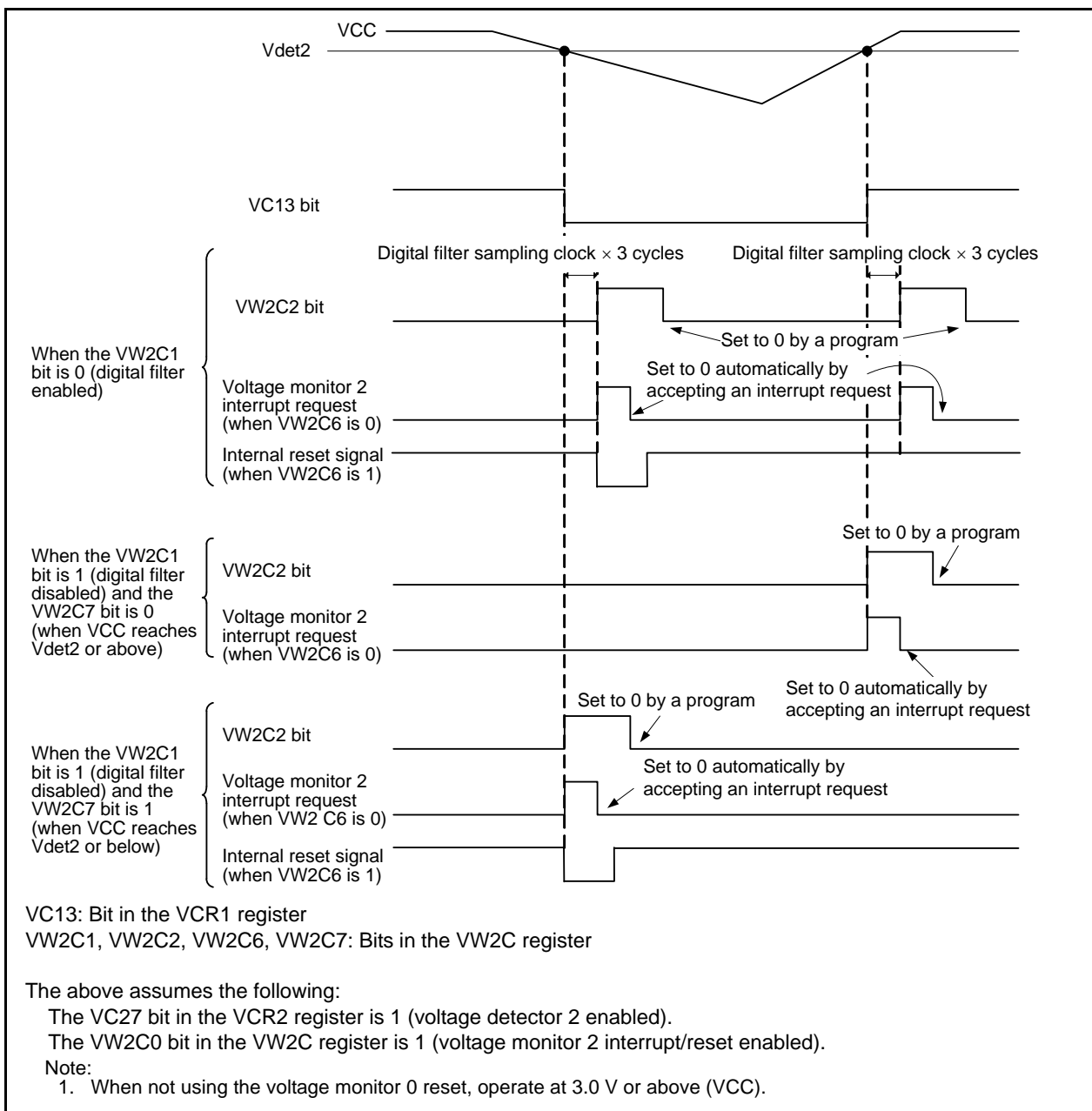


Figure 7.6 Voltage Monitor 2 Interrupt/Reset Operation Example

## 7.5 Interrupts

The voltage monitor 2 interrupt is a non-maskable interrupt.

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share the same vector. When using some functions together, read the detect flags of the events in an interrupt processing program, and determine the source of the interrupt.

The detect flag for voltage monitor 2 is the VW2C2 bit in the VW2C register. After the interrupt source is determined, set the VW2C2 bit to 0 (not detected).

## 8. Clock Generator

### 8.1 Introduction

The clock generator generates operating clocks for the CPU and peripheral functions. The following circuits are incorporated to generate the system clock signals.

- Main clock oscillator
- PLL frequency synthesizer
- 40 MHz on-chip oscillator
- 125 kHz on-chip oscillator
- Sub clock oscillator

Table 8.1 lists the specifications of the clock generator, and Figure 8.1 shows the block diagram of system clock generator.

**Table 8.1 Clock Generator Specifications**

Item	Main Clock Oscillator	PLL Frequency Synthesizer	On-Chip Oscillator		Sub Clock Oscillator
			40 MHz on-chip oscillator	125 kHz on-chip oscillator	
Application	<ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> </ul>	<ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> </ul>	<ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> <li>• CPU and peripheral function clock sources when the main clock stops oscillating</li> </ul>	<ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> <li>• CPU and peripheral function clock sources when the main clock stops oscillating</li> <li>• Watchdog timer count source when the CPU clock is stopped</li> </ul>	<ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> </ul>
Clock frequency	f(XIN)	f(PLL)	fOCO40M	fOCO-S	f(XCIN)
Connectable oscillators	<ul style="list-style-type: none"> <li>• Ceramic resonator</li> <li>• Crystal</li> </ul>	- (see note 1)	-	-	Crystal
Pins connecting to oscillator	XIN, XOUT	- (see note 1)	-	-	XCIN, XCOU
Oscillator start/stop function	Enabled	Enabled	Enabled	Enabled	Enabled
Oscillator status after reset	Oscillating	Stopped	Stopped	Oscillating	Stopped
Other	An externally generated clock can be input.	- (see note 1)	-	-	-

Note:

1. The PLL frequency synthesizer uses the main clock oscillator as a reference clock source. The items above are based on the main clock oscillator.

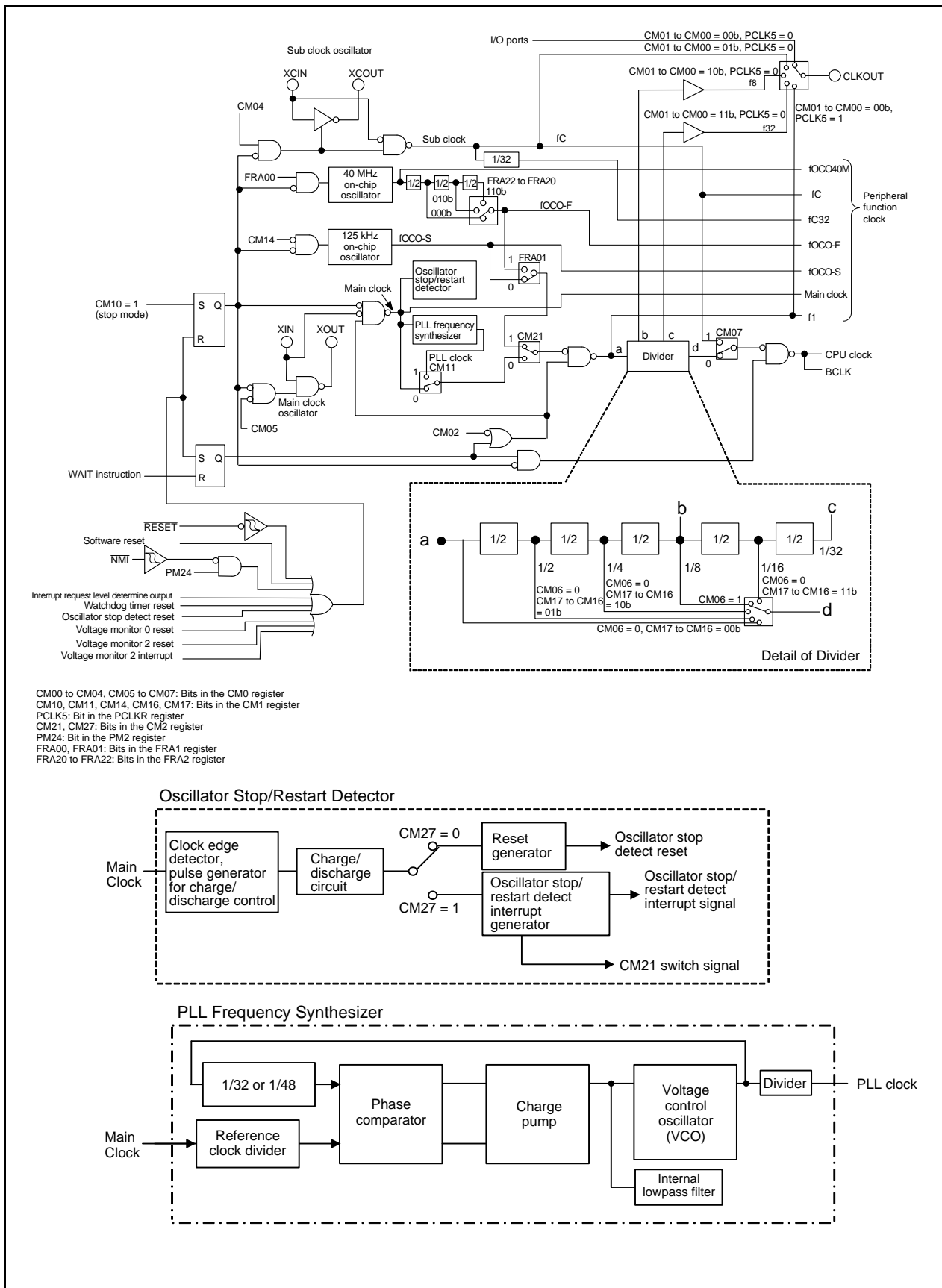


Figure 8.1 System Clock Generator



**Table 8.2 I/O Pins**

Pin Name	I/O	Function
XIN	Input	I/O pins for the main clock oscillator
XOUT	Output	
XCIN	Input (1)	I/O pins for a sub clock oscillator
XCOU	Output (1)	
CLKOUT	Output	Clock output

Note:

1. Set the port direction bits which share pins to 0 (input mode).

## 8.2 Registers

**Table 8.3 Registers**

Address	Register	Symbol	Reset Value
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (1)
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0024h	40 MHz On-Chip Oscillator Control Register 2	FRA2	0XX0 X000b

Note:

1. Bits CM20, CM21, and CM27 remain unchanged at oscillator stop detect reset.

### 8.2.1 System Clock Control Register 0 (CM0)

System Clock Control Register 0			
	Symbol CM0	Address 0006h	Reset Value 0100 1000b
Bit Symbol	Bit Name	Function	RW
CM00	Clock output function select bit	b1 b0 0 0 : I/O port 0 1 : Output fC 1 0 : Output f8 1 1 : Output f32	RW
CM01			
CM02	Wait mode peripheral function clock stop bit	0 : Peripheral function clock f1 does not stop in wait mode 1 : Peripheral function clock f1 stops in wait mode	RW
CM03	XCIN-XCOUT drive capacity select bit	0 : Low 1 : High	RW
CM04	Port XC select bit	0 : I/O port 1 : XCIN-XCOUT oscillation function	RW
CM05	Main clock stop bit	0 : On 1 : Off	RW
CM06	Main clock division select bit 0	0 : Bits CM16 and CM17 in the CM1 register enabled 1 : Divide-by-8 mode	RW
CM07	System clock select bit	0 : Main clock, PLL clock, or on-chip oscillator clock 1 : Sub clock	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register. See Table 9.3 "Clock-Related Bit Setting and Modes" to select a clock and mode.

#### CM01 and CM00 (Clock output function select bit) (b1-b0)

The CLKOUT pin outputs can be selected. These bits are enabled when the PCLK5 bit in the PCLKR register is set to 0. When the PCLK5 bit is 1, set bits CM01 and CM00 to 00b. Table 8.4 lists CLKOUT Pin Functions.

**Table 8.4 CLKOUT Pin Functions**

PCLKR Register PCLK5 bit	CM0 Register		CLKOUT Pin Output
	CM01 bit	CM00 bit	
0	0	0	I/O port
0	0	1	fC is output
0	1	0	f8 is output
0	1	1	f32 is output
1	0	0	f1 is output

Only set the combinations listed above.

**CM02 (Wait mode peripheral function clock stop bit) (b2)**

This bit is used to stop the f1 peripheral function clock in wait mode. fC, fC32, fOCO-S, fOCO-F, and fOCO40M are not affected by the CM02 bit.

When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM02 bit remains unchanged even when written to.

**CM03 (XCIN-XCOOUT drive capacity select Bit) (b3)**

Setting the driving capacity to low while sub clock oscillation is stable reduces power consumption.

The CM03 bit becomes 1 (high) while the CM04 bit is 0 (P8\_6 and P8\_7 are I/O ports), or when entering stop mode.

**CM04 (Port XC select bit) (b4)**

The CM03 bit becomes 1 (high) while the CM04 bit is 0 (P8\_6 and P8\_7 are I/O ports).

**CM05 (Main clock stop bit) (b5)**

This bit is used to stop the main clock. The main clock is allowed to stop in the following cases.

- Entering low power mode
- Entering 125 kHz on-chip oscillator low power mode
- Stopping the main clock in 40 MHz on-chip oscillator mode

This bit cannot be used to detect if the main clock is stopped or not. Refer to 8.7 "Oscillator Stop/Restart Detect Function" for details on main clock stop detection.

When the PM21 bit in the PM2 register is 1 (clock change disabled), this bit remains unchanged even when written to.

**CM06 (Main clock division select bit) (b6)**

The CM06 bit becomes 1 (divide-by-8 mode) under the following conditions:

- When entering stop mode
- When the CM21 bit in the CM2 register is 0 (main clock or PLL clock) and the CM05 bit is 1 (main clock off)

**CM07 (System clock select bit) (b7)**

The CPU clock source and the peripheral function clock f1 depend on combinations of the bit status of the CM07 bit, the CM11 bit in the CM1 register, and the CM21 bit in the CM2 register. When the CM07 bit is 0 (main clock, PLL clock or on-chip oscillator clock used as CPU clock), the CPU clock source and the peripheral function clock f1 can be selected by combinations of the bit status of the CM11 bit and the CM21 bit. When the CM07 bit is 1 (sub clock used as CPU clock), the CPU clock source is fC, and the peripheral function clock f1 can be selected by combinations of the bit status of bits CM11 and CM21.

When setting the PM21 bit in the PM2 register to 1 (clock change disabled), set the CM07 bit to 0 (main clock) before setting the PM21 bit to 1. When the PM21 bit is set to 1, this bit remains unchanged even when written to.

## 8.2.2 System Clock Control Register 1 (CM1)

System Clock Control Register 1			
Bit	Symbol	Address	Reset Value
b7		0007h	0010 0000b
b6			
b5			
b4			
b3			
b2			
b1			
b0	0		
Symbol: CM1			
Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit	0 : Clock on 1 : All clocks off (stop mode)	RW
CM11	System clock select bit 1	0 : Main clock 1 : PLL clock	RW
— (b2)	Reserved bit	Set to 0	RW
CM13	XIN-XOUT feedback resistor select bit	0 : Internal feedback resistor connected 1 : Internal feedback resistor not connected	RW
CM14	125 kHz on-chip oscillator stop bit	0 : 125 kHz on-chip oscillator on 1 : 125 kHz on-chip oscillator off	RW
CM15	XIN-XOUT drive capacity select bit	0 : Low 1 : High	RW
CM16	Main clock division select bit 1	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			

Rewrite the CM1 register after setting the PRC0 bit in the PRCR register to 1 (write enabled). See Table 9.3 “Clock-Related Bit Setting and Modes” to select a clock and a mode.

### CM10 (All clock stop control bit) (b0)

When the CM11 bit is 1 (PLL clock), or the CM20 bit in the CM2 register is 1 (oscillator stop/restart detect function enabled), do not set the CM10 bit to 1.

In the following cases, this bit remains unchanged even when written to (The MCU does not enter stop mode).

- The PM21 bit in the PM2 register is 1 (clock change disabled).
- The CSPRO bit in the CSPR register is 1 (watchdog timer count source protection mode enabled).
- The PLC07 bit in the PLC0 register is 1 (PLL on).
- A low is input to the  $\overline{\text{NMI}}$  pin.

### CM11 (System clock select bit) (b1)

The CM11 bit is valid when the CM21 bit in the CM2 register is set to 0 (main clock or PLL clock).

The CPU clock source and the peripheral function clock f1 can be selected by the CM11 bit when the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock used as CPU clock). The peripheral function clock f1 can be selected by the CM11 bit when the CM07 bit is 1 (sub clock used as CPU clock).

When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM11 bit remains unchanged even when written to.

### CM13 (XIN-XOUT feedback resistor select bit) (b3)

The CM13 bit can be used when the main clock is not used at all, or when the externally generated clock is supplied to the XIN pin. When connecting a ceramic resonator or crystal between pins XIN and XOUT, set the CM13 bit to 0 (internal feedback resistor connected). Do not set this bit to 1.

When the CM10 bit is 1 (stop mode), the feedback resistor is not connected regardless of the CM13 bit value.

### CM14 (125 kHz on-chip oscillator stop bit) (b4)

The CM14 bit can be set to 1 (125 kHz on-chip oscillator off) when the CM21 bit is 0 (main clock or PLL clock). When the CM21 bit is set to 1 (on-chip oscillator clock), the CM14 bit is automatically set to 0 (125 kHz on-chip oscillator on) and remains unchanged even when 1 is written to this bit. Note that the 125 kHz on-chip oscillator does not stop.

When the CSPRO bit in the CSPR register is 1 (watchdog timer count source protection mode), the CM14 bit is automatically set to 0 (125 kHz on-chip oscillator on) and remains unchanged even when 1 is written to this bit. Note that the 125 kHz on-chip oscillator does not stop.

### CM15 (XIN-XOUT drive capacity select bit) (b5)

In the following cases, the CM15 bit is fixed as 1 (drive capacity high):

- Entering stop mode.
- The CM21 bit in the CM2 register is 0 (main clock or PLL clock) and the CM05 bit in the CM0 register is set to 1 (main clock stopped).

### CM17 and CM16 (Main clock division select bit 1) (b7-b6)

Bits CM17 and CM16 are enabled when the CM06 bit is 0 (bits CM17 and CM16 enabled).

### 8.2.3 Oscillation Stop Detection Register (CM2)

Oscillation Stop Detection Register										
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
	X	0	0					CM2	000Ch	0X00 0010b
Bit Symbol	Bit Name	Function	RW							
CM20	Oscillator stop/restart detect enable bit	0: Oscillator stop/restart detect function disabled 1: Oscillator stop/restart detect function enabled	RW							
CM21	System clock select bit 2	0: Main clock or PLL clock 1: On-chip oscillator clock	RW							
CM22	Oscillator stop/restart detect flag	0: Main clock stop/restart not detected 1: Main clock stop/restart detected	RW							
CM23	XIN monitor flag	0: Main clock oscillating 1: Main clock stopped	RO							
— (b5-b4)	Reserved bits	Set to 0	RW							
— (b6)	No register bit. If necessary, set to 0. The read value is undefined.		—							
CM27	Operation select bit (when an oscillator stop/restart is detected)	0: Oscillator stop detect reset 1: Oscillator stop/restart detect interrupt	RW							

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

Bits CM20, CM21, and CM27 do not change at oscillator stop detect reset.

See Table 9.3 “Clock-Related Bit Setting and Modes” to select a clock and a mode.

#### CM20 (Oscillator stop/restart detect enable bit) (b0)

Set the CM20 bit to 0 (oscillator stop/restart detect function disabled) to enter stop mode. Set the CM20 bit back to 1 (enabled) after exiting stop mode.

When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM20 bit remains unchanged even when being written.

#### CM21 (System clock select bit 2) (b1)

When the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock used as CPU clock source), the CPU clock source and the peripheral function clock f1 can be selected by the CM21 bit. When the CM07 bit is 1 (sub clock used as CPU clock source), the peripheral function clock f1 can be selected by the CM21 bit.

To set the CM21 bit to 1 (on-chip oscillator clock), set the FRA01 bit in the FRA0 register to select either the 125 kHz on-chip oscillator, or the 40 MHz on-chip oscillator.

When the CM20 bit is 1 (oscillator stop/restart detect function enabled) and the CM23 bit is 1 (main clock stopped), do not set the CM21 bit to 0 (main clock or PLL clock).

When the CM20 bit is 1 (oscillator stop/restart detect function enabled), the CM27 bit is 1 (oscillator stop/restart detect interrupt), and the main clock is used as a CPU clock source, the CM21 bit becomes 1 (on-chip oscillator clock) if the main clock stop is detected. Refer to 8.7 “Oscillator Stop/Restart Detect Function” for details.

### CM22 (Oscillator stop/restart detect flag) (b2)

Condition to become 0:

- Set it to 0.

Conditions to become 1:

- Main clock stop is detected.
- Main clock restart is detected.

(The CM22 bit remains unchanged even if 1 is written.)

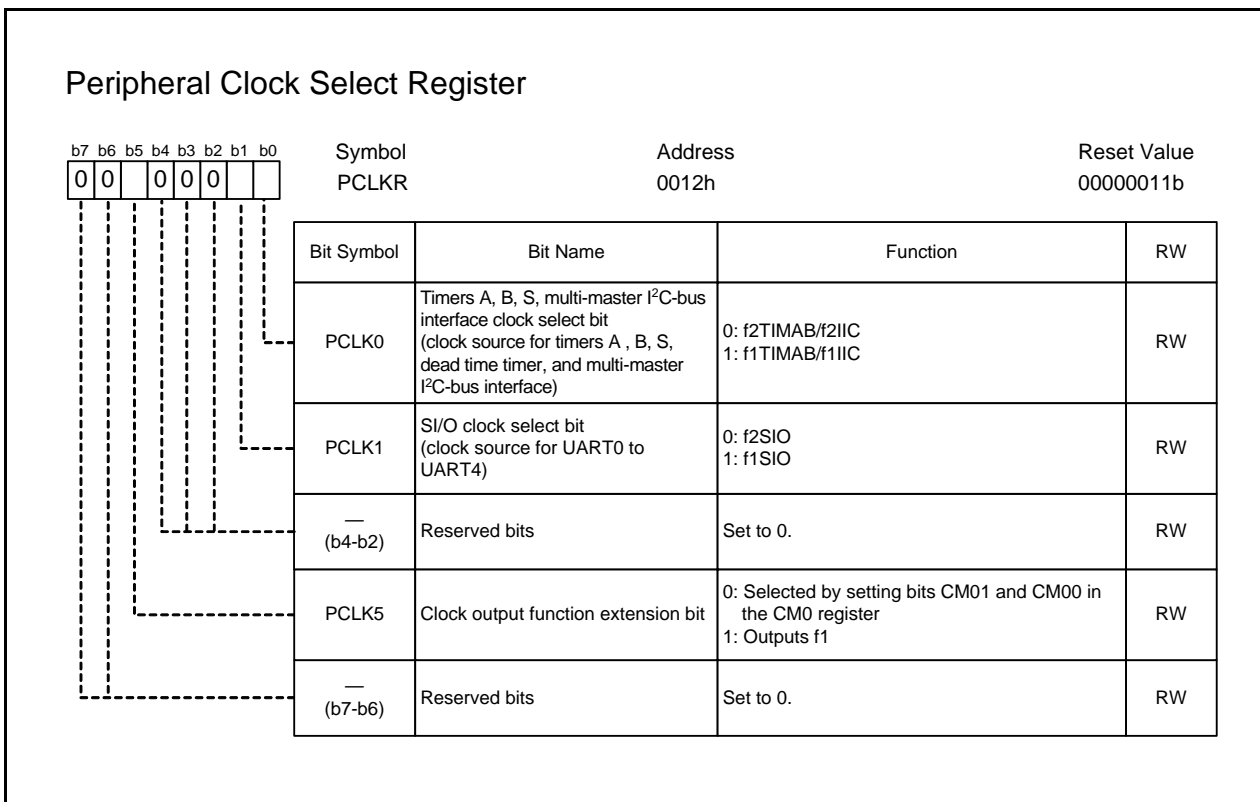
When the CM22 bit changes state from 0 to 1, an oscillator stop/restart detect interrupt is generated. Use this bit in an interrupt routine to determine the factors of interrupts between the oscillator stop/restart detect interrupt and other interrupts.

When the CM22 bit is 1 and oscillator stop or restart is detected, an oscillator stop/restart detect interrupt is not generated. The bit does not become 0 even if an oscillator stop/restart detect interrupt request is accepted.

### CM23 (XIN monitor flag) (b3)

Determine the main clock status by reading the CM23 bit several times in the oscillator stop/restart detect interrupt routine.

### 8.2.4 Peripheral Clock Select Register (PCLKR)



Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

#### PCLK5 (Clock output function extension bit) (b5)

Output from the CLKOUT pin is selectable. When the PCLK5 bit is 1, set bits CM01 and CM00 to 00b. See Table 8.4 “CLKOUT Pin Functions”.



## 8.2.5 PLL Control Register 0 (PLC0)

PLL Control Register 0												
b7	b6	b5	b4	b3	b2	b1	b0	Symbol PLC0	Address 001Ch	Reset Value 0X01 X010b		
								Bit Symbol	Bit Name	Function	RW	
								PLC00	PLL multiplying factor select bit	b2 b1 b0 0 0 0 : Do not set 0 0 1 : Multiply-by-2 0 1 0 : Multiply-by-4 0 1 1 : Multiply-by-6 1 0 0 : Multiply-by-8	RW	
								PLC01				RW
								PLC02			1 0 0 : Multiply-by-8 1 0 1 : ] Do not set these values 1 1 0 : ] 1 1 1 : ]	RW
								— (b3)		Reserved bit	The read value is undefined	RO
								PLC04		Reference frequency counter set bit	b5 b4 0 0 : No division 0 1 : Divide-by-2 1 0 : Divide-by-4 1 1 : Do not set	RW
								PLC05				RW
								— (b6)	No register bit. If necessary, set to 0. The read value is undefined.		—	
								PLC07	Operation enable bit	0 : PLL off 1 : PLL on	RW	

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

### PLC02 to PLC00 (PLL multiplying factor select bit) (b2-b0)

Write to bits PLC00 to PLC02 when the PLC07 bit is 0 (PLL off).

When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to bits PLC02 to PLC00 has no effect.

### PLC05 and PLC04 (Reference frequency counter set bit) (b5-b4)

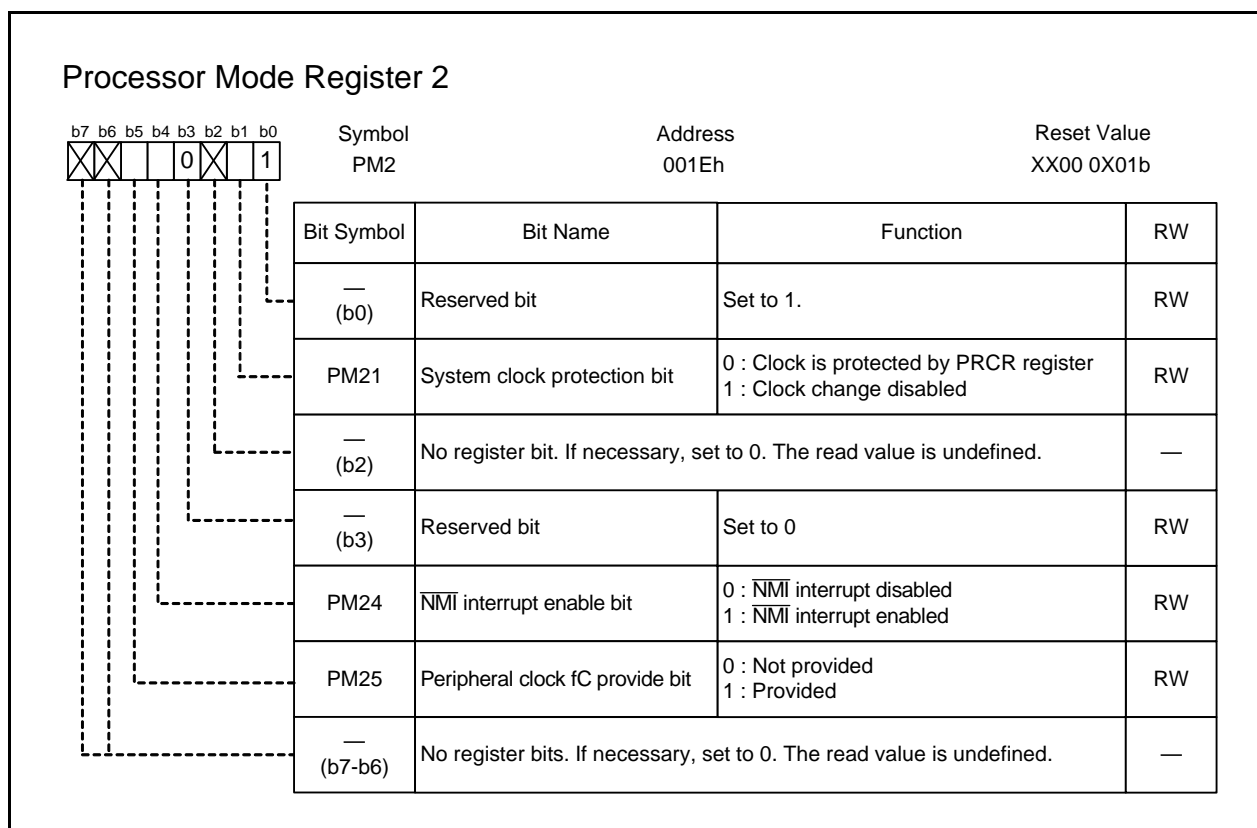
Write to bits PLC05 and PLC04 when the PLC07 bit is 0 (PLL off).

When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to bits PLC05 and PLC04 has no effect.

### PLC07 (Operation enable bit) (b7)

When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to the PLC07 bit has no effect.

## 8.2.6 Processor Mode Register 2 (PM2)



Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.

### PM21 (System clock protection bit) (b1)

The PM21 bit is used to protect the CPU clock. (Refer to 8.6 “System Clock Protection Function”).  
When the PM21 bit is set to 1, writing to the following bits has no effect:

- Bits CM02, CM05, and CM07 in the CM0 register
- Bits CM10 and CM11 in the CM1 register
- The CM20 bit in the CM2 register
- All bits in the PLC0 register

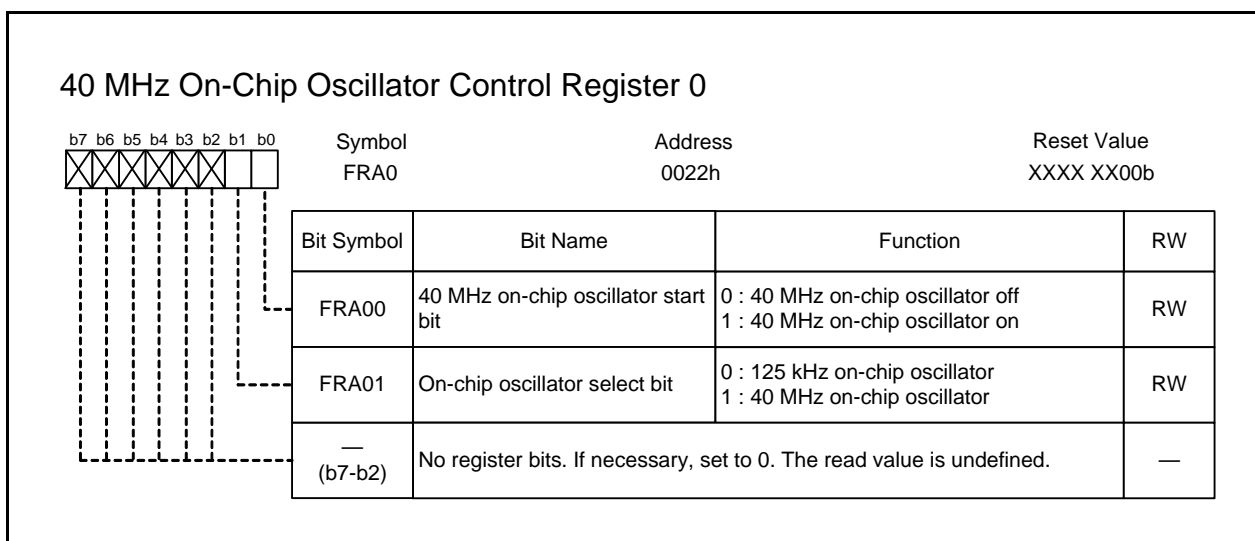
Do not execute the WAIT instruction when the PM21 bit is 1.

Once the PM21 bit is set to 1, it cannot be set to 0 by a program (writing 0 has no effect).

### PM25 (Peripheral clock fC provide bit) (b5)

The PM25 bit provides fC to the real-time clock. (See Figure 8.5 “Peripheral Function Clocks”.)

### 8.2.7 40 MHz On-Chip Oscillator Control Register 0 (FRA0)



Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled). See Table 9.3 “Clock-Related Bit Setting and Modes” to select a clock and a mode.

#### FRA00 (40 MHz on-chip oscillator start bit) (b0)

When using an oscillator stop/restart detect interrupt, do not set the FRA00 bit to 0 (40 MHz on-chip oscillator off) while the FRA01 bit to 1 (40 MHz on-chip oscillator), and vice versa.

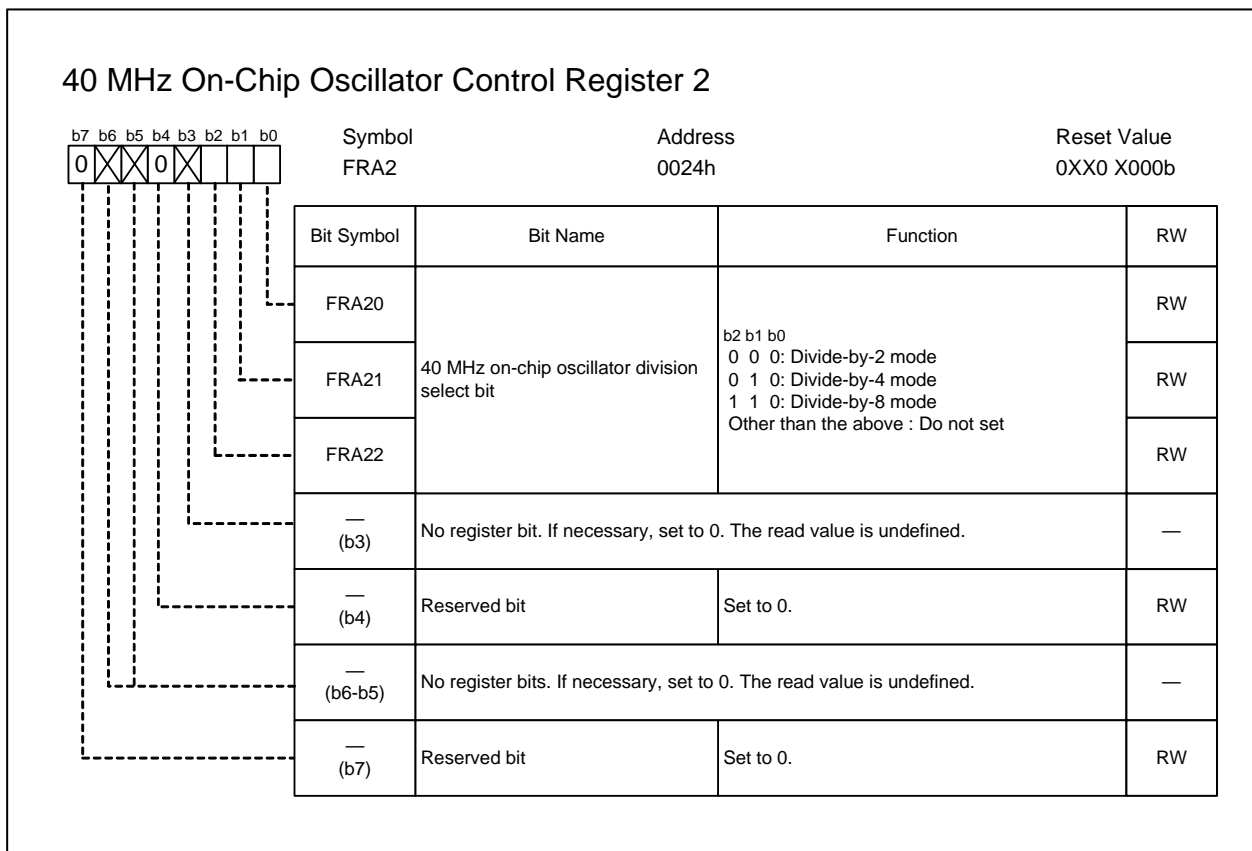
#### FRA01 (On-chip oscillator select bit) (b1)

Change the FRA01 bit if the both of the following conditions are met:

- When the FRA00 bit is 1 (40 MHz on-chip oscillator on) and oscillation is stable
- When the CM14 bit in the CM1 register is 0 (125 kHz on-chip oscillator on) and oscillation is stable

When setting the FRA01 bit to 0 (125 kHz on-chip oscillator), do not set the FRA00 bit to 0 (40 MHz on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

### 8.2.8 40 MHz On-Chip Oscillator Control Register 2 (FRA2)



Set the FRA2 register after the PRC0 bit in the PRCR register is set to 1 (write enabled).

## 8.3 Clocks Generated by Clock Generators

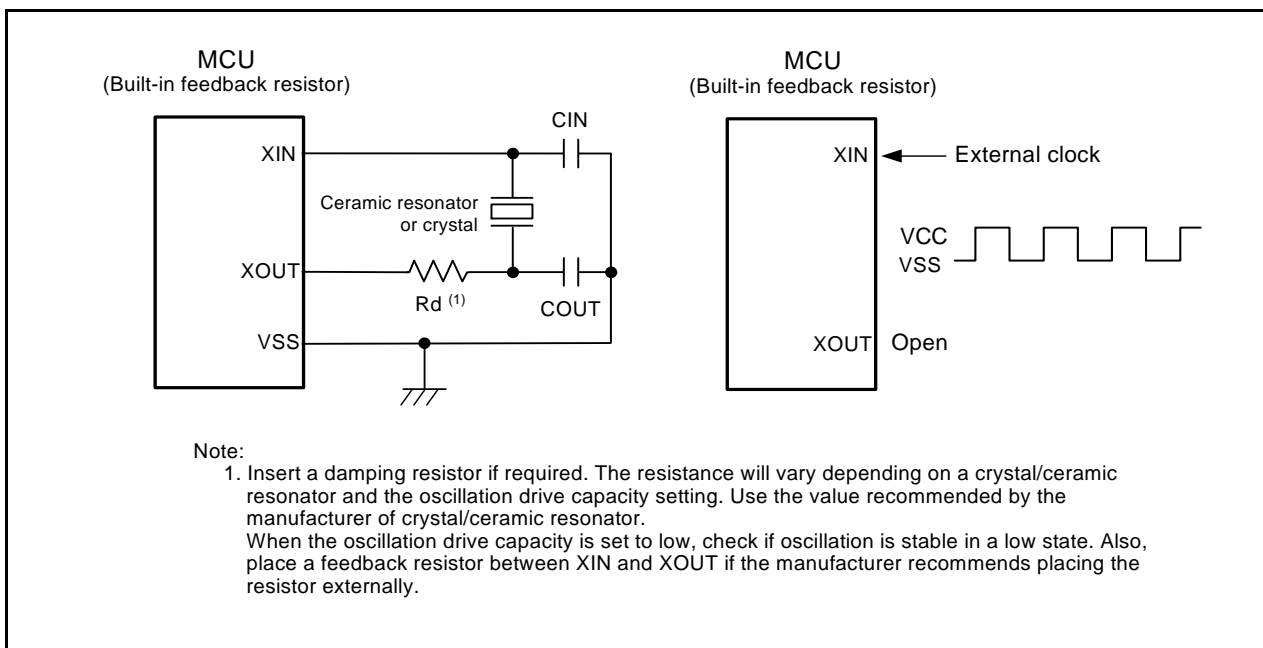
Clocks generated by the clock generators are described below.

### 8.3.1 Main Clock

This clock is supplied by the main clock oscillator and used as a clock source for the CPU and peripheral function clocks. After reset, the main clock is running, but is not used as a clock source for the CPU.

The main clock oscillator is configured by connecting a ceramic resonator or crystal between pins XIN and XOUT. The main clock oscillator contains a feedback resistor, which is disconnected from the oscillator in stop mode in order to reduce the amount of power consumed by the chip. The main clock oscillator may also be configured by feeding an externally generated clock to the XIN pin.

Figure 8.2 shows Main Clock Connection Example.



**Figure 8.2 Main Clock Connection Example**

The XOUT becomes high by setting the CM05 bit in the CM0 register to 1 (main clock oscillator turned off) after switching the clock source for the CPU clock to the sub clock (fC) or on-chip oscillator clock (fOCO-F, fOCO-S). In this case, the XIN is pulled high to the XOUT via the feedback resistor because the internal feedback resistor remains connected.

When the main clock oscillator is not used, setting the CM13 bit in the CM1 register to 1 enables to select the internal feedback resistor not connected.

Perform the following steps to start or stop the main clock. Refer to 8.2 “Registers” for details on register and bit access.

To start the main clock oscillation:

- (1) Set the CM15 bit to 1 (drive capacity high) when a ceramic resonator or crystal is connected between pins XIN and XOUT.
- (2) Set the CM05 bit to 0 (main clock oscillating).
- (3) Wait until main clock oscillation stabilizes. (When using an external clock, input the external clock through the XIN pin.)

To stop the main clock oscillation,

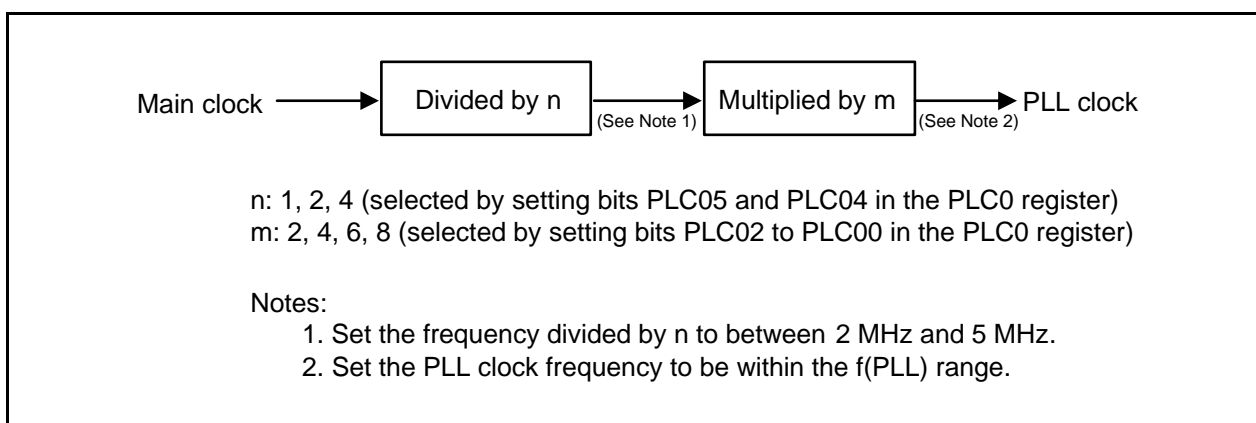
- (1) Set the CM20 bit in the CM2 register to 0 (oscillator stop/restart detect function disabled).
- (2) Set the CM05 bit to 1 (stop).
- (3) Stop the external clock (when inputting the external clock through the XIN pin).

### 8.3.2 PLL Clock

PLL clock is generated by the PLL frequency synthesizer. This clock is used as the clock source for the CPU and peripheral function clocks.

After reset, the PLL frequency synthesizer is stopped.

PLL clock is a clock which divides the main clock by the selected values of bits PLC05 to PLC04 in the PLC0 register, and then multiplied by the selected values of bits PLC02 to PLC00. Set bits PLC05 and PLC04 to fit divided frequency between 2 MHz and 5 MHz. Figure 8.3 shows Relation between Main Clock and PLL Clock.



**Figure 8.3 Relation between Main Clock and PLL Clock**

**Table 8.5 Example Settings for PLL Clock Frequencies**

Main Clock	Setting Value		PLL Clock
	Bits PLC05 to PLC04	Bits PLC02 to PLC00	
10 MHz	01b (divide-by-2)	010b (multiply-by-4)	20 MHz
5 MHz	00b (not divided)	010b (multiply-by-4)	
12 MHz	10b (divide-by-4)	100b (multiply-by-8)	24 MHz
6 MHz	01b (divide-by-2)	100b (multiply-by-8)	
16 MHz	10b (divide-by-4)	100b (multiply-by-8)	32 MHz
8 MHz	01b (divide-by-2)	100b (multiply-by-8)	

### 8.3.3 fOCO40M

fOCO40M is a 40 MHz clock (approx.) supplied by the 40 MHz on-chip oscillator. It is the clock source for  $\phi$ AD in the A/D converter.

Follow the steps below to start or stop the 40 MHz on-chip oscillator clock. Refer to 8.2 “Registers” for details on register and bit access.

40 MHz on-chip oscillator start

- (1) Set the FRA00 bit in the FRA0 register to 1 (40 MHz on-chip oscillator on).
- (2) Wait for  $t_{su}(fOCO40M)$ .

40 MHz on-chip oscillator stop

- (1) Set the FRA01 bit in the FRA0 register to 0 (125 MHz on-chip oscillator) (when the CM27 bit is 1 (oscillator stop/restart detect interrupt)).
- (2) Set the FRA00 bit in the FRA0 register to 0 (40 MHz on-chip oscillator off).

### 8.3.4 fOCO-F

fOCO-F is a 40 MHz clock (approx.) supplied by the 40 MHz on-chip oscillator, and divided by the selected values of bits FRA22 to FRA20 in the FRA2 register. It is the clock source for the CPU and peripheral function clocks.

After reset, fOCO-F is stopped.

If the main clock stops oscillating and the FRA01 bit is 1 when the CM20 bit in the CM2 register is 1 (oscillator stop/restart detect function enabled), and the CM27 bit is 1 (oscillator stop/restart detect interrupt), fOCO-F is used as the clock source for the CPU.

Refer to 8.3.3 “fOCO40M” to start or stop the 40 MHz on-chip oscillator clock.

### 8.3.5 125 kHz On-Chip Oscillator Clock (fOCO-S)

This clock is approximately 125 kHz, and is supplied by the 125 kHz on-chip oscillator. It is used as the clock source for the CPU and peripheral function clocks. In addition, when the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), this clock is used as the count source for the watchdog timer (refer to 13.4.3 “Count Source Protection Mode Enabled”).

After reset, fOCO-S divided by 8 becomes the CPU clock.

If the main clock stops oscillating and the FRA01 bit is 0, when the CM20 bit in the CM2 register is 1 (oscillator stop/restart detect function enabled) and the CM27 bit is 1 (oscillator stop/restart detect interrupt), the 125 kHz on-chip oscillator automatically starts operating and supplying the necessary clock for the MCU.

Follow the steps below to start or stop fOCO-S. Refer to 8.2 “Registers” for details on register and bit access.

To start fOCO-S:

- (1) Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on).
- (2) Wait for  $t_{su}(fOCO-S)$ .

To start fOCO-S:

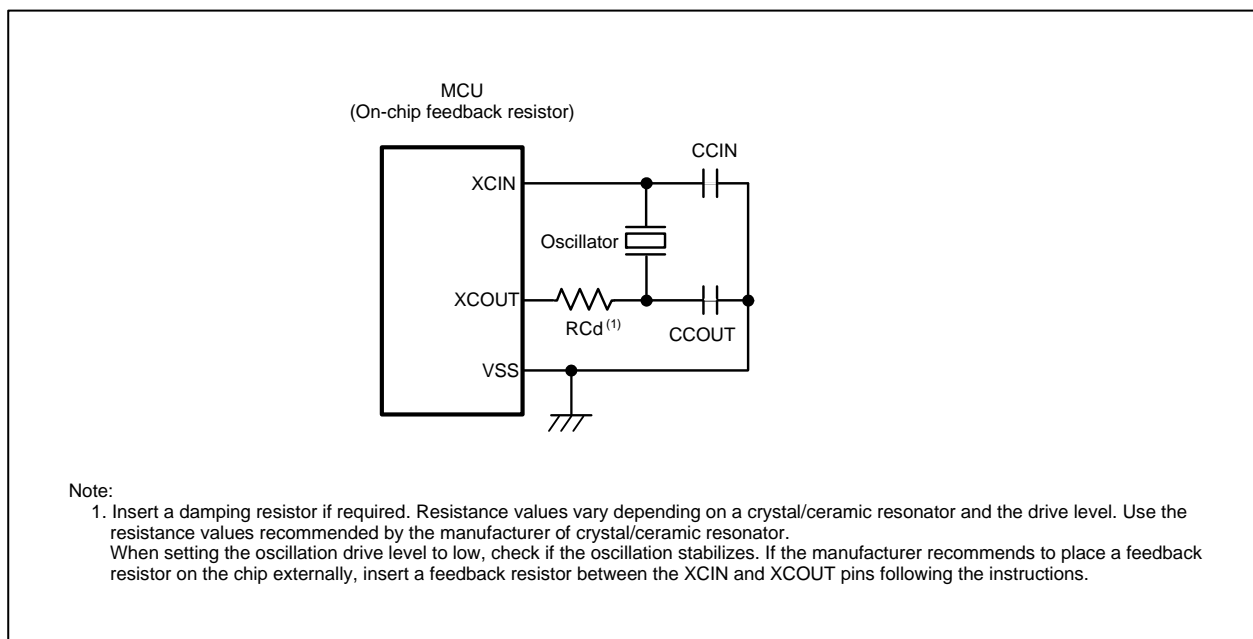
- (1) Set the CM14 bit in the CM1 register to 1 (125 kHz on-chip oscillator off).

When the CM21 bit is 1 (on-chip oscillator used as the clock source for the CPU), the CM14 bit becomes 0 (125 kHz on-chip oscillator on).

### 8.3.6 Sub Clock (fC)

The sub clock is supplied by the sub clock oscillator. This clock is the clock source for count sources of the CPU clock, timer A, timer B, real-time clock.

The sub clock oscillator is configured by connecting a crystal between pins XCIN and XCOUT. The sub clock oscillator contains a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. Figure 8.4 shows Sub Clock Connection Example.



**Figure 8.4 Sub Clock Connection Example**

After reset, the sub clock is stopped. At this time, the feedback resistor is disconnected from the oscillator.

Follow the steps below to start the sub clock. Refer to 8.2 "Registers" for details on register and bit access.

- (1) Set the PU21 bit in the PUR2 register to 0 (P8\_4 to P8\_7 not pulled high).
- (2) Set bits PD8\_6 and PD8\_7 in the PD8 register to 0 (P8\_6, P8\_7 function as input ports).
- (3) Set the CM04 bit to 1 (XCIN-XCOUT oscillation function). Set the CM03 bit to 1 (XCIN-XCOUT drive capacity high).
- (4) Wait until sub clock oscillation stabilizes.



## 8.4 CPU Clock and Peripheral Function Clocks

The CPU is run by the CPU clock, and the peripheral functions are run by the peripheral function clocks.

### 8.4.1 CPU Clock and BCLK

The CPU clock is an operating clock for the CPU and watchdog timer.

The main clock, PLL clock, fOCO-F, fOCO-S, or fC can be selected as the clock source for the CPU clock. (See Table 9.2 “Clocks in Normal Operating Mode”.)

When the main clock, PLL clock, fOCO-F or fOCO-S is selected as the clock source for the CPU clock, the selected clock divided by 1, 2, 4, 8 or 16 becomes the CPU clock. Use the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register to select a frequency-divided value.

When fC is selected as the clock source for the CPU clock, it is not divided and is used directly as the CPU clock.

After reset, fOCO-S divided by 8 becomes the CPU clock. Note that when entering stop mode or when the CM21 bit in the CM2 register is 0 (main clock or PLL clock) and the CM05 bit is 1 (main clock off), the CM06 bit in the CM0 register becomes 1 (divide-by-8 mode).

BCLK is a bus reference clock.

### 8.4.2 Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC, Main Clock)

f1, fOCO40M, fOCO-F, fOCO-S, and fC32 are operating clocks for the peripheral functions.

f1 is one of the following:

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

f1 is used for timers A, B, and S, the task monitor timer, real-time clock, UART0 to UART4, multi-master I<sup>2</sup>C-bus interface, and the A/D converter. It also can be used as a sampling clock for  $\overline{\text{NMI}}$ , P1\_7 digital debounce filter.

When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to 1 (peripheral function clock f1 turned off during wait mode), the f1 clock is stopped.

fOCO40M can be used for the A/D converter. fOCO40M can be used when the FRA00 bit in the FRA0 register is 1 (40 MHz on-chip oscillator on).

fOCO-F can be used for timers A and B, and UART0 to UART4.

fOCO-F can be used when the FRA00 bit in the FRA0 register is 1 (40 MHz on-chip oscillator on).

fOCO-S is used for timers A and B. It is also used for reset, voltage detector. fOCO-S is also used when the CM14 bit in the CM1 register is set to 0 (125 kHz on-chip oscillator on).

fC divided by 32 becomes fC32. fC32 is used for timers A and B, and can be used when the sub clock is on.

fC is used as the count source for the real-time clock when the PM25 bit in the PM2 register is 1 (peripheral clock fC provided). fC can be used when the sub clock is on.

The main clock can be used for CAN module.

Figure 8.5 shows Peripheral Function Clocks.

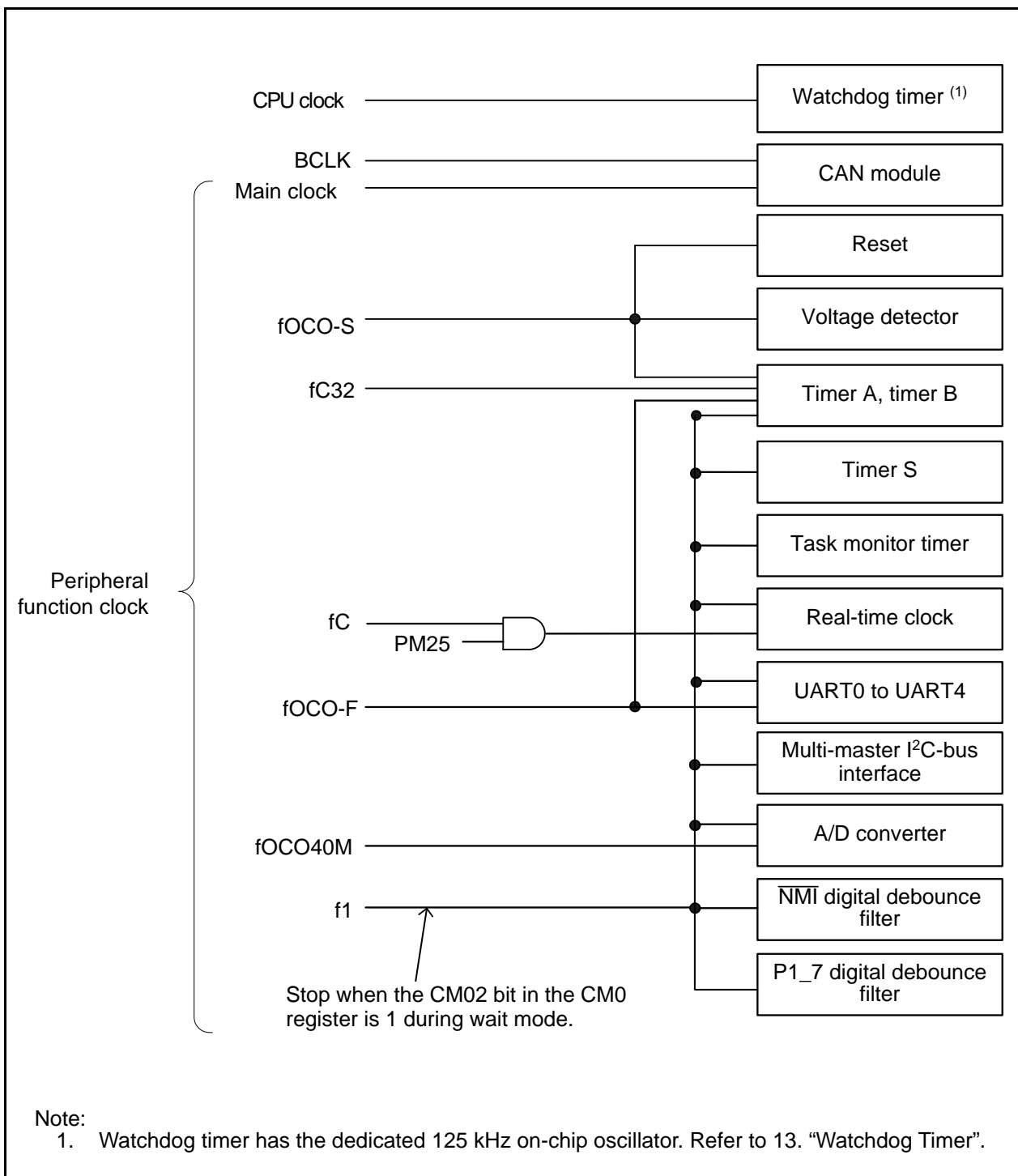


Figure 8.5 Peripheral Function Clocks

## 8.5 Clock Output Function

The f1, f8, f32 or fC clock can be output from the CLKOUT pin. Use bits CM01 to CM00 in the CM0 register, and the PCLK5 bit in the PCLKR register to select a clock. f8 has the same frequency as f1 divided by 8, and f32 has the same frequency as f1 divided by 32.

Set the frequency of the clock output from the CLKOUT pin to 25 MHz or below.

## 8.6 System Clock Protection Function

The system clock protection function prohibits the CPU clock from changing clock sources when the main clock is selected as the CPU clock source. This is to prevent the CPU clock from stopping due to an unexpected program operation.

When the PM21 bit in the PM2 register is set to 1 (clock change disabled), the following bits remain unchanged even if they are written to:

- The CM02 bit in the CM0 register (peripheral function clock f1 in wait mode)
- The CM05 bit in the CM0 register (to prevent the main clock from being stopped)
- The CM07 bit in the CM0 register (clock source of the CPU clock)
- The CM10 bit in the CM1 register (MCU does not enter stop mode)
- The CM11 bit in the CM1 register (clock source of the CPU clock)
- The CM20 bit in the CM2 register (oscillator stop/restart detect function set)
- All bits in the PLC0 register (PLL frequency synthesizer set)

To use the system clock protect function, set the CM05 bit in the CM0 register to 0 (main clock oscillation) and CM07 bit to 0 (main clock as CPU clock source), and then follow the steps below.

- (1) Set the PRC1 bit in the PRCR register to 1 (write to PM2 register enabled).
- (2) Set the PM21 bit in the PM2 register to 1 (clock change disabled).
- (3) Set the PRC1 bit in the PRCR register to 0 (write to PM2 register disabled).

When the PM21 bit is 1, do not execute the WAIT instruction.

## 8.7 Oscillator Stop/Restart Detect Function

This function detects a stop/restart of the main clock oscillator. The oscillator stop/restart detect function can be enabled and disabled with the CM20 bit in the CM2 register.

A reset or oscillator stop/restart detect interrupt is generated when an oscillator stop or restart is detected.

Set the CM27 bit in the CM2 register to select the reset or interrupt.

Table 8.6 lists Oscillator Stop/Restart Detect Function Specifications.

**Table 8.6 Oscillator Stop/Restart Detect Function Specifications**

Item	Specification
Oscillator stop detectable clock and frequency bandwidth	$f(XIN) \geq 2 \text{ MHz}$
Enabling condition for the oscillator stop/restart detect function	Set the CM20 bit to 1 (enabled)
Operation when oscillator stop/restart detected	When CM27 bit is 0: Oscillator stop detect reset generated When CM27 bit is 1: Oscillator stop/restart detect interrupt generated

### 8.7.1 Operation When CM27 Bit is 0 (Oscillator Stop Detect Reset)

When main clock stop is detected while the CM20 bit is 1 (oscillator stop/restart detect function enabled), the MCU is initialized, and then stops (oscillator stop reset). Refer to 4. "Special Function Registers (SFRs)" and 6. "Resets".

The status can be cancelled by a hardware reset or a voltage monitor 0 reset. The MCU can also be initialized and stopped when a restart is detected, but do not use the MCU in this manner. During main clock stop, do not set the CM20 bit to 1 and the CM27 bit to 0.

### 8.7.2 Operation When CM27 Bit is 1 (Oscillator Stop/Restart Detect Interrupt)

When the CM20 bit is 1 (oscillator stop/restart detect function enabled), the system is placed in the state shown in Table 8.7 if the main clock detects oscillator stop or restart.

The CM21 bit becomes 1 in high-speed, medium-speed, or low-speed mode. The FRA01 bit does not change. Thus, high-speed and medium-speed mode become 125 kHz on-chip oscillator mode or 40 MHz on-chip oscillator mode. Because the CM07 bit does not change, low-speed mode remains in low-speed mode, but fOCO-S or fOCO-F becomes the clock source for the peripheral functions.

When the CM21 bit is set to 1, the CM14 bit becomes 0 (125 kHz on-chip oscillator on), but the FRA00 bit does not change (40 MHz on-chip oscillator does not oscillate automatically). Thus, when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). Do not set the FRA00 bit to 0 while the FRA01 bit is 1, and vice versa.

Since the CM21 bit does not change in PLL operating mode, change the mode to 125 kHz on-chip oscillator mode or 40 MHz on-chip oscillator mode in the interrupt routine.

**Table 8.7 State after Oscillator Stop/Restart Detect When CM27 Bit is 1**

Condition		After Detection
Main clock oscillator stop detected	High-speed mode Medium-speed mode	<ul style="list-style-type: none"> <li>• Oscillator stop/restart detect interrupt is generated</li> <li>• CM14 bit is 0 (125 kHz on-chip oscillator on)</li> <li>• CM21 bit is 1 (fOCO-S or fOCO-F is used as the clock source for the CPU and peripheral function clocks) <sup>(1, 2)</sup></li> <li>• CM22 bit is 1 (main clock stop detected)</li> <li>• CM23 bit is 1 (main clock stopped)</li> </ul>
	Low-speed mode	
	40 MHz on-chip oscillator mode	
	125 kHz on-chip oscillator mode	
	PLL operating mode	<ul style="list-style-type: none"> <li>• Oscillator stop/restart detect interrupt is generated</li> <li>• CM14 bit is 0 (125 kHz on-chip oscillator on)</li> <li>• CM21 bit remains unchanged</li> <li>• CM22 bit is 1 (main clock stop detected)</li> <li>• CM23 bit is 1 (main clock stopped)</li> </ul>
Main clock oscillator restart detected	-	<ul style="list-style-type: none"> <li>• Oscillator stop/restart detect interrupt is generated</li> <li>• CM14 bit is 0 (125 kHz on-chip oscillator on)</li> <li>• CM21 bit does not change</li> <li>• CM22 bit is 1 (main clock stop detected)</li> <li>• CM23 bit is 0 (main clock oscillating)</li> </ul>

CM14 bit: Bit in the CM1 register

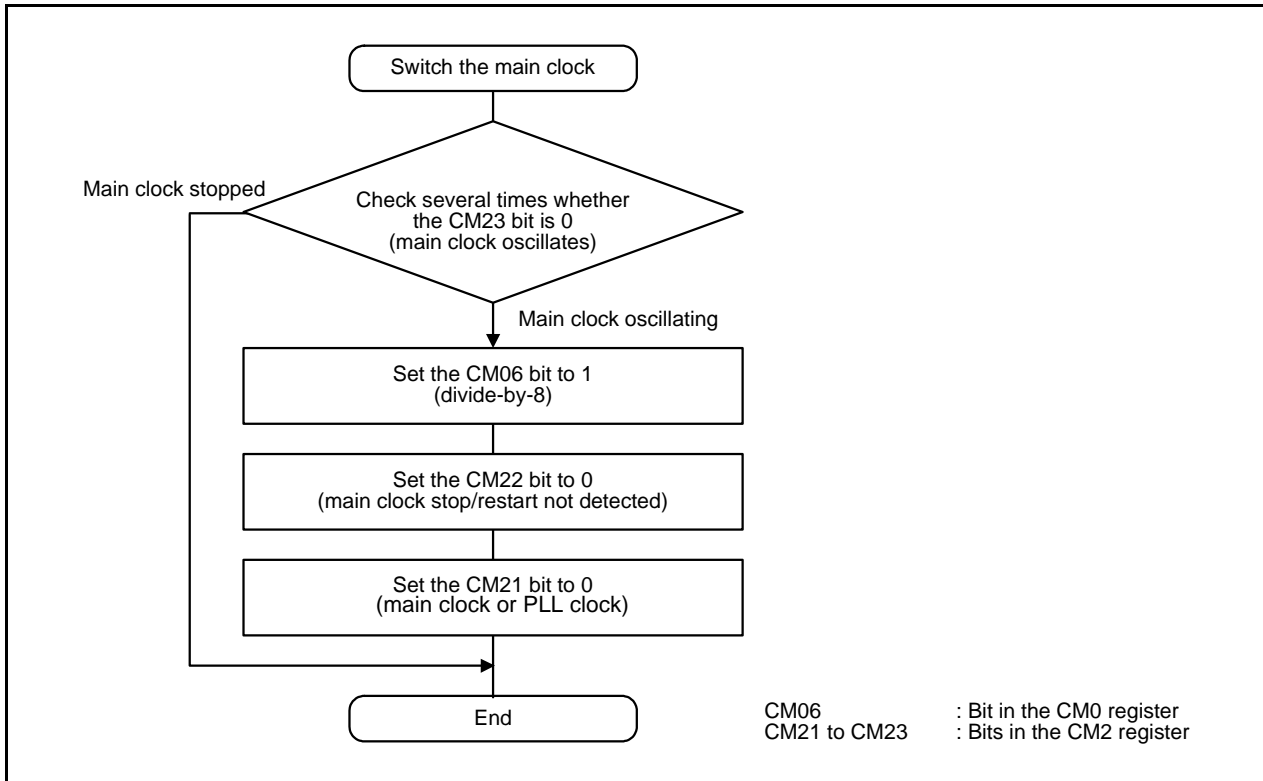
Bits CM21, CM22, CM23: Bits in the CM2 register

Notes:

1. fOCO-S or fOCO-F is selected depending on the FRA01 bit setting.
2. fC is used as the CPU clock in low-speed mode.

### 8.7.3 Using the Oscillator Stop/Restart Detect Function

After oscillator stop is detected, if the main clock reoscillates, set the main clock back to the clock source for the CPU clock and peripheral functions by a program. Figure 8.6 shows the Switching from On-Chip Oscillator Clock to Main Clock.



**Figure 8.6 Switching from On-Chip Oscillator Clock to Main Clock**

The CM22 bit becomes 1 at the same time an oscillator stop/restart detect interrupt is generated. When the CM22 bit is 1, the oscillator stop/restart detect interrupt is disabled. When setting the CM22 bit to 0 by a program, the oscillator stop/restart detect interrupt is enabled.

## 8.8 Interrupt

The oscillator stop/restart detect interrupt is a non-maskable interrupt.

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share the same vector. When using multiple interrupts together, read the detect flags of the events in the interrupt processing program, and determine the source of the interrupt.

The detect flag for oscillator stop/restart detect is the CM22 bit in the CM2 register. After the interrupt source is determined, set the CM22 bit to 0 (not detected).

## 8.9 Notes on Clock Generator

### 8.9.1 Oscillator Using a Crystal or a Ceramic Resonator

To connect a crystal/ceramic resonator follow the instructions below:

- The oscillation characteristics are tied closely to the user's board design. Perform a careful evaluation of the board before connecting an oscillator.
- Oscillator structure depends on a crystal/ceramic resonator. The M16C/5L Group, M16C/56 Group MCUs contain a feedback resistor, but an additional external feedback resistor may be required. Contact the manufacturer of crystal/ceramic resonator regarding circuit constants, as they are dependent on the a crystal/ceramic resonator or stray capacitance of the mounted circuit.
- Check output from the CLKOUT pin to confirm that the clock generated by the oscillator is properly transmitted to the MCU.

The procedure for outputting a clock from the CLKOUT pin is listed below. Set the clock output from the CLKOUT pin to 25 MHz or lower.

Outputting the main clock

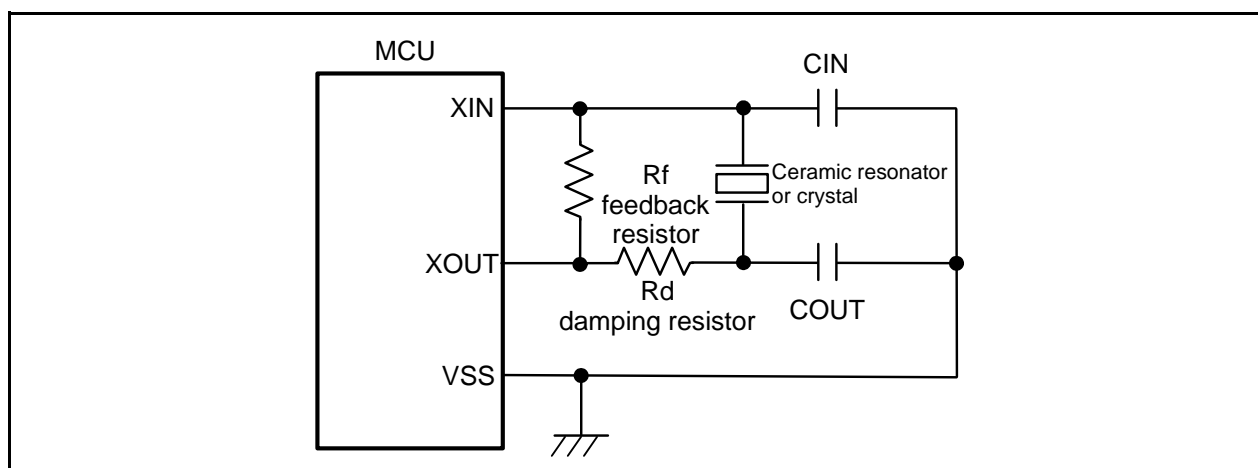
- (1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
- (2) Set the CM11 bit in the CM1 register, the CM07 bit in the CM0 register, and the CM21 bit in the CM2 register all to 0 (main clock selected).
- (3) Select the clock output from the CLKOUT pin (see the table below).
- (4) Set the PRC0 bit in the PRCR register to 0 (write disabled).

**Table 8.8 Output from CLKOUT Pin When Selecting Main Clock**

Bit Setting		Output from the CLKOUT Pin
PCLKR register	CM0 register	
PCLK5 bit	Bits CM01 to CM00	
1	00b	Clock with the same frequency as the main clock
0	10b	Main clock divided by 8
0	11b	Main clock divided by 32

Outputting the sub clock

- (1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
- (2) Set the CM07 bit in the CM0 register to 1 (sub clock selected).
- (3) Set the PCLK5 bit in the PCLKR register to 0, and bits CM01 to CM00 in the CM0 register to 01b (fC output from CLKOUT pin).
- (4) Set the PRC0 bit in the PRCR register to 0 (write disabled).



**Figure 8.7 Oscillator Example**

## 8.9.2 Noise Countermeasure

### 8.9.2.1 Clock I/O Pin Wiring

- Connect the shortest possible wiring to the clock I/O pin.
- Connect (a) the capacitor's ground lead connected to the crystal/ceramic resonator, and (b) the MCU's VSS pin, with the shortest possible wiring (maximum 20 mm).

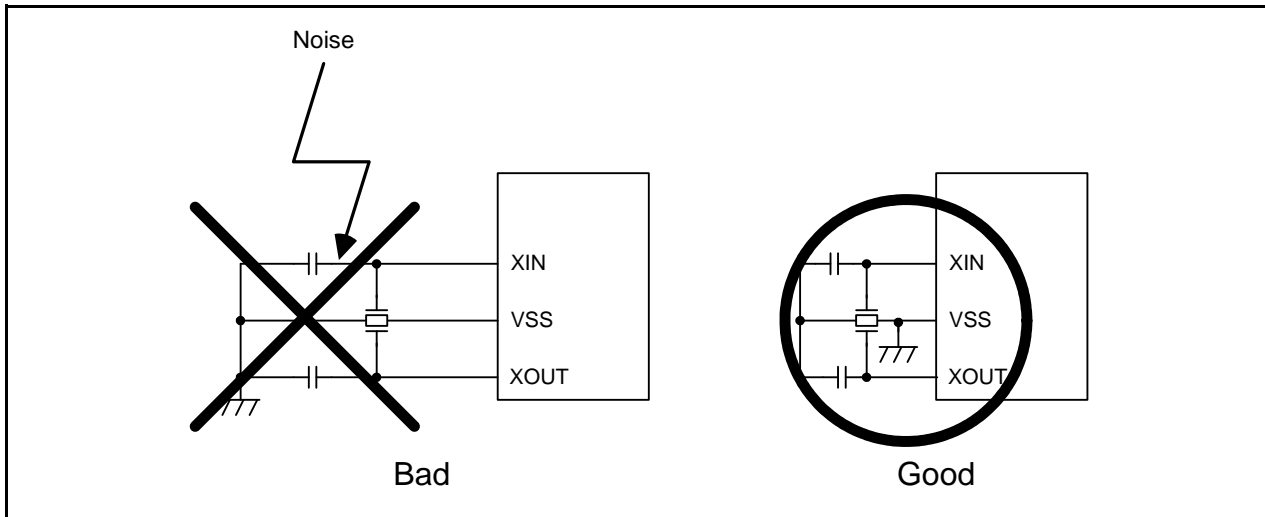


Figure 8.8 Clock I/O Pin Wiring

Reason:

When noise enters the clock I/O pin, the clock waveform becomes unstable, which causes an error in operation or a program runaway. Also, if a potential difference attributed to the noise occurs between the VSS level of the MCU and the VSS level of the crystal/ceramic resonator, an accurate clock is not input to the MCU.

### 8.9.2.2 Large Current Signal Line

For large currents that exceed the MCU's current range, wire the signal lines as far away from the MCU as possible (especially the crystal/ceramic resonator).

Reason:

In the system using the MCU, there are signal lines for controlling motors, LEDs, and thermal heads. When a large current flows through these signal lines, noise is generated due to mutual inductance.

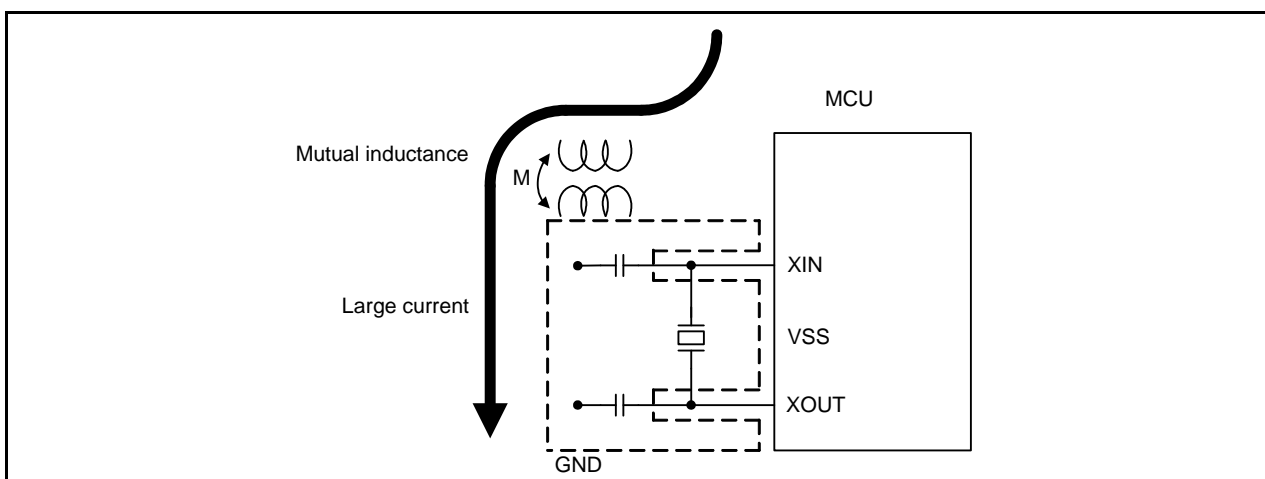


Figure 8.9 Large Current Signal Line Wiring



### 8.9.2.3 Signal Line Whose Level Changes at a High-Speed

For a signal line whose level changes at a high-speed, wire it as far away from the crystal/ceramic resonator and its wiring pattern as possible. Do not wire it across or extend it parallel to a clock-related signal line or other signal lines which are sensitive to noise.

Reason:

A signal whose level changes at a high-speed (such as the signal from the TAIOUT pin) affects other signal lines due to the level change at rising or falling edges. Specifically, when the signal line crosses the clock-related signal line, the clock waveform becomes unstable, which causes an error in operation or a program runaway.

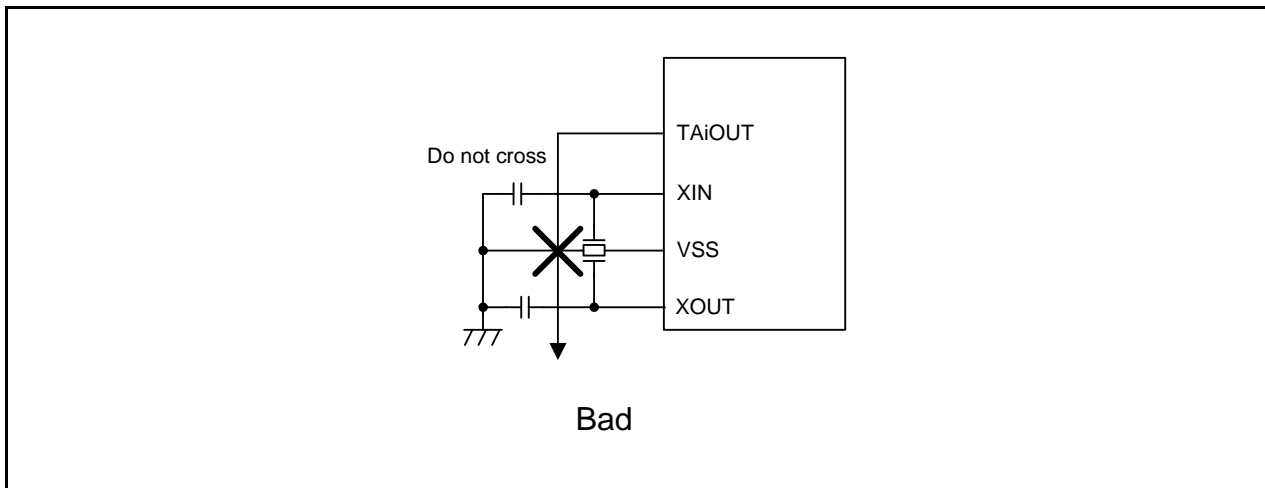


Figure 8.10 Wiring of Signal Line Whose Level Changes at High-Speed

### 8.9.3 CPU Clock

(Technical update number: TN-M16C-109-0309)

When an external clock is input from the XIN pin and the main clock is used as the CPU clock, do not stop the external clock.

### 8.9.4 Oscillator Stop/Restart Detect Function

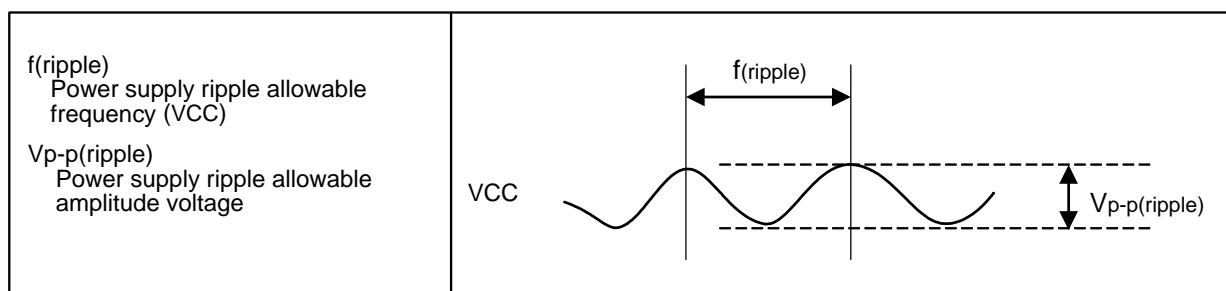
- In the following cases, set the CM20 bit to 0 (oscillator stop/restart detect function disabled), and then change the setting of each bit.
  - When the CM05 bit is set to 1 (main clock stopped)
  - When the CM10 bit is set to 1 (stop mode)
- To enter wait mode while using the oscillator stop/restart detect function, set the CM02 bit to 0 (peripheral function clock f1 not turned off during wait mode).
- This function cannot be used if the main clock frequency is 2 MHz or lower. In that case, set the CM20 bit to 0 (oscillator stop/restart detect function disabled).
- While the CM27 bit is 1 (oscillation stop/restart detect interrupt), when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). (Do not set the FRA00 bit to 0 while FRA01 bit is 1, and vice versa.)

### 8.9.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage within the acceptable range of power supply ripple.

**Table 8.9 Acceptable Range of Power Supply Ripple**

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
f(ripple)	Power supply ripple allowable frequency (VCC)			10	kHz
VP-P(ripple)	Power supply ripple allowable amplitude voltage	(VCC = 5 V)		0.5	V
		(VCC = 3 V)		0.3	V
VCC( ΔV / ΔT )	Power supply ripple rising/falling gradient	(VCC = 5 V)		0.3	V/ms
		(VCC = 3 V)		0.3	V/ms



**Figure 8.11 Voltage Fluctuation Timing**

## 9. Power Control

### 9.1 Introduction

This chapter describes how to reduce the amount of current consumption.

### 9.2 Registers

Refer to 8. "Clock Generator" for clock-related registers.

**Table 9.1** Registers

Address	Register	Symbol	Reset Value
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b

### 9.2.1 Flash Memory Control Register 0 (FMR0)

Flash Memory Control Register 0			
Bit	Symbol	Address	Reset Value
b7			
b6			
b5			
b4			
b3			
b2			
b1			
b0			
FMR0			
Symbol		Address	Reset Value
FMR0		0220h	0000 0001b (other than user boot mode) 0010 0001b (user boot mode)
Bit Symbol	Bit Name	Function	RW
FMR00	RY/ $\overline{\text{BY}}$ status flag	0 : Busy (being written or erased) 1 : Ready	RO
FMR01	CPU rewrite mode select bit	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Lock bit disable select bit	0 : Lock bit enabled 1 : Lock bit disabled	RW
FMSTP	Flash memory stop bit	0 : Flash memory operation enabled 1 : Flash memory operation stopped (low power-mode, flash memory initialized)	RW
— (b4)	Reserved bit	Set to 0	RW
— (b5)	Reserved bit	Set to 0 in other than user boot mode Set to 1 in user boot mode	RW
FMR06	Program status flag	0 : Completed as expected 1 : Completed in error	RO
FMR07	Erase status flag	0 : Completed as expected 1 : Completed in error	RO

#### FMR01 (CPU rewrite mode select bit) (b1)

Commands can be accepted by setting the FMR01 bit to 1 (CPU rewrite mode enabled).

To set the FMR01 bit to 1, write 0 and then 1 in succession. Do not generate any interrupts or DMA transfers between setting 0 and 1.

Change the FMR01 bit when the PM24 bit in the PM2 register is 0 ( $\overline{\text{NMI}}$  interrupt disabled) or high is input to the  $\overline{\text{NMI}}$  pin.

While in EW0 mode, write to this bit from a program in RAM.

Enter read array mode, and then set this bit to 0.

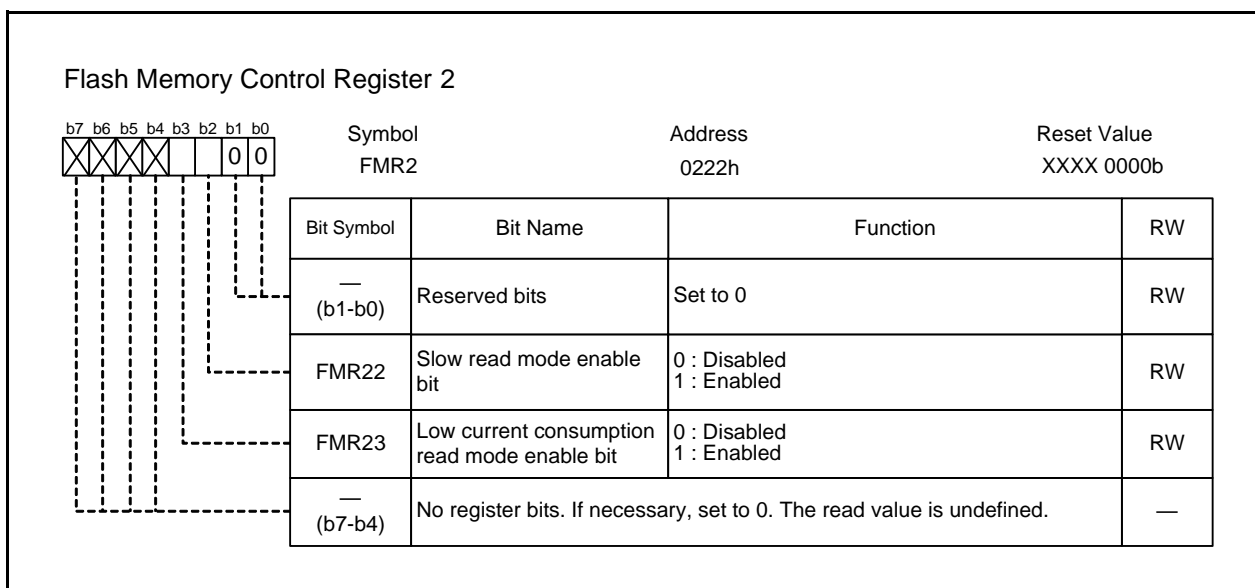
#### FMSTP (Flash memory stop bit) (b3)

The FMSTP bit resets the flash memory control circuits and minimizes current consumption in the flash memory. Access to the internal flash memory is disabled when the FMSTP bit is set to 1 (flash memory operation stopped). Set the FMSTP bit by a program located in RAM.

Set the FMSTP bit to 1 under the following condition:

- A flash memory access error occurs while erasing or programming in EW0 mode (the FMR00 bit does not revert to 1 (ready)).

## 9.2.2 Flash Memory Control Register 2 (FMR2)



### FMR22 (Slow read mode enable bit) (b2)

This bit enables the mode which reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR22 bit to 0 (slow read mode disabled).

To set the FMR22 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur between writing 0 and 1.

Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (low current consumption read mode disabled). Do not change the FMR22 bit and FMR23 bit at the same time.

### FMR23 (Low current consumption read mode enable bit) (b3)

This bit enables the mode which reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR23 bit to 0 (low current consumption read mode disabled).

Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock).

To set the FMR23 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur between writing 0 and 1.

Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (low current consumption read mode disabled). Do not change bits FMR22 and FMR23 at the same time.

Do not set the FMR23 bit to 1 (low current consumption read mode enabled) when any of the following occurs:

- When the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).
- When the FMR22 bit is 0 (slow read mode disabled)
- When the FMSTP bit is 1 (flash memory stopped)
- During the wake up operation when the FMSTP bit is changed from 1 to 0 (tps)

Do not perform the operations below when the FMR23 bit is 1. Set the FMR23 to 0 before performing them.

- Change the CPU clock
- Set to the FMSTP bit to 1 (flash memory stopped)
- Enter the wait mode or stop mode
- Execute the following commands:  
Program, block erase, lock bit program, read lock bit status, and block blank check

## 9.3 Clock

The amount of current consumption correlates with the number of operating clocks and frequency. When there are fewer operating clocks and a lower frequency, current consumption will be low.

Normal operating mode, wait mode, and stop mode can be used to control power consumption. All mode states, except wait mode and stop mode, are referred to as normal operating mode in this document.

### 9.3.1 Normal Operating Mode

In normal operating mode, because both the CPU clock and the peripheral function clocks are supplied, the CPU and the peripheral functions are operating. Power control is exercised by controlling the CPU clock frequency. The higher the CPU clock frequency, the higher the processing capability. The lower the CPU clock frequency, the lower the power consumption in the chip. If unnecessary oscillator are stopped, power consumption is further reduced.

#### 9.3.1.1 High-Speed Mode and Medium-Speed Mode

In high-speed mode, the main clock divided by 1 (no division) is used as the CPU clock.

In medium-speed mode, the main clock divided by 2, 4, 8 or 16 is used as the CPU clock.

f1 with the same frequency of the main clock divided by 1 is used as the peripheral function clocks in both high-speed and medium-speed modes. When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

#### 9.3.1.2 PLL Operating Mode

The PLL clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the PLL clock divided by 1 (no division) is used as the peripheral function clocks.

When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

PLL operating mode can be entered and exited from high-speed mode or medium-speed mode. To enter other modes including wait mode and stop mode, enter high-speed mode or medium-speed mode first, and then enter the intended mode. Refer to Figure 9.1 "Clock Mode Transition" for details.

#### 9.3.1.3 40 MHz On-Chip Oscillator Mode

The fOCO-F clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-F clock divided by 1 is used as the peripheral function clocks.

When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. fOCO40M and fOCO-F can be used as the peripheral function clocks.

### 9.3.1.4 125 kHz On-Chip Oscillator Mode

The fOCO-S clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.

When fC is supplied, fC and fC32 can be used as the peripheral function clocks. fOCO-S can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

### 9.3.1.5 125 kHz On-Chip Oscillator Low Power Mode

The main clock and fOCO-F are turned off after the MCU enters 125 kHz on-chip oscillator mode. The fOCO-S clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.

When fC is supplied, fC and fC32 can be used as the peripheral function clocks. fOCO-S can be used as the peripheral function clocks.

### 9.3.1.6 Low-Speed Mode

fC is used as the CPU clock.

When the CM21 bit is 0 and the CM11 bit is 0 (main clock), f1 with the same frequency of the main clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 0 and the CM11 bit is 1 (PLL clock), f1 with the same frequency of the PLL clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 0 (125 kHz on-chip oscillator), f1 with the same frequency as the fOCO-S clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 1 (40 MHz on-chip oscillator), f1 with the same frequency as the fOCO-F clock divided by 1 is used as the peripheral function clocks.

fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

### 9.3.1.7 Low Power Mode

The main clock and fOCO-F are stopped after the MCU enters low-speed mode. fC is used as the CPU clock. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 0 (125 kHz on-chip oscillator clock), f1 with the same frequency as the fOCO-S clock divided by 1 is used as the peripheral function clocks.

fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks.



**Table 9.2 Clocks in Normal Operating Mode**

Mode	CPU Clock	Peripheral Clocks <sup>(2)</sup>			
		f1	fC, fC32	fOCO-S	fOCO-F fOCO40M
High-speed mode	Main clock divided by 1 <sup>(1)</sup>	Main clock divided by 1	Enabled	Enabled	Enabled
Medium-speed mode	Main clock divided by n <sup>(1)</sup>				
PLL operating mode	PLL clock divided by n <sup>(1)</sup>	PLL clock divided by 1			
40 MHz on-chip oscillator mode	fOCO-F divided by n <sup>(1)</sup>	fOCO-F divided by 1	Enabled	Enabled	Enabled
125 kHz on-chip oscillator mode	fOCO-S divided by n <sup>(1)</sup>	fOCO-S divided by 1	Enabled	Enabled	Enabled
125 kHz on-chip oscillator low power mode	fOCO-S divided by n <sup>(1)</sup>	fOCO-S divided by 1	Enabled	Enabled	Disabled
Low-speed mode	fC	Any of the following: Main clock divided by 1 (when the CM21 is 0 and the CM11 is 0) PLL clock divided by 1 (when the CM21 is 0 and the CM11 is 1) fOCO-F divided by 1 (when the CM21 is 1 and the FRA01 is 1) fOCO-S divided by 1 (when the CM21 is 1 and the FRA01 is 0)	Enabled	Enabled	Enabled
Low power mode	fC	fOCO-S divided by 1 (when the CM21 is 1 and the FRA01 is 0)	Enabled	Enabled	Disabled

CM11 : Bit in the CM1 register

CM21 : Bit in the CM2 register

FRA01 : Bit in the FRA0 register

**Notes:**

1. Select by setting the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register.
2. The peripheral clock is enabled when each clock is supplied. Refer to 8. "Clock Generator" for the clock supply method.

**Table 9.3 Clock-Related Bit Setting and Modes**

Mode	CM2 Register	CM1 Register		CM0 Register			FRA0 Register	
	CM21	CM14	CM11	CM07	CM05	CM04	FRA01	FRA00
High-speed mode, medium-speed mode	0	–	0	0	0	–	–	–
PLL operating mode	0	–	1	0	0	–	–	–
40 MHz on-chip oscillator mode	1	–	0	0	–	–	1	1
125 kHz on-chip oscillator mode	1	0	0	0	0 <sup>(1)</sup>	–	0	1 <sup>(1)</sup>
125 kHz on-chip oscillator low power mode	1	0	0	0	1	–	0	0
Low-speed mode	–	–	0	1	0 <sup>(1)</sup>	1	–	1 <sup>(1)</sup>
Low power mode	–	–	0	1	1	1	–	0

–: 0 or 1

**Note:**

1. Both or either the main clock and fOCO-F are oscillated.

**Table 9.4 Selecting Clock Division Related Bits <sup>(1)</sup>**

Division	CM1 Register	CM0 Register
	Bits CM17 to CM16	CM06 bit
No division <sup>(2)</sup>	00b	0
Divide-by-2	01b	0
Divide-by-4	10b	0
Divide-by-8	–	1
Divide-by-16	11b	0

–: Any value from 00b to 11b

## Notes:

1. While in high-speed mode, medium-speed mode, PLL operating mode, 125 kHz on-chip oscillator mode, or 125 kHz on-chip oscillator low power mode.
2. Select divide-by-1 (no division) in high-speed mode.

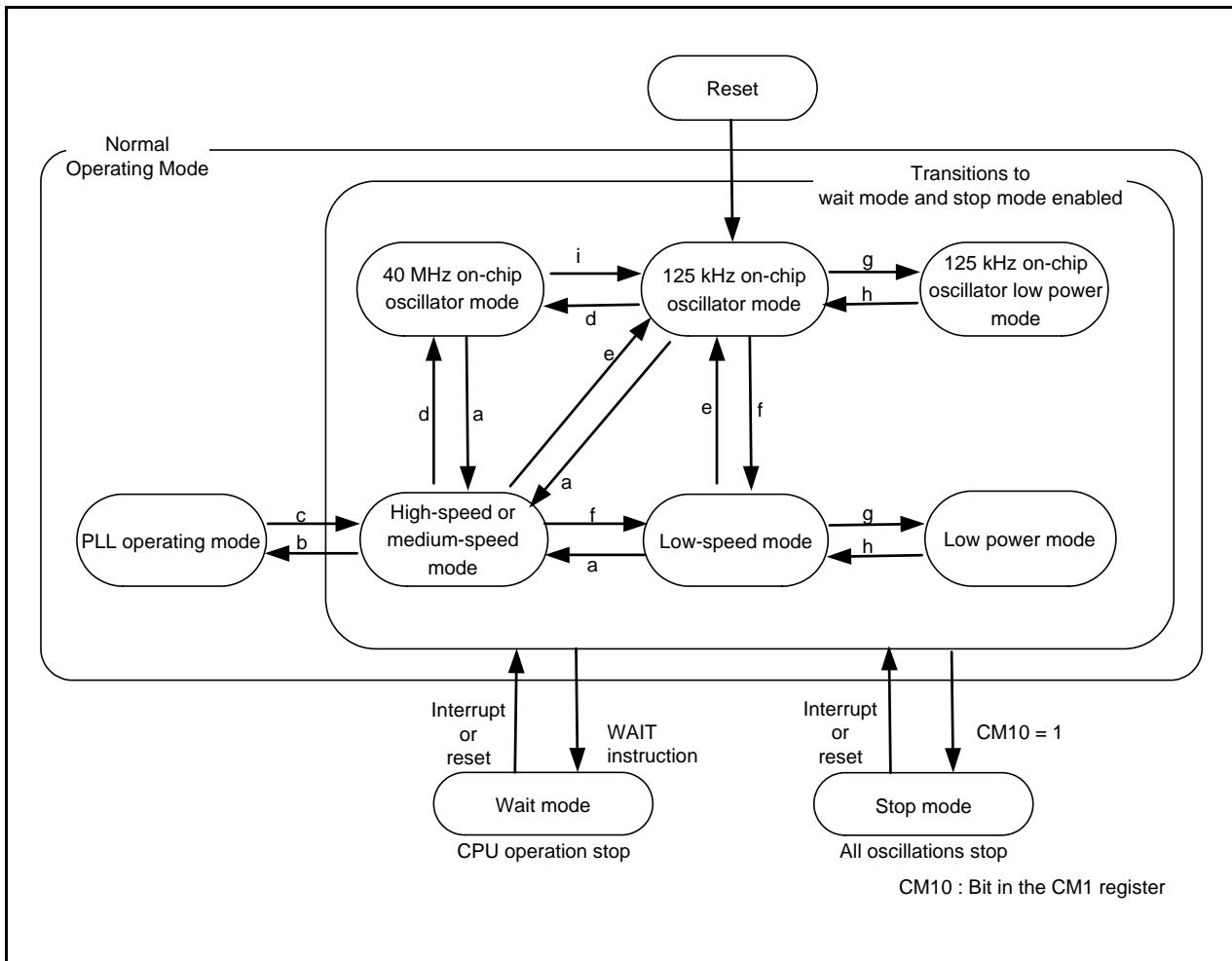
**Table 9.5 Example Settings for 40 MHz On-Chip Oscillator Mode Division Related Bits**

Division	CPU Clock Frequency	FRA2 Register	CM1 Register	CM0 Register
		Bits FRA22 to FRA20	Bits CM17 to CM16	CM06 bit
Divide-by-2	Approx. 20 MHz	000b (divide-by-2)	00b (no division)	0
Divide-by-4	Approx. 10 MHz	000b (divide-by-2)	01b (divide-by-2)	0
Divide-by-8	Approx. 5 MHz	000b (divide-by-2)	10b (divide-by-4)	0
Divide-by-16	Approx. 2.5 MHz	000b (divide-by-2)	–	1 (divide-by-8)
Divide-by-32	Approx. 1.25 MHz	000b (divide-by-2)	11b (divide-by-16)	0
Divide-by-64	Approx. 625 kHz	010b (divide-by-4)	11b (divide-by-16)	0
Divide-by-128	Approx. 312.5 kHz	110b (divide-by-8)	11b (divide-by-16)	0

–: Any value from 00b to 11b

### 9.3.2 Clock Mode Transition Procedure

Figure 9.1 shows Clock Mode Transition. Arrows indicate possible mode transitions.



**Figure 9.1** Clock Mode Transition

To start or stop clock oscillations, or to change modes in normal operating mode, follow the instructions below.

- Enter a different mode after the clock for that mode stabilizes completely.
- When stopping a clock, do it after mode transition is completed. Do not stop the clock at the same time as mode transition.
- To change the mode, follow procedures listed below. For details on register and bit access, refer to 9.2 “Registers”. Letters a to i correspond to those in Figure 9.1 “Clock Mode Transition”.
- For details on oscillator start and stop, refer to 8.3.1 “Main Clock” to 8.3.6 “Sub Clock (fC)”.

- a. Entering high-speed mode or medium-speed mode from 40 MHz on-chip oscillator mode, 125 kHz on-chip oscillator mode or low-speed mode
  - (1) Start the main clock and wait until the oscillation stabilizes. Refer to 8.3.1 “Main Clock” for details.
  - (2) Set the CM06 bit to 1 (divide-by-8 mode).
  - (3) Set the CM11 bit to 0, the CM21 bit to 0 and the CM07 bit to 0 (main clock selected as CPU clock source).
- b. Entering PLL operating mode from high-speed mode or medium-speed mode
  - (1) Select the division of reference frequency counter by setting bits PLC05 and PLC04 in the PLC0 register, and the multiplication rate by setting bits PLC02 to PLC00 in the PLC0 register.
  - (2) Set the PLC07 bit to 1 (PLL on).
  - (3) Wait for  $t_{su}(PLL)$  until the PLL clock stabilizes.
  - (4) Set the CM11 bit to 1, the CM21 bit to 0, and the CM07 bit to 0 (PLL clock selected as CPU clock source).
- c. Entering high-speed mode or medium-speed mode from PLL operating mode
  - (1) Select the main clock divide ratio by the CM06 bit and bits CM17 to CM16.
  - (2) Set the CM11 bit to 0, the CM21 bit to 0, and the CM07 bit to 0 (main clock selected as CPU clock source).
  - (3) Set the PLC07 bit to 0 (PLL off).
- d. Entering 40 MHz on-chip oscillator mode from high-speed mode, medium-speed mode, or 125 kHz on-chip oscillator mode
  - (1) Start the 40 MHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.4 “fOCO-F” for details.
  - (2) Set the CM06 bit to 1 (divide-by-8 mode)
  - (3) Set the FRA01 bit to 1 (40 MHz on-chip oscillator).
  - (4) Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).
- e. Entering 125 kHz on-chip oscillator mode from high-speed mode, medium-speed mode, or low-speed mode
  - (1) Start the 125 kHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.5 “125 kHz On-Chip Oscillator Clock (fOCO-S)” for details.
  - (2) Set the FRA01 bit to 0 (125 kHz on-chip oscillator).
  - (3) Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).
  - (4) Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).
- f. Entering low-speed mode from high-speed mode, medium-speed mode, or 125 kHz on-chip oscillator mode
  - (1) Start the sub clock and wait until the oscillation stabilizes. Refer to 8.3.6 “Sub Clock (fC)” for details.
  - (2) Set the CM07 bit to 1 (sub clock selected as CPU clock source).
- g. Entering 125 kHz on-chip oscillator low power mode from 125 kHz on-chip oscillator mode  
Entering low power mode from low-speed mode  
Follow both or either of the procedures below (in no particular order).
  - (1) Stop the main clock. Refer to 8.3.1 “Main Clock” for details.
  - (2) Stop the 40 MHz on-chip oscillator. Refer to 8.3.4 “fOCO-F” for details for details.

- h. Entering 125 kHz on-chip oscillator mode from 125 kHz on-chip oscillator low power mode  
Entering low-speed mode from low power mode  
Follow both or either of the procedures below (in no particular order).
  - (1) Start the main clock and wait until the oscillation stabilizes. Refer to 8.3.1 “Main Clock” for details.
  - (2) Start the 40 MHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.4 “fOCO-F” for details.
  
- i. Entering 125 kHz on-chip oscillator mode from 40 MHz on-chip oscillator mode
  - (1) Start the 125 kHz on-chip oscillator and wait until the oscillation stabilizes. Refer to 8.3.5 “125 kHz On-Chip Oscillator Clock (fOCO-S)” for details.
  - (2) Set the CM06 bit to 1 (divide-by-8 mode) or the bits FRA22 to FRA20 to 110b (divide-by-8 mode).
  - (3) Set the FRA01 bit to 0 (125 kHz on-chip oscillator).

### 9.3.3 Wait Mode

The CPU clock stops in wait mode, therefore, the CPU and the watchdog timer clocked by the CPU clock stops running. However, if the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the watchdog timer remains active. Because the clock generator does not stop, peripheral functions supplied by a peripheral clock keep operating.

#### 9.3.3.1 Peripheral Function Clock Stop Function

When the CM02 bit is 1 (peripheral function clock f1 stops in wait mode), the f1 clock is turned off while in wait mode, and power consumption is reduced. However, all the peripheral clocks except f1 (i.e. fOCO40M, fOCO-F, fOCO-S, fC, and fC32) do not stop.

#### 9.3.3.2 Entering Wait Mode

The MCU enters wait mode by executing a WAIT instruction.

When the CM11 bit is 1 (PLL clock selected as CPU clock source), set the CM11 bit to 0 (main clock selected as CPU clock source) before entering wait mode. Chip power consumption can be reduced by setting the PLC07 bit to 0 (PLL off).

When using wait mode, set the following:

- (1) Set the I flag to 0.
- (2) Set the interrupt priority level of bits ILVL2 to ILVL0 in the interrupt control register for the peripheral function interrupt which is used to exit wait mode. Start the peripheral function which is used to exit wait mode if it is stopped.
- (3) Set 000b (interrupt disabled) to bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupts not used to exit wait mode.  
(When using any of the following resets or interrupts to exit wait mode, set 000b to bits ILVL2 to ILVL0 in all interrupt control registers for peripheral function interrupts: hardware reset, voltage monitor 0 reset, voltage monitor 2 reset, watchdog timer reset,  $\overline{\text{NMI}}$  interrupt, or voltage monitor 2 interrupt).
- (4) Set the I flag to 1.
- (5) Execute the WAIT instruction.

#### 9.3.3.3 Pin Status in Wait Mode

Table 9.6 lists Pin Status in Wait Mode.

**Table 9.6 Pin Status in Wait Mode**

Pin		Pin State
I/O ports		Maintains the pin state immediately before entering wait mode
CLKOUT	When fC is selected	Continues to output the clock
	When f1, f8, f32 are selected	<ul style="list-style-type: none"> <li>• When the CM02 bit is 0 (peripheral clock, f1, does not stop in wait mode): Continues to output the clock</li> <li>• When the CM02 bit is 1 (peripheral clock, f1, stops in wait mode): Maintains the pin state immediately before entering wait mode</li> </ul>

### 9.3.3.4 Exiting Wait Mode

The MCU exits wait mode by a reset or interrupt. Table 9.7 lists Resets and Interrupts to Exit Wait Mode and Conditions for Use.

The peripheral function interrupts are affected by the CM02 bit in the CM0 register. When the CM02 bit is 0 (peripheral function clock f1 does not stop in wait mode), peripheral function interrupts can be used to exit wait mode. When the CM02 bit is 1 (peripheral function clock f1 stops in wait mode), the peripheral functions using the peripheral function clock f1 stop operating, so the peripheral functions activated by external signals and the peripheral function clocks except f1 (fOCO40M, fOCO-F, fOCO-S, fC, fC32) can be used to exit wait mode.

**Table 9.7 Resets and Interrupts to Exit Wait Mode and Conditions for Use**

Interrupt, Reset		Conditions for Use		
		CM02 = 0	CM02 = 1	
Interrupt	Peripheral function interrupt	INT	Usable	Usable (INT5 is usable when the digital debounce filter is disabled (P17DDR register is FFh))
		Key input	Usable	Usable
		Timer A, timer B	Usable in all modes	Usable when fOCO-F, fOCO-S or fC32 is supplied and is used as count source. Usable when counting external signals in event counter mode.
		Timer S	Usable in all modes except the following: not usable in IC/OC interrupt 0 and 1	Not usable
		Serial interface	Usable in internal clock or external clock	Usable in external clock The internal clock can be used when fOCO-F is supplied and the internal clock is operated by fOCO-F
		Multi-master I <sup>2</sup> C-bus interface	Usable	SCL/SDA interrupt is usable
		CAN0 wake-up	Usable in CAN sleep mode	Usable in CAN sleep mode
		A/D converter	Usable in one-shot mode or single sweep mode.	Usable when fOCO40M is supplied and is used as fAD in one-shot mode or single sweep mode.
		Real-time clock	Usable when fC is supplied and is used as count source	
		Voltage monitor 2	Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1). Usable when the digital filter is enabled (VW2C1 bit in the VW2C register is 0) and fOCO-S is supplied (CM14 bit in the CM1 register is 0).	
	NMI	Usable	Usable when the digital debounce filter is disabled (NDDR register is FFh)	
Reset	Hardware reset	Usable		
	Voltage monitor 0 reset	Usable		
	Voltage monitor 2 reset	Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1). Usable when the digital filter is enabled (VW2C1 bit in the VW2C register is 0) and fOCO-S is supplied (CM14 bit in the CM1 register is 0).		
	Watchdog timer	Usable when count source protection mode is enabled (the CSPRO bit in the CSPR register is 1).		

When the MCU exits wait mode by using an interrupt, an interrupt request is generated, the CPU clock starts running, and interrupt routine is performed.

When the MCU exits wait mode by an interrupt, the CPU clock is the same CPU clock used while executing the WAIT instruction.

### 9.3.4 Stop Mode

In stop mode, all oscillator are stopped, so the CPU clock and peripheral function clocks are also stopped. Therefore, the CPU and the peripheral functions using these clocks stop operating. The least amount of power is consumed in this mode. If the voltage applied to pin VCC is VRAM or greater, the contents of internal RAM are retained. When applying 3.0 V or less to pin VCC, make sure  $VCC \geq VRAM$ .

However, the peripheral functions activated by external signals keep operating.

#### 9.3.4.1 Entering Stop Mode

The MCU enters stop mode by setting the CM10 bit in the CM1 register to 1 (all clocks turned off). At the same time, the CM06 bit in the CM0 register becomes 1 (divide-by-8 mode), and the CM15 bit in the CM1 register becomes 1 (main clock oscillator drive capability high).

Before entering stop mode, set the CM20 bit to 0 (oscillator stop/restart detect function disabled).

When the CM11 bit is 1 (PLL clock used as the CPU clock source), set the CM11 bit to 0 (main clock used as the CPU clock source), and then the PLC07 bit to 0 (PLL turned off) before entering stop mode.

When using stop mode, set the following:

- (1) Set the I flag to 0.
- (2) Set the interrupt priority level of bits ILVL2 to ILVL0 in the interrupt control register for the peripheral function interrupt which is used to exit stop mode. Start the peripheral function which is used to stop mode if it is stopped.
- (3) Set 000b (interrupt disabled) to bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupts not used to exit stop mode.  
(When using any of the following resets or interrupts to exit stop mode, set 000b to bits ILVL2 to ILVL0 in all interrupt control registers for peripheral function interrupts: hardware reset, voltage monitor 0 reset,  $\overline{NMI}$  interrupt, or voltage monitor 2 interrupt)
- (4) Set the I flag to 1.
- (5) Set the CM10 bit in the CM1 register to 1.

When using the  $\overline{NMI}$  interrupt to exit stop mode, set the NDDR register to FFh before setting the CM10 bit to 1. When using the  $\overline{INT5}$  interrupt to exit stop mode, set the P17DDR register to FFh before setting the CM10 bit to 1.

#### 9.3.4.2 Pin Status in Stop Mode

Table 9.8 lists Pin Status in Stop Mode.

**Table 9.8 Pin Status in Stop Mode**

Pin	Pin State
I/O ports	Maintains the pin state immediately before entering stop mode
CLKOUT	High
XOUT	High
XCIN, XCOUT	High-impedance



### 9.3.4.3 Exiting Stop Mode

Use a reset or an interrupt to exit stop mode. Table 9.9 lists Resets and Interrupts to Exit Stop Mode and Conditions for Use.

**Table 9.9 Resets and Interrupts to Exit Stop Mode and Conditions for Use**

Interrupt, Reset		Conditions for Use	
Interrupt	Peripheral function interrupt	$\overline{\text{INT}}$	Usable ( $\overline{\text{INT5}}$ is usable when the digital debounce filter is disabled (P17DDR register is FFh))
		Key input	Usable
		Timer A, timer B	Usable when counting external signals in event counter mode
		Serial interface	Usable when an external clock is selected
		Multi-master I <sup>2</sup> C-bus interface	SCL/SDA interrupt is usable
		CAN0 wake-up	Usable in CAN sleep mode
	Voltage monitor 2 interrupt	Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1)	
	$\overline{\text{NMI}}$	Usable when the digital debounce filter is disabled (NDDR register is FFh)	
Reset	Hardware reset	Usable	
	Voltage monitor 0 reset	Usable	

To exit stop mode by using hardware reset, voltage monitor 0 reset,  $\overline{\text{NMI}}$  interrupt, or voltage monitor 2 interrupt, set bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupt to 000b (interrupt disabled) before setting the CM10 bit to 1.

When the MCU exits stop mode by using an interrupt, an interrupt request is generated, the CPU clock starts running, and interrupt routine is performed.

When exiting stop mode by means of an interrupt, the CPU clock source varies depending on the CPU clock source setting before the MCU had entered stop mode. Table 9.10 lists CPU Clock After Exiting Stop Mode.

**Table 9.10 CPU Clock After Exiting Stop Mode**

CPU Clock Before Entering Stop Mode	CPU Clock After Exiting Stop Mode
Main clock divided by 1 (no division), 2, 4, 8 or 16	Main clock divided by 8
fOCO-S divided by 1 (no division), 2, 4, 8 or 16	fOCO-S divided by 8
fOCO-F divided by 1 (no division), 2, 4, 8 or 16	fOCO-F divided by 8
fC	fC

## 9.4 Power Control in Flash Memory

### 9.4.1 Stopping Flash Memory

When the flash memory is stopped, current consumption is reduced. Execute a program in the RAM. Figure 9.2 shows the setting procedure to stop and restart the flash memory. Follow the flowchart of Figure 9.2.

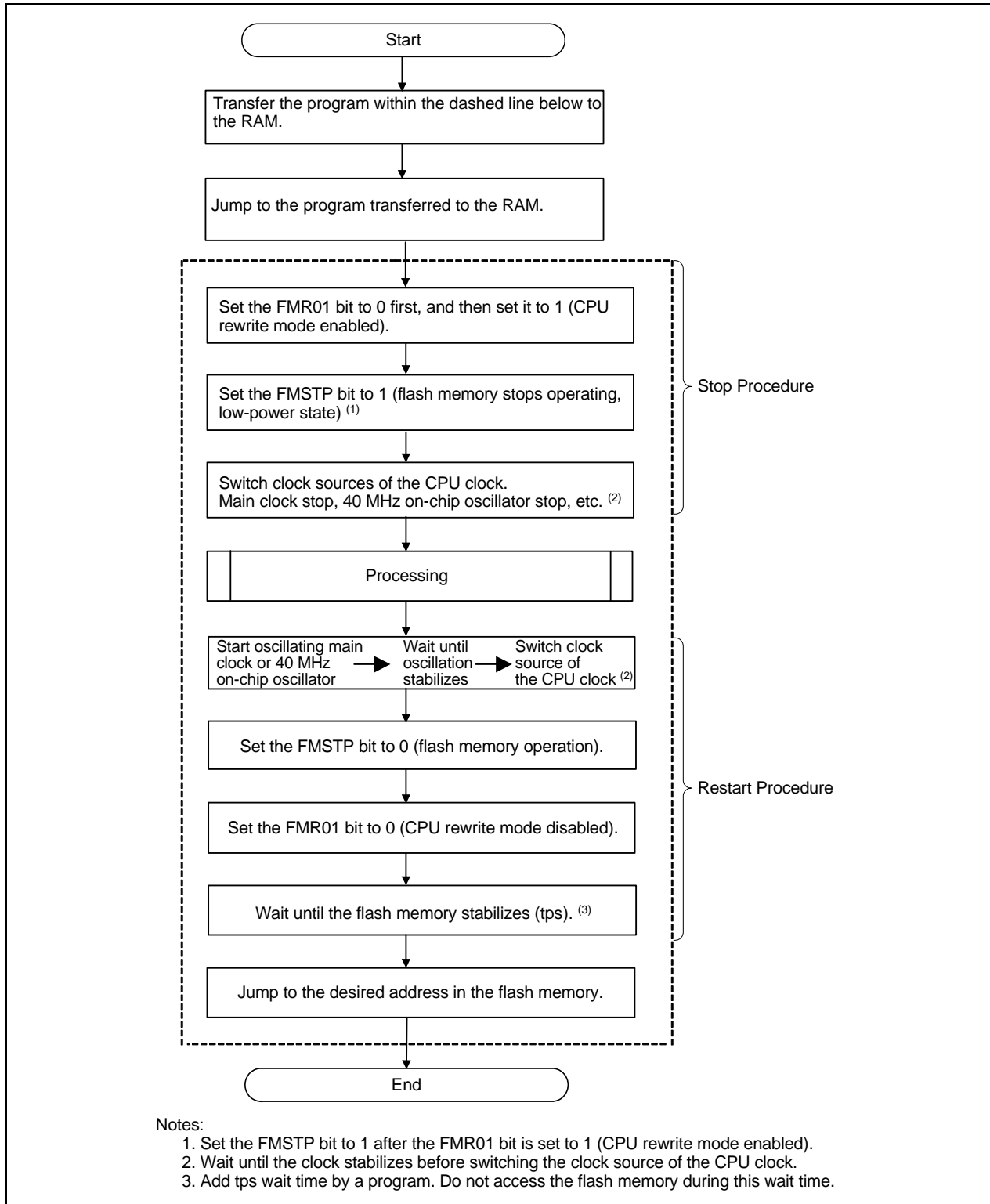


Figure 9.2 Stop and Restart of the Flash Memory

### 9.4.2 Reading Flash Memory

Current consumption while reading the flash memory can be reduced by using bits FMR22 and FMR23 in the FMR2 register.

#### 9.4.2.1 Slow Read Mode

Slow read mode can be used when  $f(\text{BCLK})$  is less than or equal to  $f(\text{SLOW\_R})$  and the PM17 bit in the PM1 register is 1 (one wait). Figure 9.3 shows Setting and Canceling Slow Read Mode.

When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is unnecessary (technical update number: TN-16C-A179A/E).

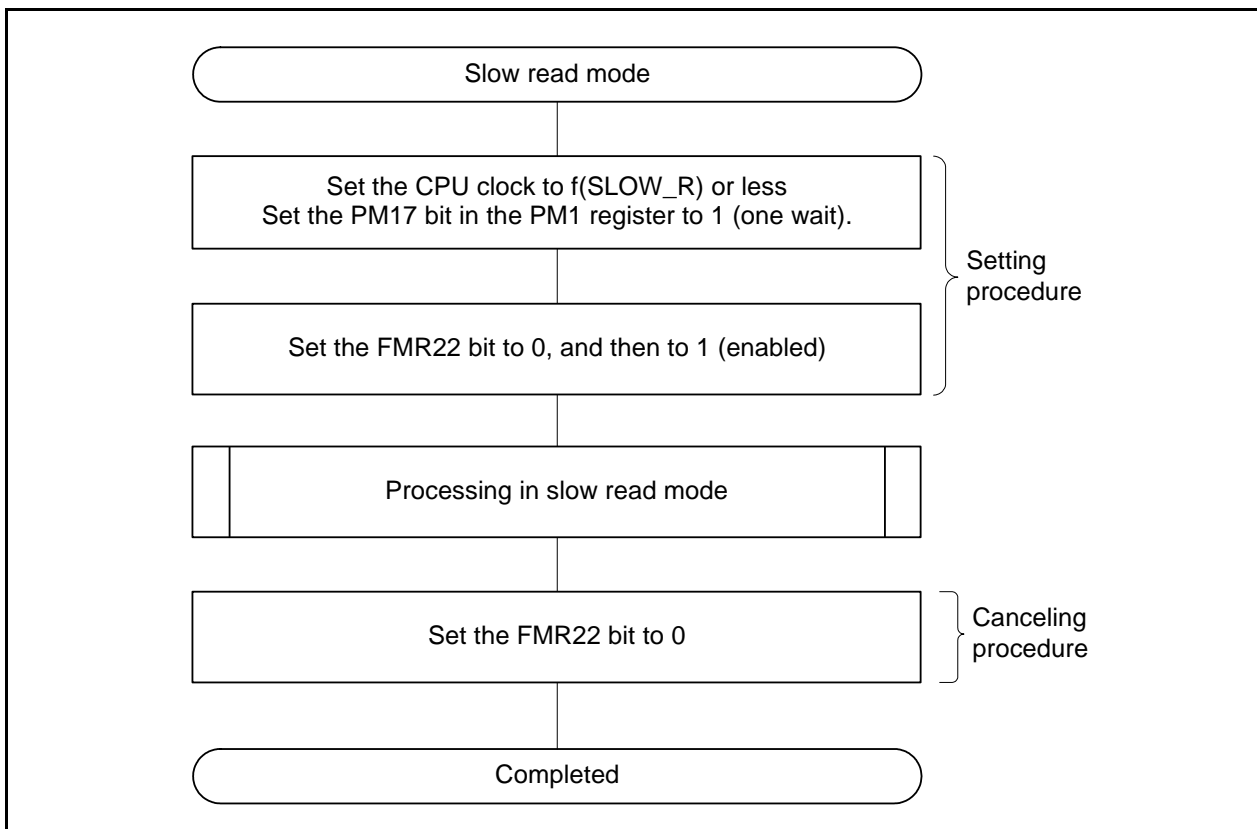


Figure 9.3 Setting and Canceling Slow Read Mode

### 9.4.2.2 Low Current Consumption Read Mode

Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock). Figure 9.4 shows Setting and Canceling Low Current Consumption Read Mode.

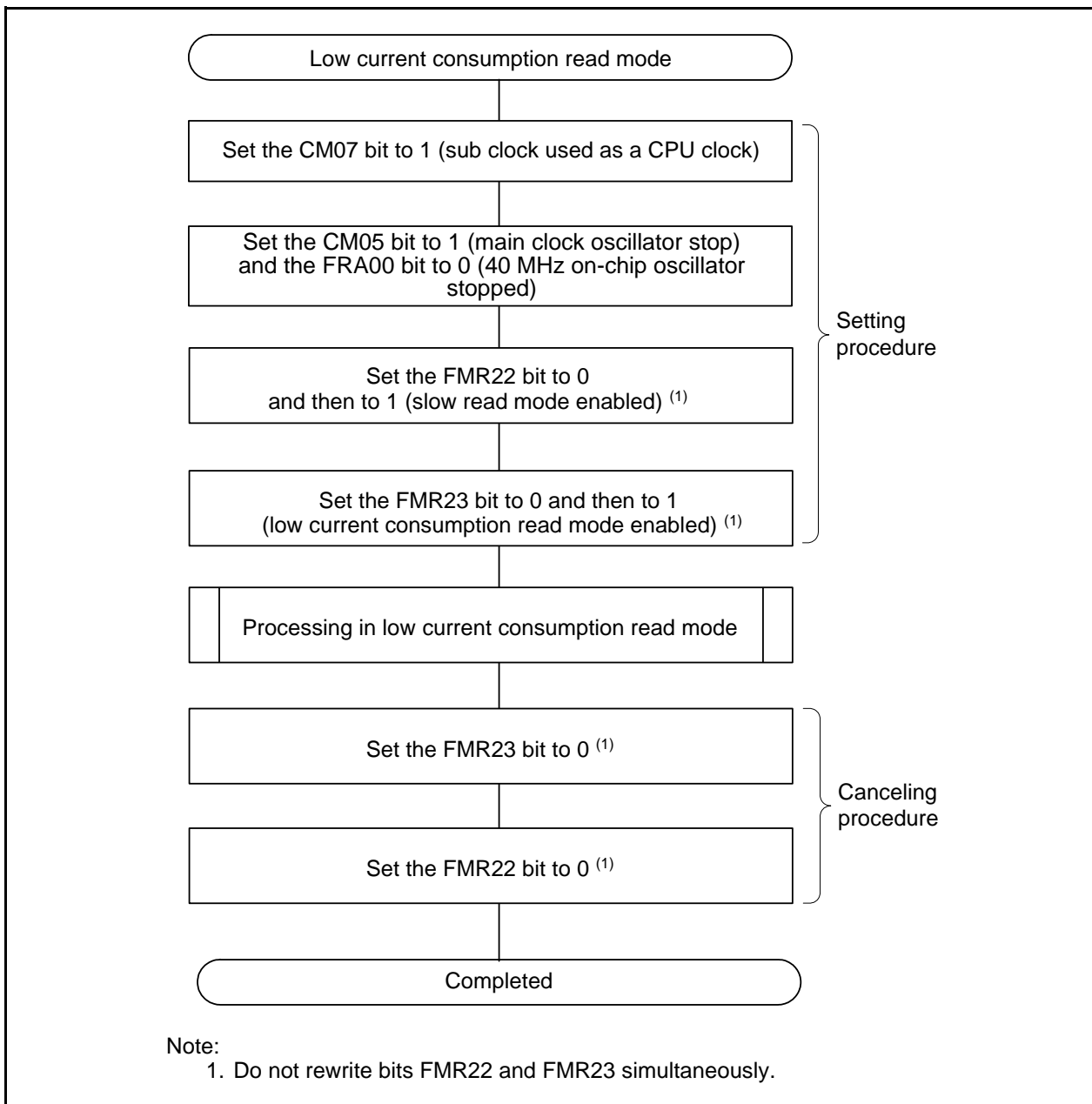


Figure 9.4 Setting and Canceling Low Current Consumption Read Mode

## 9.5 Reducing Power Consumption

To reduce power consumption, refer to the following descriptions when designing a system or writing a program.

### 9.5.1 Ports

The MCU retains the state of each I/O port even when it enters wait mode or stop mode. A current flows in the active output ports. A shoot-through current flows to the input ports in the high-impedance state. Set the unassigned pins to input state, wait until the potential stabilizes, and then enter wait mode or stop mode.

### 9.5.2 A/D Converter

When not performing A/D conversion, set the ADSTBY bit in the ADCON1 register to 0 (A/D operation stopped).

### 9.5.3 Stopping Peripheral Functions

Use the CM02 bit in the CM0 register to stop the unnecessary peripheral functions while in wait mode.

### 9.5.4 Switching the Oscillation-Driving Capacity

Set the driving capacity to low when oscillation is stable.

## 9.6 Notes on Power Control

### 9.6.1 CPU Clock

When switching the CPU clock source, wait until oscillation of the switched clock source is stable. After exiting stop mode, wait until oscillation stabilizes before changing the division.

### 9.6.2 Wait Mode

- Insert four or more NOP instructions following the WAIT instruction. When entering wait mode, because the instruction queue prefetches instructions that follow the WAIT instruction, prefetched instructions are sometimes executed prior to the interrupt routine used to exit wait mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the WAIT instruction, interrupt requests are not accepted before the WAIT instruction is executed.

The following is an example program for entering wait mode:

```

Program Example: FSET   I       ;
                  WAIT      ; Enter wait mode
                  NOP       ; Insert at least four NOP instructions
                  NOP
                  NOP
                  NOP

```

- Do not enter wait mode from PLL operating mode. To enter wait mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter wait mode from low current consumption read mode. To enter wait mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter wait mode from CPU rewrite mode. To enter wait mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Set the PLC07 bit in the PLC0 register to 0 (PLL off). When the PLC07 bit is 1 (PLL on), current consumption cannot be reduced even in wait mode.

### 9.6.3 Stop Mode

- When exiting stop mode by a hardware reset, drive the  $\overline{\text{RESET}}$  pin low for 20 fOCO-S cycles or more.
- Set the MR0 bit in the TAiMR register ( $i = 0$  to 4) to 0 (pulse not output) when using timer A to exit stop mode.
- When entering stop mode, insert a JMP.B instruction immediately after executing an instruction that sets the CM10 bit in the CM1 register to 1 (stop mode), and then insert at least four NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to 1. Thus, some of the instructions may be executed before the MCU enters stop mode or before the interrupt routine for returning from stop mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the instruction to set the CM10 bit to 1, interrupt requests are not accepted before entering stop mode.

The following is an example program for entering stop mode:

```

Program Example:  FSET    I
                  BSET    0, CM1 ; Enter stop mode
                  JMP.B   L2      ; Insert a JMP.B instruction
L2:
                  NOP                ; At least four NOP instructions
                  NOP
                  NOP
                  NOP

```

- The CLKOUT pin outputs a high-level signal in stop mode. Thus, if stop mode is entered right after output on the CLKOUT pin changes state from high to low, the low-level duration of the output signal to the CLKOUT pin becomes shorter.



- Do not enter stop mode from PLL operating mode. To enter stop mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter stop mode from low current consumption read mode. To enter stop mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter stop mode from CPU rewrite mode. To enter stop mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Do not enter stop mode when the oscillator stop/restart detect function is enabled. To enter stop mode, set the CM20 bit in the CM2 register to 0 (oscillator stop/restart detect function disabled).
- Do not enter stop mode when the FMR01 bit is 1 (CPU rewrite mode enabled), and do not enter stop mode when the flash memory is stopped (bits FMR01 and FMSTP are 1).

#### 9.6.4 Low Current Consumption Read Mode

- Enter low current consumption read mode through slow read mode (see Figure 9.4 “Setting and Canceling Low Current Consumption Read Mode” for details).
- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.
- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR23 bit in the FMR2 register to 1 (low current consumption read mode enable).

#### 9.6.5 Slow Read Mode

- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR22 bit in the FMR2 register to 1 (slow read mode enabled).

## 10. Processor Mode

### 10.1 Introduction

Single-chip mode is supported as a processor mode. Table 10.1 lists the Processor Mode Features.

**Table 10.1 Processor Mode Features**

Processor Mode	Access Space	Pins Assigned as I/O Ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

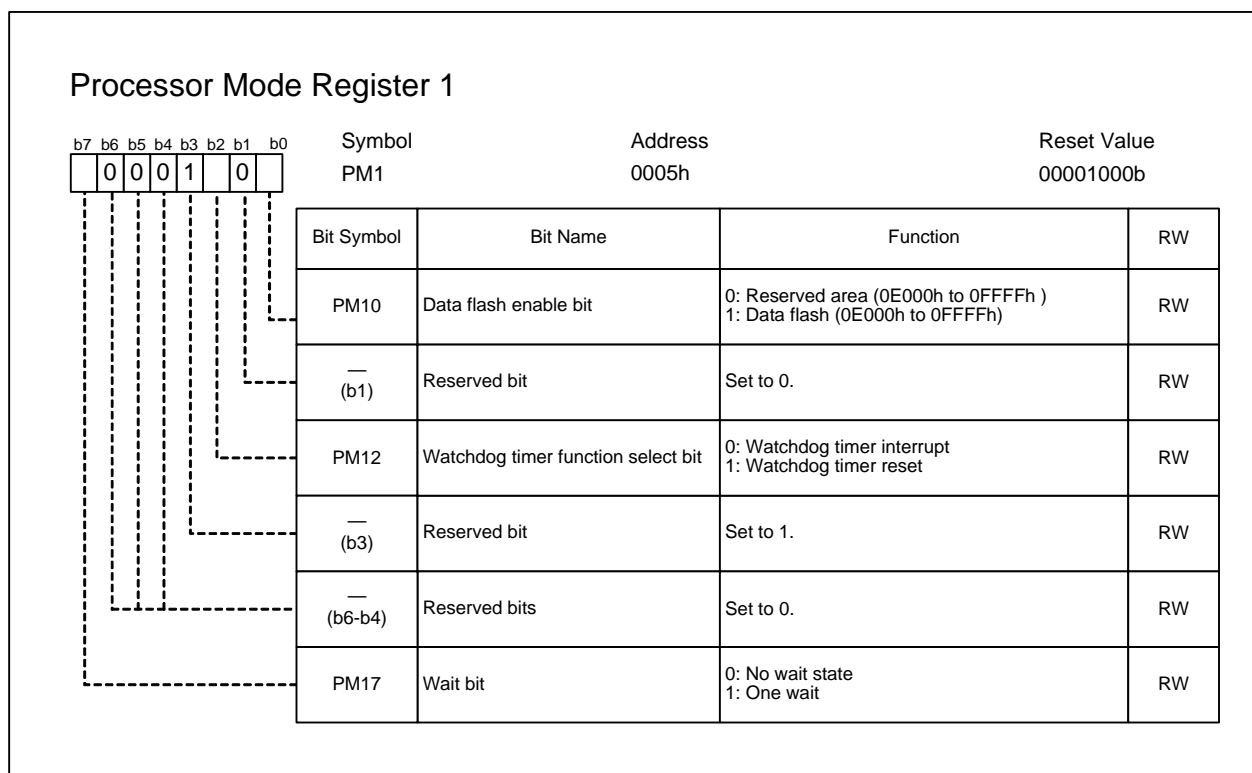


## 10.2 Registers

**Table 10.2 Registers**

Address	Register	Symbol	Reset Value
0005h	Processor Mode Register 1	PM1	0000 1000b
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb

### 10.2.1 Processor Mode Register 1 (PM1)



Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register. The PM12 bit becomes 1 by a program. Setting it to 0 has no effect.

#### PM10 (Data flash enable bit) (b0)

This bit is used to select the function of addresses 0E000h to 0FFFFh.

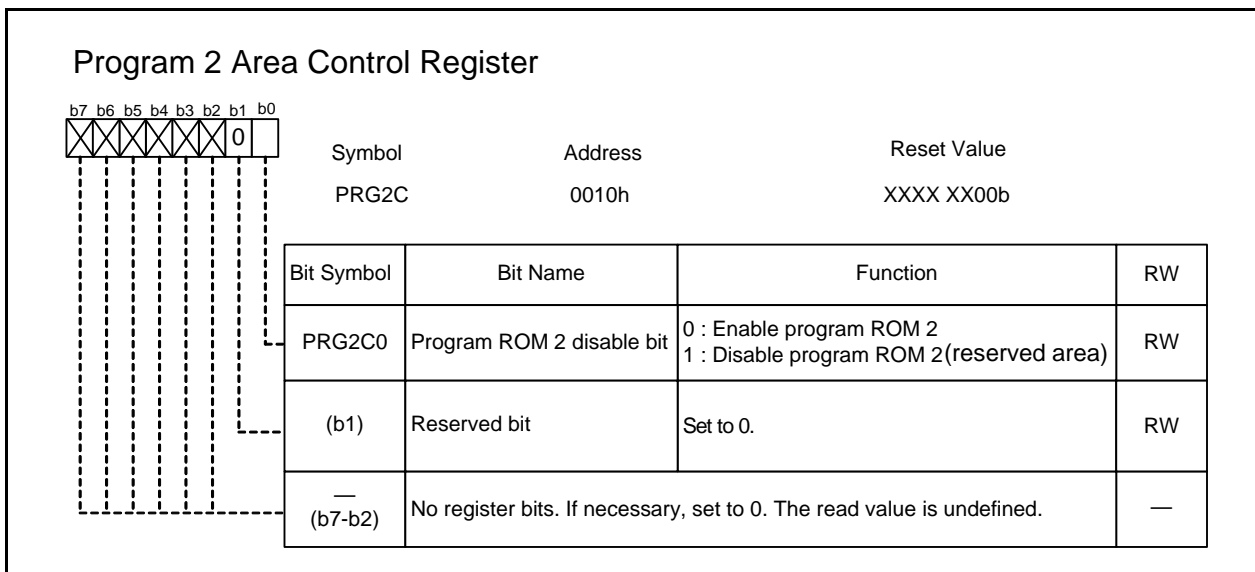
Data flash includes block A (addresses 0E000h to 0EFFFh) and block B (addresses 0F000h to 0FFFFh). When data flash is selected by the setting of the PM10 bit, both block A and block B can be used.

The PM10 bit automatically becomes 1 while the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode).

#### PM17 (Wait Bit) (b7)

This is a software wait select bit for internal memory.

### 10.2.2 Program 2 Area Control Register (PRG2C)



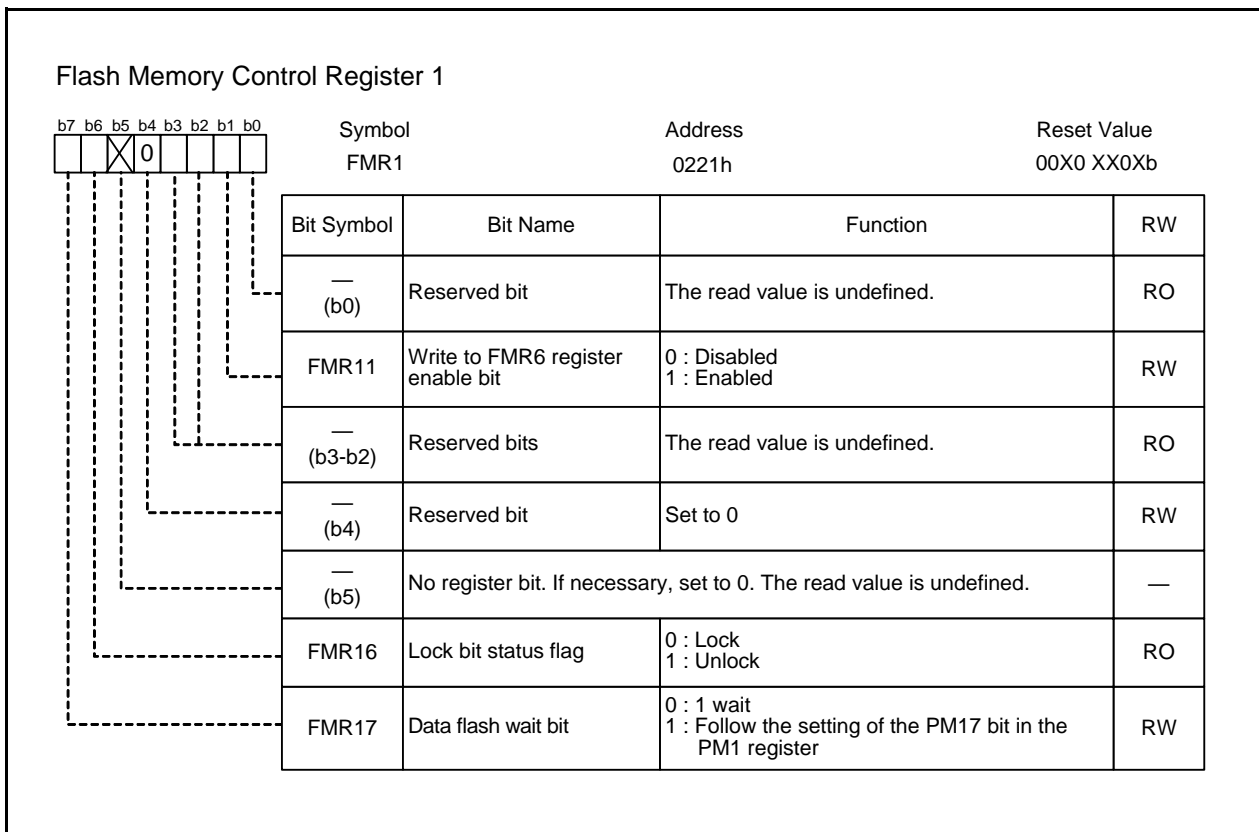
Set the PRC6 bit in the PRCR register to 1 (write enabled) before rewriting this register.

#### PRG2C0 (Program ROM 2 disable bit) (b0)

This bit is used to select the function of program ROM 2 (addresses 10000h to 13FFFh).

Program ROM 2 includes the on-chip debugger monitor area and user boot code area. Refer to 26.7.1 “User Boot Function” for details.

### 10.2.3 Flash Memory Control Register 1 (FMR1)



#### FMR17 (Data Flash Wait Bit) (b7)

This bit is used to select the number of wait states for data flash.

When setting this bit to 0, one wait is inserted to the read cycle of the data flash. The write cycle is not affected.

### 10.3 Software Wait

The PM17 bit in the PM1 register, PM20 bit in the PM2 register, and FMR17 bit in the FMR1 register select software wait and the bus cycles will be determined accordingly. Table 10.3 lists the relation between software wait related bits and bus cycle.

**Table 10.3 Software Wait Related Bits and Bus Cycles**

Area		Software Wait Related Bits and Settings		Software Wait	Bus Cycle
		FMR17 bit in the FMR1 register	PM17 bit in the PM1 register		
SFR		—	—	1 wait	2 BCLK cycles <sup>(1)</sup>
Internal RAM		—	0	no wait	1 BCLK cycle <sup>(1)</sup>
			1	1 wait	2 BCLK cycles
Internal ROM	Program ROM 1	—	0	no wait	1 BCLK cycles <sup>(1)</sup>
	Program ROM 2		1	1 wait	2 BCLK cycles
	Data flash	0	—	1 wait	2 BCLK cycles <sup>(1)</sup>
		1	0	no wait	1 BCLK cycle
			1	1 wait	2 BCLK cycles

—: 0 or 1 has no effect

Note:

1. Status after reset.

### 10.4 Bus Hold

The internal bus is in a hold state under the following condition:

- Rewriting the flash memory in EW1 mode while auto-programming or auto-erasing

When the bus is in hold state, the following occur:

- CPU stops.
- DMAC stops.
- The watchdog timer stops when the CSPRO bit in the CSPR register is 0 (count source protection mode disabled).
- The I/O port state is maintained.

Bus use priority is given to bus hold, DMAC, and CPU in descending order. However, if the CPU is accessing an odd address in word units, DMAC cannot gain control of the bus between two separate accesses. Figure 10.1 “Bus Use Priority” shows the bus use priority.

**Bus Hold > DMAC > CPU**

**Figure 10.1 Bus Use Priority**

## 11. Programmable I/O Ports

### Note

The 64-pin package has no P0\_4 to P0\_7, P1\_0 to P1\_4, P3\_4 to P3\_7, P9\_5 to P9\_7.

### 11.1 Introduction

Table 11.1 lists Programmable I/O Port Specifications (hereafter referred to as I/O ports).

Each pin functions as a programmable I/O port or a peripheral function input/output.

To set peripheral functions, refer to the description for the individual function. To use ports as peripheral function input/output pins, refer to 11.4 "Peripheral Function I/O".

Table 11.2 lists the I/O ports.

**Table 11.1 Programmable I/O Port Specifications**

Item	Specification	
	80-pin	64-pin
Number of ports	71 (CMOS input/output)	55 (CMOS input/output)
Input/output	Select input/output for each port by a program.	
Selectable function	A pull-up resistor is selectable for every four input ports. Select the input level for every eight input ports.	

**Table 11.2 I/O Ports**

Pin Name		I/O Type	Function
80-pin	64-pin		
P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	P0_0 to P0_3, P1_5 to P1_7, P2_0 to P2_7, P3_0 to P3_3, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P10_0 to P10_7	I/O	Input/output port CMOS output, pull-up resistor selectable Input level selectable

### 11.2 I/O Ports and Pins

Figure 11.1 to Figure 11.6, and Table 11.3 and Table 11.8 show the programmable I/O ports, and Figure 11.7 shows the pins.

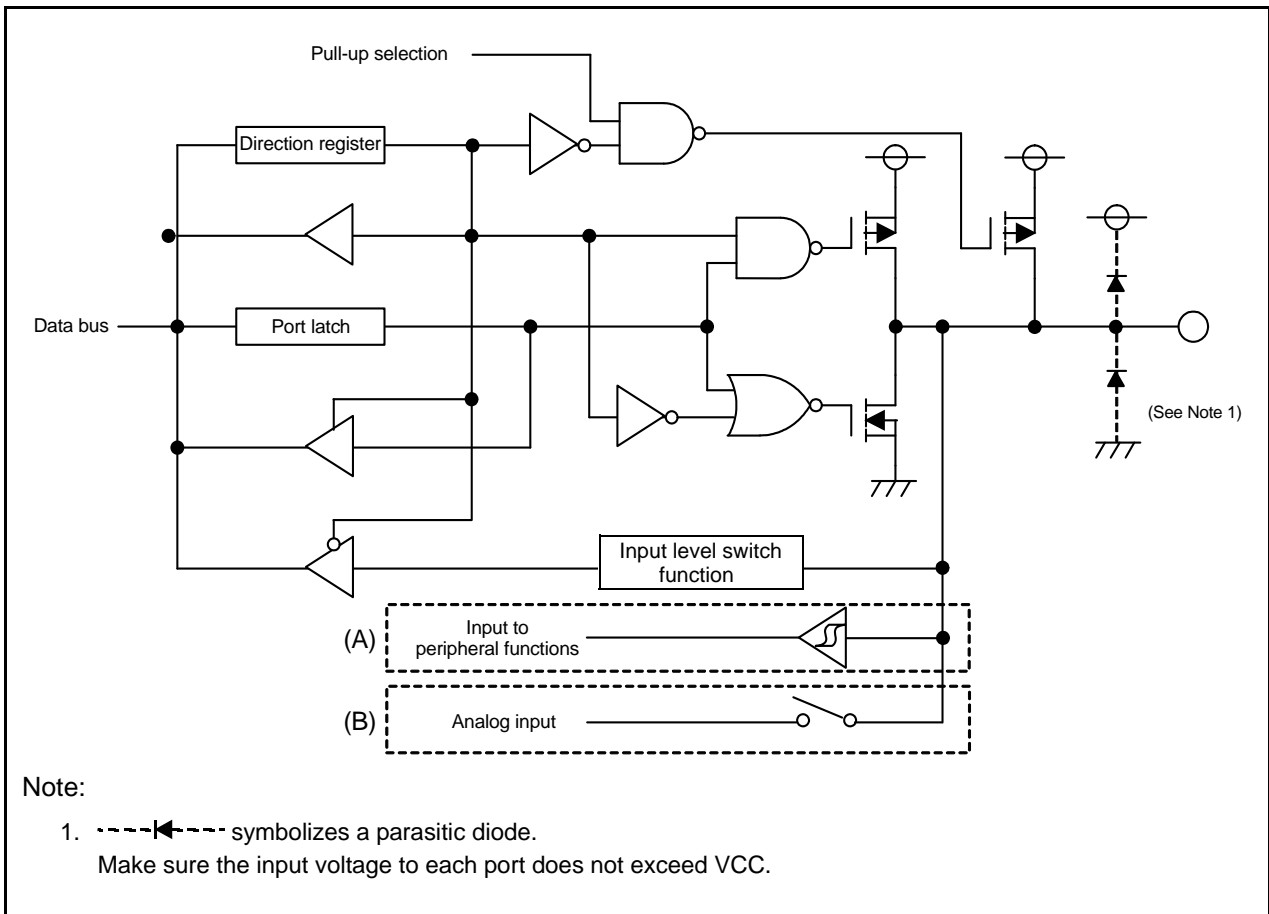


Figure 11.1 I/O Ports (Basic)

Table 11.3 I/O Ports (Basic)

Port	Peripheral Function I/O	
	Peripheral function input (A) in Figure 11.1	Analog input (B) in Figure 11.1
P3_4 to P3_7	N/A	N/A
P0_0 to P0_7, P10_0 to P10_3, P9_3 (1)	N/A	Available
P3_1, P6_2, P6_6, P7_7, P8_2 to P8_4	Available	N/A
P9_1, P9_2, P9_7, P10_4 to P10_7	Available	Available

Note:

- P9\_3 is for the M16C/56 Group

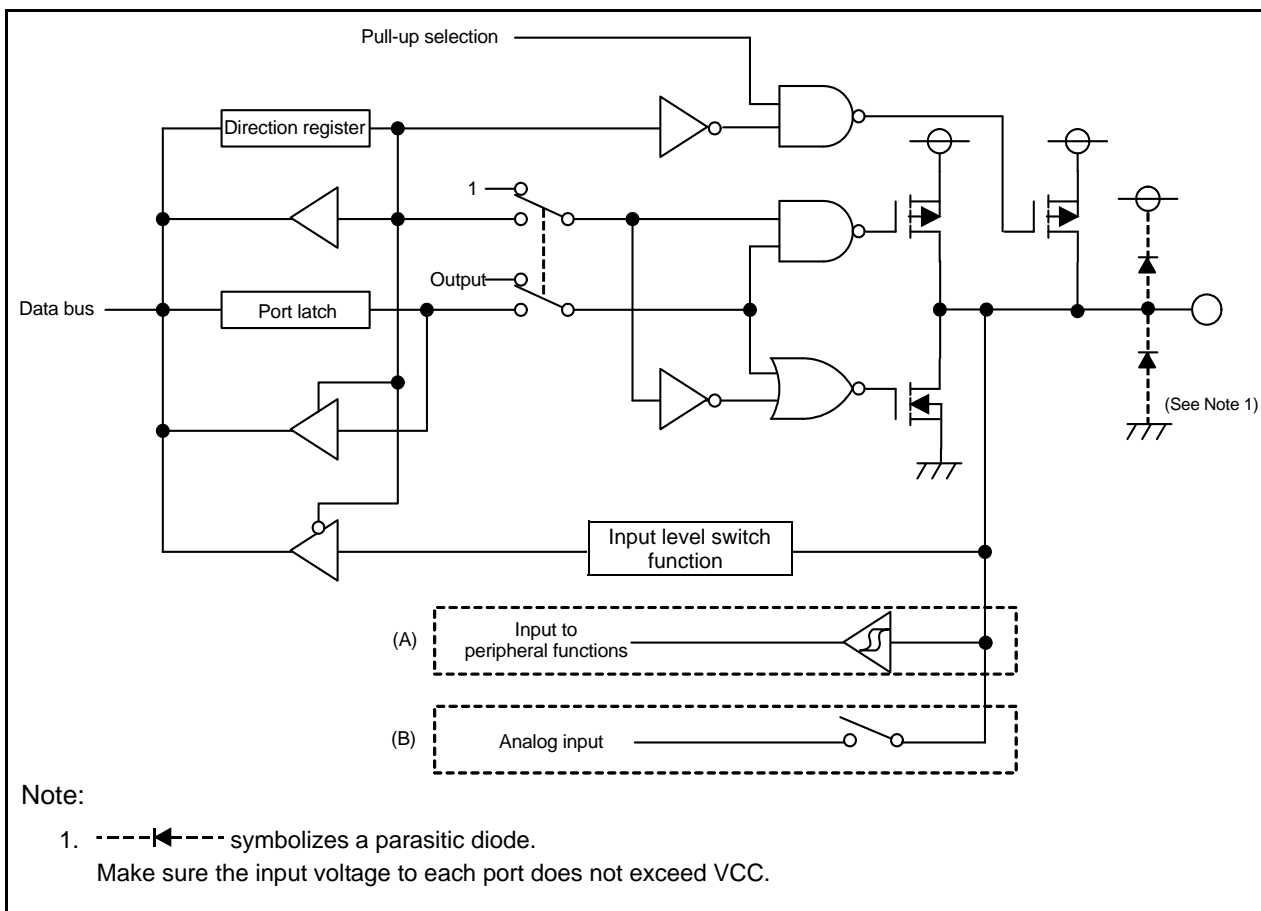


Figure 11.2 I/O Ports (Output)

Table 11.4 I/O Ports (Output)

Port	Peripheral Function I/O	
	Peripheral function input (A) in Figure 11.2	Analog input (B) in Figure 11.2
P9_3 (1)	N/A	Available
P2_2 to P2_7, P3_0, P3_3, P6_0, P6_1, P6_4, P6_5, P7_4 to P7_6, P8_0, P8_1	Available	N/A
P9_0, P9_5	Available	Available

Note:

- P9\_3 is for the M16C/5L Group

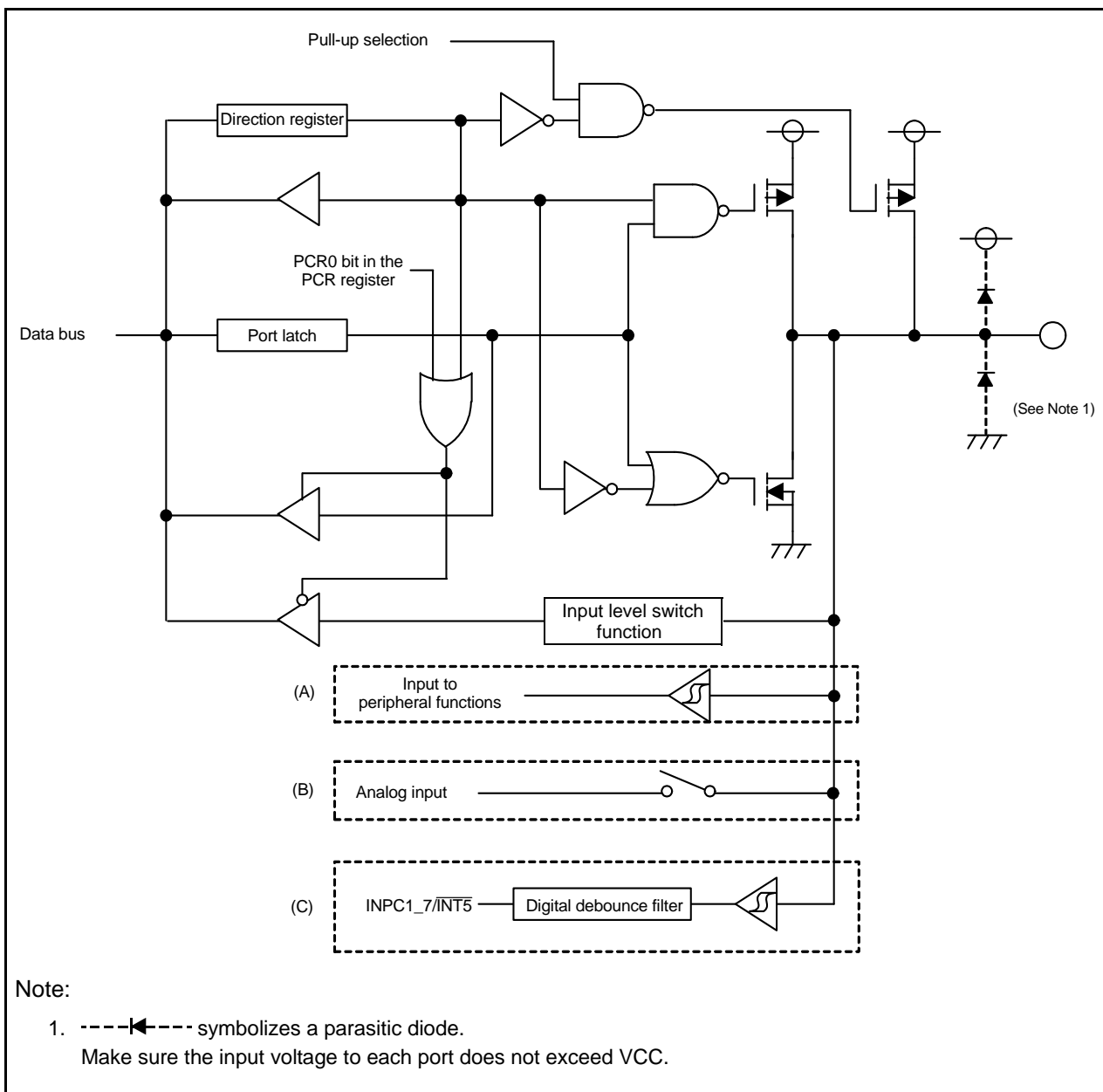


Figure 11.3 I/O Ports (Port P1, P1\_7)

Table 11.5 I/O Ports (Port P1, P1\_7)

Port	Peripheral Function I/O		
	Peripheral Function Input (A) in Figure 11.3	Analog input (B) in Figure 11.3	Peripheral function input (C) in Figure 11.3
P1_4	N/A	N/A	N/A
P1_0 to P1_3	N/A	Available	N/A
P1_5, P1_6	Available	N/A	N/A
P1_7	Available	N/A	Available



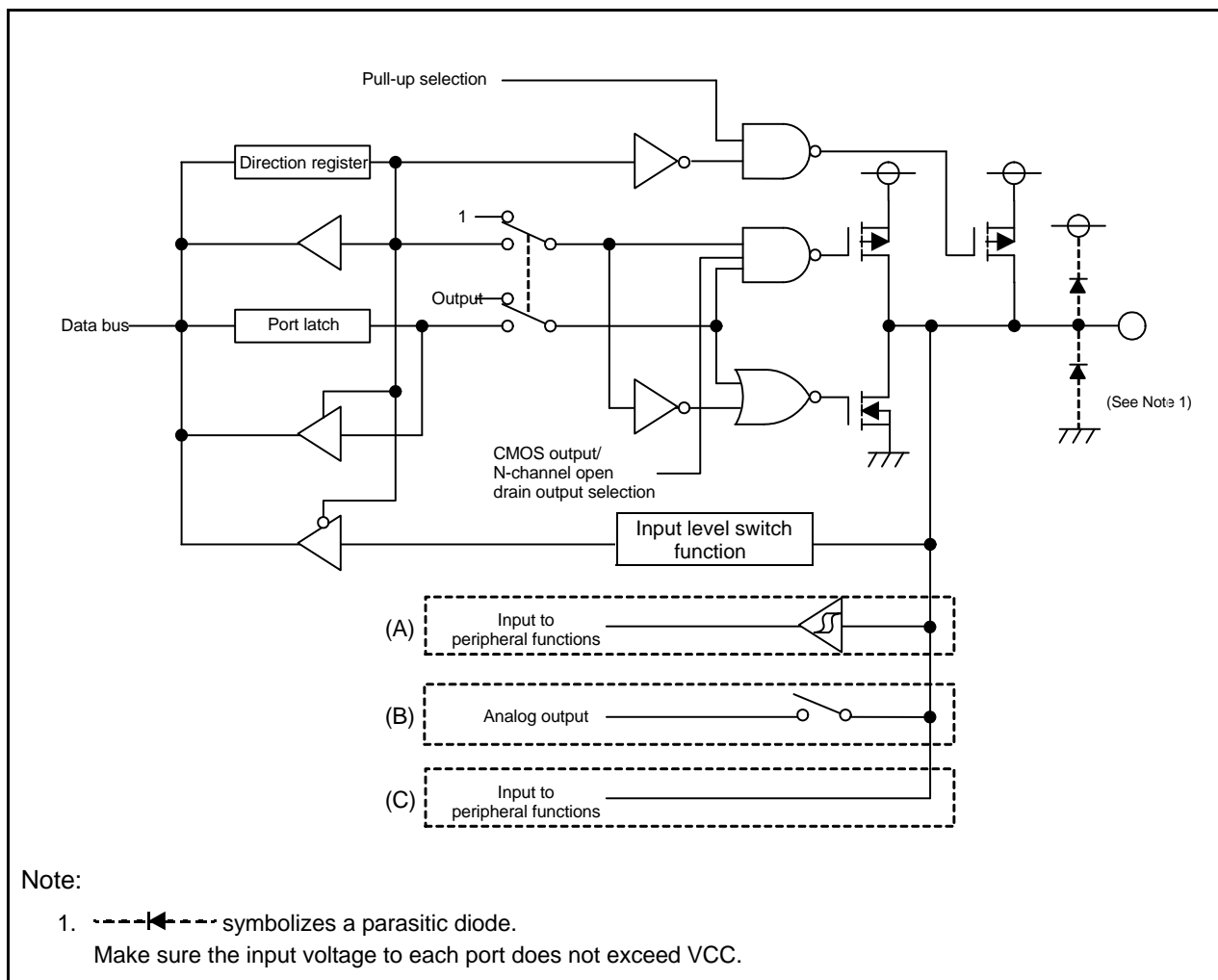


Figure 11.4 I/O Ports (CMOS output/N-channel open drain output selection)

Table 11.6 I/O Ports (CMOS output/N-channel open drain output selection)

Port	Peripheral Function I/O		
	Peripheral function input (A) in Figure 11.4	Analog input (B) in Figure 11.4	Peripheral function input (C) in Figure 11.4
P3_2, P6_3, P6_7	N/A	N/A	N/A
P9_6	N/A	Available	N/A
P7_0 to P7_3	Available	N/A	N/A
P2_0, P2_1	Available	N/A	Available

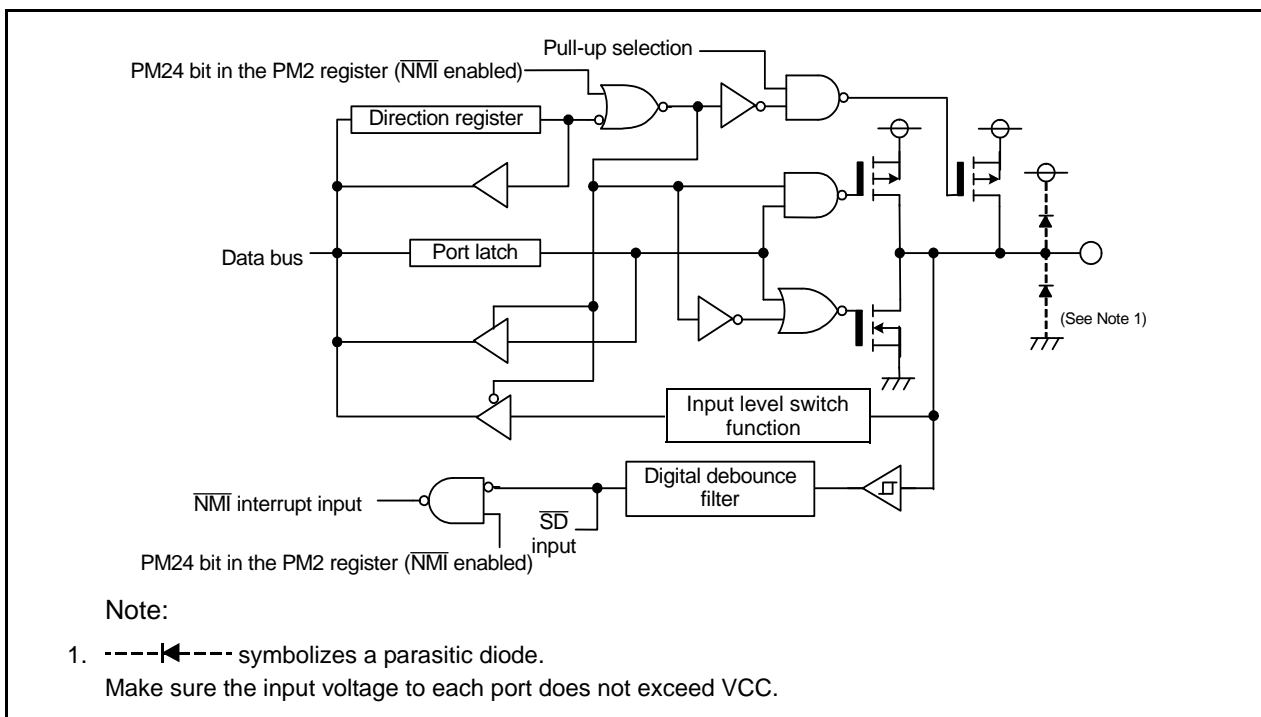


Figure 11.5 I/O Ports ( $\overline{\text{NMI}}$ )

Table 11.7 I/O Ports ( $\overline{\text{NMI}}$ )

Port	Peripheral Function I/O	
	Peripheral function input	Analog input
P8_5	Available	N/A

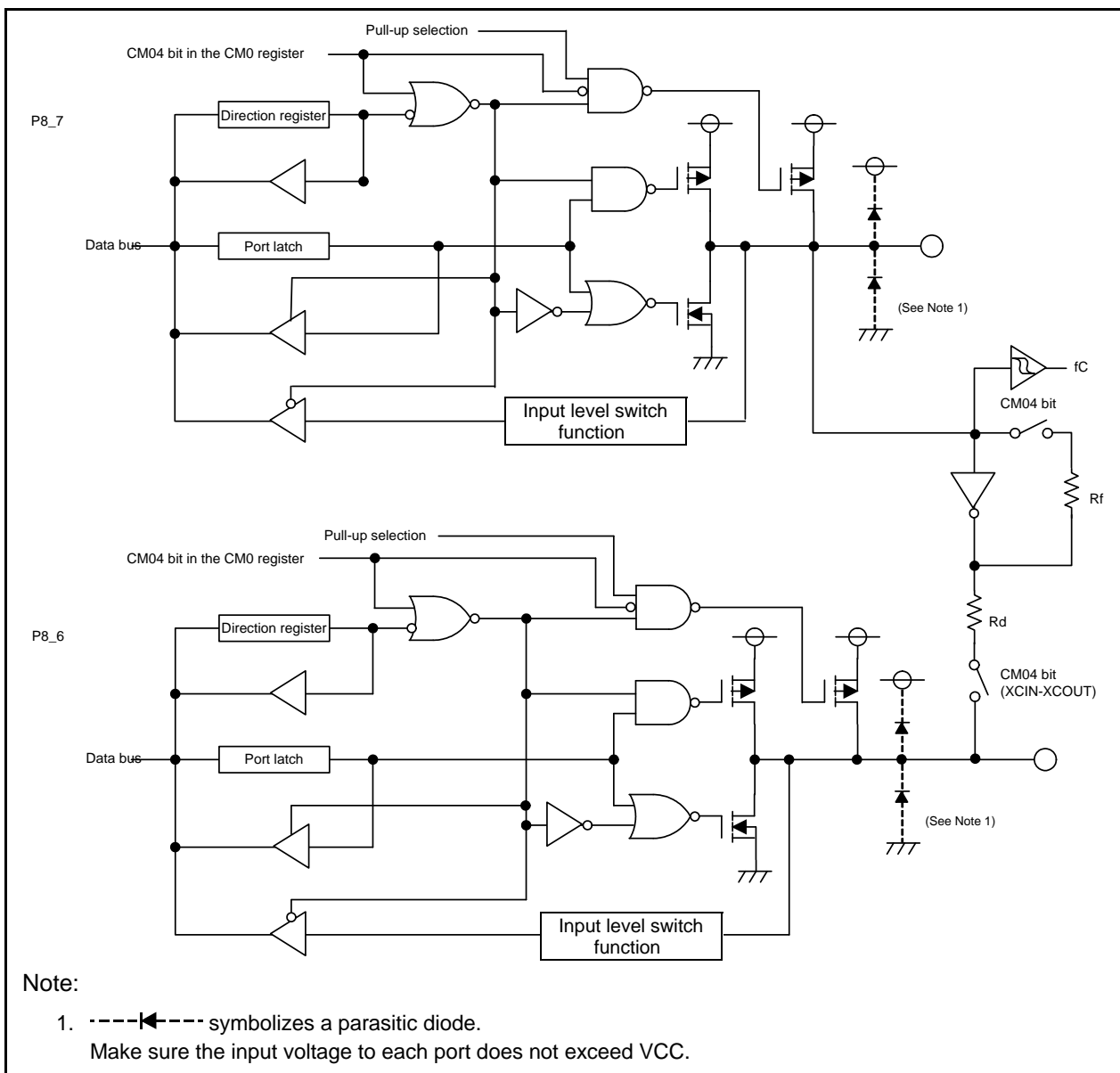
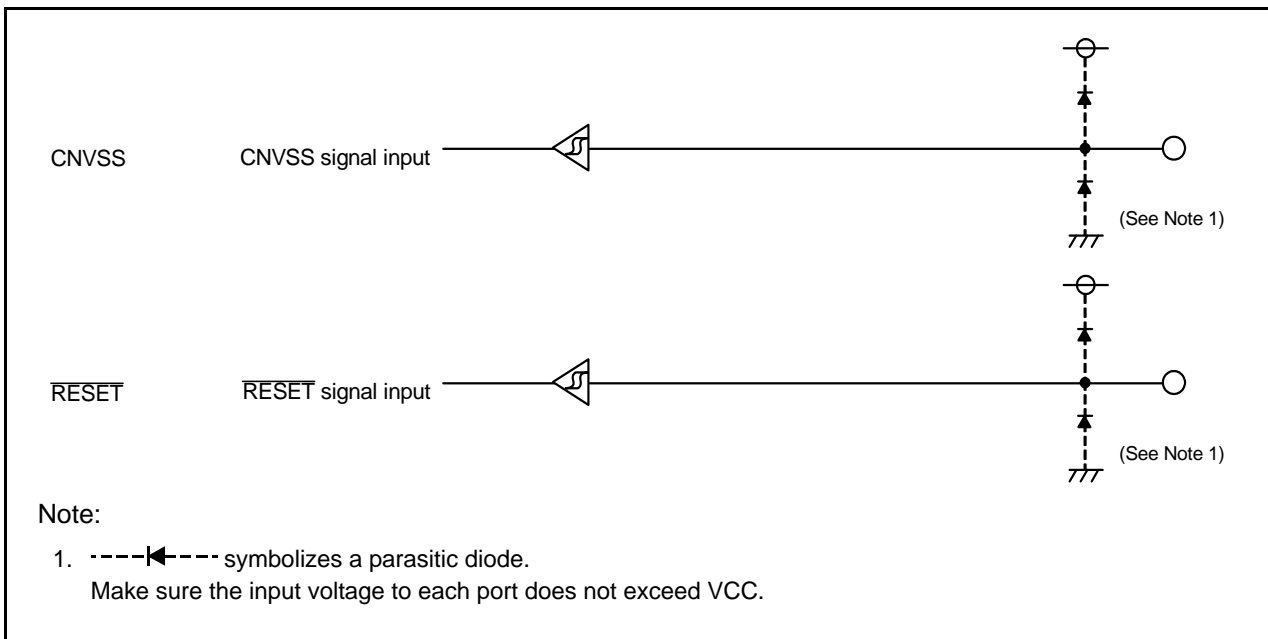


Figure 11.6 I/O Ports (XC)

Table 11.8 I/O Ports (XC)

Port	Peripheral Function I/O	
	Peripheral function input	Analog input
P8_6, P8_7	N/A	N/A

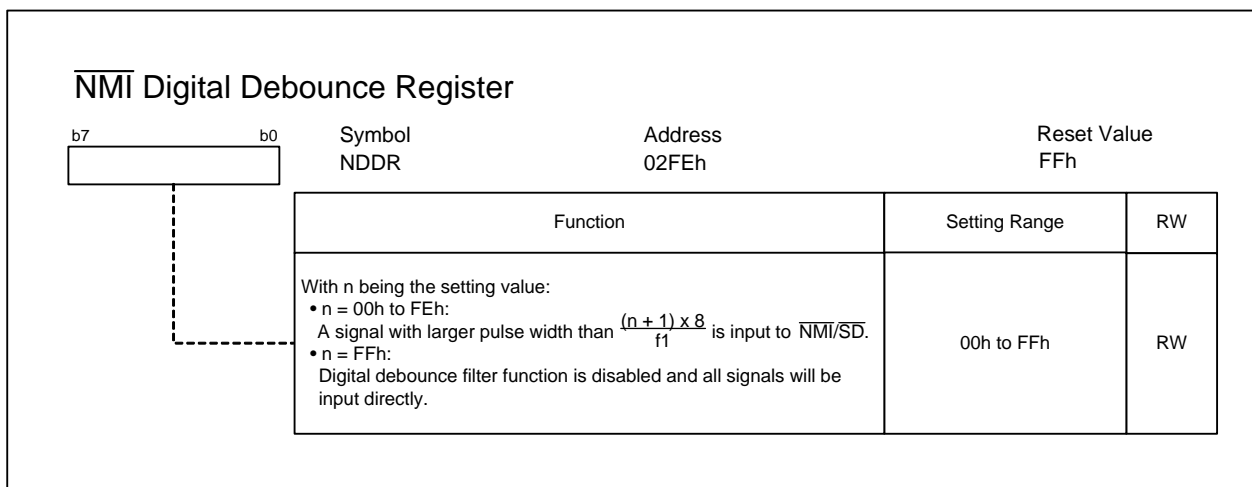
**Figure 11.7 Pins**

## 11.3 Registers

**Table 11.9 Registers**

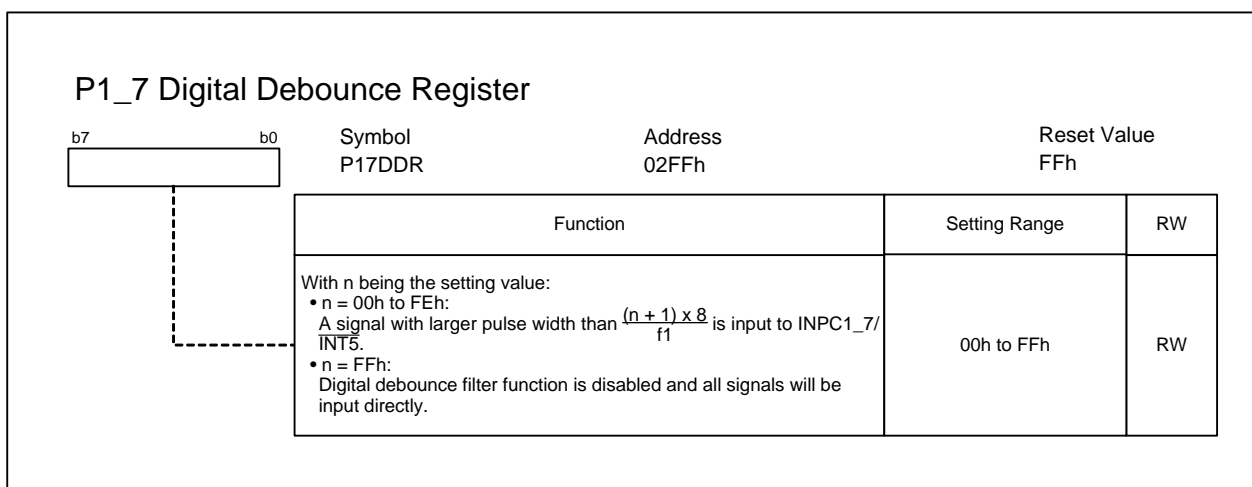
Address	Register Name	Register Symbol	Reset Value
02FEh	NMI Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	00h
0362h	Pull-Up Control Register 2	PUR2	00h
0366h	Port Control Register	PCR	0XX0 0XX0b
036Ch	Input Threshold Select Register 0	VLT0	00h
036Dh	Input Threshold Select Register 1	VLT1	0000 XXXXb
036Eh	Input Threshold Select Register 2	VLT2	XX00 0000b
0370h	Pin Assignment Control Register	PACR	0XXX X000b
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	000X 0000b
03F4h	Port P10 Register	P10	XXh
03F6h	Port P10 Direction Register	PD10	00h

### 11.3.1 $\overline{\text{NMI}}$ Digital Debounce Register (NDDR)



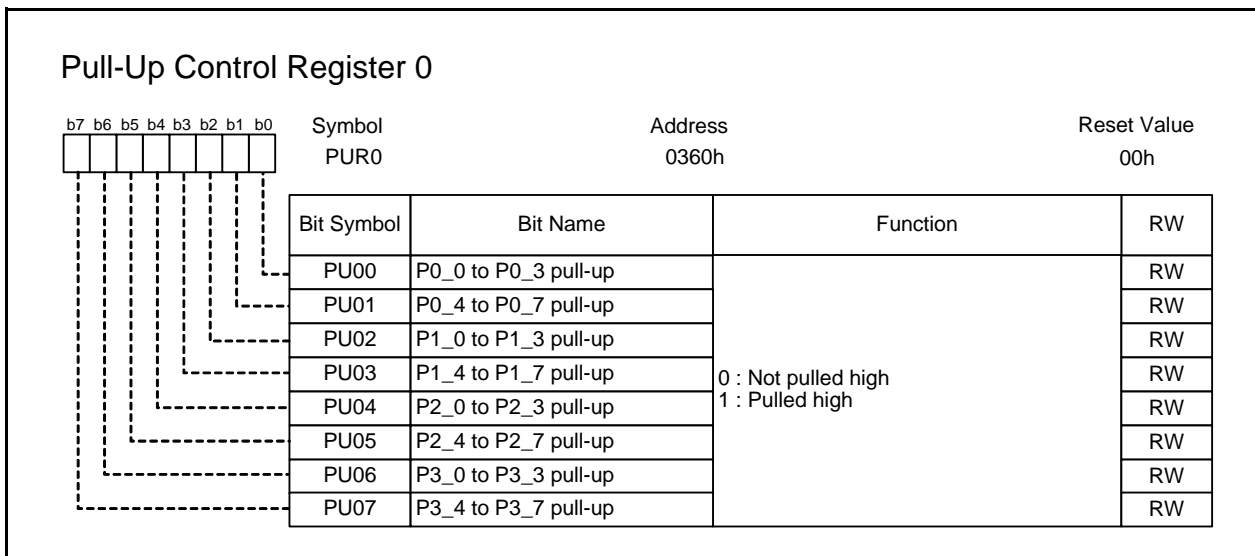
When using the  $\overline{\text{NMI}}$  interrupt to exit from stop mode, set FFh to the NDDR register before entering stop mode. The NDDR register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupt or DMA transfer should be generated between these two instructions.

### 11.3.2 P1\_7 Digital Debounce Register (P17DDR)



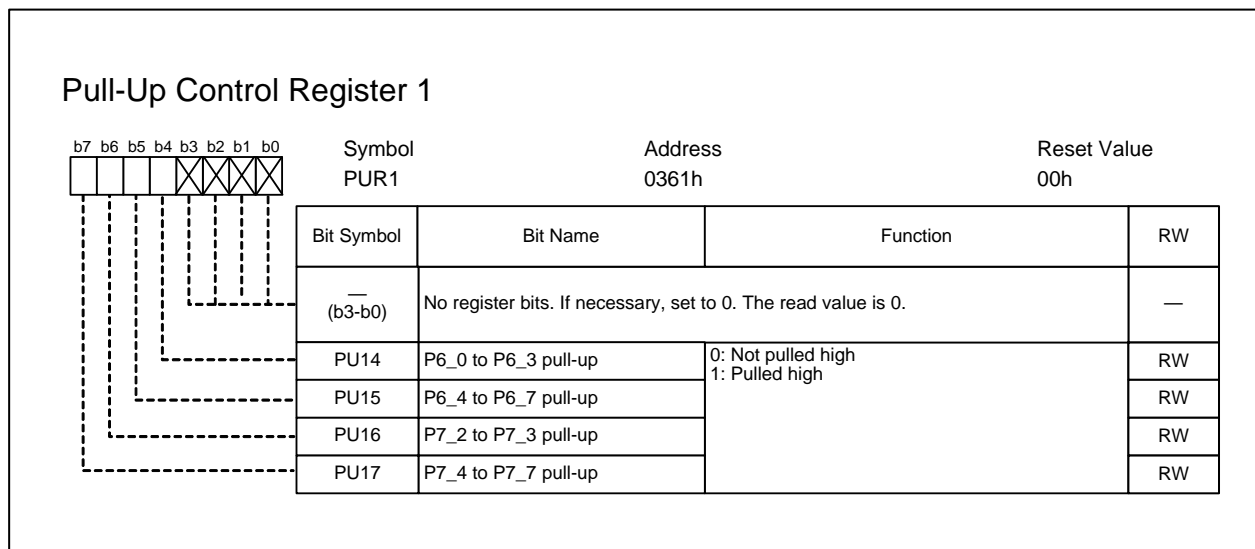
When using the  $\overline{\text{INT5}}$  interrupt to exit from stop mode, set FFh to the P17DDR register before entering stop mode.

### 11.3.3 Pull-Up Control Register 0 (PUR0)



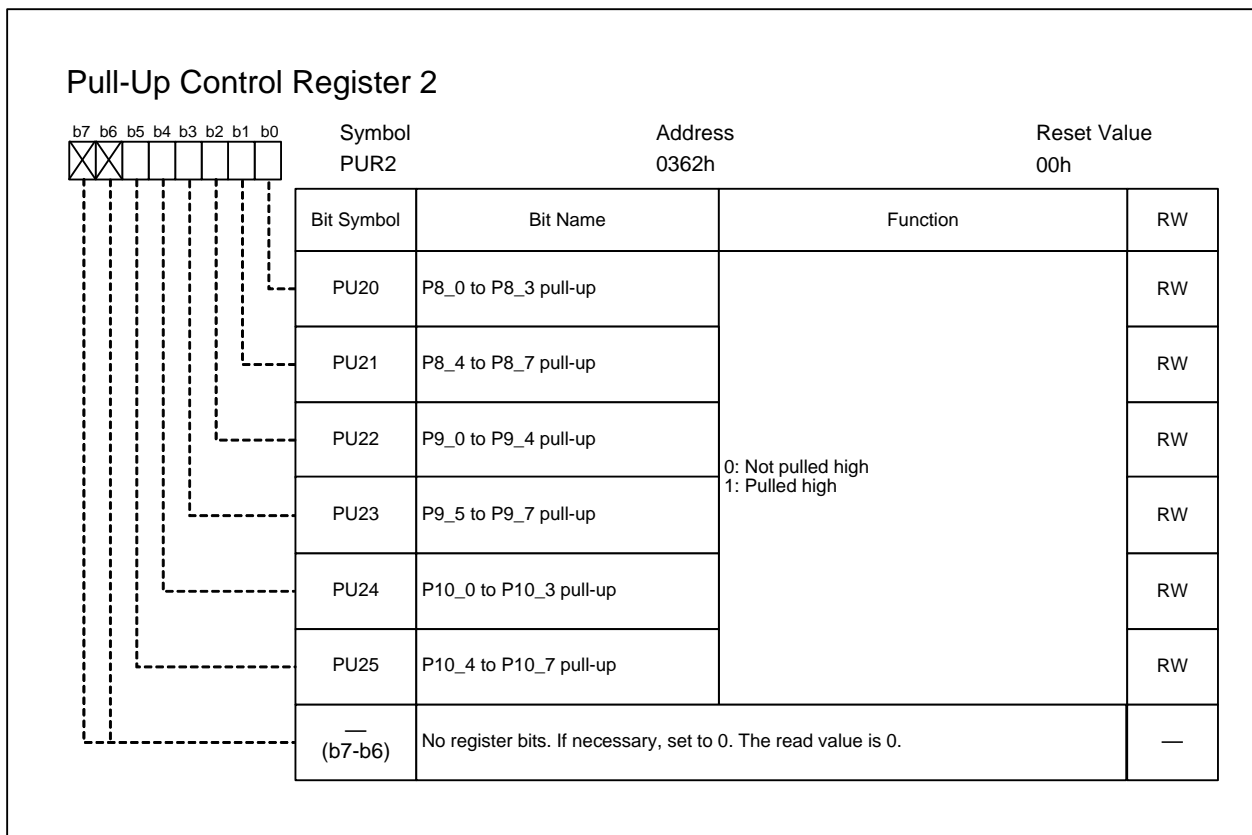
The pin for which the bit in the PUR0 register is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

### 11.3.4 Pull-Up Control Register 1 (PUR1)



The pin for which the bit in the PUR1 register is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

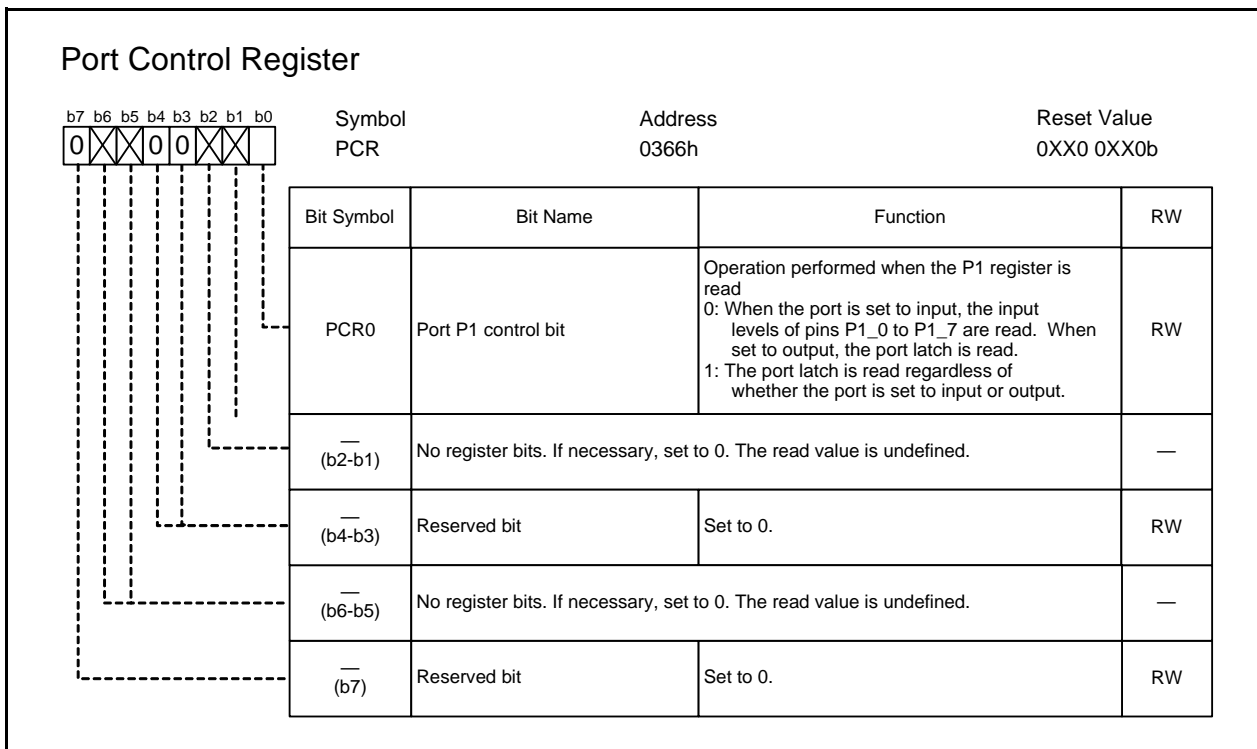
### 11.3.5 Pull-Up Control Register 2 (PUR2)



The pin for which the bit in the PUR2 register is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.



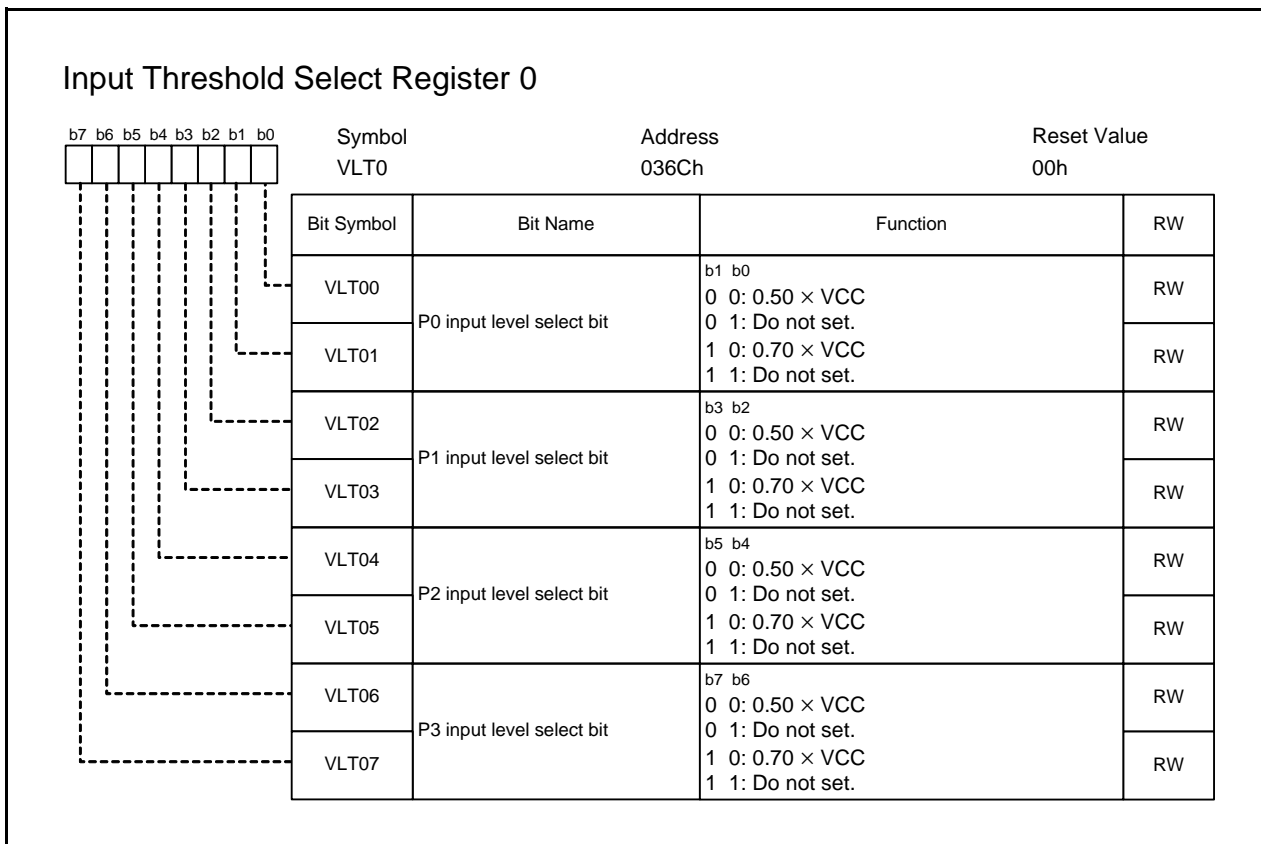
### 11.3.6 Port Control Register (PCR)



#### PCR0 (Port P1 Control Bit) (b0)

When the P1 register is read after the PCR0 bit is set to 1, the corresponding port latch is read regardless of the PD1 register setting.

### 11.3.7 Input Threshold Select Register 0 (VLT0)



The input level of ports can be selected. The input level of peripheral functions is not affected.

### 11.3.8 Input Threshold Select Register 1 (VLT1)

Input Threshold Select Register 1			
	Symbol VLT1	Address 036Dh	Reset Value 0000XXXXb
Bit Symbol	Bit Name	Function	RW
— (b3-b0)	No register bits. If necessary, set to 0. The read value is undefined.		—
VLT14	P6 input level select bit	b5 b4 0 0 : 0.50 x VCC 0 1 : Do not set 1 0 : 0.70 x VCC 1 1 : Do not set	RW
VLT15			RW
VLT16			P7 input level select bit
VLT17	RW		

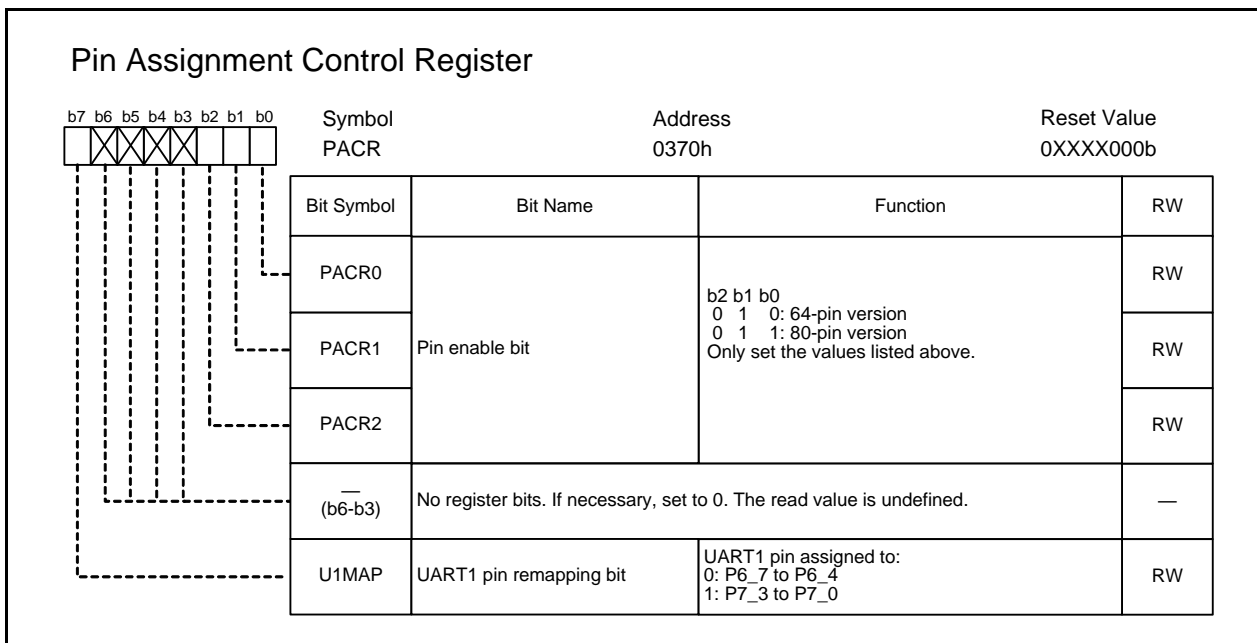
The input level of ports can be selected. The input level of peripheral functions is not affected.

### 11.3.9 Input Threshold Select Register 2 (VLT2)

Input Threshold Select Register 2			
	Symbol VLT2	Address 036Eh	Reset Value XX00 0000b
Bit Symbol	Bit Name	Function	RW
VLT20	P8 input level select bit	b1 b0 0 0 : 0.50 x VCC 0 1 : Do not set. 1 0 : 0.70 x VCC 1 1 : Do not set.	RW
VLT21			RW
VLT22			P9_0 to P9_3, P9_5 to P9_7 input level select bit
VLT23	RW		
VLT24	P10 input level select bit	b5 b4 0 0 : 0.50 x VCC 0 1 : Do not set. 1 0 : 0.70 x VCC 1 1 : Do not set.	RW
VLT25			RW
— (b7-b6)			No register bits. If necessary, set to 0. The read value is undefined.

The input level of ports can be selected. The input level of peripheral functions is not affected.

### 11.3.10 Pin Assignment Control Register (PACR)



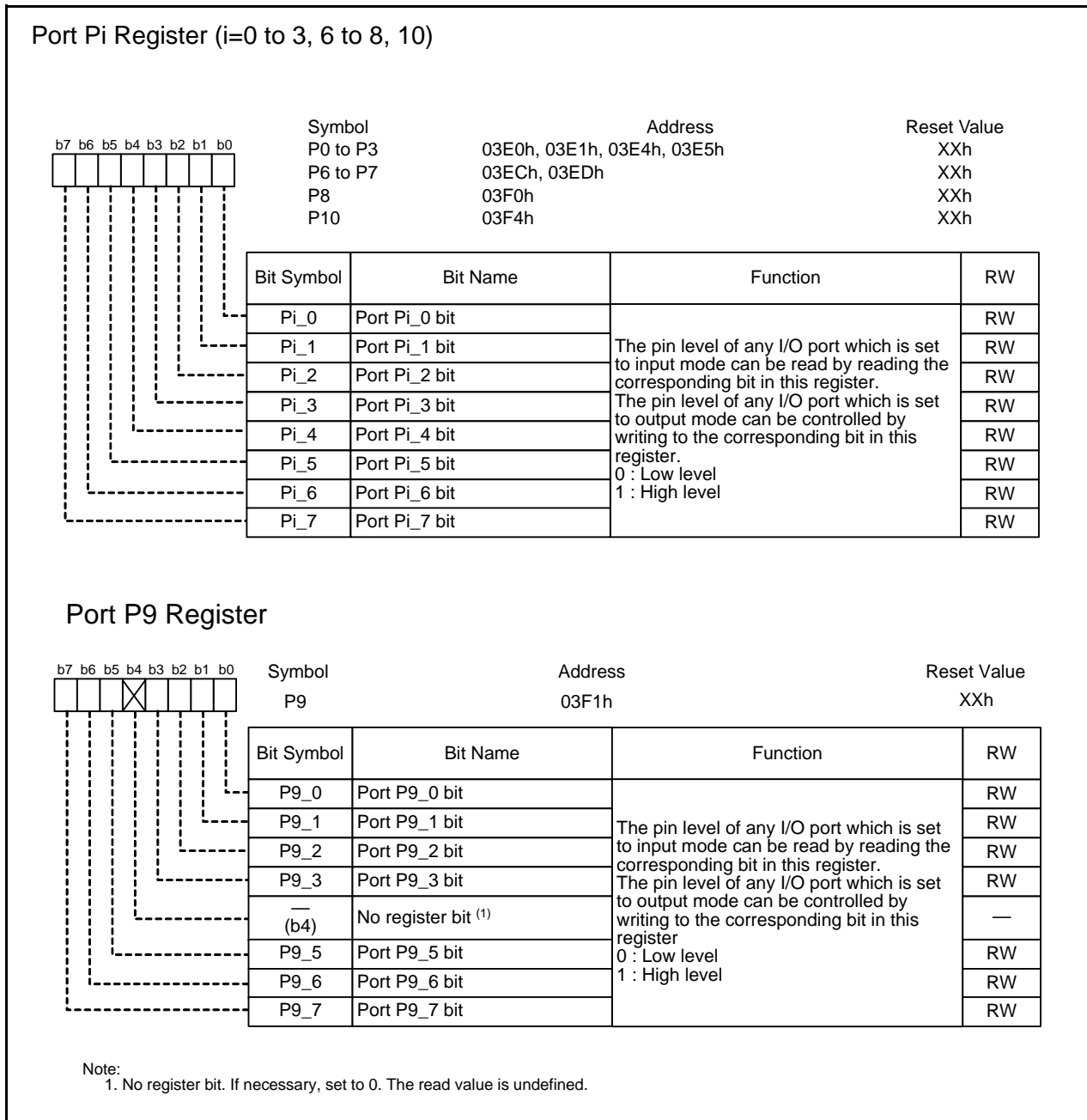
Write to the PACR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

#### PACR2 to PACR0 (Pin Enable Bit) (b2 to b0)

Bits PACR2 to PACR0 are 000b after reset. Select either 010b (64-pin package), or 011b (80-pin package) depending on a product.

Set bits PACR2 to PACR0 before inputting or outputting to each pin. When their value does not change after reset, I/O function of some the pins is disabled.

### 11.3.11 Port Pi Register (Pi) (i = 0 to 3, 6 to 10)



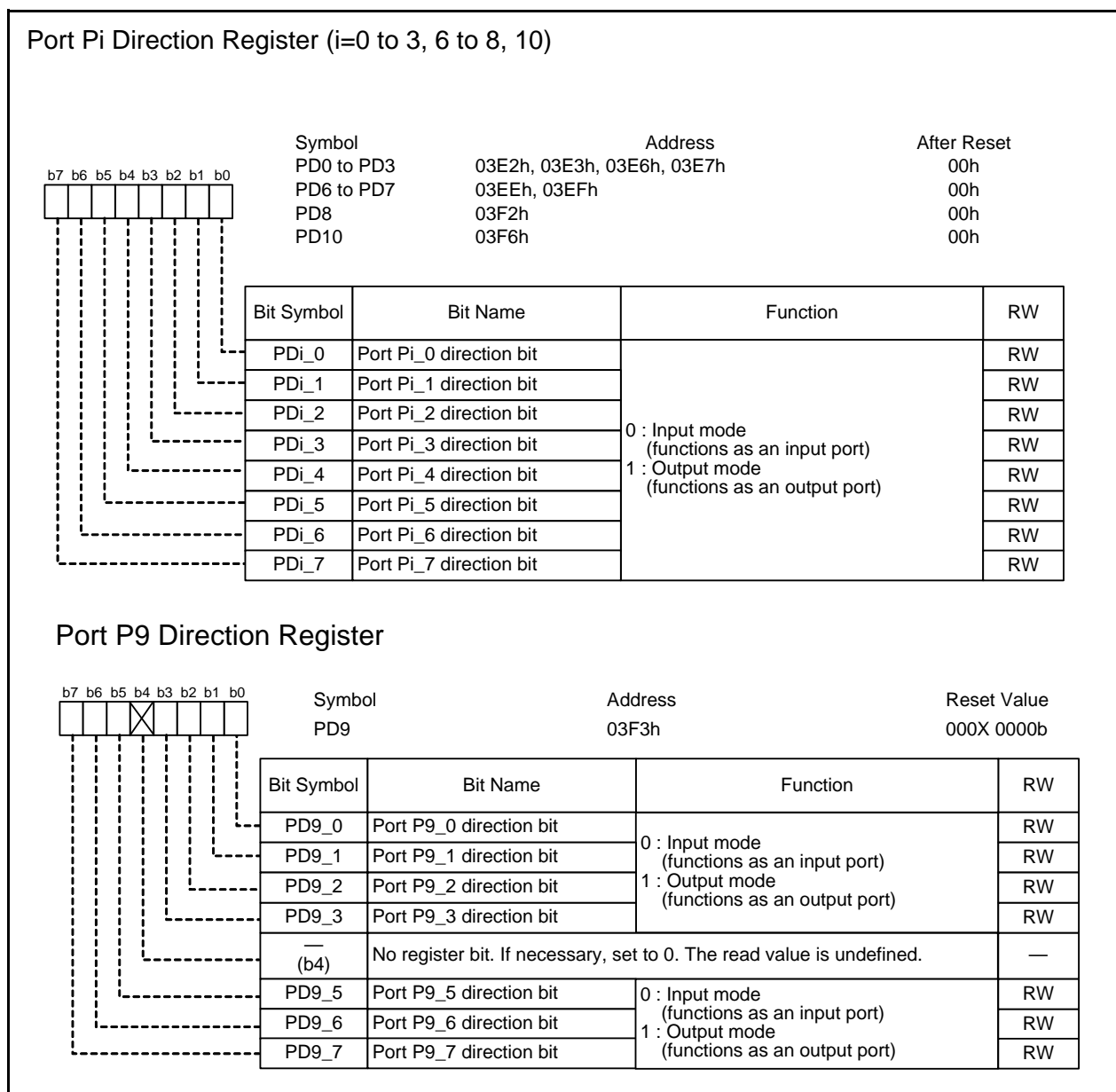
Data input/output to and from external devices are accomplished by reading and writing to the Pi register.

Each bit in the Pi register consists of a port latch to hold the output data and a circuit to read the pin status.

For ports set to input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.

For ports set to output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

### 11.3.12 Port Pi Direction Register (PDi) (i = 0 to 3, 6 to 10)



Write to the PD9 register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

These registers select whether I/O ports are to be used for input or output. Each bit in the PDi register corresponds to one port.

To use I/O pins shared with the following peripheral functions, set the corresponding port direction bit to 0 (input mode):

## 11.4 Peripheral Function I/O

### 11.4.1 Peripheral Function I/O and Port Direction Bits

Programmable I/O ports can share pins with peripheral function I/O (see Table 1.7 to Table 1.10 Pin Names). Some peripheral function I/O are affected by a port direction bit which shares the same pin. Table 11.10 lists The Setting of Direction Bits Functioning as Peripheral Function I/O. For peripheral function settings, see descriptions of each function.

**Table 11.10 The Setting of Direction Bits Functioning as Peripheral Function I/O**

Peripheral Function I/O	The Setting of the Port Direction Bit Sharing the Same Pin
Input	Set to 0 (input mode).
Output	Set to either 0 or 1 (outputs regardless of the direction bit setting).

### 11.4.2 Priority Level of Peripheral Function I/O

Multiple peripheral functions can share the same pin.

For example, when peripheral function A and peripheral function B share a pin, input and output are as follows:

- When the pin functions as input for peripheral functions A and B  
The same signal is input as an input signal for each function. However, the timing of accepting the signal differs depending on conditions (e.g. internal delay) of peripheral functions A and B.
- When the pin functions as output for peripheral function A and as input for peripheral function B  
Peripheral function A outputs a signal from the pin, and peripheral function B inputs the signal.

### 11.4.3 Digital Debounce Filters

The MCU has two digital debounce filters for noise reduction, assigned to  $\overline{\text{NMI/SD}}$  and  $\overline{\text{INT5/INPC1\_7}}$ . Registers NDDR and P17DDR set the filter widths, respectively.

The digital debounce function is triggered by a rising or falling edge of digital input signal to either  $\overline{\text{NMI/SD}}$  and  $\overline{\text{INT5/INPC1\_7}}$ . When the input pulse is longer than the filter width set by a program, the signal level is determined. Any noise that is shorter than the filter width is blocked by this function. Digital debounce function is disabled to the port P1\_7/IDU input and the port P8\_5 input.

Filter width:  $\frac{(n + 1) \times 8}{f_1}$                       n: the NDDR or P17DDR register setting value

Registers NDDR and P17DDR decrement the setting value as  $f_1$  divided-by-8 is the count source. When reading the NDDR or P17DDR register, the count value is returned. The setting value is reloaded at every falling or rising edge of the pin input.

When using the digital debounce function, the programmable value for the NDDR or P17DDR register is 00h to FFh. When setting FFh to the register, digital debounce filter function is not selected. See Figure 11.8 for details.



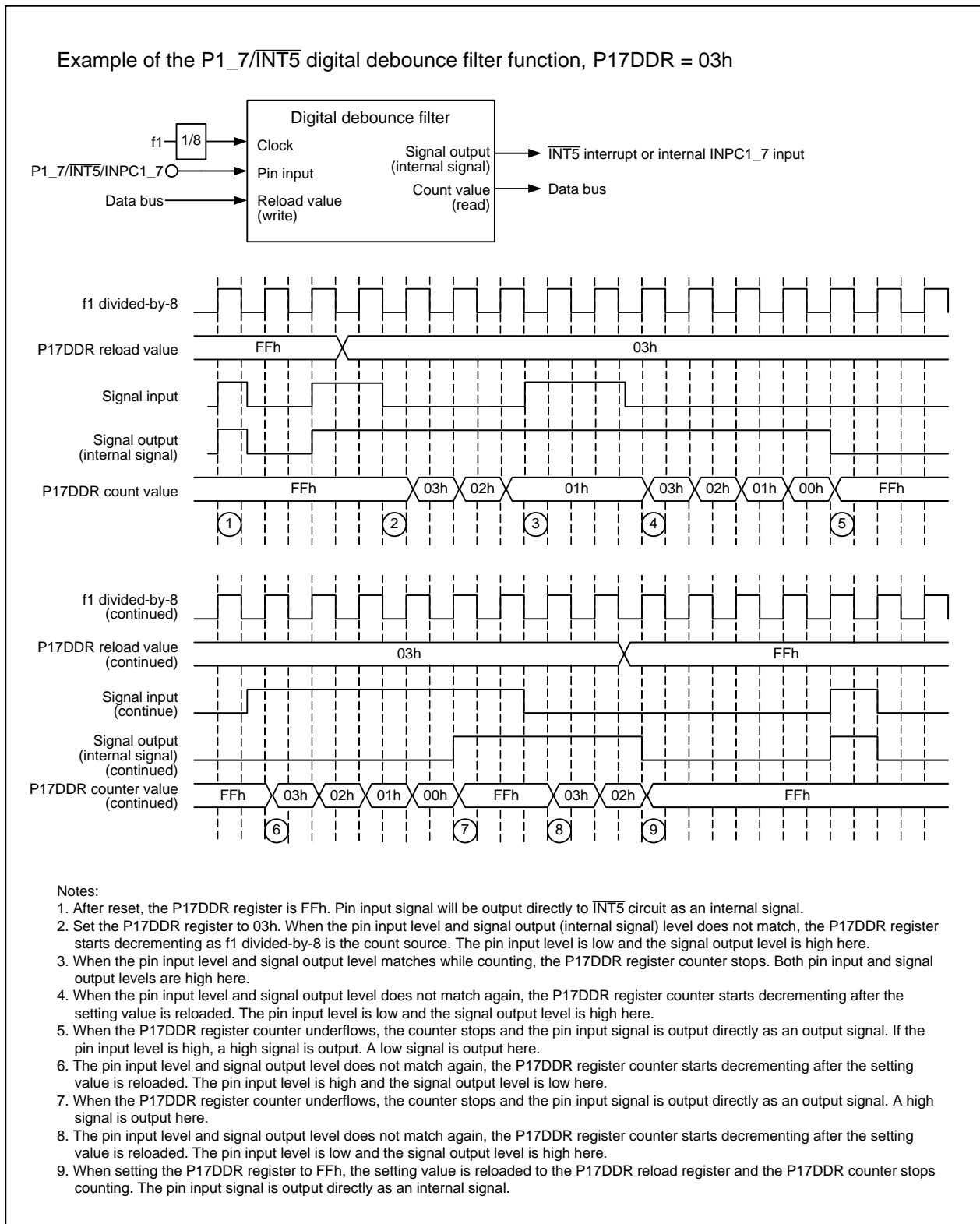


Figure 11.8 Digital Debounce Filter Operation

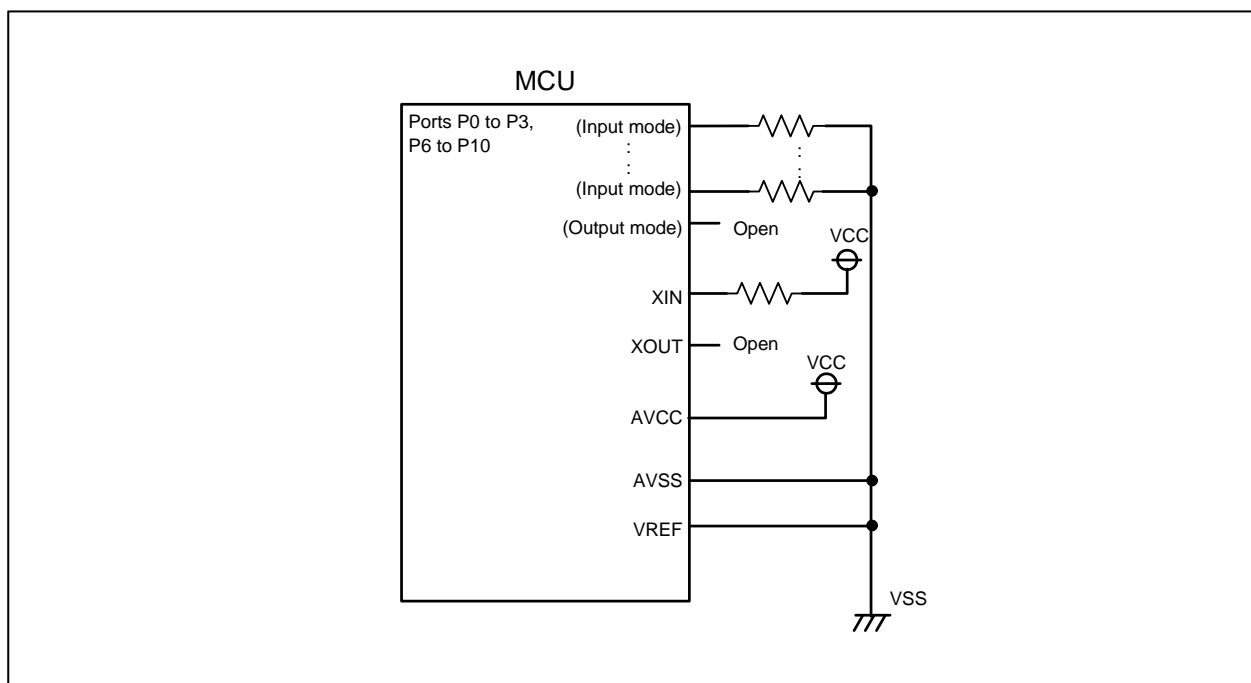
## 11.5 Unassigned Pin Handling

**Table 11.11 Unassigned Pin Handling in Single-Chip Mode**

Pin Name	Connection <sup>(2)</sup>
Ports P0 to P3, P6 to P10	One of the following: <ul style="list-style-type: none"> <li>• Set the pin to input mode and connect a pin to VSS via resistor (pull-down)</li> <li>• Set the pin to input mode and connect a pin to VCC via resistor (pull-up)</li> <li>• Set the pin to output mode and leave the pin open <sup>(1)</sup></li> </ul>
XOUT <sup>(3)</sup>	Open
XIN	Connect to VCC via a resistor (pull-up)
AVCC	Connect to VCC
AVSS, VREF	Connect to VSS

**Notes:**

1. When setting a port to output mode and leaving it open, be aware that the port remains in input mode until it is switched to output mode by a program after reset. For this reason, the voltage level on the pin becomes indeterminate, causing the power supply current to increase while the port remains in input mode.  
Furthermore, since the values of the direction registers can be changed by noise or noise-induced loss of control, it is recommended that the contents of the direction registers be regularly reset in software to improve the program reliability.
2. Make sure unused pins are connected with the shortest possible wiring from the MCU pins (maximum 2 cm).
3. Leave the XOUT pin open when inputting an external clock to the XIN pin or when connecting VCC via a resistor.



**Figure 11.9 Unassigned Pin Handling**

## 11.6 Notes on Programmable I/O Ports

### 11.6.1 Pin Assignment Control

Bits PACR2 to PACR0 in the PACR register are 000b after reset. Set 010b (64-pin package) or 011b (80-pin package) to select the pin package, depending on the product.

After setting bits PACR2 to PACR0, set the programmable I/O ports and I/O pins for peripherals.

### 11.6.2 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/ $\overline{CTS2}$ / $\overline{RTS2}$ /TA1IN/ $\overline{V}$ /TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/ $\overline{W}$ , P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/ $\overline{U}$ /TSUDB

### 11.6.3 Input Voltage Threshold

The input threshold voltage differs in the programmable I/O port and peripherals. When the programmable I/O port and peripheral is sharing the same pin, and the pin input level is lower than  $V_{IH}$  and higher than  $V_{IL}$  (input voltage is neither high or low), the input signal voltage level may be determined differently between the programmable I/O port and peripheral because the input voltage thresholds for those two are not necessarily the same.

## 12. Interrupts

### 12.1 Introduction

Table 12.1 lists Types of Interrupts, and Table 12.2 lists I/O Pins. The pins shown in Table 12.2 are external interrupt input pins. Refer to the peripheral functions for the pins related to the peripheral functions.

**Table 12.1 Types of Interrupts**

Type		Interrupt	Function
Software		Undefined instruction (UND instruction) Overflow (INTO instruction) BRK instruction INT instruction	An interrupt is generated by executing an instruction. Non-maskable interrupt <sup>(2)</sup>
Hardware	Specific	NMI Watchdog timer Oscillator stop/restart detect Voltage monitor 2 Address match Single step <sup>(1)</sup> $\overline{DBC}$ <sup>(1)</sup>	Interrupt by the MCU hardware Non-maskable interrupt <sup>(2)</sup>
	Peripheral function	$\overline{INT}$ , timers, etc. (Refer to 12.6.2 "Relocatable Vector Tables".)	Interrupt by the peripheral functions in the MCU Maskable interrupt (interrupt priority level: 7 levels) <sup>(2)</sup>

Notes:

1. This interrupt is provided exclusively for developers and should not be used.
2. Maskable interrupt: Interrupt status (enabled or disabled) can be selected by the interrupt enable flag (I flag).  
Interrupt priority can be changed by the interrupt priority level.

Non-maskable interrupt: Interrupt status (enabled or disabled) cannot be selected by the interrupt enable flag (I flag).  
Interrupt priority cannot be changed by the interrupt priority level.

**Table 12.2 I/O Pins**

Pin Name	I/O	Function
$\overline{NMI}$	Input <sup>(1)</sup>	$\overline{NMI}$ interrupt input
$\overline{INTi}$	Input <sup>(1)</sup>	$\overline{INTi}$ interrupt input
$\overline{KI0}$ to $\overline{KI3}$	Input <sup>(1)</sup>	Key input

i = 0 to 5

Note:

1. Set the port direction bits which share pins to 0 (input mode).

## 12.2 Registers

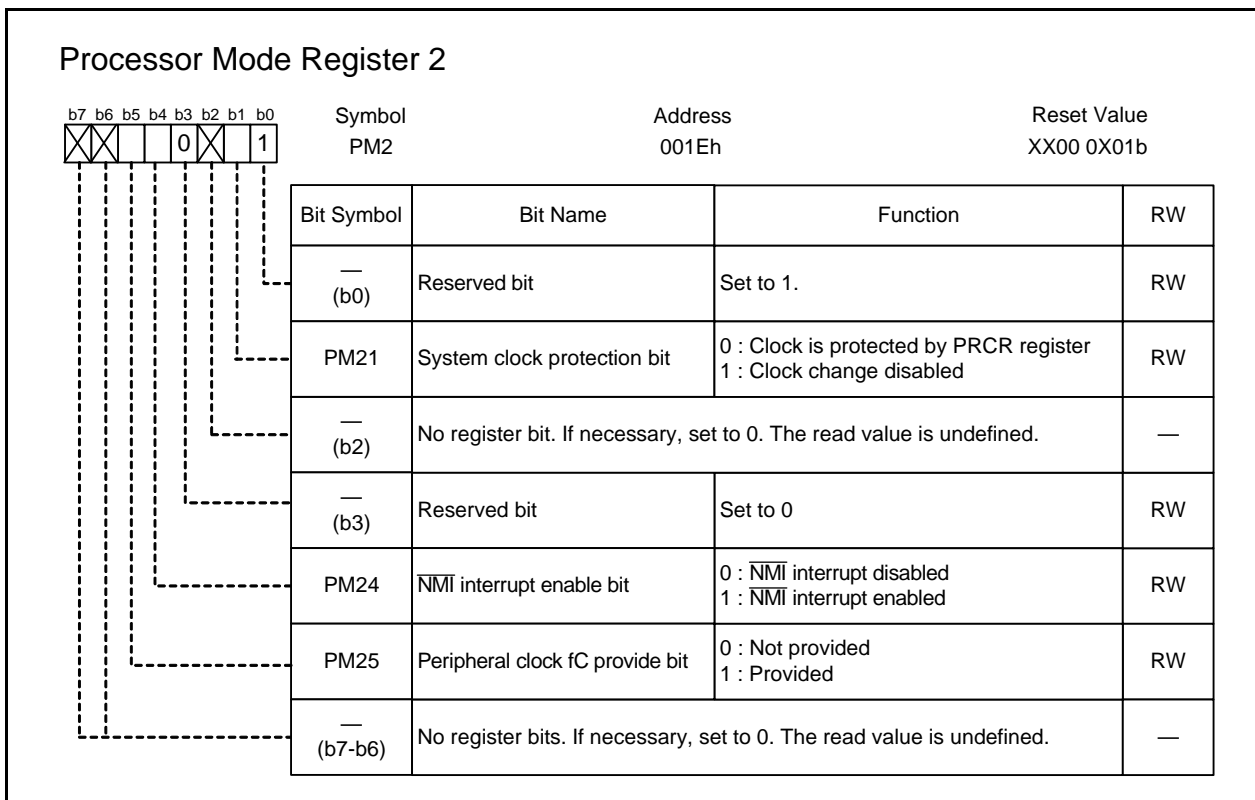
**Table 12.3 Registers (1/2)**

Address	Register	Symbol	Reset Value
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0048h	$\overline{\text{INT5}}$ Interrupt Control Register	INT5IC	XX00 X000b
0049h	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register, Task Monitoring Timer Interrupt Control Register	BCNIC, TMOSIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b

**Table 12.4 Registers (2/2)**

Address	Register	Symbol	Reset Value
006Fh	UART4 Transmit Interrupt Control Register, Real-Time Clock Compare Interrupt Control Register	S4TIC, RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register,CAN0 Error Interrupt Control Register	S3TIC, C0EIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register	RTCTIC	XXXX X000b
0075h	CAN0 Reception Complete Interrupt Control Register	C0RIC	XXXX X000b
0076h	CAN0 Transmission Complete Interrupt Control Register	C0TIC	XXXX X000b
0077h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0078h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I2C-bus Interface Interrupt Control Register	ICOC1IC IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
02FEh	NMI Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh

### 12.2.1 Processor Mode Register 2 (PM2)



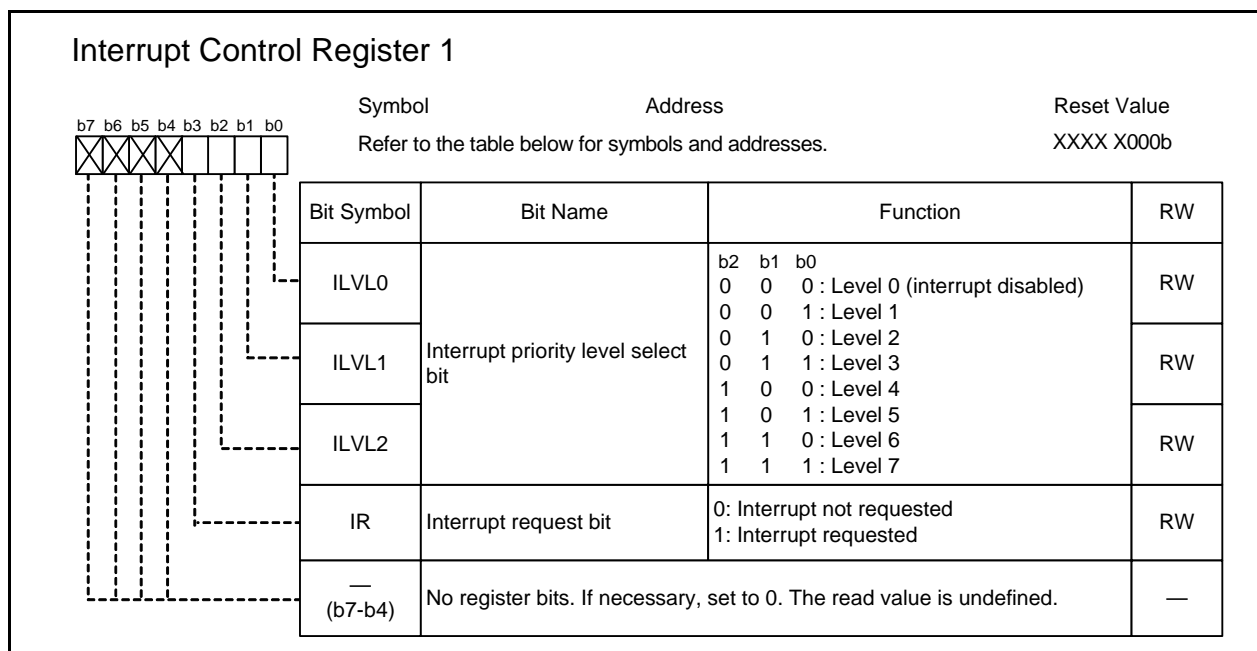
Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.

#### PM24 ( $\overline{\text{NMI}}$ interrupt enable bit) (b4)

Once this bit is set to 1, it cannot be set to 0 by a program (writing 0 has no effect).

## 12.2.2 Interrupt Control Register 1

(BCNIC/TMOSIC, DM0IC to DM3IC, KUPIC,ADIC, S0TIC to S2TIC, S0RIC to S3RIC, TA0IC to TA4IC, TB0IC to TB2IC, S4TIC/RTCCIC, S4RIC, C0WIC,S3TIC/C0EIC, RTCTIC C0RIC, C0TIC, C0FRIC, C0FTIC, ICOC0IC, ICOCH0IC, ICOC1IC/IICIC, ICOCH1IC/SCLDAIC, ICOCH2IC to ICOCH3IC, BTIC)



Symbol	Address
BCNIC/TMOSIC	004Ah
DM0IC	004Bh
DM1IC	004Ch
DM2IC	0069h
DM3IC	006Ah
KUPIC	004Dh
ADIC	004Eh
S0TIC	0051h
S1TIC	0053h
S2TIC	004Fh
S0RIC	0052h
S1RIC	0054h
S2RIC	0050h
S3RIC	0073h

Symbol	Address
TA0IC	0055h
TA1IC	0056h
TA2IC	0057h
TA3IC	0058h
TA4IC	0059h
TB0IC	005Ah
TB1IC	005Bh
TB2IC	005Ch
S4TIC/RTCCIC	006Fh
S4RIC	0070h
C0WIC	0071h
S3TIC/C0EIC	0072h

Symbol	Address
RTCTIC	0074h
C0RIC	0075h
C0TIC	0076h
C0FRIC	0077h
C0FTIC	0078h
ICOC0IC	0079h
ICOCH0IC	007Ah
ICOC1IC/IICIC	007Bh
ICOCH1IC/SCLDAIC	007Ch
ICOCH2IC	007Dh
ICOCH3IC	007Eh
BTIC	007Fh

Rewrite these registers at a point where an interrupt request for the corresponding register is not generated.

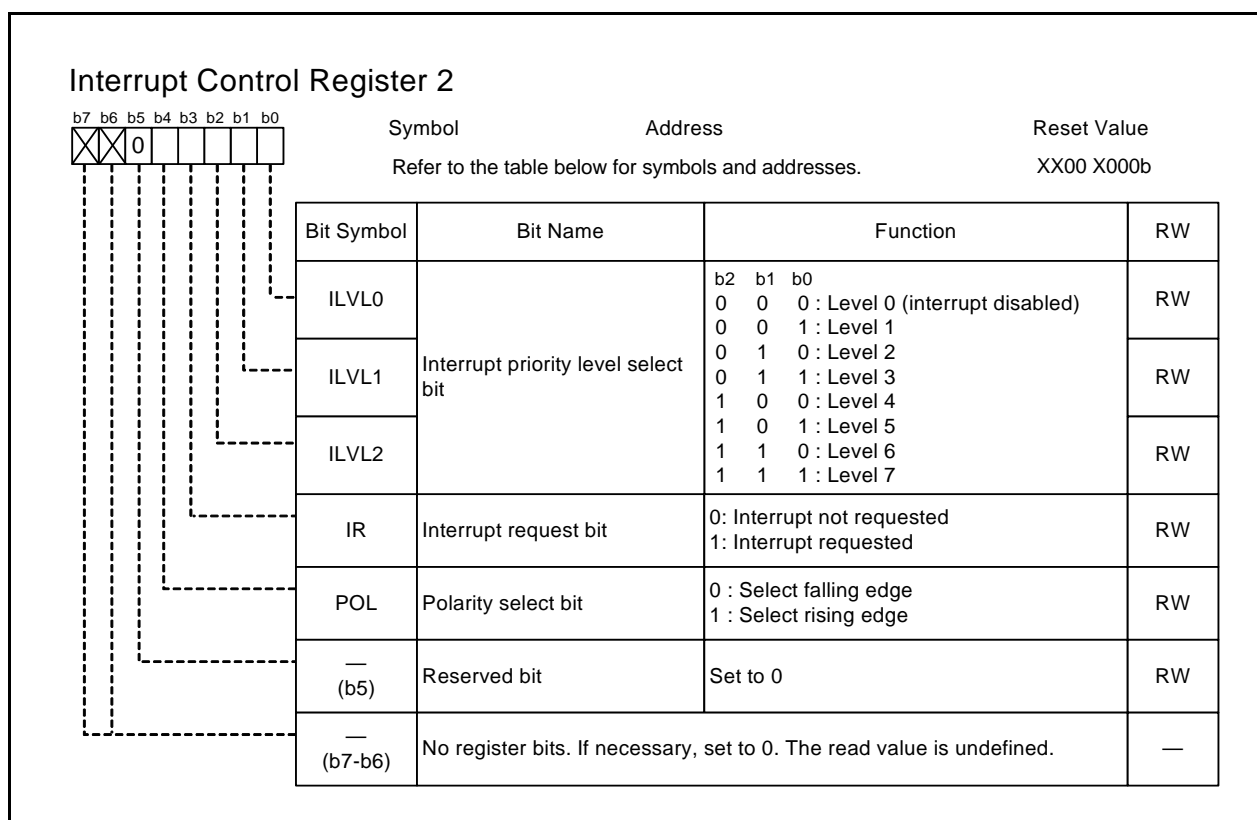
When multiple interrupt sources share the register, select an interrupt source in registers IFSR2A and IFSR3A.

IR (Interrupt request bit) (b3)

Do not set the IR bit to 1 when it is 0.



### 12.2.3 Interrupt Control Register 2 (INT3IC, INT5IC, INT4IC, INT0IC to INT2IC)



Symbol	Address
INT3IC	0044h
INT5IC	0048h
INT4IC	0049h

Symbol	Address
INT0IC	005Dh
INT1IC	005Eh
INT2IC	005Fh

Rewrite these registers at a point where an interrupt request for the corresponding register is not generated.

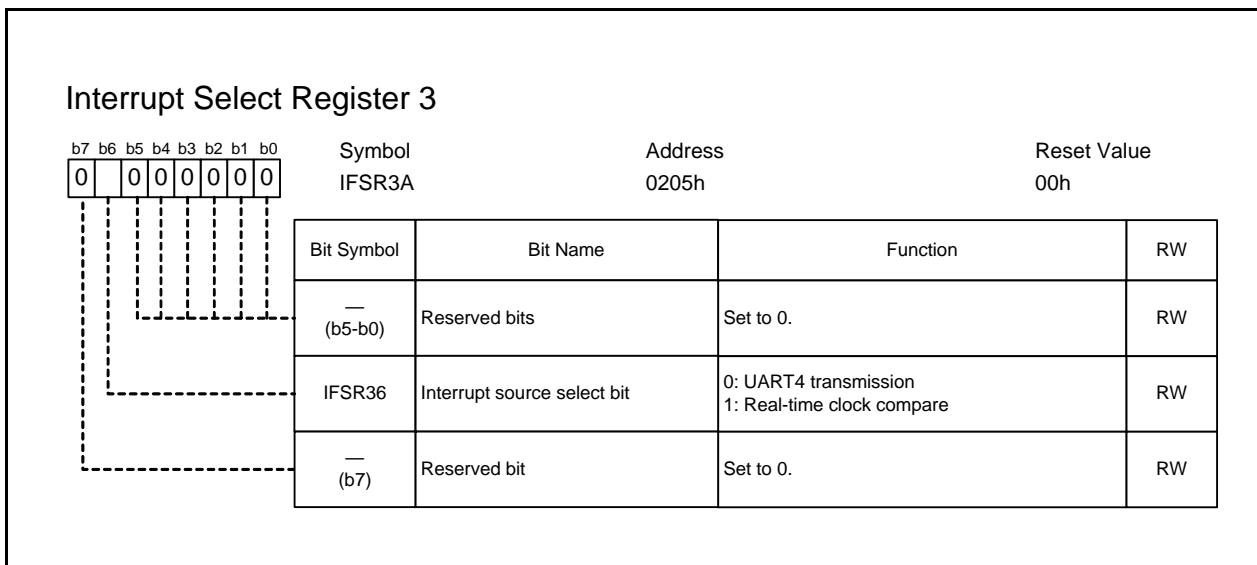
#### IR (Interrupt request bit) (b3)

Do not set the IR bit to 1 when it is 0.

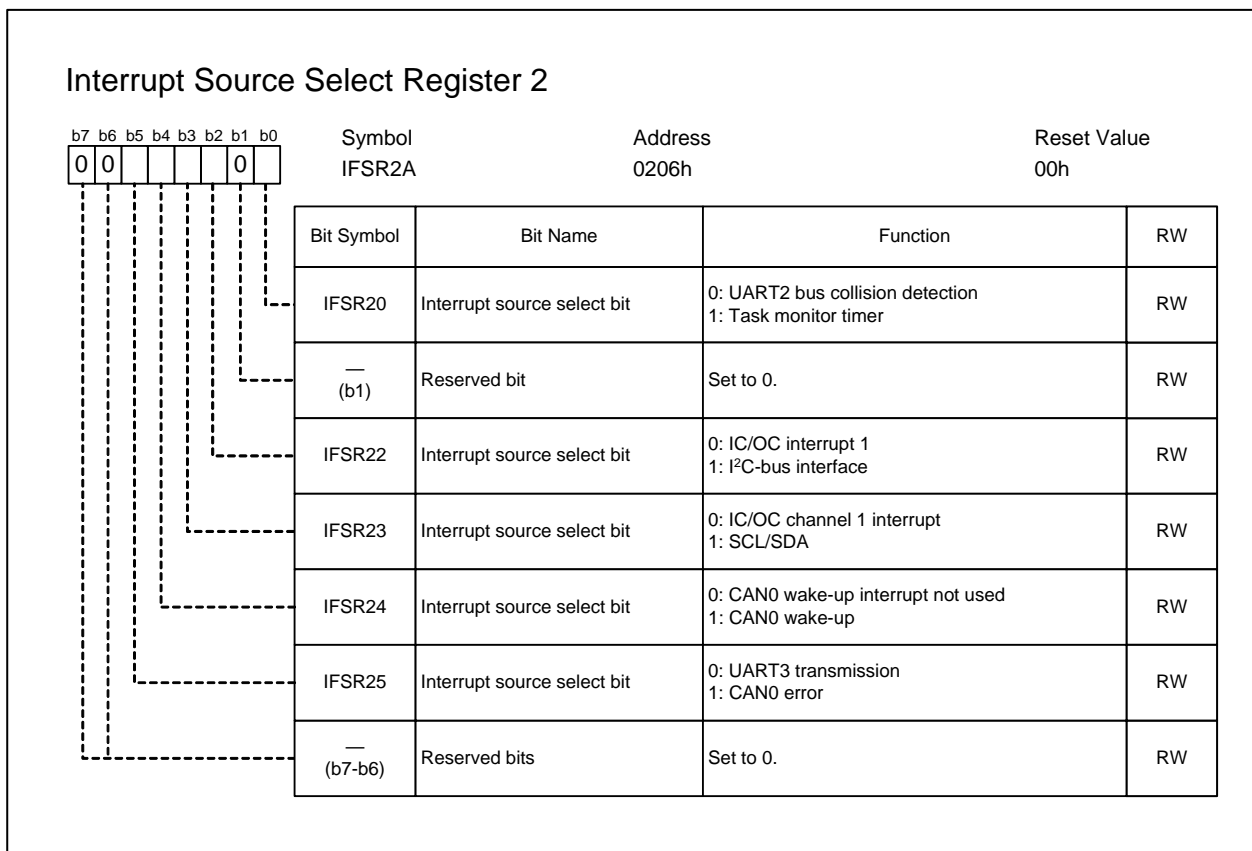
#### POL (Polarity select bit) (b4)

When the IFSR<sub>i</sub> bit in the IFSR register is 1 (both edges), set the POL bit in the INT<sub>i</sub>IC register to 0 (falling edge) (i = 0 to 5).

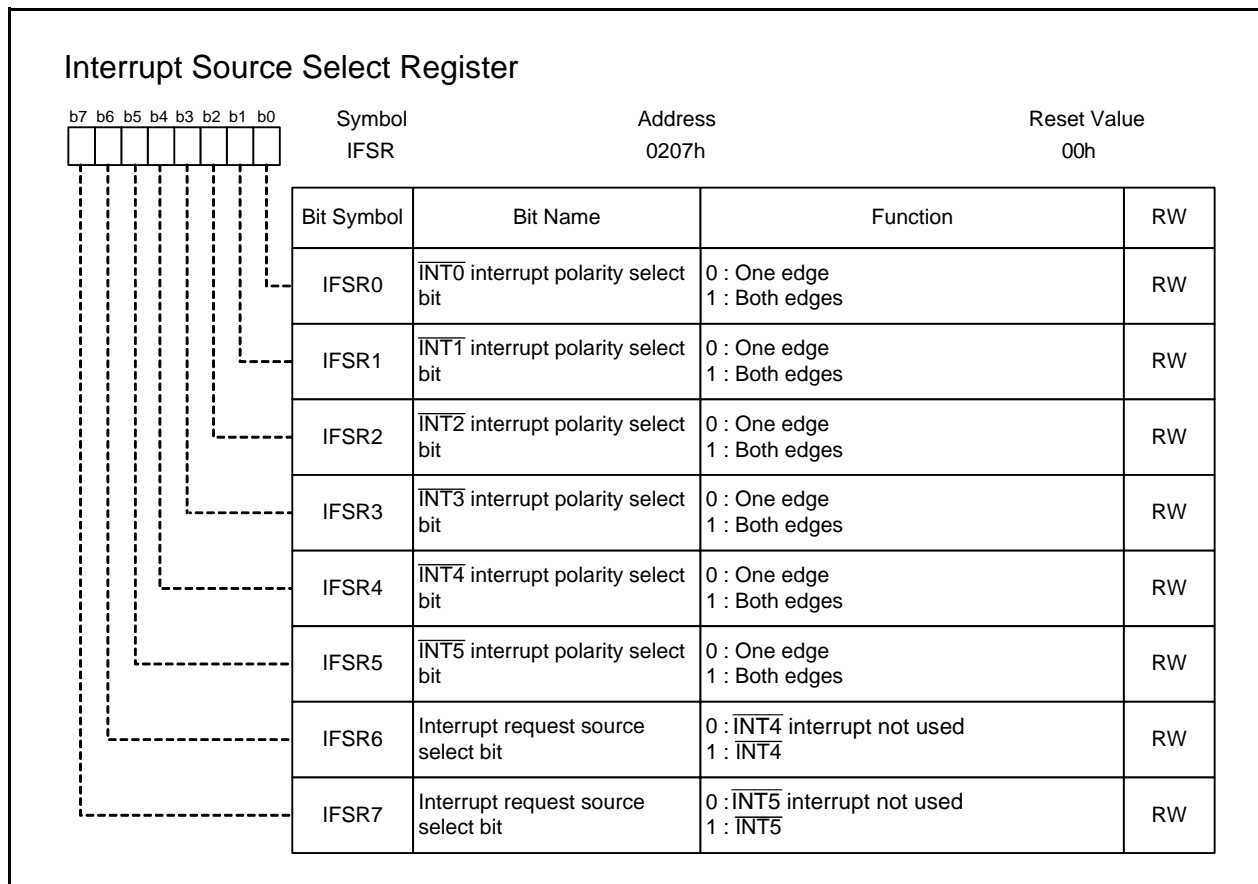
### 12.2.4 Interrupt Source Select Register 3 (IFSR3A)



### 12.2.5 Interrupt Source Select Register 2 (IFSR2A)



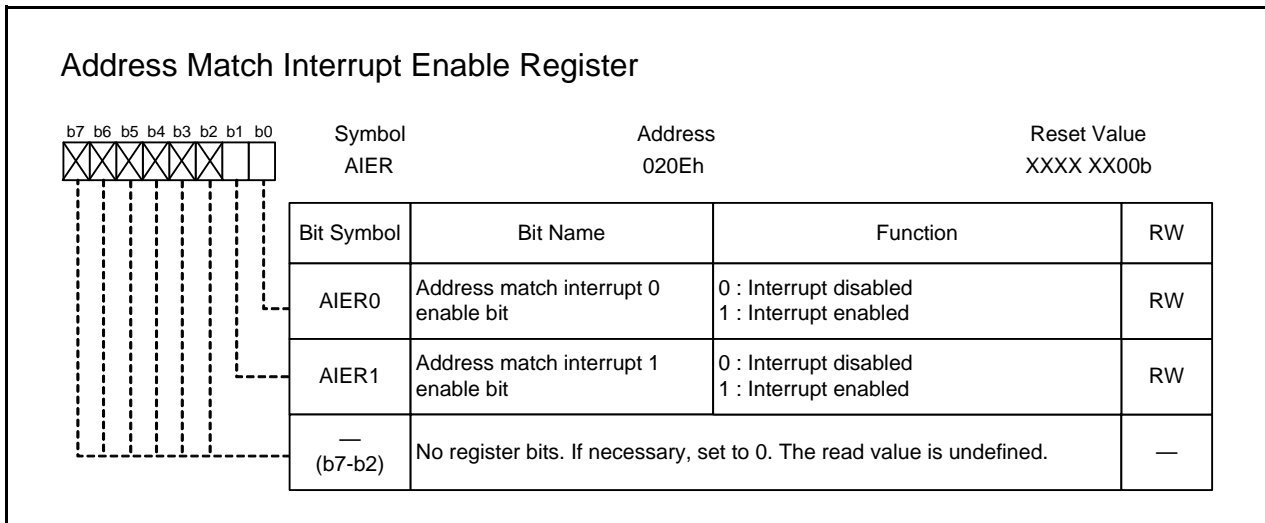
### 12.2.6 Interrupt Source Select Register (IFSR)



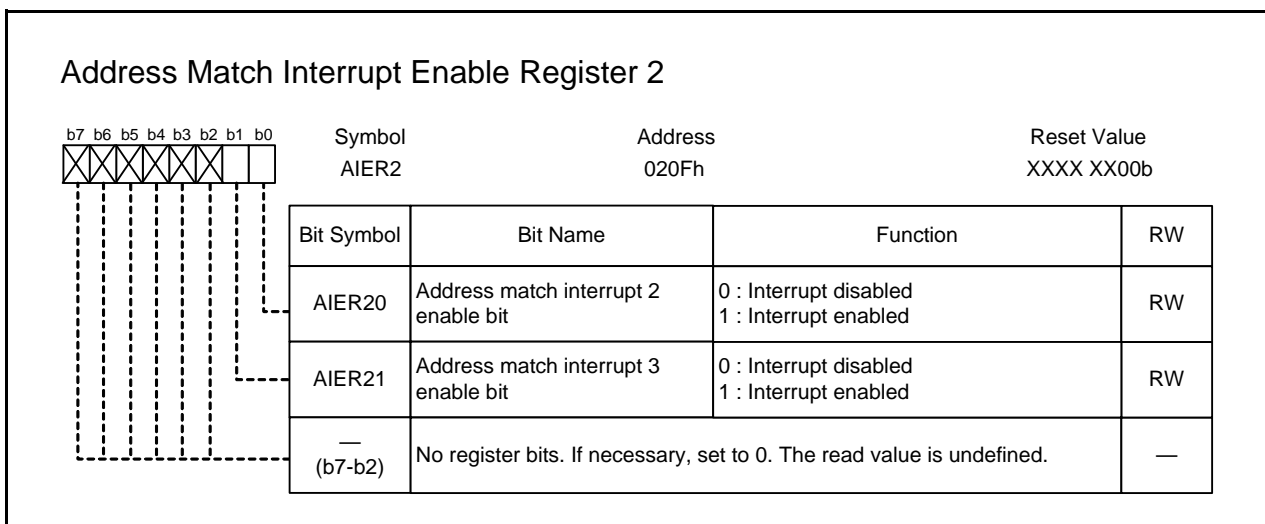
#### IFSR5-IFSR0 ( $\overline{\text{INT5}}$ - $\overline{\text{INT0}}$ interrupt polarity select bit) (b5-b0)

When setting these bits to 1 (both edges), make sure the corresponding POL bit in registers INT0IC to INT5IC is set to 0 (falling edge).

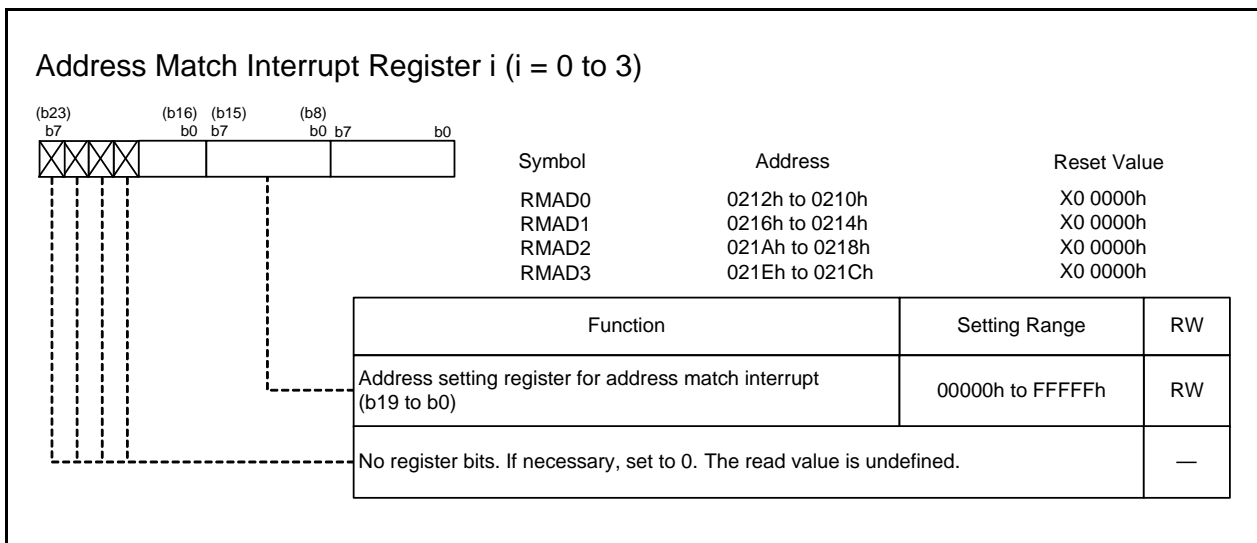
### 12.2.7 Address Match Interrupt Enable Register (AIER)



### 12.2.8 Address Match Interrupt Enable Register 2 (AIER2)



### 12.2.9 Address Match Interrupt Register i (RMADi) (i = 0 to 3)



### 12.2.10 $\overline{\text{NMI}}$ Digital Debounce Register (NDDR)

$\overline{\text{NMI}}$ Digital Debounce Register			
b7 [ ] b0	Symbol NDDR	Address 02FEh	Reset Value FFh
	Function	Setting Range	RW
	With n being the setting value: <ul style="list-style-type: none"> <li>• n = 00h to FEh: A signal with larger pulse width than <math>\frac{(n+1) \times 8}{f_1}</math> is input to <math>\overline{\text{NMI}}/\overline{\text{SD}}</math>.</li> <li>• n = FFh: Digital debounce filter function is disabled and all signals will be input directly.</li> </ul>	00h to FFh	RW

When using the  $\overline{\text{NMI}}$  interrupt to exit from stop mode, set FFh to the NDDR register before entering stop mode. Write to the NDDR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled). No interrupt or DMA transfer should be generated between these two instructions.

### 12.2.11 P1\_7 Digital Debounce Register (P17DDR)

P1_7 Digital Debounce Register			
b7 [ ] b0	Symbol P17DDR	Address 02FFh	Reset Value FFh
	Function	Setting Range	RW
	With n being the setting value: <ul style="list-style-type: none"> <li>• n = 00h to FEh: A signal with larger pulse width than <math>\frac{(n+1) \times 8}{f_1}</math> is input to INPC1_7/ INT5.</li> <li>• n = FFh: Digital debounce filter function is disabled and all signals will be input directly.</li> </ul>	00h to FFh	RW

When using the  $\overline{\text{INT5}}$  interrupt to exit from stop mode, set FFh to the P17DDR register before entering stop mode.

### 12.3 Types of Interrupts

Figure 12.1 shows Types of Interrupts.

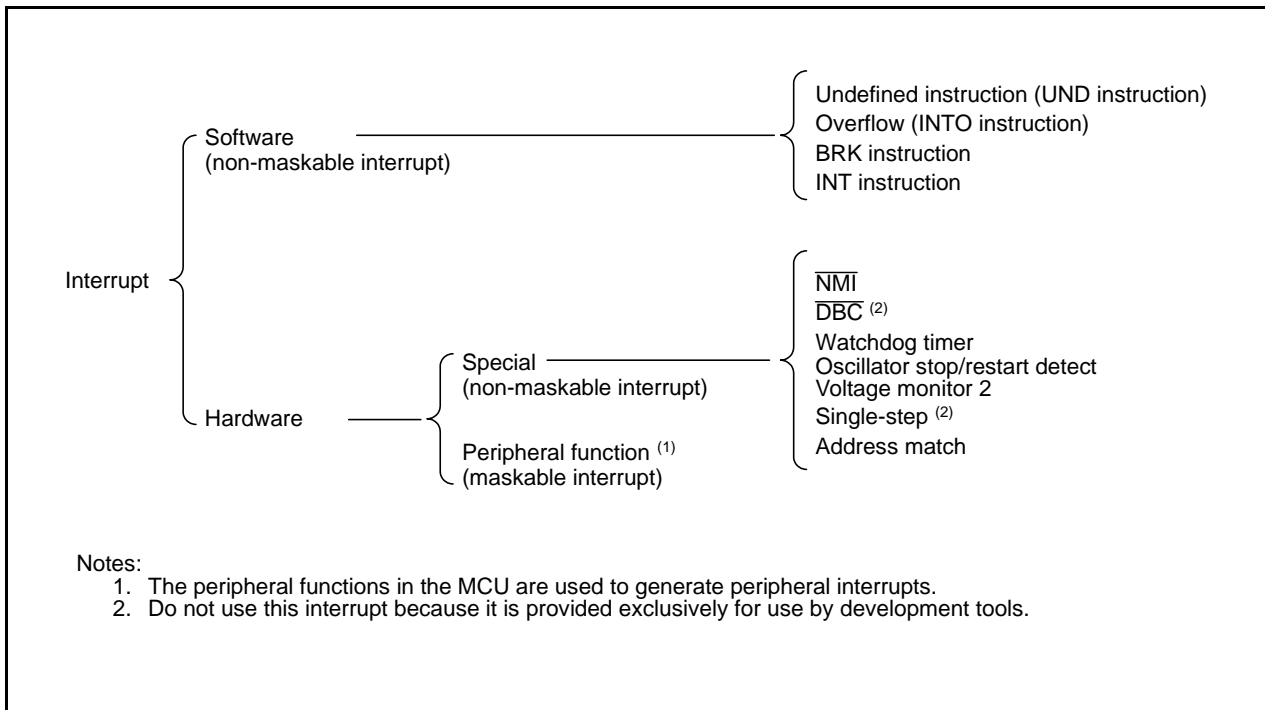


Figure 12.1 Types of Interrupts

- Maskable interrupt : The I flag (interrupt enable flag) **can** enable/disable these interrupts. The interrupt priority order **can be changed** by using the interrupt priority level.
- Non-maskable interrupt : The I flag (interrupt enable flag) **cannot** enable/disable these interrupts. The interrupt priority order **cannot be changed** by using the interrupt priority level.



## 12.4 Software Interrupts

A software interrupt occurs when executing instructions. Software interrupts are non-maskable interrupts.

### 12.4.1 Undefined Instruction Interrupt

An undefined instruction interrupt occurs when executing the UND instruction.

### 12.4.2 Overflow Interrupt

An overflow interrupt occurs when executing the INTO instruction with the O flag in the FLG register set to 1 (the operation resulted in an overflow). The following are instructions whose O flag changes by an arithmetic operation:

ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB

### 12.4.3 BRK Interrupt

A BRK interrupt occurs when the BRK instruction is executed.

### 12.4.4 INT Instruction Interrupt

An INT instruction interrupt occurs when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified for the INT instruction. Because software interrupt numbers 4, 8 to 31, 41, 42, and 47 to 63 are assigned to peripheral function interrupts, the same interrupt routine used for peripheral function interrupts can be executed by executing the INT instruction.

For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and is cleared to 0 (ISP selected) before executing an interrupt sequence. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the SP selected at the time is used.

## 12.5 Hardware Interrupts

Hardware interrupts are classified into two types: special interrupts and peripheral function interrupts.

### 12.5.1 Special Interrupts

Special interrupts are non-maskable interrupts.

#### 12.5.1.1 $\overline{\text{NMI}}$ Interrupt

An  $\overline{\text{NMI}}$  interrupt is generated when input on the  $\overline{\text{NMI}}$  pin changes state from high to low. For details on the  $\overline{\text{NMI}}$  interrupt, refer to 12.9 “ $\overline{\text{NMI}}$  Interrupt”.

#### 12.5.1.2 $\overline{\text{DBC}}$ Interrupt

Do not use this interrupt because it is provided exclusively for use by development tools.

#### 12.5.1.3 Watchdog Timer Interrupt

This interrupt is generated by the watchdog timer. Once a watchdog timer interrupt is generated, be sure to refresh the watchdog timer. For details on the watchdog timer, refer to 13. “Watchdog Timer”.

#### 12.5.1.4 Oscillator Stop/Restart Detect Interrupt

The interrupt is generated by the oscillator stop/restart detect function. For details on this function, refer to 8. “Clock Generator”.

#### 12.5.1.5 Voltage Monitor 2 Interrupt

The interrupt is generated by the voltage detector. For details on the voltage detector, refer to 7. “Voltage Detector”.

#### 12.5.1.6 Single-Step Interrupt

Do not use this interrupt because it is provided exclusively for use by development tools.

#### 12.5.1.7 Address Match Interrupt

When the AIER0 or AIER1 bit in the AIER register, or the AIER20 or AIER21 bit in the AIER2 register is 1 (address match interrupt enabled), an address match interrupt is generated immediately before executing an instruction at the address indicated by the corresponding registers RMAD0 to RMAD3. For details on the address match interrupt, refer to 12.11 “Address Match Interrupt”.

### 12.5.2 Peripheral Function Interrupts

A peripheral function interrupt occurs when a request from a peripheral function in the MCU is acknowledged. Peripheral function interrupts are maskable interrupts. See Table 12.6 and Table 12.7 “Relocatable Vector Tables”. Refer to the descriptions of each function for details on how the corresponding peripheral function interrupt is generated.

## 12.6 Interrupts and Interrupt Vectors

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows an Interrupt Vector.

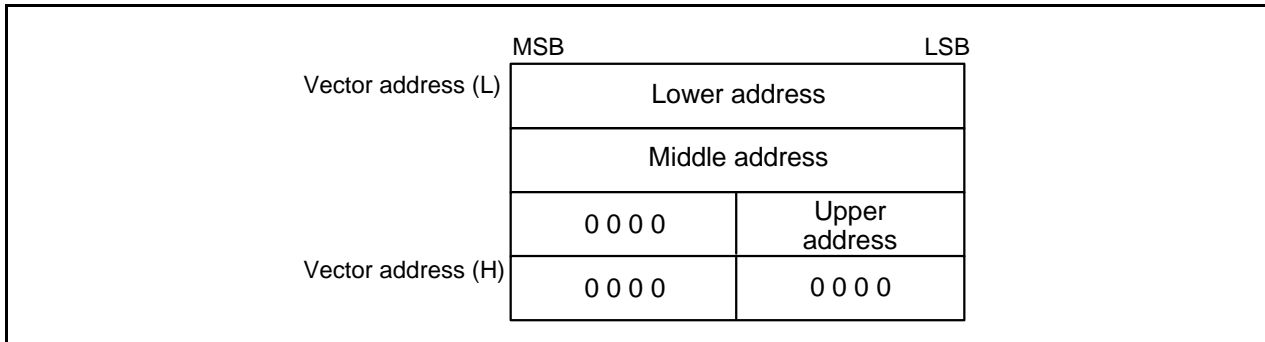


Figure 12.2 Interrupt Vector

### 12.6.1 Fixed Vector Tables

The fixed vector tables are allocated to addresses from FFFDCh to FFFFFh. Table 12.5 lists the Fixed Vector Tables. In the flash memory MCU version, the vector addresses (H) of fixed vectors are used for the ID code check function and OFS1 address. For details, refer to 26. "Flash Memory".

Table 12.5 Fixed Vector Tables

Interrupt Source	Vector Table Addresses Address (L) to Address (H)	Reference
Undefined instruction (UND instruction)	FFFDCh to FFFDFh	M16C/60, M16C/20, M16C/Tiny Series Software Manual
Overflow (INTO instruction)	FFFE0h to FFFE3h	
BRK instruction (2)	FFFE4h to FFFE7h	
Address match	FFFE8h to FFFEBh	12.11 "Address Match Interrupt"
Single-step (1)	FFFECh to FFFEFh	-
Watchdog timer, oscillator stop/restart detect, voltage monitor 2	FFFF0h to FFFF3h	13. "Watchdog Timer" 8. "Clock Generator" 7. "Voltage Detector"
$\overline{\text{DBC}}$ (1)	FFFF4h to FFFF7h	-
NMI	FFFF8h to FFFFBh	12.9 "NMI Interrupt"
Reset	FFFFCh to FFFFFh	6. "Resets"

Notes:

- Do not use this interrupt because it is provided exclusively for use by development tools.
- If the value of address FFFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.

### 12.6.2 Relocatable Vector Tables

The 256 bytes beginning with the start address set in the INTB register compose a relocatable vector table area. Setting an even address in the INTB register results in the interrupt sequence being executed faster than setting an odd address.

**Table 12.6 Relocatable Vector Tables (1/2)**

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Reference
INT instruction interrupt (5)	+0 to +3 (0000h to 0003h) to +252 to +255 (00FCh to 00FFh)	0 to 63	M16C/60, M16C/20, M16C/Tiny Series Software Manual
BRK instruction (5)	+0 to +3 (0000h to 0003h)	0	
- (Reserved)	+4 to +7 (0004h to 0007h)	1	
- (Reserved)	+8 to +11 (0008h to 000Bh)	2	
- (Reserved)	+12 to +15 (000Ch to 000Fh)	3	
INT3	+16 to +19 (0010h to 0013h)	4	12.8 "INT Interrupt"
- (Reserved)	+20 to +23 (0014h to 0017h)	5	
- (Reserved)	+24 to +27 (0018h to 001Bh)	6	
- (Reserved)	+28 to +31 (001Ch to 001Fh)	7	
INT5 (2)	+32 to +35 (0020h to 0023h)	8	12.8 "INT Interrupt"
INT4 (3)	+36 to +39 (0024h to 0027h)	9	
UART2 bus collision detection (6), task monitor timer (7)	+40 to +43 (0028h to 002Bh)	10	21. "Serial Interface UARTi (i = 0 to 4)" 19. "Task Monitor Timer"
DMA0	+44 to +47 (002Ch to 002Fh)	11	14. "DMAC"
DMA1	+48 to +51 (0030h to 0033h)	12	
Key input interrupt	+52 to +55 (0034h to 0037h)	13	12.10 "Key Input Interrupt"
A/D converter	+56 to +59 (0038h to 003Bh)	14	24. "A/D Converter"
UART2 transmit, NACK2 (4)	+60 to +63 (003Ch to 003Fh)	15	21. "Serial Interface UARTi (i = 0 to 4)"
UART2 receive, ACK2 (4)	+64 to +67 (0040h to 0043h)	16	
UART0 transmit	+68 to +71 (0044h to 0047h)	17	
UART0 receive	+72 to +75 (0048h to 004Bh)	18	
UART1 transmit	+76 to +79 (004Ch to 004Fh)	19	
UART1 receive	+80 to +83 (0050h to 0053h)	20	
Timer A0	+84 to +87 (0054h to 0057h)	21	15. "Timer A"
Timer A1	+88 to +91 (0058h to 005Bh)	22	
Timer A2	+92 to +95 (005Ch to 005Fh)	23	
Timer A3	+96 to +99 (0060h to 0063h)	24	
Timer A4	+100 to +103 (0064h to 0067h)	25	16. "Timer B"
Timer B0	+104 to +107 (0068h to 006Bh)	26	
Timer B1	+108 to +111 (006Ch to 006Fh)	27	
Timer B2	+112 to +115 (0070h to 0073h)	28	

Notes:

- Address relative to address in INTB.
- Set the IFSR7 bit in the IFSR register to 1.
- Set the IFSR6 bit in the IFSR register to 1.
- In I<sup>2</sup>C mode, NACK and ACK are interrupt sources.
- These interrupts cannot be disabled using the I flag.
- Bus collision detection: In IE mode, bus collision detection is the interrupt source. In I<sup>2</sup>C mode, however, start condition or a stop condition detection are the interrupt sources.
- Use the IFSR20 bit in the IFSR2A register to select.

**Table 12.7 Relocatable Vector Tables (2/2)**

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Reference
INT0	+116 to +119 (0074h to 0077h)	29	12.8 "INT Interrupt"
INT1	+120 to +123 (0078h to 007Bh)	30	
INT2	+124 to +127 (007Ch to 007Fh)	31	
DMA2	+164 to +167 (00A4h to 00A7h)	41	14. "DMAC"
DMA3	+168 to +171 (00A8h to 00ABh)	42	
- (Reserved)	+172 to +175 (00ACh to 00AFh)	43	
- (Reserved)	+176 to +179 (00B0h to 00B3h)	44	
- (Reserved)	+180 to +183 (00B4h to 00B7h)	45	
- (Reserved)	+184 to +187 (00B8h to 00BBh)	46	
UART4 transmit, real-time clock compare (2)	+188 to +191 (00BCh to 00BFh)	47	21. "Serial Interface UARTi (i = 0 to 4)" 20. "Real-Time Clock"
UART4 receive	+192 to +195 (00C0h to 00C3h)	48	
CAN0 wake-up	+196 to +199 (00C4h to 00C7h)	49	23. "CAN Module"
UART3 transmit, CAN0 error (4)	+200 to +203 (00C8h to 00CBh)	50	21. "Serial Interface UARTi (i = 0 to 4)"
UART3 receive	+204 to +207 (00CCh to 00CFh)	51	
Real-time clock cycle	+208 to +211 (00D0h to 00D3h)	52	20. "Real-Time Clock"
CAN0 reception complete	+212 to +215 (00D4h to 00D7h)	53	23. "CAN Module"
CAN0 transmission complete	+216 to +219 (00D8h to 00DBh)	54	
CAN0 receive FIFO	+220 to +223 (00DCh to 00DFh)	55	
CAN0 transmit FIFO	+224 to +227 (00E0h to 00E3h)	56	
IC/OC interrupt 0 (0 to 7)	+228 to +231 (00E4h to 00E7h)	57	18. "Timer S" 22. "Multi-master I <sup>2</sup> C-bus Interface"
IC/OC channel 0	+232 to +235 (00E8h to 00EBh)	58	
IC/OC interrupt 1 (0 to 7), I <sup>2</sup> C-bus interrupt (3)	+236 to +239 (00ECh to 00EFh)	59	
IC/OC channel 1, SCL/SDA interrupt (5)	+240 to +243 (00F0h to 00F3h)	60	
IC/OC channel 2	+244 to +247 (00F4h to 00F7h)	61	
IC/OC channel 3	+248 to +251 (00F8h to 00FBh)	62	
IC/OC base timer	+252 to +255 (00FCh to 00FFh)	63	

## Notes:

1. Address relative to address in INTB.
2. Use the IFSR36 bit in the IFSR3A register to select.
3. Use the IFSR22bit in the IFSR2A register to select.
4. Use the IFSR25 bit in the IFSR2A register to select.
5. Use the IFSR23 bit in the IFSR2A register to select.

## 12.7 Interrupt Control

### 12.7.1 Maskable Interrupt Control

The settings for enabling/disabling the maskable interrupts and of the acceptance priority are explained below. Note that these explanations do not apply to non-maskable interrupts.

Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

#### 12.7.1.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

#### 12.7.1.2 IR Bit

The IR bit becomes 1 (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted, the IR bit becomes 0 (interrupt not requested).

The IR bit can be set to 0 by a program. Do not write 1 to this bit.

#### 12.7.1.3 Bits ILVL2 to ILVL0 and IPL

Interrupt priority levels can be selected by setting bits ILVL2 to ILVL0.


Table 12.8 lists the Settings of Interrupt Priority Levels and Table 12.9 lists the Interrupt Priority Levels Enabled by IPL.

An interrupt request is accepted under the following conditions.

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

**Table 12.8 Settings of Interrupt Priority Levels**

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	-
001b	Level 1	Low  High
010b	Level 2	
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	

**Table 12.9 Interrupt Priority Levels Enabled by IPL**

IPL	Enabled Interrupt Priority Levels
000b	Level 1 and above are enabled
001b	Level 2 and above are enabled
010b	Level 3 and above are enabled
011b	Level 4 and above are enabled
100b	Level 5 and above are enabled
101b	Level 6 and above are enabled
110b	Level 7 and above are enabled
111b	All maskable interrupts are disabled

### 12.7.2 Interrupt Sequence

The interrupt sequence is explained here. The sequence starts when an interrupt request is accepted and ends when the interrupt routine is executed.

When an interrupt request occurs during execution of an instruction, the processor determines its priority after the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. However, if an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR, or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

The CPU behavior during the interrupt sequence is described below. Figure 12.3 shows Time Required for Executing Interrupt Sequence.

- (1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. Then, the IR bit applicable to the interrupt information is set to 0 (interrupt not requested).
- (2) The FLG register, prior to the interrupt sequence, is saved to a temporary register <sup>(1)</sup> within the CPU.
- (3) Flags I, D, and U in the FLG register are set as follows:  
The I flag is set to 0 (interrupt disabled)  
The D flag is set to 0 (single-step interrupt disabled).  
The U flag is set to 0 (ISP selected).  
Note that the U flag does not change states when an INT instruction for software interrupt numbers 32 to 63 is executed.
- (4) The temporary register <sup>(1)</sup> within the CPU is saved on the stack.
- (5) The PC is saved on the stack.
- (6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
- (7) The start address of the relevant interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt routine.

#### Note:

1. Temporary registers cannot be modified by the user.

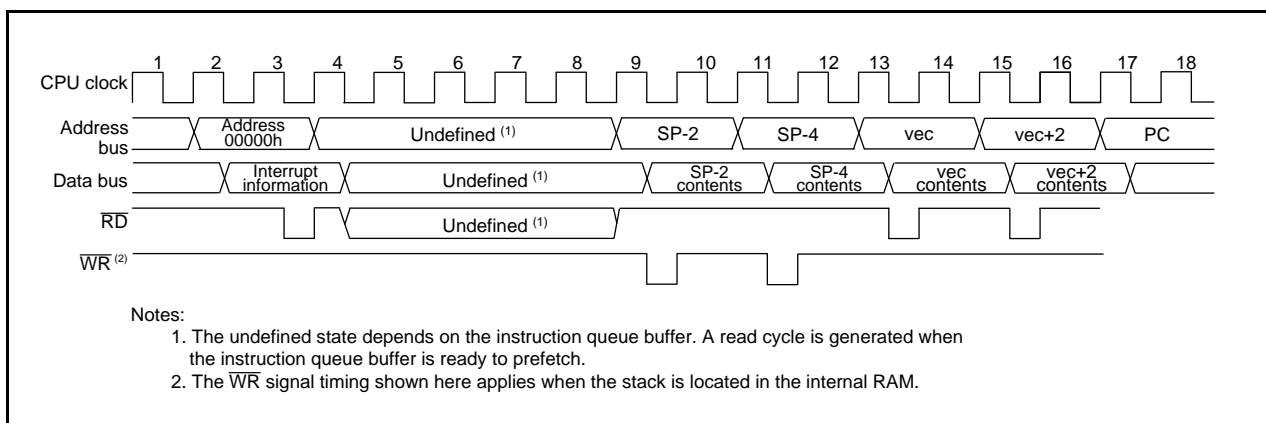


Figure 12.3 Time Required for Executing Interrupt Sequence

### 12.7.3 Interrupt Response Time

Figure 12.4 shows the Interrupt Response Time. The interrupt response or interrupt acknowledge time denotes the time from when an interrupt request is generated until the first instruction in the interrupt routine is executed. Specifically, it consists of the time from when an interrupt request is generated until the executing instruction is completed ((a) in Figure 12.4) and the time during which the interrupt sequence is executed ((b) in Figure 12.4).

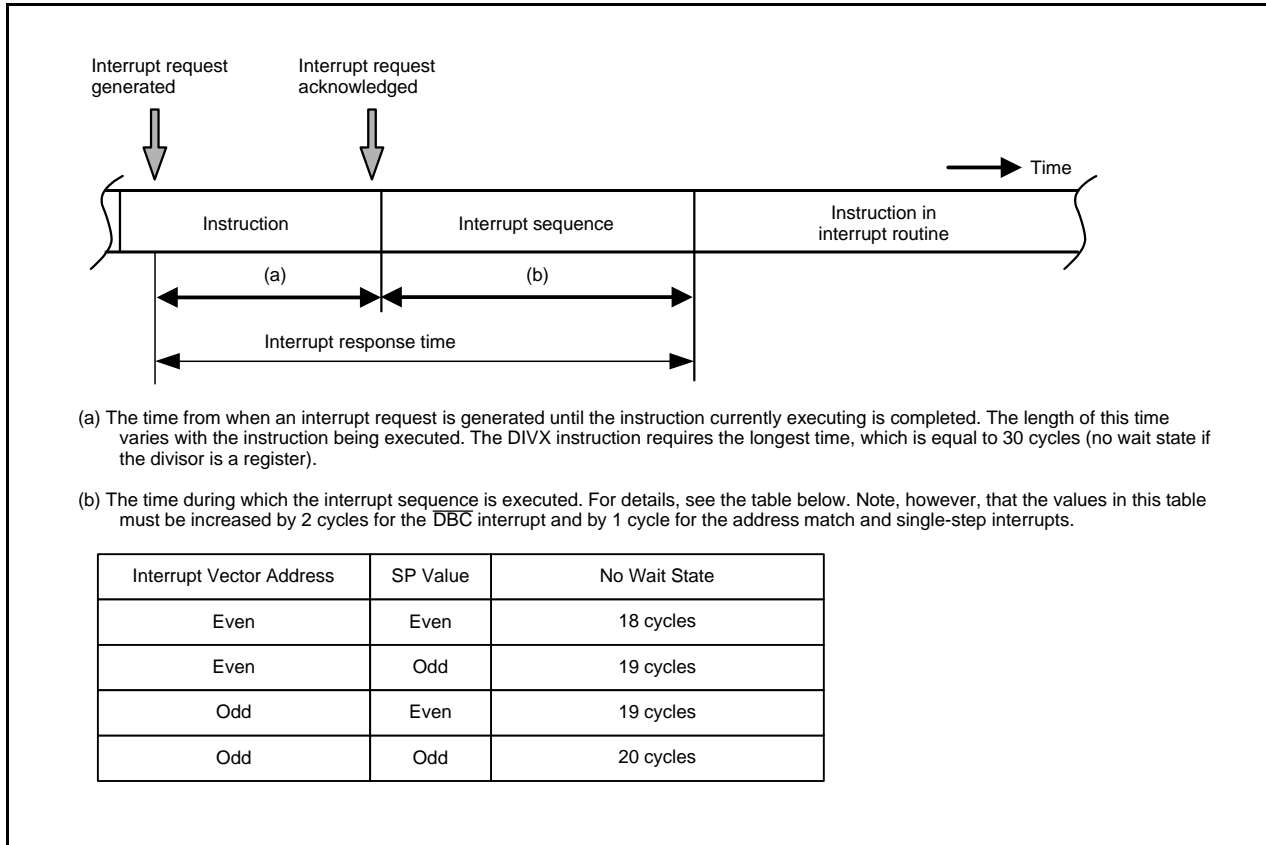


Figure 12.4 Interrupt Response Time

### 12.7.4 Variation of IPL When Interrupt Request is Accepted

When a maskable interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

When a software interrupt or special interrupt request is accepted, one of the interrupt priority levels listed in Table 12.10 is set in the IPL. Table 12.10 lists the IPL Level Set in IPL When Software or Special Interrupt is Accepted.

Table 12.10 IPL Level Set in IPL When Software or Special Interrupt is Accepted

Interrupt Source	Level Set in IPL
Watchdog timer, $\overline{NMI}$ , oscillator stop/restart detect, voltage monitor 2	7
Software, address match, $\overline{DBC}$ , single-step	Not changed

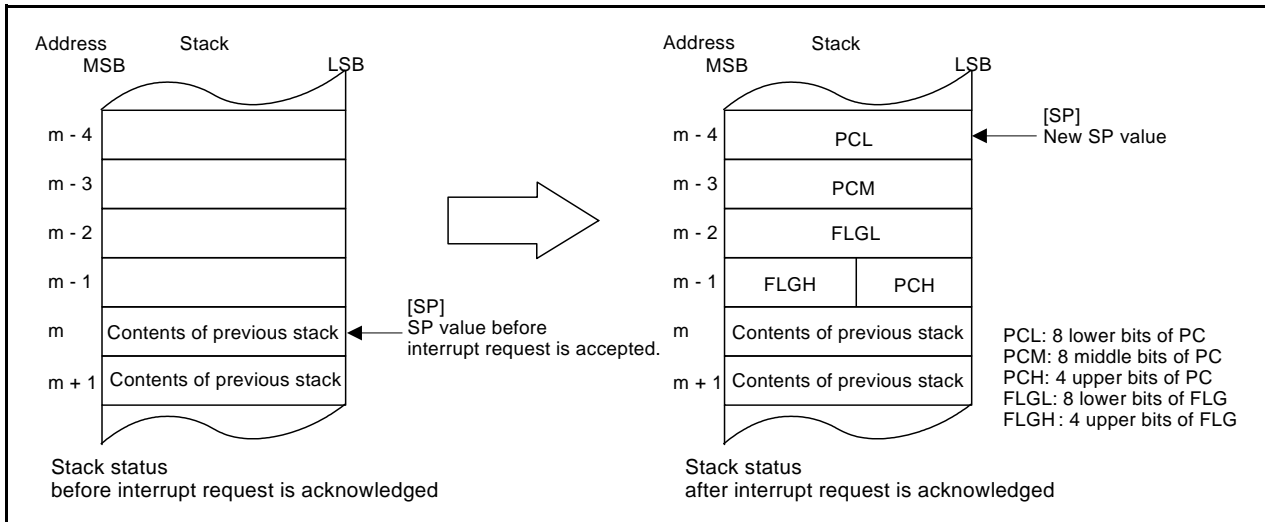


### 12.7.5 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.

At this time, the 4 upper bits of the PC and the 4 upper (IPL) and 8 lower bits in the FLG register, 16 bits in total, are saved on the stack first. Next, the 16 lower bits of the PC are saved. Figure 12.5 shows the Stack Status Before and After Acceptance of Interrupt Request.

The other necessary registers must be saved by a program at the beginning of the interrupt routine. Use the PUSHM instruction, and all registers except SP can be saved with a single instruction.

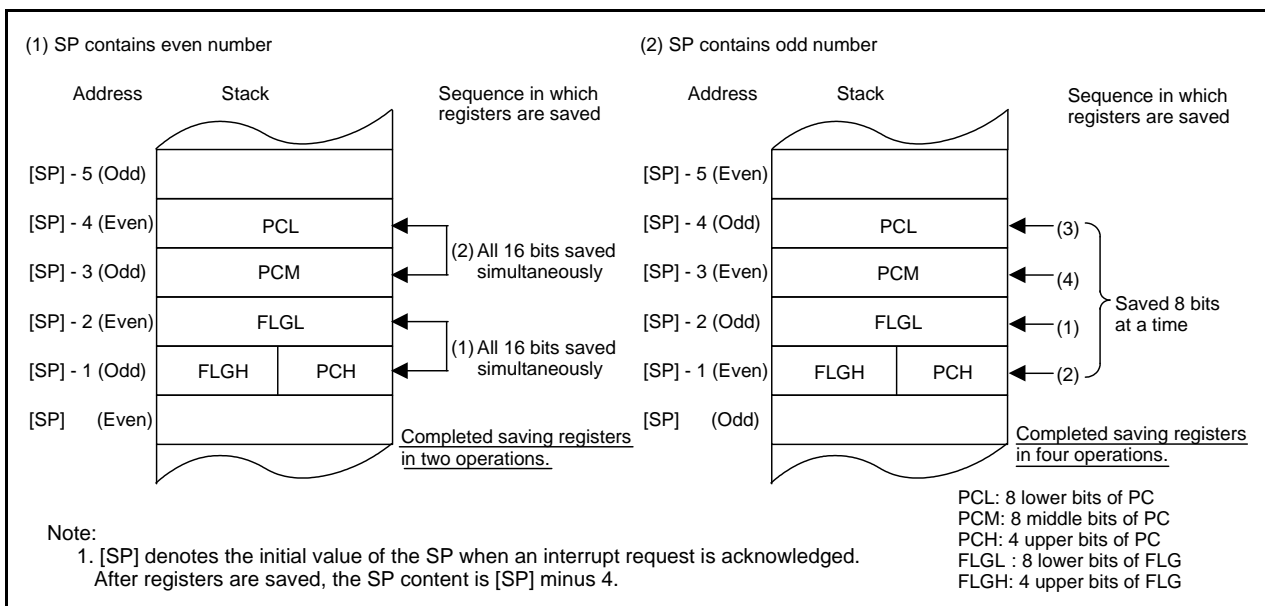


**Figure 12.5 Stack Status Before and After Acceptance of Interrupt Request**

The register save operation carried out in the interrupt sequence is dependent on whether the SP (1), at the time of acceptance of an interrupt request, is even or odd. If the SP (1) is even, the FLG register and the PC are saved 16 bits at a time. If odd, they are saved in two steps, 8 bits at a time. Figure 12.6 shows the Register Save Operation.

Note:

1. When an INT instruction with software numbers 32 to 63 has been executed, it is the SP indicated by the U flag. Otherwise, it is the ISP.



**Figure 12.6 Register Save Operation**

### 12.7.6 Returning from an Interrupt Routine

The FLG register and PC saved in the stack immediately before entering the interrupt sequence are restored from the stack by executing the REIT instruction at the end of the interrupt routine. Then, the CPU returns to the program which was being executed before the interrupt request was accepted.

Restore the other registers saved by a program within the interrupt routine using the POPM or a similar instruction before executing the REIT instruction.

The register bank is switched back to the bank used prior to the interrupt sequence by the REIT instruction.

### 12.7.7 Interrupt Priority

If two or more interrupt requests occur at the same sampling points (the point in time at which interrupt requests are detected), the interrupt with the highest priority is acknowledged.

For maskable interrupts (peripheral function interrupts), any priority level can be selected using bits ILVL2 to ILVL0. However, if two or more maskable interrupts have the same priority level, their interrupt priority is selected by hardware, with the highest priority interrupt accepted.

The watchdog timer interrupt and other special interrupts have their priority levels set in hardware. Figure 12.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. When an instruction is executed, control always branches to the interrupt routine.

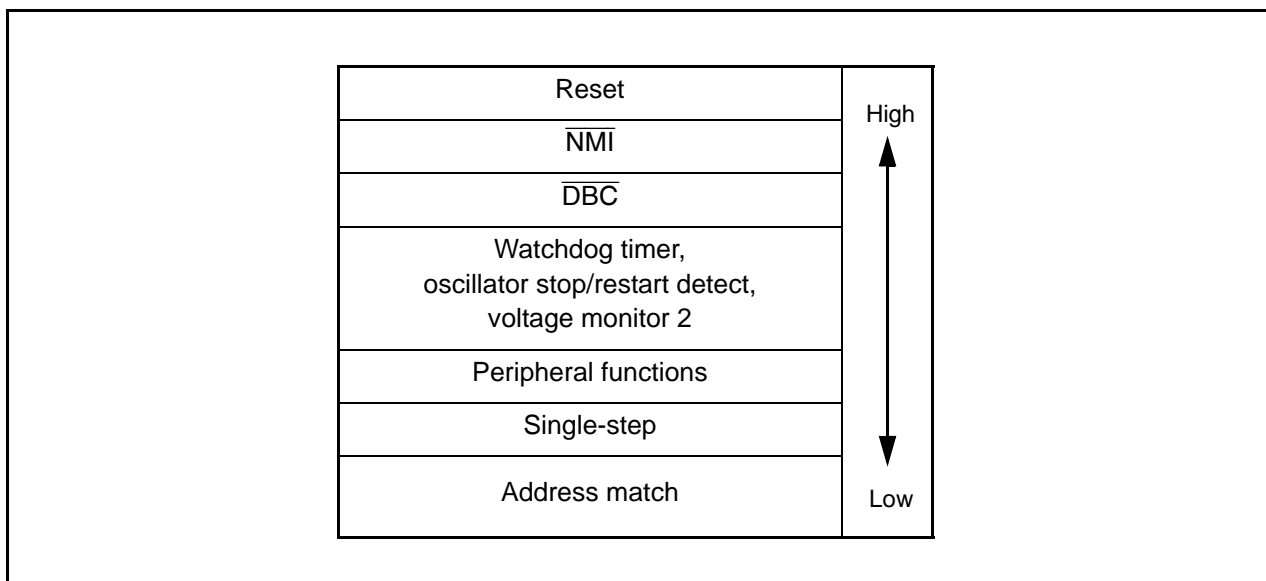


Figure 12.7 Hardware Interrupt Priority

### 12.7.8 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt among sampled interrupt requests at the same sampling point.

Figure 12.8 shows the Interrupt Priority Select Circuit.

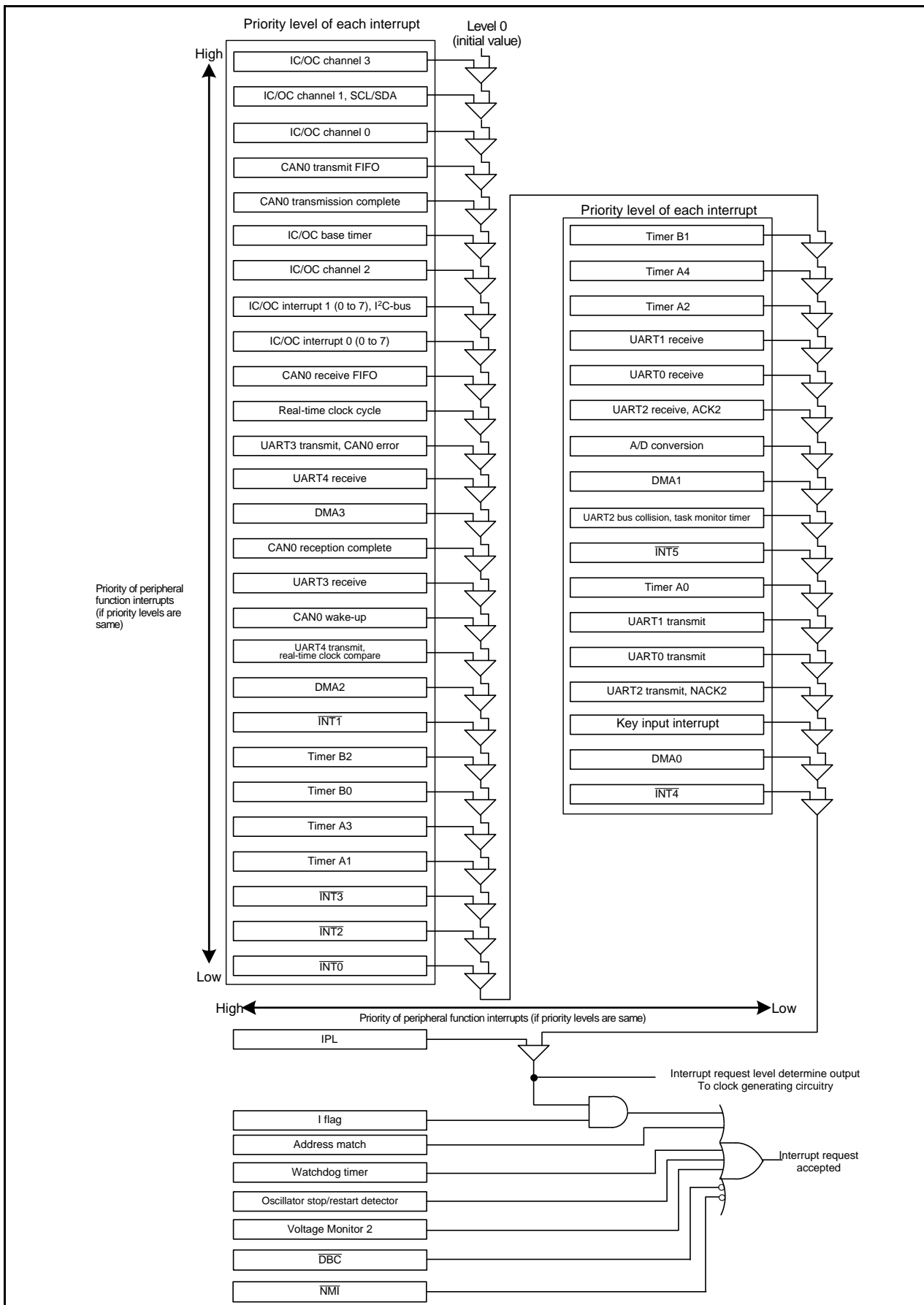


Figure 12.8 Interrupt Priority Select Circuit

### 12.7.9 Multiple Interrupts

The following shows the internal bit states when control has branched to an interrupt routine.

- I flag = 0 (interrupt disabled)
- IR bit = 0 (interrupt not requested)
- Interrupt priority level = IPL

By setting the I flag to 1 (interrupt enabled) in the interrupt routine, an interrupt request with higher priority than the IPL can be acknowledged.

The interrupt requests not acknowledged because of their low interrupt priority level are kept pending. When the IPL is restored by an REIT instruction and interrupt priority is resolved against it, the pending interrupt request is acknowledged if the following condition is met:

Interrupt priority level of pending interrupt request > Restored IPL

### 12.8 $\overline{\text{INT}}$ Interrupt

The  $\overline{\text{INT}}_i$  interrupt ( $i = 0$  to  $5$ ) is triggered by the edges of external inputs. The edge polarity is selected using the IFSR $_i$  bit in the IFSR register.

To use the  $\overline{\text{INT}}_4$  interrupt, set the IFSR6 bit in the IFSR register to 1 ( $\overline{\text{INT}}_4$ ). To use the  $\overline{\text{INT}}_5$  interrupt, set the IFSR7 bit in the IFSR register to 1 ( $\overline{\text{INT}}_5$ ).

## 12.9 $\overline{\text{NMI}}$ Interrupt

An  $\overline{\text{NMI}}$  interrupt is generated when input to the  $\overline{\text{NMI}}$  pin changes state from high to low. The  $\overline{\text{NMI}}$  interrupt is a non-maskable interrupt. To use the  $\overline{\text{NMI}}$  interrupt, set the PM24 bit in the PM2 register to 1 ( $\overline{\text{NMI}}$  interrupt enabled). The  $\overline{\text{NMI}}$  input uses a digital debounce function. Refer to 11. "Programmable I/O Ports" for the digital debounce function. Figure 12.9 shows  $\overline{\text{NMI}}$  Interrupt Block Diagram.

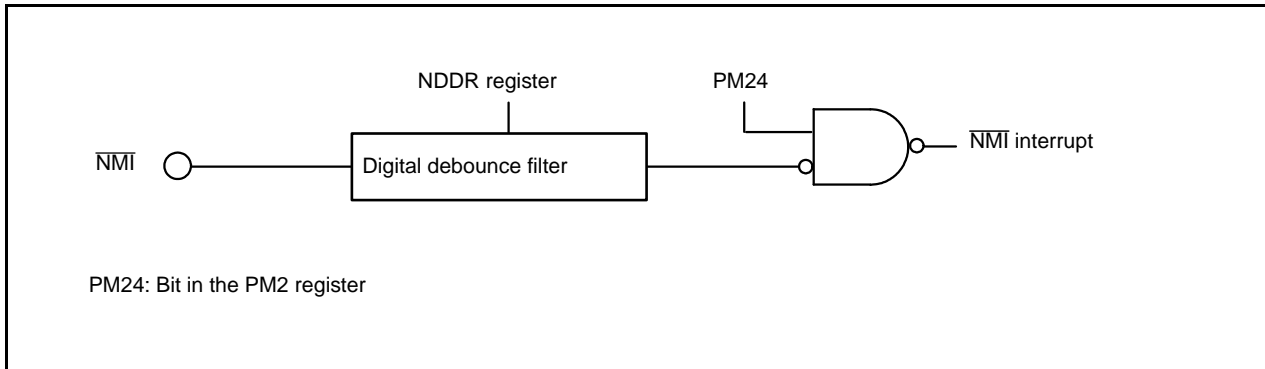


Figure 12.9  $\overline{\text{NMI}}$  Interrupt Block Diagram

## 12.10 Key Input Interrupt

When input to any pin from P10\_4 to P10\_7 becomes low where the corresponding PD10\_4 to PD10\_7 bit in the PD10 register is 0 (input), the IR bit in the KUPIC register becomes 1 (key input interrupt request). When using any pin from  $\overline{\text{KI0}}$  to  $\overline{\text{KI3}}$  for the key input interrupt, do not use all four pins AN4 to AN7 as analog input pins. While input to any pin from P10\_4 to P10\_7 is low, inputs to all other pins of the port are not detected as interrupts.

Key input interrupts can be used as a key-on wake up function for getting the MCU out of wait or stop mode.

Figure 12.10 shows Block Diagram of Key Input Interrupt.

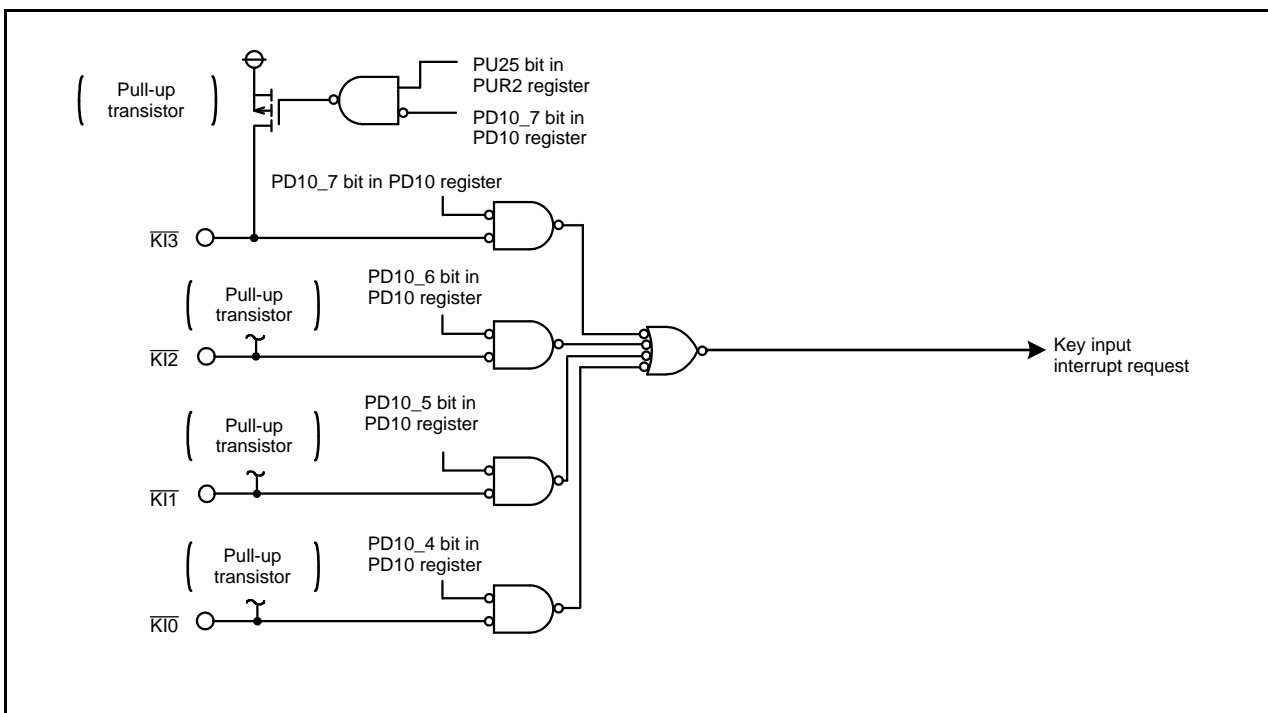


Figure 12.10 Block Diagram of Key Input Interrupt

## 12.11 Address Match Interrupt

An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMAD<sub>i</sub> register (i = 0 to 3). Set the start address of any instruction in the RMAD<sub>i</sub> register. Use bits AIER0 and AIER1 in the AIER register, and bits AIER20 and AIER21 in the AIER2 register to enable or disable the interrupt. Note that the address match interrupt is unaffected by the I flag and IPL. When an address match interrupt request is acknowledged, the value of the PC that is saved to the stack area (refer to 12.7.5 “Saving Registers”) varies depending on the instruction at the address indicated by the RMAD<sub>i</sub> register. (The value of the PC that is saved to the stack area is not the correct return address.) Therefore, use one of the following methods to return from the address match interrupt:

- Rewrite the values of the stack and then use the REIT instruction to return.
- Restore the stack to its previous state by using the POP or similar instructions before the interrupt request was accepted and then use a jump instruction to return.

**Table 12.11 Value of PC Saved on Stack Area When Address Match Interrupt Request Accepted**

Instruction at the Address Indicated by the RMAD <sub>i</sub> Register	Value of the PC That Is Saved to the Stack Area
<ul style="list-style-type: none"> <li>• 16-bit operation code instructions</li> <li>• Instruction shown below among 8-bit operation code instructions</li> </ul> ADD.B:S #IMM8, dest    SUB.B:S #IMM8, dest    AND.B:S #IMM8, dest OR.B:S #IMM8, dest    MOV.B:S #IMM8, dest    STZ #IMM8, dest STNZ #IMM8, dest    STZX #IMM81, #IMM82,dest CMP.B:S #IMM8, dest    PUSHM src    POPM dest JMPS #IMM8    JSRS #IMM8 MOV.B:S #IMM, dest (however, dest = A0 or A1)	The address indicated by the RMAD <sub>i</sub> register +2
Instructions not listed above	The address indicated by the RMAD <sub>i</sub> register +1

Refer to 12.7.5 “Saving Registers” for PC values saved to the stack area.

**Table 12.12 Relationship between Address Match Interrupt Sources and Associated Registers**

Address Match Interrupt Sources	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1
Address match interrupt 2	AIER20	RMAD2
Address match interrupt 3	AIER21	RMAD3

## 12.12 Non-Maskable Interrupt Source Discrimination

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share the same interrupt vector. When using some functions together, read the detect flags of the events in an interrupt processing program, and determine the source of the interrupt. Table 12.13 lists Bits Used for Non-Maskable Interrupt Source Discrimination.

**Table 12.13 Bits Used for Non-Maskable Interrupt Source Discrimination**

Interrupt	Detect Flag	
	Bit Position	Function
Watchdog timer	VW2C3 bit in the VW2C register (watchdog timer underflow detected)	0: Not detected 1: Detected
Oscillator stop/restart detect	CM22 bit in the CM2 register (oscillator stop/restart detected)	
Voltage monitor 2	VW2C2 bit in the VW2C register (Vdet2 passage detected)	

## 12.13 Notes on Interrupts

### 12.13.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from address 00000h during the interrupt sequence. At this time, the IR bit of the accepted interrupt is cleared to 0 (interrupt not requested).

If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts becomes 0. This may cause problems such as interrupts being canceled or an unexpected interrupt request being generated.

### 12.13.2 SP Setting

Set a value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is set to 0000h after reset. Therefore, if an interrupt is accepted before setting a value in the SP (USP, ISP), the program may go out of control.

Set a value in the ISP at the beginning of the program. For the first instruction after reset only, all interrupts are disabled.

### 12.13.3 $\overline{\text{NMI}}$ Interrupt

- When not using the  $\overline{\text{NMI}}$  interrupt, set the PM24 bit in the PM2 register to 0 ( $\overline{\text{NMI}}$  interrupt disabled).
- The  $\overline{\text{NMI}}$  interrupt is disabled after reset. The  $\overline{\text{NMI}}$  interrupt is enabled by setting the PM24 bit in the PM2 register to 1. Set the PM24 bit to 1 when a high-level signal is applied to the  $\overline{\text{NMI}}$  pin. When the PM24 bit is set to 1 while a low-level signal is applied, an  $\overline{\text{NMI}}$  interrupt is generated. Once the  $\overline{\text{NMI}}$  interrupt is enabled, it cannot be disabled until the MCU is reset.
- The MCU cannot enter stop mode while the PM24 bit is 1 ( $\overline{\text{NMI}}$  interrupt enabled) and input on the  $\overline{\text{NMI}}$  pin is low. When input on the  $\overline{\text{NMI}}$  pin is low, the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while the PM24 bit is 1 ( $\overline{\text{NMI}}$  interrupt enabled) and a low signal is input to the  $\overline{\text{NMI}}$  pin. When the  $\overline{\text{NMI}}$  pin is driven low, the CPU clock remains active even though the CPU stops, and therefore, the current consumption of the chip does not drop. In this case, the normal condition is restored by the next interrupt generation.
- Set the low- and high-level durations of the input signal to the  $\overline{\text{NMI}}$  pin to 2 CPU clock cycles + 300 ns or more.



### 12.13.4 Changing an Interrupt Source

When the interrupt source is changed, the IR bit in the interrupt control register may become 1 (interrupt requested). To use an interrupt, change the interrupt source, and then set the IR bit to 0 (interrupt not requested).

In this section, the changing of an interrupt source refers to all elements used in changing the interrupt source, polarity, and timing assigned to each software interrupt number. Therefore, if a mode change of any peripheral function involves changing the source, polarity or timing of an interrupt, be sure to clear the IR bit for that interrupt to 0 (interrupt not requested) after making such changes. Refer to the descriptions of the individual peripheral functions for details of the interrupts.

Figure 12.11 shows the Procedure for Changing the Interrupt Generate Source.

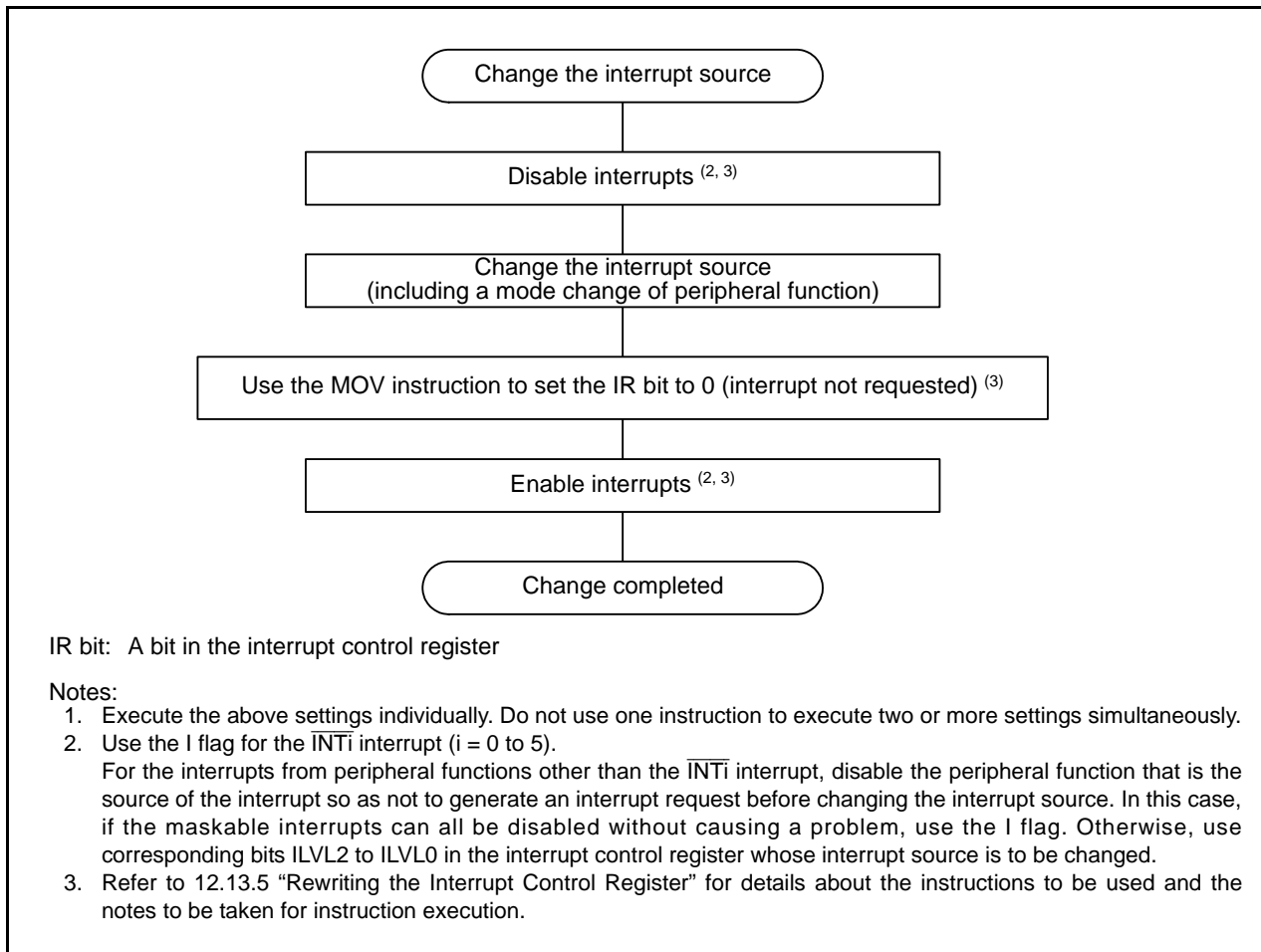


Figure 12.11 Procedure for Changing the Interrupt Generate Source

### 12.13.5 Rewriting the Interrupt Control Register

To modify the interrupt control register, follow either of the procedures below:

- Modify in places where no interrupt requests corresponding to the interrupt control register may occur.
- If an interrupt request can be generated, disable that interrupt and then rewrite the interrupt control register.

When using the I flag to disable an interrupt, set the I flag as shown in the sample program code below. (Refer to 12.13.6 “Instruction to Rewrite the Interrupt Control Register” for rewriting the interrupt control registers using the sample program code.)

Examples 1 through 3 show how to prevent the I flag from becoming 1 (interrupt enabled) before the contents of the interrupt control register is rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to pause the program until the interrupt control register is modified

```
INT_SWITCH1:
  FCLR      I                ; Disable interrupts.
  AND.B     #00H, 0055H      ; Set the TA0IC register to 00h.
  NOP
  NOP
  FSET      I                ; Enable interrupts.
```

Example 2: Using a dummy read to delay the FSET instruction

```
INT_SWITCH2:
  FCLR      I                ; Disable interrupts.
  AND.B     #00H, 0055H      ; Set the TA0IC register to 00h.
  MOV.W     MEM, R0          ; Dummy read.
  FSET      I                ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC     FLG
  FCLR      I                ; Disable interrupts.
  AND.B     #00H, 0055H      ; Set the TA0IC register to 00h.
  POPC      FLG              ; Enable interrupts.
```

### 12.13.6 Instruction to Rewrite the Interrupt Control Register

- Do not use the BTSTC and BTSTS instructions to rewrite the interrupt control registers.
- Use the AND, OR, BCLR, BSET, or MOV instruction to rewrite interrupt control registers. When an interrupt request is generated for the register being rewritten while executing an AND, OR, BCLR, or BSET instruction, the IR bit becomes 1 (interrupt requested) and remains 1.

### 12.13.7 $\overline{\text{INT}}$ Interrupt

- Either a low level of at least  $t_w(\text{INL})$  width or a high level of at least  $t_w(\text{INH})$  width is necessary for the signal input to pins  $\overline{\text{INT0}}$  through  $\overline{\text{INT5}}$ , regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT5IC or bits IFSR7 to IFSR0 in the IFSR register are changed, the IR bit may inadvertently become 1 (interrupt requested). Be sure to set the IR bit to 0 (interrupt not requested) after changing any of these register bits.

## 13. Watchdog Timer

### 13.1 Introduction

The watchdog timer contains a 15-bit counter, and the count source protection mode can be enabled/disabled.

Table 13.1 shows the watchdog timer specifications and Figure 13.1 shows a block diagram of the watchdog timer. Refer to 6.4.7 “Watchdog Timer Reset” for details on the watchdog timer reset.

**Table 13.1 Watchdog Timer Specifications**

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Dedicated 125 kHz on-chip oscillator for watchdog timer (fWDT)
Count operation	Decrements	
Count start conditions	One of the following is selectable: (Selected by the WDTON bit in the OFS1 address) <ul style="list-style-type: none"> <li>Counting starts automatically after reset.</li> <li>Counting starts by a write to the WDTS register.</li> </ul>	
Count stop conditions	<ul style="list-style-type: none"> <li>Stop mode</li> <li>Wait mode</li> <li>Software commands executed in EW1 mode, except when executing the suspend function.</li> </ul>	None
Watchdog timer counter refresh timing	<ul style="list-style-type: none"> <li>Resets (refer to 6. “Resets” for details)</li> <li>Write 00h followed by FFh to the WDTR register.</li> <li>Watchdog timer underflow</li> </ul>	
Watchdog timer initial value	7FFFh	Selectable by using bits WDTUFS1 and WDTUFS0 in the OFS2 address
When underflows	A watchdog timer interrupt is generated or watchdog timer reset is initiated	Watchdog timer reset is initiated
Selectable functions	<ul style="list-style-type: none"> <li>Prescaler divide ratio Divide-by-16 or divide-by-128 (selected by the WDC7 bit in the WDC register) However, divide-by-2 is selected when the CM07 bit in the CM0 register is 1 (sub clock).</li> <li>Count source protection mode Enabled or disabled (selected by the CSPROINI bit in the OFS1 address and the CSPRO bit in the CSPR register)</li> <li>Watchdog timer refresh period Selectable by setting bits WDTRCS1 and WDTRCS0 in the OFS2 address.</li> </ul>	

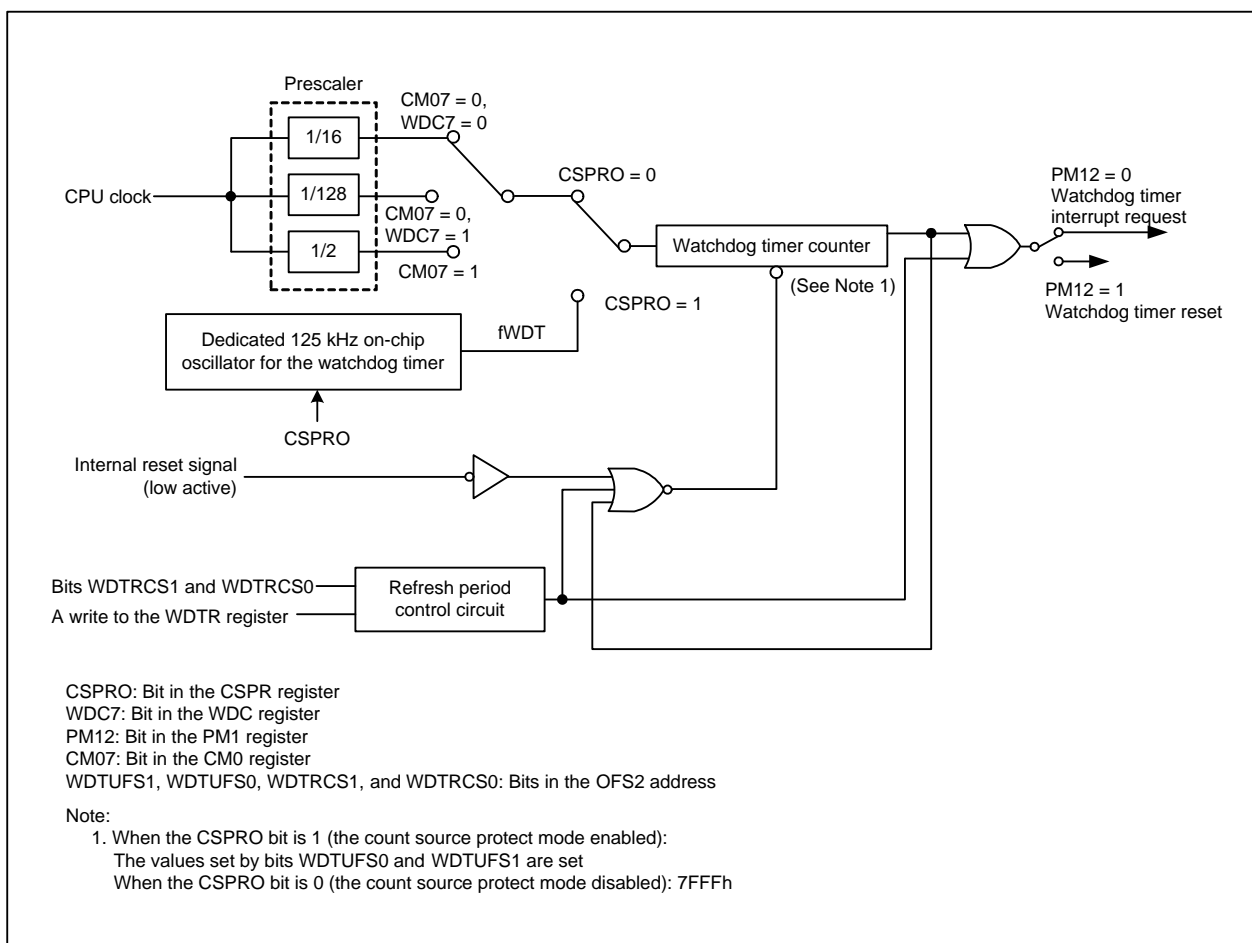


Figure 13.1 Watchdog Timer Block Diagram

## 13.2 Registers

**Table 13.2 Registers**

Address	Register Names	Register Symbol	Reset Value
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b
037Ch	Count Source Protection Mode Register	CSPR	00h (1)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb

Note:

1. When the CSPROINI bit in the OFS1 address is set to 0, the reset value is 1000 0000b.

### 13.2.1 Voltage Monitor 2 Control Register (VW2C)

Voltage Monitor 2 Control Register				
		Symbol VW2C	Address 002Ch	Reset Value 1000 0X10b (hardware reset, power-on reset, voltage monitor 0 reset)
Bit Symbol	Bit Name	Function	RW	
VW2C0	Voltage monitor 2 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW	
VW2C1	Voltage monitor 2 digital filter disable mode select bit	0 : Digital filter enabled 1 : Digital filter disabled	RW	
VW2C2	Voltage change detection flag	0 : Not detected 1 : Vdet2 passage detected	RW	
VW2C3	Watchdog timer detection flag	0 : Not detected 1 : Watchdog timer underflow detected	RW	
VW2F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW	
VW2F1				
VW2C6	Voltage monitor 2 mode select bit	0 : Voltage monitor 2 interrupt at Vdet2 passage 1 : Voltage monitor 2 reset at Vdet2 passage	RW	
VW2C7	Voltage monitor 2 interrupt/ reset generation condition select bit	0: When VCC reaches or goes above Vdet2 1: When VCC reaches or goes below Vdet2	RW	

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.

Bits VW2C2 and VW2C3 do not change at voltage monitor 2 reset, oscillator stop detect reset, watchdog timer reset, or software reset.

When rewriting the VW2C register (excluding the VW2C3 bit), the VW2C2 bit may become 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.

#### VW2C3 (WDT Detection Flag) (b3)

Use this bit in an interrupt routine to determine the source of the interrupts from the watchdog timer, the oscillator stop/restart detect, and voltage monitor 2.

Conditions to become 0:

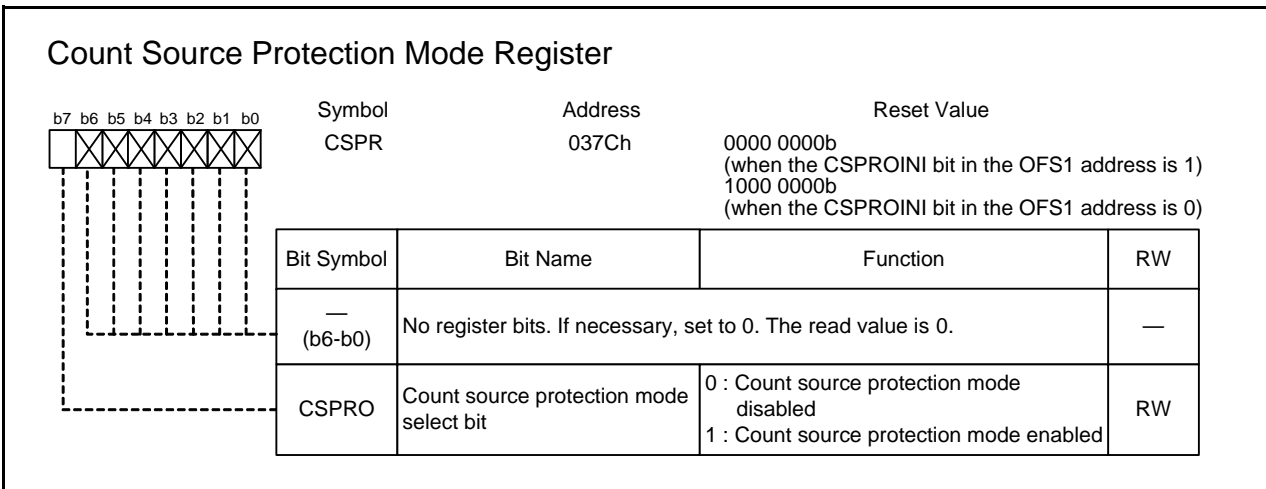
- Writing 0 by a program

Condition to become 1:

- Watchdog timer underflow detected

This flag remains unchanged even if 1 is written by a program.

### 13.2.2 Count Source Protection Mode Register (CSPR)



#### CSPRO (Count Source Protection Mode Select Bit) (b7)

To set the CSPRO bit to 1, write 1 immediately after writing 0. The CSPRO bit cannot be set to 0 by a program.

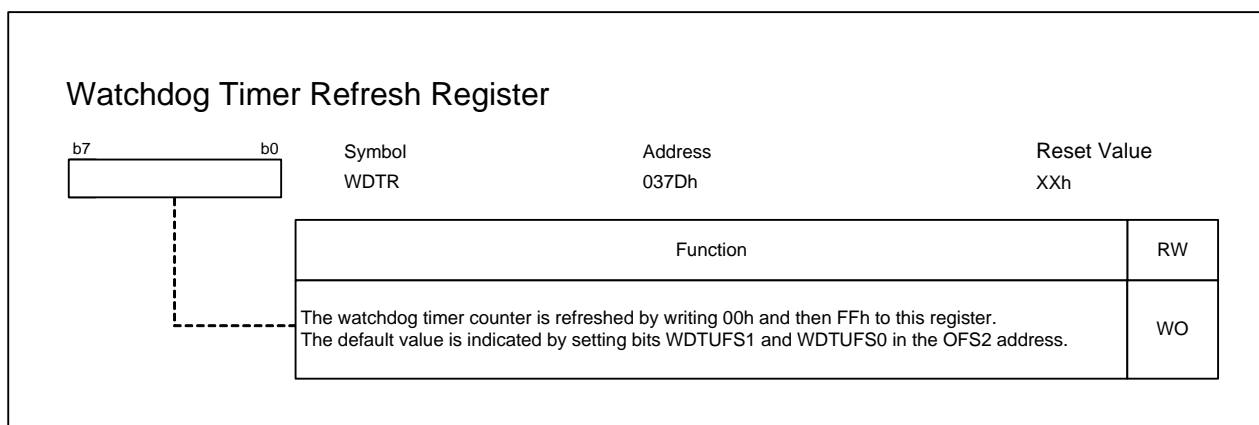
When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), the following are automatically set:

- Dedicated 125 kHz on-chip oscillator for the watchdog timer starts oscillating.
- The PM12 bit in the PM1 register is set to 1 (watchdog timer reset is initiated when the watchdog timer underflows.).
- The initial value of the watchdog timer is a value set by setting bits WDTUFS1 and WDTUFS0 in the OFS2 address.

When the CSPROINI bit in the OFS1 address is 0, the CSPRO bit becomes 1. The CSPROINI bit cannot be changed by a program. In order to set the CSPROINI bit, write 0 to bit 7 of address 0FFFFh by using a flash programmer.

Do not change the CSPRO bit setting while the watchdog timer is operating.

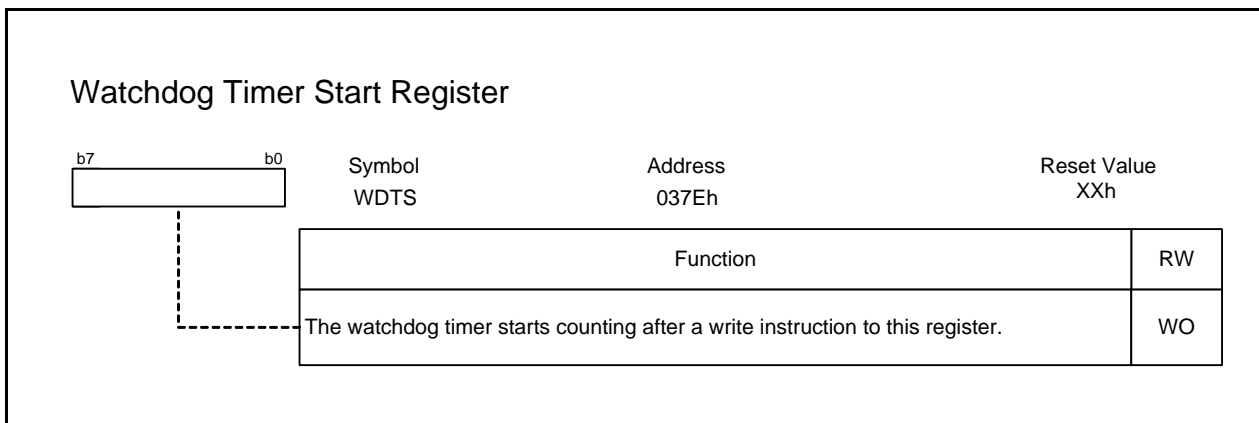
### 13.2.3 Watchdog Timer Refresh Register (WDTR)



After the watchdog timer interrupt is generated, refresh the watchdog timer by writing to the WDTR register.

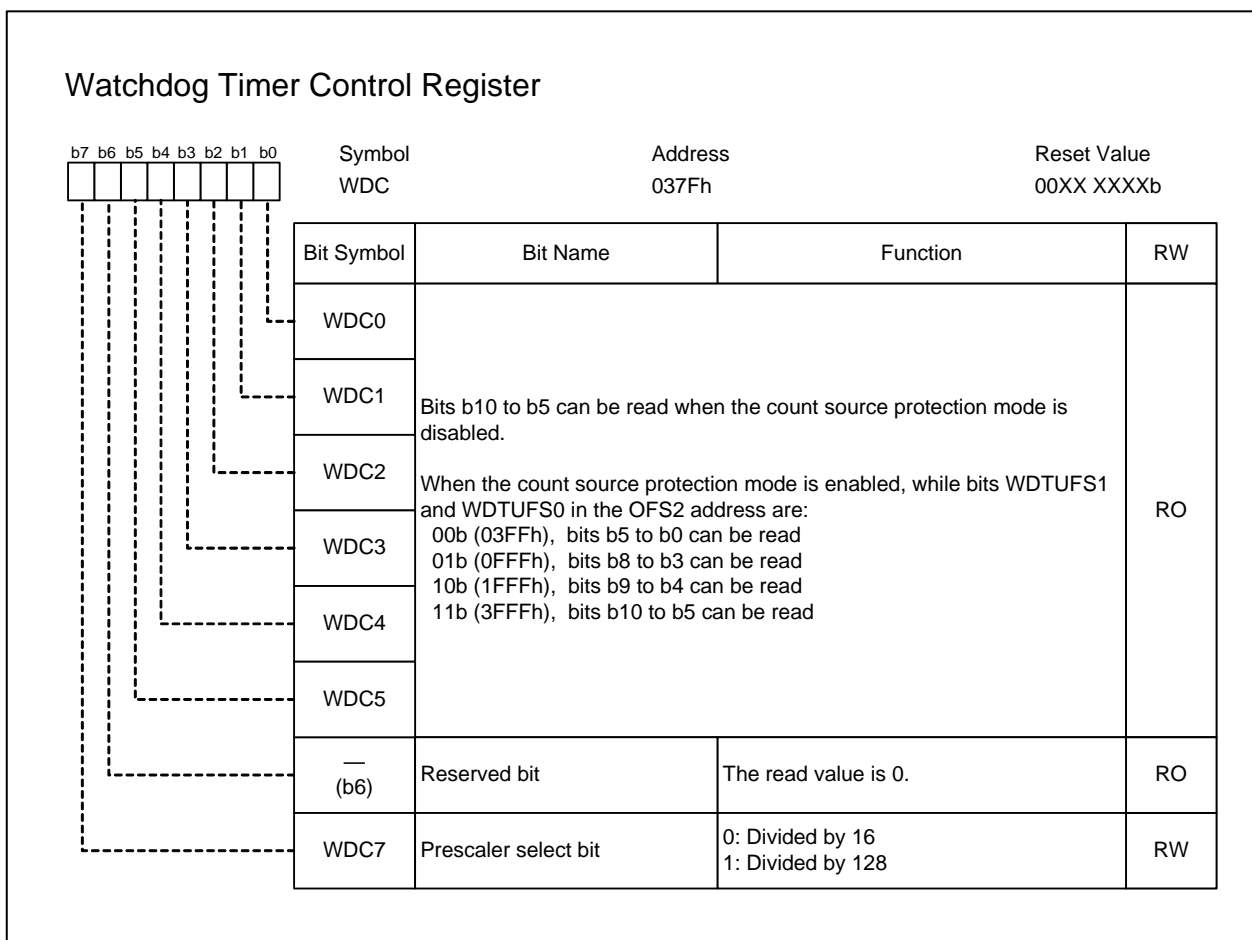


### 13.2.4 Watchdog Timer Start Register (WDTS)



The WDTS register is enabled when the WDTON bit in the OFS1 address is 1 (watchdog timer stops after reset).

### 13.2.5 Watchdog Timer Control Register (WDC)



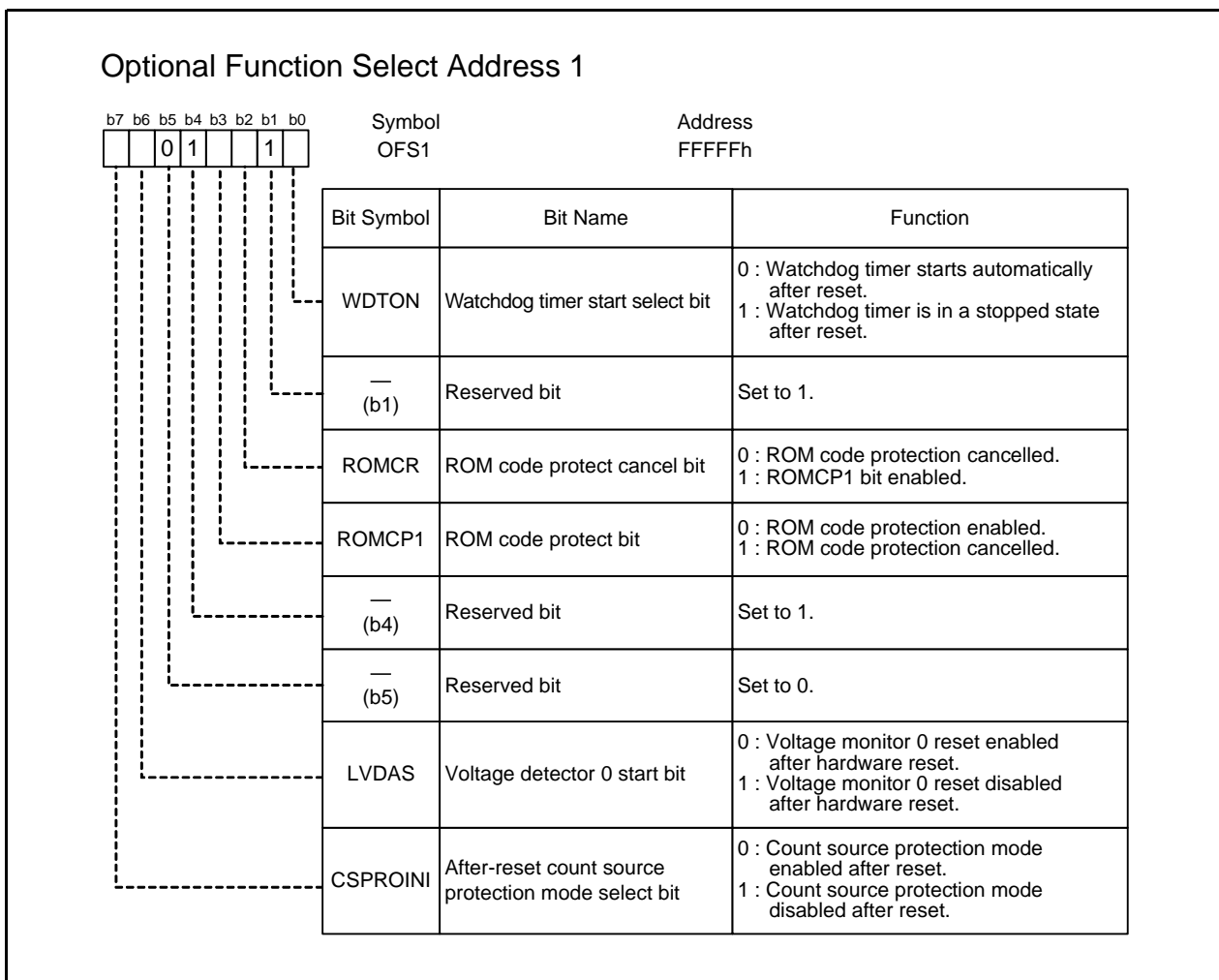
### 13.3 Optional Function Select Area

In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

In blank products, the OFS1 and OFS2 address values are FFh when shipped. After a value is written by the user, this address takes on the written value. In programmed products, the OFS1 and OFS2 address values are the value set in the user program prior to shipping.

#### 13.3.1 Optional Function Select Address 1 (OFS1)



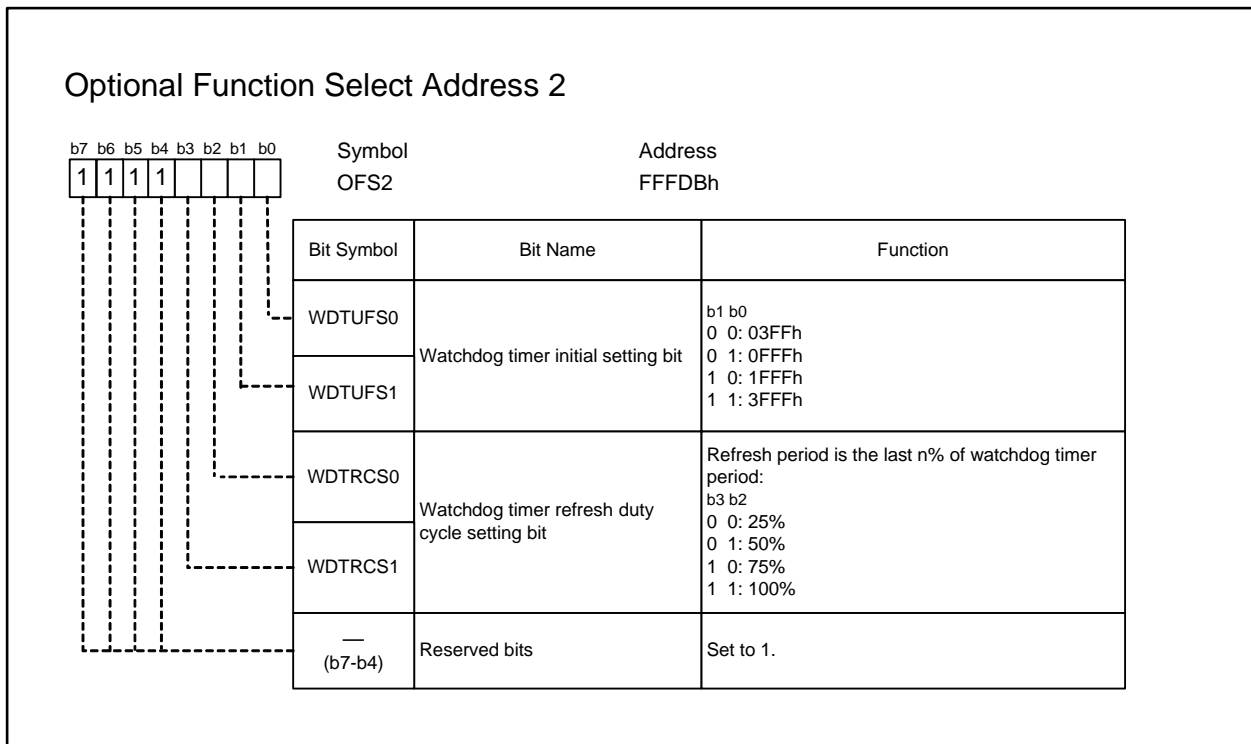
**WDTON (Watchdog Timer Start Select Bit) (b0)**

**CSPROINI (After-Reset Count Source Protection Mode Select Bit) (b7)**

These bits control the state of watchdog timer after reset.

When setting the CSPROINI bit to 0 (count source protection mode enabled after reset), set the WDTON bit to 0 (watchdog timer starts automatically after reset) as well.

### 13.3.2 Optional Function Select Address 2 (OFS2)



**WDTUFS1 to WDTUFS0 (Watchdog Timer Initial Setting Bit) (b0-b1)**  
 Enabled when CSPRO bit in the CSPR register is 1 (count source protection mode enabled).

**WDTRCS1 to WDTRCS0 (Watchdog Timer Refresh Duty Cycle Setting Bit) (b3-b2)**  
 Assuming the cycle of the watchdog timer underflow is 100%, bits WDTRCS1 and WDTRCS0 select the refresh period for the watchdog timer.  
 Refer to 13.4.1 “Refresh Operation Period” for details.

### 13.4 Operations

#### 13.4.1 Refresh Operation Period

To refresh the watchdog timer, the period writing to the WDTR register can be limited to the fixed period before the underflow. The refresh period can be selected by setting bits WDTRCS1 and WDTRCS0 in the OFS2 address. The period specified by these bits assumes that an underflow period of the watchdog timer is 100%. Figure 13.2 shows the refresh operation period for the watchdog timer.

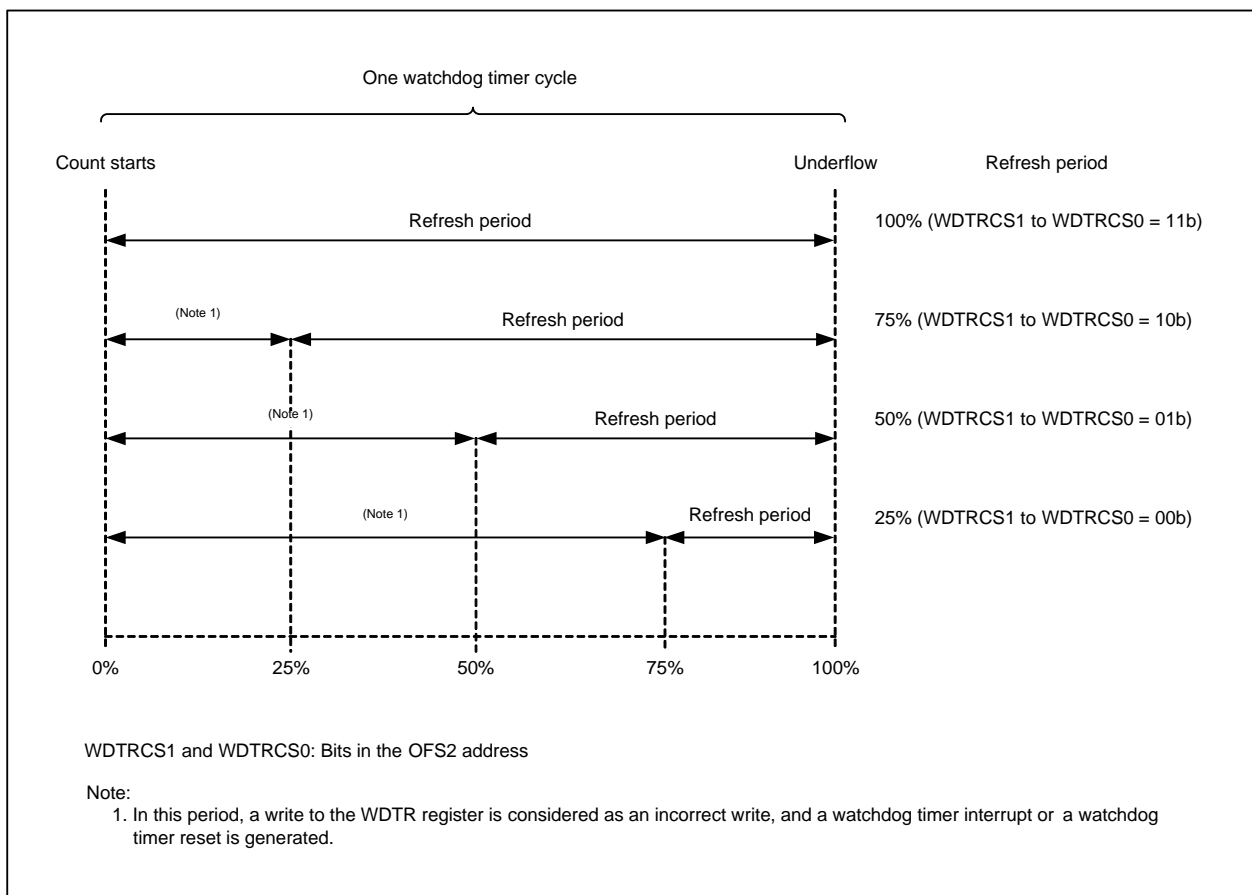


Figure 13.2 Watchdog Timer Refresh Period

### 13.4.2 Count Source Protection Mode Disabled

The CPU clock is used as the watchdog timer count source when the count source protection mode is disabled.

Table 13.3 lists the specifications of watchdog timer when the count source protection mode is disabled.

**Table 13.3 Watchdog Timer Specifications (When Count Source Protection Mode is Disabled)**

Item	Specification
Count source	CPU clock
Count operation	Decrements
Watchdog timer cycle	<p>When the CM07 bit in the CM0 register is 0 (main clock, PLL clock, 40 MHz on-chip oscillator clock, 125 kHz on-chip oscillator clock): <sup>(1)</sup></p> $\frac{\text{Prescaler divider factor (n)} \times \text{watchdog timer count value (32768)}}{\text{CPU clock}}$ <p>n = 16 or 128, selected by the WDC7 bit in the WDC register            Example: When CPU clock frequency is 16 MHz and the prescaler divider factor is 16, the watchdog timer cycle is approximately 32.8 ms.</p> <p>When the CM07 bit is 1 (sub clock): <sup>(1)</sup></p> $\frac{\text{Prescaler divider factor (2)} \times \text{watchdog timer count value (32768)}}{\text{CPU clock}}$
Watchdog timer counter refresh timing	<ul style="list-style-type: none"> <li>• Resets (refer to 6. "Resets" for details)</li> <li>• Write 00h, and then FFh to the WDTR register.</li> <li>• Watchdog timer underflow</li> </ul>
Count start conditions	<p>Set the WDTON bit in the OFS1 address to select the watchdog timer state after reset.</p> <ul style="list-style-type: none"> <li>• When the WDTON bit is 1 (watchdog timer is in a stop state after reset): The watchdog timer and prescaler stop after reset and the watchdog timer starts counting by writing to the WDTS register.</li> <li>• When the WDTON bit is 0 (watchdog timer starts automatically after reset): The watchdog timer and prescaler start counting automatically after reset.</li> </ul>
Count stop conditions	<ul style="list-style-type: none"> <li>• Wait mode</li> <li>• Stop mode</li> <li>• While executing software commands in EW1 mode, except when executing the suspend function. The count resumes from the value held after exiting the modes above.</li> </ul>
Operations when the watchdog timer underflows	<ul style="list-style-type: none"> <li>• When the PM12 bit in the PM1 register is 0, a watchdog timer interrupt is generated.</li> <li>• When the PM12 bit in the PM1 register is 1, the watchdog timer is reset. (refer to 6.4.7 "Watchdog Timer Reset" for details)</li> </ul>

Note:

1. Writing 00h and then FFh to the WDTR register refreshes the watchdog timer counter, but not the prescaler. Therefore, marginal differences in the watchdog timer cycle can be expected. The prescaler is initialized by a reset.

### 13.4.3 Count Source Protection Mode Enabled

When the count source protection mode is enabled, fWDT is used as the watchdog timer count source. Table 13.4 lists the specifications of the watchdog timer when the count source protection mode is enabled.

**Table 13.4 Watchdog Timer Specifications (When Count Source Protection Mode is Enabled)**

Item	Specification
Count source	fWDT
Count operation	Decrements
Watchdog timer cycle	$\frac{\text{Watchdog timer count value (m)}}{f\text{WDT}}$ <p>m: The value set by setting bits WDTUFS1 and WDTUFS0 in the OFS2 address. Example: When bits WDTUFS1 to WDTUFS0 are 00b (watchdog timer cycle setting is 03FFh), the watchdog timer cycle is approximately 8.2 ms.</p>
Watchdog timer counter refresh timing	<ul style="list-style-type: none"> <li>Resets (refer to 6. "Resets" for details)</li> <li>Write 00h, and then FFh to the WDTR register.</li> <li>Watchdog timer underflow</li> </ul>
Count start conditions	<p>Set the WDTON bit in the OFS1 address to select the watchdog timer operation after reset.</p> <ul style="list-style-type: none"> <li>When the WDTON bit is set to 1 (watchdog timer is in stop state after reset): The watchdog timer and prescaler stop after reset and the count starts by writing to the WDTS register.</li> <li>When the WDTON bit is set to 0 (watchdog timer starts automatically after reset): The watchdog timer and prescaler start counting automatically after reset.</li> </ul>
Count stop condition	<p>None.</p> <p>Count continues even in wait mode once the count starts. The MCU does not enter stop mode.</p>
Operations when the watchdog timer underflows	The watchdog timer is reset. (refer to 6.4.7 "Watchdog Timer Reset" for details)

The dedicated 125 kHz on-chip oscillator for the watchdog timer (fWDT) is used as the watchdog timer count source when the count source protection mode is enabled.

The dedicated 125 kHz on-chip oscillator for the watchdog timer (fWDT) automatically oscillates when the CSPRO bit in the CSPR register is 1 (count source protection mode enabled).

### 13.5 Interrupts

The watchdog timer interrupt is a non-maskable interrupt.

The watchdog timer interrupt, oscillator stop/restart detect interrupt, and voltage monitor 2 interrupt share an vector. When using multiple functions, read the detect flag in an interrupt handler to determine which interrupt factor generates an interrupt request.

- The VW2C3 bit in the VW2C register is the detect flag for the watchdog timer. After the interrupt factor is determined, set the VW2C3 bit to 0 (not detected) by a program.

### 13.6 Notes on the Watchdog Timer

After the watchdog timer interrupt is generated, use the WDTR register to refresh the watchdog timer counter.



## 14. DMAC

### 14.1 Introduction

The direct memory access controller (DMAC) allows data to be transferred without CPU intervention.

There are four DMAC channels. Each time a DMA request occurs, the DMAC transfers one (8- or 16-bit) unit of data from the source address to the destination address. The DMAC uses the same data bus used by the CPU. Because the DMAC has higher priority for bus control than the CPU, and because it makes use of a cycle steal method, it can transfer 1 word (16 bits) or 1 byte (8 bits) of data within a very short time after a DMA request is generated. Table 14.1 lists DMAC Specifications, and Figure 14.1 shows the DMAC Block Diagram.

**Table 14.1 DMAC Specifications**

Item	Specification	
Number of channels	4 (cycle steal method)	
Transfer memory spaces	<ul style="list-style-type: none"> <li>From a given address in a 1 MB space to a fixed address</li> <li>From a fixed address to a given address in a 1 MB space</li> <li>From a fixed address to a fixed address</li> </ul>	
Maximum number of bytes transferred	128 KB (with 16-bit transfers) or 64 KB (with 8-bit transfers)	
DMA request sources	41 sources Falling edge of $\overline{INT0}$ to $\overline{INT5}$ (6) Both edge of $\overline{INT0}$ to $\overline{INT5}$ (6) Timer A0 to timer A4 interrupt request (5) Timer B0 to timer B2 interrupt request (3) UART0 to UART4 transmission interrupt request (5) UART0, UART1, UART3, UART4 reception interrupt request (4) UART2 reception/ACK interrupt request (1) IC/OC base timer interrupt request (1) IC/OC channel 0 to IC/OC channel 7 interrupt (8) A/D conversion interrupt request (1) Software trigger (1)	
Channel priority	DMA0 > DMA1 > DMA2 > DMA3 (DMA0 takes precedence)	
Transfers	8 bits or 16 bits	
Transfer address direction	Forward or fixed (The source and destination addresses cannot both be in the forward direction.)	
Transfer mode	Single transfer	Transfer is completed when the DMA <sub>i</sub> transfer counter underflows.
	Repeat transfer	When the DMA <sub>i</sub> transfer counter underflows, it is reloaded with the value of the DMA <sub>i</sub> transfer counter reload register, and DMA transfer continues.
DMA interrupt request generation timing	When the DMA <sub>i</sub> transfer counter underflows	
DMA transfer start	Data transfer is initiated each time a DMA request is generated when the DMAE bit in the DMiCON register is 1 (enabled).	
DMA transfer stop	Single transfer	<ul style="list-style-type: none"> <li>When the DMAE bit is set to 0 (disabled)</li> <li>After the DMA<sub>i</sub> transfer counter underflows</li> </ul>
	Repeat transfer	When the DMAE bit is set to 0 (disabled)
Reload timing for forward address pointer and DMA <sub>i</sub> transfer counter	When a data transfer is started after setting the DMAE bit to 1 (enabled), the forward address pointer is reloaded with the value of the SAR <sub>i</sub> or DAR <sub>i</sub> register (whichever is specified to be in the forward direction), and the DMA <sub>i</sub> transfer counter is reloaded with the value of the DMA <sub>i</sub> transfer counter reload register.	
DMA transfer cycles	Minimum 3 cycles between SFR and internal RAM	

$i = 0$  to 3

Note:

- The selectable sources of DMA requests differ for each channel.

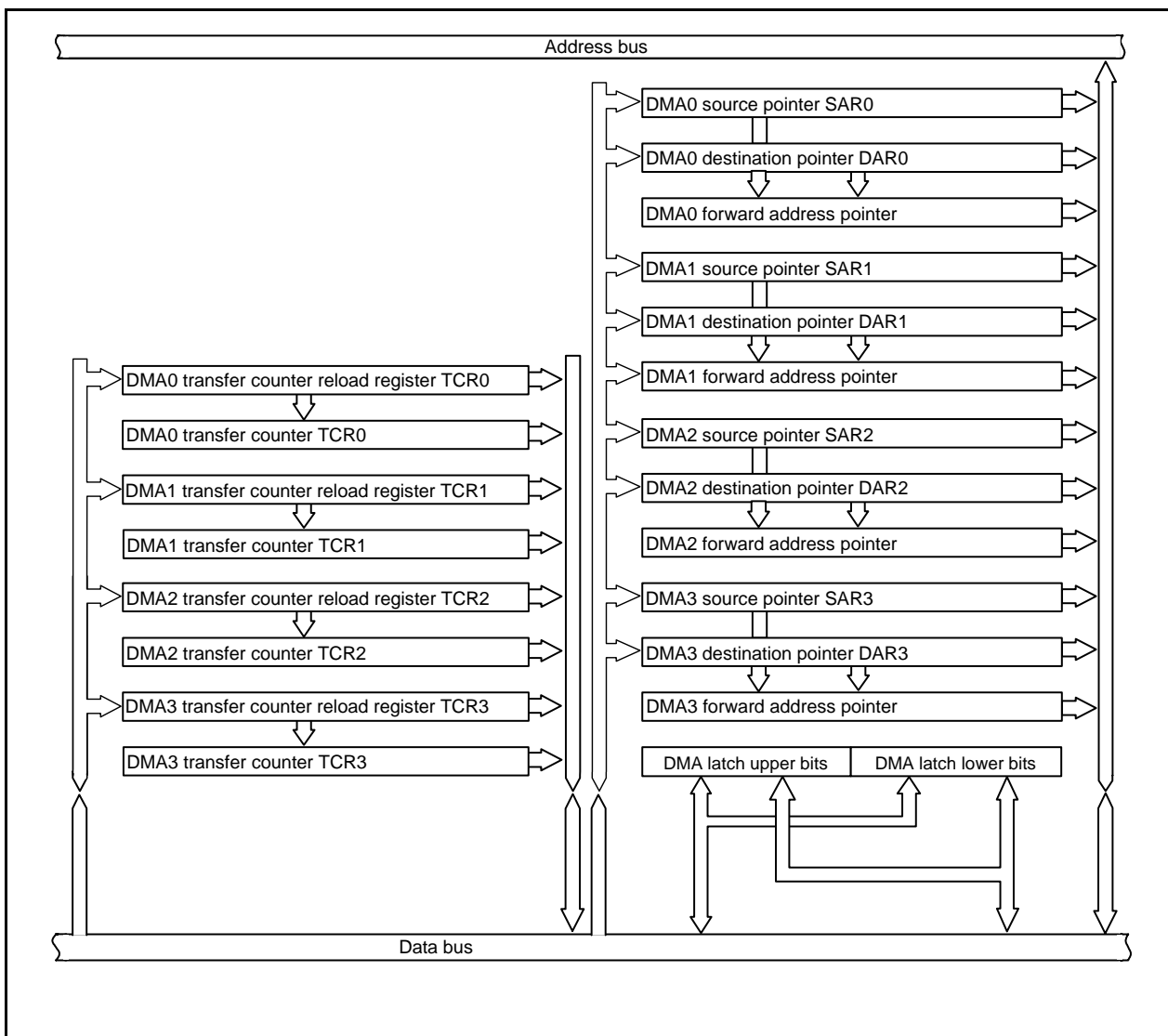


Figure 14.1 DMAC Block Diagram

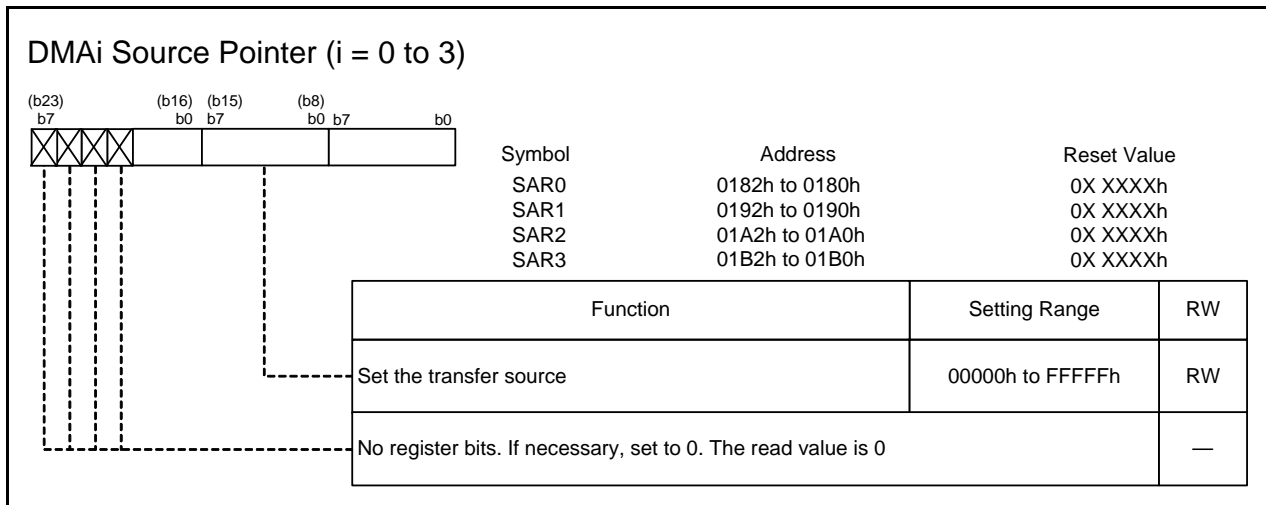
## 14.2 Registers

Table 14.2 lists Registers. Do not access these registers using the DMAC.

**Table 14.2 Registers**

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
0390h	DMA2 Source Select Register	DM2SL	00h
0392h	DMA3 Source Select Register	DM3SL	00h
0398h	DMA0 Source Select Register	DM0SL	00h
039Ah	DMA1 Source Select Register	DM1SL	00h

### 14.2.1 DMAi Source Pointer (SARi) (i = 0 to 3)



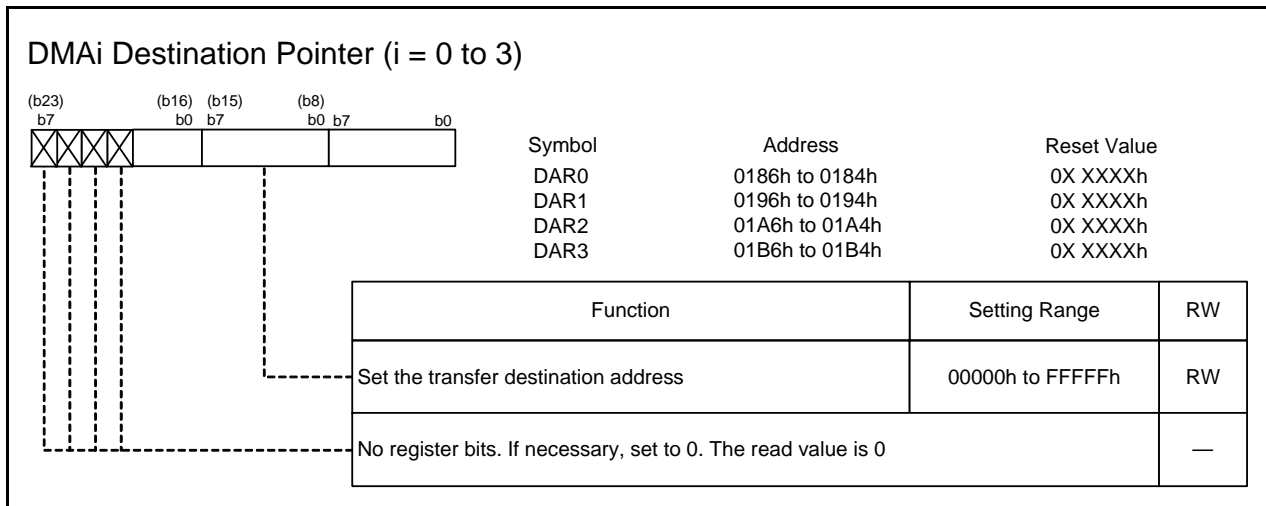
If the DSD bit in the DMiCON register is 0 (fixed), write to SARi register when the DMAE bit in the DMiCON register is 0 (DMA disabled).

If the DSD bit is 1 (forward direction), this register can be written to at any time.

If the DSD bit is 1 and the DMAE bit is 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.

The forward address pointer increments when a DMA request is accepted.

### 14.2.2 DMAi Destination Pointer (DARi) (i = 0 to 3)



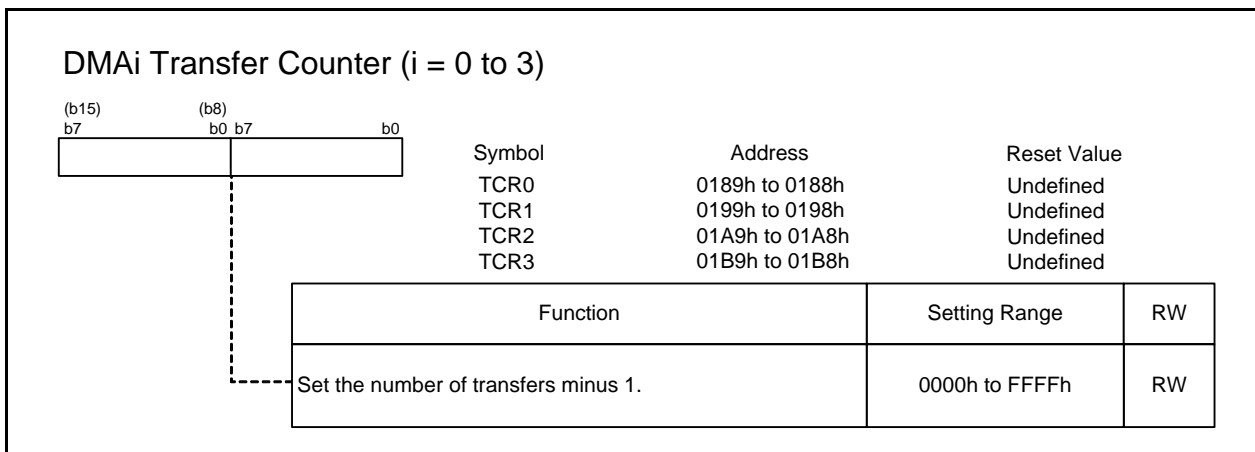
If the DAD bit in the DMiCON register is 0 (fixed), write to the DARi register when the DMAE bit in the DMiCON register is 0 (DMA disabled).

If the DAD bit is 1 (forward direction), this register can be written to at any time.

If the DAD bit is 1 and the DMAE bit is 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.

The forward address pointer increments when a DMA request is accepted.

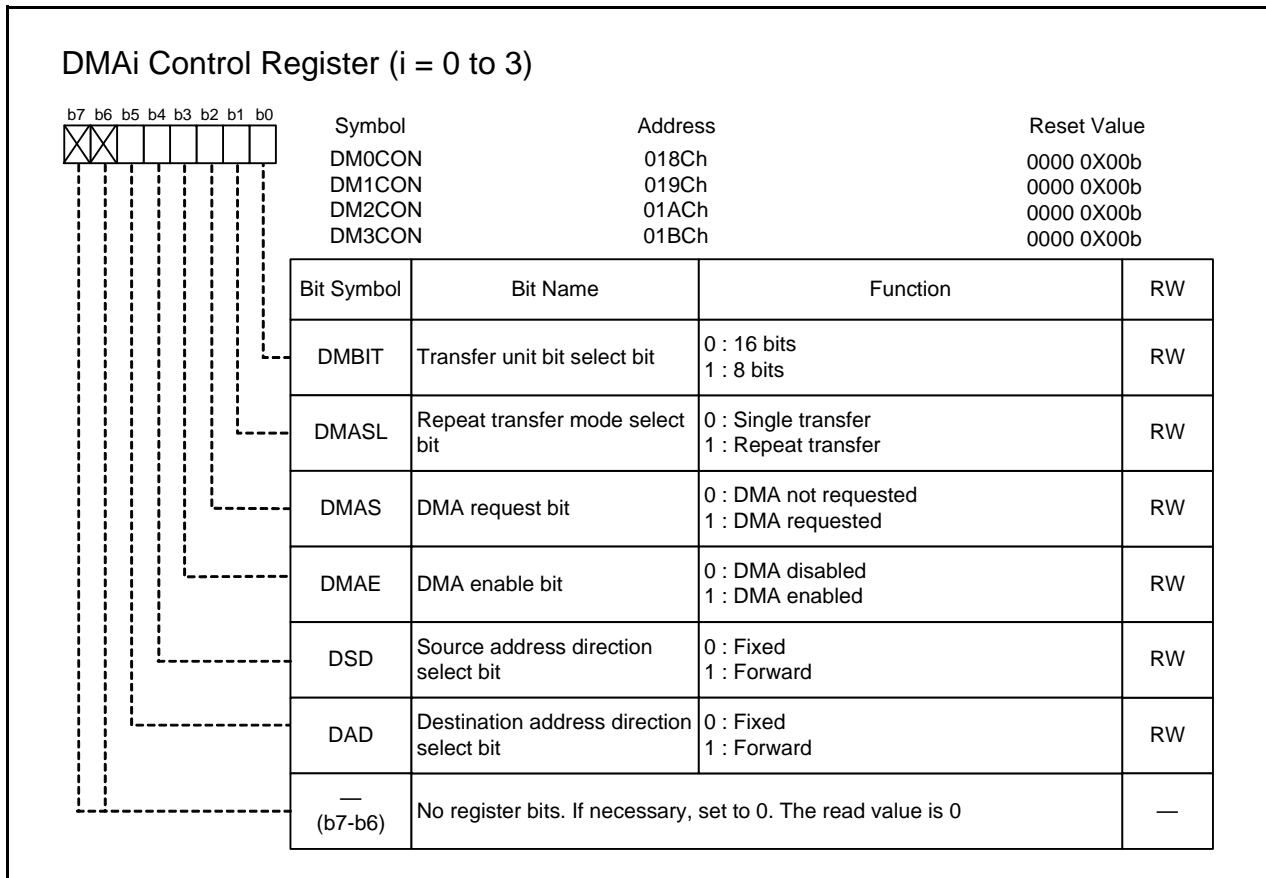
### 14.2.3 DMAi Transfer Counter (TCRi) (i = 0 to 3)



The value written in the TCRi register is stored in the DMAi transfer counter reload register. The DMAi transfer counter reload register value is transferred to the DMAi transfer counter in either of the following cases:

- The DMAE bit in the DMiCON register is set to 1 (DMA enabled) (single transfer mode, repeat transfer mode).
- The DMAi transfer counter underflows (repeat transfer mode).

### 14.2.4 DMAi Control Register (DMiCON) (i = 0 to 3)



#### DMAS (DMA request bit) (b2)

Conditions to become 0:

- Set the bit to 0.
- Start data transfer

Condition to become 1:

- Set the bit to 1.

#### DMAE (DMA enable bit) (b3)

Conditions to become 0:

- Set the bit to 0.
- The DMA transfer counter underflows (single transfer mode).

Condition to become 1:

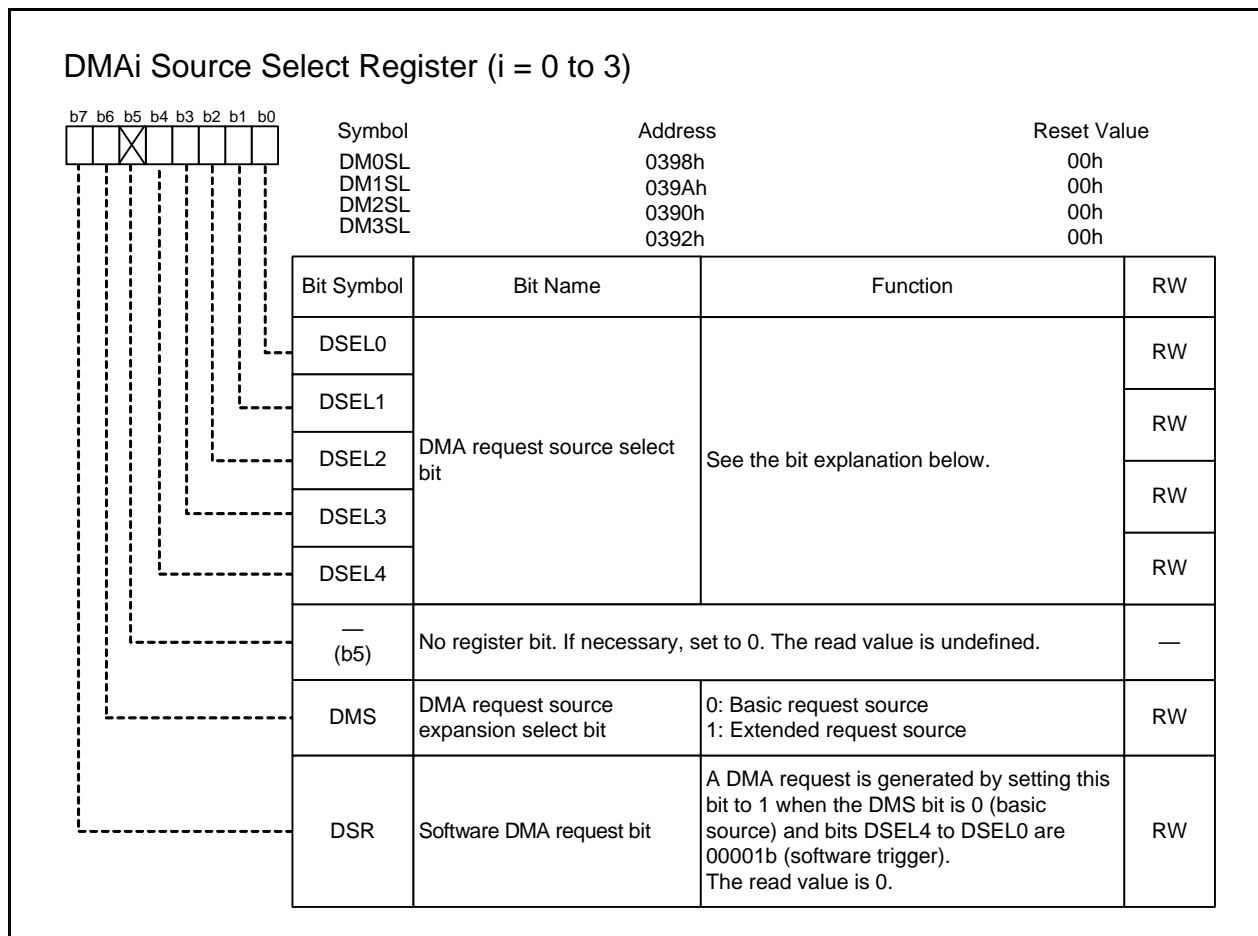
- Set the bit to 1.

#### DSD (Source address direction select bit) (b4)

#### DAD (Destination address direction select bit) (b5)

Set the DAD bit and/or DSD bit to 0 (address direction fixed).

### 14.2.5 DMAi Source Select Register (DMiSL) (i = 0 to 3)



#### DSEL4-DSEL0 (DMA request source select bit) (b4-b0)

The DMAi request sources can be selected by a combination of the DMS bit and bits DSEL4 to DSEL0 in the manner shown in Table 14.3 to Table 14.6. These tables list the DMAi request sources.

**Table 14.3 Sources of DMA Request (DMA0)**

DSEL4 to DSEL0	DMS is 0 (Basic Source of Request)	DMS is 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the INT0 pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	Both edges of the INT0 pin
0 0 1 1 1 b	Timer B0	–
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 transmission	IC/OC channel 7
1 0 0 0 0 b	UART1 reception	Falling edge of the INT4 pin
1 0 0 0 1 b	–	Both edges of the INT4 pin
1 0 0 1 0 b	–	–
1 0 0 1 1 b	UART4 transmission	–
1 0 1 0 0 b	UART4 reception	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 –: Do not set.

**Table 14.4 Source of DMA Request (DMA1)**

DSEL4 to DSEL0	DMS = 0 (Basic Source of Request)	DMS = 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the INT1 pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	–
0 0 1 1 1 b	Timer B0	Both edges of the INT1 pin
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception/ACK2	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 reception	IC/OC channel 7
1 0 0 0 0 b	UART1 transmission	Falling edge of the INT5 pin
1 0 0 0 1 b	–	Both edges of the INT5 pin
1 0 0 1 0 b	–	–
1 0 0 1 1 b	UART4 transmission	–
1 0 1 0 0 b	UART4 reception4	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 –: Do not set.



**Table 14.5 Sources of DMA Request (DMA2)**

DSEL4 to DSEL0	DMS is 0 (Basic Source of Request)	DMS is 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the INT2 pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	Both edges of the INT2 pin
0 0 1 1 1 b	Timer B0	–
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 transmission	IC/OC channel 7
1 0 0 0 0 b	UART1 reception	–
1 0 0 0 1 b	–	–
1 0 0 1 0 b	–	–
1 0 0 1 1 b	UART4 transmission	–
1 0 1 0 0 b	UART4 reception	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 – Do not set.

**Table 14.6 Source of DMA Request (DMA3)**

DSEL4 to DSEL0	DMS is 0 (Basic Source of Request)	DMS is 1 (Expanded Source of Request)
0 0 0 0 0 b	Falling edge of the INT3 pin	IC/OC base timer
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	IC/OC channel 0
0 0 0 1 1 b	Timer A1	IC/OC channel 1
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	–
0 0 1 1 1 b	Timer B0	Both edges of the INT3 pin
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	IC/OC channel 2
0 1 0 1 1 b	UART0 reception	IC/OC channel 3
0 1 1 0 0 b	UART2 transmission	IC/OC channel 4
0 1 1 0 1 b	UART2 reception/ACK2	IC/OC channel 5
0 1 1 1 0 b	A/D converter	IC/OC channel 6
0 1 1 1 1 b	UART1 reception	IC/OC channel 7
1 0 0 0 0 b	UART1 transmission	–
1 0 0 0 1 b	–	–
1 0 0 1 0 b	–	–
1 0 0 1 1 b	UART4 transmission	–
1 0 1 0 0 b	UART4 reception	–
1 0 1 0 1 b	UART3 transmission	–
1 0 1 1 0 b	UART3 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X: 0 or 1 – Do not set.

## 14.3 Operations

### 14.3.1 DMA Enabled

When data transfer starts after setting the DMAE bit in the DMiCON register to 1 (enabled), the DMAC operates as listed below ( $i = 0$  to 3). If 1 is written to the DMAE bit when it is already set to 1, the DMAC also performs the following operations.

- The forward address pointer is reloaded with the SAR<sub>i</sub> register value when the DSD bit in the DMiCON register is 1 (forward), or the DAR<sub>i</sub> register value when the DAD bit in the DMiCON register is 1 (forward).
- The DMA<sub>i</sub> transfer counter is reloaded with the DMA<sub>i</sub> transfer counter reload register value.

### 14.3.2 DMA Request

The DMAC can generate a DMA request as triggered by the request source that is selected with the DMS bit and bits DSEL4 to DSEL0 in the DMiSL register ( $i = 0$  to 3) on each channel. Table 14.7 lists the Timing at Which the DMAS Bit Value Changes.

When a DMA request is generated, the DMAS bit becomes 1 (DMA requested) regardless of the DMAE bit status. If the DMAE bit is 1 (enabled) when this occurs, the DMAS bit becomes 0 (DMA not requested) immediately before a data transfer starts. This bit cannot be set to 1 by a program (writing 1 has no effect).

If the DMAE bit is 1, data transfers start immediately after a DMA request is generated, so the DMAS bit in almost all cases is 0 when read in a program. Read the DMAE bit to determine whether the DMAC is enabled. When a DMA request transfer cycle is shorter than the DMA transfer cycle, the number of transfer requests and the number of transfers do not match.

When a peripheral function is selected as the DMA source, relations with the interrupt control registers are as follows:

- DMA transfers are not affected by the I flag or interrupt control registers. DMA requests are always accepted even when interrupt requests are not accepted.
- The IR bit in the interrupt control register retains its value when a DMA transfer is accepted.

**Table 14.7 Timing at Which the DMAS Bit Value Changes**

DMA Source	DMAS Bit in the DMiCON Register	
	Timing at which the bit becomes 1	Timing at which the bit becomes 0
Software trigger	When the DSR bit in the DMiSL register is set to 1.	<ul style="list-style-type: none"> <li>• Immediately before a data transfer starts</li> <li>• When set to 0 by a program</li> </ul>
External source	When an input edge of pins $\overline{\text{INT0}}$ to $\overline{\text{INT5}}$ matches with what is selected by setting bits DSEL4 to DSEL0 and DMS in the DMiSL register.	
Peripheral function	When an interrupt request is generated by the peripheral function selected by setting the DMS bit and bits DSEL4 to DSEL0 in the DMiSL register. (If the IR bit in an interrupt control register is 0, the timing is when the IR bit becomes 1.)	

$i = 0$  to 3

### 14.3.3 Transfer Cycles

A transfer cycle is composed of a bus cycle to read data from a source address (source read), and a bus cycle to write data to a destination address (destination write). The number of read and write bus cycles varies with the source and destination addresses.

Figure 14.2 shows Source Read Cycle Example. For convenience, the destination write cycle is shown as one bus cycle and the source read cycles for the different conditions are shown. In reality, the destination write cycle is subject to the same conditions as the source read cycle, with the transfer cycle changing accordingly. When calculating transfer cycles, take into consideration each condition for the source read and the destination write cycle. For example, when data is transferred in 16-bit units, and the source and destination addresses are both odd addresses ((2) in Figure 14.2), two source read bus cycles and two destination write bus cycles are required.

#### 14.3.3.1 Effect of Source and Destination Addresses

When a 16-bit unit of data is transferred and the source address starts with an odd address, the source read cycle increments by one bus cycle, compared to a source address starting with an even address.

When a 16-bit unit of data is transferred and the destination address starts with an odd address, the destination write cycle increments by one bus cycle, compared to a destination address starting with an even address.

#### 14.3.3.2 Effect of Software Wait

For memory or SFR accesses in which one or more software wait states are inserted, the number of bus cycles required increases by an amount equal to the number of software wait states.

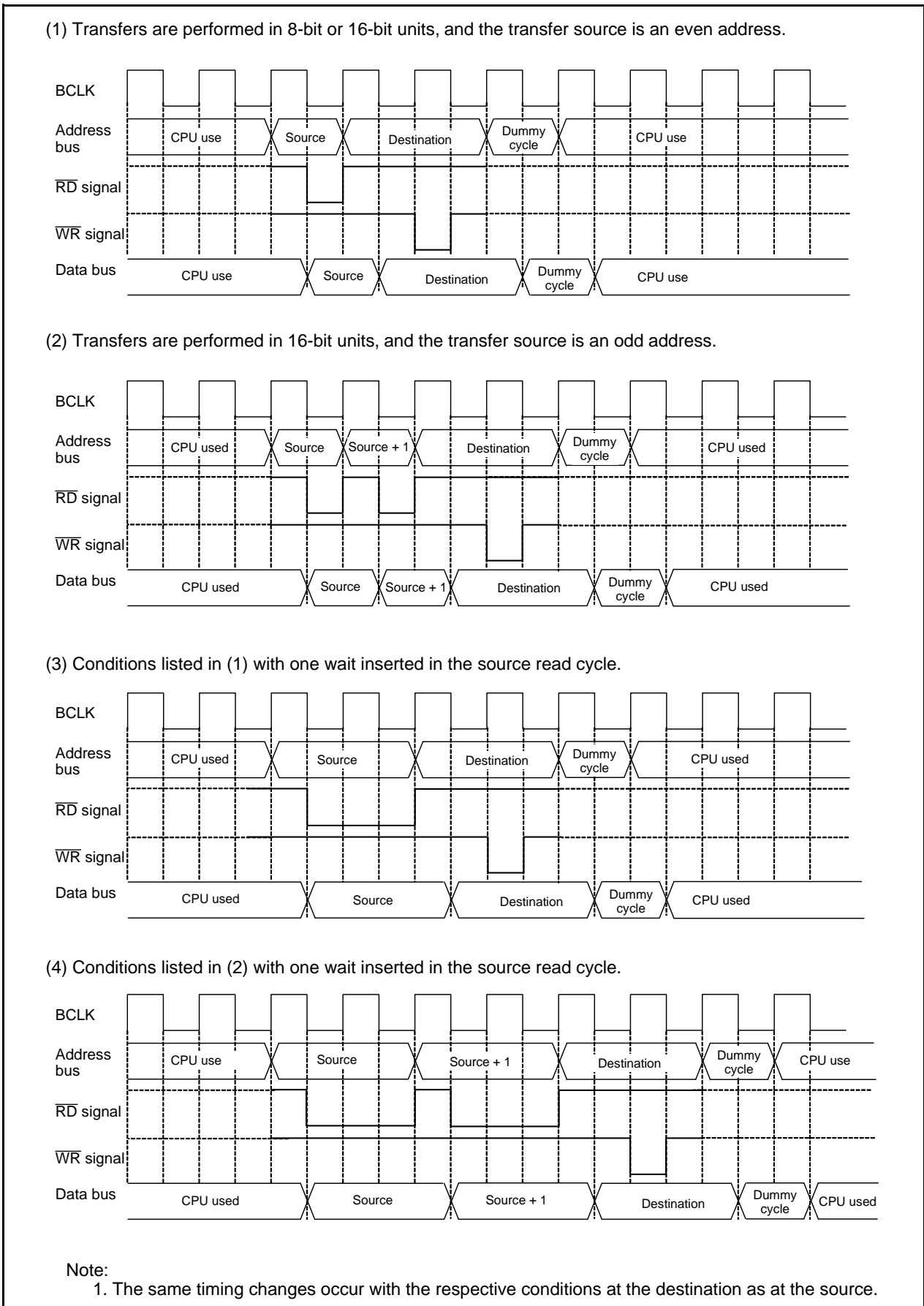


Figure 14.2 Source Read Cycle Example

### 14.3.4 DMAC Transfer Cycles

The formula for calculating the number of DMAC transfer cycles is shown below.

Number of transfer cycles per transfer unit = Number of read cycles  $\times$  j + Number of write cycles  $\times$  k

**Table 14.8 DMAC Transfer Cycles**

Transfer Unit	Access Address	Single-Chip Mode	
		Number of Read Cycles	Number of Write Cycles
8-bit transfers (DMBIT = 1)	Even	1	1
	Odd	1	1
16-bit transfers (DMBIT = 0)	Even	1	1
	Odd	2	2

DMBIT: Bit in the DMiCON register (i = 0 to 3)

**Table 14.9 Coefficients j and k**

	Internal Area		
	Internal ROM, RAM		SFR
	No waits inserted	Wait inserted	one wait inserted
j	1	2	2
k	1	2	2

### 14.3.5 Single Transfer Mode

In single transfer mode, the transfer stops when the DMAi transfer counter underflows. Figure 14.3 shows an Operation Example in Single Transfer Mode.

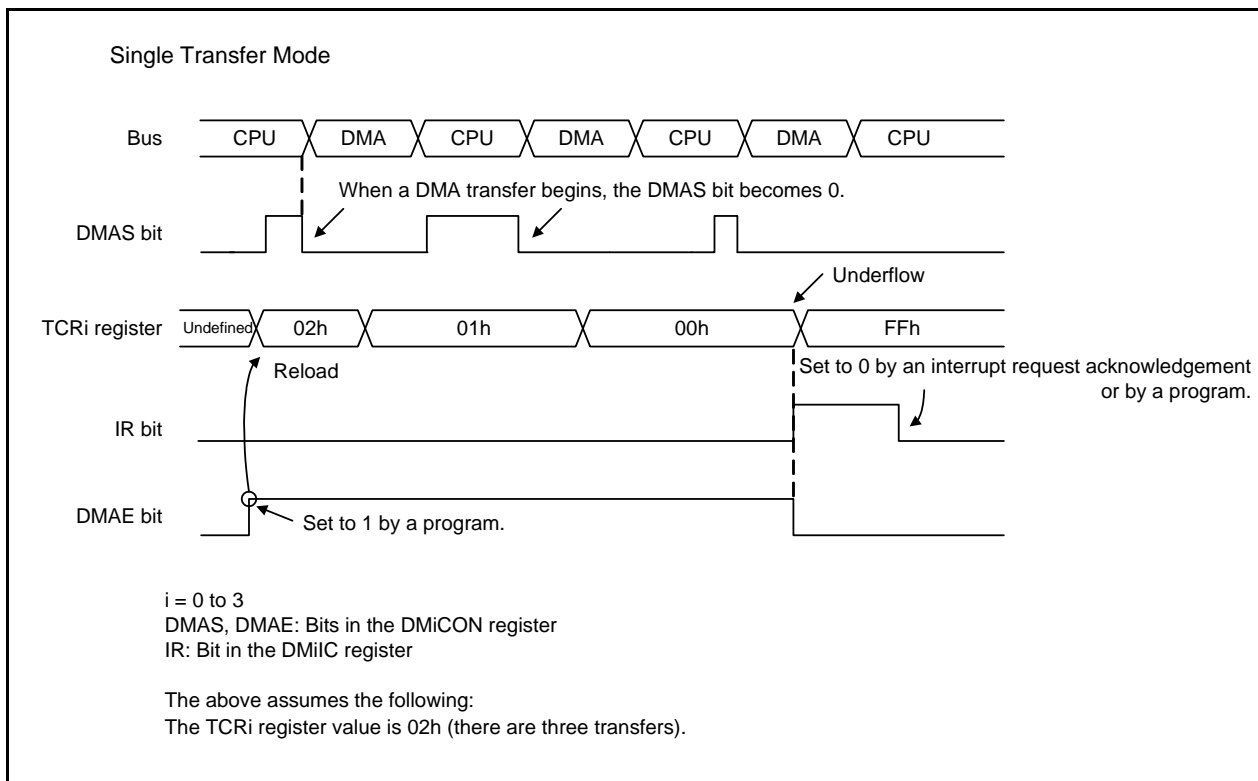


Figure 14.3 Operation Example in Single Transfer Mode

### 14.3.6 Repeat Transfer Mode

In repeat transfer mode, when the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register and DMA transfer continues. Figure 14.4 shows an Operation Example in Repeat Transfer Mode.

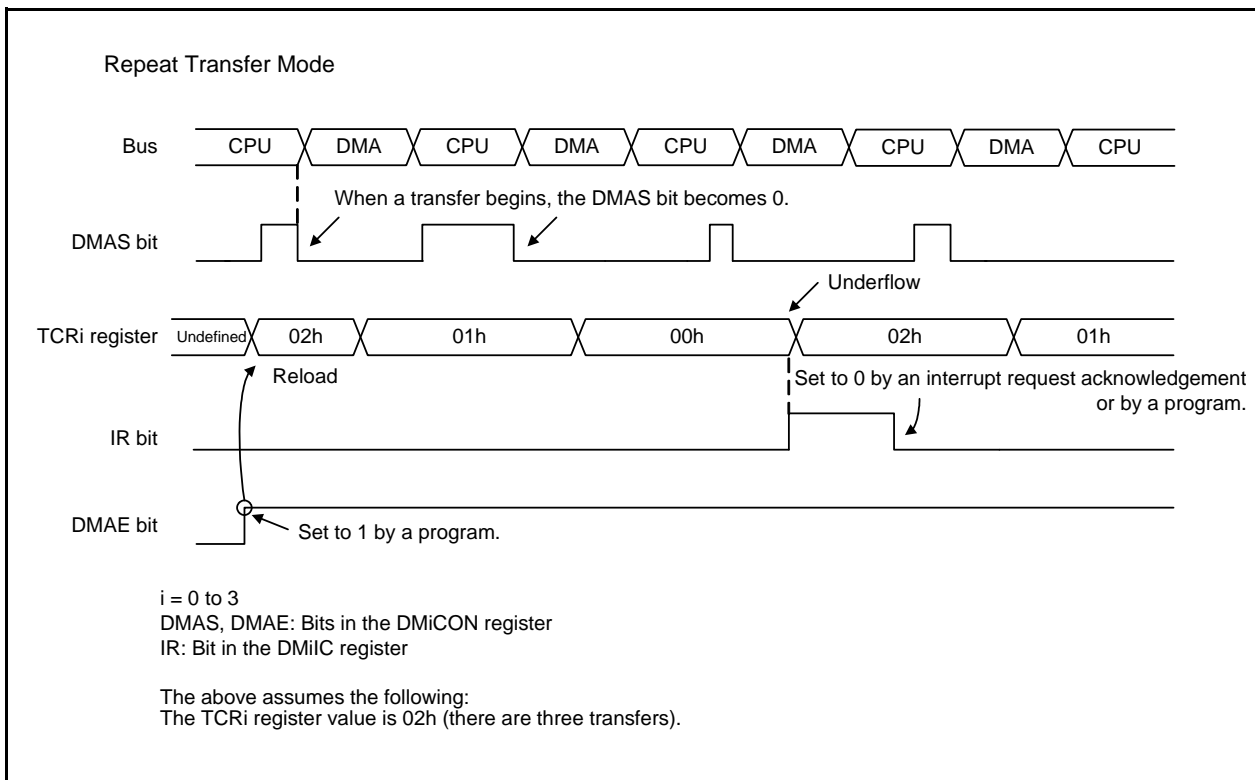


Figure 14.4 Operation Example in Repeat Transfer Mode

### 14.3.7 Channel Priority and DMA Transfer Timing

If multiple channels among DMA0 to DMA3 are enabled and DMA transfer request signals are detected as active in the same sampling period (one period from a falling edge to the next falling edge of BCLK), the DMAS bit on each channel becomes 1 (DMA requested) at the same time. In this case, the DMA requests are arbitrated according to the following channel priority: DMA0 > DMA1 > DMA2 > DMA3. DMAC operation when DMA0 and DMA1 requests are detected as active in the same sampling period is described below. Figure 14.5 shows an example of DMA Transfer Initiated by External Sources.

In Figure 14.5, as DMA0 and DMA1 requests are generated simultaneously, the higher channel prioritized DMA0 is received first, and data transfer starts. After one DMA0 transfer is completed, the bus access privilege is returned to the CPU. When the CPU has completed one bus access, a DMA1 transfer starts. After one DMA1 transfer is completed, the bus access privilege is again returned to the CPU.

In addition, DMA requests cannot increment since each channel has one DMAS bit. Therefore, when DMA requests, such as DMA1 in Figure 14.5, occur more than once, the DMAS bit is set to 0 after receiving the bus access privilege. The bus access privilege is returned to the CPU when one transfer is completed.

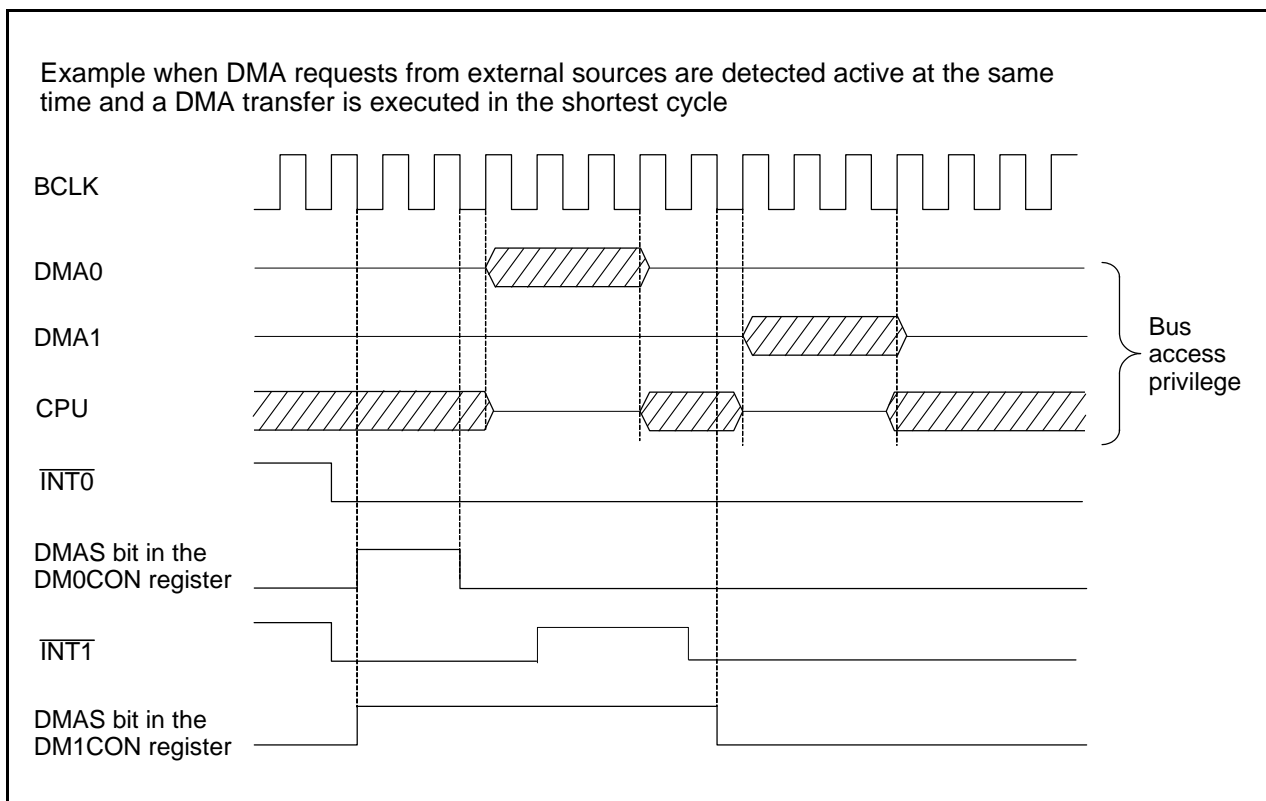


Figure 14.5 DMA Transfer Initiated by External Sources



## 14.4 Interrupts

Refer to operation examples for interrupt request generation timing.  
For details on interrupt control, refer to 12.7 "Interrupt Control".

**Table 14.10 DMAC Interrupt Related Registers**

Address	Register	Symbol	Reset Value
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b

When the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested) (i = 0 to 3). Therefore, set the DMAS bit to 0 (DMA not requested) after the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed. Refer to 12.13 "Notes on Interrupts" for more details.

## 14.5 Notes on DMAC

### 14.5.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

(Technical update number: TN-M16C-92-0306)

When both of the following conditions are met, follow steps (1) and (2) below.

#### Conditions

- Write 1 (DMAi is in active state) to the DMAE bit when it is 1.
- A DMA request may be generated simultaneously when writing to the DMAE bit.

#### Steps

- (1) Set bits DMAE and DMAS in the DMiCON register to 1 simultaneously. <sup>(1)</sup>
- (2) Make sure the DMAi circuit is in an initialized state <sup>(2)</sup> by a program.  
If DMAi is not in an initialized state, repeat these two steps.

#### Notes:

1. The DMAS bit does not change even if set to 1. However, it becomes 0 when set to 0 (DMA not requested). Therefore, when writing to the DMiCON register to set the DMAE bit to 1, set the value to be written to the DMAS bit to 1 to retain its state immediately before writing. Similarly, when writing to the DMAE bit with a read-modify-write instruction, set the DMAS bit to 1 to retain the DMA request that was generated while executing the instruction.
2. Read the TCRi register to verify whether DMAi is in an initialized state.  
If the read value is equal to the value that was written to the TCRi register before the DMA transfer started, DMAi is in an initialized state. When a DMA request is generated after writing to the DMAE bit, the read value is a value written to the TCRi register minus 1. If the read value is a value in the middle of a transfer, DMAi is not in an initialized state.

### 14.5.2 Changing the DMA Request Source

When the DMS bit or any of bits from DSEL4 to DSEL0 in the DMiSL register is changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Set the DMAS bit to 0 (DMA not requested) after changing the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register.

## 15. Timer A

### 15.1 Introduction

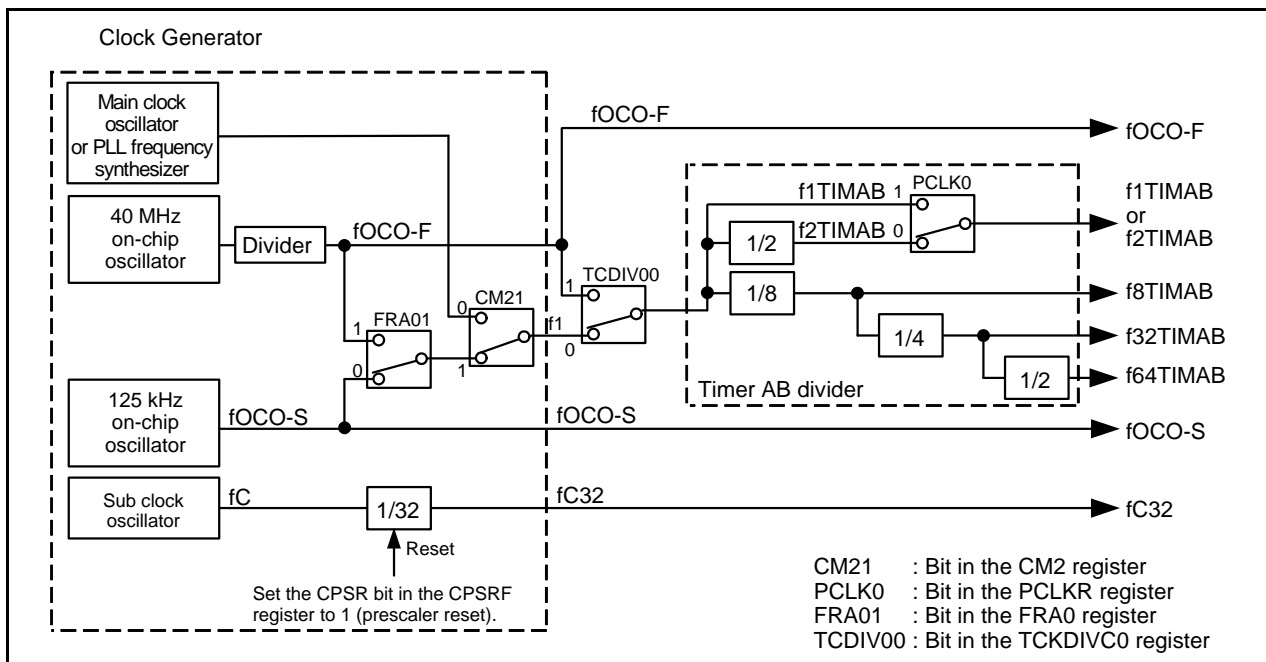
Timers A consists of timers A0 to A4. Each timer operates independently of the others. Table 15.1 lists Timer A Specifications, Table 15.2 lists Differences in Timer A Mode, Figure 15.1 shows Timer A and B Count Sources, Figure 15.2 shows Timer A Configuration, Figure 15.3 shows Timer A Block Diagram, and Table 15.3 lists I/O Ports.

**Table 15.1 Timer A Specifications**

Item	Specification
Configuration	16-bit timer x 5
Operating modes	<ul style="list-style-type: none"> <li>• Timer mode The timer counts an internal count source.</li> <li>• Event counter mode The timer counts pulses from an external device, or overflows and underflows of other timers.</li> <li>• One-shot timer mode The timer outputs a single pulse before it reaches the count 0000h.</li> <li>• Pulse width modulation mode (PWM mode) The timer outputs pulses of given width and cycle successively.</li> <li>• Programmable output mode The timer outputs a given pulse width of a high/low level signal (timers A1, A2, and A4).</li> </ul>
Interrupt sources	Overflow/underflow x 5

**Table 15.2 Differences in Timer A Mode**

Item	Timer				
	A0	A1	A2	A3	A4
Event counter mode (two-phase pulse signal processing)	No	No	Yes	Yes	Yes
Programmable output mode	No	Yes	Yes	No	Yes



**Figure 15.1 Timer A and B Count Sources**

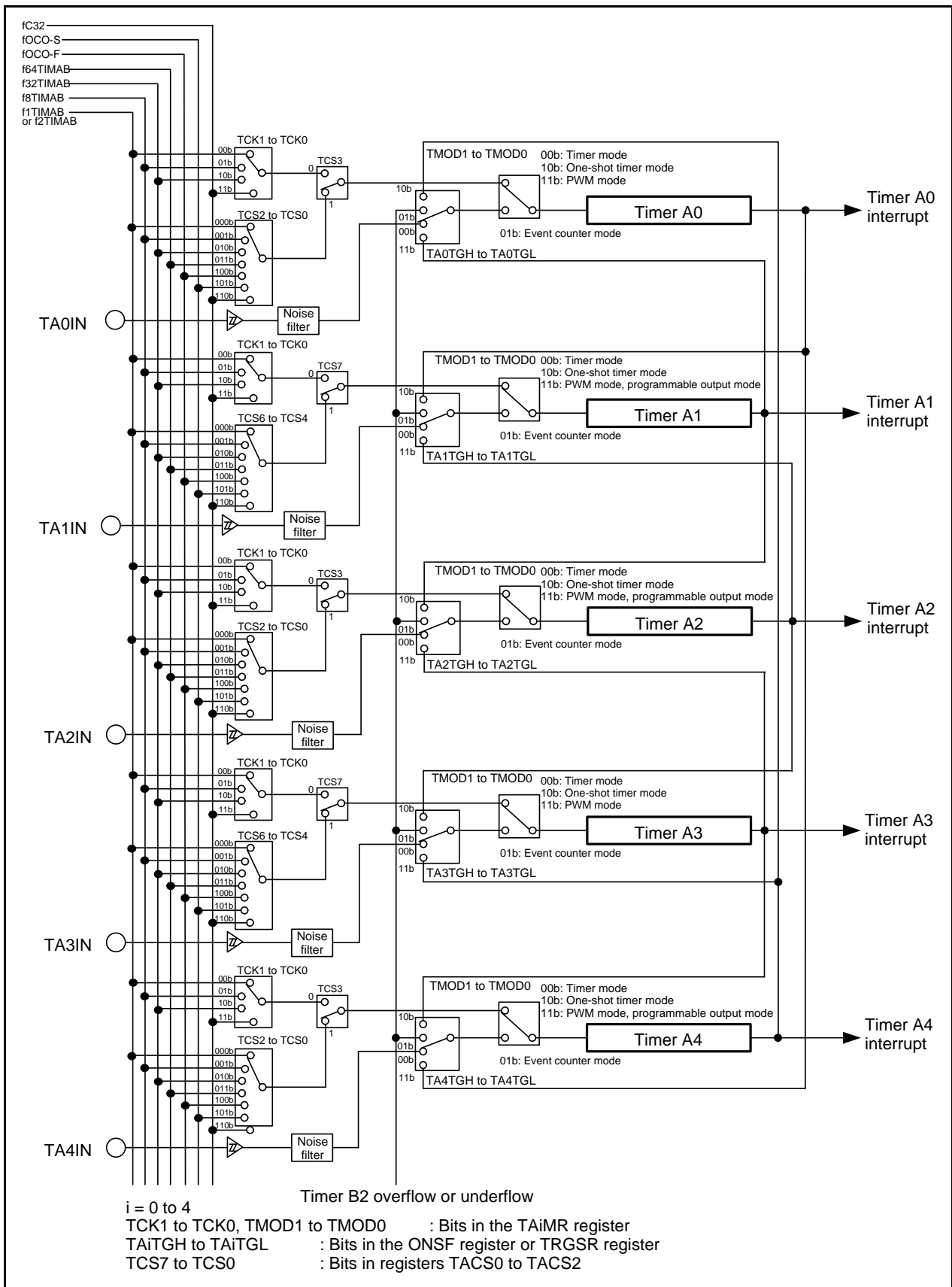


Figure 15.2 Timer A Configuration

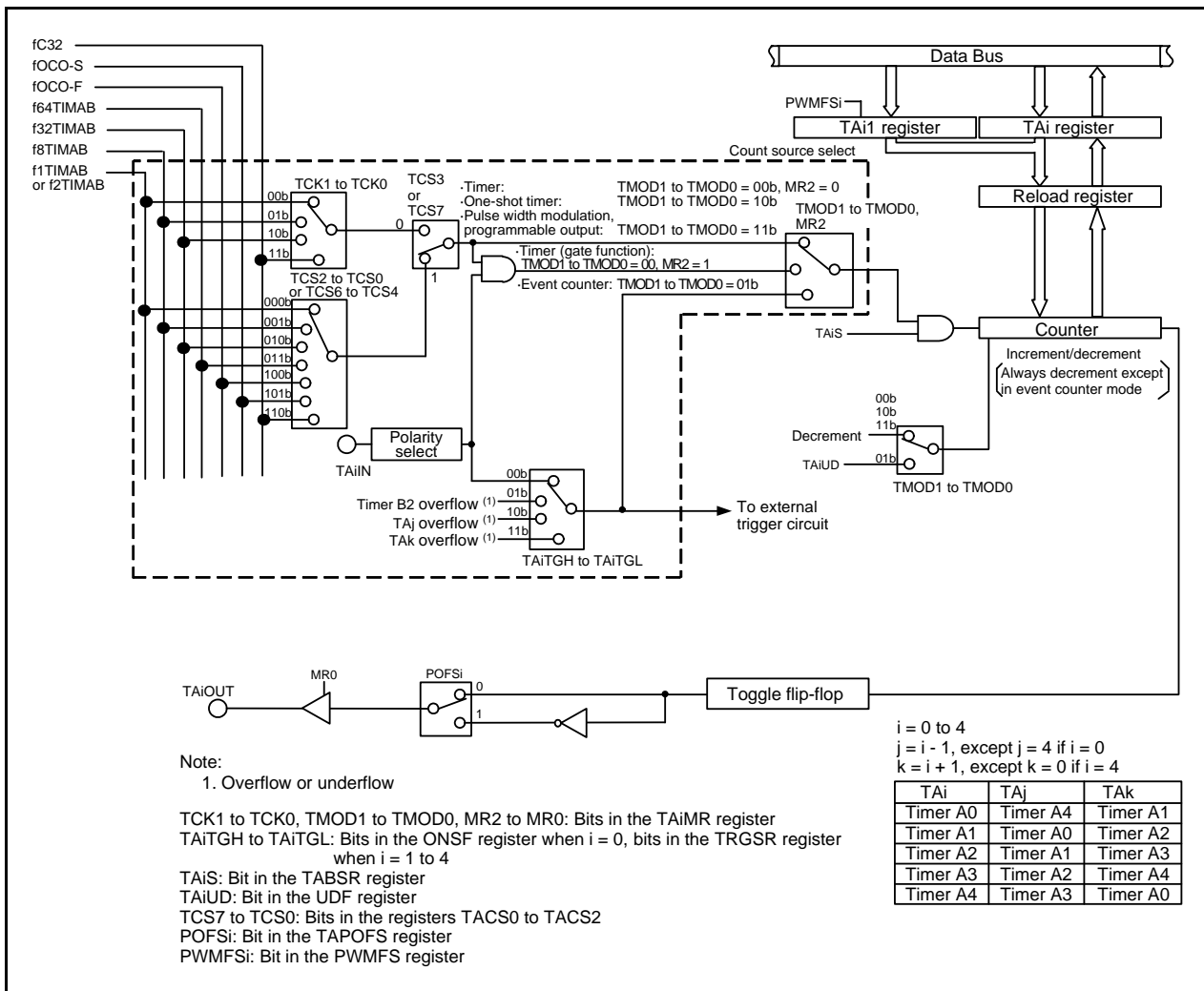


Figure 15.3 Timer A Block Diagram

Table 15.3 I/O Ports

Pin Name	I/O	Function
TA <sub>i</sub> IN	Input (1)	Gate input (timer mode) Count source input (event counter mode) Two-phase signal input (event counter mode (two-phase pulse signal processing)) Trigger input (one-shot timer mode, PWM mode, programmable output mode)
TA <sub>i</sub> OUT	Output	Pulse output (timer mode, event counter mode, one-shot timer mode, PWM mode, and programmable output mode)
	Input (1)	Two-phase pulse input (event counter mode (two-phase pulse signal processing))
ZP	Input (1)	Z-phase (counter initialization) input (event counter mode (two-phase pulse signal processing))

i = 0 to 4; however, i = 2, 3, 4 for two-phase pulse input, and i = 1, 2, 4 in programmable output mode

Note:

- When using pins TA<sub>i</sub>IN, TA<sub>i</sub>OUT, and ZP for input, set the port direction bits sharing pins to 0 (input mode).

## 15.2 Registers

Table 15.4 lists registers associated with timer A.

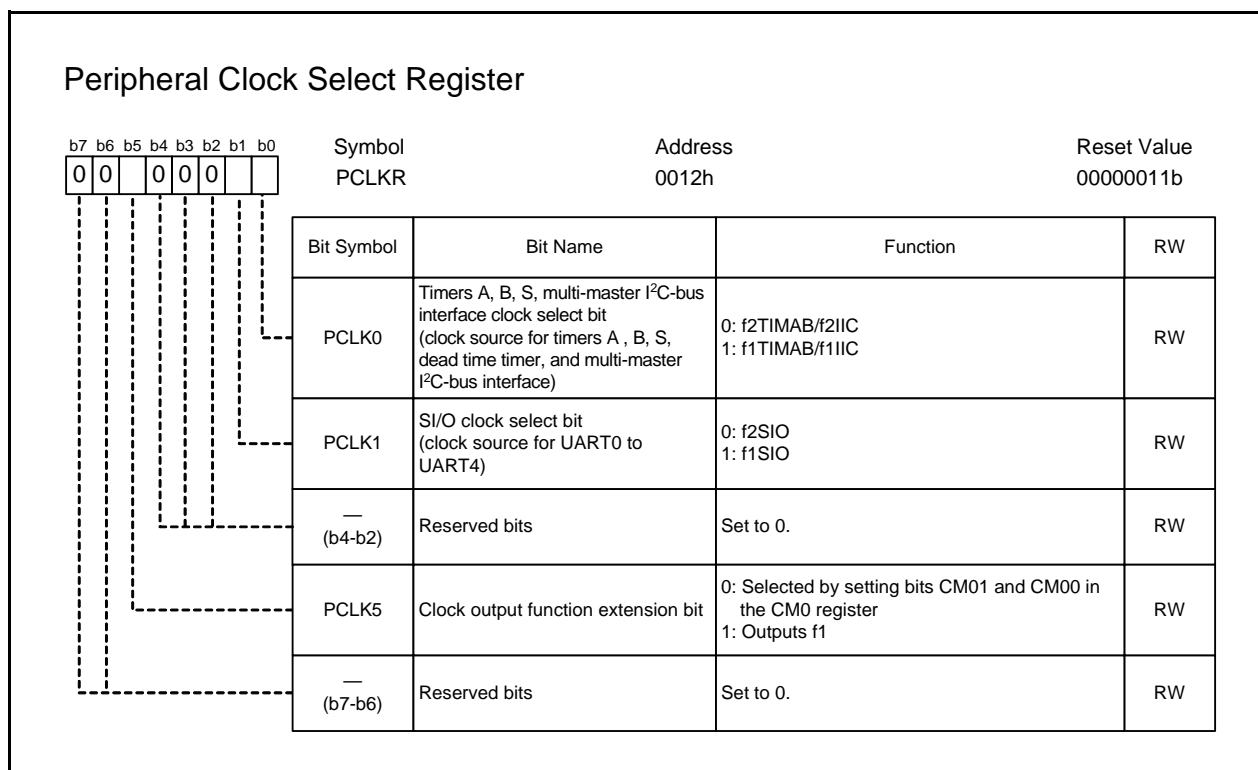
Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Refer to “registers and the setting” in each mode for registers and bit settings.

**Table 15.4 Registers**

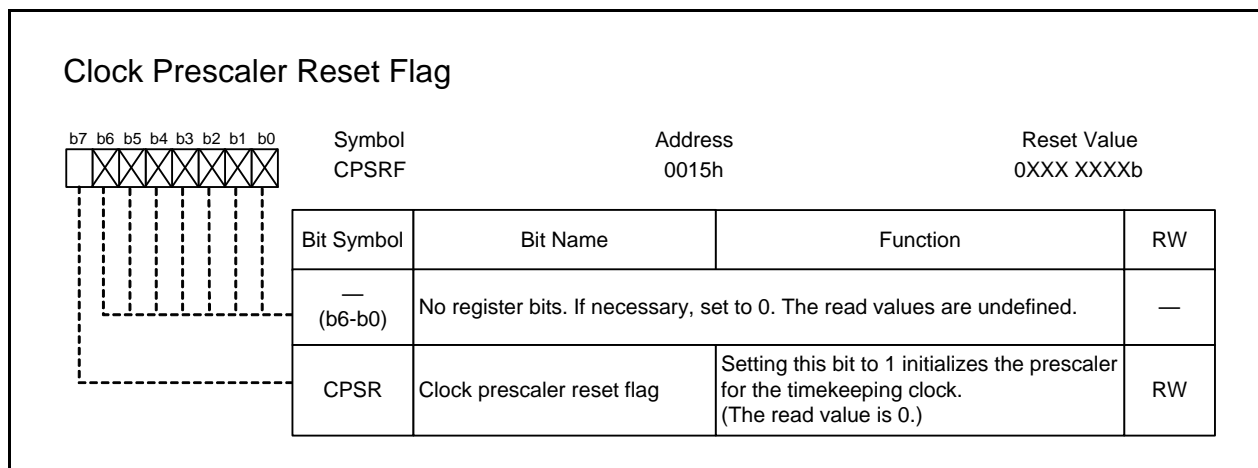
Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0320h	Count Start Flag	TABSR	00h
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h

### 15.2.1 Peripheral Clock Select Register (PCLKR)

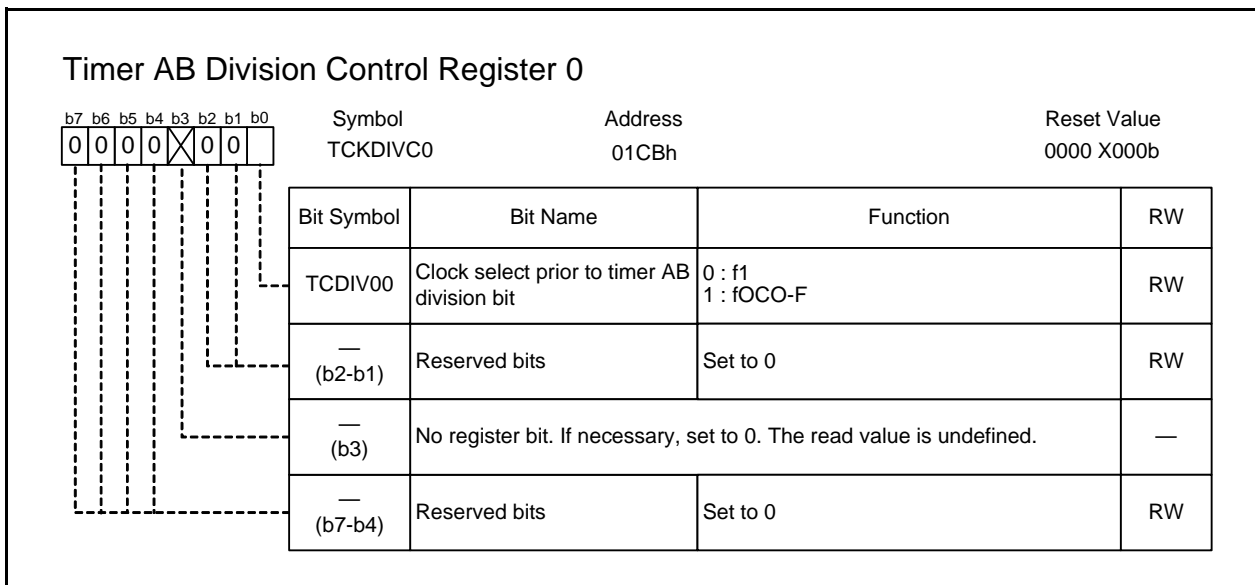


Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

### 15.2.2 Clock Prescaler Reset Flag (CPSRF)



### 15.2.3 Timer AB Division Control Register 0 (TCKDIVC0)



#### TCDIV00 (Clock select prior to timer AB division bit) (b0)

Set the TCDIV00 bit while timers A and B are stopped.

Set the TCDIV00 bit before setting other registers associated with timer A.

After changing the TCDIV00 bit, set other registers associated with timer A again.



### 15.2.4 Timer A Count Source Select Register i (TACSi) (i = 0 to 2)

Timer A Count Source Select Register 0, Timer A Count Source Select Register 1

Symbol	Address	Reset Value
TACS0 to TACS1	01D0h to 01D1h	00h

Bit Symbol	Bit Name	Function	RW
TCS0	TA <sub>i</sub> count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB	RW
TCS1		0 0 1 : f8TIMAB	RW
TCS2		0 1 0 : f32TIMAB	RW
TCS3		0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS3	TA <sub>i</sub> count source option specified bit	0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled 1 : TCK0, TCK1 disabled, TCS0 to TCS2 enabled	RW
TCS4	TA <sub>j</sub> count source select bit	b6 b5 b4 0 0 0 : f1TIMAB or f2TIMAB	RW
TCS5		0 0 1 : f8TIMAB	RW
TCS6		0 1 0 : f32TIMAB	RW
TCS7		0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS7	TA <sub>j</sub> count source option specified bit	0 : TCK0, TCK1 enabled, TCS4 to TCS6 disabled 1 : TCK0, TCK1 disabled, TCS4 to TCS6 enabled	RW

TACS0 register: i = 0, j = 1      TACS1 register: i = 2, j = 3

Timer A Count Source Select Register 2

Symbol	Address	Reset Value
TACS2	01D2h	X0h

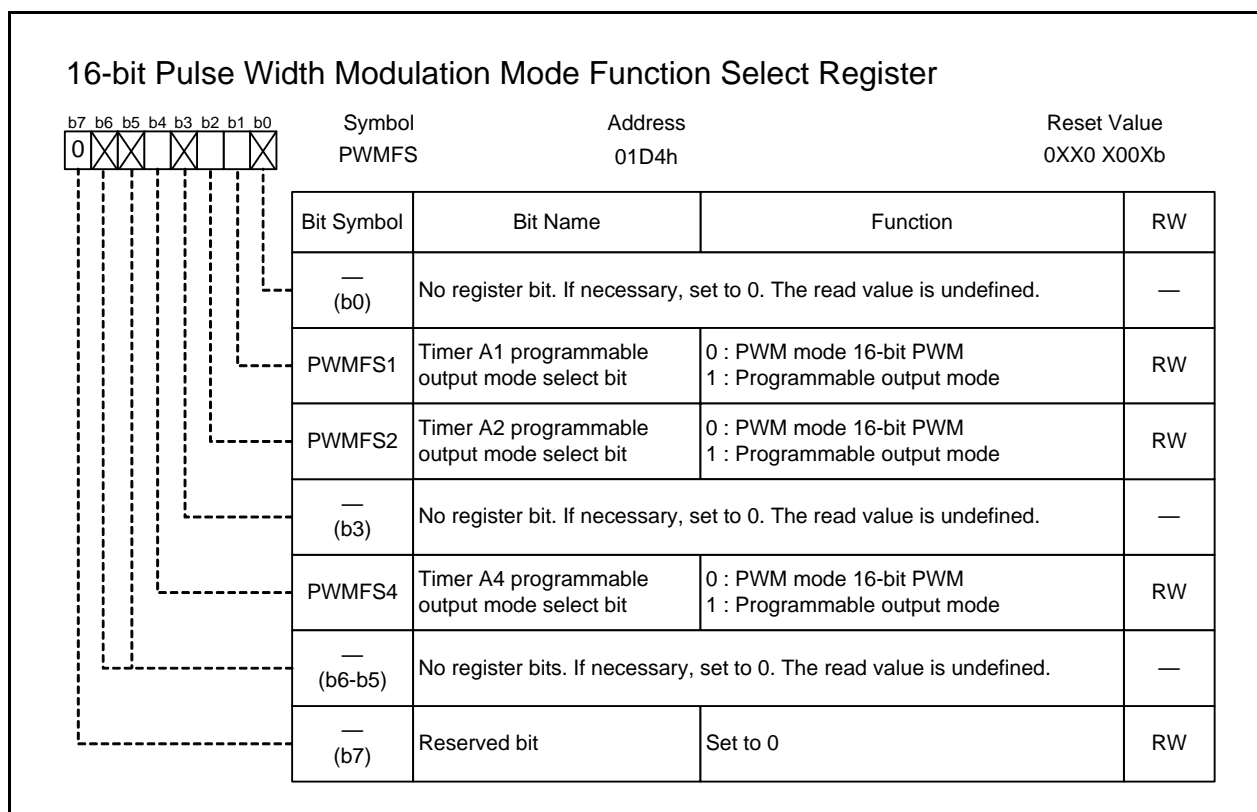
Bit Symbol	Bit Name	Function	RW
TCS0	TA4 count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB	RW
TCS1		0 0 1 : f8TIMAB	RW
TCS2		0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS3	TA4 count source option specified bit	0 : TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1 : TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. The read values are undefined.		—

TCS2 to TCS0 (TA<sub>i</sub> count source select bit) (b2-b0) (i = 0, 2, 4)

TCS6 to TCS4 (TA<sub>j</sub> count source select bit) (b6-b4) (i = 1, 3)

Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.

### 15.2.5 16-bit Pulse Width Modulation Mode Function Select Register (PWMFS)



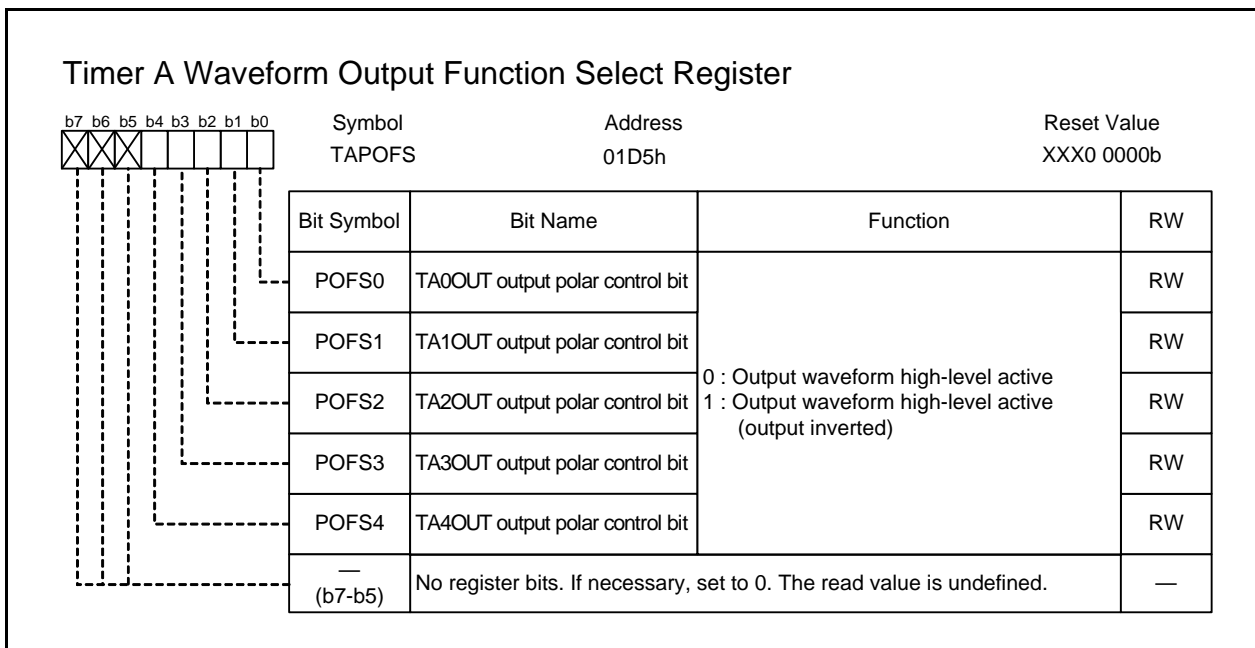
PWMFS1 (Timer A1 programmable output mode select bit) (b1)

PWMFS2 (Timer A2 programmable output mode select bit) (b2)

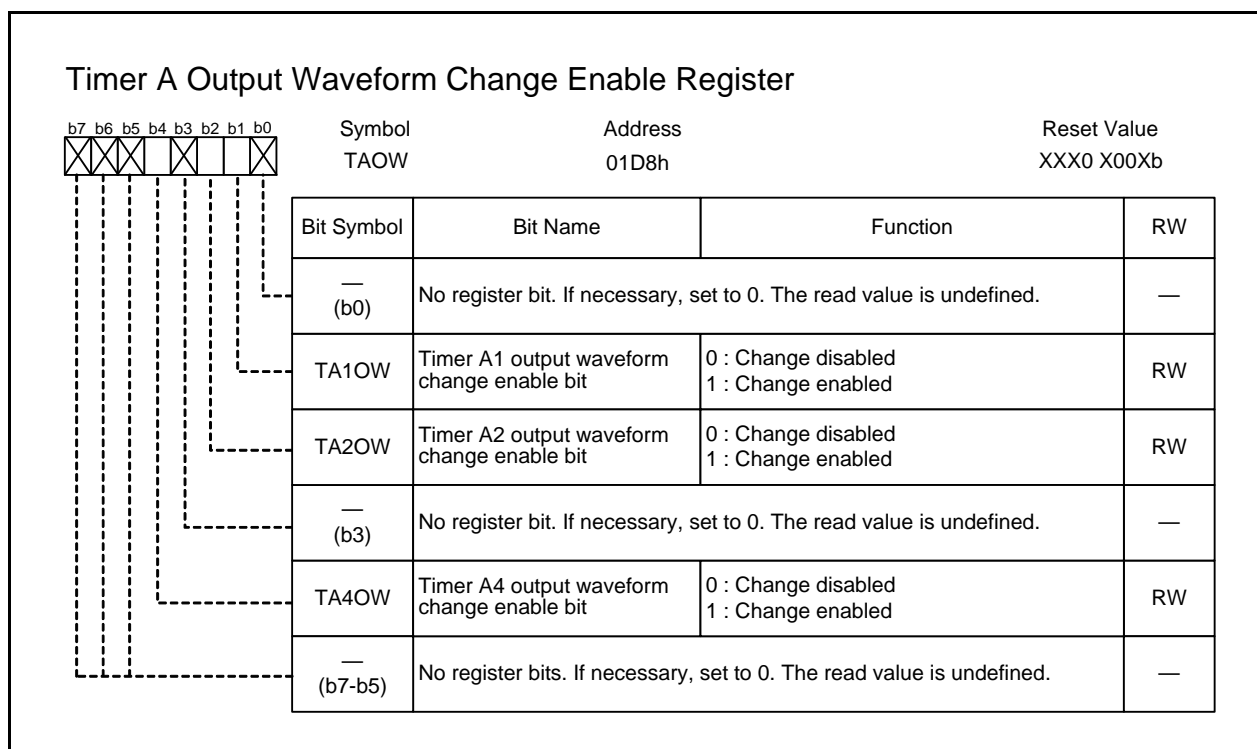
PWMFS4 (Timer A4 programmable output mode select bit) (b4)

These bits are enabled when bits TMOD1 to TMOD0 in the TAIiMR register are 11b (PWM mode or programmable output mode), and the MR3 bit in the TAIiMR register is 0 (16-bit PWM mode).

### 15.2.6 Timer A Waveform Output Function Select Register (TAPOFS)



## 15.2.7 Timer A Output Waveform Change Enable Register (TAOW)



The TAOW register is enabled in programmable output mode.

To change cycles or width of the output waveform, follow the instructions below.

- (1) Set the TAIOW bit to 0 (output waveform change disabled). (i = 1, 2, 4)
- (2) Write to the TAI register and/or the TAI1 register.
- (3) Set the TAIOW bit to 1 (output waveform change enabled).

The updated value is reloaded when the TAIOW bit is 1 (output waveform change enabled) at one cycle before the rising edge of the TAIOUT output (the falling edge when the POFSi bit is 1). The value before the update is reloaded when the TAIOW bit is 0 (output waveform change disabled).

## 15.2.8 Timer Ai Register (TAi) (i = 0 to 4)

Timer Ai Register (i = 0 to 4)																					
<div style="display: flex; justify-content: space-around;"> <span>(b15) b7</span> <span>(b8) b0 b7</span> <span>b0</span> </div>	<table border="1"> <thead> <tr> <th>Symbol</th> <th>Address</th> <th>Reset Value</th> </tr> </thead> <tbody> <tr> <td>TA0</td> <td>0327h to 0326h</td> <td>XXXXh</td> </tr> <tr> <td>TA1</td> <td>0329h to 0328h</td> <td>XXXXh</td> </tr> <tr> <td>TA2</td> <td>032Bh to 032Ah</td> <td>XXXXh</td> </tr> <tr> <td>TA3</td> <td>032Dh to 032Ch</td> <td>XXXXh</td> </tr> <tr> <td>TA4</td> <td>032Fh to 032Eh</td> <td>XXXXh</td> </tr> </tbody> </table>	Symbol	Address	Reset Value	TA0	0327h to 0326h	XXXXh	TA1	0329h to 0328h	XXXXh	TA2	032Bh to 032Ah	XXXXh	TA3	032Dh to 032Ch	XXXXh	TA4	032Fh to 032Eh	XXXXh		
Symbol	Address	Reset Value																			
TA0	0327h to 0326h	XXXXh																			
TA1	0329h to 0328h	XXXXh																			
TA2	032Bh to 032Ah	XXXXh																			
TA3	032Dh to 032Ch	XXXXh																			
TA4	032Fh to 032Eh	XXXXh																			
Mode	Function	Setting Range	RW																		
Timer mode	When n is a setting value, counter cycle: $\frac{(n + 1)}{f_j}$	0000h to FFFFh	RW																		
Event counter mode	When n is a set value, FFFFh - n + 1 count (at increment) n + 1 count (at decrement)	0000h to FFFFh	RW																		
One-shot timer mode	When n is a set value, pulse width: $\frac{n}{f_j}$	0000h to FFFFh	WO																		
Pulse width modulation mode (16-bit PWM mode)	When n is a set value, PWM period: $\frac{(2^{16} - 1)}{f_j}$ PWM pulse width: $\frac{n}{f_j}$	0000h to FFFEh	WO																		
Pulse width modulation mode (8-bit PWM mode)	When n is an upper address setting value, and m is a lower address setting value, PWM period: $\frac{(2^8 - 1) \times (m + 1)}{f_j}$ PWM pulse width: $\frac{(m + 1)n}{f_j}$	00h to FEh (upper address) 00h to FFh (lower address)	WO																		
Programmable output mode	When n is a setting value of TAI1 register, and m is a setting value of TAI register, high-level duration: $\frac{m}{f_j}$ low-level duration: $\frac{n}{f_j}$	0000h to FFFFh	WO																		

$f_j$  : Count source frequency

Access the register in 16-bit units. Use the MOV instruction to write to the TAI register.

### Event Counter Mode

The timer counts pulses from an external device, or the overflows/underflows of other timers.

### One-Shot Timer Mode

If the TAI register is set to 0000h, the counter does not work and timer Ai interrupt requests are not generated. Furthermore, if pulse output is selected, no pulses are output from the TAIOUT pin.

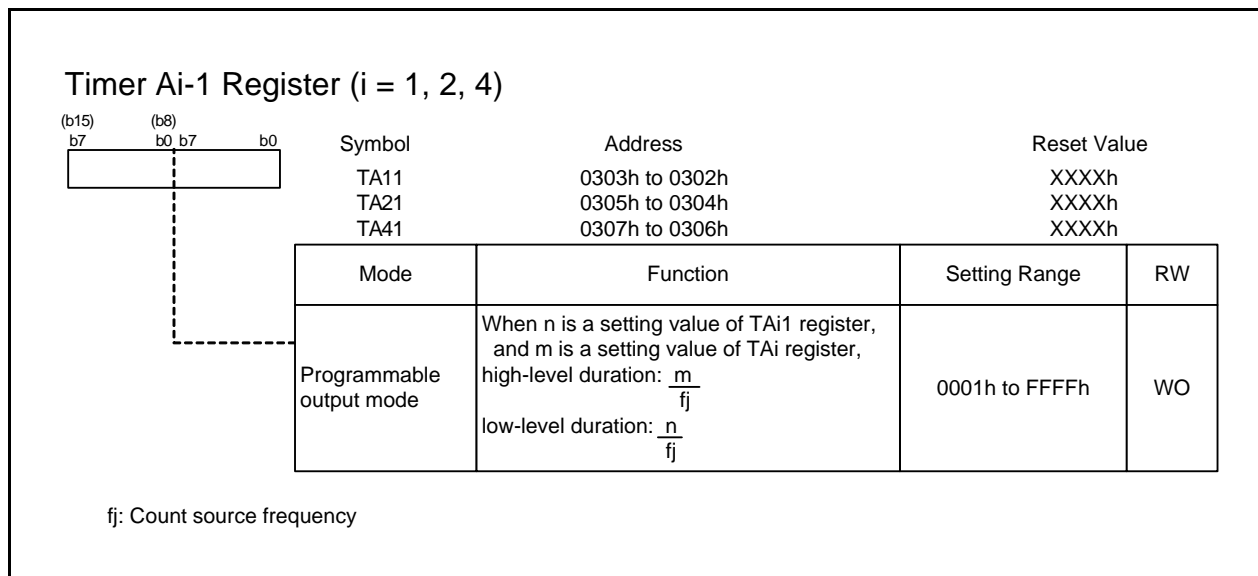
### Pulse Width Modulation Mode (16-bit PWM mode)

When the TAI register is set to 0000h, the counter does not work, the output level on the TAIOUT pin remains low, and timer Ai interrupt requests are not generated.

### Pulse Width Modulation Mode (8-bit PWM mode)

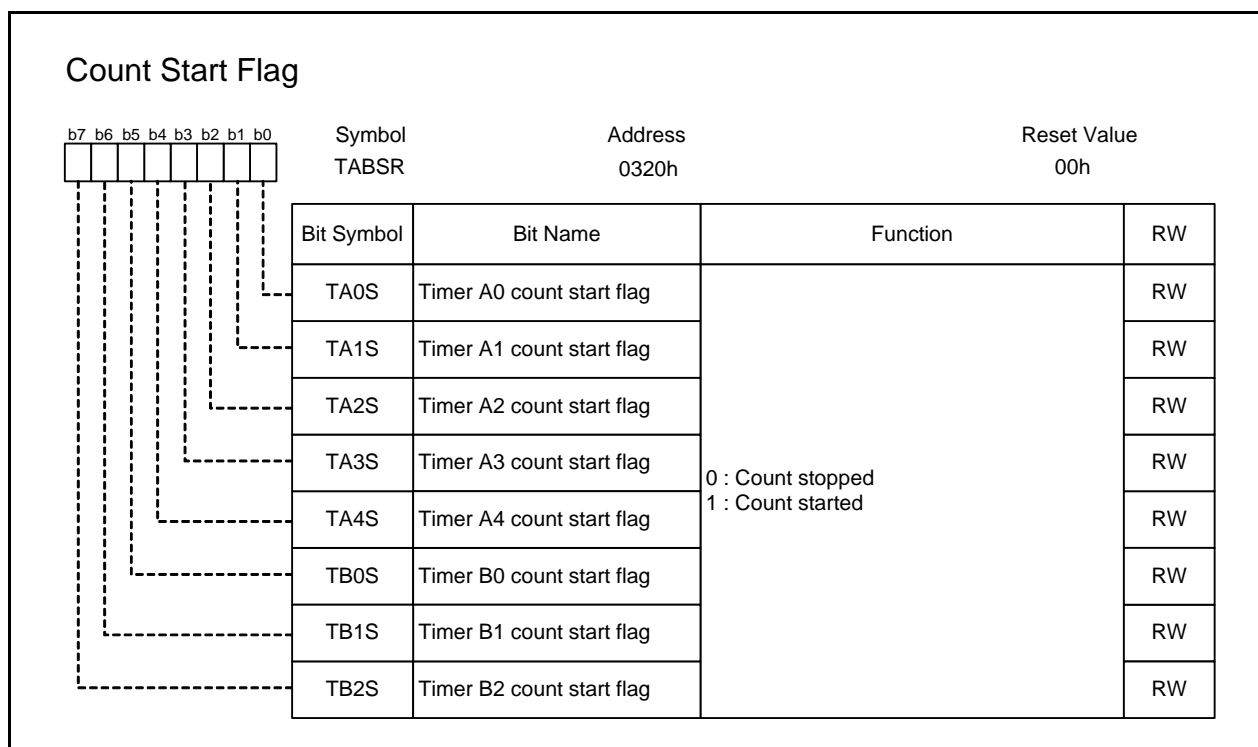
This mode operates as an 8-bit prescaler (lower 8 bits) and an 8-bit pulse width modulator (upper 8 bits). When the upper 8 bits of the TAI register are set to 00h, the counter does not work, the output level on the TAIOUT pin remains low, and a timer Ai interrupt request is not generated.

### 15.2.9 Timer Ai-1 Register (TAi1) (i = 1, 2, 4)



Access the register in 16-bit units. Use the MOV instruction to write to the TAi1 register.

### 15.2.10 Count Start Flag (TABSR)



### 15.2.11 One-Shot Start Flag (ONSF)

One-Shot Start Flag		Symbol	Address	Reset Value
		ONSF	0322h	00h
Bit Symbol	Bit Name	Function	RW	
TA0OS	Timer A0 one-shot start flag	The timer starts counting by setting this bit to 1. The read values are 0.	RW	
TA1OS	Timer A1 one-shot start flag		RW	
TA2OS	Timer A2 one-shot start flag		RW	
TA3OS	Timer A3 one-shot start flag		RW	
TA4OS	Timer A4 one-shot start flag		RW	
TAZIE	Z-phase input enable bit	0 : Z-phase input disabled 1 : Z-phase input enabled	RW	
TA0TGL	Timer A0 event/trigger select bit	b7 b6 0 0 : Input on TA0IN pin selected 0 1 : Timer B2 selected 1 0 : Timer A4 selected 1 1 : Timer A1 selected	RW	
TA0TGH			RW	

#### TAiOS (Timer Ai one-shot start flag) (b4-b0) (i = 0 to 4)

This bit is enabled in one-shot timer mode. When the MR2 bit in the TAI register is 0 (TAiOS bit enabled), the timer Ai count starts by setting the TAIOS bit to 1 after setting the TAI5 bit in the TABSR register to 1 (start counting).

#### TAZIE (Z-phase input enable bit) (b5)

This bit is used in event counter mode (two-phase pulse signal processing) of timer A3. Refer to 15.3.4.3 "Counter Initialization Using Two-Phase Pulse Signal Processing" for details.

#### TA0TGH-TA0TGL (Timer A0 event/trigger select bit) (b7-b6)

These bits are used to select an event or a trigger in the following modes:

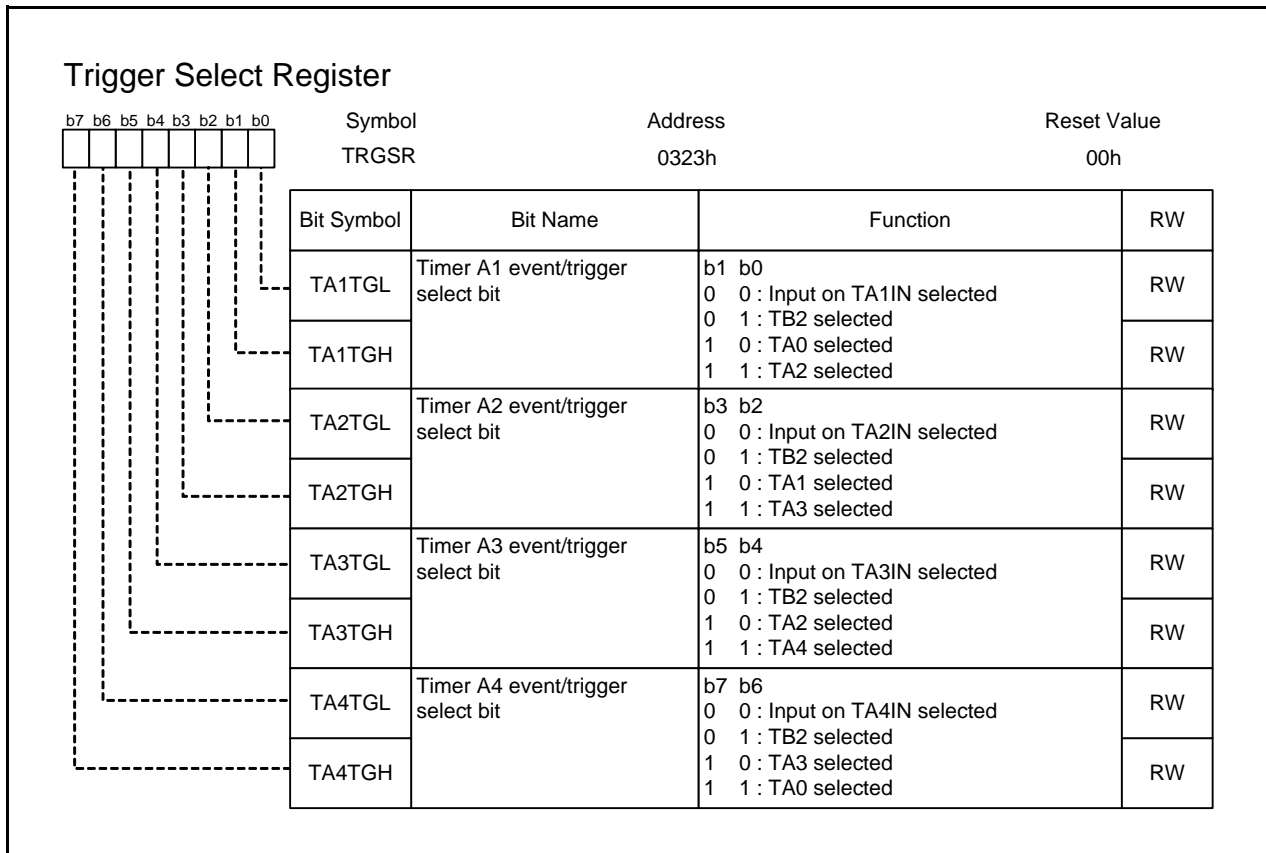
- An event in event counter mode (when not using two-phase pulse signal processing)
- A trigger in one-shot timer mode or PWM mode

The above applies when the MR2 bit in the TA0MR register is 1 (trigger selected by setting bits TA0TGH to TA0TGL).

When bits TA0TGH to TA0TGL are 00b, the active edge of input signals can be selected by setting the MR1 bit in the TA0MR register.

When bits TA0TGH to TA0TGL are set to 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request for the selected timer is generated. An event or trigger can occur while interrupts are disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

### 15.2.12 Trigger Select Register (TRGSR)



TA1TGH-TA1TGL (Timer A1 event/trigger select bit) (b1-b0)

TA2TGH-TA2TGL (Timer A2 event/trigger select bit) (b3-b2)

TA3TGH-TA3TGL (Timer A3 event/trigger select bit) (b5-b4)

TA4TGH-TA4TGL (Timer A4 event/trigger select bit) (b7-b6)

These bits are used to select an event or a trigger of the following modes:

- An event in event counter mode (when not using two-phase pulse signal processing)
- A trigger in one-shot timer mode, PWM mode, or programmable output mode

The above applies when the MR2 bit in the TAI<sub>i</sub>MR register is 1 (trigger selected by setting bits TAI<sub>i</sub>TGH to TAI<sub>i</sub>TGL).

When bits TAI<sub>i</sub>TGH to TAI<sub>i</sub>TGL are 00b, the active edge of input signals can be selected by setting the MR1 bit in the TAI<sub>i</sub>MR register.

When bits TAI<sub>i</sub>TGH to TAI<sub>i</sub>TGL are set to 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. An event or trigger can occur while interrupts are disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.



### 15.2.13 Increment/Decrement Flag (UDF)

Increment/Decrement Flag		Symbol	Address	Reset Value
		UDF	0324h	00h
Bit Symbol	Bit Name	Function		RW
TA0UD	Timer A0 increment/ decrement flag	0 : Decrement 1 : Increment		RW
TA1UD	Timer A1 increment/ decrement flag			RW
TA2UD	Timer A2 increment/ decrement flag			RW
TA3UD	Timer A3 increment/ decrement flag			RW
TA4UD	Timer A4 increment/ decrement flag			RW
TA2P	Timer A2 two-phase pulse signal processing select bit	0 : Two-phase pulse signal processing disabled 1 : Two-phase pulse signal processing enabled		RW
TA3P	Timer A3 two-phase pulse signal processing select bit			RW
TA4P	Timer A4 two-phase pulse signal processing select bit			RW

TA<sub>i</sub>UD (Timer A<sub>i</sub> increment/decrement flag) (b<sub>4</sub> to b<sub>0</sub>) (i = 0 to 4)

Enabled in event counter mode (when not using two-phase pulse signal processing).

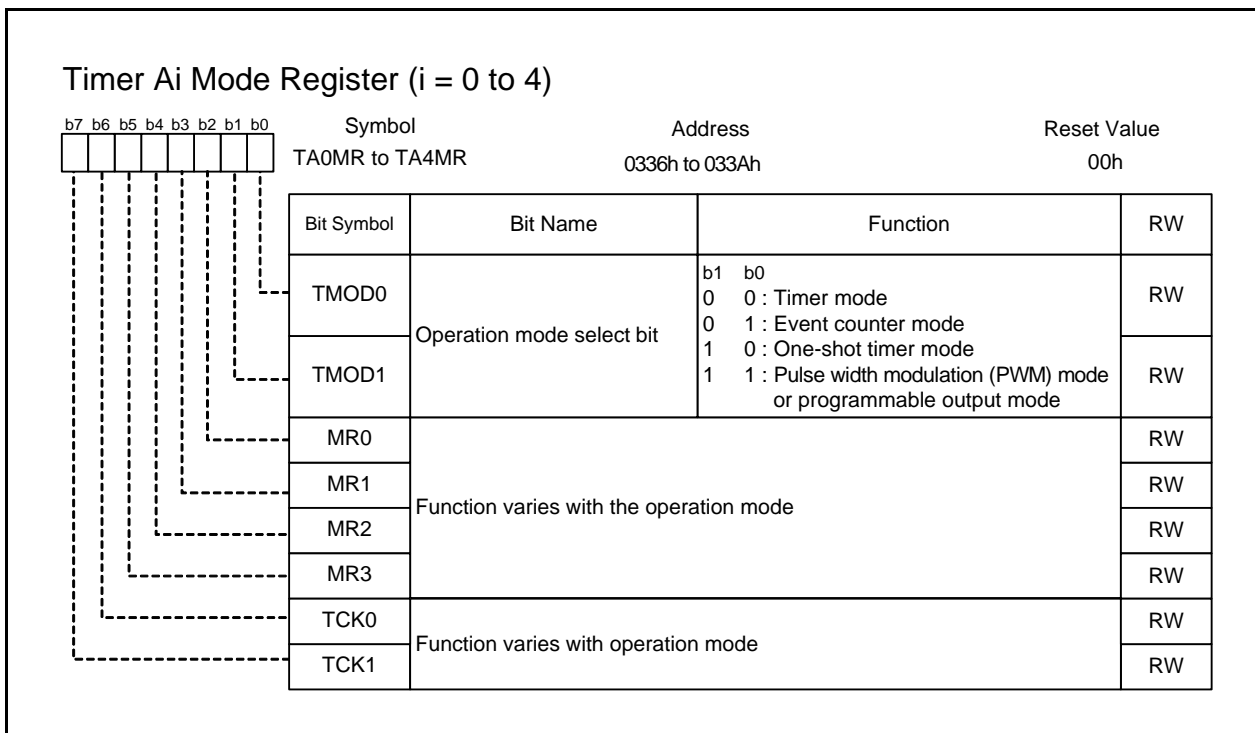
TA2P (Timer A2 two-phase pulse signal processing select bit) (b<sub>5</sub>)

TA3P (Timer A3 two-phase pulse signal processing select bit) (b<sub>6</sub>)

TA4P (Timer A4 two-phase pulse signal processing select bit) (b<sub>7</sub>)

Set these bits to 0 when not using two-phase pulse signal processing.

**15.2.14 Timer Ai Mode Register (TAiMR) (i = 0 to 4)**



## 15.3 Operations

### 15.3.1 Common Operations

#### 15.3.1.1 Operating Clock

The count source for each timer acts as a clock, controlling such timer operations as counting and reloading.

If the conditions to start counting are met, the stopped counter starts counting at the count timing of the first count source. For this reason, a delay exists between when the count start conditions are met and the counter starts counting. Figure 15.4 shows Output Example of One-Shot Timer Mode.

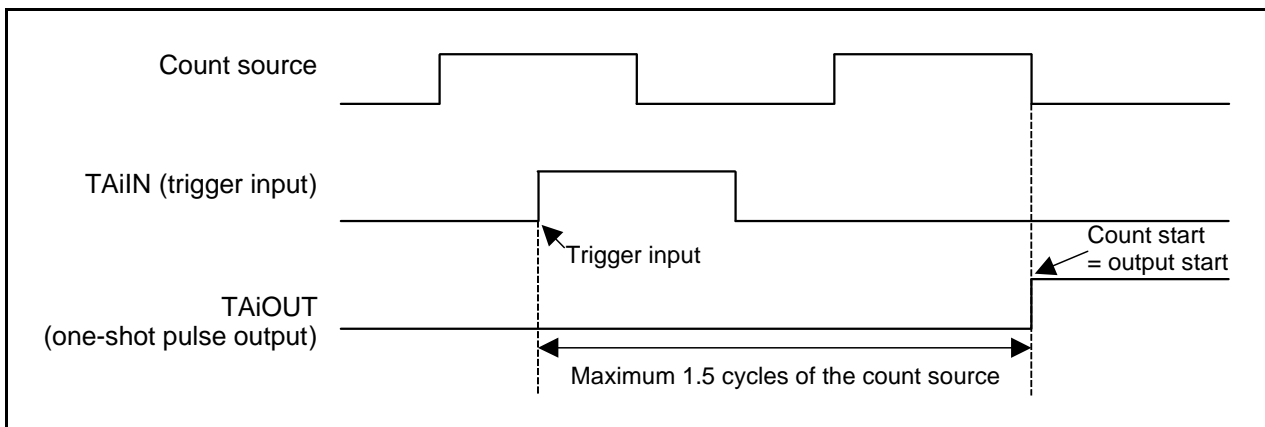


Figure 15.4 Output Example of One-Shot Timer Mode

#### 15.3.1.2 Counter Reload Timing

Timer Ai starts counting from the value set (n) in the TAI register. The TAI register consists of a counter and a reload register. The counter starts decrementing the count source from n, reloads a value in the reload register at the next count source after the value becomes 0000h, and continues decrementing. When incrementing, the counter reloads a value in the reload register at the next count source after the value becomes FFFFh.

The value written in the TAI register is reflected in the counter and the reload register at the following timings:

- When the count is stopped
- Between when the count starts and when the first count source is input
  - A value written to the TAI register is immediately written to the counter and the reload register.
- After the count starts and the first count source is input
  - A value written to the TAI register is immediately written to the reload register. The counter continues counting and reloads the value in the reload register at the next count source after the value becomes 0000h (or FFFFh).

### 15.3.1.3 Count Source

Internal clocks are counted in timer mode, one-shot timer mode, PWM mode, and programmable output mode. Refer to Figure 15.1 “Timer A and B Count Sources” for details. Table 15.5 lists the Timer A Count Sources.

f1 is any of the clocks listed below (refer to 8. “Clock Generator” for details).

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

**Table 15.5 Timer A Count Sources**

Count Source	Bit Setting Value				Remarks
	PCLK0	TCS3	TCS2 to TCS0	TCK1 to TCK0	
		TCS7	TCS6 to TCS4		
f1TIMAB	1	0	-	00b	f1 or fOCO-F (1)
		1	000b	-	
f2TIMAB	0	0	-	00b	f1 divided by 2 or fOCO-F divided by 2 (1)
		1	000b	-	
f8TIMAB	-	0	-	01b	f1 divided by 8 or fOCO-F divided by 8 (1)
		1	001b	-	
f32TIMAB	-	0	-	10b	f1 divided by 32 or fOCO-F divided by 32 (1)
		1	010b	-	
f64TIMAB	-	1	011b	-	f1 divided by 64 or fOCO-F divided by 64 (1)
fOCO-F	-	1	100b	-	fOCO-F
fOCO-S	-	1	101b	-	fOCO-S
fC32	-	0	-	11b	fC32
		1	110b	-	

PCLK0: Bit in the PCLKR register

TCS7 to TCS0: Bits in registers TACS0 to TACS2

TCK1 to TCK0: Bits in the TAIMR register (i = 0 to 4)

Note:

1. Set the TCDIV00 bit in the TCKDIVC0 register to select f1 or fOCO-F.

### 15.3.2 Timer Mode

In timer mode, the timer counts an internally generated count source. Table 15.6 lists Timer Mode Specifications, Table 15.7 lists Registers and the Setting in Timer Mode, and Figure 15.5 shows an Operation Example in Timer Mode.

**Table 15.6 Timer Mode Specifications**

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operation	<ul style="list-style-type: none"> <li>• Decrement</li> <li>• When the timer underflows, it reloads the reload register value and continues counting.</li> </ul>
Counter cycles	$\frac{(n + 1)}{fj}$ n: set value of TAI register, 0000h to FFFFh fj: frequency of count source
Count start condition	Set the TAI <sub>S</sub> bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAI <sub>S</sub> bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TAiIN pin function	I/O port or gate input
TAiOUT pin function	I/O port or pulse output
Read from timer	The count value can be read by reading the TAI register.
Write to timer	<ul style="list-style-type: none"> <li>• When not counting Value written to the TAI register is written to both the reload register and counter.</li> <li>• When counting Value written to the TAI register is only written to reload register (transferred to counter when reloaded next).</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>• Gate function Counting can be started and stopped by an input signal to the TAI<sub>IN</sub> pin.</li> <li>• Pulse output function Whenever the timer underflows, the output polarity of the TAI<sub>OUT</sub> pin is inverted. When the TAI<sub>S</sub> bit is set to 0 (stop counting), the pin outputs a low-level signal.</li> <li>• Output polarity control The output polarity of the TAI<sub>OUT</sub> pin is inverted. (While the TAI<sub>S</sub> bit is set to 0 (stop counting), a high-level signal is output.)</li> </ul>

i = 0 to 4

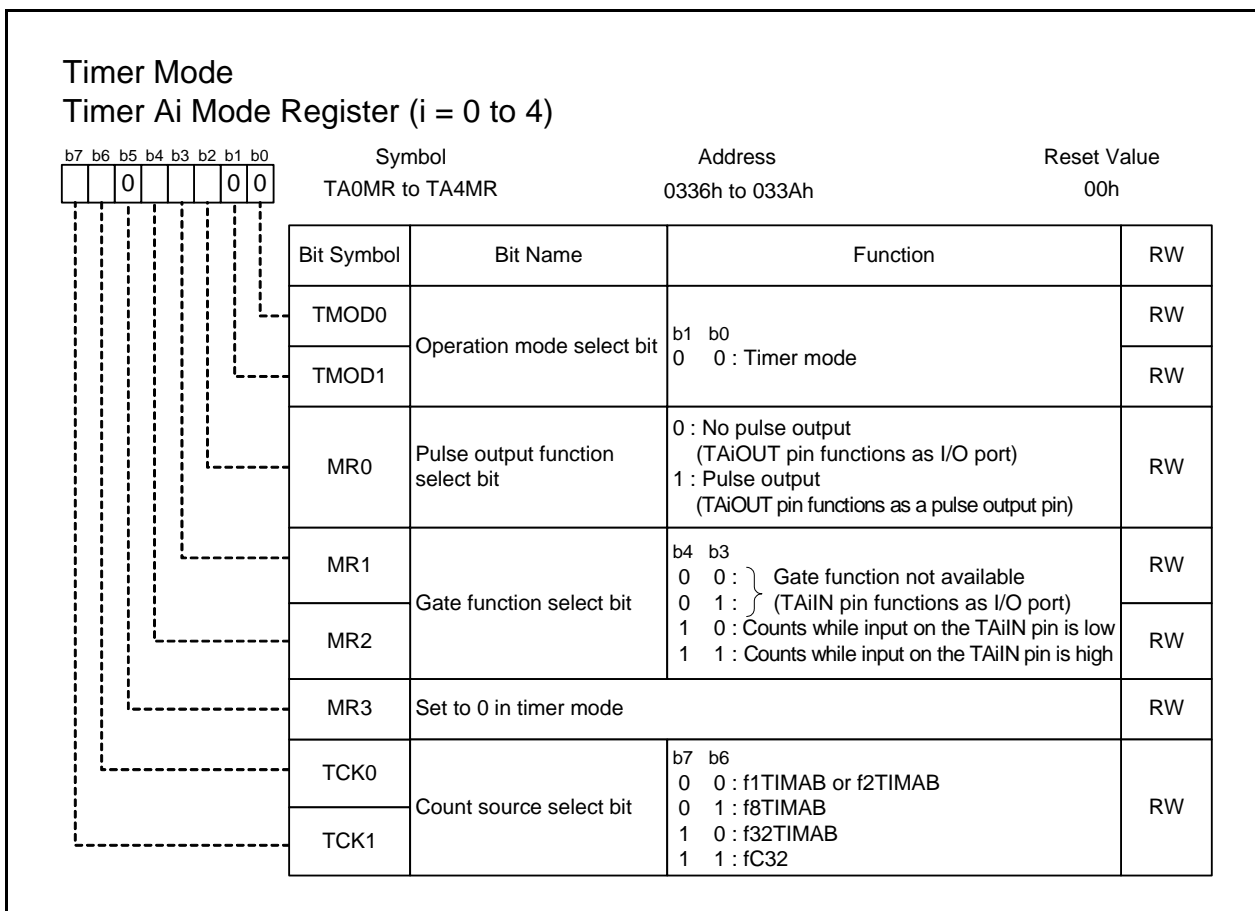
**Table 15.7 Registers and Settings in Timer Mode (1)**

Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select the clock used prior to timer AB frequency dividing.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAIiMR register is 1 (pulse output).
TAOW	TAiOW	Set to 0.
TAI1	15 to 0	- (does not need to be set)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Set to 00b.
TRGSR	TAiTGH to TAIiTGL	Set to 00b.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the TAIiMR register below

i = 0 to 4

Note:

1. This table does not describe a procedure.



**TCK1-TCK0 (Count source select bit) (b7-b6)**

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.

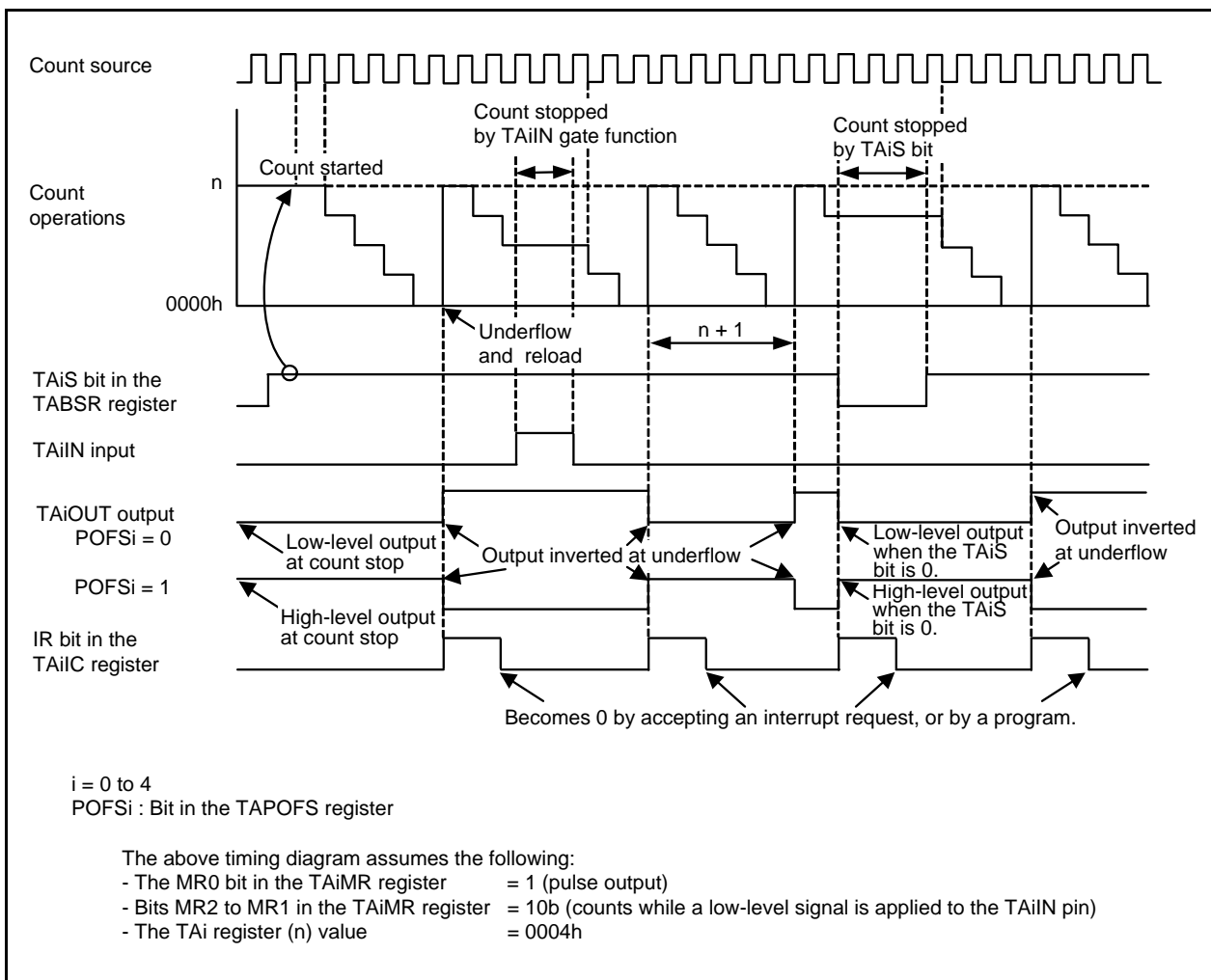


Figure 15.5 Operation Example in Timer Mode



### 15.3.3 Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing)

In event counter mode, the timer counts pulses from an external device, or overflows/underflows of other timers. Timers A2, A3, and A4 can count two-phase external signals. Refer to 15.3.4 “Event Counter Mode (When Processing Two-Phase Pulse Signal)” for details. Table 15.8 lists Event Counter Mode Specifications (When Not Using Two-Phase Pulse Signal Processing). Table 15.9 lists Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal). Figure 15.6 shows Operation Example in Event Counter Mode.

**Table 15.8 Event Counter Mode Specifications (When Not Using Two-Phase Pulse Signal Processing)**

Item	Specification
Count source	<ul style="list-style-type: none"> <li>External signals input to the TAIiN pin (active edge can be selected)</li> <li>Timer B2 overflows or underflows</li> <li>Timer Aj overflows or underflows (<math>j = i - 1</math>, except <math>j = 4</math> if <math>i = 0</math>)</li> <li>Timer Ak overflows or underflows (<math>k = i + 1</math>, except <math>k = 0</math> if <math>i = 4</math>)</li> </ul>
Count operations	<ul style="list-style-type: none"> <li>Increment or decrement can be selected by a program.</li> <li>When the timer overflows or underflows, it reloads the reload register value and continues counting. When selecting free-run type, the timer continues counting without reloading.</li> </ul>
Number of counts	When selecting reload type: <ul style="list-style-type: none"> <li>FFFFh - n + 1 for increment</li> <li>n + 1 for decrement</li> </ul> n: setting value of the TAI register, 0000h to FFFFh
Count start condition	Set the TAIiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAIiS bit to 0 (stop counting).
Interrupt request generation timing	Timer overflow or underflow
TAIiN pin function	I/O port or count source input
TAIiOUT pin function	I/O port or pulse output
Read from timer	Count value can be read by reading the TAI register.
Write to timer	<ul style="list-style-type: none"> <li>When not counting Value written to the TAI register is written to both the reload register and counter.</li> <li>When counting Value written to the TAI register is written to only reload register (transferred to counter when reloaded next).</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded.</li> <li>Pulse output function Whenever the timer underflows or underflows, the output polarity of the TAIiOUT pin is inverted. When the TAIiS bit is set to 0 (stop counting), the pin outputs a low-level signal.</li> <li>Output polarity control The output polarity of the TAIiOUT pin is inverted. (While the TAIiS bit is set to 0 (stop counting), a high-level signal is output.)</li> </ul>

i = 0 to 4

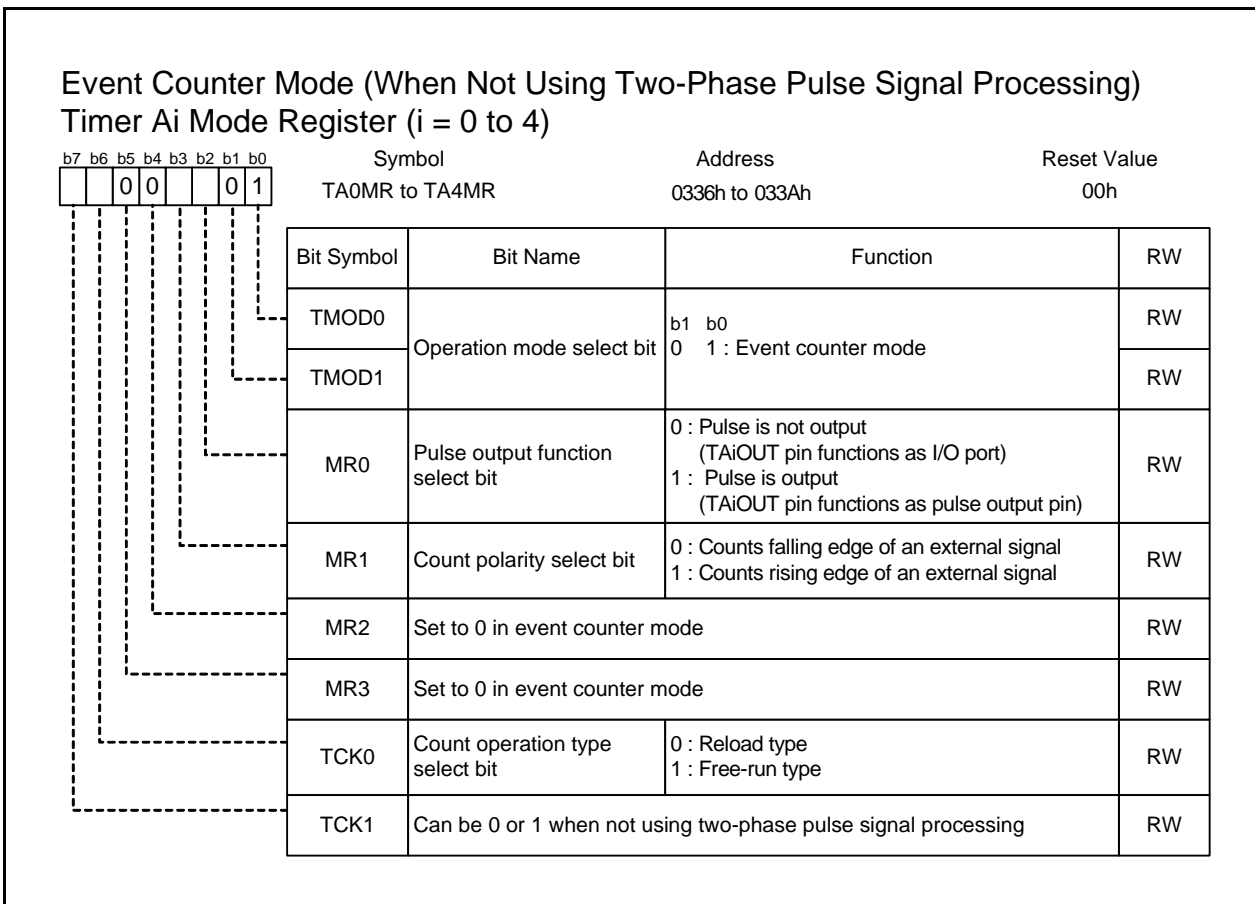
**Table 15.9 Registers and Settings in Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing) (1)**

Register	Bit	Function and Setting
PCLKR	PCLK0	- (setting unnecessary)
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	- (setting unnecessary)
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	- (setting unnecessary)
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAIiMR register is 1 (pulse output).
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Select a count source.
TRGSR	TAiTGH to TAIiTGL	Select a count source.
UDF	TAiUD	Select a count operation.
	TAiP	Set to 0.
TAi	15 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the TAIiMR register below.

i = 0 to 4

Note:

1. This table does not describe a procedure.



**MR1 (Count polarity select bit) (b3)**

This bit is enabled when bits TAI<sub>TGH</sub> to TAI<sub>TGL</sub> in the ONSF or TRGSR register are 00b (TAi<sub>IN</sub> pin input).

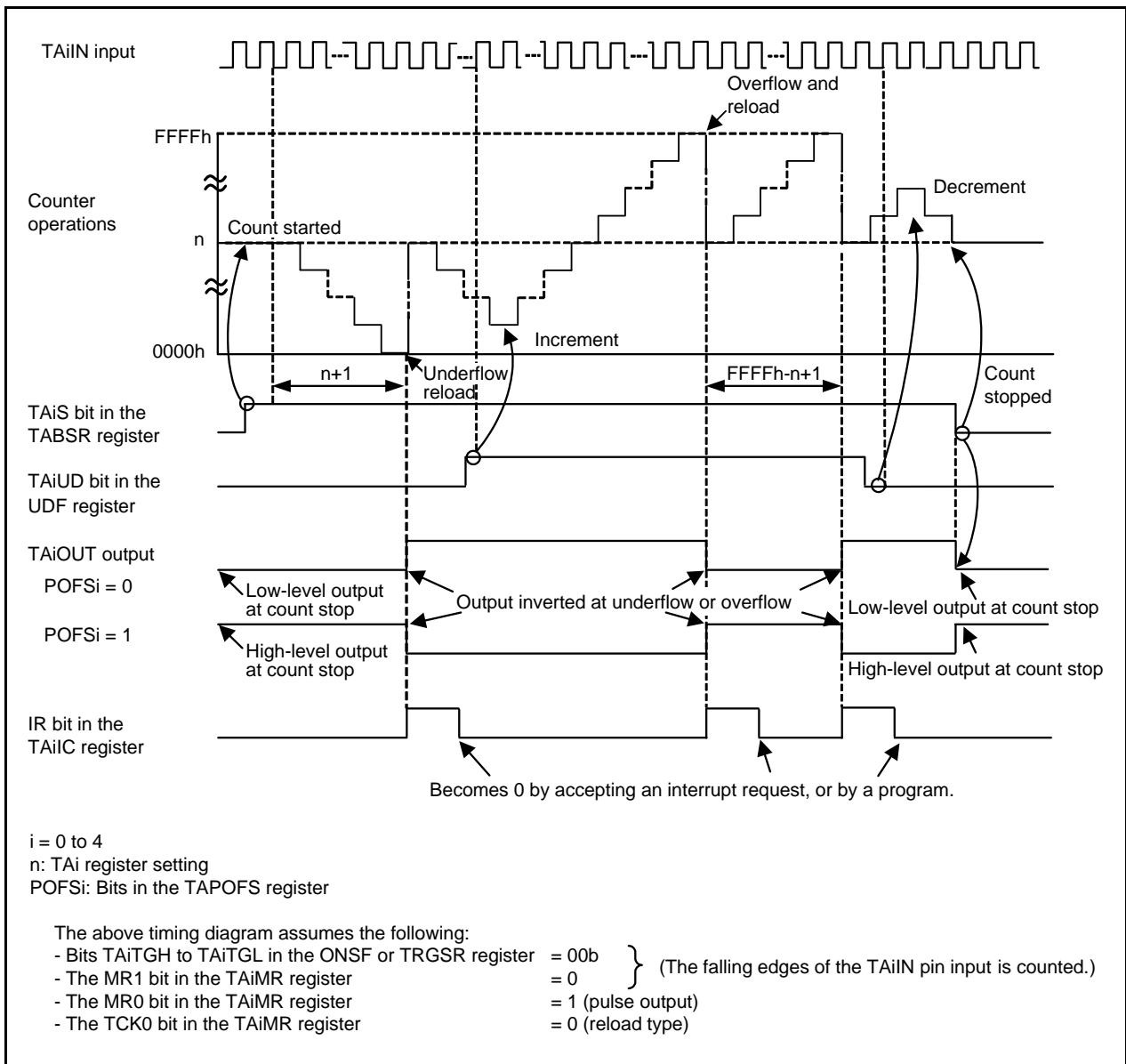


Figure 15.6 Operation Example in Event Counter Mode

### 15.3.4 Event Counter Mode (When Processing Two-Phase Pulse Signal)

Timers A2, A3, and A4 can be used to count two-phase pulse signals. Table 15.10 lists Event Counter Mode Specifications (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4). Table 15.11 lists Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal).

**Table 15.10 Event Counter Mode Specifications (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4)**

Item	Specification
Count source	Two-phase pulse signals input to the TAI <sub>i</sub> N or TAI <sub>i</sub> OUT pin
Count operations	<ul style="list-style-type: none"> <li>• Increment or decrement can be selected by a two-phase pulse signal.</li> <li>• When the timer overflows or underflows, it reloads the reload register value and continues counting. When selecting free-run type, the timer continues counting without reloading.</li> </ul>
Number of counts	When selecting reload type: <ul style="list-style-type: none"> <li>• FFFFh - n + 1 when incrementing</li> <li>• n + 1 when decrementing</li> </ul> n: setting value of the TAI register, 0000h to FFFFh
Count start condition	Set the TAI <sub>i</sub> S bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAI <sub>i</sub> S bit to 0 (stop counting).
Interrupt request generation timing	Timer overflow or underflow
TAI <sub>i</sub> N pin function	Two-phase pulse input
TAI <sub>i</sub> OUT pin function	Two-phase pulse input
Read from timer	Count value can be read by reading timer A2, A3, or A4 register.
Write to timer	<ul style="list-style-type: none"> <li>• When not counting Value written to the TAI register is written to both the reload register and counter.</li> <li>• When counting Value written to the TAI register is written to only reload register (transferred to counter when reloaded next).</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>• Select normal or multiply-by-4 processing operation (timer A3).</li> <li>• Counter initialization by Z-phase input (timer A3) The timer count value is initialized to 0 by Z-phase input.</li> </ul>

i = 2 to 4

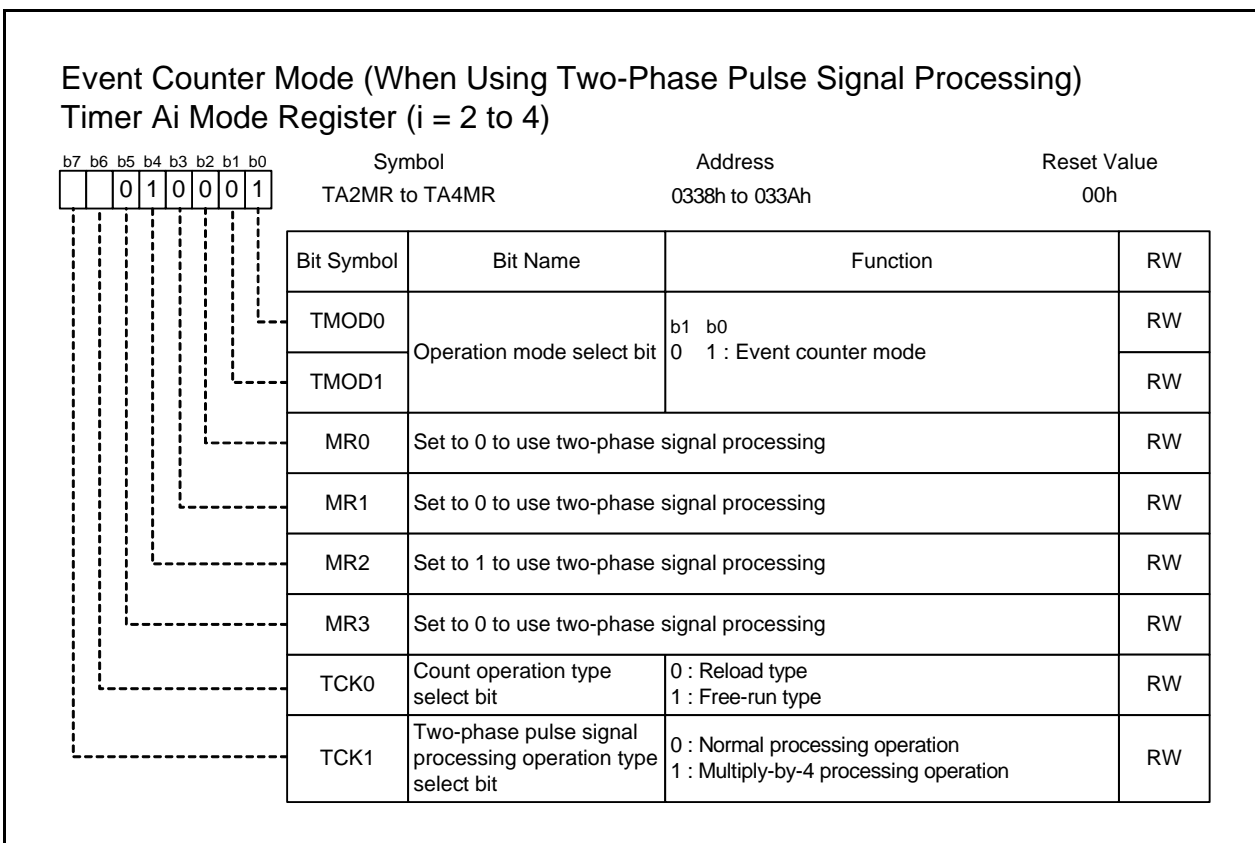
**Table 15.11 Registers and Settings in Event Counter Mode (When Processing Two-Phase Pulse Signal) (1)**

Register	Bit	Function and Setting
PCLKR	PCLK0	- (setting unnecessary)
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	- (setting unnecessary)
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	- (setting unnecessary)
TAPOFS	POFSi	Set to 0.
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 1 when using Z-phase input with timer A3.
	TA0TGH to TA0TGL	- (setting unnecessary)
TRGSR	TAiTGH to TAiTGL	Set to 00b.
UDF	TAiUD	Set to 0.
	TAiP	Set to 1.
TAi	15 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 2 to 4

Note:

1. This table does not describe a procedure.



**TCK1 (Two-phase pulse signal processing operation type select bit) (b7)**

The TCK1 bit can be set only for timer A3. No matter how this bit is set, timers A2 and A4 always operate in normal processing mode and multiply-by-4 processing mode, respectively.

### 15.3.4.1 Normal Processing

The timer increments at rising edges or decrements at falling edges on the TAJIN pin when input signals to the TAJOUT ( $j = 2, 3$ ) pin is high level.

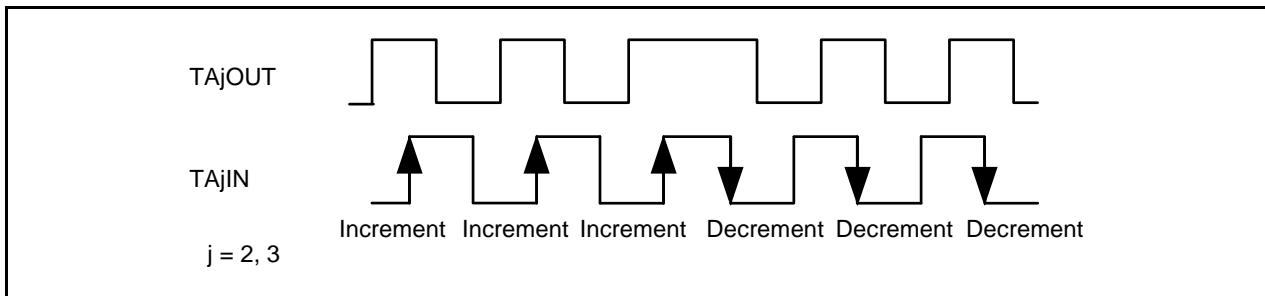


Figure 15.7 Normal Processing

### 15.3.4.2 Multiply-by-4 Processing

If the phase relationship is such that the input signal to the TAKIN pin goes high while the input signal to the TAKOUT pin ( $k = 3, 4$ ) is high, the timer increments at both rising and falling edges of the input signal to pins TAKOUT and TAKIN. If the phase relationship is such that the input signal to the TAKIN pin goes low while the input signal to the TAKOUT pin is high, the timer decrements at both rising and falling edges of the input signal to pins TAKOUT and TAKIN.

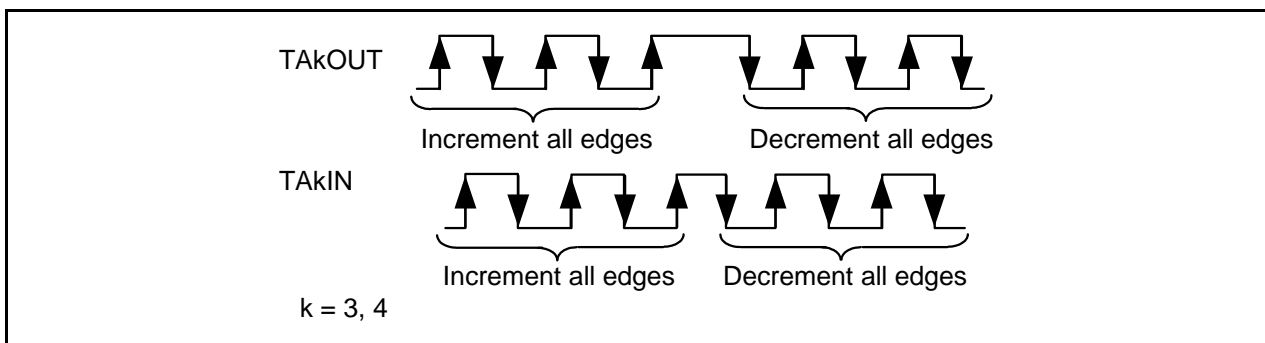


Figure 15.8 Multiply-by-4 Processing



### 15.3.4.3 Counter Initialization Using Two-Phase Pulse Signal Processing

This function initializes the timer count value to 0000h using Z-phase (counter initialization) input during two-phase pulse signal processing.

This function can only be used in timer A3 event counter mode during two-phase pulse signal processing, free-running type, multiply-by-4 processing, with Z-phase entered from the ZP pin.

Counter initialization by Z-phase input is enabled by writing 0000h to the TA3 register and setting the TAZIE bit in the ONSF register to 1 (Z-phase input enabled).

Counter initialization is accomplished by Z-phase input edge detection. The rising or falling edge can be selected as the active edge by setting the POL bit in the INT2IC register. The Z-phase pulse width must be equal to or greater than one clock cycle of the timer A3 count source.

The counter is initialized at the next count timing after accepting Z-phase input. Figure 15.9 shows the Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase.

When timer A3 overflow or underflow coincides with counter initialization by Z-phase input, a timer A3 interrupt request is generated twice in succession. Do not use the timer A3 interrupt when using this function.

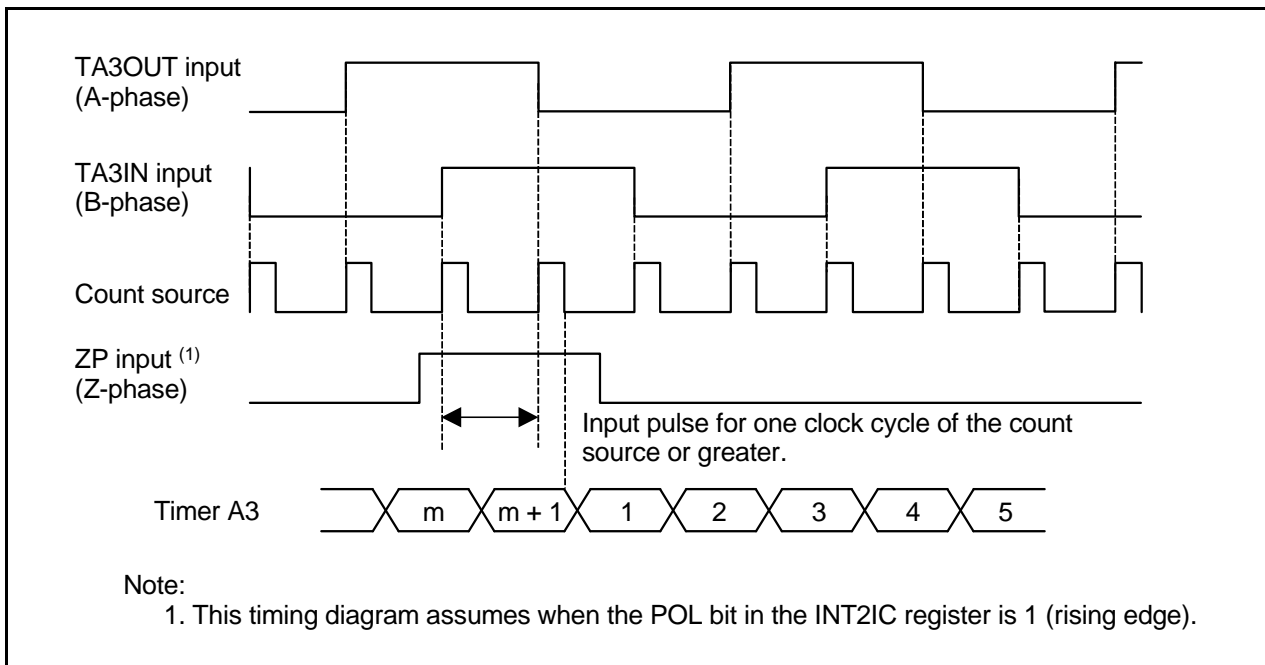



Figure 15.9 Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase

### 15.3.5 One-Shot Timer Mode

In one-shot timer mode, the timer is activated only once per trigger. When the trigger occurs, the timer starts and continues operating for a given period. Table 15.12 lists One-Shot Timer Mode Specifications. Table 15.13 lists Registers and the Setting in One-Shot Timer Mode. Figure 15.10 shows Operation Example in One-Shot Timer Mode.

**Table 15.12 One-Shot Timer Mode Specifications**

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	<ul style="list-style-type: none"> <li>Decrement</li> <li>When the timer counter reaches 0000h, it stops running after the reload register value is reloaded</li> <li>When a trigger occurs while counting, the reload register value is reloaded into the counter to continue counting</li> </ul>
Pulse width	$\frac{n}{f_j}$  <p>n: Set value of the TAI register, 0000h to FFFFh However, the counter does not run if 0000h is set.</p> <p>fj: Count source frequency</p>
Count start condition	<p>The TAI<sub>S</sub> bit in the TABSR register is 1 (start counting) and one of the following triggers occurs:</p> <ul style="list-style-type: none"> <li>External trigger input from the TAI<sub>IN</sub> pin</li> <li>Timer B2 overflow or underflow</li> <li>Timer A<sub>j</sub> overflow or underflow (j = i - 1, except j = 4 if i = 0)</li> <li>Timer A<sub>k</sub> overflow or underflow (k = i + 1, except k = 0 if i = 4)</li> <li>The TAI<sub>OS</sub> bit in the ONSF register is set to 1 (one-shot timer start).</li> </ul>
Count stop condition	<ul style="list-style-type: none"> <li>When the counter is reloaded after reaching 0000h</li> <li>The TAI<sub>S</sub> bit is set to 0 (stop counting)</li> </ul>
Interrupt request generation timing	When the counter reaches 0000h
TAI <sub>IN</sub> pin function	I/O port or trigger input
TAI <sub>OUT</sub> pin function	I/O port or pulse output
Read from timer	An undefined value is read when reading the TAI register.
Write to timer	<ul style="list-style-type: none"> <li>When not counting and until the first count source is input after counting starts, the value written to the TAI register is written to both the reload register and counter.</li> <li>When counting (after the first count source input), the value written to the TAI register is written to only the reload register (transferred to the counter when reloaded next time).</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>Pulse output function The timer outputs a low-level signal when not counting and a high-level signal when counting.</li> <li>Output polarity control The output polarity of the TAI<sub>OUT</sub> pin is inverted. (While the TAI<sub>S</sub> bit is set to 0 (stop counting), a high-level signal is output.)</li> </ul>

i = 0 to 4

**Table 15.13 Registers and Settings in One-Shot Timer Mode (1)**

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to dividing timer AB frequency.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAIiMR register is 1 (pulse output).
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 1 when starting counting while the MR2 bit is 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Select a count trigger.
TRGSR	TAiTGH to TAIiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Set a high-level pulse width. (2)
TAiMR	7 to 0	Refer to the TAIiMR register below.

i = 0 to 4

**Notes:**

1. This table does not describe a procedure.
2. This applies when the POFSi bit in the TAPOFS register is 0.

One-Shot Timer Mode Timer Ai Mode Register (i = 0 to 4)		Symbol TA0MR to TA4MR	Address 0336h to 033Ah	Reset Value 00h
Bit Symbol	Bit Name	Function	RW	
TMOD0	Operation mode select bit	b1 b0 1 0 : One-shot timer mode	RW	
TMOD1			RW	
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as an I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW	
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW	
MR2	Trigger select bit	0 : TAiOS bit enabled 1 : Selected by bits TAiTGH and TAiTGL	RW	
MR3	Set to 0 in one-shot timer mode		RW	
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW	
TCK1				

### MR1 (External trigger select bit) (b3)

This bit is enabled when the MR2 bit is 1 and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

### TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.

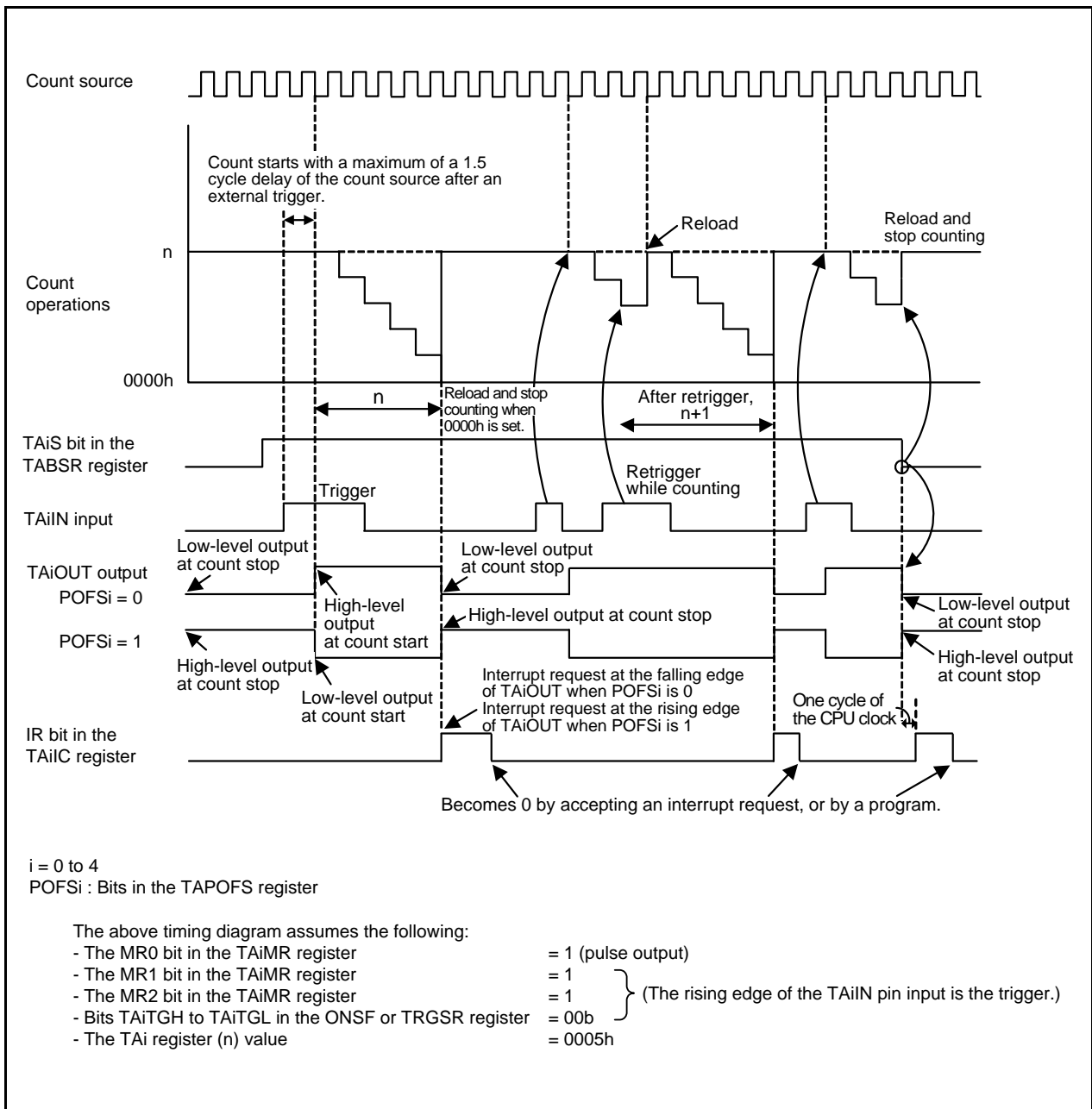
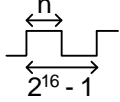
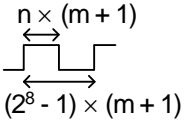


Figure 15.10 Operation Example in One-Shot Timer Mode

### 15.3.6 Pulse Width Modulation (PWM) Mode

In PWM mode, the timer outputs pulses of a given width in succession. The counter functions as either a 16-bit pulse width modulator or 8-bit pulse width modulator. Table 15.14 lists PWM Mode Specifications. Table 15.15 lists Registers and the Setting in PWM Mode. Figure 15.11 and Figure 15.12 show Operation Example in 16-Bit Pulse Width Modulation Mode and Operation Example in 8-Bit Pulse Width Modulation Mode, respectively.

**Table 15.14 PWM Mode Specifications**

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	<ul style="list-style-type: none"> <li>Decrement (operating as an 8-bit or a 16-bit pulse width modulator)</li> <li>The timer reloads the reload register value at a rising edge of PWM pulse and continues counting.</li> <li>The timer is not affected by a trigger that occurs during counting.</li> </ul>
16-bit PWM	<ul style="list-style-type: none"> <li>Pulse width <math>\frac{n}{f_j}</math></li> <li>Cycle time <math>\frac{(2^{16}-1)}{f_j}</math></li> </ul> <p>n: set value of the TAI register fj: count source frequency</p> 
8-bit PWM	<ul style="list-style-type: none"> <li>Pulse width <math>\frac{n \times (m+1)}{f_j}</math></li> <li>Cycle time <math>\frac{(2^8-1) \times (m+1)}{f_j}</math></li> </ul> <p>m: set value of the TAI register lower address n: set value of the TAI register upper address fj: count source frequency</p> 
Count start condition	<ul style="list-style-type: none"> <li>The TAI<sub>S</sub> bit of the TABSR register is set to 1 (start counting).</li> <li>The TAI<sub>S</sub> bit is 1 and external trigger input from the TAI<sub>IN</sub> pin</li> <li>The TAI<sub>S</sub> bit is 1 and one of the following triggers occurs <ul style="list-style-type: none"> <li>Timer B2 overflow or underflow</li> <li>Timer A<sub>j</sub> overflow or underflow (j = i - 1, except j = 4 if i = 0)</li> <li>Timer A<sub>k</sub> overflow or underflow (k = i + 1, except k = 0 if i = 4)</li> </ul> </li> </ul>
Count stop condition	The TAI <sub>S</sub> bit is set to 0 (stop counting).
Interrupt request generation timing	On the falling edge of the PWM pulse
TAI <sub>IN</sub> pin function	I/O port or trigger input
TAI <sub>OUT</sub> pin function	Pulse output
Read from timer	An undefined value is read when reading the TAI register.
Write to timer	<ul style="list-style-type: none"> <li>When not counting Value written to the TAI register is written to both the reload register and counter.</li> <li>When counting Value written to the TAI register is written to only the reload register (transferred to counter when reloaded next time).</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>Output polarity control The output polarity of the TAI<sub>OUT</sub> pin is inverted. (While the TAI<sub>S</sub> bit is set to 0 (stop counting), a high-level signal is output).</li> </ul>

i = 0 to 4

**Table 15.15 Registers and Settings in PWM Mode (1)**

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select the clock used prior to dividing timer AB frequency.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity.
TAOW	TAiOW	Set to 0.
TAi1	15 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0GL	Select a count trigger.
TRGSR	TAiTGH to TAI TGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Select the PWM pulse width and cycles.
TAiMR	7 to 0	Refer to the TAI MR register below.

i = 0 to 4

Note:

1. This table does not describe a procedure.

Pulse Width Modulation (PWM) Mode Timer Ai Mode Register (i = 0 to 4)										
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value
						1	1	TA0MR to TA4MR	0336h to 033Ah	00h
Bit Symbol	Bit Name		Function				RW			
TMOD0	Operation mode select bit		b1 b0 1 1 : PWM mode or programmable output mode				RW			
							RW			
MR0	Pulse output function select bit		0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)				RW			
MR1	External trigger select bit		0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin				RW			
MR2	Trigger select bit		0 : Write 1 to the TAiS bit in the TABSR register 1 : Selected by bits TAiTGH to TAiTGL				RW			
MR3	16-/8-bit PWM mode select bit		0 : 16-bit PWM mode 1 : 8-bit PWM mode				RW			
TCK0	Count source select bit		b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32				RW			
TCK1										

### MR1 (External trigger select bit) (b3)

This bit is enabled when the MR2 bit is 1, and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

### TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.



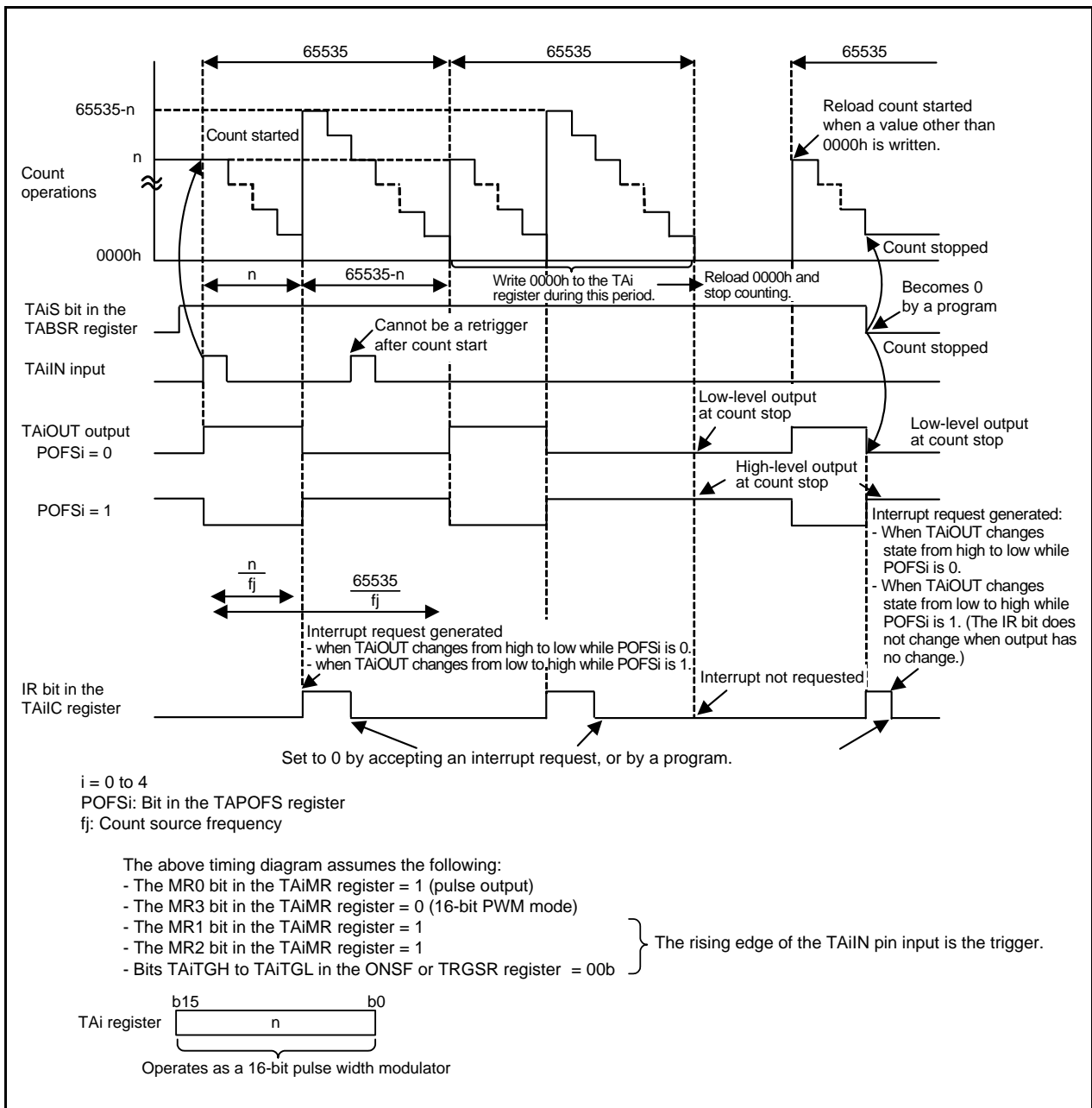


Figure 15.11 Operation Example in 16-Bit Pulse Width Modulation Mode

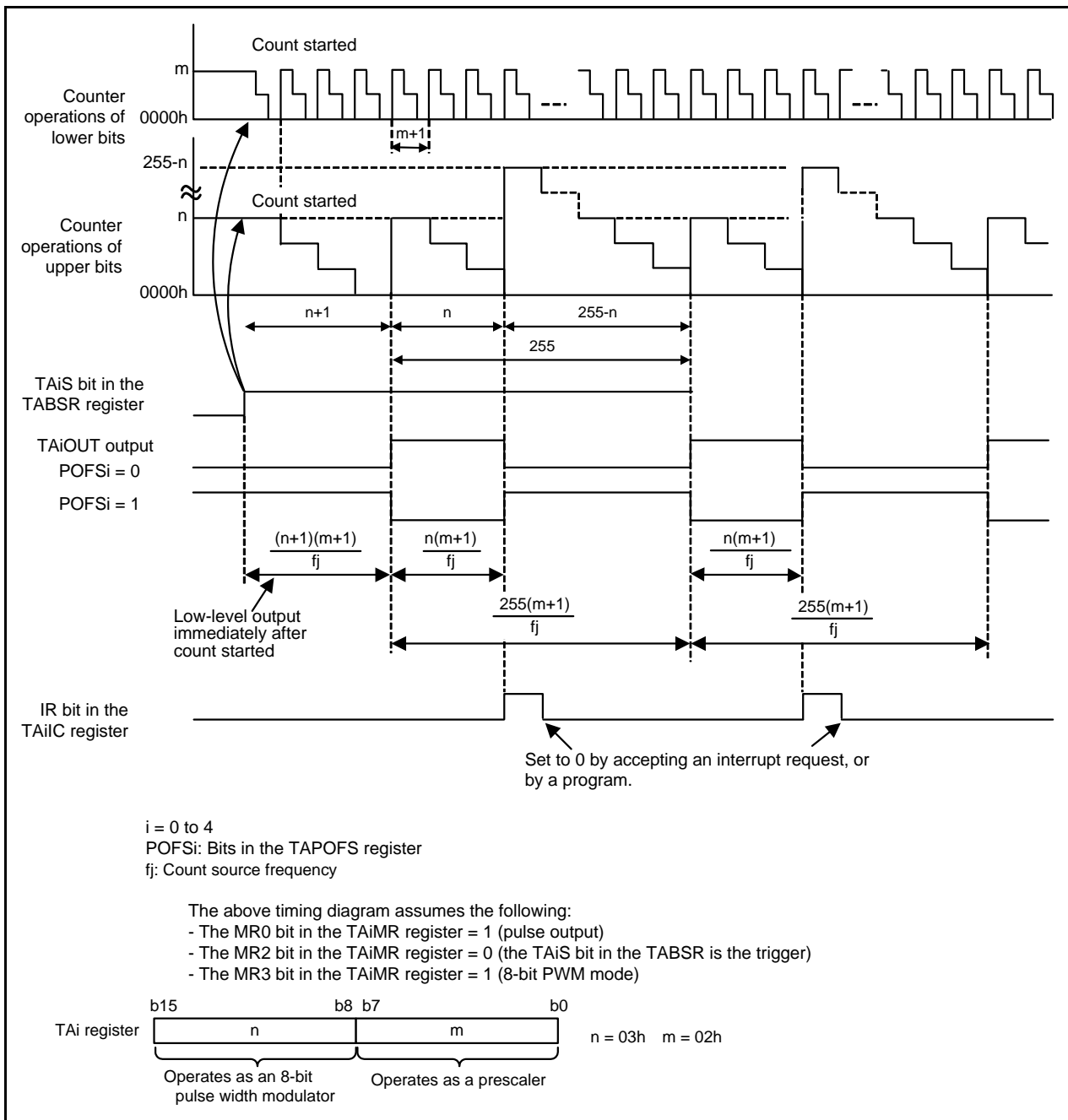
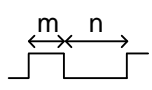


Figure 15.12 Operation Example in 8-Bit Pulse Width Modulation Mode

### 15.3.7 Programmable Output Mode (Timers A1, A2, and A4)

In programmable output mode, the timer outputs low- and high-levels of pulse width successively. Table 15.16 lists Programmable Output Mode Specifications. Table 15.17 lists Registers and the Setting in Programmable Output Mode. Figure 15.13 shows Operation Example in Programmable Output Mode.

**Table 15.16 Programmable Output Mode Specifications**

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	<ul style="list-style-type: none"> <li>• Decrement</li> <li>• The timer reloads the reload register value at the rising edge of pulse and continues counting</li> <li>• When a trigger occurs while counting, the timer is not affected.</li> </ul>
Pulse width	<ul style="list-style-type: none"> <li>• High-level pulse width <math>\frac{m}{f_j}</math></li> <li>• Low-level pulse width <math>\frac{n}{f_j}</math></li> </ul>  <p>m: set value of the TAI register n: set value of the TAI1 register fj: count source frequency</p>
Count start conditions	<ul style="list-style-type: none"> <li>• The TAI S bit of the TABSR register is set to 1 (start counting).</li> <li>• The TAI S bit is 1 and external trigger input from the TAI IN pin</li> <li>• The TAI S bit is 1 and one of the following external triggers occurs: Timer B2 overflow or underflow Timer Aj overflow or underflow (j = i - 1) Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4)</li> </ul>
Count stop condition	The TAI S bit is set to 0 (stop counting).
Interrupt request generation timing	At the rising edge of pulse
TAI IN pin function	I/O port or trigger input
TAI OUT pin function	Pulse output
Read from timer	An undefined value is read when reading registers TAI and TAI1.
Write to timer	<ul style="list-style-type: none"> <li>• When writing to registers TAI and TAI1 while not counting, the value is written to both reload register and counter.</li> <li>• When writing to registers TAI and TAI1 while counting, the value is written to the reload register. (transferred to the counter when reloaded next time).</li> </ul>
Selectable functions	Output polarity control The output polarity of the TAI OUT pin is inverted. (While the TAI S bit is set to 0 (stop counting), a high-level signal is output.)

i = 1, 2, and 4

**Table 15.17 Registers and Settings in Programmable Output Mode (1)**

Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to dividing timer AB frequency.
PWMFS	PWMFSi	Set to 1.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity.
TAOW	TAiOW	Set to 0 to disable output waveform change, and set to 1 to enable output waveform change.
TAi1	15 to 0	Set a low-level pulse width. (2)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TA0TGH to TA0TGL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	15 to 0	Set a high-level pulse width. (2)
TAiMR	7 to 0	Refer to the TAiMR register below.

i = 1, 2, and 4

Notes:

1. This table does not describe a procedure.
2. This applies when the POFSi bit in the TAPOFS register is 0.

Programmable Output Mode Timer Ai Mode Register (i = 1, 2, 4)		Symbol	Address	Reset Value
		TA0MR to TA4MR	0336h to 033Ah	00h
Bit Symbol	Bit Name	Function	RW	
TMOD0	Operation mode select bit	b1 b0 1 1 : PWM mode or programmable output mode	RW	
TMOD1			RW	
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as an I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW	
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW	
MR2	Trigger select bit	0 : Write 1 to the TAiS bit in the TABSR register 1 : Selected by bits TAiTGH to TAiTGL	RW	
MR3	Set to 0 in programmable output mode		RW	
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW	
TCK1				

### MR1 (External trigger select bit) (b3)

This bit is enabled when the MR2 bit is 1, and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

### TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.

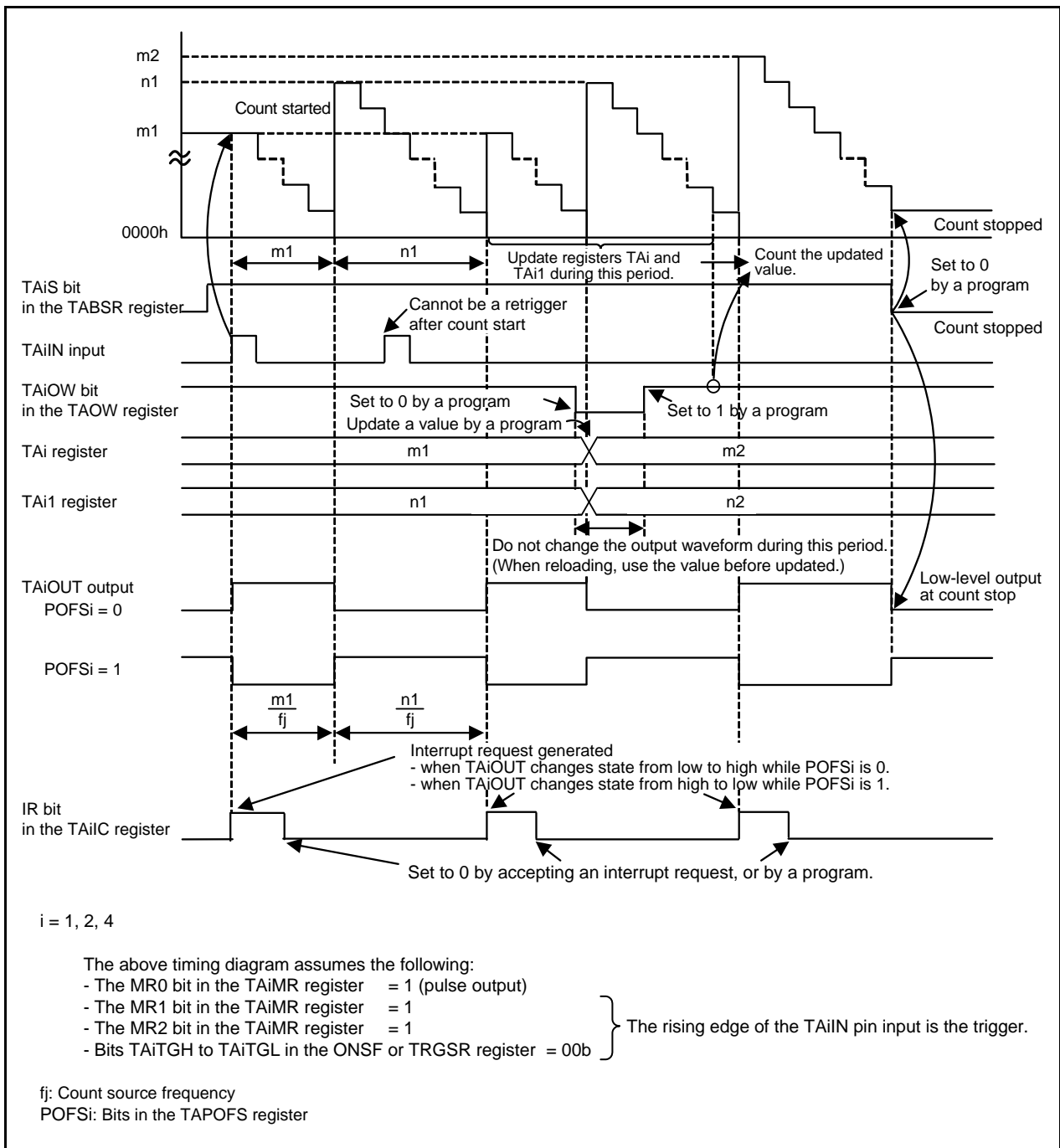


Figure 15.13 Operation Example in Programmable Output Mode

## 15.4 Interrupts

Refer to individual operation examples for interrupt request generating timing.

Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 15.18 lists Timer A Interrupt Related Registers.

**Table 15.18 Timer A Interrupt Related Registers**

Address	Register	Symbol	Reset Value
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b

The IR bit in the TAIIC register may become 1 (interrupt requested) when the TMOD1 bit in the TAIMR register is changed from 0 to 1 (change from timer mode or event counter mode to one-shot timer mode, PWM mode, or programmable output mode). Make sure to follow the procedure below when setting the TMOD1 bit to 1. Refer to 12.13 “Notes on Interrupts” for details.

- (1) Set bits ILVL2 to ILVL0 in the TAIIC register to 000b (interrupt disabled).
- (2) Set the TAIMR register.
- (3) Set the IR bit in the TAIIC register to 0 (interrupt not requested).

## 15.5 Notes on Timer A

### 15.5.1 Common Notes on Multiple Modes

#### 15.5.1.1 Register Setting

The timer stops after reset. Set the mode, count source, counter value, etc., using registers TAI<sub>MR</sub>, TAI<sub>i</sub>, TAI<sub>1</sub>, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, and TA0TGH in the ONSF register before setting the TAI<sub>S</sub> bit in the TABSR register to 1 (count started) (i = 0 to 4).

Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Always make sure registers TAI<sub>MR</sub>, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, TA0TGH in the ONSF register are modified while the TAI<sub>S</sub> bit is 0 (count stopped), regardless of whether after reset or not.

#### 15.5.1.2 Event or Trigger

When bits TAI<sub>TGH</sub> to TAI<sub>TGL</sub> in the registers ONSF or TRGSR are 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

For some modes of the timers selected using bits TAI<sub>TGH</sub> to TAI<sub>TGL</sub>, an interrupt request is generated by a source other than overflow or underflow.

For example, when using pulse-period measurement mode or pulse-width measurement mode in timer B2, an interrupt request is generated at an active edge of the measurement pulse. For details, refer to the "Interrupt request generation timing" in each mode's specification table.

#### 15.5.1.3 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/CTS2/RTS2/TA1IN/V/TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/W, P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/U/TSUDB



## 15.5.2 Timer A (Timer Mode)

### 15.5.2.1 Reading the Timer

The counter value can be read from the TAI register at any time while counting. However, if the counter is read at the same time as it is reloaded, the read value is FFFFh. Also, if the counter is read before it starts counting, or after a value is set in the TAI register while not counting, the set value is read.

## 15.5.3 Timer A (Event Counter Mode)

### 15.5.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TAI register. However, while reloading, FFFFh can be read in underflow, and 0000h in overflow. When the counter is read before it starts counting and after a value is set in the TAI register while not counting, the set value is read.

## 15.5.4 Timer A (One-Shot Timer Mode)

### 15.5.4.1 Stop While Counting

When setting the TAI<sub>S</sub> bit to 0 (count stopped), the following occurs:

- The counter stops counting and reload register values are reloaded.
- The TAI<sub>OUT</sub> pin outputs a low-level signal when the POFS<sub>i</sub> bit in the TAPOFS register is 0, and outputs a high-level signal when it is 1.
- After one cycle of the CPU clock, the IR bit in the TAI<sub>IC</sub> register becomes 1 (interrupt requested).

### 15.5.4.2 Delay between the Trigger Input and Timer Output

As the one-shot timer output is synchronized with an internally generated count source, when an external trigger is selected, a maximum 1.5 cycle delay of the count source occurs between the trigger input to the TAI<sub>IN</sub> pin and timer output.

### 15.5.4.3 Changing Operating Modes

The IR bit becomes 1 when the timer operating mode is set by any of the following:

- Selecting one-shot timer mode after reset
- Changing the operating mode from timer mode to one-shot timer mode
- Changing the operating mode from event counter mode to one-shot timer mode

To use the timer A<sub>i</sub> interrupt (IR bit), set the IR bit to 0 after the changes listed above are made.

### 15.5.4.4 Retrigger

When a trigger occurs while counting, the counter reloads the reload register to continue counting after generating a retrigger and decrementing once. To generate a trigger while counting, generate a retrigger after at least one cycle of the timer count source has elapsed following the previous trigger. When an external trigger is generated, do not generate a retrigger for 300 ns before the count value becomes 0000h. The one-shot timer may stop counting.

## 15.5.5 Timer A (Pulse Width Modulation Mode)

### 15.5.5.1 Changing Operating Modes

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

### 15.5.5.2 Stop While Counting

When setting the TAI<sub>S</sub> bit to 0 (count stopped) during PWM pulse output, the following occur:

When the POFS<sub>i</sub> bit in the TAPOFS register is 0:

- Counting stops
- When the TAI<sub>OUT</sub> pin is high, the output level goes low and the IR bit becomes 1.
- When the TAI<sub>OUT</sub> pin is low, both the output level and the IR bit remain unchanged.

When the POFS<sub>i</sub> bit in the TAPOFS register is 1:

- Counting stops.
- When the TAI<sub>OUT</sub> pin output is low, the output level goes high and the IR bit is set to 1.
- When the TAI<sub>OUT</sub> pin output is high, both the output level and the IR bit remain unchanged.

## 15.5.6 Timer A (Programmable Output Mode)

### 15.5.6.1 Changing the Operating Mode

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

### 15.5.6.2 Stop While Counting

When setting the TAI<sub>S</sub> bit to 0 (count stopped) during pulse output, the following occur:

When the POFS<sub>i</sub> bit in the TAPOFS register is 0:

- Counting stops.
- When the TAI<sub>OUT</sub> pin is high, the output level goes low.
- When the TAI<sub>OUT</sub> pin is low, the output level remains unchanged.
- The IR bit remains unchanged.

When the POFS<sub>i</sub> bit in the TAPOFS register is 1:

- Counting stops
- When the TAI<sub>OUT</sub> pin output is low, the output level goes high.
- When the TAI<sub>OUT</sub> pin output is high, the output level remains unchanged.
- The IR bit remains unchanged.

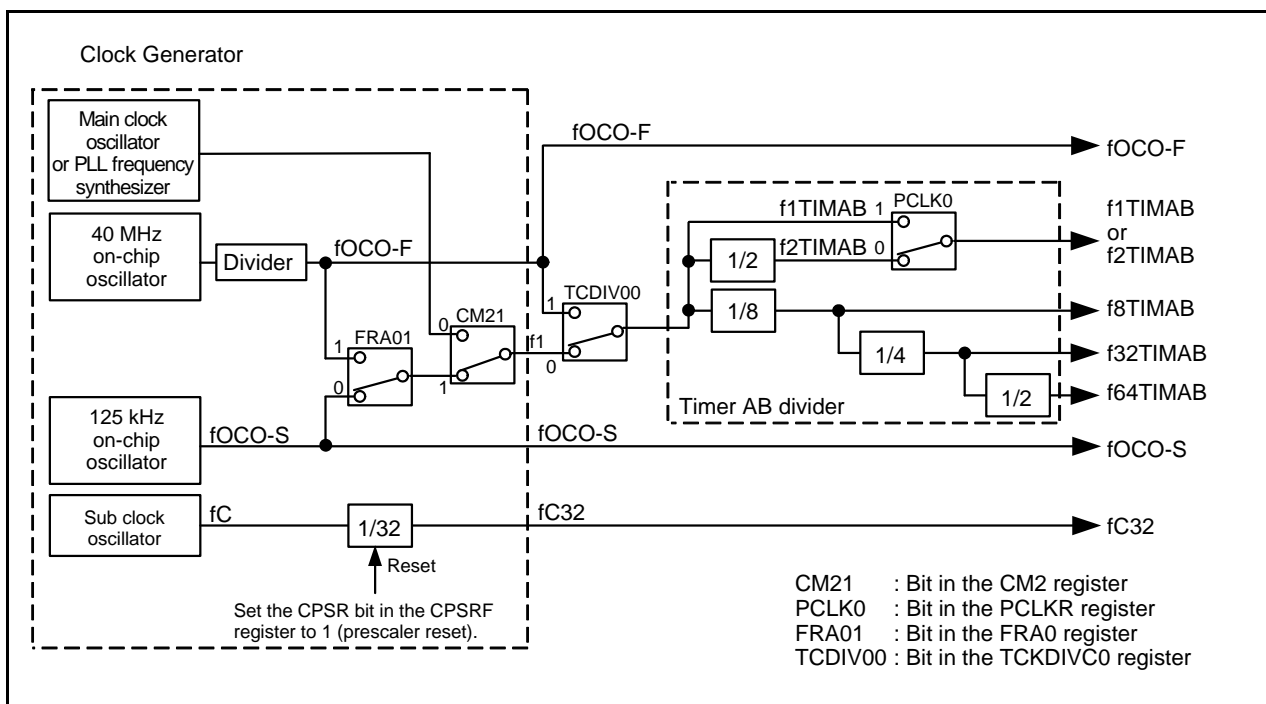
## 16. Timer B

### 16.1 Introduction

Timer B consists of timers B0 to B2. Each timer operates independently of the others. Table 16.1 lists Timer B Specifications, Figure 16.1 shows Timer A and B Count Sources, Figure 16.2 shows the Timer B Configuration, Figure 16.3 shows the Timer B Block Diagram, and Table 16.2 lists the I/O Ports.

**Table 16.1 Timer B Specifications**

Item	Specification
Configuration	16-bit timer × 3
Operating modes	<ul style="list-style-type: none"> <li>• Timer mode The timer counts an internal count source.</li> <li>• Event counter mode The timer counts pulses from an external device, or overflows and underflows of other timers.</li> <li>• Pulse period/pulse width measurement modes The timer measures pulse periods or pulse widths of an external signal.</li> </ul>
Interrupt source	Overflow/underflow/active edge of measurement pulse × 3



**Figure 16.1 Timer A and B Count Sources**

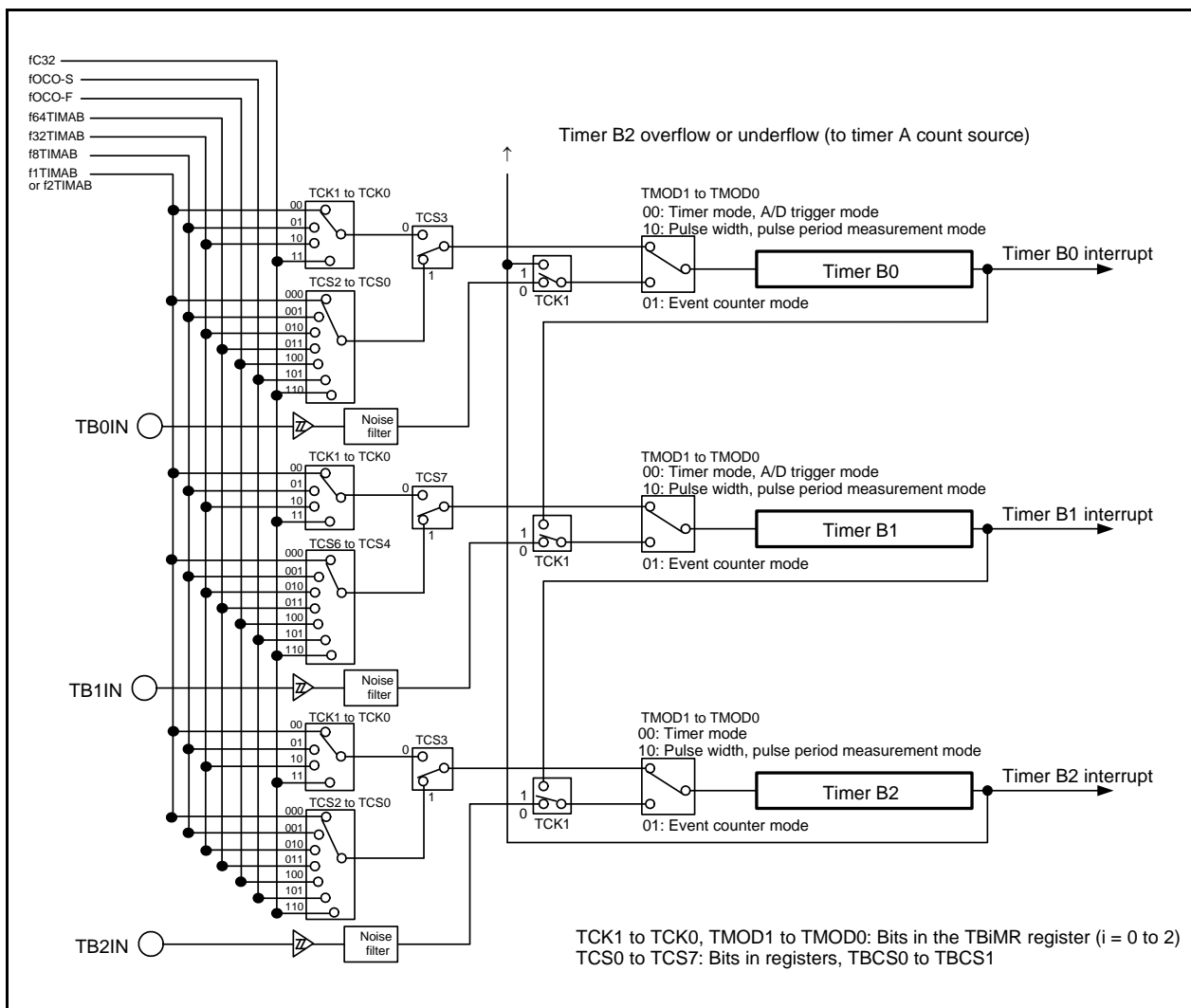


Figure 16.2 Timer B Configuration

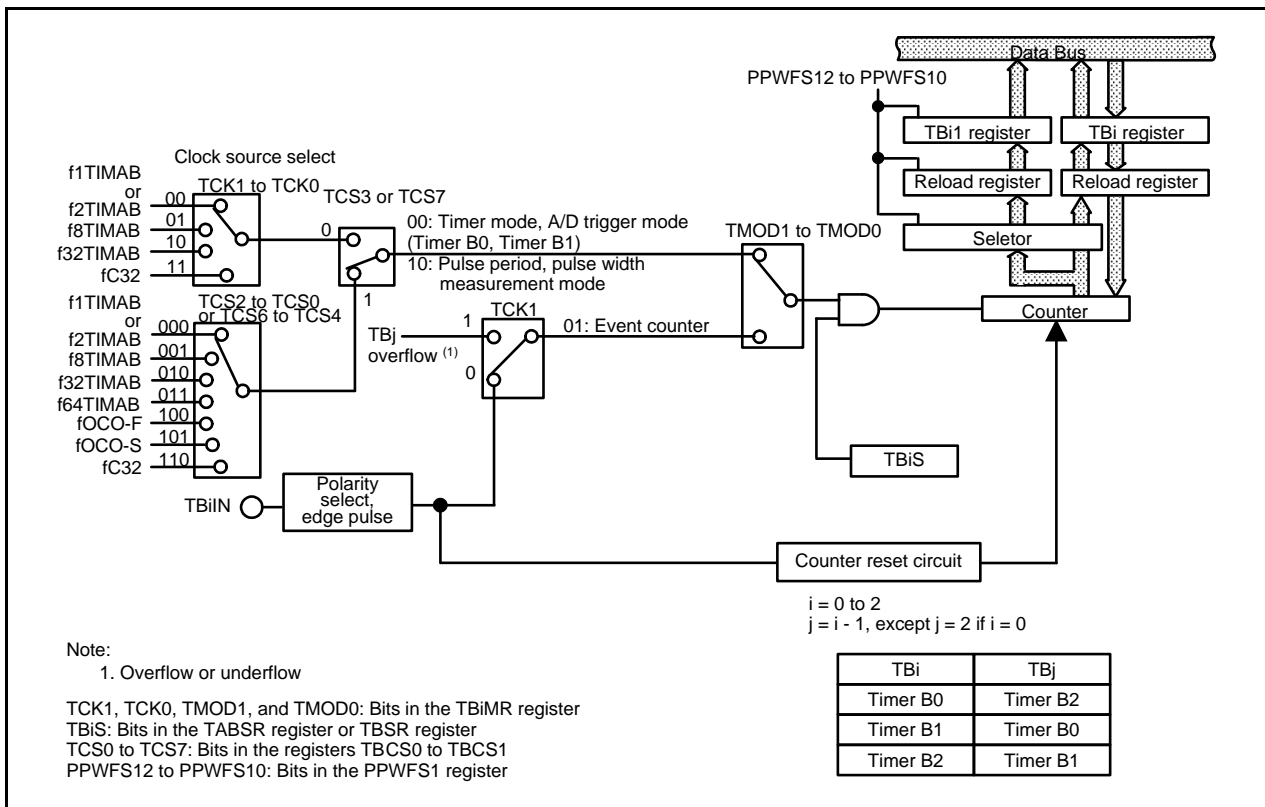


Figure 16.3 Timer B Block Diagram

Table 16.2 I/O Ports

Pin Name	I/O	Function
TBiIN	Input (1)	Count source input (event counter mode) Measurement pulse input (pulse period measurement mode, pulse width measurement mode)

$i = 0 \text{ to } 2$

Note:

- When using the TBiIN pin for input, set the port direction bit sharing the same pin to 0 (input mode).

## 16.2 Registers

Table 16.3 lists registers associated with timer B.

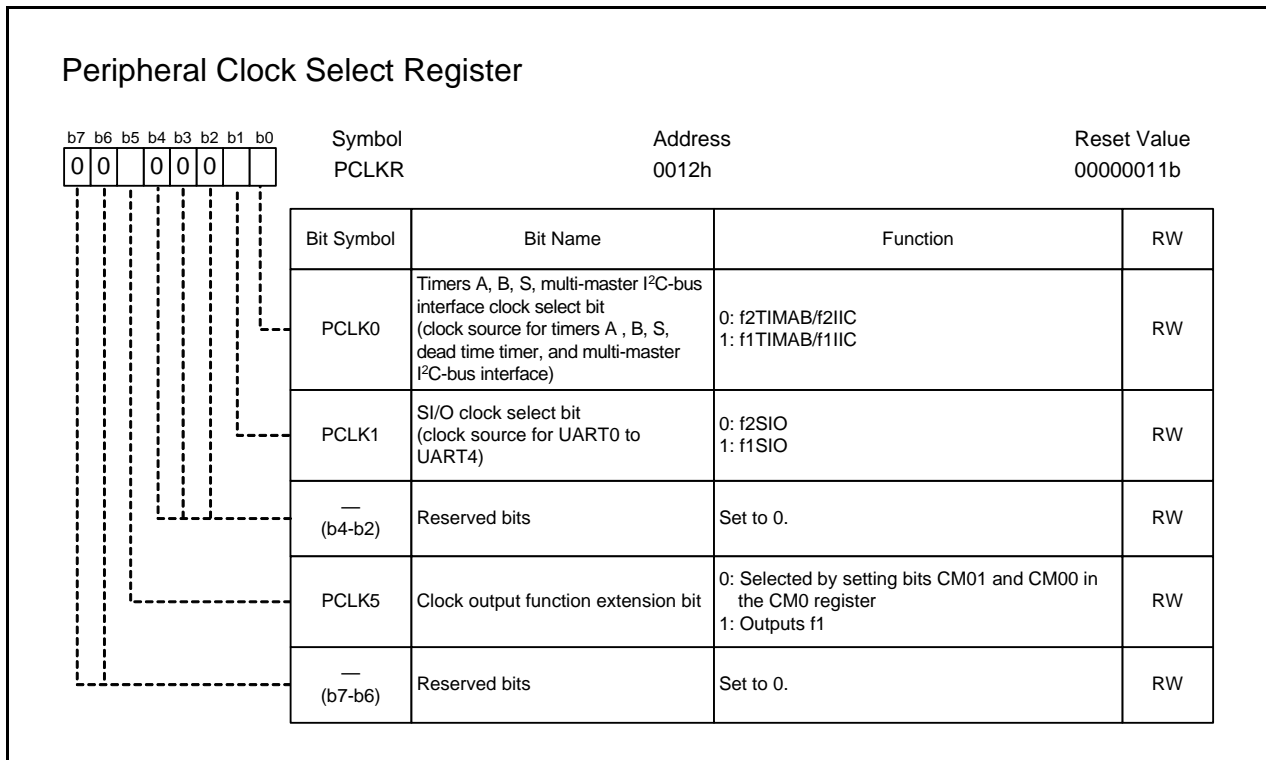
Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer B. After changing the TCDIV00 bit, set other registers associated with timer B again.

Refer to “registers and the setting” in each mode for registers and bit settings.

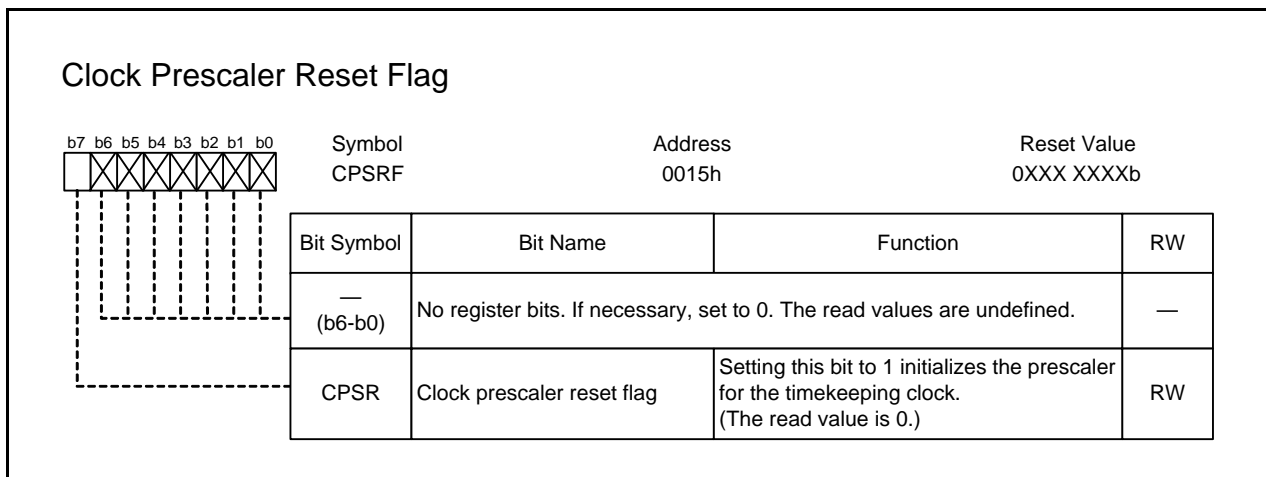
**Table 16.3 Registers**

Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
0320h	Count Start Flag	TABSR	00h
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b

### 16.2.1 Peripheral Clock Select Register (PCLKR)

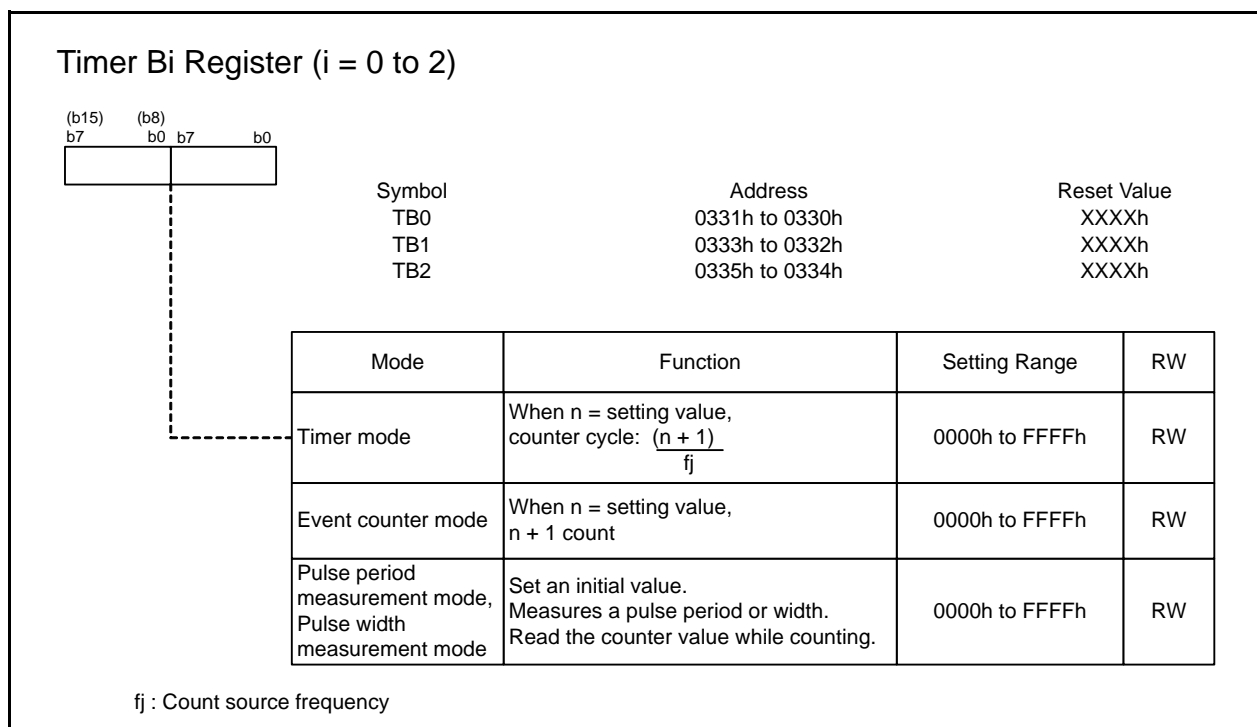


### 16.2.2 Clock Prescaler Reset Flag (CPSRF)





### 16.2.3 Timer Bi Register (TBi) (i = 0 to 2)



Access this register in 16-bit units.

#### Event Counter Mode

The timer counts pulses from an external device, or overflows or underflows of other timers.

#### Pulse Period Measurement Mode, Pulse Width Measurement Mode

Set these modes when the TBiS bit in the TABSR is 0 (count stopped).

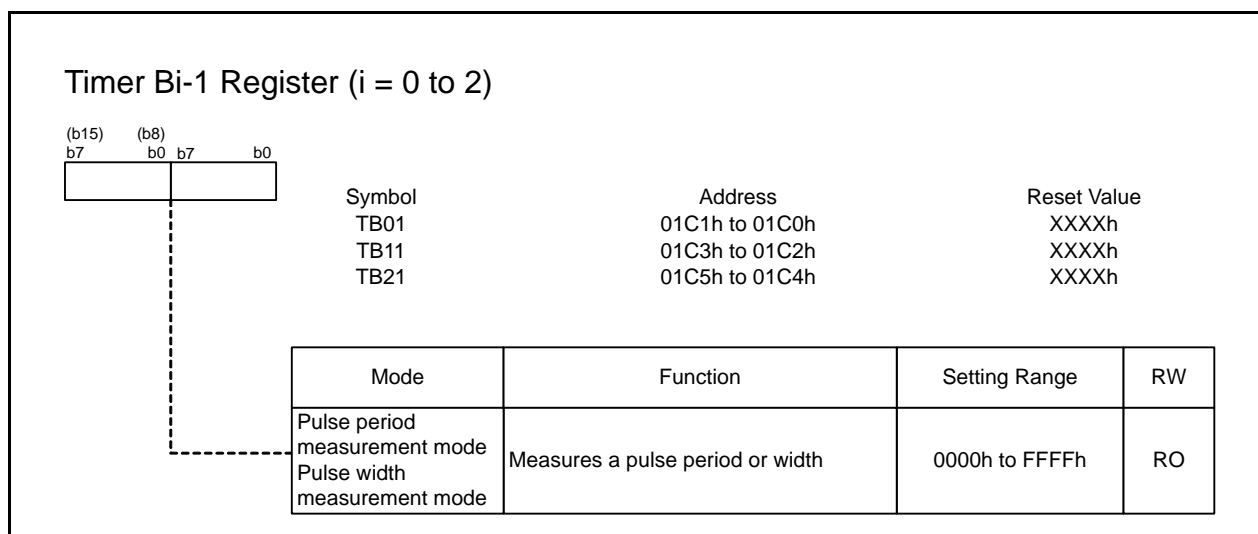
These modes become read only (RO) when the TBiS bit in the TABSR is 1 (count started).

The counter starts counting the count source at an active edge of the measurement pulse, transfers the count value to a register at the next active edge, and continues counting.

The measurement result can be read by reading the TBi register when bits PPWFS12 to PPWFS10 in the PPWFS1 register are 0.

While counting, the counter value can be read by reading the TBi register when bits PPWFS12 to PPWFS10 are 1.

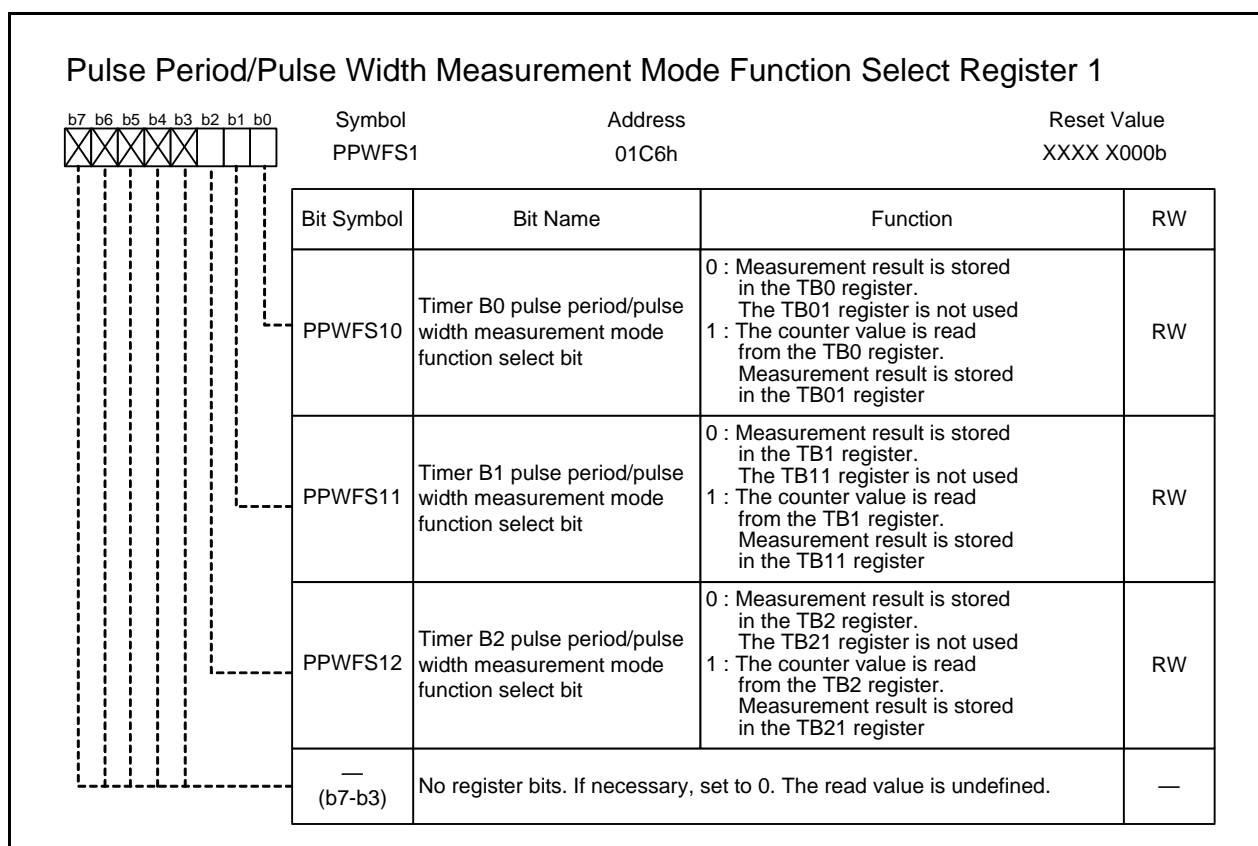
### 16.2.4 Timer Bi-1 Register (TBi1) (i = 0 to 2)



Access this register in 16-bit units.

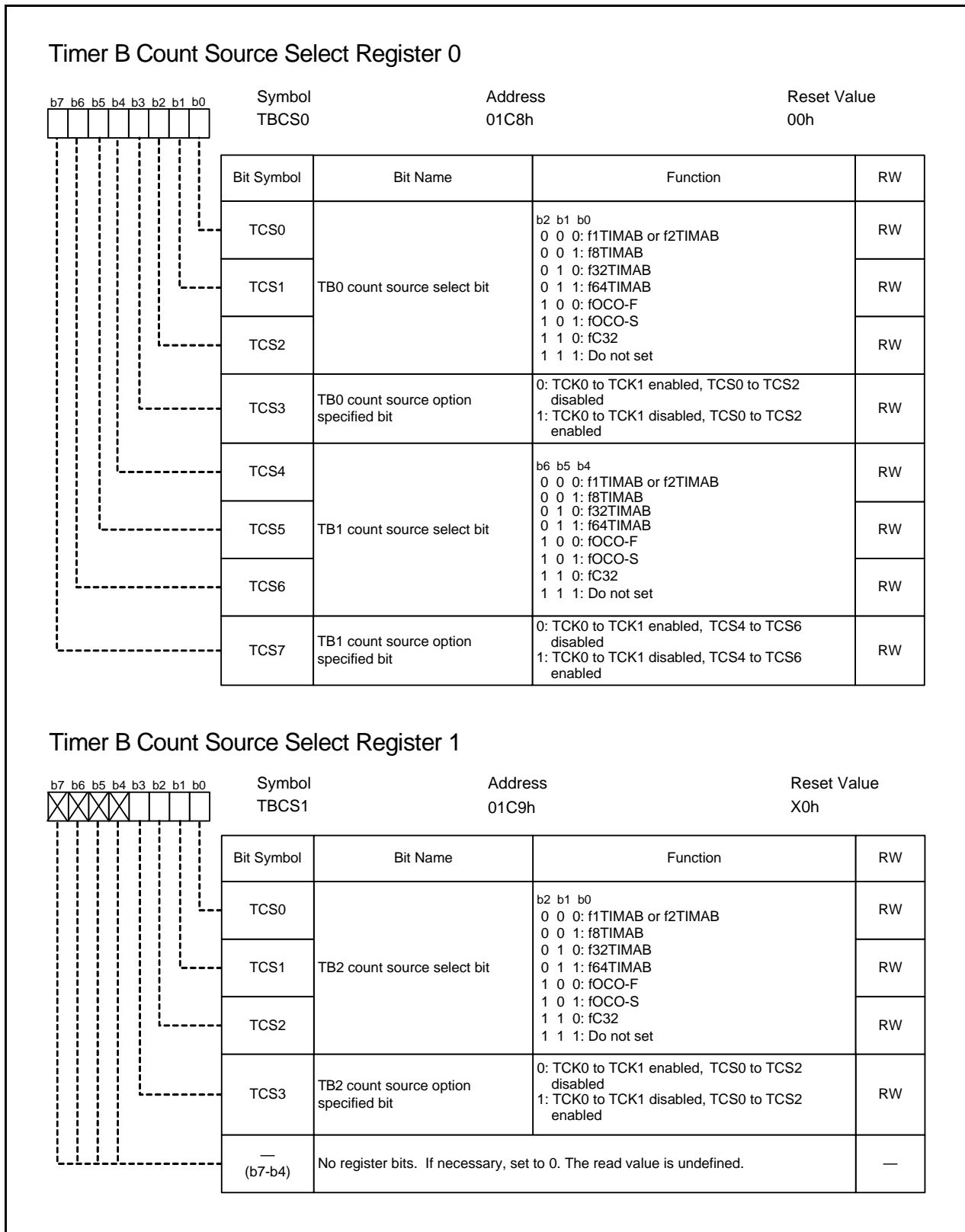
When bits PPWFS12 to PPWFS10 in the PPWFS1 register are 1, the measurement result can be read by reading the TBi-1 register. When these bits are 0, the value in this register is undefined.

### 16.2.5 Pulse Period/Pulse Width Measurement Mode Function Select Register 1 (PPWFS1)



Enabled in pulse period measurement mode or pulse width measurement mode.

## 16.2.6 Timer B Count Source Select Register i (TBCSi) (i = 0 to 1)



TCS2-TCS0 (TB<sub>i</sub> count source select bit) (b2-b0)

TCS6-TCS4 (TB<sub>j</sub> count source select bit) (b6-b4)

Select f1TIMAB or f2TIMAB by setting the PCLK0 bit in the PCLKR register.

### 16.2.7 Timer AB Division Control Register 0 (TCKDIVC0)

Timer AB Division Control Register 0			
b7 b6 b5 b4 b3 b2 b1 b0	Symbol TCKDIVC0	Address 01CBh	Reset Value 0000 X000b
0 0 0 0 X 0 0 0			
Bit Symbol	Bit Name	Function	RW
TCDIV00	Clock select prior to timer AB division bit	0 : f1 1 : fOCO-F	RW
— (b2-b1)	Reserved bits	Set to 0	RW
— (b3)	No register bit. If necessary, set to 0. The read value is undefined.		—
— (b7-b4)	Reserved bits	Set to 0	RW

#### TCDIV00 (Clock select prior to timer AB division bit) (b0)

Set the TCDIV00 bit while timers A and B are stopped.

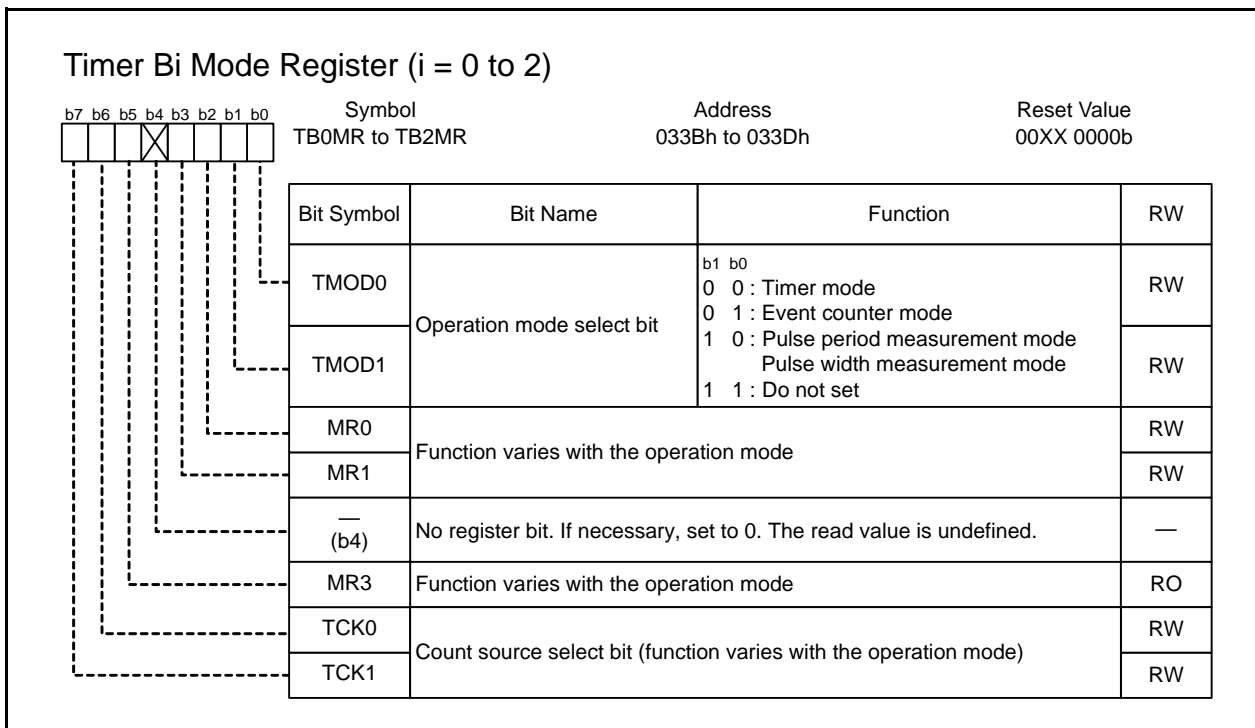
Set the TCDIV00 bit before setting other registers associated with timer B.

After changing the TCDIV00 bit, set other registers associated with timer B again.

### 16.2.8 Count Start Flag (TABSR)

Count Start Flag			
b7 b6 b5 b4 b3 b2 b1 b0	Symbol TABSR	Address 0320h	Reset Value 00h
Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Count stopped 1 : Count started	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

### 16.2.9 Timer Bi Mode Register (TBiMR) (i = 0 to 2)



## 16.3 Operations

### 16.3.1 Common Operations

#### 16.3.1.1 Operating Clock

The count source for each timer acts as a clock, controlling such timer operations as counting and reloading.

#### 16.3.1.2 Counter Reload Timing

Timer Bi starts counting from the value (n) set in the TBi register. The TBi register consists of a counter and a reload register. The counter starts decrementing the count source from n, reloads a value in the reload register at the next count source after the value becomes 0000h, and continues decrementing. The value written in the TBi register is reflected in the counter and the reload register at the following timings.

- When the count is stopped
- Between when the count starts and the first count source is input
  - The value written to the TBi register is immediately written to the counter and the reload register.
- After the count starts and the first count source is input
  - The value written to the TBi register is immediately written to the reload register.
  - The counter continues counting and reloads the value in the reload register at the next count source after the value becomes 0000h.

### 16.3.1.3 Count Source

Internal clocks are counted in timer mode, pulse period measurement mode, and pulse width measurement mode. Refer to Figure 16.1 “Timer A and B Count Sources” for details. Table 16.4 lists Timer B Count Sources.

f1 is any of the clocks listed below. Refer to 8. “Clock Generator” for details.

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

**Table 16.4 Timer B Count Sources**

Count Source	Bit Setting Value				Remarks
	PCLK0	TCS3 TCS7	TCS2 to TCS0 TCS6 to TCS4	TCK1 to TCK0	
f1TIMAB	1	0	-	00b	f1 or fOCO-F (1)
		1	000b	-	
f2TIMAB	0	0	-	00b	f1 divided by 2 or fOCO-F divided by 2 (1)
		1	000b	-	
f8TIMAB	-	0	-	01b	f1 divided by 8 or fOCO-F divided by 8 (1)
		1	001b	-	
f32TIMAB	-	0	-	10b	f1 divided by 32 or fOCO-F divided by 32 (1)
		1	010b	-	
f64TIMAB	-	1	011b	-	f1 divided by 64 or fOCO-F divided by 64 (1)
fOCO-F	-	1	100b	-	fOCO-F
fOCO-S	-	1	101b	-	fOCO-S
fC32	-	0	-	11b	fC32
		1	110b	-	

PCLK0: Bit in the PCLKR register

TCS7 to TCS0: Bits in registers TBCS0 to TBCS1

TCK1 to TCK0: Bits in the TBiMR register (i = 0 to 2)

Note:

1. Select f1 or fOCO-F by setting the TCDIV00 bit in the TCKDIVC0 register.

### 16.3.2 Timer Mode

In timer mode, the timer counts an internally generated count source. Table 16.5 lists Timer Mode Specifications, Table 16.6 lists Registers and Setting in Timer Mode, and Figure 16.4 shows an Operation Example in Timer Mode.

**Table 16.5 Timer Mode Specifications**

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	<ul style="list-style-type: none"> <li>• Decrement</li> <li>• When the timer underflows, it reloads the reload register value and continues counting.</li> </ul>
Counter cycles	$\frac{1}{(n+1)}$ n: setting value of the TBi register      0000h to FFFFh
Count start condition	Set the TBiS bit to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TBiIN pin function	I/O port
Read from timer	Count value can be read by reading the TBi register.
Write to timer	<ul style="list-style-type: none"> <li>• When not counting The value written to the TBi register is written to both the reload register and the counter.</li> <li>• When counting The value written to the TBi register is only written to the reload register (transferred to the counter when reloaded next).</li> </ul>

i = 0 to 2

TBiS: Bit in the TABSR register

**Table 16.6 Registers and Settings in Timer Mode (1)**

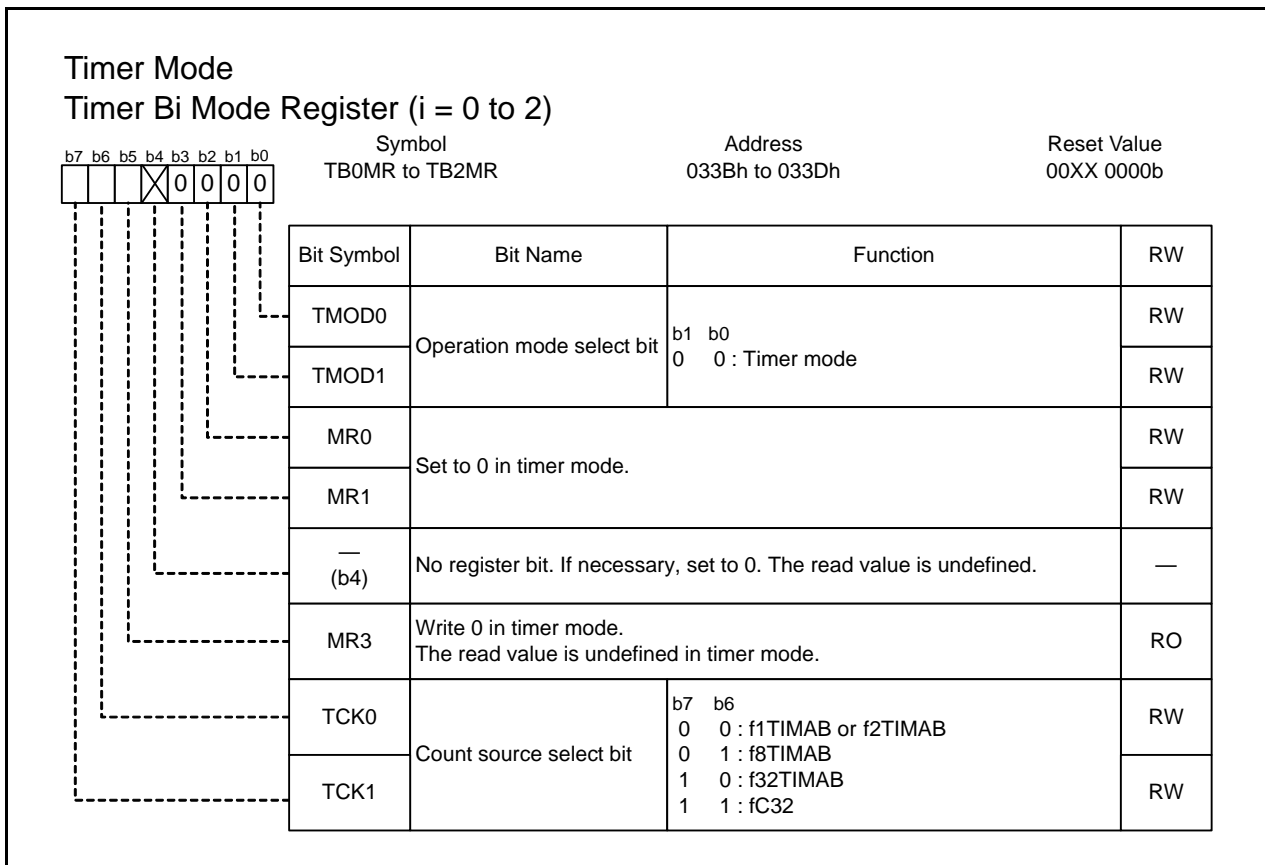
Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TBi1	15 to 0	- (setting unnecessary)
PPWFS1	PPWFS12 to PPWFS10	Set to 0.
TCKDIVC0	TCDIV00	Select the clock used prior to timer AB frequency dividing.
TBCS0 to TBCS1	7 to 0	Select the count source.
TABSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	15 to 0	Set the count value.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 2

Note:

1. This table does not describe a procedure.

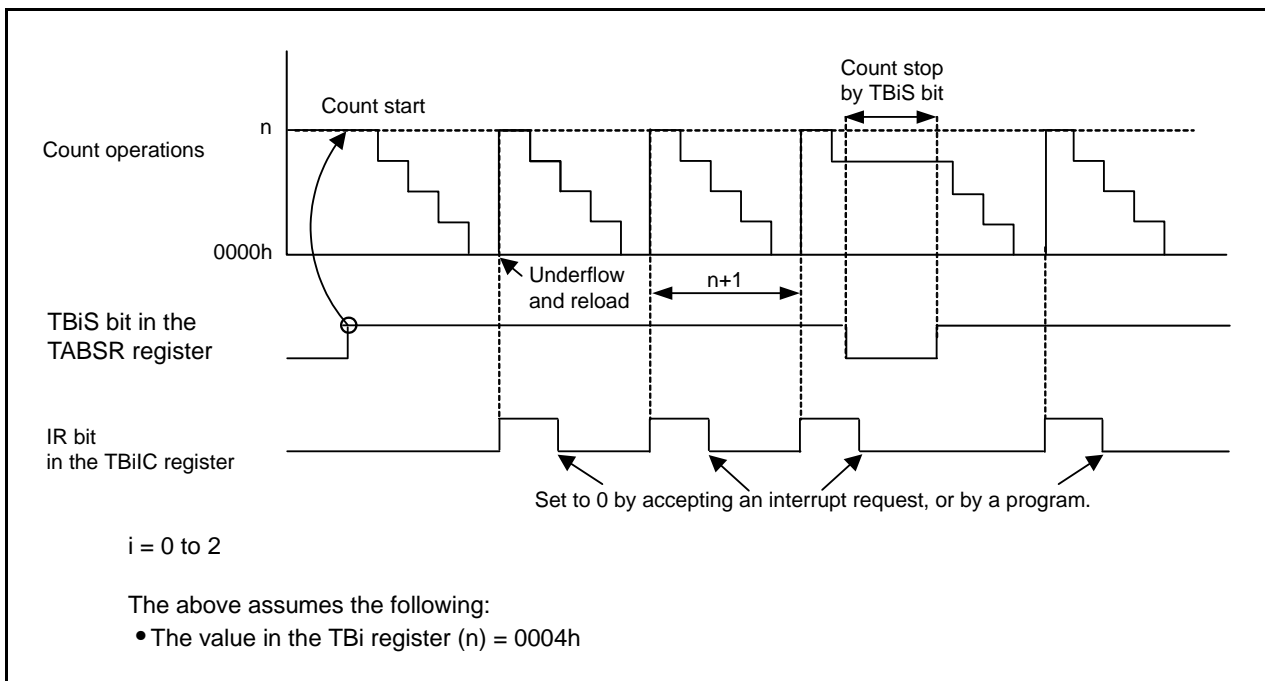




**TCK1 and TCK0 (Count source select bit) (b7-b6)**

These bits are enabled when the TCS3 or TCS7 bit in registers TBCS0 to TBCS1 is set to 0 (bits TCK0 to TCK1 enabled).

Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



**Figure 16.4 Operation Example in Timer Mode**

### 16.3.3 Event Counter Mode

In event counter mode, the timer counts pulses from an external device, or overflows and underflows of other timers. Table 16.7 lists Event Counter Mode Specifications, Table 16.8 lists Registers and Settings in Event Counter Mode, and Figure 16.5 shows an Operation Example in Event Counter Mode.

**Table 16.7 Event Counter Mode Specifications**

Item	Specification
Count sources	<ul style="list-style-type: none"> <li>External signals input to TBIIN pin (active edge can be selected by a program: rising edge, falling edge, or both rising and falling edges)</li> <li>Timer Bj overflow or underflow</li> </ul>
Count operations	<ul style="list-style-type: none"> <li>Decrement</li> <li>When the timer underflows, it reloads the reload register value and continues counting.</li> </ul>
Number of counts	$\frac{1}{(n+1)}$ n: setting value of the TBi register    0000h to FFFFh
Count start condition	Set the TBiS bit to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TBIIN pin function	Count source input
Read from timer	Count value can be read by reading the TBi register.
Write to timer	<ul style="list-style-type: none"> <li>When not counting The value written to the TBi register is written to both the reload register and the counter.</li> <li>When counting The value written to the TBi register is written to only reload register (transferred to counter when reloaded next).</li> </ul>

$i = 0$  to  $2$      $j = i - 1$ , except  $j = 2$  if  $i = 0$

TBiS: Bit in the TABSR register

**Table 16.8 Registers and Settings in Event Counter Mode (1)**

Register	Bit	Function and Setting
PCLKR	PCLK0	- (setting unnecessary)
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TBi1	15 to 0	- (setting unnecessary)
PPWFS1	PPWFS12 to PPWFS10	Set to 0.
TCKDIVC0	TCDIV00	- (setting unnecessary)
TBCS0 to TBCS1	7 to 0	- (setting unnecessary)
TABSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	15 to 0	Set the count value.
TBiMR	7 to 0	Refer to the TBiMR register below.

$i = 0$  to  $2$

Note:

1. This table does not describe a procedure.

Event Counter Mode Timer Bi Mode Register (i = 0 to 2)		Symbol TB0MR to TB2MR	Address 033Bh to 033Dh	Reset Value 00XX 0000b
Bit Symbol	Bit Name	Function	RW	
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW	
TMOD1			RW	
MR0	Count polarity select bit	b3 b2 0 0 : Counts falling edges of an external signal 0 1 : Counts rising edges of an external signal 1 0 : Counts falling and rising edges of an external signal 1 1 : Do not set	RW	
MR1			RW	
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—	
MR3	Write 0 in event counter mode. The read value is undefined in event counter mode		RO	
TCK0	Disabled in event counter mode. Set 0 or 1.		RW	
TCK1	Event clock select bit	0 : Input from TBiIN pin 1 : Timer Bj (j = i - 1; however, j = 2 if i = 0)	RW	

### MR1 and MR0 (Count polarity select bit) (b3-b2)

These bits are enabled when the TCK1 bit is 0 (input from TBiIN pin). When the TCK1 bit is 1 (timer Bj), these bits can be set to 0 or 1.

### TCK1 (Event clock select bit) (b7)

When the TCK1 bit is 1, an event occurs when an interrupt request of timer Bj (j = i - 1; however, j = 2 if i = 0,) is generated. An event occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers

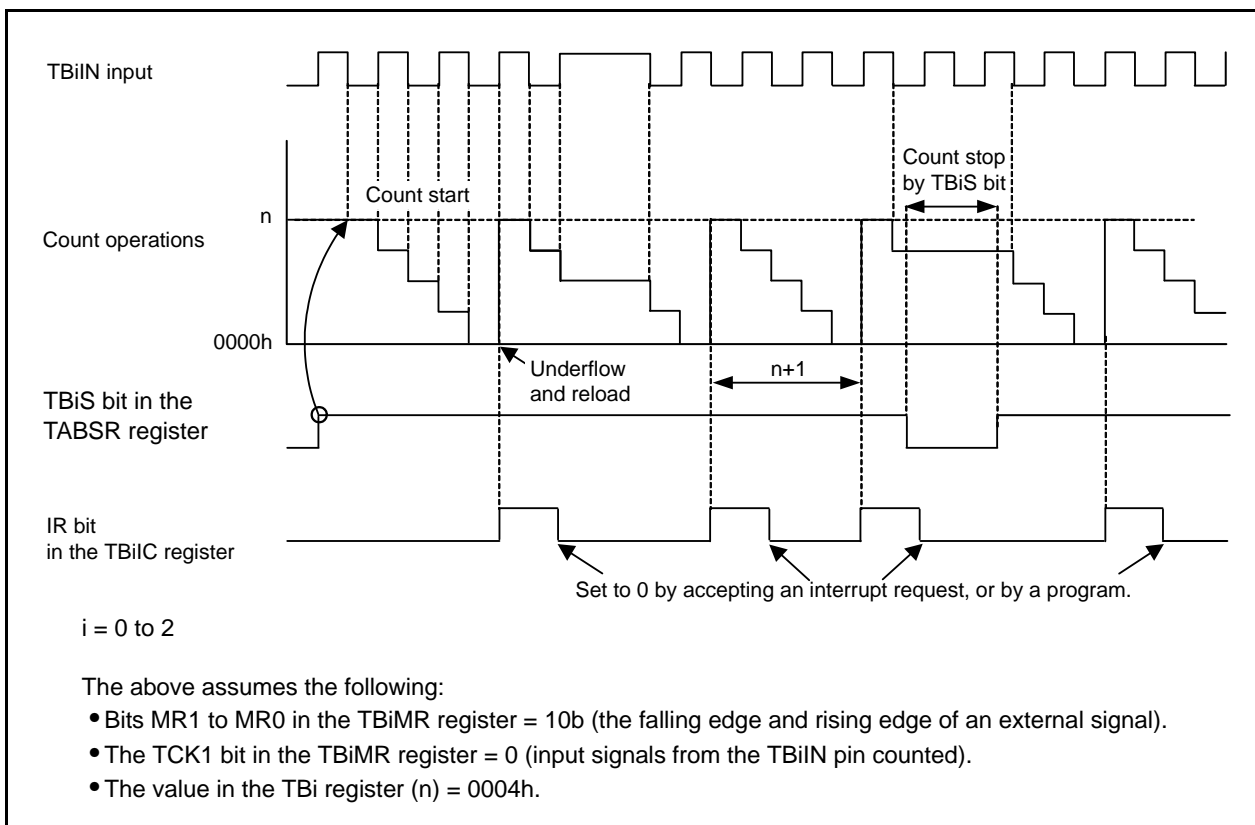


Figure 16.5 Operation Example in Event Counter Mode

### 16.3.4 Pulse Period/Pulse Width Measurement Modes

In pulse period and pulse width measurement modes, the timer measures the pulse period or pulse width of an external signal. Table 16.9 lists Specifications of Pulse Period/Pulse Width Measurement Modes, Table 16.10 lists Registers and Settings in Pulse Period/Pulse Width Measurement Modes, Figure 16.6 shows Operation Example in Pulse Period Measurement Mode, and Figure 16.7 shows an Operation Example in Pulse Width Measurement Mode.

**Table 16.9 Specifications of Pulse Period/Pulse Width Measurement Modes**

Item	Specification
Count sources	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	<ul style="list-style-type: none"> <li>• Increment</li> <li>• The counter value is transferred to the reload register at an active edge of the measurement pulse. The counter value becomes 0000h and count continues.</li> </ul>
Count start condition	Set the TBiS bit to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing <sup>(3)</sup>	<ul style="list-style-type: none"> <li>• When an active edge of measurement pulse is input <sup>(1)</sup></li> <li>• Timer overflow. The MR3 bit in the TBiMR register becomes 1 (overflowed) at the same time an overflow occurs.</li> </ul>
TBiIN pin function	Measurement pulse input
Read from timer	<p>When bits PPWFS12 to PPWFS10 in the PPWFS1 register are 0</p> <ul style="list-style-type: none"> <li>• Value of the reload register (measurement result) can be read by reading the TBi register. <sup>(2)</sup></li> </ul> <p>When bits PPWFS12 to PPWFS10 in the PPWFS1 register are 1</p> <ul style="list-style-type: none"> <li>• Value of the counter (counter value) can be read by reading the TBi register.</li> <li>• Value of the reload register (measurement result) can be read by reading the TBi1 register.</li> </ul>
Write to timer	When not counting, the value written to the TBi register is written to both the reload register and counter.

i = 0 to 2

TBiS: Bit in the TABSR register

Notes:

1. No interrupt request is generated when the first active edge is input after the timer starts counting.
2. The value read from the TBi register is undefined until the second active edge is input after the timer starts counting.
3. When timer Bi in pulse-period measurement mode or pulse-width measurement mode is used as an event or trigger for timer A or timer B other than timer Bi, an event or trigger occurs at both the overflow and active edge of the measurement pulse.

**Table 16.10 Registers and Settings in Pulse Period/Pulse Width Measurement Modes (1)**

Register	Bit	Function and Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write 1 to reset the clock prescaler.
TBi1	15 to 0	Measurement result can be read when the bits in the PPWFS1 register corresponding to timer Bi are 1.
PPWFS1	PPWFS12 to PPWFS10	Set to 1 to read the counter value while counting.
TCKDIVC0	TCDIV00	Select the clock used prior to timer AB frequency dividing.
TBCS0 to TBCS1	7 to 0	Select the count source.
TABSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	15 to 0	Set the initial value. The measurement result can be read when the bits in the PPWFS1 register corresponding to timer Bi are 0. The counter value can be read when the bits in the PPWFS1 register corresponding to timer Bi are 1.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 2

Note:

1. This table does not describe a procedure.

**Pulse Period/Pulse Width Measurement Modes**  
**Timer Bi Mode Register (i = 0 to 2)**

	Symbol TB0MR to TB2MR	Address 033Bh to 033Dh	Reset Value 00XX 0000b																
<table style="border-collapse: collapse; margin: auto;"> <tr> <td style="border: 1px solid black; padding: 2px;">b7</td> <td style="border: 1px solid black; padding: 2px;">b6</td> <td style="border: 1px solid black; padding: 2px;">b5</td> <td style="border: 1px solid black; padding: 2px;">b4</td> <td style="border: 1px solid black; padding: 2px;">b3</td> <td style="border: 1px solid black; padding: 2px;">b2</td> <td style="border: 1px solid black; padding: 2px;">b1</td> <td style="border: 1px solid black; padding: 2px;">b0</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;"></td> <td style="border: 1px solid black; padding: 2px;"></td> <td style="border: 1px solid black; padding: 2px; text-align: center;">X</td> <td style="border: 1px solid black; padding: 2px;"></td> <td style="border: 1px solid black; padding: 2px;"></td> <td style="border: 1px solid black; padding: 2px;"></td> <td style="border: 1px solid black; padding: 2px; text-align: center;">1</td> <td style="border: 1px solid black; padding: 2px; text-align: center;">0</td> </tr> </table>	b7	b6	b5	b4	b3	b2	b1	b0			X				1	0			
b7	b6	b5	b4	b3	b2	b1	b0												
		X				1	0												
Bit Symbol	Bit Name	Function	RW																
TMOD0	Operation mode select bit	b1 b0 1 0 : Pulse period/pulse width measurement modes	RW																
TMOD1			RW																
MR0	Measurement mode select bit	b3 b2 0 0 : Pulse period measurement (measurement between a falling edge and the next falling edge of measured pulse) 0 1 : Pulse period measurement (measurement between a rising edge and the next rising edge of measured pulse) 1 0 : Pulse width measurement (measurement between a falling edge and the next rising edge of measured pulse and between a rising edge and the next falling edge) 1 1 : Do not set	RW																
MR1			RW																
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—																
MR3	Timer Bi overflow flag	0 : No overflow 1 : Overflow	RO																
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW																
TCK1			RW																

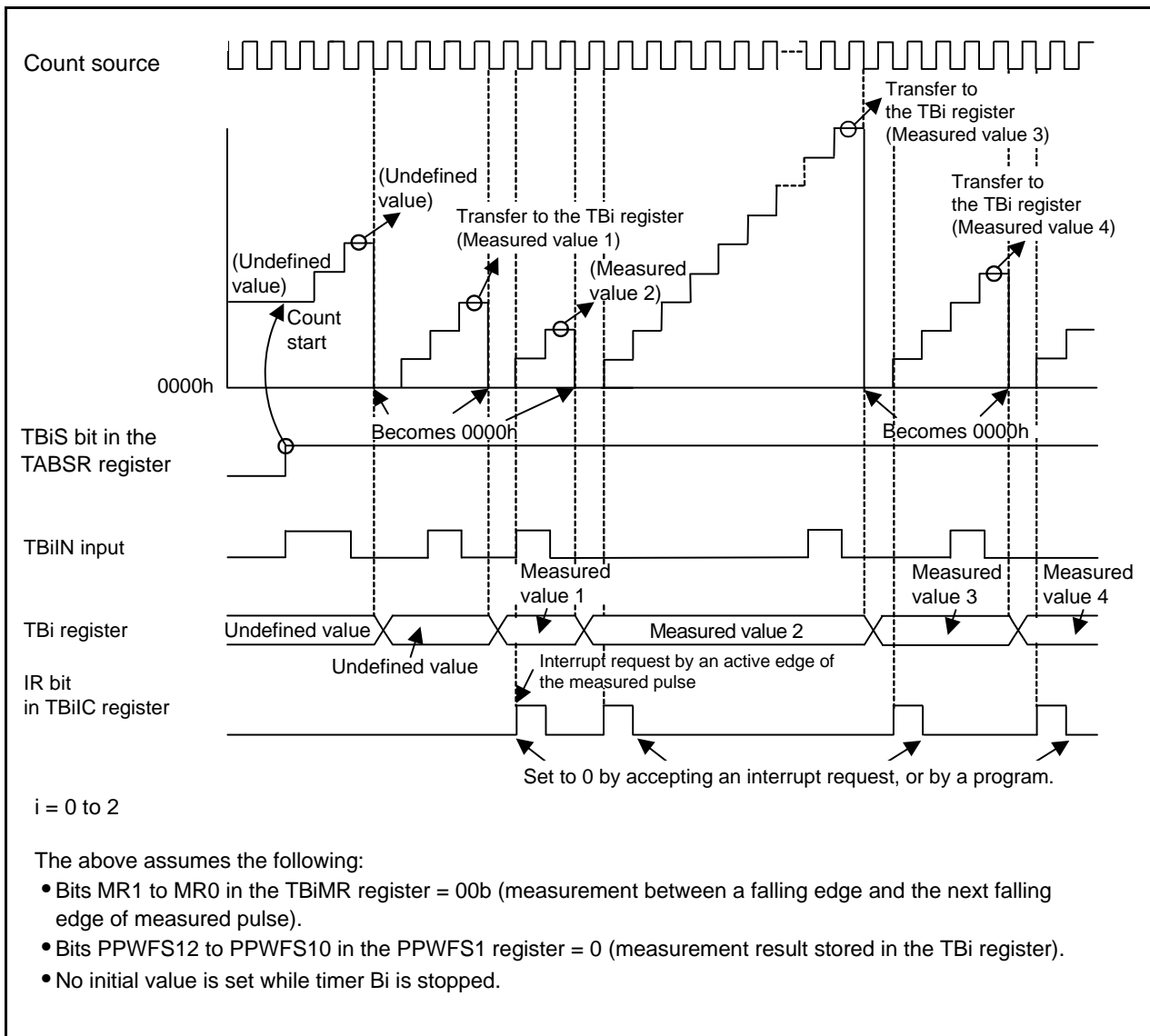
### MR3 (Timer Bi overflow flag) (b5)

This bit is undefined after reset. The MR3 bit becomes 0 (no overflow) by writing to the TBiMR register. The MR3 bit cannot be set to 1 by a program.

### TCK1 and TCK0 (Count source select bit) (b7-b6)

These bits are enabled when the TCS3 bit or TCS7 bit in registers TBSC0 to TBSC1 is set to 0 (TCK0, TCK1 enabled).

Set the PCLK0 bit in the PCLKR register to select f1TIMAB or f2TIMAB.



**Figure 16.6 Operation Example in Pulse Period Measurement Mode**



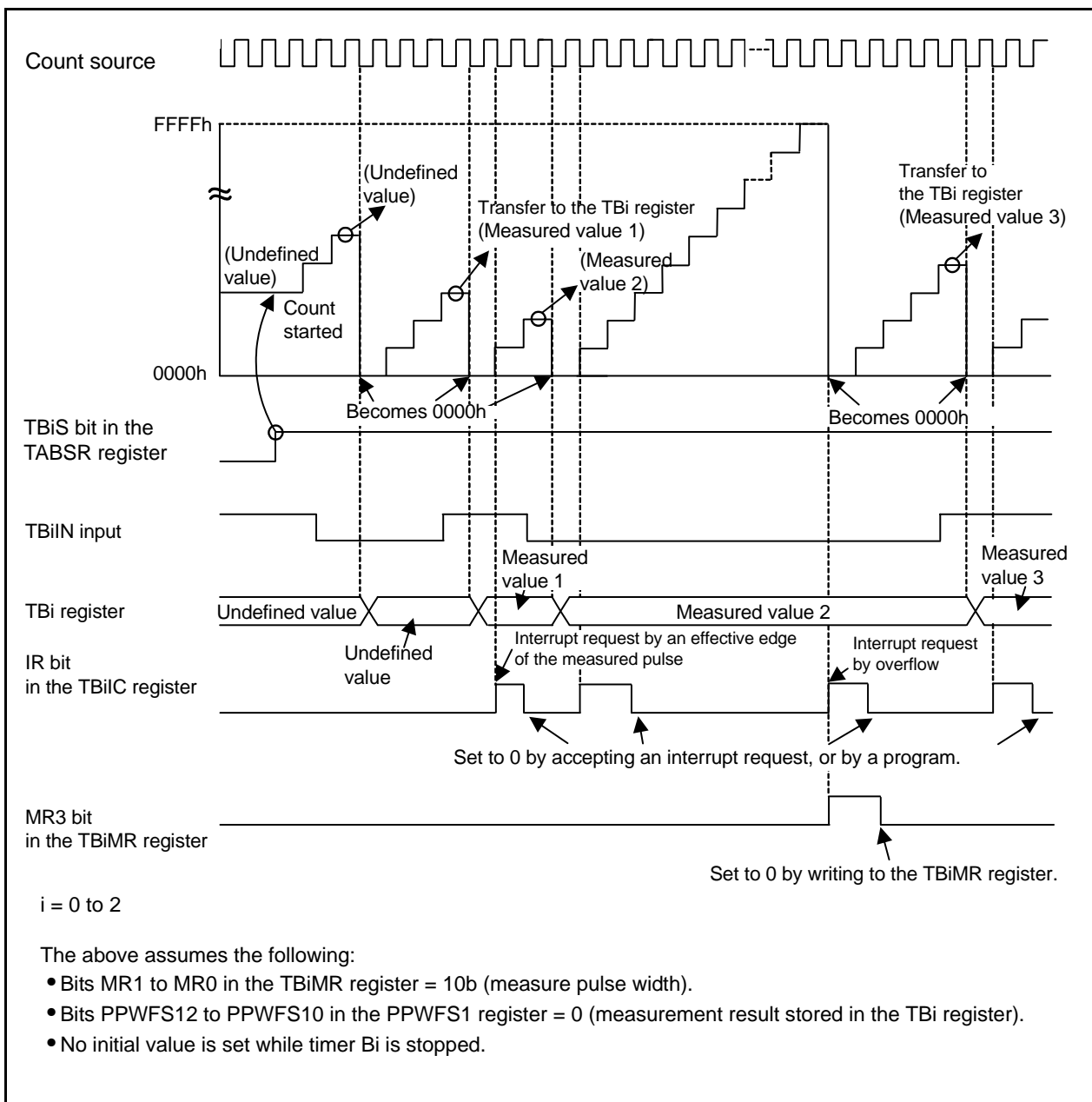


Figure 16.7 Operation Example in Pulse Width Measurement Mode

## 16.4 Interrupts

Refer to individual operation examples for interrupt request generating timing.

Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 16.11 lists Timer B Interrupt Related Registers.

**Table 16.11 Timer B Interrupt Related Registers**

Address	Register	Symbol	Reset Value
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b

## 16.5 Notes on Timer B

### 16.5.1 Common Notes on Multiple Modes

#### 16.5.1.1 Register Setting

The timer is stopped after reset. Set the mode, count source, etc., using registers TBiMR, TBCS0 to TBCS1, TBi, PCLKR and PPWFS1 before setting the TBiS bit in the TABSR register to 1 (count started) (i = 0 to 2).

Rewrite registers TBiMR, TBCS0 to TBCS1, PCLKR, and PPWFS1 while the TBiS bit is 0 (count stopped), regardless of whether after reset or not.

### 16.5.2 Timer B (Timer Mode)

#### 16.5.2.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

### 16.5.3 Timer B (Event Counter Mode)

#### 16.5.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

#### 16.5.3.2 Event

When the TCK1 bit in the TBiMR register is 1, an event occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

When the timer selected by the TCK1 bit uses pulse-period measurement mode or pulse-width measurement mode, an interrupt request is generated at an active edge of the measurement pulse.

## 16.5.4 Timer B (Pulse Period/Pulse Width Measurement Modes)

### 16.5.4.1 MR3 Bit in the TBiMR Register

To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is 1 (count started), be sure to set the same value as previously set to bits TMOD0, TMOD1, MR0, MR1, TCK0, and TCK1, and set bit 4 to 0.

### 16.5.4.2 Interrupts

The IR bit in the TBiIC register becomes 1 (interrupt requested) when an active edge of a measurement pulse is input, or timer Bi overflows ( $i = 0$  to  $2$ ). The source of an interrupt request can be determined by setting the MR3 bit in the TBiMR register within the interrupt routine.

Use the IR bit in the TBiIC register to detect overflows only. Use the MR3 bit only to determine the interrupt source.

### 16.5.4.3 Event or Trigger

When timer Bi in pulse-period measurement mode or pulse-width measurement mode is used as an event or trigger for timer A or timer B other than timer Bi, an event or trigger occurs at both the overflow and active edge of the measurement pulse.

### 16.5.4.4 Operations between Count Start and the First Measurement

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, a timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If the count is started in this state, the MR3 bit may become 1 and a timer Bi interrupt request may be generated after the count starts before an active edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stopped), the same value is written to the counter.

### 16.5.4.5 Pulse Period Measurement Mode

When an active edge and overflow are generated simultaneously, input is not recognized at the active edge because an interrupt request is generated only once. Use this mode so an overflow is not generated, or use pulse width measurement mode.

### 16.5.4.6 Pulse Width Measurement Mode

In pulse width measurement, pulse widths are measured successively. Check whether the measurement result is a high-level width or a low-level width in the user program.

When an interrupt request is generated, read the TBiIN pin level in the interrupt routine, and check whether it is the edge of an input pulse or overflow. The TBiIN pin level can be read from bits in the register of ports sharing a pin.

## 17. Three-Phase Motor Control Timer Function

### 17.1 Introduction

Timers A1, A2, A4, and B2 can be used to output three-phase motor drive waveforms.

Table 17.1 lists Three-Phase Motor Control Timer Function Specifications. Three-Phase Motor Control Timer Function Block Diagrams are shown in Figure 17.1 and Figure 17.2. Table 17.2 lists I/O Ports.

**Table 17.1 Three-Phase Motor Control Timer Function Specifications**

Item	Specification
Operation modes	<ul style="list-style-type: none"> <li>• Triangular wave modulation three-phase mode 0 Three-phase PWM waveform of triangular wave modulation is output. Output data is updated every half cycle of the carrier wave, and an output waveform is generated.</li> <li>• Triangular wave modulation three-phase mode 1 Three-phase PWM waveform of triangular wave modulation is output. Output data is updated every cycle of the carrier wave, and an output waveform is generated.</li> <li>• Sawtooth wave modulation mode Three-phase PWM waveform of sawtooth wave modulation is output.</li> </ul>
Three-phase PWM waveform output pins	6 (U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$ )
Forced cutoff input	Input a low-level signal to the $\overline{SD}$ pin
Used timers	Timers A4, A1, A2 (used in one-shot timer mode) Timer A4: U- $\bar{U}$ -phase waveform control Timer A1: V- $\bar{V}$ -phase waveform control Timer A2: W- $\bar{W}$ -phase waveform control Timer B2 (used in timer mode) Carrier wave cycle control Dead time timer (three 8-bit timers and shared reload register) Dead time control
Output waveform	Triangular wave modulation, sawtooth wave modulation <ul style="list-style-type: none"> <li>• All high or low outputs for one cycle supported</li> <li>• Output logic of high- and low-side turn-on signals can be set separately.</li> </ul>
Carrier wave cycle	Triangular wave modulation : $\frac{(m+1) \times 2}{f_i}$ Sawtooth wave modulation : $\frac{m+1}{f_i}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width	Triangular wave modulation : $\frac{n \times 2}{f_i}$ Sawtooth wave modulation : $\frac{n}{f_i}$ n: Setting value of registers TA4, TA1, and TA2 (of registers TA4, TA41, TA1, TA11, TA2, and TA21 when setting the INV11 bit to 1), 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Dead time (width)	$\frac{p}{f_i}$ or no dead time p: Setting value of the DTT register, 01h to FFh fi: Count source frequency (f1TIMAB, f2TIMAB, f1TIMAB divided by 2, f2TIMAB divided by 2)
Active level	Selectable either active high or active low
Simultaneous conduction prevention function	Simultaneous conduction prevention Simultaneous conduction detection
Interrupt frequency	A timer B2 interrupt is generated every carrier wave cycle to every 15 carrier wave cycles.

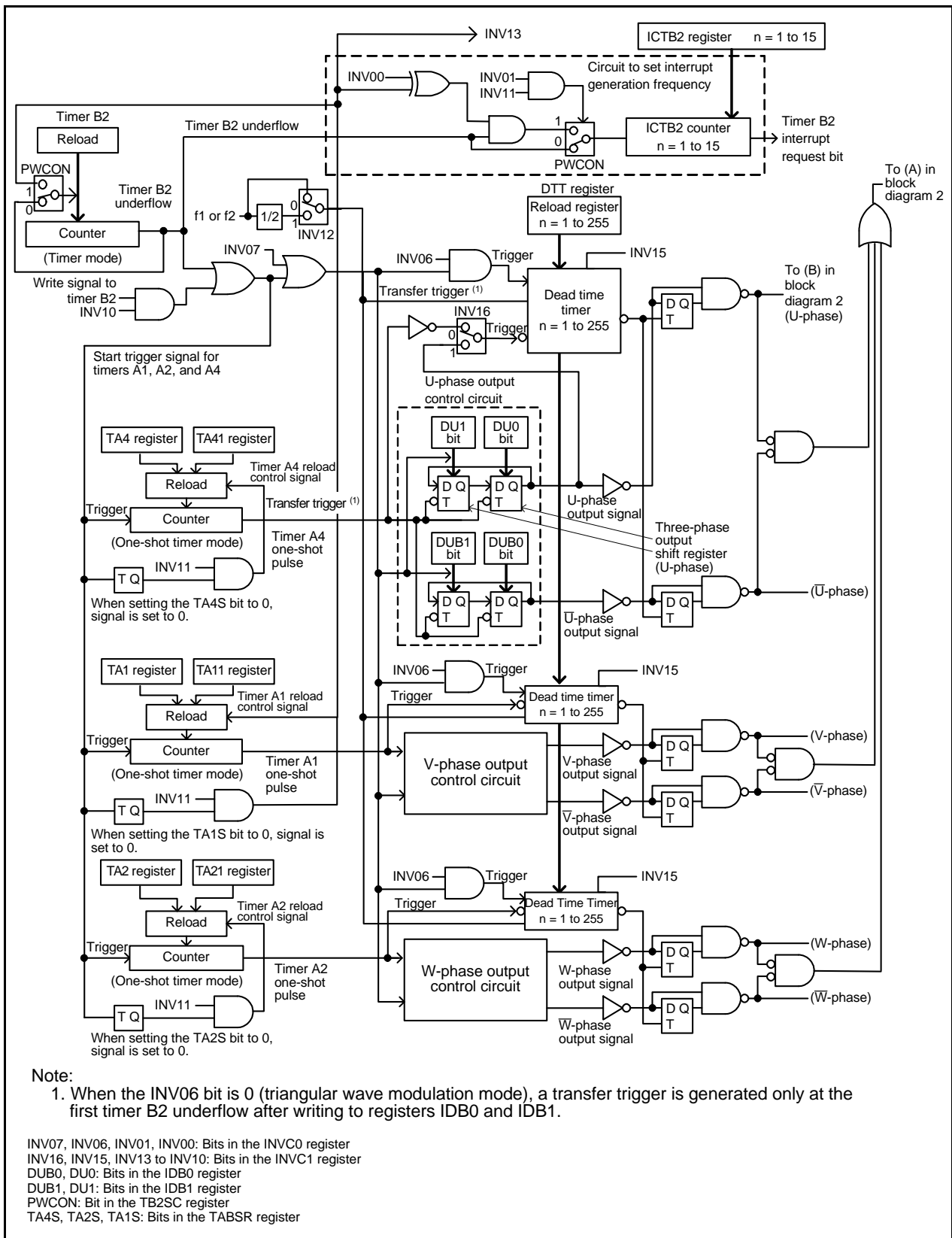


Figure 17.1 Three-Phase Motor Control Timer Function Block Diagram 1

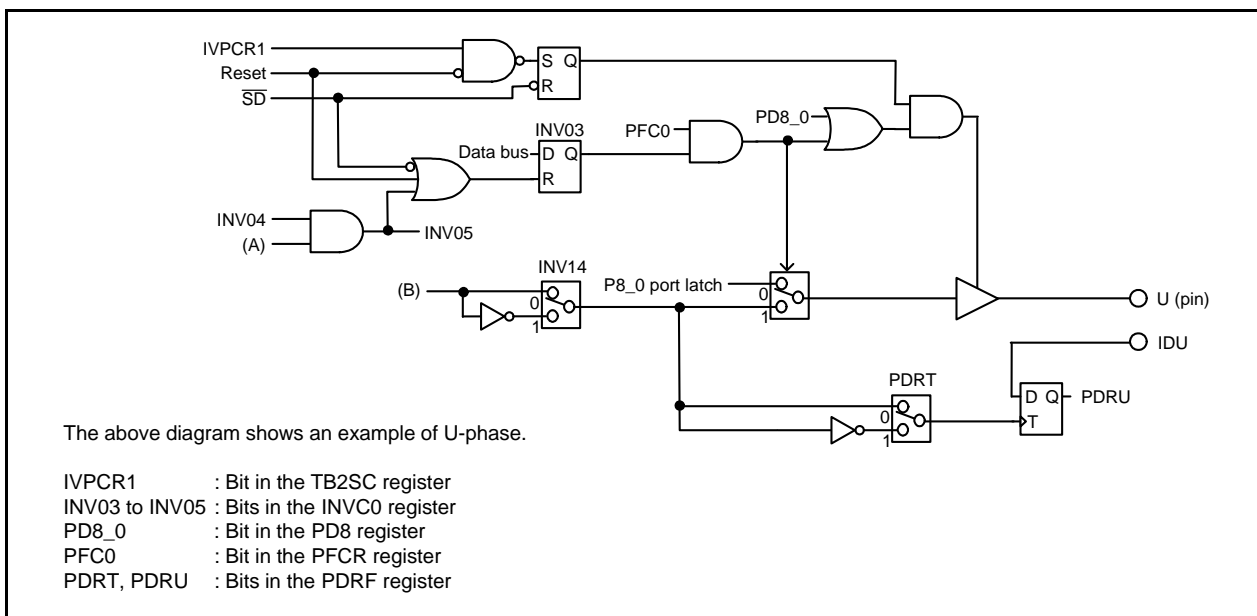


Figure 17.2 Three-Phase Motor Control Timer Function Block Diagram 2

Table 17.2 I/O Ports

Pin Name	I/O	Function
U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$	Output	Three-phase PWM waveform output
$\bar{SD}$	Input (1)	Forced cutoff input
IDU, IDV, IDW	Input (2)	Position-data-retain function input

Notes:

1. Set the port direction bits which share pins to 0 (input mode). When not using the three-phase output forced cutoff function, input a high-level signal to the  $\bar{SD}$  pin.
2. Set the port direction bits which share pins to 0 (input mode).



## 17.2 Registers

Refer to “registers and settings” in each mode for register and bit settings.

Three-phase motor control timer function uses timers A1, A2, A4, and B2. For other registers related to timers A1, A2, A4, and B2, refer to 15. “Timer A” and 16. “Timer B”.

**Table 17.3 Registers**

Address	Register	Symbol	Reset Value
01DAh	Three-Phase Protect Control Register	TPRC	00h
0302h 0303h	Timer A1-1 Register	TA11	XXh XXh
0304h 0305h	Timer A2-1 Register	TA21	XXh XXh
0306h 0307h	Timer A4-1 Register	TA41	XXh XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
0318h	Port Function Control Register	PFCR	0011 1111b
0328h 0329h	Timer A1 Register	TA1	XXh XXh
032Ah 032Bh	Timer A2 Register	TA2	XXh XXh
032Eh 032Fh	Timer A4 Register	TA4	XXh XXh
0334h 0335h	Timer B2 Register	TB2	XXh XXh
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b

### 17.2.1 Timer B2 Register (TB2)

Timer B2 Register		Symbol	Address	Reset Value
(b15) b7	(b8) b0, b7	TB2	0335h to 0334h	Undefined
		Function	Setting Range	RW
		If the setting value is $n$ , the counter frequency is $\frac{n + 1}{f_j}$ Timers A1, A2, and A4 start each time an underflow occurs.	0000h to FFFFh	RW
$f_j$ : Count source frequency				

Read and write in 16-bit units.

The carrier wave cycle is determined by this counter. Timer B2 underflow is a one-shot trigger of timers A1, A2, and A4.

In three-phase mode 1, the reload timing of the TB2 register can be selected by setting the PWCON bit in the TB2SC register.

### 17.2.2 Timer Ai, Ai-1 Register (TAi, TAI1) (i = 1, 2, 4)

Timer Ai, Ai-1 Register (i = 1, 2, 4)		Symbol	Address	Reset Value
(b15) b7	(b8) b0, b7	TA1, TA2, TA4	0329h to 0328h, 032Bh to 032Ah, 032Fh to 032Eh	Undefined
		TA11, TA21, TA41	0303h to 0302h, 0305h to 0304h, 0307h to 0306h	Undefined
		Function	Setting Range	RW
		If the setting value is $n$ , the timer stops when the $n$ th count source is counted after a start trigger is generated. Output signals of each phase change when timers A1, A2, and A4 stop.	0000h to FFFFh	WO

Write to these registers in 16-bit units. Use the MOV instruction to set registers TAi and TAI1. If the TAi or TAI1 register is set to 0000h, no counters start and no timer Ai interrupt is generated.

The TAi or TAI1 register is used to determine waveforms of U-, V-, and W-phases. It is triggered by timer B2 underflow, and operates in one-shot timer mode.

Registers TA1, TA2, and TA4 are used in sawtooth wave modulation mode and three-phase mode 0 of triangular wave modulation mode.

Registers TA1, TA2, TA4, TA11, TA21, and TA41 are used in three-phase mode 1 of triangular wave modulation mode.

When the INVC1 bit in the INVC1 register is set to 0 (dead time enabled), some high- and low-side turn-on signals, whose output level changes from inactive to active, switch the output level when the dead time timer stops.

In three-phase mode 1, the value of the TAI1 register is counted first. Then, the values of registers TAi and TAI1 are counted alternately.

### 17.2.3 Three-Phase PWM Control Register 0 (INVC0)

Three-Phase PWM Control Register 0			
Bit	Symbol	Address	Reset Value
b7			
b6			
b5			
b4			
b3			
b2			
b1			
b0			
	Symbol INVC0	Address 0308h	Reset Value 00h
Bit Symbol	Bit Name	Function	RW
INV00	ICTB2 count condition select bit	b1 b0 0 0 : Timer B2 underflow	RW
INV01		0 1 : Timer B2 underflow when timer A1 reload control signal is 0 1 0 : Timer B2 underflow when timer A1 reload control signal is 1 1 1 : Timer B2 underflow when timer A1 reload control signal is 1	RW
INV02	Three-phase motor control timer function enable bit	0 : Three-phase motor control timer function not used 1 : Three-phase motor control timer function used	RW
INV03	Three-phase motor control timer output control bit	0 : Three-phase motor control timer output disabled 1 : Three-phase motor control timer output enabled	RW
INV04	High- and low-side simultaneous turn-on disable bit	0 : Simultaneous turn-on enabled 1 : Simultaneous turn-on disabled	RW
INV05	High- and low-side simultaneous turn-on detect flag	0 : Not detected 1 : Detected	RW
INV06	Modulation mode select bit	0 : Triangular wave modulation mode 1 : Sawtooth wave modulation mode	RW
INV07	Software trigger select bit	A transfer trigger is generated when the INV07 bit is set to 1. A trigger to the dead time timer is also generated when setting the INV06 bit to 1. The read value is 0.	RW

Set the INVC0 register after the PRC1 bit in the PRCR register is set to 1 (write enabled). Rewrite bits INV00 to INV02, INV04, and INV06 when timers A1, A2, A4, and B2 are stopped.

#### INV01 and INV00 (ICTB2 count condition select bit) (b1-b0)

Bits INV00 and INV01 are enabled only when the INV11 bit in the INVC1 register is 1 (three-phase mode 1).

To set the INV01 bit to 1, set the ICTB2 register first, and then set the INV01 bit to 1. Set the TA1S bit in the TABSR register (timer A1 count start flag) to 1 prior to the first timer B2 underflow.

When the INV11 bit is 0 (three-phase mode 0), the timer B2 underflow is counted regardless of the values of bits INV01 to INV00.

#### INV02 (Three-phase motor control timer function enable bit) (b2)

Set the INV02 bit to 1 to operate the dead time timer, U-, V- and, W-phase output control circuits, and the ICTB2 counter.

**INV03 (Three-phase motor control timer output control bit) (b3)**

Conditions to become 0:

- The INV04 bit is 1 (simultaneous turn-on disabled) and the INV05 bit is 1 (simultaneous turn-on detected).
- The INV03 bit is set to 0 by a program.
- The signal applied to the  $\overline{SD}$  pin is low.

**INV05 (High- and low-side simultaneous turn-on detect flag) (b5)**

The INV05 bit cannot be set to 1 by a program. Set the INV04 bit to 0 when setting the INV05 bit to 0.

**INV06 (Modulation mode select bit) (b6)**

The following table lists items influenced by the INV06 bit.

**Table 17.4 Influence of the INV06 Bit**

Item	INV06 is 0	INV06 is 1
Mode	Triangular wave modulation mode	Sawtooth wave modulation mode
Transfer timing from registers IDB0 and IDB1 to three-phase output shift register	Transferred once by generating a transfer trigger after setting registers IDB0 and IDB1	Transferred every time a transfer trigger is generated
Trigger timing of the dead time timer when the INV16 bit is 0	Falling edge of a one-shot pulse of the timers A1, A2, or A4	<ul style="list-style-type: none"> <li>• Falling edge of a one-shot pulse of the timer A1, A2, or A4</li> <li>• Transfer trigger</li> </ul>
INV13 bit	Enabled when the INV11 bit is 1 and the INV06 bit is 0	Disabled

One of the following conditions must be met to trigger a transfer:

- Timer B2 underflows.
- A value is written to the INV07 bit.
- A value is written to the TB2 register during timer B2 stop when the INV10 bit is 1.

INV16, INV13, INV11: Bits in the INVC1 register

### 17.2.4 Three-Phase PWM Control Register 1 (INVC1)

Three-Phase PWM Control Register 1			
Bit	Symbol	Address	Reset Value
b7	INVC1	0309h	00h
b6			
b5			
b4			
b3			
b2			
b1			
b0			

Bit Symbol	Bit Name	Function	RW
INV10	Timer A1, A2 and A4 start trigger select bit	0 : Timer B2 underflow 1 : Timer B2 underflow and write to the TB2 register when timer B2 stops	RW
INV11	Timer A1-1, A2-1 and A4-1 control bit	0 : Three-phase mode 0 1 : Three-phase mode 1	RW
INV12	Dead time timer count source select bit	0 : f1TIMAB or f2TIMAB 1 : f1TIMAB divided by 2 or f2TIMAB divided by 2	RW
INV13	Carrier wave rise/fall detect flag	0 : Timer A1 reload control signal is 0 1 : Timer A1 reload control signal is 1	RO
INV14	Active level control bit	0 : Active low 1 : Active high	RW
INV15	Dead time disable bit	0 : Dead time enabled 1 : Dead time disabled	RW
INV16	Dead time timer trigger select bit	0 : Falling edge of one-shot pulse of timer (A4, A1, and A2) 1 : Rising edge of the three-phase output shift register (U-, V-, W-phase) output	RW
— (b7)	Reserved bit	Set to 0	RW

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register. Rewrite the INVC1 register while timers A1, A2, A4, and B2 are stopped.

#### INV11 (Timer A1, A2, and A4 start trigger select bit) (b1)

The following table lists items influenced by the INV11 bit.

**Table 17.5 INV11 Bit**

Item	INV11 = 0	INV11 = 1
Mode	Three-phase mode 0	Three-phase mode 1
Registers TA11, TA21 and TA41	Not used	Used
Bits INV00 to INV01 in the INVC0 register	Disabled The ICTB2 counter decrements whenever timer B2 underflows.	Enabled
INV13 bit	Disabled	Enabled when INV11 is 1 and INV06 is 0

When the INV06 bit is 1 (sawtooth wave modulation mode), set the INV11 bit to 0 (three-phase mode 0). Also, when the INV11 bit is 0, set the PWCON bit in the TB2SC register to 0 (timer B2 is reloaded when timer B2 underflows).

**INV13 (Carrier wave rise/fall detect flag) (b3)**

The INV13 bit is enabled only when the INV06 bit is set to 0 (triangular wave modulation mode) and the INV11 bit to 1 (three-phase mode 1).

**INV16 (Dead time timer trigger select bit) (b6)**

If both of the following conditions are met, set the INV16 bit to 1 (rising edge of the three-phase output shift register output).

- The INV15 bit is 0 (dead time timer enabled)
- Bits  $D_{ij}$  and  $D_{iBj}$  always have different values when the INV03 bit is set to 1 (three-phase control timer output enabled). The high- and low-side signals always output opposite level signals at any time except dead time. ( $i = U, V, \text{ or } W; j = 0, 1$ ).

If either of the above conditions is not met, set the INV16 bit to 0 (dead time timer is triggered on the falling edge of a one-shot pulse of timers).

### 17.2.5 Three-Phase Output Buffer Register i (IDBi) (i = 0, 1)

Three-Phase Output Buffer Register i (i = 0, 1)			
Bit	Symbol	Address	Reset Value
b7	IDB0	030Ah	XX11 1111b
b6			
b5	IDB1	030Bh	XX11 1111b
b4			
b3			
b2			
b1			
b0			

Bit Symbol	Bit Name	Function	RW
DUi	U-phase output buffer i	Set the output logical value of the three-phase output shift registers. The set value is reflected in each turn-on signal as follows:  0 : Active (on) 1 : Inactive (off)  When read, the values of the three-phase output shift registers are read.	RW
DUBi	$\bar{U}$ -phase output buffer i		RW
DVi	V-phase output buffer i		RW
DVBi	$\bar{V}$ -phase output buffer i		RW
DWi	W-phase output buffer i		RW
DWBi	$\bar{W}$ -phase output buffer i		RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

Values of registers IDB0 and IDB1 are transferred to the three-phase output shift registers in response to a transfer trigger. After the transfer trigger occurs, the IDB0 register value determines each phase output signal (internal signal) first. Then, the IDB1 register value on the falling edge of timers A1, A2, and A4 one-shot pulse determines each phase output signal (internal signal).

### 17.2.6 Dead Time Timer (DTT)

Dead Time Timer			
Bit	Symbol	Address	Reset Value
b7	DTT	030Ch	Undefined
b0			

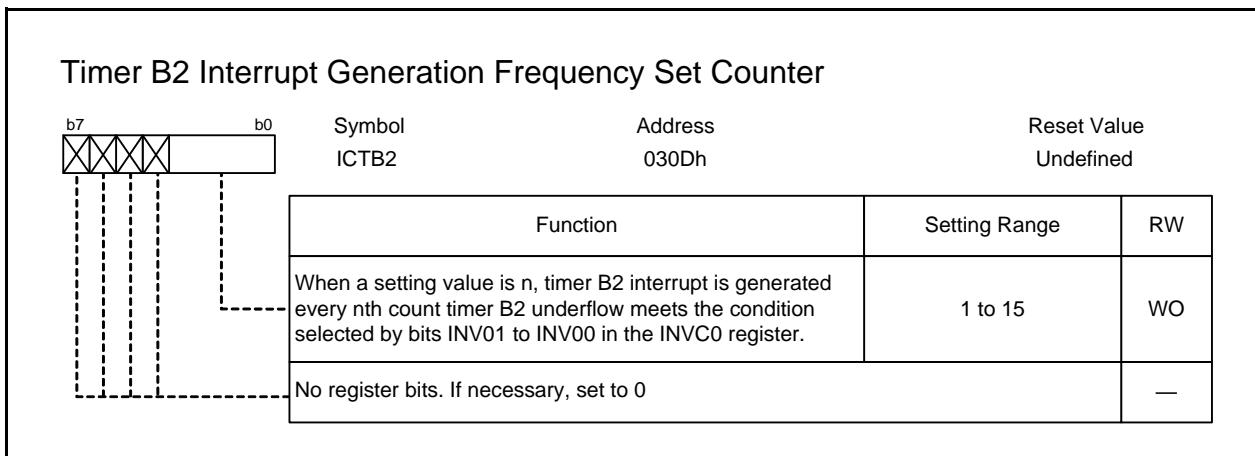
Function	Setting Range	RW
If a setting value is n, the count source is counted n times after the start trigger occurs, and then the timer stops.	1 to 255	WO

Use the MOV instruction to set the DTT register.

The DTT register acts as a one-shot timer which delays the timing for a turn-on signal to be switched to its active level in order to prevent the upper and lower transistors from being turned on simultaneously. The DTT register is enabled when the INV15 bit in the INVC1 register is set to 0 (dead time enabled). No dead time can be set when the INV15 bit is set to 1 (dead time disabled).

Select a trigger by the INV16 bit in the INVC1 register, and a count source by the INV12 bit in the INVC1 register.

### 17.2.7 Timer B2 Interrupt Generation Frequency Set Counter (ICTB2)



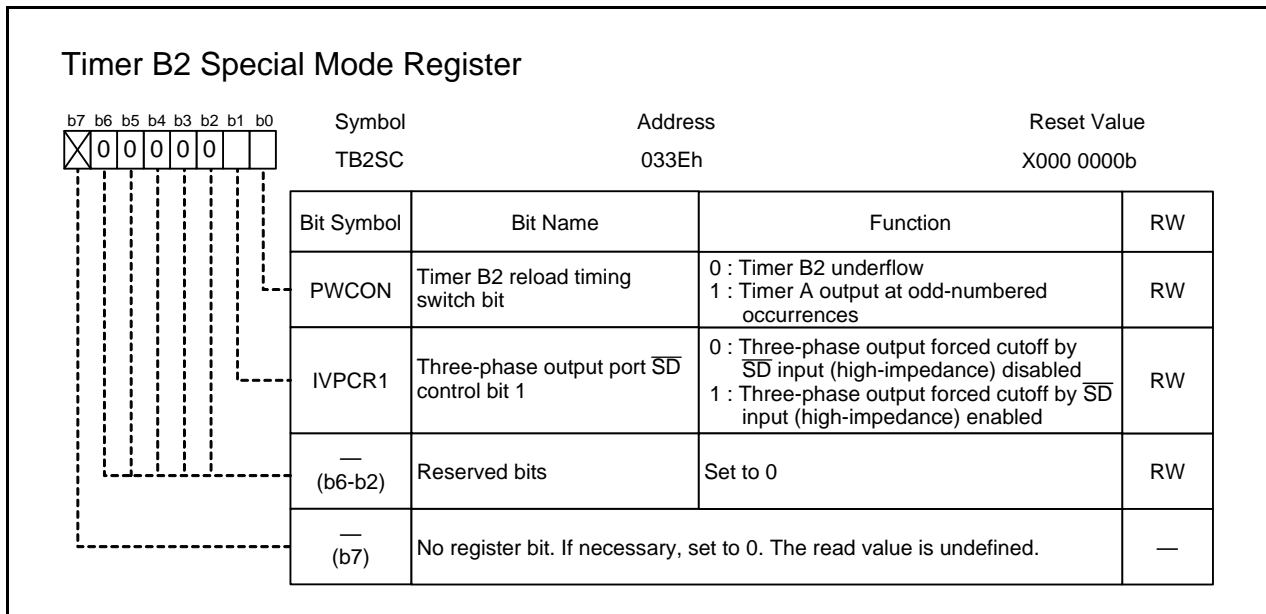
Use the MOV instruction to set the ICTB2 register.

If the INV01 bit in the INVC0 register is 1, set the ICTB2 register when the TB2S bit in the TABSR register is set to 0 (timer B2 counter stopped). If the INV01 bit is 0 and the TB2S bit to 1 (timer B2 counter start), do not set the ICTB2 register when timer B2 underflows.

When bits INV01 to INV00 are 11b, the first interrupt is generated when timer B2 underflows n-1 times if a setting value in the ICTB2 counter is n. Subsequent interrupts are generated every n times timer B2 underflows.



### 17.2.8 Timer B2 Special Mode Register (TB2SC)



Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting this register.

#### PWCON (Timer B2 reload timing switch bit) (b0)

If the INV11 bit in the INVC1 register is 0 (three-phase mode 0) or the INV06 bit in the INVC0 register is 1 (sawtooth wave modulation mode), set the PWCON bit to 0 (timer B2 underflow).

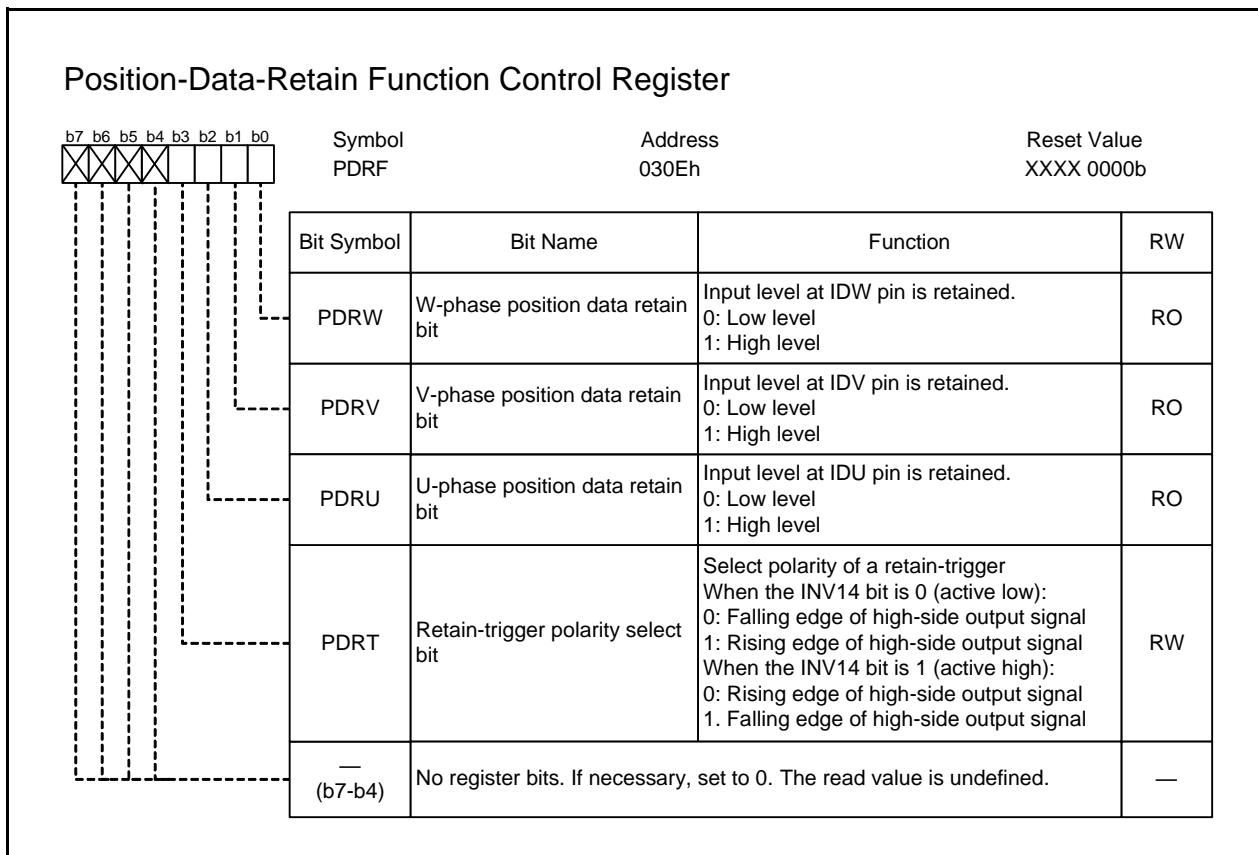
#### IVPCR1 (Three-phase output port $\overline{SD}$ control bit 1) (b1)

Related pins are U,  $\overline{U}$ , V,  $\overline{V}$ , W, and  $\overline{W}$ .

If a low-level signal is applied to the  $\overline{SD}$  pin when the IVPCR1 bit is 1, three-phase motor control timer output is disabled (INV03 bit in the INVC0 register becomes 0). Then, the target pins become high-impedance regardless of the functions those pins are using.

After a forced cutoff, input a high-level signal to the  $\overline{SD}$  pin and set the IVPCR1 bit to 0 to cancel the forced cutoff.

### 17.2.9 Position-Data-Retain Function Control Register (PDRF)



This register is only enabled in three-phase mode.

### 17.2.10 Port Function Control Register (PFCR)

Port Function Control Register			
	Symbol PFCR	Address 0318h	Reset Value 0011 1111b
Bit Symbol	Bit Name	Function	RW
PFC0	Port P8_0 output function select bit	0: I/O port P8_0 1: Three-phase PWM output (U-phase output)	RW
PFC1	Port P8_1 output function select bit	0: I/O port P8_1 1: Three-phase PWM output ( $\bar{U}$ -phase output)	RW
PFC2	Port P7_2 output function select bit	0: I/O port P7_2 1: Three-phase PWM output (V-phase output)	RW
PFC3	Port P7_3 output function select bit	0: I/O port P7_3 1: Three-phase PWM output ( $\bar{V}$ -phase output)	RW
PFC4	Port P7_4 output function select bit	0: I/O port P7_4 1: Three-phase PWM output (W-phase output)	RW
PFC5	Port P7_5 output function select bit	0: I/O port P7_5 1: Three-phase PWM output ( $\bar{W}$ -phase output)	RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is 0.		—

This register is enabled only when the INV03 bit in the INVC0 register is set to 1 (three-phase motor control timer output enabled). Set the TPRC0 bit in the TPRC register to 1 (write enabled) before rewriting this register.

### 17.2.11 Three-Phase Protect Control Register (TPRC)

Three-Phase Protect Control Register			
	Symbol TPRC	Address 01DAh	Reset Value 00h
Bit Symbol	Bit Name	Function	RW
TPRC0	Three-phase protect control bit	Enable write to the PFCR register 0: Write disabled 1: Write enabled	RW
— (b7-b1)	No register bits. If necessary, set to 0. The read value is 0.		—

Once the TPRC0 bit is set to 1 (write enabled) by a program, the set value 1 is retained. To change the register protected by this bit, follow these steps:

- (1) Set the TPRC0 bit to 1.
- (2) Set a value to the PFCR register.
- (3) Set the TPRC0 bit to 0 (write disabled).

## 17.3 Operations

### 17.3.1 Common Operations in Multiple Modes

#### 17.3.1.1 Carrier Wave Cycle Control

Timer B2 controls the cycle of the carrier wave. In triangular wave modulation mode, the cycle of the carrier wave is double the cycle of timer B2 underflow. In sawtooth wave modulation mode, the cycle of the carrier wave is equal to the cycle of timer B2 underflow. Figure 17.3 shows the Relationship between the Carrier Wave Cycle and Timer B2.

Timer B2 underflow is a start trigger for timers A1, A2, and A4, which control the three-phase PWM waveform. However, when the INV10 bit in the INVC1 register is 1, writing to the TB2 register while timer B2 is stopped also generates a trigger for timers A1, A2, and A4.

The frequency of timer B2 interrupt requests can be selected for three-phase motor control timers.

In triangular wave modulation three-phase mode 0 and sawtooth wave modulation mode, when the setting value in the ICTB2 register is  $n$ , a timer B2 interrupt request is generated every  $n$ th count of timer B2 underflow.

In triangular wave modulation three-phase mode 1, when the setting value in the ICTB2 register is  $n$ , a timer B2 interrupt request is generated every  $n$ th time of the timing selected by bits INV01 to INV00 in the INVC0 register. However, when bits INV01 to INV00 are 11b, the first interrupt is generated at the  $n-1$  time of timer B2 underflow.

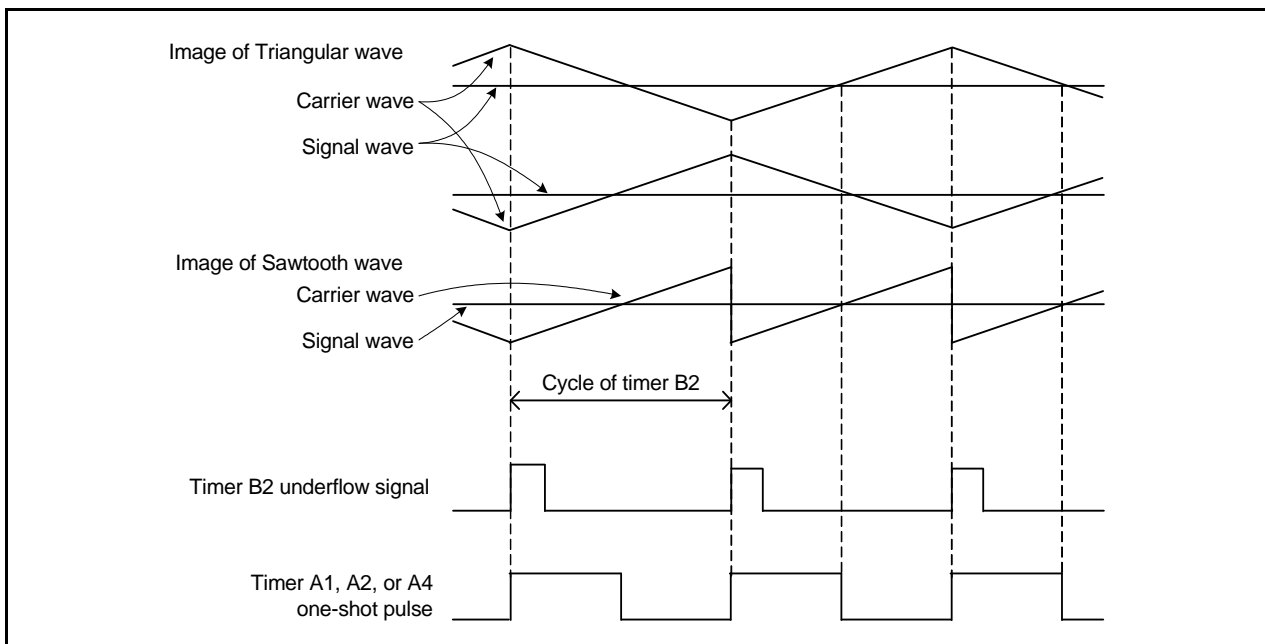


Figure 17.3 Relationship between the Carrier Wave Cycle and Timer B2

### 17.3.1.2 Three-Phase PWM Wave Control

Timer A4 controls U- and  $\bar{U}$ -phase waveforms, timer A1 controls V- and  $\bar{V}$ -phase waveforms, and timer A2 controls W- and  $\bar{W}$ -phase waveforms. Timer Ai (i = 1, 2, 4) starts counting by a trigger selected by the INV10 bit in the INVC1 register, and generates a one-shot pulse (internal signal). The output signal of each phase changes at the falling edge of the one-shot pulse.

Triangular wave modulation three-phase mode 1 counts values in the TAI1 register and TAI register alternately, and generates a one-shot pulse.

### 17.3.1.3 Dead Time Control

Due to delays in the transistors turning off, the upper and lower transistors are turned on simultaneously. To prevent this, there are three 8-bit dead time timers, one in each phase. The reload resistor is shared. When the INV15 bit in the INVC1 register is 0 (dead time enabled), the dead time set in the DTT register is enabled. When the INV15 bit is 1 (dead time disabled), no dead time is set. Select a count source for the dead time timer by setting the INV12 bit in the INVC1 register.

A trigger for the dead time timer can be selected by setting the INV16 bit in the INVC1 register.

When both of the following conditions are met, set the INV16 bit to 1 (the rising edge of the three-phase output shift register is a trigger for the dead time timer):

- The INV15 bit is 0 (dead time enabled).
- Bits Di<sub>j</sub> and Di<sub>Bj</sub> in the IDB<sub>j</sub> register have different values when the INV03 bit in the INVC0 register is 1 (three-phase motor control timer output enabled) (i = U, V or W; j = 0, 1). (During the period other than dead time, the high- and low-side output signals always output opposite level signals.)

If either of the conditions above is not met, set the INV16 bit to 0 (a trigger for the dead time timer is the falling edge of one-shot pulse of the timer).

In sawtooth wave modulation mode, the generation of a transfer trigger causes a trigger for the dead time timer.

### 17.3.1.4 Output Level of Three-Phase PWM Output Pins

Set values to registers IDB0 and IDB1 to select the state of each high- or low-side output signal (either active (on) or not active (off)). The values of registers IDB0 and IDB1 are transferred to the three-phase output shift registers by a transfer trigger. After a transfer trigger is generated, the value set in the IDB0 register becomes the first output signal of each phase (internal signal), and then at the falling edge of a timer A1, A2, or A4 (internal signal) one-shot pulse, the value set in the IDB1 register becomes the output signal of each phase.

A transfer trigger is generated under any of the following conditions:

- At the first timer B2 underflow after registers IDB0 and IDB1 are written (in triangular wave modulation mode)
- Each time timer B2 underflows (in sawtooth wave modulation mode)
- Writing to the TB2 register while timer B2 is stopped (when the INV10 bit in the INVC1 register is 1)
- Setting the INV07 bit in the INVC0 register to 1 (software trigger)

The active level can be selected by the INV14 bit in the INVC1 register.

**Table 17.6 Output Level of Three-Phase PWM Output Pins**

Value Set in Registers IDB0 and IDB1	Output Signal of Each Phase (Internal Signal)	Value Set to the INV14 Bit in the INVC1 Register	
		0 (active, low level)	1 (active, high level)
0 (active (on))	0	Low	High
1 (not active (off))	1	High	Low

### 17.3.1.5 Simultaneous Conduction Prevention

This function prevents the upper and lower output signals from being active simultaneously due to program errors or unexpected program operation. When the high- and low-side output signals become active at the same time while the simultaneous conduction is disabled by the INV04 bit in the INVC0 register, the following occur:

- The INV03 bit in the INVC0 register becomes 0 (three-phase motor control timer output disabled).
- The INV05 bit in the INVC0 register becomes 1 (simultaneous conduction detected).
- Pins U,  $\bar{U}$ , V,  $\bar{V}$ , W, and  $\bar{W}$  become high-impedance.

### 17.3.1.6 Three-Phase PWM Waveform Output Pins

Pins U,  $\bar{U}$ , V,  $\bar{V}$ , W, and  $\bar{W}$  output a PWM waveform under the following conditions:

- The INVC02 bit in the INVC0 register is 1 (three-phase motor control timer function).
- The INVC03 bit in the INVC0 register is 1 (three-phase motor control timer output enabled).
- Bits PFC5 to PFC0 in the PFCR register are 1 (three-phase PWM output (selected independently for each pin)).

The three-phase output forced cutoff by the  $\bar{SD}$  pin is available.

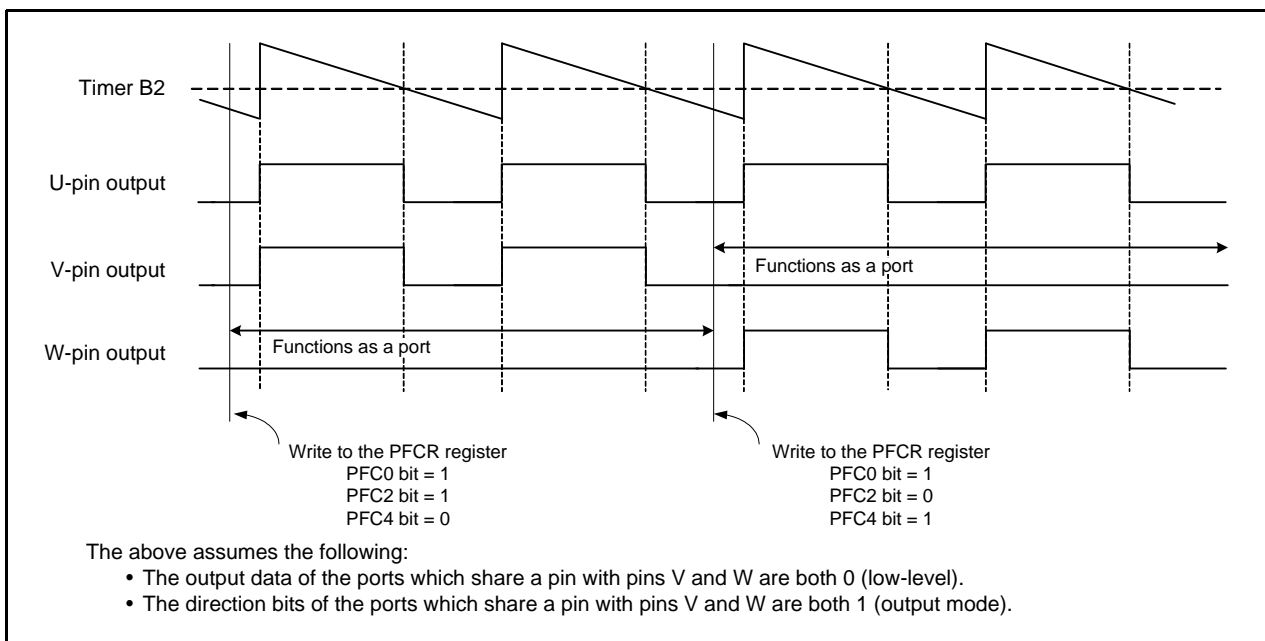
### 17.3.1.7 Three-Phase PWM Output Pin Select

Pins U,  $\bar{U}$ , V,  $\bar{V}$ , W, and  $\bar{W}$  output a three-phase PWM waveform when the PFCi bit (i = 0 to 5) in the PFCR register is 1 (three-phase PWM output). When the PFCi bit is 0 (I/O port), these pins are used as I/O ports (or other peripheral function I/O ports). Therefore, while some of the six pins output a three-phase PWM waveform, the other pins can be used as I/O ports (or other peripheral function I/O ports).

The PFCR register can be rewritten when the TPRC0 bit in the TPRC register is 1 (write to the PFCR register enabled). The functions of the three-phase PWM waveform output pins can be protected from being rewritten due to an unexpected program operation. To prevent rewrite, follow these steps:

- (1) Set the TPRC0 bit to 1.
- (2) Rewrite the PFCR register.
- (3) Set the TPRC0 bit to 0 (write to the PFCR register disabled).

Figure 17.4 shows Three-Phase Output and I/O Port Switch Function Operation.



**Figure 17.4 Three-Phase Output and I/O Port Switch Function Operation**

### 17.3.1.8 Three-Phase Output Forced Cutoff Function

While the INV02 bit in the INVC0 register is 1 (three-phase motor control timer function) and the INV03 bit is 1 (three-phase motor control timer output enabled), when a low-level signal is applied to the  $\overline{SD}$  pin, the INV03 bit in the INVC0 register becomes 0 (three-phase motor control timer output disabled), and pins corresponding to U,  $\overline{U}$ , V,  $\overline{V}$ , W and  $\overline{W}$  outputs change concurrently as follows:

- When the IVPCR1 bit in the TB2SC register is 1 (three-phase output forced cutoff enabled)
  - High-impedance
- When the IVPCR1 bit in the TB2SC register is 0 (three-phase output forced cutoff disabled)
  - I/O ports or other peripheral function I/O ports

However, applying a low-level signal to the  $\overline{SD}$  pin while the IVPCR1 bit is 1 places the pins in a high-impedance state even when the pins are used as functions other than U,  $\overline{U}$ , V,  $\overline{V}$ , W and  $\overline{W}$  outputs. Table 17.7 lists State of Pins U,  $\overline{U}$ , V,  $\overline{V}$ , W, and  $\overline{W}$ .

**Table 17.7 State of Pins U,  $\overline{U}$ , V,  $\overline{V}$ , W, and  $\overline{W}$  (1)**

State of Bit and Pin		Function or State of Pins U, $\overline{U}$ , V, $\overline{V}$ , W and $\overline{W}$
IVPCR1 bit in the TB2SC register	$\overline{SD}$ pin input	
1	High	Three-phase PWM output
	Low	High-impedance
0	High	Three-phase PWM output
	Low	I/O port or other peripheral functions

Note:

1. The above assumes bits INVC02, INVC03, and PFCi are all 1.

The digital debounce filter is available for the  $\overline{SD}$  pin. When the  $\overline{SD}$  pin level remains at a level longer than the width of the digital debounce filter, the level is transferred to the internal circuit. The NDDR register can be set the digital debounce filter width. Refer to 13.4.3 “ $\overline{NMI}/\overline{SD}$  Digital Filter” for details.

To return the pin function to three-phase PWM output after a forced cutoff, follow these steps:

- (1) Apply a high-level signal to the  $\overline{SD}$  pin.
- (2) Wait for more than width of the digital debounce filter (digital debounce filter enabled).
- (3) Set the INV03 bit in the INVC0 register to 1 (three-phase motor control timer output enabled).
- (4) Confirm that the INV03 bit is 1. If the bit is 0, return to step (3).
- (5) Set the IVPCR1 bit to 0 (three-phase output forced cutoff disabled).
- (6) Set the IVPCR1 bit to 1 (when enabling three-phase output forced cutoff again).

When not using the three-phase output forced cutoff function, set a port direction bit which shares the pin with  $\overline{SD}$  input to 0 (input port), and apply a high-level signal to the  $\overline{SD}$  pin.

The same pin is used for both  $\overline{SD}$  input and  $\overline{NMI}$  input. To disable the  $\overline{NMI}$  interrupt, set the PM24 bit in the PM2 register to 0 ( $\overline{NMI}$  interrupt disabled).



### 17.3.1.9 Position-Data-Retain Function

The position-data-retain function employs three position-data input pins: U-, V-, and W-phase. Input levels of IDU, IDV, and IDW inputs are retained. The falling edge or rising edge of the high-side output signal of each phase can be selected by setting the PDRT bit in the PDRF register as a position-data-retain trigger.

For example, in the case of U-phase, when the U-phase trigger is generated, the state of the IDU pin is transferred to the PDRU bit in the PDRF register. The value is retained until the next trigger of the U-phase waveform output.

Figure 17.5 shows Position-Data-Retain Function (U-Phase) Operation.

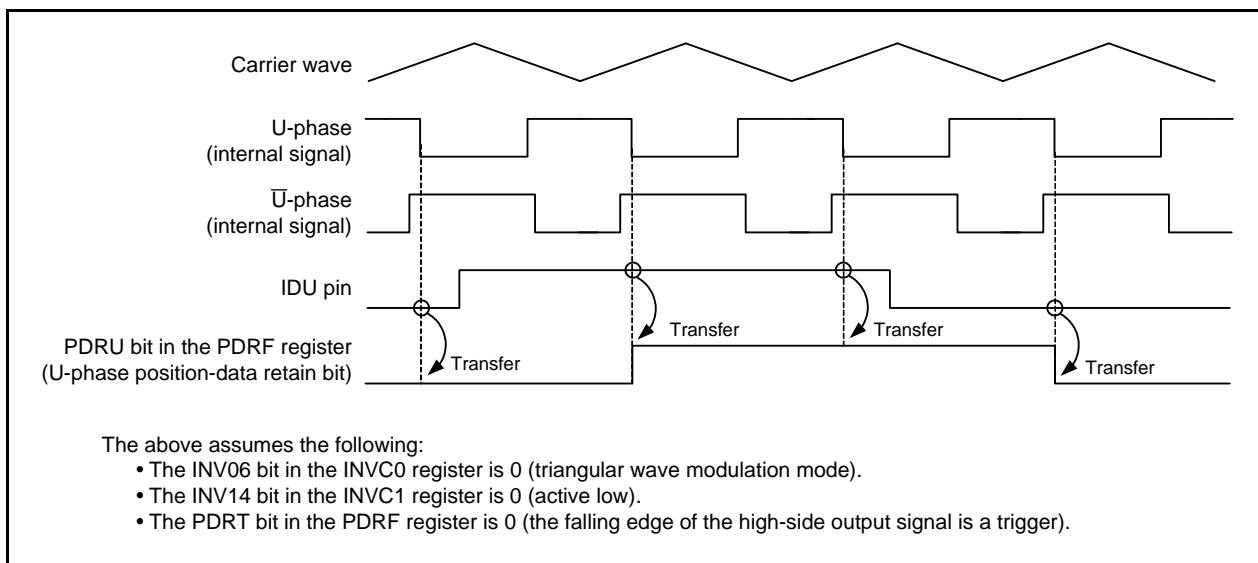


Figure 17.5 Position-Data-Retain Function (U-Phase) Operation

### 17.3.2 Triangular Wave Modulation Three-Phase Mode 0

Triangular wave modulation uses the timer B2 cycle as a reference cycle. Table 17.8 lists Three-Phase Mode 0 Specifications, and Figure 17.6 shows Example of Three-Phase Mode 0 Operation.

**Table 17.8 Three-Phase Mode 0 Specifications**

Item		Specification
Carrier wave cycle		$\frac{(m+1) \times 2}{f_i}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n \times 2}{f_i}$ n: Setting value of the TAI register, 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from three-phase mode 1	Reference cycle	Timer B2 cycle (one-half cycle of the carrier wave)
	Timer B2 reload timing	Timer B2 underflow
	Three-phase PWM waveform control	Counts the value of the TAI register every time a timer Ai start trigger is generated (the TAI1 register is not used).
	Timer B2 interrupt	When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of timer B2 underflow (not influenced by bits INV00 and INV01 in the INVC0 register).
	Detection of a carrier wave cycle (first half or last half)	Not detected (the INV13 bit in the INVC1 register is disabled).

i = 1, 2, 4

**Table 17.9 Registers and Settings in Three-Phase Mode 0 (1/2) (1)**

Register	Bit	Function and Setting
INVC0	INV00	Disabled (Despite the setting, the ICTB2 register counts timer B2 underflow.)
	INV01	
	INV02	Set to 1 (three-phase motor control timer function used).
	INV03	Set to 1 (three-phase motor control timer output enabled).
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 0 (triangular wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 0 (three-phase mode 0).
	INV12	Select a count source for the dead time timer.
	INV13	Disabled
	INV14	Select the active level (either active high or active high).
	INV15	Select dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set the output logic of the three-phase output shift registers.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of the timer B2 interrupt request.
TB2SC	PWCON	Set to 0 (timer B2 underflow).
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Not used.
TB2	15 to 0	Set one-half cycle of the carrier wave.
TRGSR	TA1TGH to TA1TGL	Set to 01b (when using V-phase output control circuit).
	TA2TGH to TA2TGL	Set to 01b (when using W-phase output control circuit).
	TA3TGH to TA3TGL	Not used for three-phase motor control timer.
	TA4TGH to TA4TGL	Set to 01b (when using U-phase output control circuit).

Note:

1. This table does not describe a procedure.

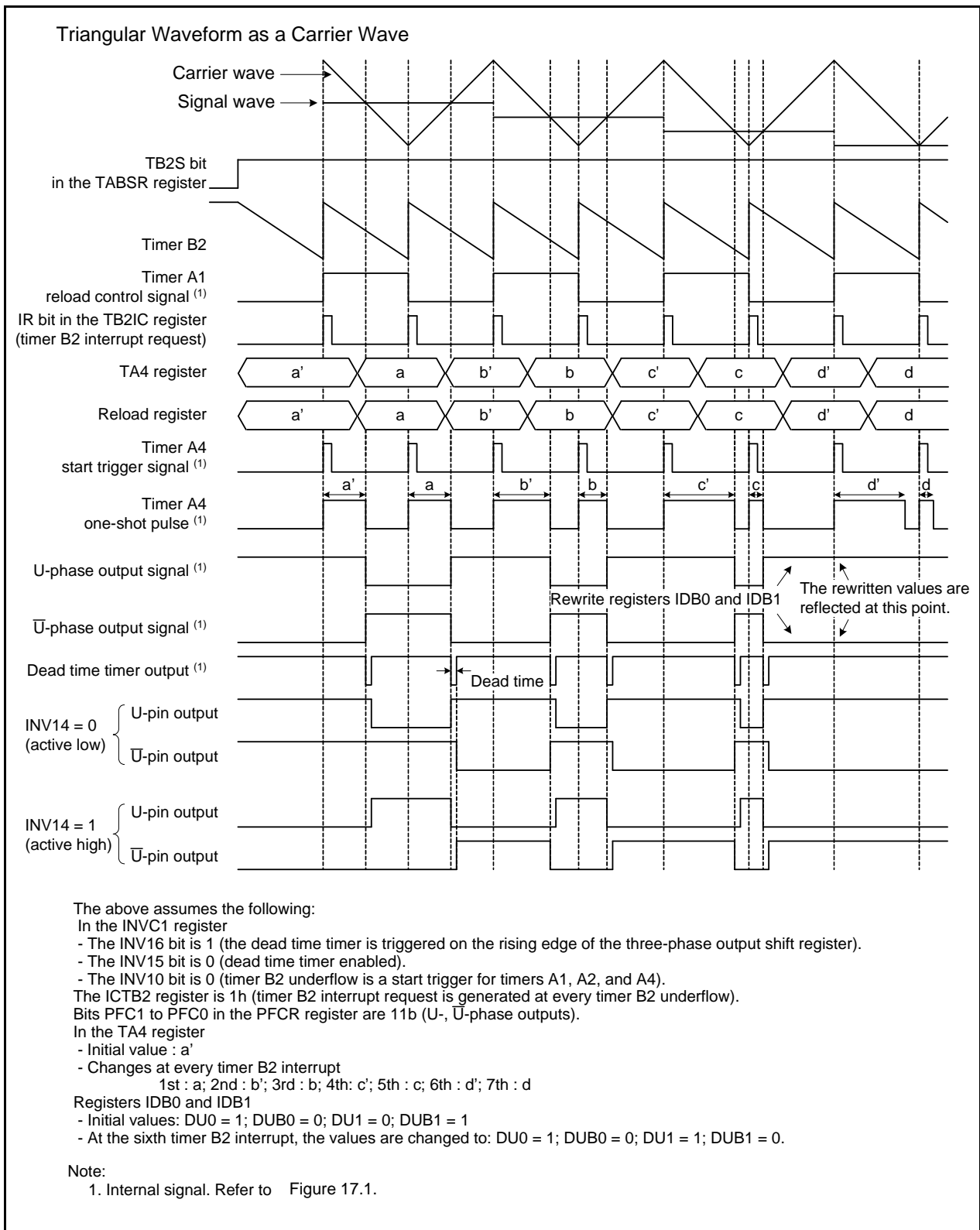
**Table 17.10 Registers and Settings in Three-Phase Mode 0 (2/2) (1)**

Register	Bit	Function and Setting
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	Set to 1 (select a trigger by setting bits TAiTGH and TAiTGL).
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select the clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.

**Figure 17.6 Example of Three-Phase Mode 0 Operation**

### 17.3.2.1 Three-Phase PWM Wave Output Timing Control

In three-phase mode 0, when a start trigger for timers A1, A2, and A4 is generated, the counter starts counting the value of the TAI register ( $i = 1, 2, 4$ ).

### 17.3.2.2 Three-Phase PWM Waveform Output Level Control

In triangular wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift registers by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register becomes the output signal for each phase (internal signal), then at the falling edge of one-shot pulse for timers A1, A2, and A4, followed by the values set in the IDB1 register. Consequently, the three-phase PWM output changes. Afterward, the values in registers IDB0 and IDB1 alternately become output signals for each phase at every falling edge of the one-shot pulse for timers A1, A2, and A4.

When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- The first timer B2 underflow after registers IDB0 and IDB1 are written.
- Writing to the TB2 register when timer B2 is stopped (when the INV10 bit in the INVC1 register is 1).
- Setting the INV07 bit in the INVC0 register to 1 (software trigger).

### 17.3.3 Triangular Wave Modulation Three-Phase Mode 1

Triangular wave modulation uses twice the cycles of timer B2 as a reference cycle. Table 17.11 lists Three-Phase Mode 1 Specifications, and Figure 17.7 shows Example of Three-Phase Mode 1 Operation.

**Table 17.11 Three-Phase Mode 1 Specifications**

Item		Specification
Carrier wave cycle		$\frac{(m + 1) \times 2}{f_i}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n \times 2}{f_i}$ n: Setting value of the TAI register, 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from three-phase mode 0	Reference cycle	Twice the cycle of timer B2 (cycle of the carrier wave)
	Timer B2 reload timing	Select either of the following: <ul style="list-style-type: none"> <li>• Timer B2 underflow</li> <li>• Timer A output at an odd number of times</li> </ul>
	Three-phase PWM waveform control	Counts the values of registers TAI and TAI1 alternately every time a timer Ai start trigger is generated
	Timer B2 interrupt	Select a count timing for the ICTB2 register by bits INV01 to INV00 in the INVC0 register: <ul style="list-style-type: none"> <li>• Timer B2 underflow (each time)</li> <li>• Timer B2 underflow when the INV13 bit in the INVC1 register is 0</li> <li>• Timer B2 underflow when the INV13 bit is 1</li> </ul> When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of the timing selected by setting bits INV01 to INV00.
	Detection of a carrier wave cycle (first half or last half)	Detected (The INV13 bit in the INVC1 register is enabled.)

i = 1, 2, 4

**Table 17.12 Registers and Settings in Three-Phase Mode 1 (1/2) (1)**

Register	Bit	Functions and Setting
INVC0	INV00	Select the timing that the ICTB2 register starts counting.
	INV01	
	INV02	Set to 1 (three-phase motor control timer function used).
	INV03	Set to 1 (three-phase motor control timer output enabled).
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 0 (triangular wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 1 (three-phase mode 1).
	INV12	Select a count source for the dead time timer.
	INV13	Carrier wave state detect flag
	INV14	Select the active level (either active high or active high).
	INV15	Select dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift registers.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of the timer B2 interrupt request.
TB2SC	PWCON	Select timer B2 reload timing.
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Set the one-shot pulse width.
TB2	15 to 0	Set one-half cycle of the carrier wave.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.



**Table 17.13 Registers and Settings in Three-Phase Mode 1 (2/2) (1)**

Register	Bit	Function and Setting
TRGSR	TA1TGH to TA1TGL	Set to 01b (when using V-phase output control circuit).
	TA2TGH to TA2TGL	Set to 01b (when using W-phase output control circuit).
	TA3TGH to TA3TGL	(Not used for three-phase motor control timer.)
	TA4TGH to TA4TGL	Set to 01b (when using U-phase output control circuit).
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	Set to 1 (select a trigger by setting bits TAiTGH and TAiTGL.).
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select the clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.

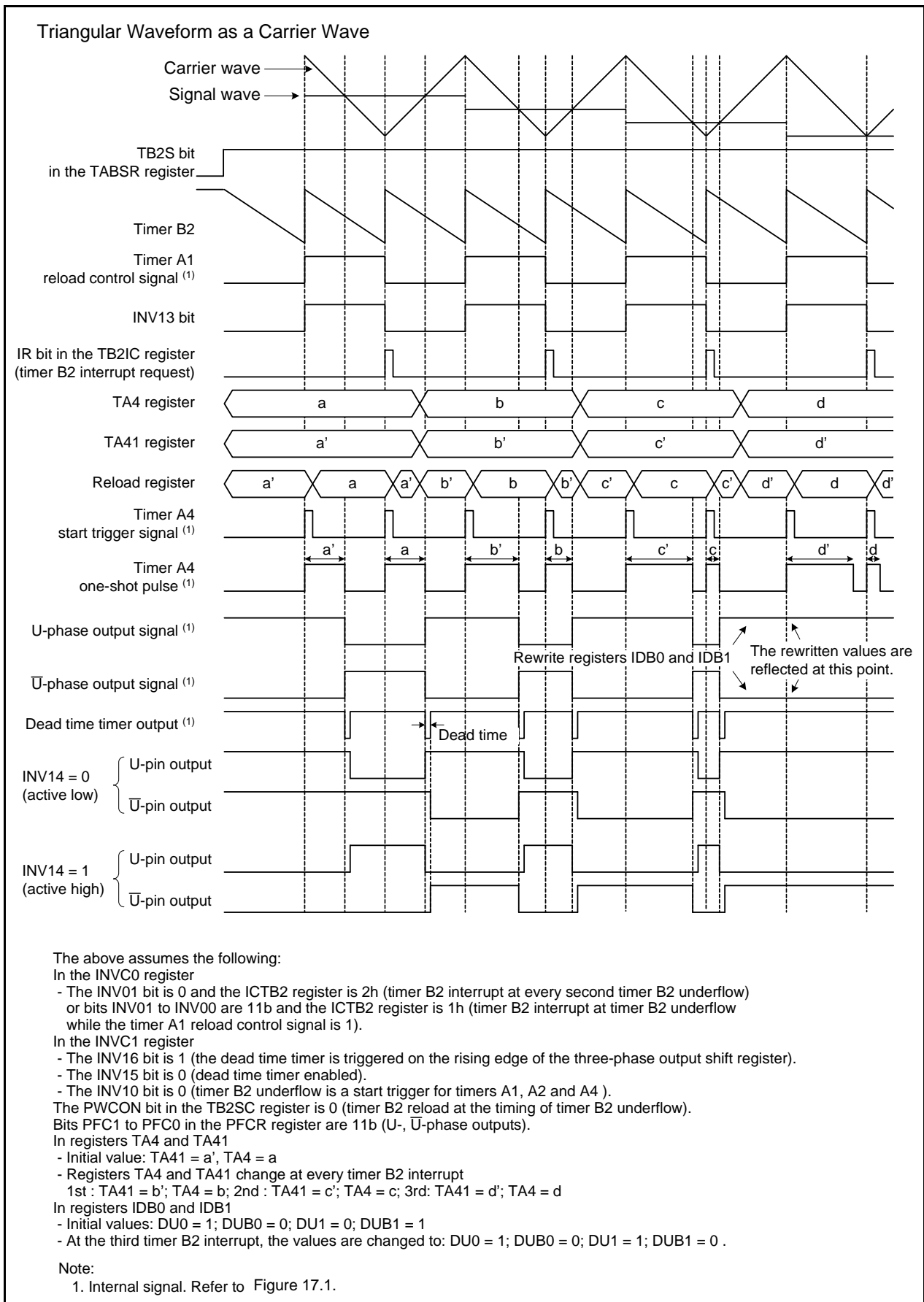


Figure 17.7 Example of Three-Phase Mode 1 Operation

### 17.3.3.1 INV13 Bit in the INVC1 Register

In three-phase mode 1, the INV13 bit can be used to detect whether the cycle of the carrier wave is the first half or the last half. The INV13 bit is a flag which checks the state of timer A1 reload control signals. The timer A1 reload control signal becomes 0 while timer A1 is stopped, and the value is inverted at every start trigger signal for timers A1, A2, and A4. Thus, if the cycle of the carrier wave starts at the first timer B2 underflow, the first half comes when the INV13 bit is 1, and the last half comes when it is 0. Table 17.14 lists Relations of the INV13 Bit with Other Factors.

**Table 17.14 Relations of the INV13 Bit with Other Factors**

INV13 bit	1	0
Timer A1 reload control signal		
One-shot pulse count value	TAi1 register value	TAi register value
Timer B2 underflow	At an odd number of times	At an even number of times
Carrier wave	First half	Last half

i = 1, 2, 4

### 17.3.3.2 Three-Phase PWM Waveform Output Timing Control

In three-phase mode 1, when a start trigger for timers A1, A2, and A4 is generated, the value set in the TAI1 register is counted first. Afterward, the values in registers TAI1 and TAI are alternately counted every time a start trigger for timers A1, A2, and A4 is generated.

When the values in registers TAI1 and TAI are rewritten during processing, the updated value is output from the next carrier wave cycle. Figure 17.8 shows Update Timing of Registers TAI and TAI1 in Three-Phase Mode 1.

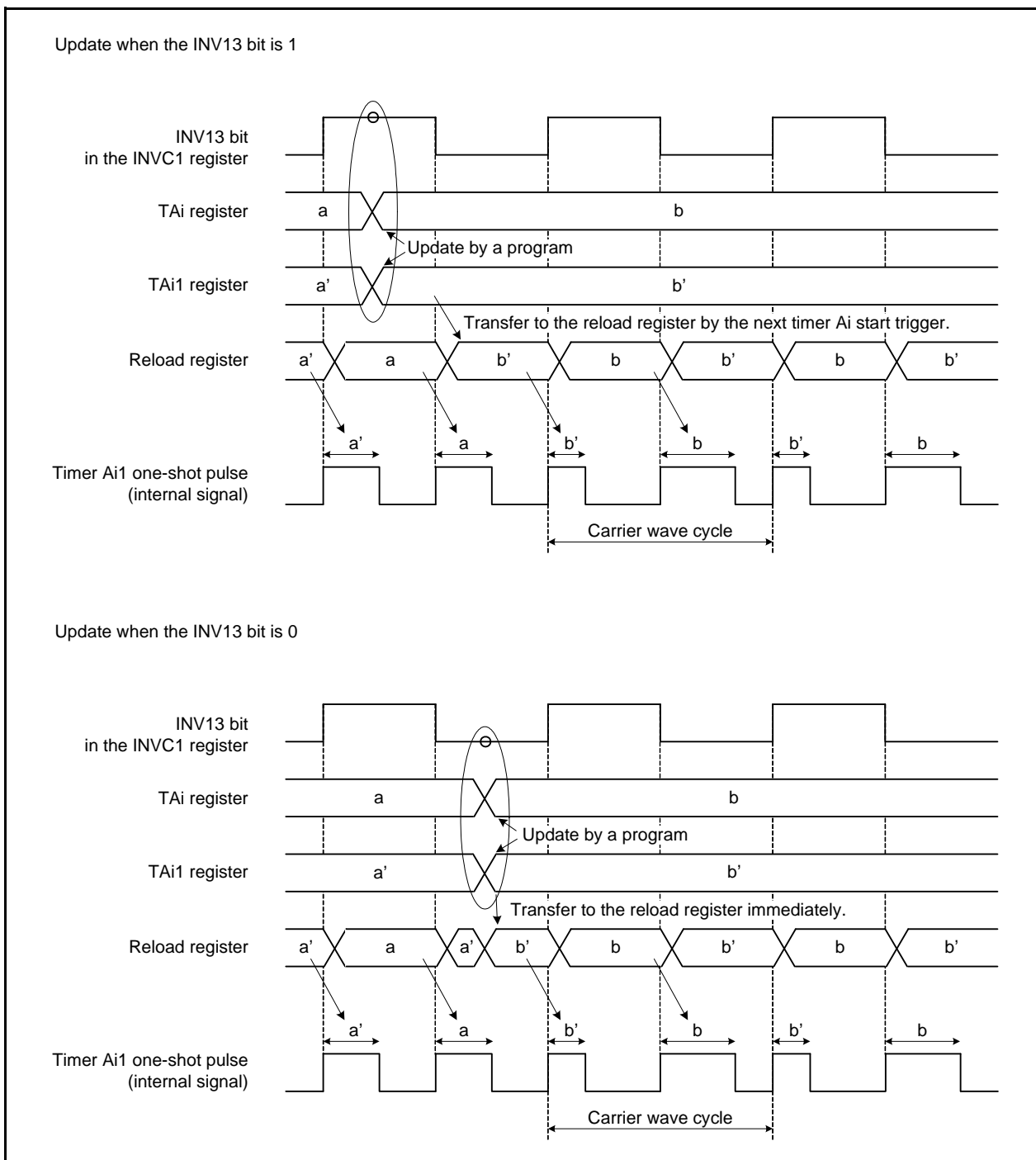


Figure 17.8 Update Timing of Registers TAI and TAI1 in Three-Phase Mode 1

### 17.3.3.3 Carrier Wave Control

In three-phase mode 1, the reload timing of the TB2 register can be selected by setting the PWCON bit in the TB2SC register.

### 17.3.3.4 Three-Phase PWM Waveform Output Level Control

In triangular wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift registers by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then, at the falling edge of one-shot pulse for timers A1, A2, and A4, the values set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Afterward, the values in registers IDB0 and IDB1 alternately become an output signal for each phase at every falling edge of one-shot pulse for timers A1, A2, and A4.

When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- The first timer B2 underflow after registers IDB0 and IDB1 are written.
- Writing to the TB2 register when timer B2 is stopped (when the INV10 bit in the INVC1 register is 1).
- Setting the INV07 bit in the INVC0 register to 1 (software trigger).

### 17.3.4 Sawtooth Wave Modulation Mode

In this mode, the sawtooth wave is modulated. Table 17.15 lists Sawtooth Wave Modulation Mode Specifications, and Figure 17.9 shows Example of Sawtooth Wave Modulation Mode Operation.

**Table 17.15 Sawtooth Wave Modulation Mode Specifications**

Item		Specification
Carrier wave cycle		$\frac{m+1}{f_i}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n}{f_i}$ n: Setting value of the TAI register, 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from triangular wave modulation mode	Reference cycle	Timer B2 cycle (cycle of the carrier wave)
	Timer B2 reload timing	Timer B2 underflow
	Three-phase PWM waveform control	Counts the value of the TAI register every time a timer Ai start trigger is generated (the TAI1 register is not used).
		The output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register at every timer B2 underflow.
	Timer B2 interrupt	When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of timer B2 underflow (not influenced by bits INV00 and INV01 in the INVC0 register).
	Dead time timer trigger	Both of the following: <ul style="list-style-type: none"> <li>• Transfer trigger (generated at every timer B2 underflow)</li> <li>• Falling edge of timer Ai one-shot pulse</li> </ul>
	Detection of a carrier wave cycle (first half or last half)	-

i = 1, 2, 4

**Table 17.16 Registers and Settings in Sawtooth Wave Modulation Mode (1/2) (1)**

Register	Bit	Function and Setting
INVC0	INV00	Disabled (Despite the settings, the ICTB2 register counts timer B2 underflow.)
	INV01	
	INV02	Set to 1 (three-phase motor control timer function used).
	INV03	Set to 1 (three-phase motor control timer output enabled).
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 1 (sawtooth wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 0.
	INV12	Select a count source for the dead time timer.
	INV13	Disabled
	INV14	Select the active level (either active high or active high).
	INV15	Select dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift register.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of timer B2 interrupt request.
TB2SC	PWCON	Set to 0 (timer B2 underflow).
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Not used
TB2	15 to 0	Set the cycle of the carrier wave.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.

**Table 17.17 Registers and Settings in Sawtooth Wave Modulation Mode (2/2) (1)**

Register	Bit	Function and Setting
TRGSR	TA1TGH to TA1TGL	Set to 01b (when using V-phase output control circuit).
	TA2TGH to TA2TGL	Set to 01b (when using W-phase output control circuit).
	TA3TGH to TA3TGL	(Not used for three-phase motor control timer.)
	TA4TGH to TA4TGL	Set to 01b (when using U-phase output control circuit).
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	Set to 1 (select a trigger by setting bits TAiTGH and TAiTGL).
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select the clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4

Note:

1. This table does not describe a procedure.



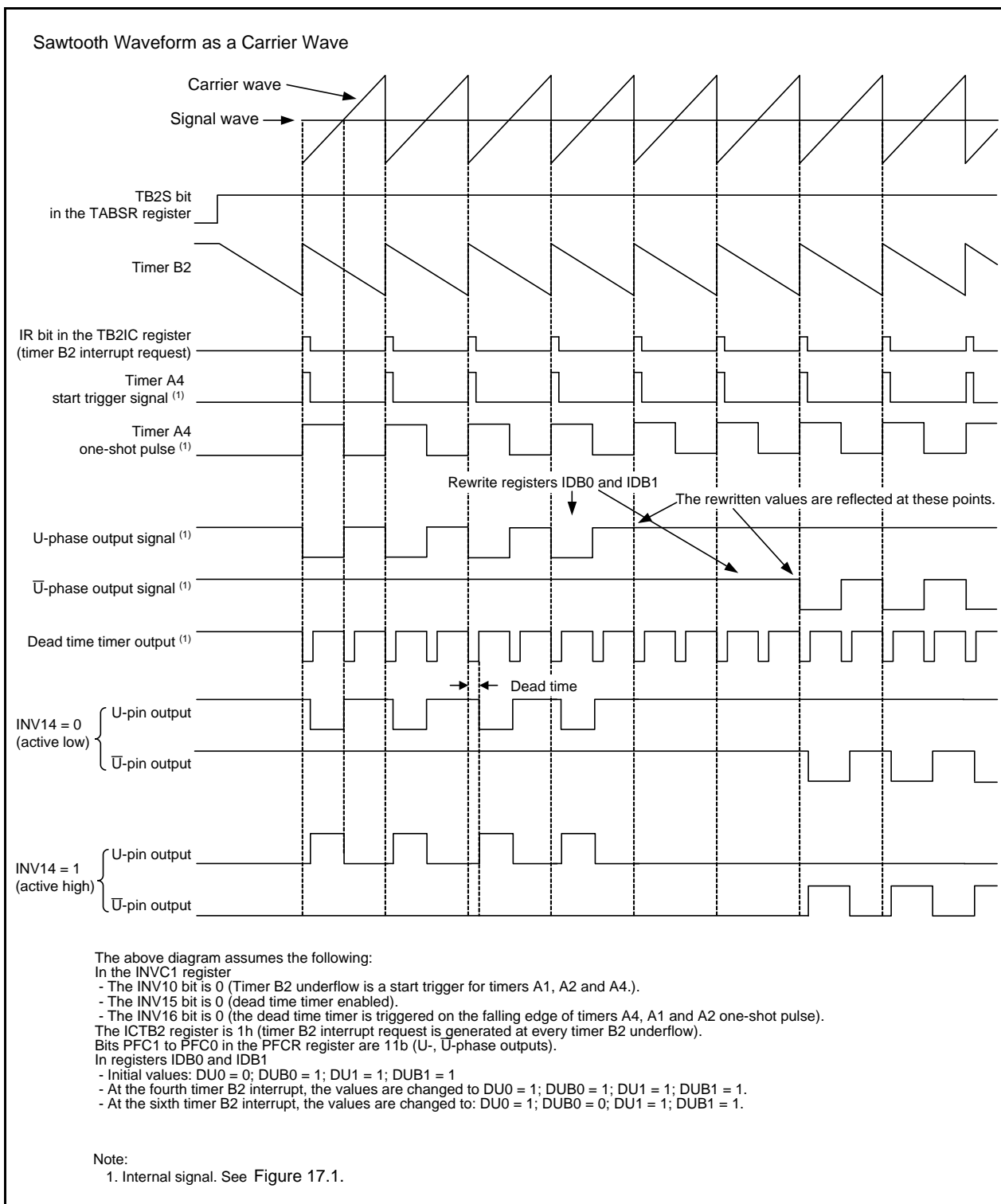


Figure 17.9 Example of Sawtooth Wave Modulation Mode Operation

#### 17.3.4.1 Three-Phase PWM Waveform Output Timing Control

In sawtooth wave modulation mode, when a start trigger for timers A1, A2, and A4 is generated, the counter starts counting the value in the TAI register ( $i = 1, 2, 4$ ).

#### 17.3.4.2 Three-Phase PWM Waveform Output Level Control

In sawtooth wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then at the falling edge of one-shot pulse for timers A1, A2, and A4, the value set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Then, the following two actions are repeated:

(1) The setting levels are transferred to the three-phase output shift register by a transfer trigger generated at timer B2 underflow, and therefore, the value in the IDB0 register becomes output signals for each phase. (2) The values set in the IDB1 register become output signals for each phase at the falling edge of one-shot pulse for timers A1, A2, and A4.

When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- Timer B2 underflow (each time).
- Writing to the TB2 register when timer B2 is stopped (when the INV10 bit in the INVC1 register is 1).
- Setting the INV07 bit in the INVC0 register to 1 (software trigger).

## 17.4 Interrupts

The timer B2 interrupt and timer A1, A2, and A4 interrupts can be used with the three-phase motor control timer.

### 17.4.1 Timer B2 Interrupt

When the setting value in the ICTB2 register is  $n$ , a timer B2 interrupt request is generated at the timings below. For details, refer to the specifications and usage examples of each mode.

In triangular wave modulation three-phase mode 0 and sawtooth wave modulation mode, an interrupt request is generated at the  $n$ th count of timer B2 underflow.

In triangular wave modulation three-phase mode 1, an interrupt request is generated at the  $n$ th count of timing selected by setting bits INV01 to INV00 in the INVC0 register.

Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 17.18 lists the Timer B2 Interrupt Related Register.

**Table 17.18 Timer B2 Interrupt Related Register**

Address	Register	Symbol	Reset Value
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b

### 17.4.2 Timer A1, A2, and A4 Interrupts

A timer  $A_i$  interrupt request is generated at the falling edge of timer  $A_i$  one-shot pulse (internal signal) ( $i = 1, 2, 4$ ). Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 17.19 lists Timer A1, A2, and A4 Interrupt Related Registers.

**Table 17.19 Timer A1, A2, and A4 Interrupt Related Registers**

Address	Register	Symbol	Reset Value
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b

In the timer  $A_i$  interrupt, when the TMOD1 bit in the  $TAiMR$  register is changed from 0 to 1 (from timer mode or event counter mode to one-shot timer mode, PWM mode, or programmable output mode), the IR bit in the  $TAiIC$  register is occasionally becomes 1 (interrupt requested). Thus, when changing the TMOD1 bit, follow the steps below. Also refer to 12.13 “Notes on Interrupts”.

- (1) Set bits ILVL2 to ILVL0 in the  $TAiIC$  register to 000b (interrupt disabled).
- (2) Set the  $TAiMR$  register.
- (3) Set the IR bit in the  $TAiIC$  register to 0 (interrupt not requested).

## 17.5 Notes on Three-Phase Motor Control Timer Function

### 17.5.1 Timer A and Timer B

Refer to 15.5 "Notes on Timer A" and 16.5 "Notes on Timer B".

### 17.5.2 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/CTS2/RTS2/TA1IN/V/TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/ $\overline{W}$ , P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/ $\overline{U}$ /TSUDB

## 18. Timer S

### 18.1 Introduction

Timer S has an input capture/output compare function (IC/OC). The input capture (IC) is used for time measurement and the output compare (OC) is used for waveform generation. The IC/OC has one 16-bit free-running base timer and eight channels for time measurement and waveform generation.

Table 18.1 lists the specifications of the IC/OC.

**Table 18.1 IC/OC Specifications**

	Item	Specification
Time measurement function (1)	Measurement channels	8 channels (channels 0 to 7)
	Trigger input edges	Selectable from rising edge, falling edge, or both edges of the INPC1_j pin
	Digital filter function	8 channels (channels 0 to 7)
	Prescaler function	2 channels (channels 6 and 7)
	Gate function	2 channels (channels 6 and 7)
	Digital debounce filter	1 channel (channel 7)
Waveform generation function (1)	Waveform generating channels	8 channels (channels 0 to 7)
	Waveform generation functions	Single-phase waveform output, inverted waveform output, and SR waveform output
	Output level select function when there is a compare-match	The output level can be changed from low to high or high to low.
	Selectable port function	Waveform output port or programmable I/O port selectable
	Other functions	Selectable initial output level Invertible output waveform
Base timer	Bit length	16 bits
	Count sources	$f1TMS$ or $f2TMS$ divided by $(n + 1)$ , two-phase pulse input divided by $(n + 1)$ $n$ is a G1DV register setting value from 0 to 255. There is no division when $n = 0$ .
	Count operations	Increment, increment/decrement, two-phase pulse signal processing
	Base timer reset conditions	<ul style="list-style-type: none"> <li>• Base timer value matches the G1PO0 register value (RST1)</li> <li>• Low is input to external interrupt pin <math>\bar{INT}1</math> (RST2)</li> <li>• Base timer value matches the G1BTRR register value (RST4)</li> </ul>
Interrupts	IC/OC channel interrupts	6 (IC/OC channel 0 interrupt, IC/OC channel 1 interrupt, IC/OC channel 2 interrupt, IC/OC channel 3 interrupt, IC/OC interrupt 0 (channels 0 to 7), IC/OC interrupt 1 (channels 0 to 7))
	IC/OC base timer interrupts	1 (The base timer interrupt is generated by base timer overflow, or by a base timer reset request that occurs when the G1BTRR register matches the base timer.)

$j = 0$  to  $7$

Note:

1. The time measurement function shares pins with the waveform generation function. Either the time measurement function or waveform generation function is selectable for each channel.

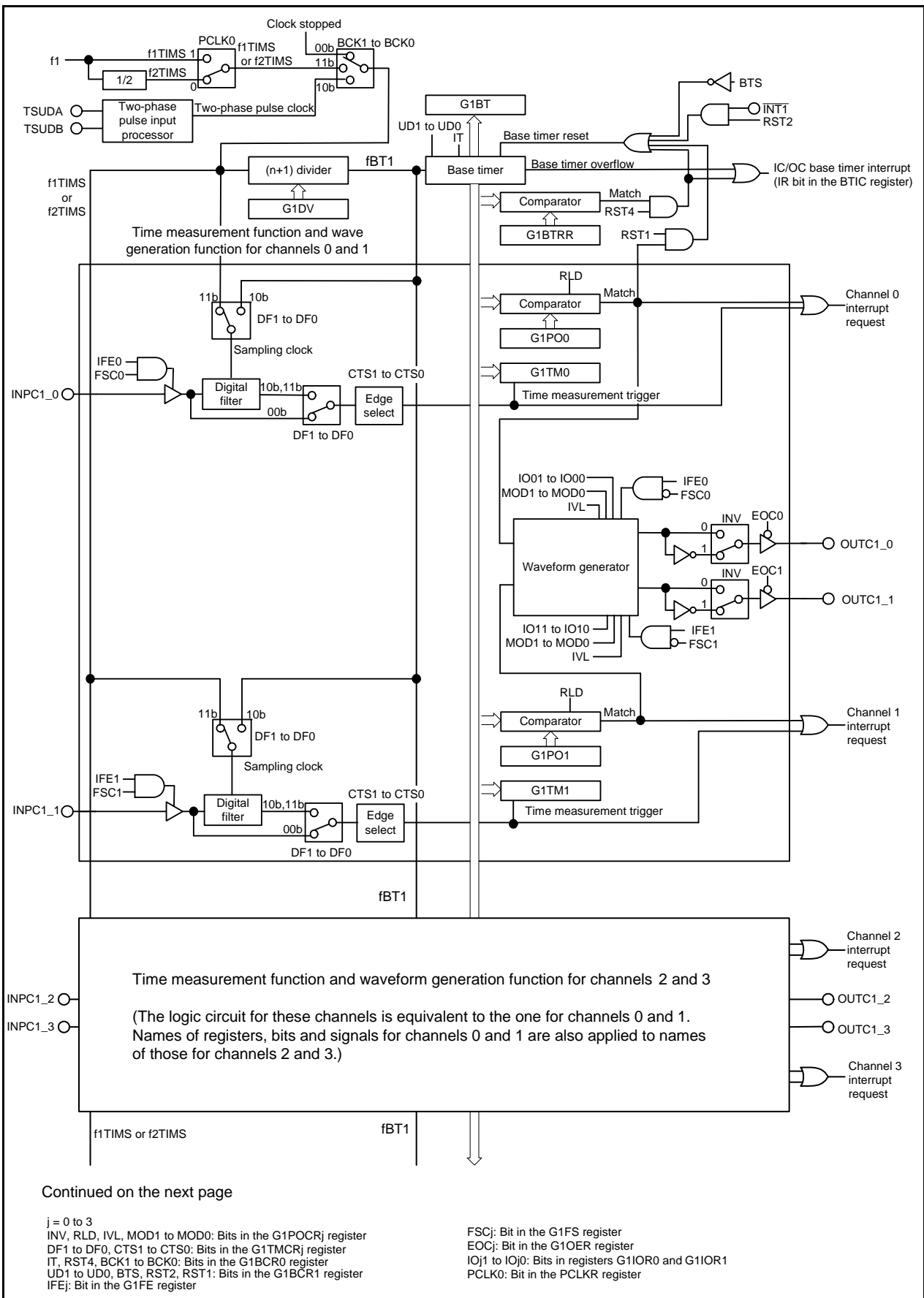


Figure 18.1 IC/OC Block Diagram (1/2)

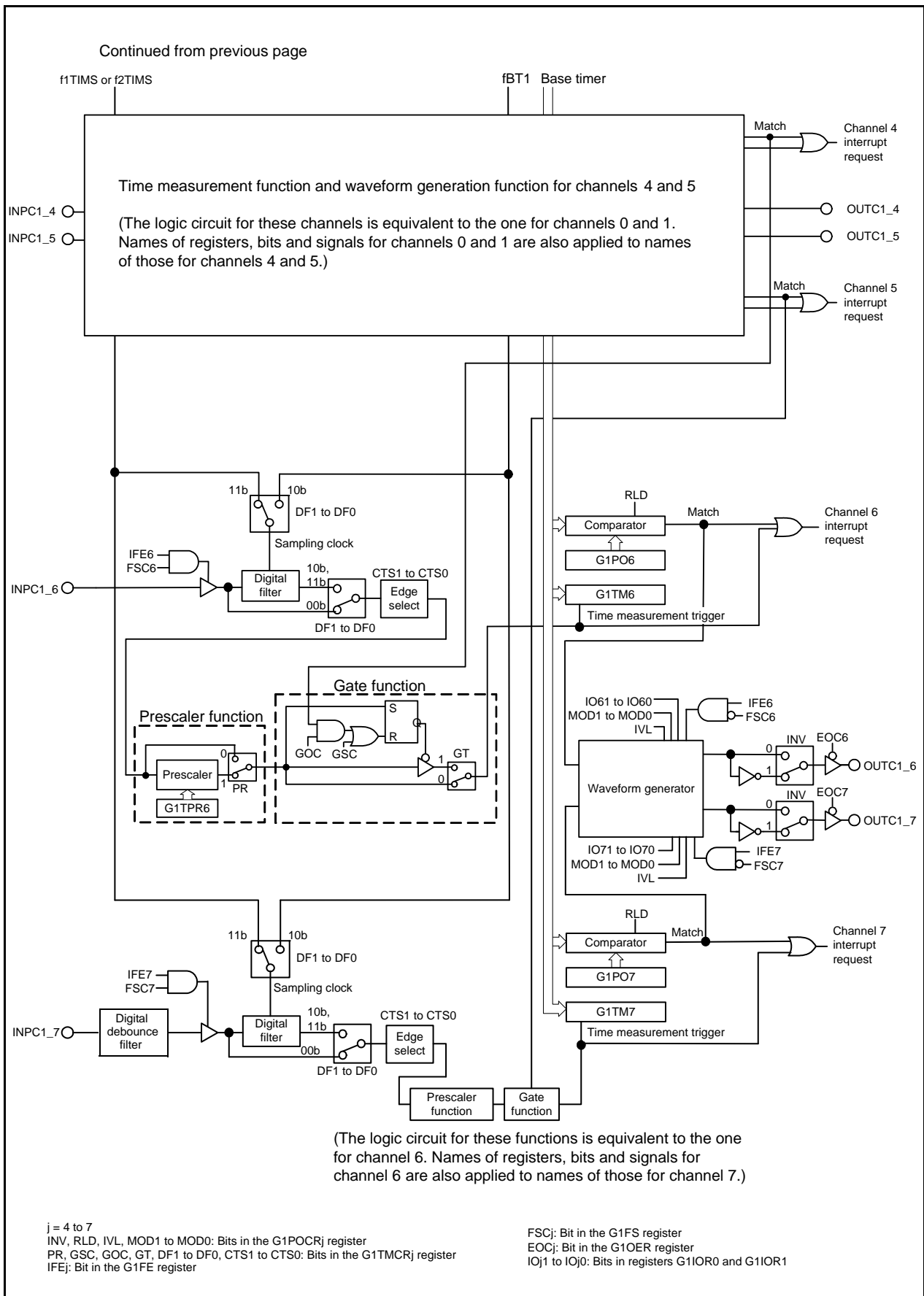


Figure 18.2 IC/OC Block Diagram (2/2)

**Table 18.2 I/O Pins**

Pin Name	I/O	Function
INPC1_0	Input (1)	Input pins for the time measurement function
INPC1_1	Input (1)	
INPC1_2	Input (1)	
INPC1_3	Input (1)	
INPC1_4	Input (1)	
INPC1_5	Input (1)	
INPC1_6	Input (1)	
INPC1_7	Input (1)	
OUTC1_0	Output	Output pins for the waveform generation function
OUTC1_1	Output	
OUTC1_2	Output	
OUTC1_3	Output	
OUTC1_4	Output	
OUTC1_5	Output	
OUTC1_6	Output	
OUTC1_7	Output	
TSUDA	Input (1)	A-phase input of two-phase pulse input signal processing
TSUDB	Input (1)	B-phase input of two-phase pulse input signal processing
INT1	Input (1)	Z-phase input of two-phase pulse input signal processing

## Notes:

1. When pins are used as input, set the port direction bits sharing pins to 0 (input mode).
2. Refer to 18.3.4 "I/O Port Select Function" for details on selecting the INPC1\_j or OUTC1\_j pin (j = 0 to 7).



## 18.2 Registers

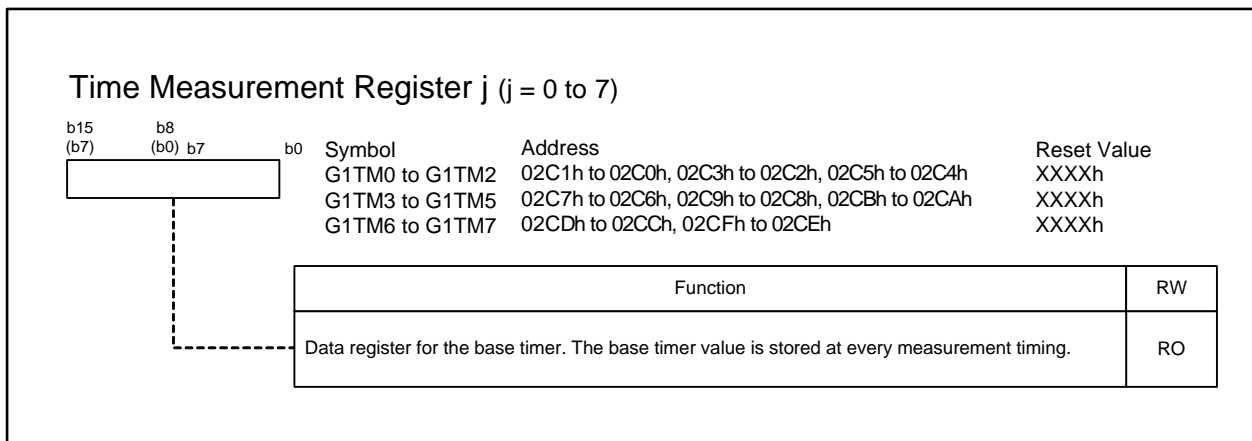
**Table 18.3 Registers (1/2)**

Address	Register Name	Register Symbol	Reset Value
02C0h	Time Measurement Register 0,	G1TM0, G1PO0	XXh
02C1h	Waveform Generation Register 0		XXh
02C2h	Time Measurement Register 1,	G1TM1, G1PO1	XXh
02C3h	Waveform Generation Register 1		XXh
02C4h	Time Measurement Register 2,	G1TM2, G1PO2	XXh
02C5h	Waveform Generation Register 2		XXh
02C6h	Time Measurement Register 3,	G1TM3, G1PO3	XXh
02C7h	Waveform Generation Register 3		XXh
02C8h	Time Measurement Register 4,	G1TM4, G1PO4	XXh
02C9h	Waveform Generation Register 4		XXh
02CAh	Time Measurement Register 5,	G1TM5, G1PO5	XXh
02CBh	Waveform Generation Register 5		XXh
02CCh	Time Measurement Register 6,	G1TM6, G1PO6	XXh
02CDh	Waveform Generation Register 6		XXh
02CEh	Time Measurement Register 7,	G1TM7, G1PO7	XXh
02CFh	Waveform Generation Register 7		XXh
02D0h	Waveform Generation Control Register 0	G1POCR0	0X00 XX00b
02D1h	Waveform Generation Control Register 1	G1POCR1	0X00 XX00b
02D2h	Waveform Generation Control Register 2	G1POCR2	0X00 XX00b
02D3h	Waveform Generation Control Register 3	G1POCR3	0X00 XX00b
02D4h	Waveform Generation Control Register 4	G1POCR4	0X00 XX00b
02D5h	Waveform Generation Control Register 5	G1POCR5	0X00 XX00b
02D6h	Waveform Generation Control Register 6	G1POCR6	0X00 XX00b
02D7h	Waveform Generation Control Register 7	G1POCR7	0X00 XX00b
02D8h	Time Measurement Control Register 0	G1TMCR0	00h
02D9h	Time Measurement Control Register 1	G1TMCR1	00h
02DAh	Time Measurement Control Register 2	G1TMCR2	00h
02DBh	Time Measurement Control Register 3	G1TMCR3	00h
02DCh	Time Measurement Control Register 4	G1TMCR4	00h
02DDh	Time Measurement Control Register 5	G1TMCR5	00h
02DEh	Time Measurement Control Register 6	G1TMCR6	00h
02DFh	Time Measurement Control Register 7	G1TMCR7	00h
02E0h	Base Timer Register	G1BT	XXh
02E1h			XXh
02E2h	Base Timer Control Register 0	G1BCR0	00h
02E3h	Base Timer Control Register 1	G1BCR1	00h
02E4h	Time Measurement Prescaler Register 6	G1TPR6	00h
02E5h	Time Measurement Prescaler Register 7	G1TPR7	00h
02E6h	Function Enable Register	G1FE	00h
02E7h	Function Select Register	G1FS	00h
02E8h	Base Timer Reset Register	G1BTRR	XXh
02E9h			XXh
02EAh	Count Source Divide Register	G1DV	00h
02ECh	Waveform Output Master Enable Register	G1OER	00h
02EEh	Timer S I/O Control Register 0	G1IOR0	00h

**Table 18.4 Registers (2/2)**

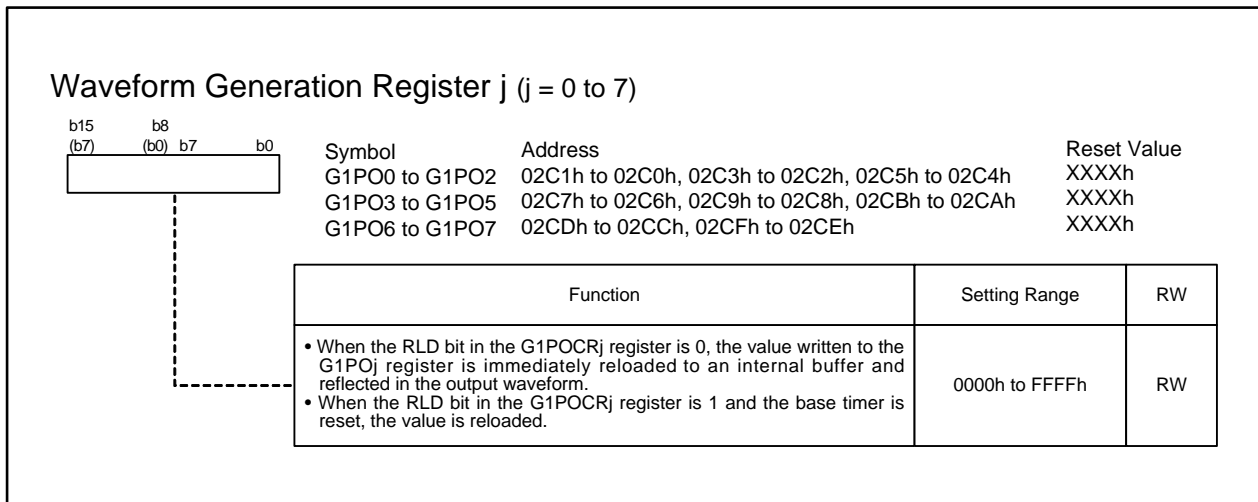
Address	Register Name	Register Symbol	Reset Value
02EFh	Timer S I/O Control Register 1	G1IOR1	00h
02F0h	Interrupt Request Register	G1IR	XXh
02F1h	Interrupt Enable Register 0	G1IE0	00h
02F2h	Interrupt Enable Register 1	G1IE1	00h

### 18.2.1 Time Measurement Register j (G1TMj) (j = 0 to 7)



Read the G1TMj register in 16-bit units.

## 18.2.2 Waveform Generation Register j (G1POj) (j = 0 to 7)



Write to the G1POj register in 16-bit units.

The value written to this register is reflected to the internal buffer when the clock is synchronized with the base timer count source (fBT1). When the waveform generation function is used, the output waveform is changed when this register matches with the base timer. Refer to 18.3.3.1 “Single-Phase Waveform Output Mode”, 18.3.3.2 “Inverted Waveform Output Mode” and 18.3.3.3 “Set/Reset Waveform Output Mode (SR Waveform Output Mode)” for details.

When the base timer value matches the G1PO0 register value while the RST1 bit in the G1BCR1 register is 1, the base timer becomes 0000h. When this function is used, the value of the G1POj register (j = 1 to 7) used to generate output waveforms should be smaller than the value of the G1PO0 register. Do not set the G1PO0 register to 0000h. While the RST1 bit is 1, rewrite the G1PO0 register when the BTS bit in the G1BCR1 register is 0 (base timer reset). Refer to 18.3.1.4 “Base Timer Reset While the Base Timer is Counting” for details.

When the base timer value matches the G1POk register value (k = j - 2), while bits GT and GOC in the G1TMCRj register (j = 6, 7) are both 1 (GT = 1: gate function used), the gate function is released. When this function is used, the value set in the G1POk register should be smaller than the maximum value of the base timer.

When the base timer reset is used with the G1BTRR register, set the register values as follows:

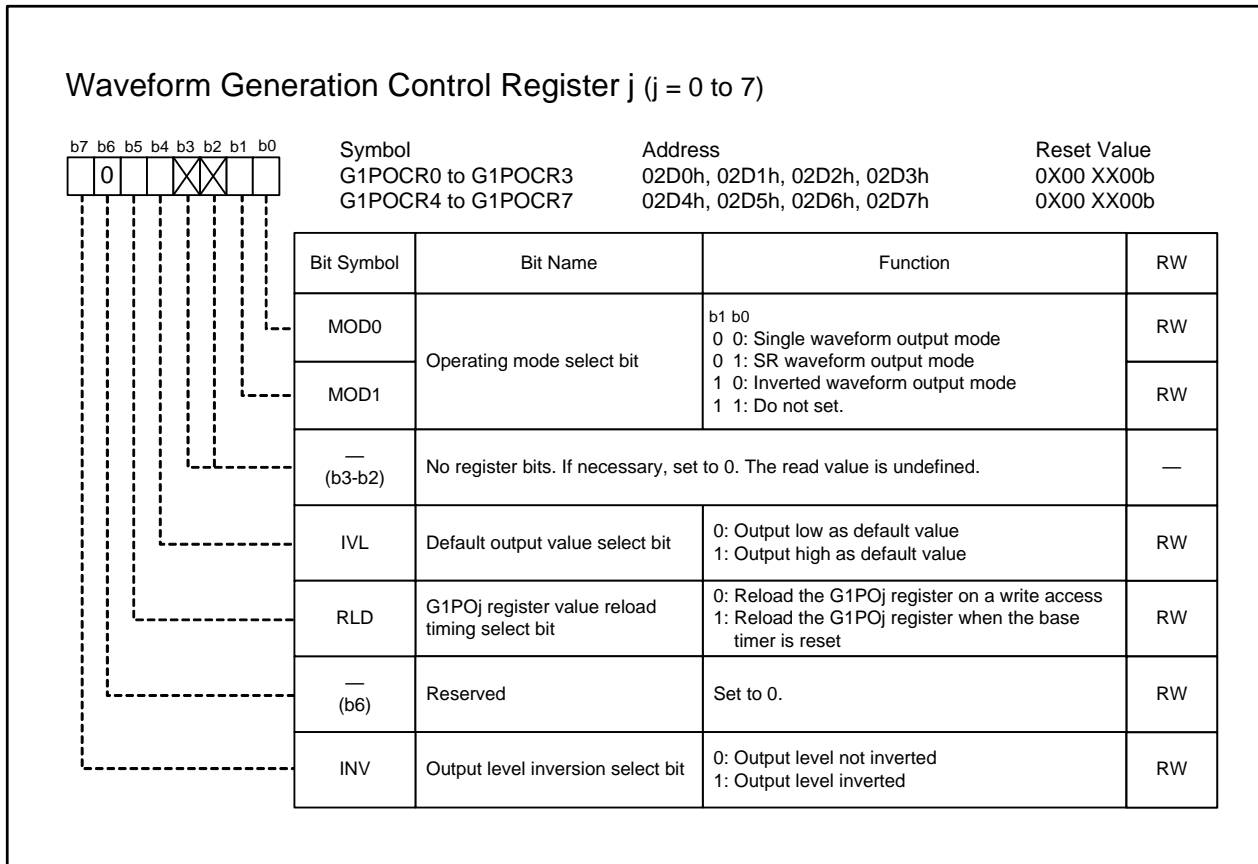
$$G1POk \text{ value} < G1BTTR \text{ value}$$

When the base timer reset is used with the G1PO0 register, set the register values as follows:

$$G1POk \text{ value} < G1PO0 \text{ value}$$

Refer to 18.3.2.1 “Gate Function (Channel 6 and 7)” for details.

### 18.2.3 Waveform Generation Control Register j (G1POCRj) (j = 0 to 7)



Rewrite the G1POCRj register when the BTS bit in the G1BCR1 is 0 (base timer reset), the FSCj bit in the G1FS register is 0 (waveform generation function selected), and the IFEj bit in the G1FE register is 0 (channel j function disabled). When the G1POCRj register is rewritten, set the BTS bit to 1 after one or more fBT1 cycles.

#### MOD1 and MOD0 (Operating mode select bit) (b1-b0)

To select SR waveform output mode, set bits MOD1 and MOD0 of an even channel (channel j (j = 0, 2, 4, or 6)) and bits MOD1 and MOD0 of the next odd channel (channel j + 1) both to 01b. The waveform is output from the OUT1\_j pin of an even channel. In SR waveform output mode, set EOCj + 1 bit in the G1OER register to 1 (output disabled).

#### IVL (Output default select bit) (b4)

When a value is written to the IVL bit, the FSCj bit (j = 0 to 7) in the G1FS register is set to 0 (waveform generation function selected), and the IFEj bit in the G1FE register is set to 1 (channel j function enabled), the set level is output.

**RLD (G1POj register value reload timing select bit) (b5)**

For SR waveform output mode, set both even channels (channel j (j = 0, 2, 4, or 6)) and odd channels (channel j+1).

When writing a value to the G1POj register (j = 0 to 7) while the BTS bit is 0 (base timer reset) and the RLD bit is 1 (reload the G1POj register when the base timer is reset), the written value will not be reloaded to a buffer.

Therefore, when the BTS bit is 0, set the RLD bit to 0 (reload on a write access), write a value to the G1POj register, and then set the RLD bit to 1 after one or more fBT1 cycles.

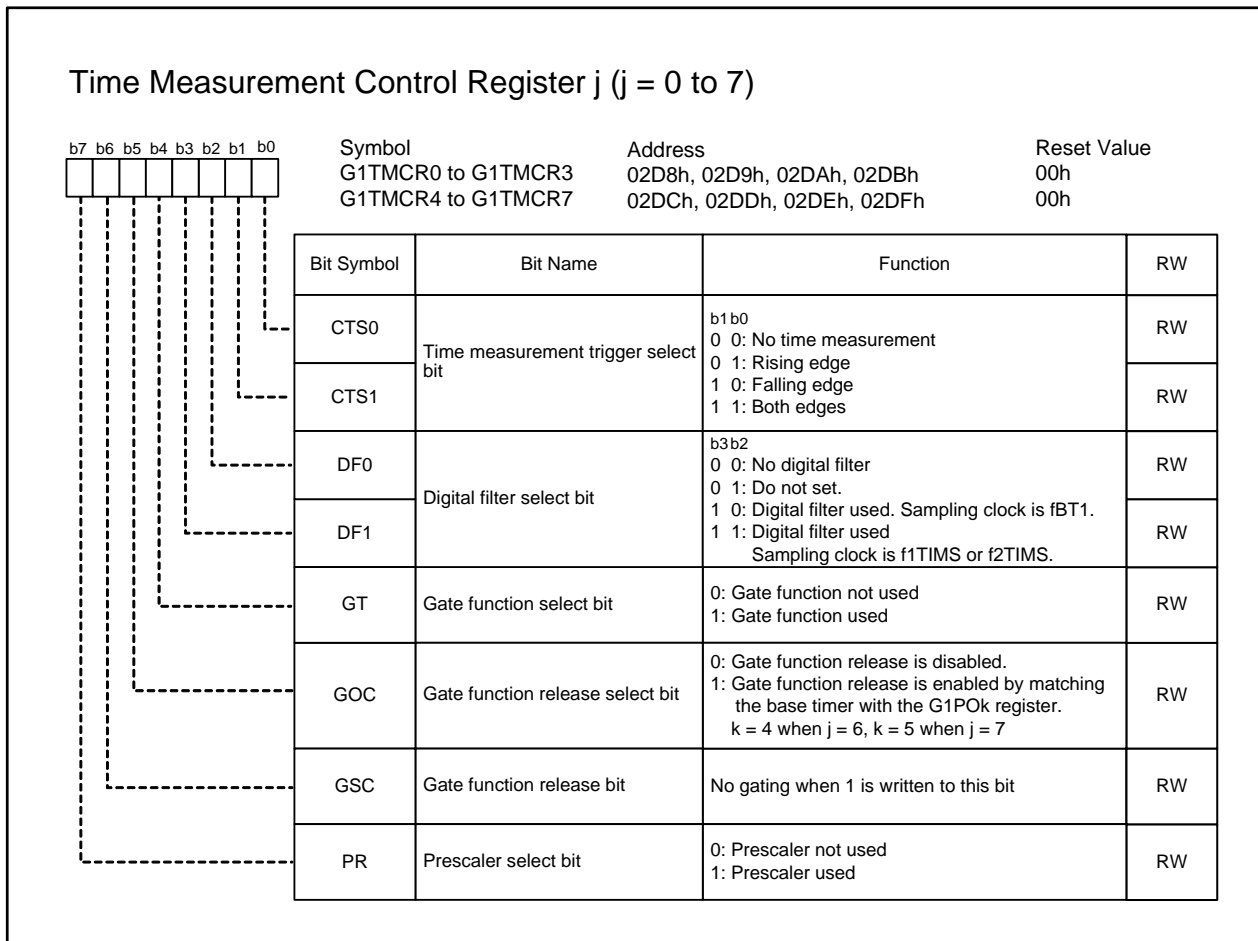
When the RLD bit is set to 1, the value will not be reloaded at the following timings:

- When the base timer counter changes from FFFFh to 0000h immediately after writing FFFFh to the base timer while incrementing in increment mode or increment/decrement mode.
- When the base timer counter changes from 0000h to FFFFh immediately after writing 0000h to the base timer while decrementing in increment/decrement mode.

**INV (Output level inversion select bit) (b7)**

The output level inversion function is located at the final step of waveform generation circuit. When the INV bit is set to 1 (output level inverted), the default output value becomes high if the IVL bit is set to 0, and the default output value becomes low if the IVL bit is set to 1.

## 18.2.4 Time Measurement Control Register j (G1TMCRj) (j = 0 to 7)



When writing to registers G1TMCR6 and G1TMCR7, use the MOV instruction. To release the gate during a write access, set the GSC bit to 1; otherwise, set it to 0.

### CTS1 and CTS0 (Time measurement trigger select bit) (b1-b0)

Rewrite these bits when the BTS bit in the G1BCR1 register is 0 (base timer reset).

### DF1 and DF0 (Digital filter select bit) (b3-b2)

Rewrite these bits when the BTS bit is 0.

When the PCLK0 bit in the PCLKR register is 0 while bits DF1 and DF0 are 11b, f2TIMS is selected as the sampling clock, and when the PCLK0 bit is 1, f1TIMS is selected as the sampling clock.

The two-phase pulse clock does not become a sampling clock of digital filter even if bits BCK1 and BCK0 are 10b (two-phase pulse clock).

### GT (Gate function select bit) (b4)

The GT bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.

The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

**GOC (Gate function release select bit) (b5)**

The GOC bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.

The GOC bit is enabled only when the GT bit is 1.

Refer to 18.2.2 “Waveform Generation Register j (G1POj) (j = 0 to 7)” for details on the G1POk register (k = 4 when j = 6; k = 5 when j = 7).

The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

**GSC (Gate function release bit) (b6)**

The GSC bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.

The GSC bit is enabled only when the GT bit is 1.

Set this bit to 1 when the gate function is released; otherwise set it to 0.

The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

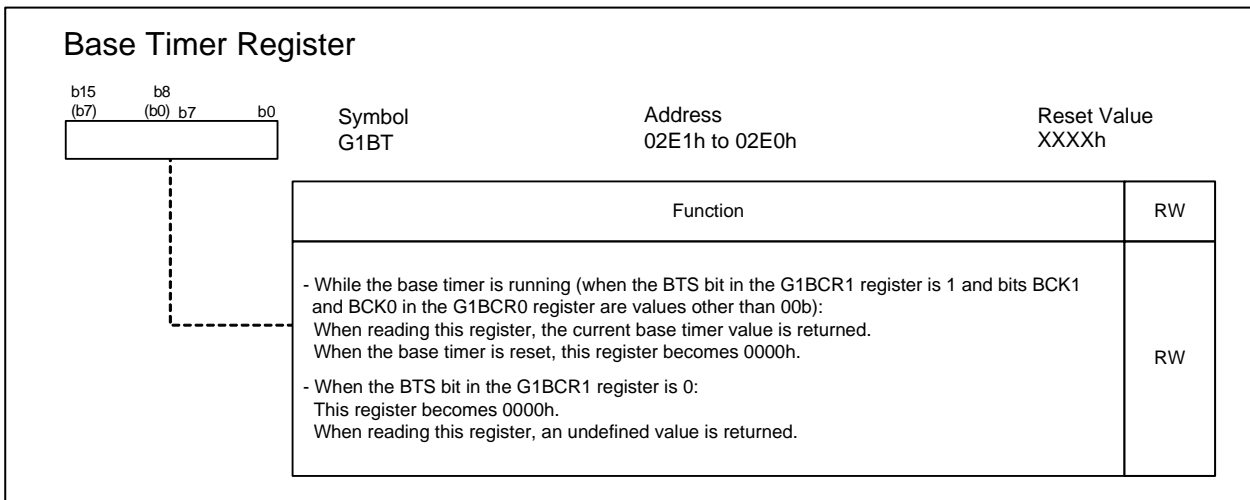
**PR (Prescaler select bit) (b7)**

Rewrite the PR bit when bits BCK1 and BCK0 in the G1BCR0 register are 00b (clock stops).

The PR bit is only available in registers G1TMCR6 and G1TMCR7. Set bits 7 to 4 in registers G1MCR0 to G1TMCR5 to 0000b.



### 18.2.5 Base Timer Register (G1BT)



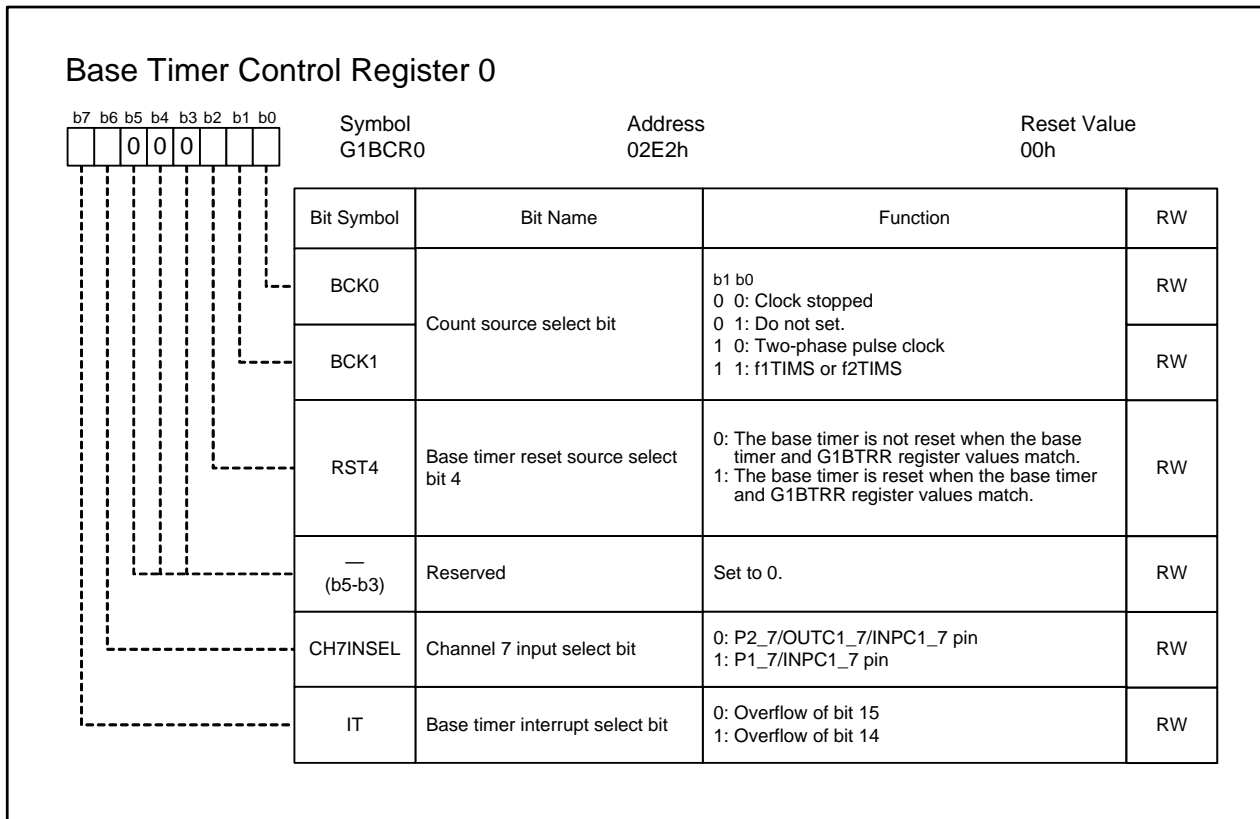
Read the G1BT register in 16-bit units. Do not write to this register.

While the base timer is counting, the base timer value is stored to this register, and synchronized with the base timer count source (fBT1).

The base timer stops counting only when bits BCK1 and BCK0 in the G1BCR0 register are 00b (clock stopped). When bits BCK1 and BCK0 are not 00b, the base timer operates.

When the BTS bit in the G1BCR1 register is 0 (base timer reset), the G1BT register is held in the reset state (0000h). The counter stays in this state without counting. When the BTS bit is set to 1, the state is released and the base timer starts counting.

## 18.2.6 Base Timer Control Register 0 (G1BCR0)



Rewrite the G1BCR0 register when the BTS bit in the G1BCR1 register is 0 (base timer reset).

### BCK1 and BCK0 (Count source select bit) (b1-b0)

After rewriting bits BCK1 and BCK0 from 00b (clock stopped) to another value, before rewriting these bits to another value, first set them to 00b, wait four or more cycles of the previous count source, and then rewrite the bits.

The two-phase pulse clock (10b) can be used only when bits UD1 and UD0 in the G1BCR1 register are 10b (two-phase pulse signal processing). Do not set bits BCK1 and BCK0 to 10b with other count operations.

When bits BCK1 and BCK0 are 11b and the PCLK0 bit in the PCLKR register is 0, f2TIMS is selected. When the PCLK0 bit is 1, f1TIMS is selected. Change the PCLK0 bit when bits BCK1 and BCK0 are 00b.

### RST4 (Base timer reset source select bit 4) (b2)

When the RST4 bit is 1, set the RST1 bit in the G1BCR1 register to 0.

### IT (Base timer interrupt select bit) (b7)

While the IT bit is 0 (overflow of bit 15), when incrementing, if b15 of the base timer becomes 0 from 1 (i.e. the base timer value becomes 0000h from FFFFh) during counting, the base timer overflows. When decrementing, the base timer overflows if b15 of the base timer becomes 1 from 0 (i.e. 7FFFh from 8000h).

While the IT bit is 1 (overflow of bit 14), when incrementing, if b14 of the base timer becomes 0 from 1 during counting, the base timer overflows. When decrementing, the base timer overflows if b14 of the base timer becomes 1 from 0.

When the base timer overflows, the IR bit in the BTIC register becomes 1 (IC/OC base timer interrupt requested).

## 18.2.7 Base Timer Control Register 1 (G1BCR1)

Base Timer Control Register 1											
b7	b6	b5	b4	b3	b2	b1	b0	Symbol G1BCR1	Address 02E3h	Reset Value 00h	
0				0			0				
								Bit Symbol	Bit Name	Function	RW
								— (b0)	Reserved	Set to 0.	RW
								RST1	Base timer reset source select bit 1	0: The base timer is not reset when the base timer and G1PO0 register values match. 1: The base timer is reset when the base timer and G1PO0 register values match.	RW
								RST2	Base timer reset source select bit 2	0: The base timer is not reset when low is input to the INT1 pin. 1: The base timer is reset when low is input to the INT1 pin.	RW
								— (b3)	Reserved	Set to 0.	RW
								BTS	Base timer start bit	0: Base timer reset 1: Base timer starts counting	RW
								UD0	Increment/decrement control bit	b6 b5 0 0: Increment 0 1: Increment/decrement 1 0: Two-phase pulse signal processing 1 1: Do not set.	RW
							UD1				
								— (b7)	Reserved	Set to 0.	RW

### RST1 (Base timer reset source select bit 1) (b1)

To rewrite the RST1 bit, rewrite it while the BTS bit is 0 (base timer reset) and then change the BTS bit to 1 (base timer starts counting).

When the base timer value matches the G1PO0 register value while the RST1 bit is 1, the base timer is reset after two fBT1 cycles. Refer to 18.3.1.4 “Base Timer Reset While the Base Timer is Counting” for details. When the RST1 bit is 1, set the RST4 bit in the G1BCR0 register to 0 (the base timer is not reset when the base timer and G1BTRR register values match).

### RST2 (Base timer reset source select bit 2) (b2)

To rewrite the RST2 bit, rewrite it while the BTS bit is 0 and then rewrite the BTS bit to 1.

### BTS (Base timer start bit) (b4)

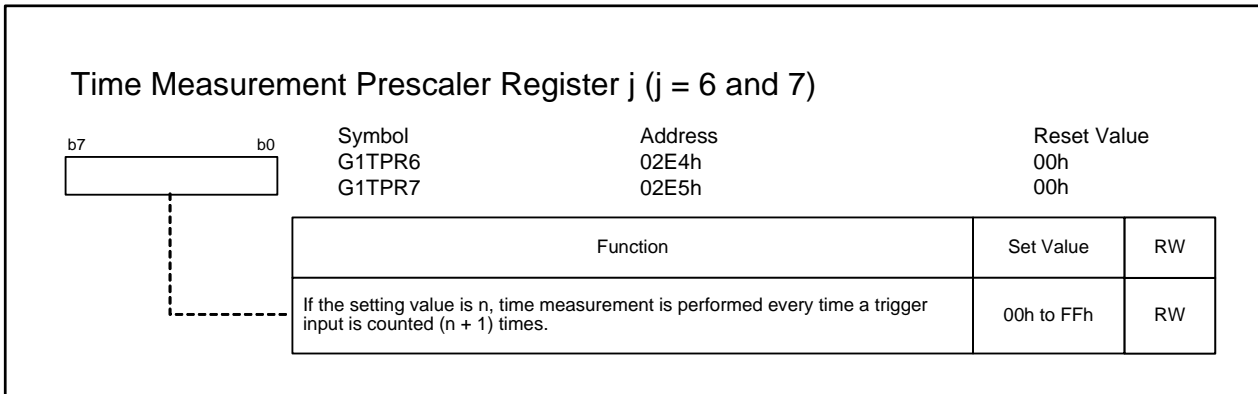
The value written to this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

### UD1 and UD0 (Increment/decrement control bit) (b6-b5)

To rewrite bits UD1 and UD0, rewrite them while the BTS bit is 0 and then rewrite the BTS bit to 1.

When single-waveform output mode or SR waveform output mode is selected, set bits UD1 and UD0 to 00b (increment). When inverted waveform output mode is selected, set these bits to 00b (increment) or 01b (increment/decrement).

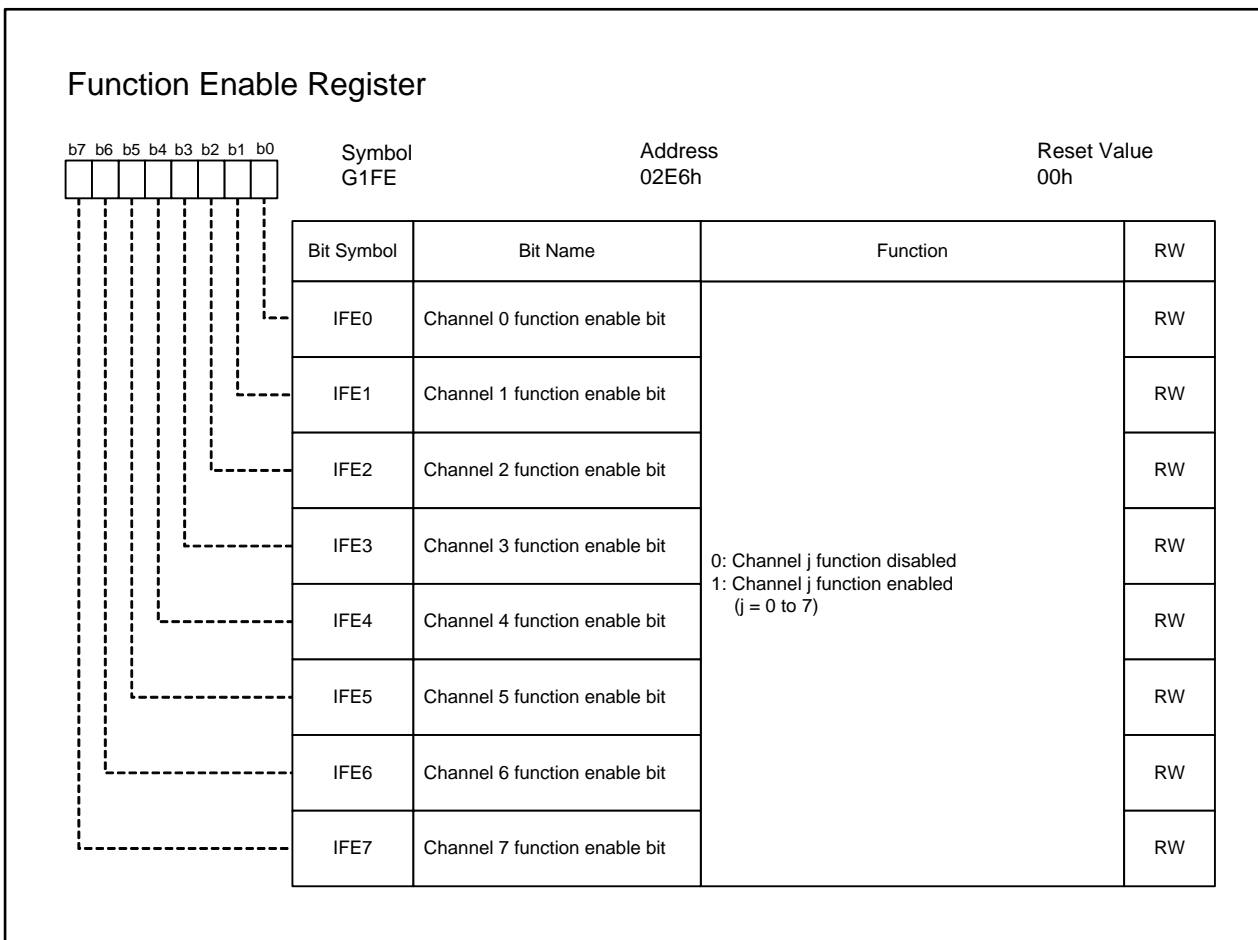
### 18.2.8 Time Measurement Prescaler Register j (G1TPRj) (j = 6 and 7)



The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

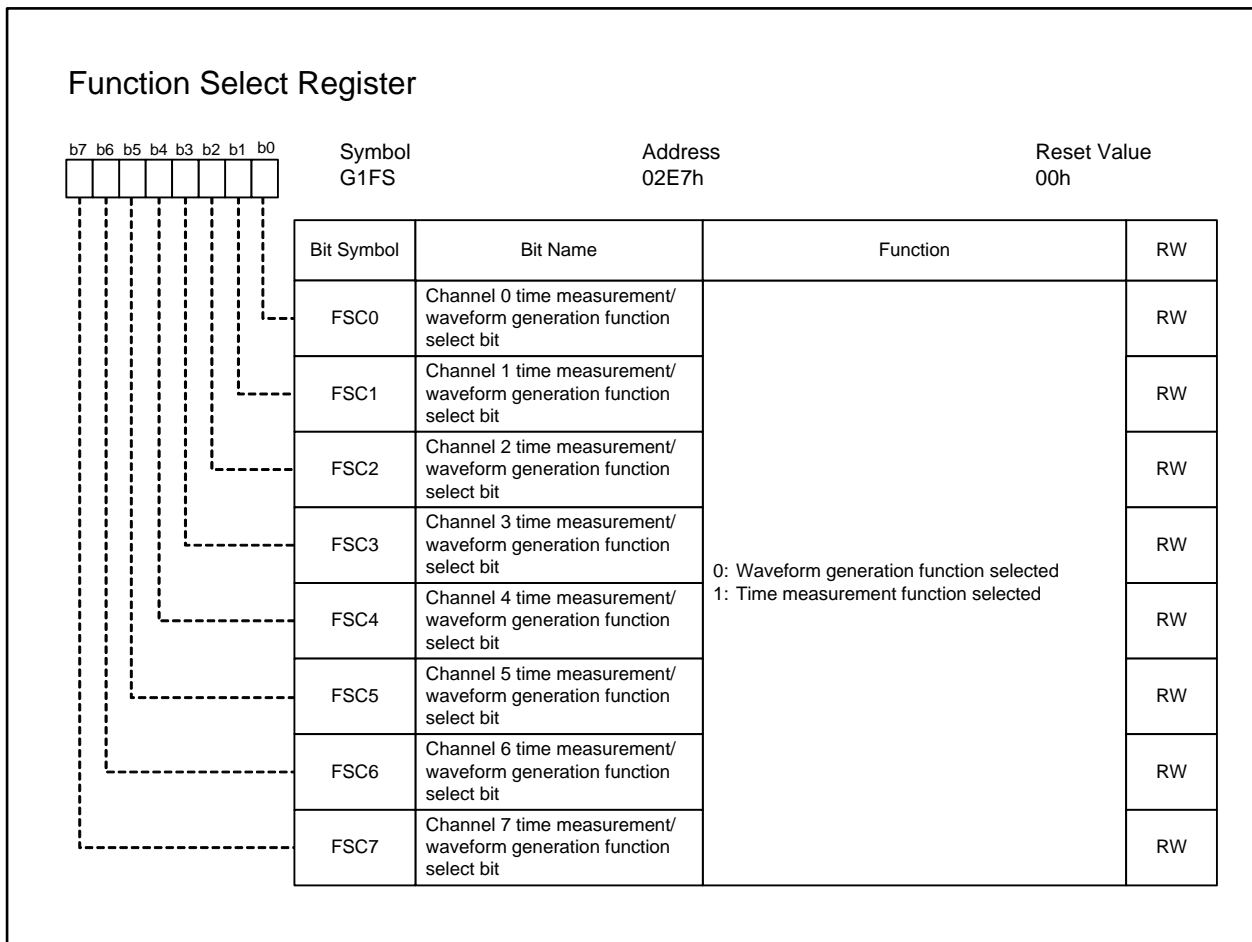
After rewriting the PR bit in the G1TMCRj register to 1 (prescaler function used) from 0 (prescaler function not used), the first prescaler cycle may remain as n instead of being counted as (n + 1). In the subsequent prescaler cycles, the setting value n becomes (n + 1).

### 18.2.9 Function Enable Register (G1FE)



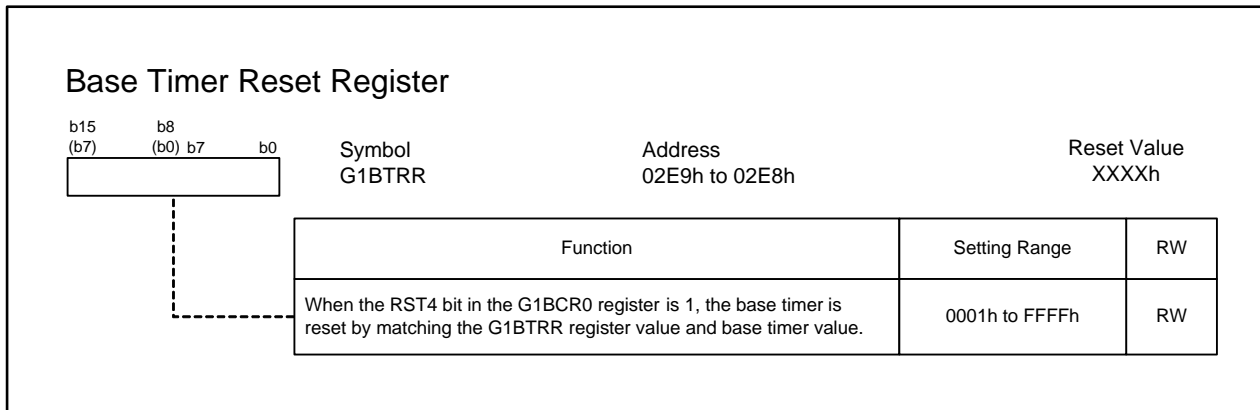
The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1). When the channel j (j = 0 to 7) function is disabled, the corresponding pins become programmable I/O ports.

### 18.2.10 Function Select Register (G1FS)



Rewrite the G1FS register when the BTS bit in the G1BCR1 register is 0 (base timer reset).

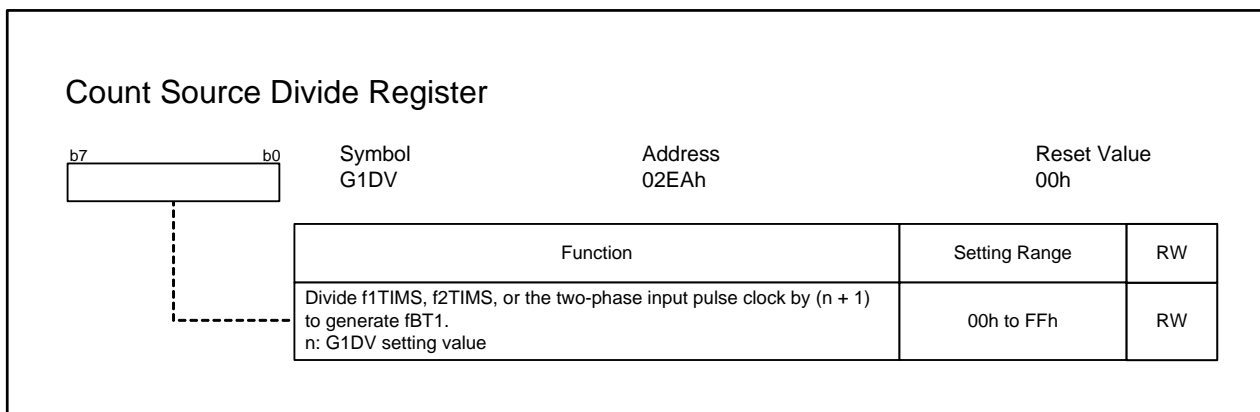
### 18.2.11 Base Timer Reset Register (G1BTRR)



Write to the G1BTRR register in 16-bit units. The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

While the RST4 bit in the G1BCR0 register is 1, rewrite the G1BTRR register when the BTS bit in the G1BCR1 register is 0 (base timer reset).

### 18.2.12 Count Source Divide Register (G1DV)



Rewrite the G1DV register when bits BCK1 and BCK0 in the G1BCR0 register are 00b (clock stopped).

### 18.2.13 Waveform Output Master Enable Register (G1OER)

Waveform Output Master Enable Register			
	Symbol G1OER	Address 02ECh	Reset Value 00h
Bit Symbol	Bit Name	Function	RW
EOC0	OUTC1_0 output disable bit	0: Output enabled 1: Output disabled (OUTC1_0 pin is used as a programmable I/O port)	RW
EOC1	OUTC1_1 output disable bit	0: Output enabled 1: Output disabled (OUTC1_1 pin is used as a programmable I/O port)	RW
EOC2	OUTC1_2 output disable bit	0: Output enabled 1: Output disabled (OUTC1_2 pin is used as a programmable I/O port)	RW
EOC3	OUTC1_3 output disable bit	0: Output enabled 1: Output disabled (OUTC1_3 pin is used as a programmable I/O port)	RW
EOC4	OUTC1_4 output disable bit	0: Output enabled 1: Output disabled (OUTC1_4 pin is used as a programmable I/O port)	RW
EOC5	OUTC1_5 output disable bit	0: Output enabled 1: Output disabled (OUTC1_5 pin is used as a programmable I/O port)	RW
EOC6	OUTC1_6 output disable bit	0: Output enabled 1: Output disabled (OUTC1_6 pin is used as a programmable I/O port)	RW
EOC7	OUTC1_7 output disable bit	0: Output enabled 1: Output disabled (OUTC1_7 pin is used as a programmable I/O port)	RW

The EOC<sub>j</sub> bit ( $j = 0$  to  $7$ ) is enabled only when the FSC<sub>j</sub> bit in the G1FS register is 0 (waveform generation function is selected) and the IFE<sub>j</sub> bit in the G1FE register is 1 (channel  $j$  function enabled). When an odd channel is selected in SR waveform output mode or the FSC<sub>j</sub> bit in the G1FS register is 1 (time measurement function is selected), set the EOC<sub>j</sub> bit to 1. The value written to the EOC<sub>j</sub> bit is immediately reflected in output waveforms, independently of fBT1.

### 18.2.14 Timer S I/O Control Register 0 (G1IOR0)

Timer S I/O Control Register 0			
Bit	Symbol	Address	Reset Value
b7		02EEh	00h
b6			
b5			
b4			
b3			
b2			
b1			
b0			
IO00	OUTC1_0 output control bit	b1 b0 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR0 register. 0 1: Outputs low by compare match with the G1PO0 register. 1 0: Outputs high by compare match with the G1PO0 register. 1 1: Do not set.	RW
IO01			RW
IO10	OUTC1_1 output control bit	b3 b2 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR1 register. 0 1: Outputs low by compare match with the G1PO1 register. 1 0: Outputs high by compare match with the G1PO1 register. 1 1: Do not set.	RW
IO11			RW
IO20	OUTC1_2 output control bit	b5 b4 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR2 register. 0 1: Outputs low by compare match with the G1PO2 register. 1 0: Outputs high by compare match with the G1PO2 register. 1 1: Do not set.	RW
IO21			RW
IO30	OUTC1_3 output control bit	b7 b6 0 0: Outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCR3 register. 0 1: Outputs low by compare match with the G1PO3 register. 1 0: Outputs high by compare match with the G1PO3 register. 1 1: Do not set.	RW
IO31			RW

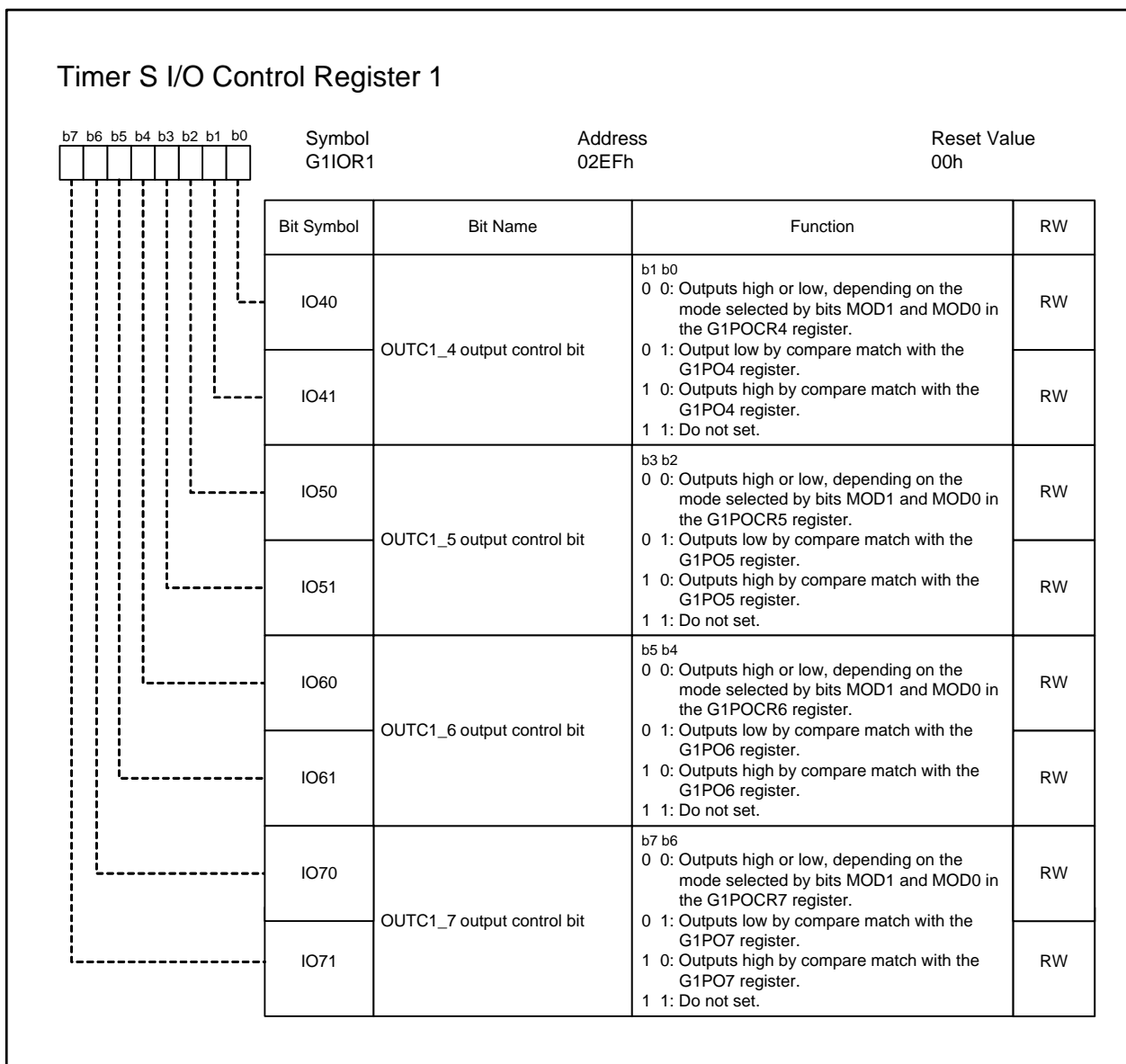
The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

Set the corresponding output control bits IOj1 and IOj0 to 00b for the input channels selected by setting the FSCj bit (j = 0 to 3) in the G1FS register to 1 (time measurement function is selected).

In SR waveform output mode, set bits IOj1 and IOj0 to 00b for both odd and even channels.



### 18.2.15 Timer S I/O Control Register 1 (G1IOR1)

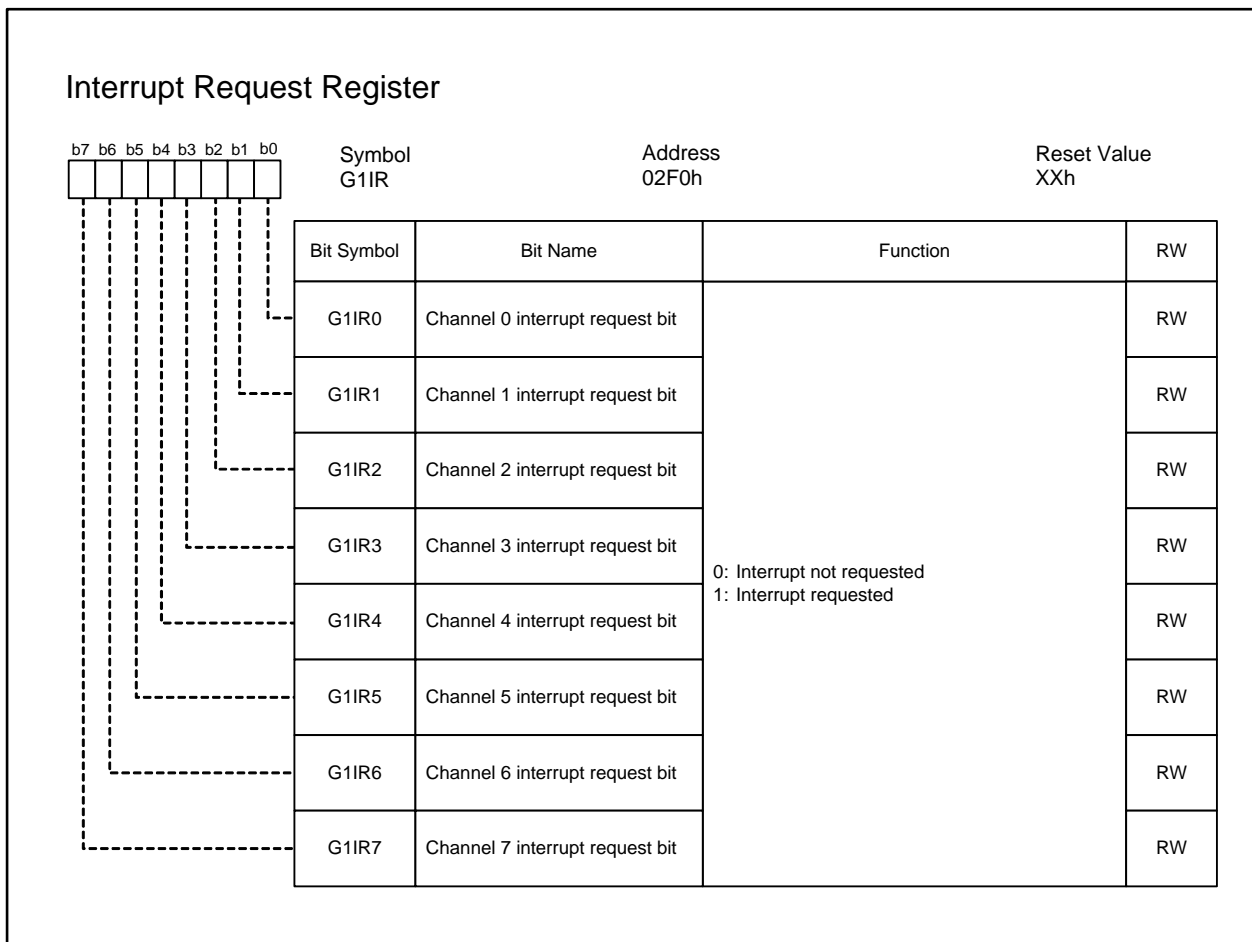


The value written to this register is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1).

Set the corresponding output control bits IOj1 and IOj0 to 00b for the input channels determined by setting the FSCj bit (j = 4 to 7) in the G1FS register to 1 (time measurement function is selected).

In SR waveform output mode, set bits IOj1 and IOj0 to 00b for both odd and even channels.

### 18.2.16 Interrupt Request Register (G1IR)

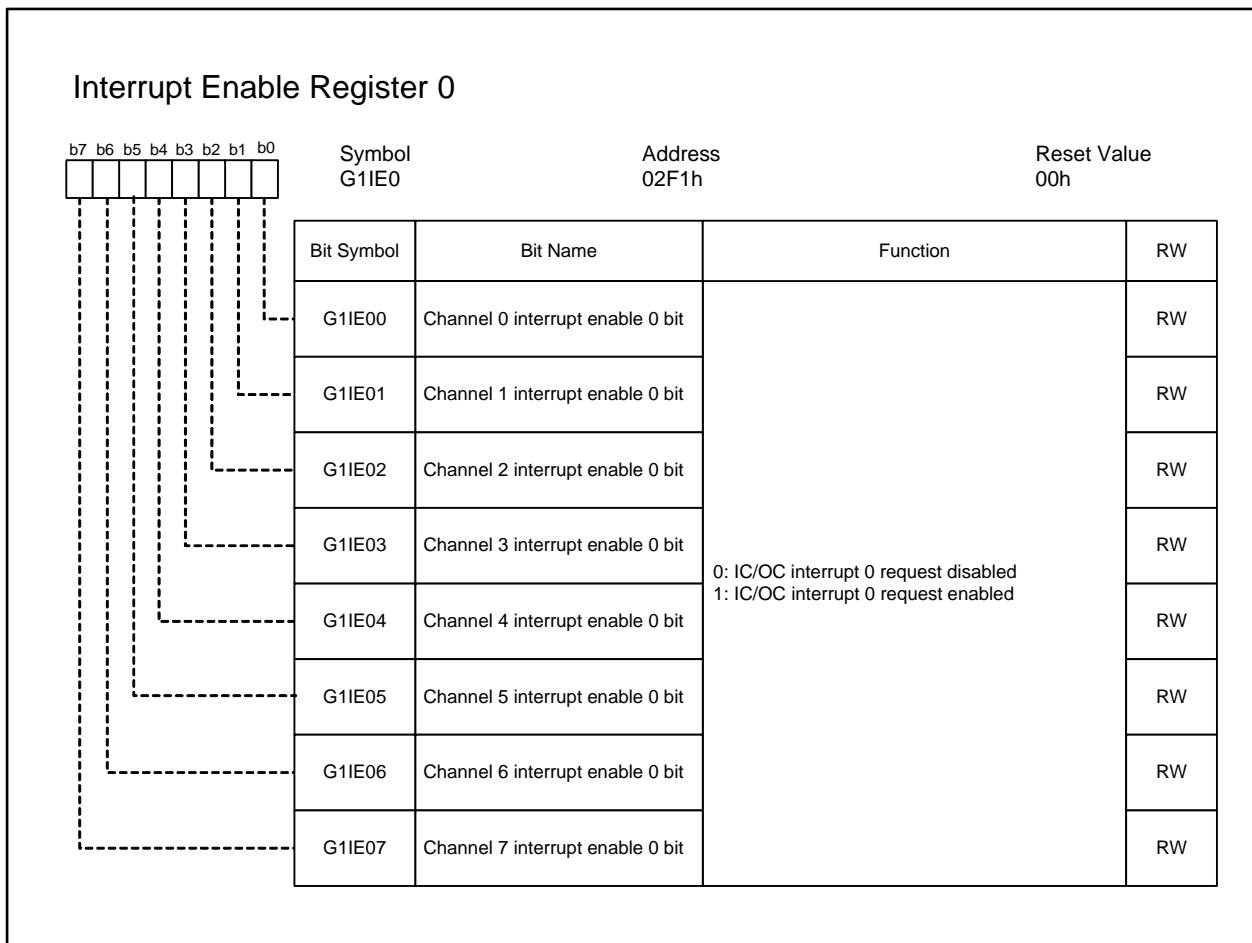


The G1IR<sub>j</sub> bit does not become 0 (interrupt not requested) automatically when an interrupt is received (j = 0 to 7).

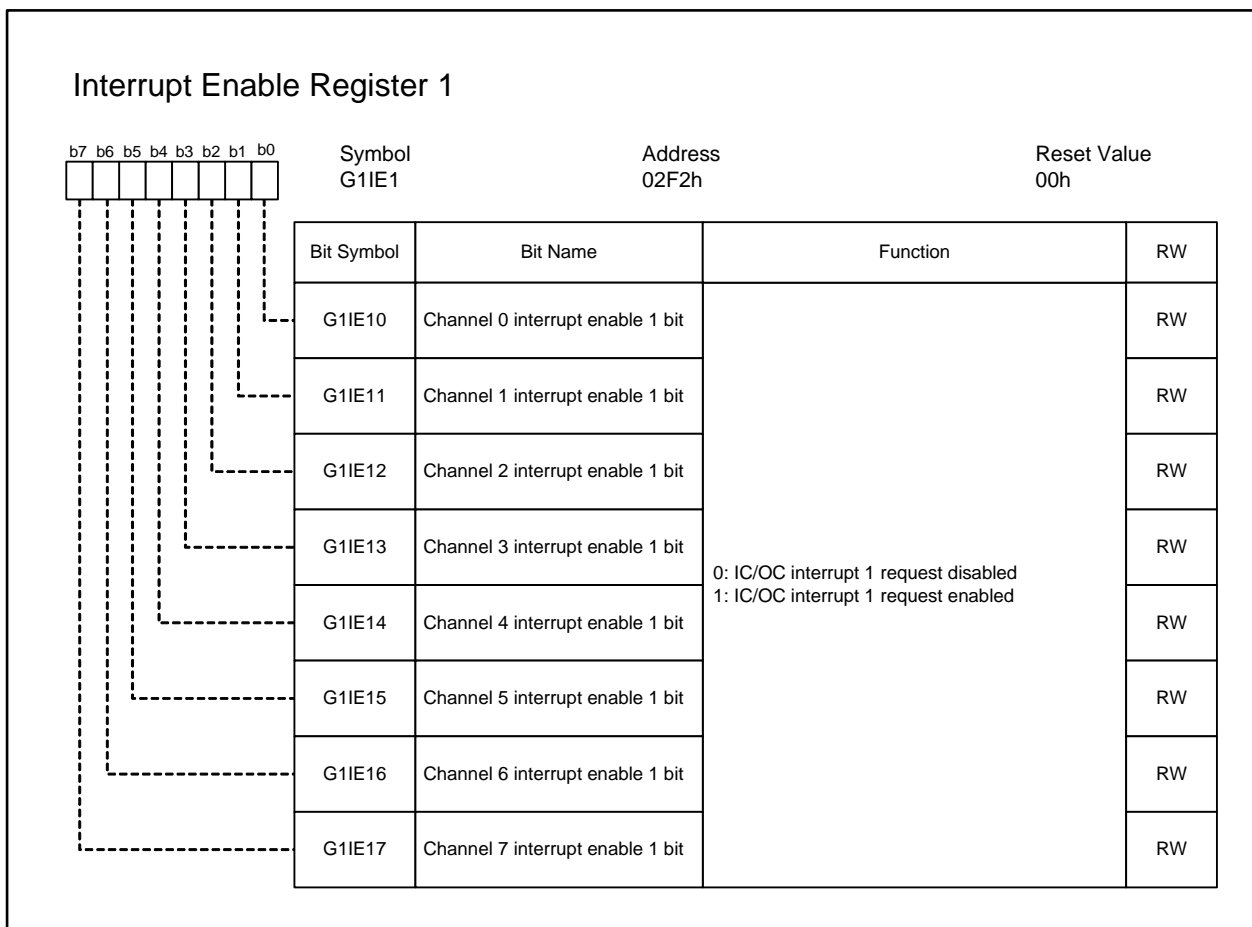
To set the bit to 0, wait one or more fBT1 cycles after the G1IR<sub>j</sub> bit becomes 1 (interrupt requested), and perform the operation shown in 18.5.2 “Changing the G1IR Register”.

The value written to these bits is reflected to the internal circuit in synchronization with the CPU clock.

### 18.2.17 Interrupt Enable Register 0 (G1IE0)



### 18.2.18 Interrupt Enable Register 1 (G1IE1)



## 18.3 Operations

### 18.3.1 Base Timer

The base timer is a free-running counter which counts an internally generated count source.

Table 18.5 lists the specifications of the base timer, Figure 18.3 shows the block diagram of the base timer, Table 18.6 lists the base timer associated registers and their settings, Figure 18.4 shows an operation example with incrementing, Figure 18.5 shows an operation example with incrementing/decrementing, and Figure 18.7 shows an operation example with two-phase pulse signal processing.

**Table 18.5 Base Timer Specifications**

Item	Specification
Count source (fBT1)	f1TIMS or f2TIMS divided by (n + 1), two-phase pulse clock divided by (n + 1) n is a G1DV register setting value from 0 to 255. However, when n is 0, there is no division.
Count operations	<ul style="list-style-type: none"> <li>• Increment</li> <li>• Increment/decrement</li> <li>• Two-phase pulse signal processing</li> </ul>
Count start condition	Set the BTS bit in the G1BCR1 register to 1 (base timer starts counting).
Count stop condition	Set the BTS bit in the G1BCR1 register to 0 (base timer reset).
Base timer reset conditions	<ul style="list-style-type: none"> <li>• The base timer value matches the G1BTRR register value.</li> <li>• The base timer value matches the G1PO0 register value.</li> <li>• A low signal is input to the <math>\overline{\text{INT1}}</math> external interrupt pin.</li> <li>• The BTS bit in the G1BCR1 register is 0 (base timer reset).</li> </ul>
Base timer reset value	0000h
Interrupt requests	<ul style="list-style-type: none"> <li>• Bit 14 or bit 15 in the G1BT register overflows.</li> <li>• The base timer value matches the G1BTRR register value.</li> </ul>
Read from base timer	<ul style="list-style-type: none"> <li>• The count value is returned when reading the G1BT register while the base timer is counting.</li> <li>• An undefined value is returned when reading the G1BT register while the base timer is being reset and the BTS bit is 0.</li> </ul>

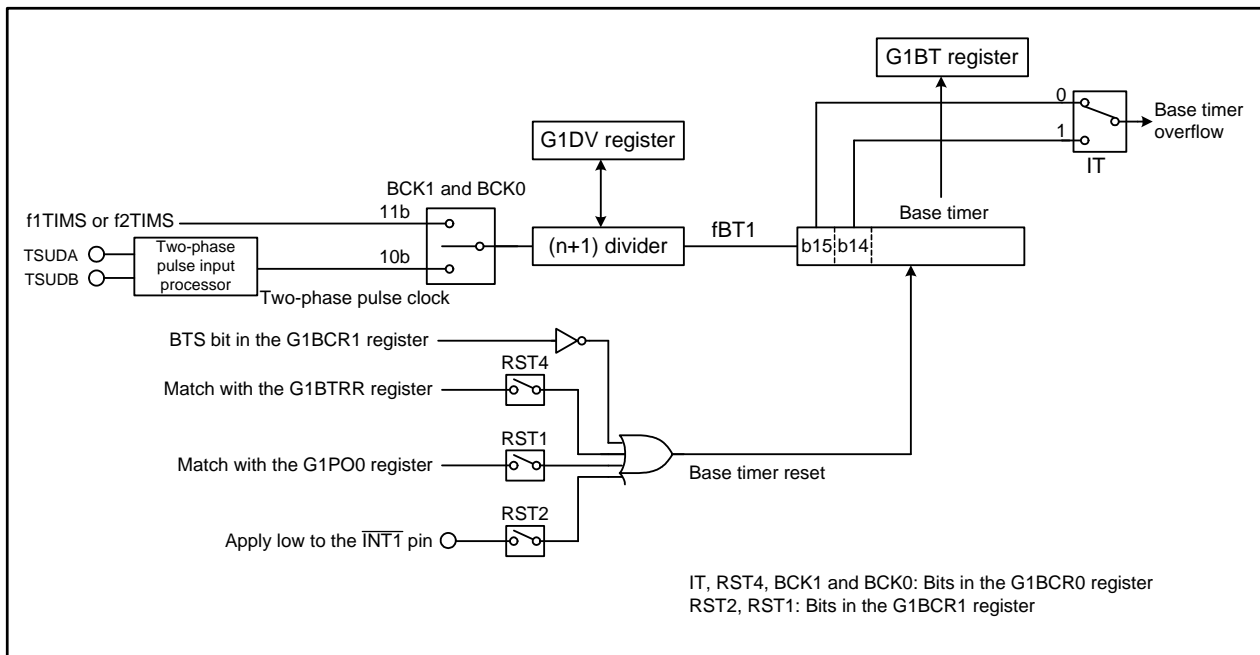


Figure 18.3 Base Timer Block Diagram

Table 18.6 Base Timer Associated Register Settings (1)

Register	Bit	Function and Setting Value		
		Base timer reset not used	Base timer reset by matching with the G1BTRR register	Base timer reset by matching with the G1PO0 register
G1BCR0	BCK1 and BCK0	Select a count source.	Select a count source.	Select a count source.
	RST4	Set to 0.	Set to 1.	Set to 0.
	IT	Select a timing of IC/OC base timer interrupt request.	Select a timing of IC/OC base timer interrupt request.	Select a timing of IC/OC base timer interrupt request.
G1BCR1	RST1	Set to 0.	Set to 0.	Set to 1.
	RST2	Select whether the $\overline{\text{INT1}}$ pin is used for base timer reset.	Select whether the $\overline{\text{INT1}}$ pin is used for base timer reset.	Select whether the $\overline{\text{INT1}}$ pin is used for base timer reset.
	BTS	Set to 1 to start the base timer count. Set to 0 to reset the base timer count.	Set to 1 to start the base timer count. Set to 0 to reset the base timer count.	Set to 1 to start the base timer count. Set to 0 to reset the base timer count.
	UD1 and UD0	Select a count operation.	Select a count operation.	Select a count operation.
G1BT	—	Base timer value can be read.	Base timer value can be read.	Base timer value can be read.
G1DV	—	Set a divide ratio of the count source.	Set a divide ratio of the count source.	Set a divide ratio of the count source.
G1BTRR	—	— (Do not use)	Set a base timer reset timing	— (Do not use)
G1POCR0	MOD1 and MOD0	— (Do not use for the base timer)		Set to 00b
G1PO0	—	— (Do not use for the base timer)		Set a base timer reset timing
G1FS	FSC0	— (Do not use for the base timer)		Set to 0.
G1FE	IFE0	— (Do not use for the base timer)		Set to 1.
G1IOR0	IO01 and IO00	— (Do not use for the base timer)		Set to 00b.

Note:

1. This table does not describe a procedure.

### 18.3.1.1 Increment

The counter starts incrementing from 0000h to FFFFh, then returns back to 0000h, and continues to increment.

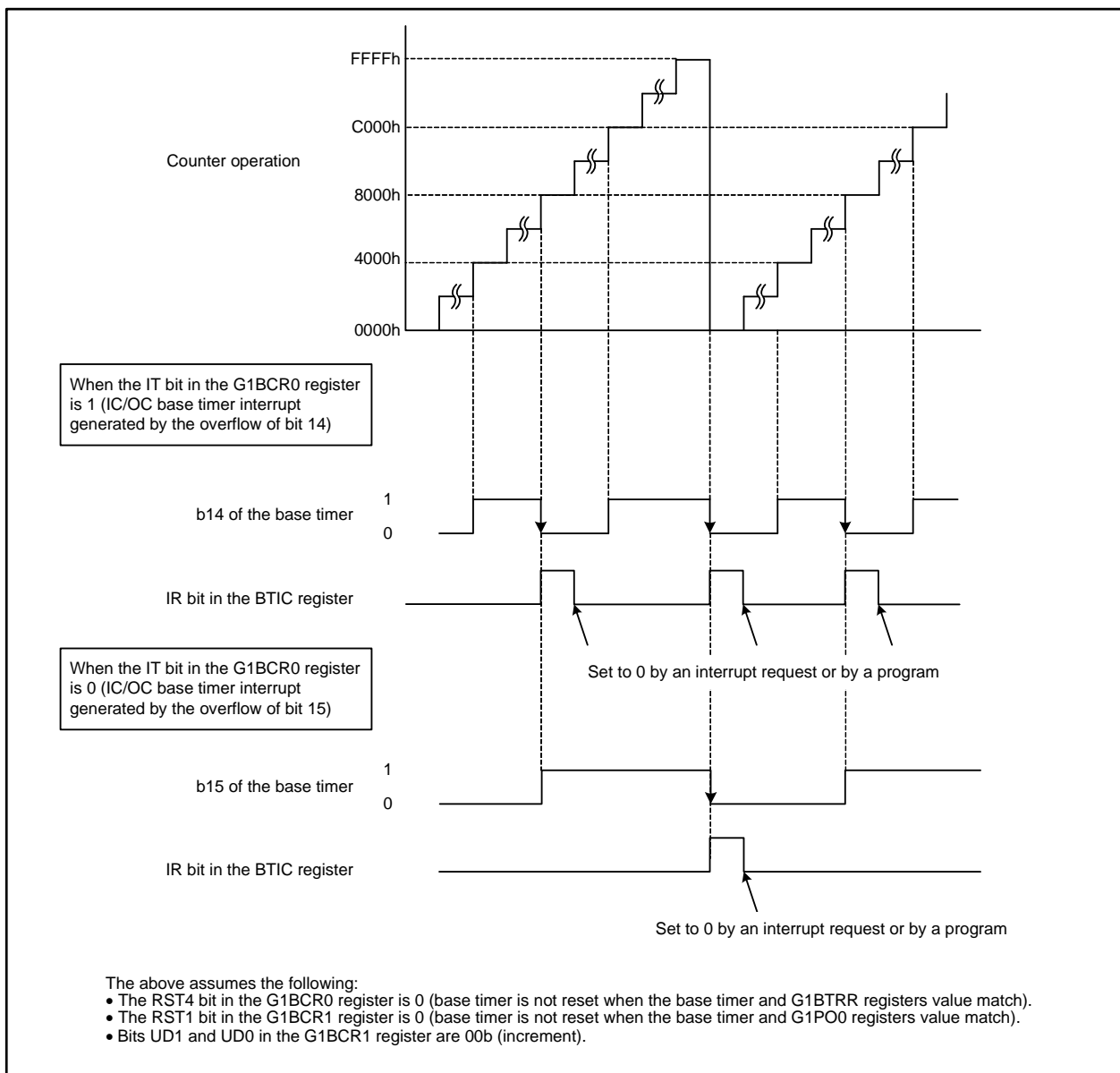


Figure 18.4 Increment

### 18.3.1.2 Increment/Decrement

The counter starts incrementing from 0000h to FFFFh, then decrements from FFFFh to 0000h. When the counter reaches 0000h, the base timer increments again.

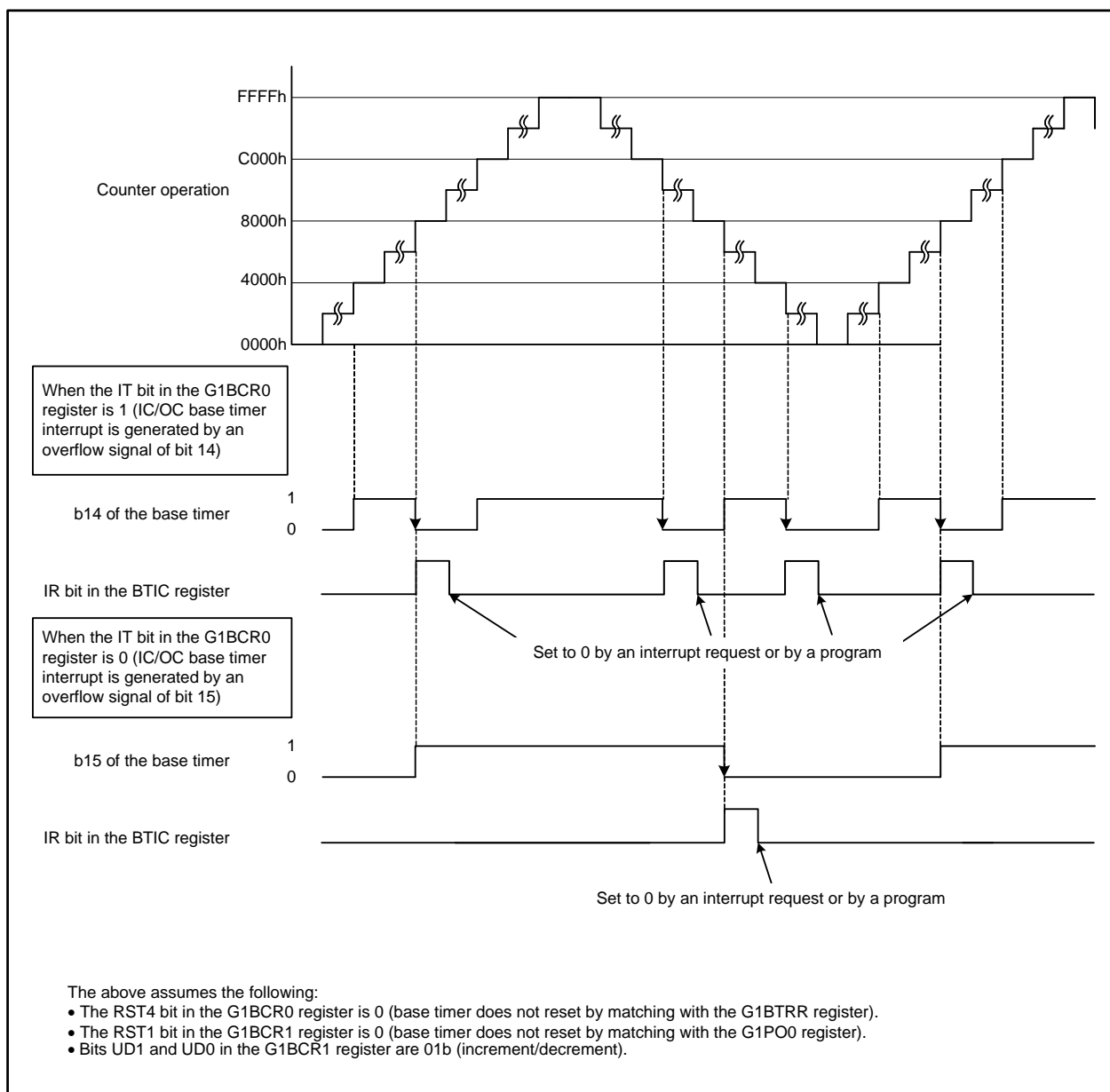


Figure 18.5 Increment/Decrement



### 18.3.1.3 Two-Phase Pulse Signal Processing

This count operation counts two-phase pulse input from pins TSUDA and TSUDB.

Set the following bits as shown below for two-phase pulse signal processing.

Bits BCK1 and BCK0 in the G1BCR0 register: 10b (two-phase pulse clock)

RST2 bit in the G1BCR1 register: 1 (the base timer is reset when low is input to the  $\overline{\text{INT1}}$  pin.)

Bits UD1 to UD0 in the G1BCR1 register (two-phase pulse signal processing)

Figure 18.6 shows Two-Phase Pulse Signal Processing, and Figure 18.7 shows Two-Phase Pulse Signal Processing (When Using the Base Timer Reset).

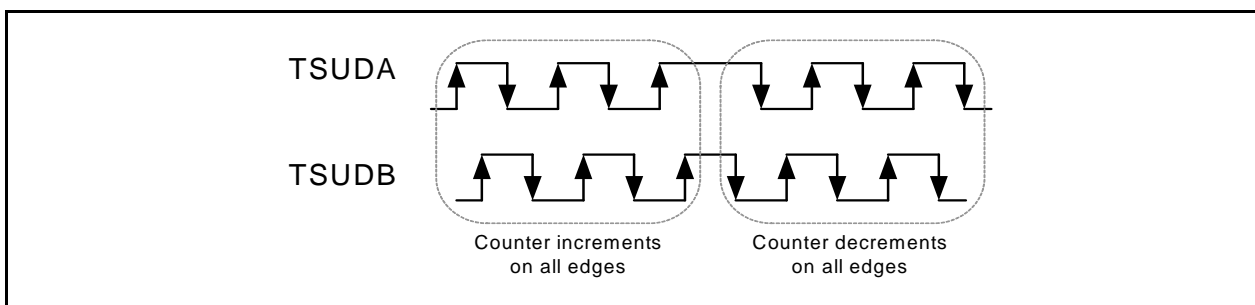
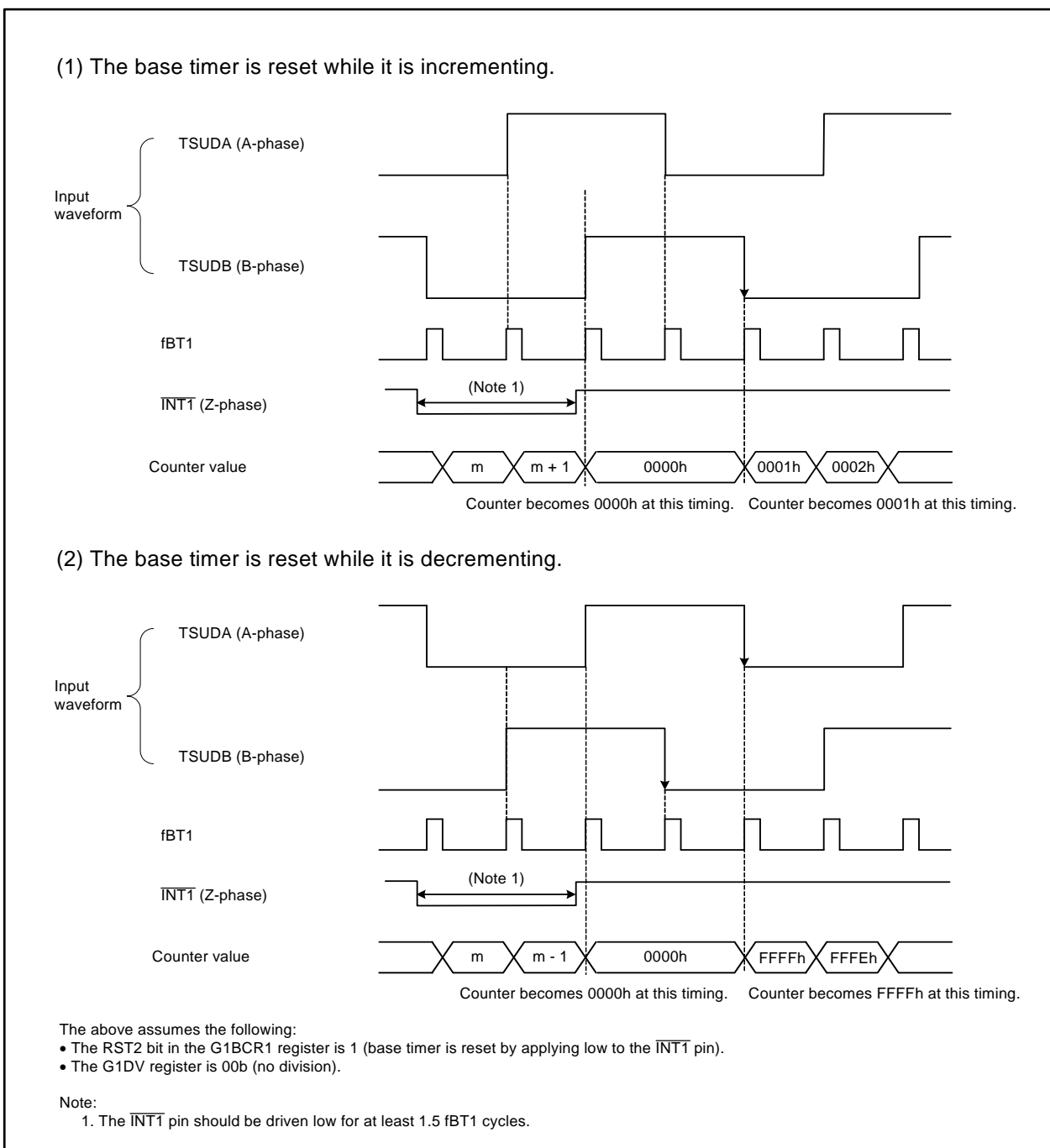


Figure 18.6 Two-Phase Pulse Signal Processing



**Figure 18.7 Two-Phase Pulse Signal Processing (When Using the Base Timer Reset)**

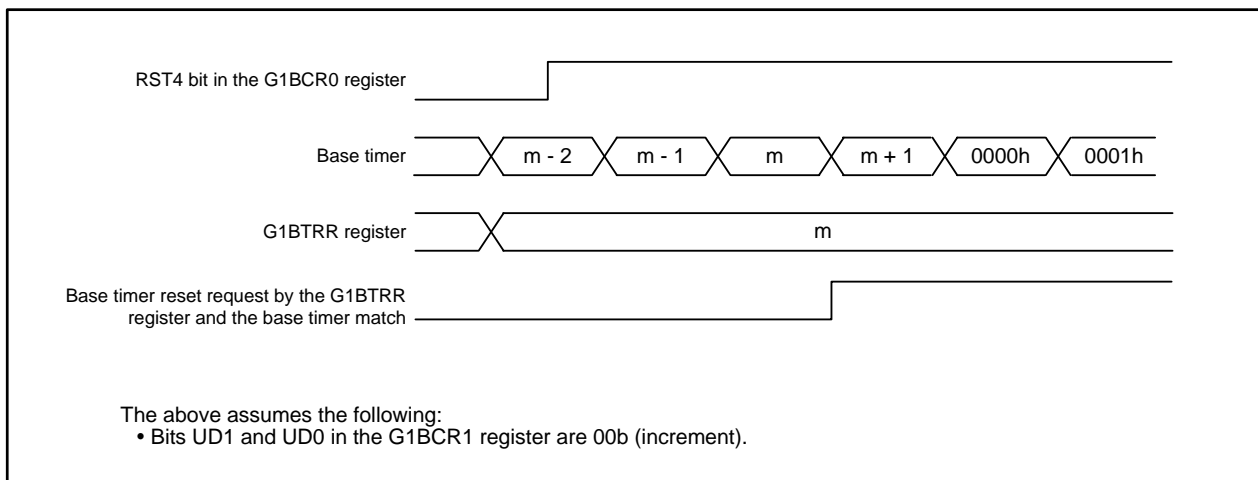
### 18.3.1.4 Base Timer Reset While the Base Timer is Counting

The base timer is reset by one of the following conditions:

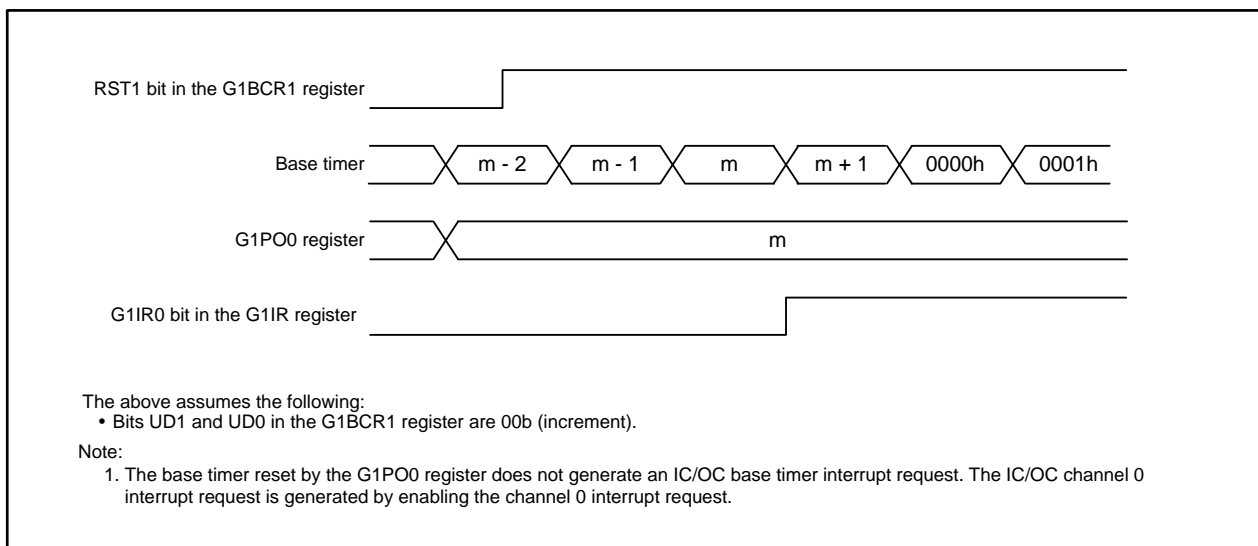
- The G1BTRR register value matches the base timer value after setting the RST4 in the G1BCR0 register to 1 (the base timer is reset by matching with the G1BTRR register).
- The G1PO0 register value matches the base timer value after setting the RST1 bit in the G1BCR1 register to 1 (the base timer is reset by matching with the G1PO0 register).
- Apply a low signal to the  $\overline{\text{INT1}}$  external interrupt pin after setting the RST2 bit in the G1BCR1 register to 1 (the base timer is reset by applying a low signal to the  $\overline{\text{INT1}}$  pin).

Do not set bits RST4 and RST1 to 1 at the same time.

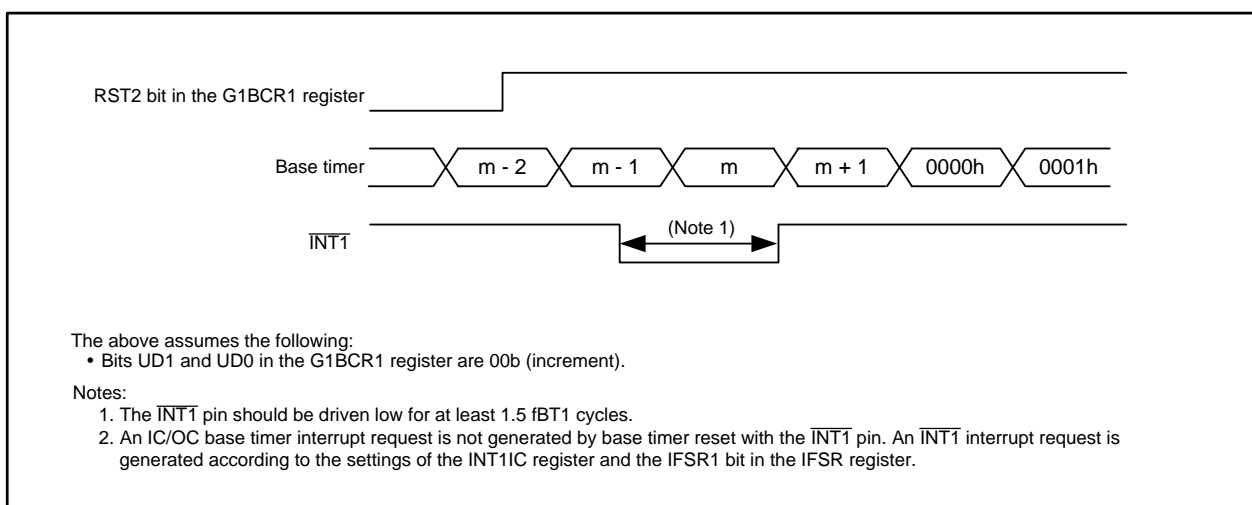
When the base timer counter is running, but not free-running, and the base timer is reset by matching the G1BTRR register, channel 0 can be used for the waveform generation function.



**Figure 18.8 Base Timer Reset with the G1BTRR Register**



**Figure 18.9 Base Timer Reset with the G1PO0 Register**



**Figure 18.10 Base Timer Reset with  $\overline{INT1}$  Pin Input**

Table 18.7 to Table 18.9 list the relationship between base timer count operation and the count value when the base timer is reset.

**Table 18.7 Increment**

Reset Source	Count Direction	Count Value
RST1 reset	No change (increments)	0000h
RST2 reset	No change (increments)	0000h
RST4 reset	No change (increments)	0000h

**Table 18.8 Increment/Decrement**

Reset Source	Increment Operation		Decrement Operation	
	Count direction	Count value	Count direction	Count value
RST1 reset	Increment to decrement	— (count continues)	No change (decrements)	— (count continues)
RST2 reset	Increment to decrement	— (count continues)	No change (decrements)	— (count continues)
RST4 reset	Increment to decrement	— (count continues)	No change (decrements)	— (count continues)

**Table 18.9 Two-Phase Pulse Signal Processing**

Reset Source	Increment Operation		Decrement Operation	
	Count direction	Count value	Count direction	Count value
RST1 reset	No change (increments)	0000h	No change (decrements)	— (count continues)
RST2 reset	No change (increments)	0000h	No change (decrements)	0000h
RST4 reset	No change (increments)	0000h	No change (decrements)	— (count continues)

### 18.3.2 Time Measurement Function

The base timer value is stored in the G1TMj register ( $j = 0$  to  $7$ ) using an external input as a trigger. Table 18.10 lists the specifications of the time measurement function. Table 18.11 lists the time measurement function associated registers and their settings. Figure 18.11 to Figure 18.12 show the operation examples of the time measurement function.

Figure 18.13 shows the operation example of the prescaler function and gate function.

**Table 18.10 Time Measurement Function Specifications**

Item	Specification
Measurement channels	Channels 0 to 7
Trigger input polarity	Selectable from rising edge, falling edge, or both edges of the INPC1_j pin input.
Measurement start condition	While the FSCj bit in the G1FS register is 1 (time measurement function selected), set the IFEj bit in the G1FE register to 1 (channel j function enabled).
Measurement stop condition	Set the IFEj bit to 0 (channel j function disabled).
Time measurement timing	<ul style="list-style-type: none"> <li>• Without prescaler: every trigger input</li> <li>• With prescaler (channels 6 and 7): every (G1TPRk register value + 1) time a trigger is input</li> </ul>
Interrupt request occurrence timing	At the time measurement timing
INPC1_j pin function	Trigger input
Selectable functions	<ul style="list-style-type: none"> <li>• Digital filter The digital filter judges a trigger input level at each sampling clock (f1TIMS, f2TIMS, or fBT1) and passes the pulse that matches its signal level three times.</li> <li>• Prescaler (channels 6 and 7) Time measurement is executed every (G1TPRk register value + 1) times a trigger is input.</li> <li>• Gate function (channels 6 and 7) After a time measurement is performed by the first trigger input, subsequent trigger inputs are disabled.</li> <li>• Digital debounce filter (channel 7) When P1_7/INPC1_7 is selected, the digital debounce filter is enabled.</li> </ul>

$j = 0$  to  $7$ ;  $k = 6$  and  $7$

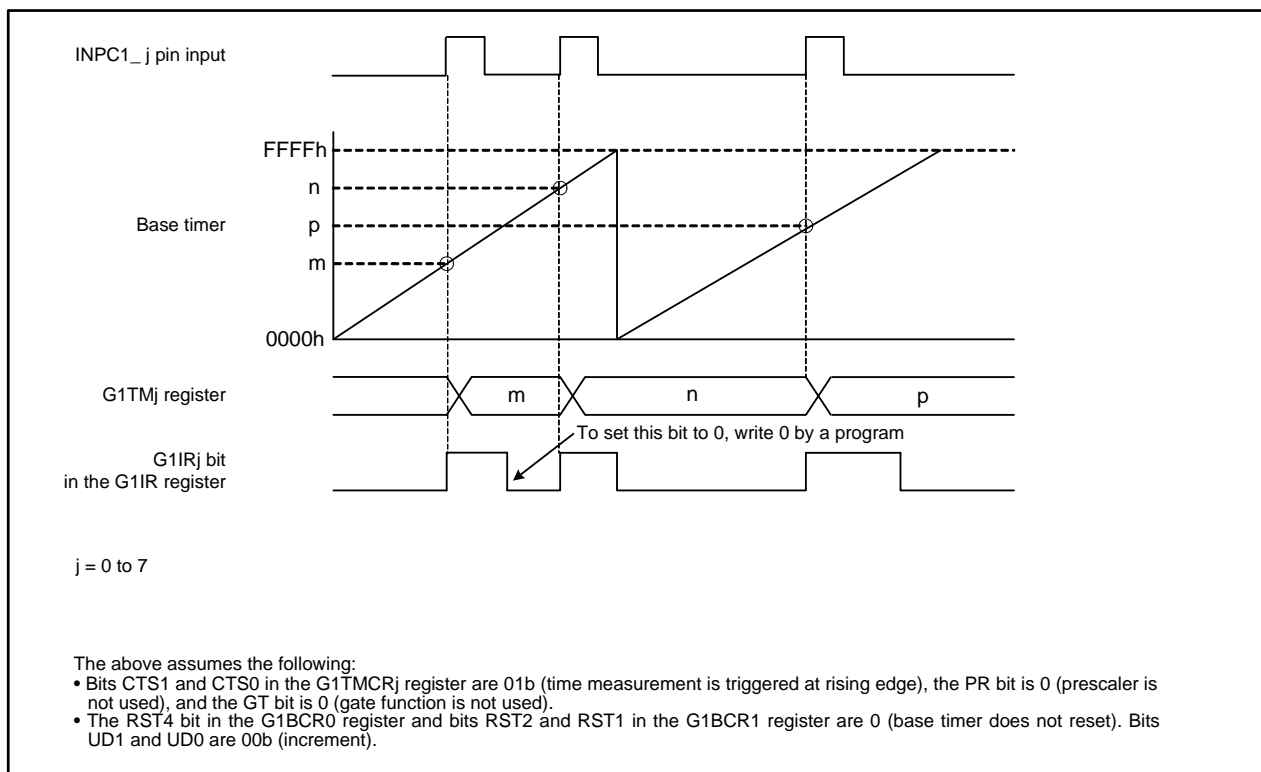
**Table 18.11 Time Measurement Function Associated Registers (1)**

Register	Bit	Function
G1TMj	—	Time measurement result can be read.
G1TMCRj	CTS1 and CTS0	Select a time measurement trigger.
	DF1 and DF0	Select whether the digital filter function is used. If used, select a sampling clock to use for the function.
G1TMCRk	GT, GOC, GSC	Select if the gate function is used.
	PR	Select whether the prescaler function is used.
G1TPRk	—	Set a value if the prescaler function is used.
G1FS	FSCj	Set to 1 (time measurement function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).
G1POCRp	MOD1 and MOD0	Set to 00b. (2)
G1POp	—	Set a gate release timing. (2)
G1FS	FSCp	Set to 0. (2)
G1FE	IFEp	Set to 1. (2)
G1OER	EOCp	Set to 1. (2)
G1IOR1	IOp1 and IOp0	Set to 00b. (2)
G1CBR0	CH7INSEL	Select a pin to allocate INPC1_7.

j = 0 to 7; k = 6 and 7; p = k - 2

Notes:

1. This table does not describe a procedure.
2. Set when bits GT and GOC in the G1TMCRk register are 1.

**Figure 18.11 Time Measurement Function (1/2)**

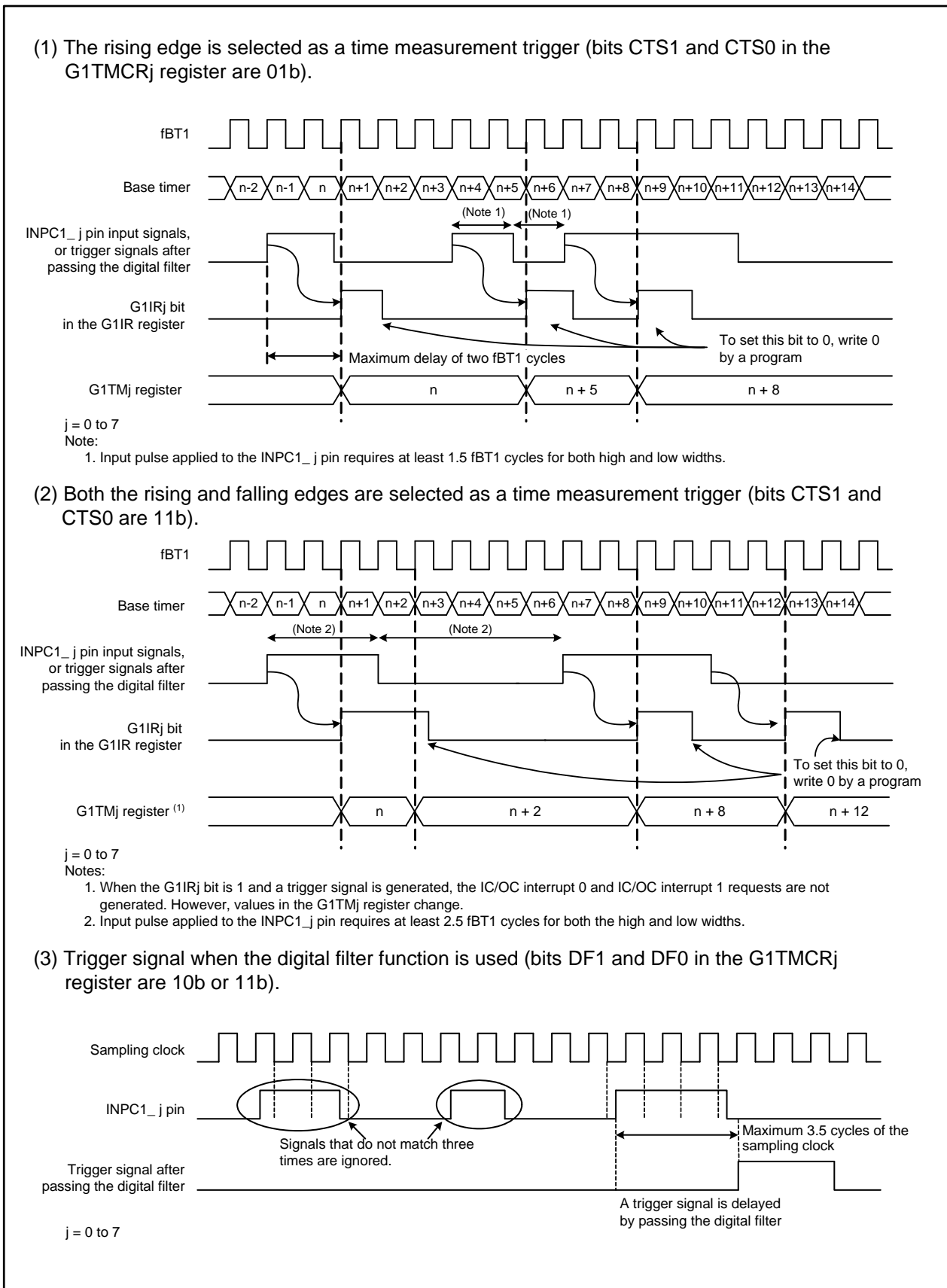


Figure 18.12 Time Measurement Function (2/2)

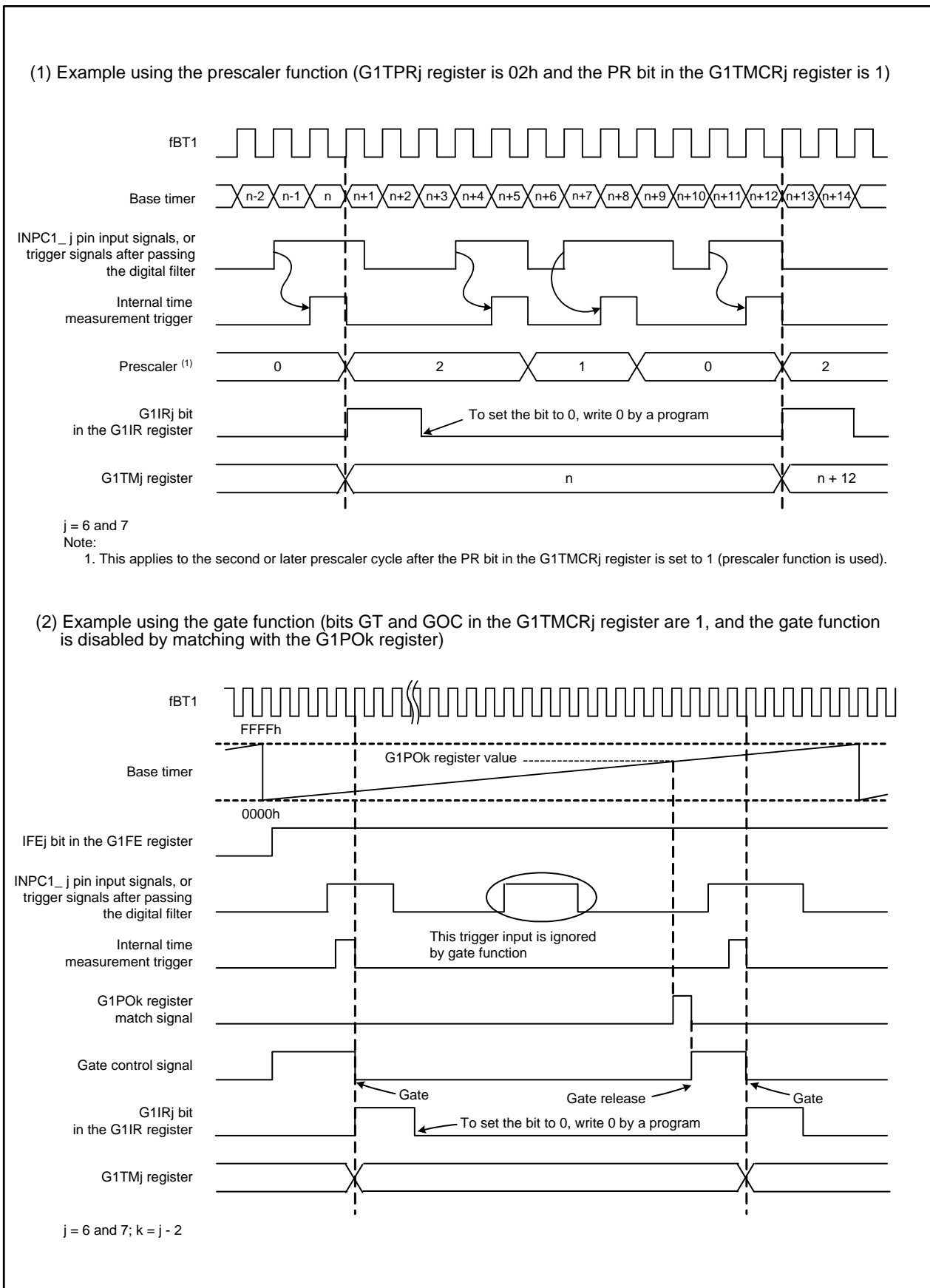


Figure 18.13 Prescaler and Gate Functions



### 18.3.2.1 Gate Function (Channel 6 and 7)

When the GT bit in the G1TMCRj register (j = 6 and 7) is 1 (gate function used), acceptance of trigger inputs is disabled after the time measurement by the first trigger input.

When 1 is written to the GSC bit in the G1TMCRj register, acceptance of trigger inputs becomes enabled again.

When the GOC bit in the G1TMCRj register is 1, acceptance of trigger inputs also becomes enabled again by matching the base timer with the G1POk register (k = j - 2).

“(2) Example using the gate function” in Figure 18.13 “Prescaler and Gate Functions” shows the operation example of this function.

### 18.3.3 Waveform Generation Function

A waveform is generated using the base timer value and the G1POj register value (j = 0 to 7). The waveform generation function has the following three modes:

- Single-phase waveform output mode
- Inverted waveform output mode
- Set/reset (SR) waveform output mode

In single-phase waveform output mode and inverted waveform output mode, compare match output is selectable.

In all three modes, each channel output can be temporarily disabled and used as a programmable I/O port when the waveform generation is in progress.

### 18.3.3.1 Single-Phase Waveform Output Mode

The OUTC1<sub>j</sub> pin outputs high when the base timer value matches the G1PO<sub>j</sub> register value ( $j = 0$  to  $7$ ) and the INV bit in the G1POCR<sub>j</sub> register is 0 (output level is not inverted).

The OUTC1<sub>j</sub> pin outputs low when the base timer reaches 0000h. When bits MOD1 and MOD0 in the G1POCR<sub>j</sub> register are 00b (single-phase waveform output mode), set bits UD1 and UD0 in the G1BCR register to 00b (increment). Table 18.12 lists the specifications of single-phase waveform output mode, Figure 18.14 to Figure 18.15 show operational examples in single-phase waveform output mode.

**Table 18.12 Single-Phase Waveform Output Mode Specifications**

Item	Specification
Output waveform	<ul style="list-style-type: none"> <li>Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0 (base timer is not reset))</li> </ul> <p>Cycle: <math>\frac{65536}{f_{BT1}}</math></p> <p>Initial output level width: <math>\frac{m}{f_{BT1}}</math></p> <p>Inverted output level width: <math>\frac{65536 - m}{f_{BT1}}</math></p> <ul style="list-style-type: none"> <li>When the base timer matches either of following registers, the base timer is reset to 0000h. <ul style="list-style-type: none"> <li>G1PO0 register (when the RST1 bit is 1, and bits RST4 and RST2 are 0)</li> <li>G1BTRR register (when the RST4 bit is 1, and bits RST2 and RST1 are 0)</li> </ul> </li> </ul> <p>Cycle: <math>\frac{n + 2}{f_{BT1}}</math></p> <p>Initial output level width: <math>\frac{m}{f_{BT1}}</math></p> <p>Inverted output level width: <math>\frac{n + 2 - m}{f_{BT1}}</math></p> <p>m: G1PO<sub>j</sub> register setting value  n: G1PO0 register or G1BTRR register setting value  0001h ≤ m &lt; n ≤ FFFDh</p>
Waveform output start condition	Set the IFE <sub>j</sub> bit in the G1FE register to 1 (channel j function enabled).
Waveform output stop condition	Set the IFE <sub>j</sub> bit to 0 (channel j function disabled).
Interrupt request occurrence timing	When the base timer value matches the G1PO <sub>j</sub> register value.
OUTC1 <sub>j</sub> pin	Pulse output or I/O port
Selectable functions	<ul style="list-style-type: none"> <li>Default value setting Select the starting waveform output level.</li> <li>Output level inversion Output an inverted waveform from the OUTC1<sub>j</sub> pin.</li> <li>Compare match output When using the compare match output function, the output level is fixed to high or low from when the base timer value matches the G1PO<sub>j</sub> register value. If the compare match output function is released, a single-phase waveform is output again when the base timer next matches the G1PO<sub>j</sub> register.</li> <li>Output disabled function When the EOC<sub>j</sub> bit in the G1OER register is 1 (output disabled), the OUTC1<sub>j</sub> pin stops waveform output and becomes a programmable I/O port. When the EOC<sub>j</sub> bit is 0 (output enabled), the OUTC1<sub>j</sub> pin outputs a single-phase waveform again.</li> </ul>

$j = 0$  to  $7$

**Table 18.13 Registers and Settings in Single-Phase Waveform Output Mode (1)**

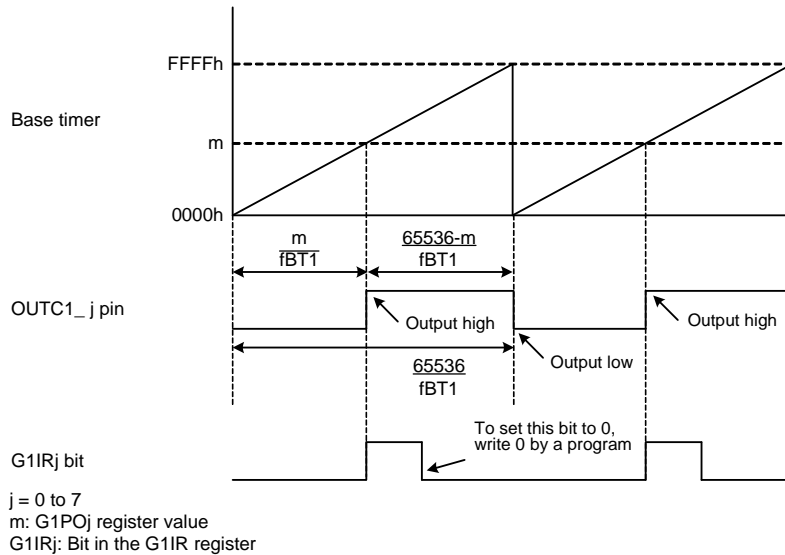
Register	Bit	Function
G1POj	—	Set the timing for an output level to become high. (2)
G1FS	FSCj	Set to 0 (waveform generation function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).
G1POCRj	MOD1 and MOD0	Set to 00b.
	IVL	Select a default value of an output level.
	RLD	Select the reload timing for the G1POj register value.
	INV	Select whether an output level is inverted.
G1OER	EOCj	Set to 1 when the OUTC1_j output is disabled.
G1IOR0 G1IOR1	IOj1 and IOj0	Select an output level when compare results match.
G1BCR1	UD1 and UD0	Set to 00b.

j = 0 to 7, however, when the RST1 bit in the G1BCR1 register is 1 (the base timer is reset when the base timer and G1PO0 register values match), then j = 1 to 7.

## Notes:

1. This table does not describe a procedure.
2. When the INV bit in the G1POCRj register is 0 (output level not inverted).

- (1) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0).

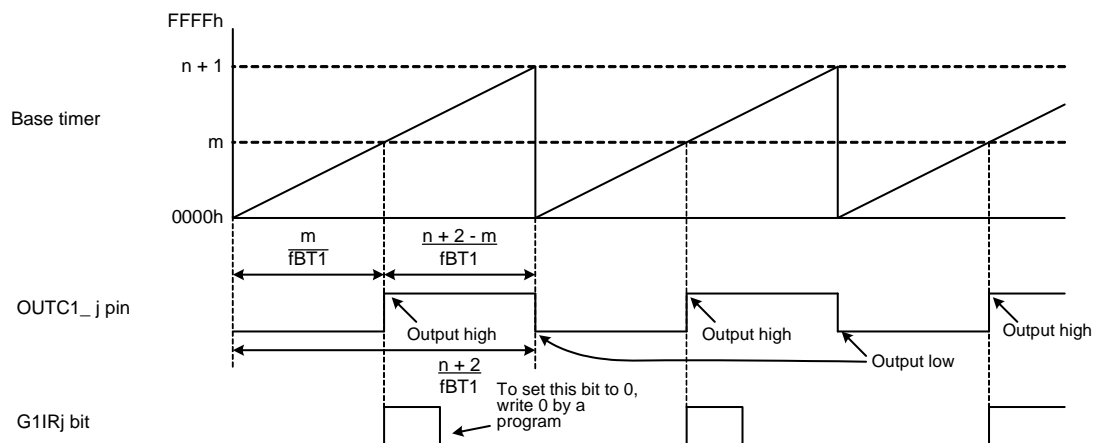


The diagram above applies under the following conditions:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

- (2) When the base timer matches either of the following registers, the base timer is reset:

- (a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)  
 (b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



When (a),  $j = 1$  to 7. When (b),  $j = 0$  to 7.

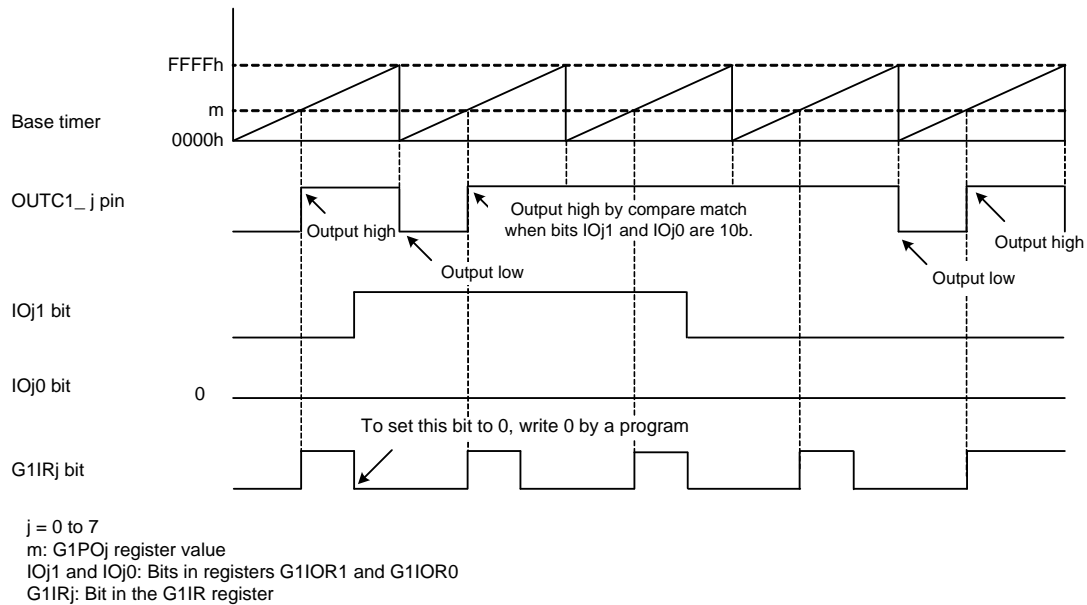
$m$ : G1POj register value  
 $n$ : G1PO0 register or G1BTRR register setting value  
 G1IRj: Bit in the G1IR register

The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.14 Single-Phase Waveform Output Mode Operation (1/2)

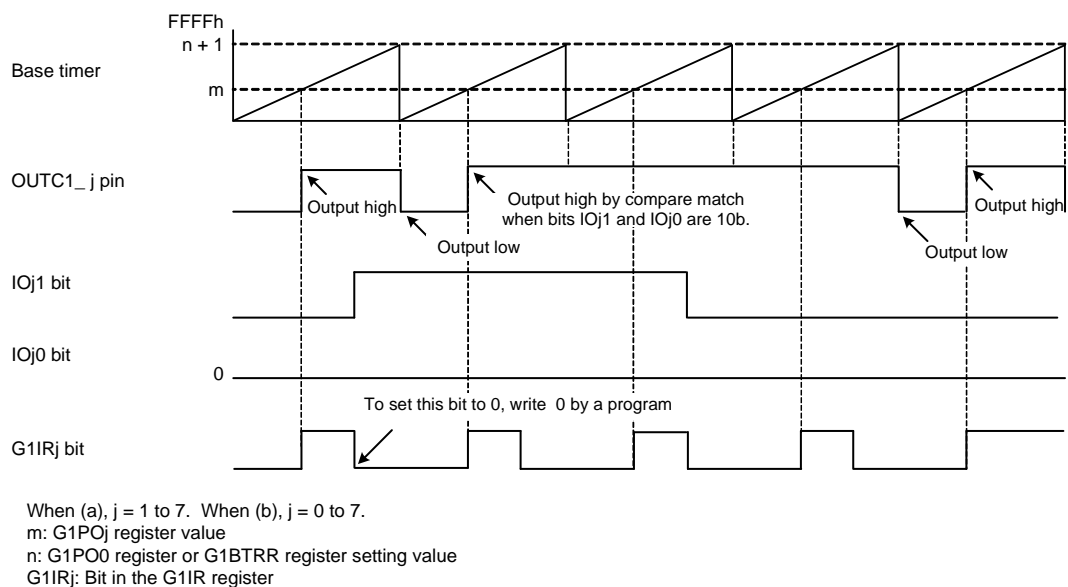
- (3) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0).



The above assumes the following:

- IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- EOCj bit in the G1OER register is 0 (output enabled).

- (4) When the base timer matches either of following registers, the base timer is reset:
- G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
  - G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.15 Single-Phase Waveform Output Mode Operation (2/2)

### 18.3.3.2 Inverted Waveform Output Mode

The output level at the OUTC1\_j pin is inverted every time the base timer value matches the G1POj register value (j = 0 to 7). When bits MOD1 and MOD0 in the G1POCRj register are 10b (inverted waveform output mode), set bits UD1 and UD0 in the G1BCR1 register to 00b (increment) or 01b (increment/decrement).

Table 18.14 lists the specifications of inverted waveform output mode. Figure 18.16 and Figure 18.17 show the operational examples of inverted waveform output mode.

**Table 18.14 Inverted Waveform Output Mode Specifications**

Item	Specification
Output waveform	<ul style="list-style-type: none"> <li>Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0 (the base timer is not reset))</li> </ul> <p>Cycle: <math>\frac{65536 \times 2}{f_{BT1}}</math></p> <p>High or low width: <math>\frac{65536}{f_{BT1}}</math></p> <ul style="list-style-type: none"> <li>When the base timer matches either of the following registers, the base timer is set to 0000h: <ul style="list-style-type: none"> <li>G1PO0 register (when the RST1 bit is 1, and bits RST4 and RST2 are 0)</li> <li>G1BTRR register (when the RST4 bit is 1, and bits RST2 and RST1 are 0)</li> </ul> </li> </ul> <p>Cycle: <math>\frac{2(n+2)}{f_{BT1}}</math></p> <p>High or low width: <math>\frac{n+2}{f_{BT1}}</math></p> <p>m: G1POj register setting value  n: G1PO0 register or G1BTRR register setting value  0000h ≤ m &lt; n ≤ FFFDh</p>
Waveform output start condition	Set the IFEj bit in the G1FE register to 1 (channel j function enabled).
Waveform output stop condition	Set the IFEj bit to 0 (channel j function disabled).
Interrupt request occurrence timing	When the base timer value matches the G1POj register value.
OUTC1_j pin	Pulse output or I/O port
Selectable functions	<ul style="list-style-type: none"> <li>Default value setting Select the starting waveform output level.</li> <li>Output level inversion Select if the waveform level output from the OUTC1_j pin is inverted.</li> <li>Compare match output function When the compare match output function is set, the output level is fixed to high or low from when the base timer value matches the G1POj register value. When the compare match output function is disabled, an inverted waveform is output again from the next compare match timing.</li> <li>Output disabled function When the EOCj bit in the G1OER register is 1 (output disabled), the OUTC1_j pin stops waveform output and becomes a programmable I/O port. When the EOCj bit is 0 (output enabled), the OUTC1_j pin outputs inverted waveform again.</li> </ul>

j = 0 to 7

**Table 18.15 Registers and Settings in Inverted Waveform Output Mode <sup>(1)</sup>**

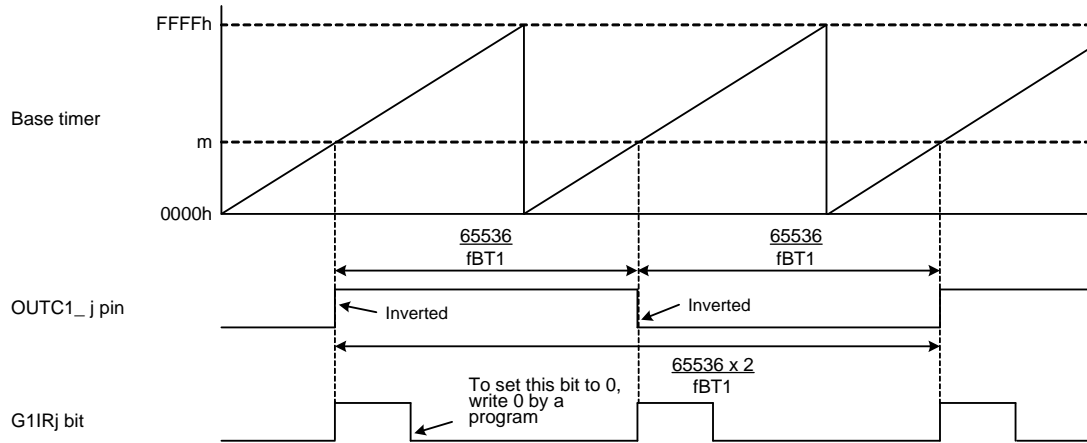
Register	Bit	Function
G1POj	—	Set the timing for the waveform to be inverted.
G1FS	FSCj	Set to 0 (waveform generation function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).
G1POCRj	MOD1 and MOD0	Set to 10b.
	IVL	Select a default value of an output level.
	RLD	Select the reload timing for the G1POj register value.
	INV	Select whether an output level is inverted.
G1OER	EOCj	Set to 1 when the OUTC1_j output is disabled.
G1IOR0 G1IOR1	IOj1 and IOj0	Select an output level when compare results match.
G1BCR1	UD1 and UD0	Set to 00b or 01b.

j = 0 to 7, however, when the RST1 bit in the G1BCR1 register is 1 (the base timer is reset when the base timer and G1PO0 register values match), then j = 1 to 7.

**Note:**

1. This table does not describe a procedure.

(1) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0)



$j = 0$  to 7  
 m: G1POj register value  
 G1IRj: Bit in the G1IR register

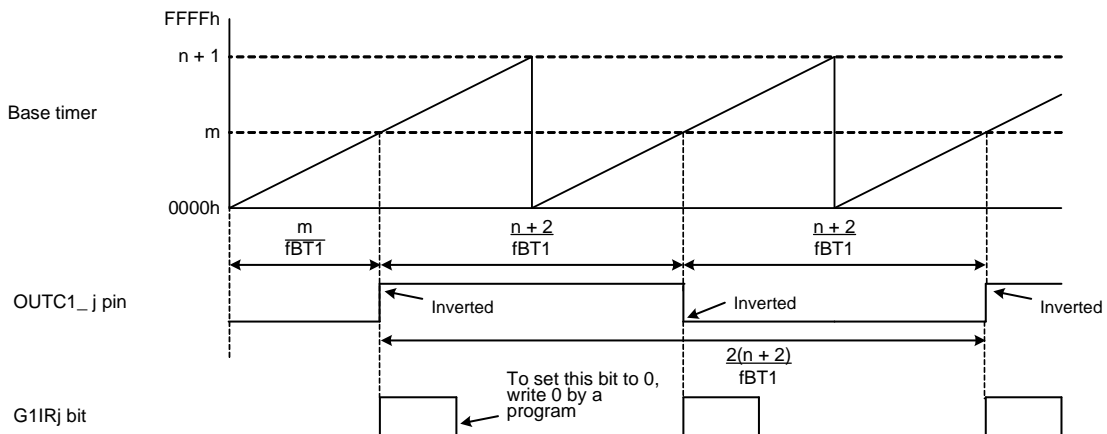
The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

(2) When the base timer matches either of following registers, the base timer is reset:

(a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)

(b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



When (a),  $j = 1$  to 7. When (b),  $j = 0$  to 7.

m: G1POj register value  
 n: G1PO0 register or G1BTRR register value  
 G1IRj: Bit in the G1IR register

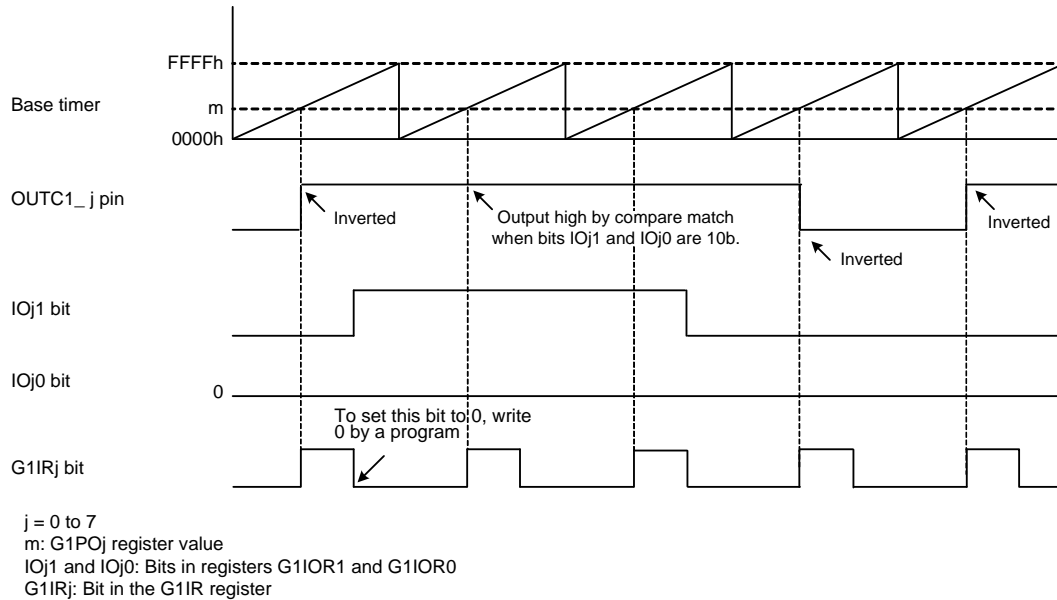
The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.16 Inverted Waveform Output Mode Operation (1/2)



(3) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0):

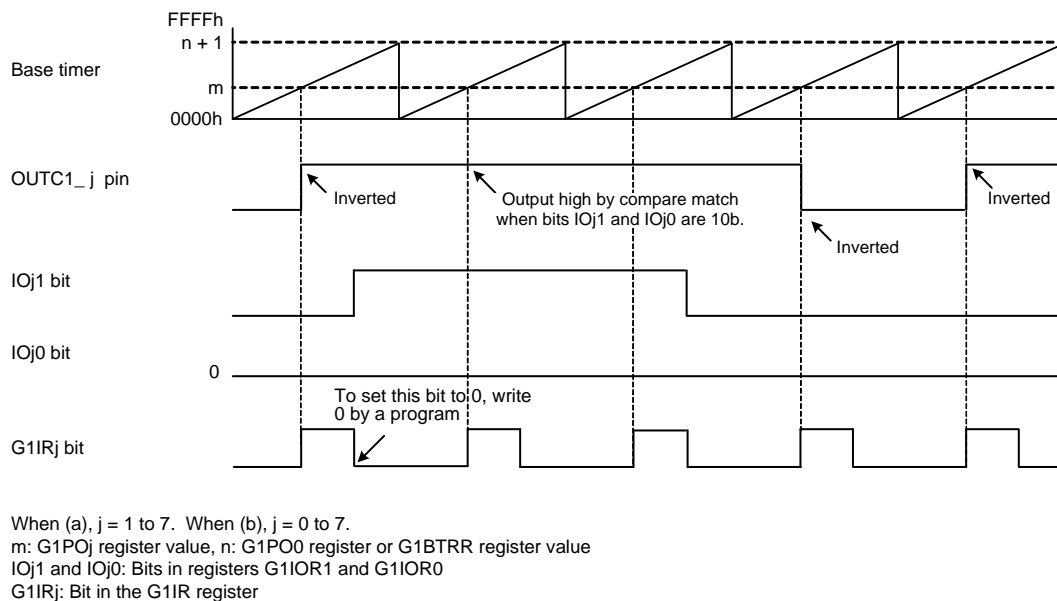


The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (Output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- The EOCj bit in the G1OER register is 0 (output enabled).

(4) When the base timer matches either of following registers, the base timer is reset:

- (a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)  
 (b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- Bits UD1 and UD0 in the G1BCR1 register are 00b (increment).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.17 Inverted Waveform Output Mode Operation (2/2)

### 18.3.3.3 Set/Reset Waveform Output Mode (SR Waveform Output Mode)

The OUTC1<sub>j</sub> pin outputs high when the INV bit in the G1POCR<sub>j</sub> register ( $j = 0, 2, 4, 6$ ) is 0 (output level is not inverted) and the base timer value matches the G1PO<sub>j</sub> register value. When the base timer value matches the G1PO<sub>k</sub> register value ( $k = j + 1$ ), the OUTC1<sub>j</sub> pin outputs low.

When bits MOD1 and MOD0 in registers G1POCR<sub>j</sub> and G1POCR<sub>k</sub> are 01b (SR waveform output mode), set bits UD1 and UD0 in the G1BCR register to 00b (increment).

Table 18.16 lists the specifications of SR waveform output mode and Figure 18.18 shows the operational example of SR waveform output mode.

**Table 18.16 SR Waveform Output Mode Specifications**

Item	Specification
Output waveform	<ul style="list-style-type: none"> <li>Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0 (the base timer is not reset))</li> </ul> <p>Cycle: <math>\frac{65536}{f_{BT1}}</math></p> <p>Inverted output level width: <math>\frac{n-m}{f_{BT1}}</math></p> <ul style="list-style-type: none"> <li>When the base timer matches either of following registers, the base timer is reset to 0000h: <ul style="list-style-type: none"> <li>G1PO0 register (when the RST1 bit is 1, and bits RST4 and RST2 are 0) <sup>(1)</sup></li> <li>G1BTRR register (when the RST4 bit is 1, and bits RST2 and RST1 are 0)</li> </ul> </li> </ul> <p>Cycle: <math>\frac{p+2}{f_{BT1}}</math></p> <p>Inverted output level width: <math>\frac{n-m}{f_{BT1}}</math></p> <p>m: G1PO<sub>j</sub> register setting value  n: G1PO<sub>k</sub> register setting value  p: G1PO0 register or G1BTRR register value  0000h ≤ m &lt; n &lt; p ≤ FFFDh</p>
Waveform output start condition	Set bits IFE <sub>j</sub> and IFE <sub>k</sub> in the G1FE register to 1 (channel j function enabled).
Waveform output stop condition	Set bits IFE <sub>j</sub> and IFE <sub>k</sub> to 0 (channel j function disabled).
Interrupt request occurrence timing	<ul style="list-style-type: none"> <li>Channel j When the base timer value matches the G1PO<sub>j</sub> register value.</li> <li>Channel k When the base timer value matches the G1PO<sub>k</sub> register value.</li> </ul>
OUTC1 <sub>j</sub> pin	Pulse output or I/O port
Selectable functions	<ul style="list-style-type: none"> <li>Default value setting Select the starting waveform output level.</li> <li>Output level inversion Select if the waveform level output from the OUTC1<sub>j</sub> pin is inverted.</li> <li>Output disabled When the EOC<sub>j</sub> bit in the G1OER register is 1 (output disabled), the OUTC1<sub>j</sub> pin stops waveform output and becomes a programmable I/O port. When the EOC<sub>j</sub> bit is 0 (output enabled), the OUTC1<sub>j</sub> pin outputs SR waveform again.</li> </ul>

$j = 0, 2, 4, 6; k = j + 1$

Note:

- When the RST1 bit in the G1BCR1 register is 1 (the base timer is reset by the G1PO0 register), SR waveform output mode is disabled for channels 0 and 1.

**Table 18.17 Registers and Settings in SR Waveform Output Mode (1)**

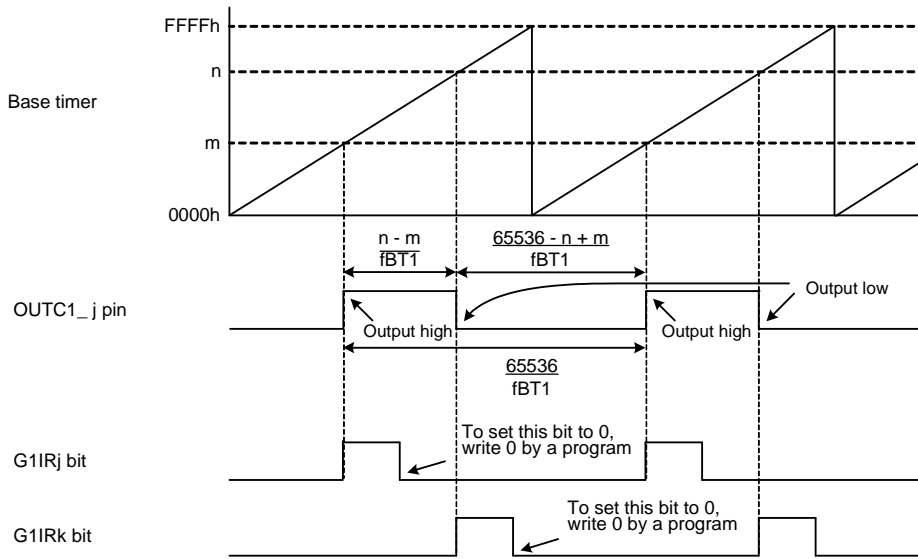
Register	Bit	Function	
		Even channel (channel j)	Odd channel (channel k)
G1POj	—	Set the timing for an output level to become high. (2)	Set the timing for an output level to become low. (2)
G1FS	FSCj	Set to 0 (waveform generation function selected).	Set to 0 (waveform generation function selected).
G1FE	IFEj	Set to 1 (channel j function enabled).	Set to 1 (channel k function enabled).
G1POCRj	MOD1 and MOD0	Set to 01b.	Set to 01b.
	IVL	Select a default value of an output level.	— (invalid)
	RLD	Select the reload timing for the G1POj register value.	Select the reload timing for the G1POk register value.
	INV	Select whether an output level is inverted.	— (invalid)
G1OER	EOCj	Set to 1 when the OUTC1_j is disabled.	Set to 1.
G1IOR0 G1IOR1	IOj1 and IOj0	Set to 00b.	Set to 00b.
G1BCR1	UD1 and UD0	Set to 00b.	

j = 0, 2, 4, 6; k = j + 1, however, when the RST1 bit in the G1BCR1 register is 1 (the base timer is reset when the base timer and G1PO0 register values match), then j = 2, 4, 6.

## Notes:

1. This table does not describe a procedure.
2. When the INV bit in the G1POCRj register is 0 (output level not inverted).

(1) Free-running operation (when bits RST2 and RST1 in the G1BCR1 register and the RST4 bit in the G1BCR0 register are all 0)



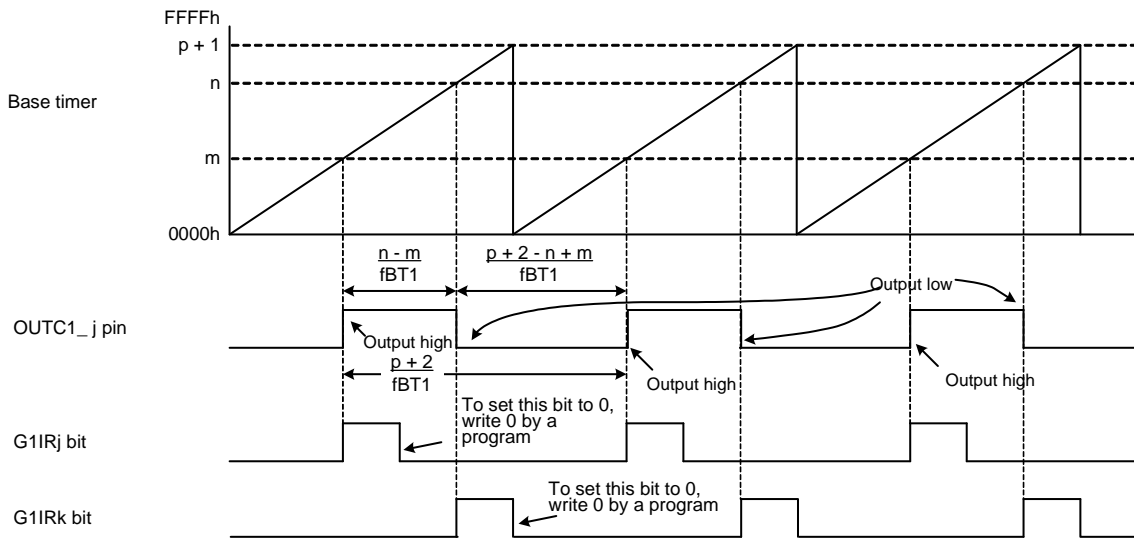
$j = 0, 2, 4, 6; k = j + 1$   
 m: G1POj register value  
 n: G1POk register value  
 G1IRj and G1IRk: Bits in the G1IR register

The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- The EOCj bit in the G1OER register is 0 (output enabled).

(2) When the base timer matches either of following registers, the base timer is reset:

- (a) G1PO0 register (when the RST1 bit is 1 and bits RST4 and RST2 are 0)
- (b) G1BTRR register (when the RST4 bit is 1 and bits RST2 and RST1 are 0)



When (a),  $j = 2, 4, 6$ . When (b),  $j = 0, 2, 4, 6$ .  
 $k = j + 1$   
 m: G1POj register value  
 p: Either G1PO0 or G1BTRR register value  
 G1IRj and G1IRk: Bits in the G1IR register

The above assumes the following:

- The IVL bit in the G1POCRj register is 0 (output low as default) and the INV bit is 0 (output is not inverted).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 18.18 Operation Example in SR Waveform Output Mode

### 18.3.4 I/O Port Select Function

The I/O direction of IC/OC pins is determined by registers G1FE, G1FS, and G1OER.

In SR waveform output mode, an even channel and an odd channel are used for each output waveform, but a waveform is output only from the even channel. In this case, the corresponding pin for the odd channel can be used as an I/O port.

**Table 18.18 Pin Settings for Time Measurement and Waveform Generation**

Pin	Pin Settings				Pin Function
	IFE	FSC	MOD1 and MOD0	EOC	
P2_j/ INPC1_j/ OUTC1_j	0	—	—	—	P2_j used as I/O port
	1	1	—	—	INPC1_j (1)
	1	0	00b	0	Single-phase waveform output from OUTC1_j
	1	0	00b	1	P2_j used as I/O port
	1	0	01b	0	SR waveform output from OUTC1_j
	1	0	01b	1	P2_j used as I/O port
	1	0	10b	0	Inverted waveform output from OUTC1_j
	1	0	10b	1	P2_j used as I/O port

j = 0 to 7

—: 0 or 1

IFE: IFE<sub>j</sub> bit in the G1FE register

FSC: FSC<sub>j</sub> bit in the G1FS register

MOD1 and MOD0: Bits in the G1POCR<sub>j</sub> register

EOC: EOC<sub>j</sub> bit in the G1OER register

Note:

1. Set the port direction bits sharing pins to 0 (input mode).

The P2\_7/OUTC1\_7/INPC1\_7 pin or P1\_7/INPC1\_7 pin can be selected as a time measurement pin for IC/OC channel 7 by the CH7INSEL bit in the G1BCR0 register (channel 7 input select bit).

The digital debounce filter for noise reduction can be used with an input to the INP1\_7 pin from the P1\_7/INP1\_7 pin. Refer to 11.4.3 “Digital Debounce Filters” for details.

### 18.4 Interrupts

Refer to each operation example for interrupt request occurrence timings.

Refer to 12.7 “Interrupt Control” for details on interrupt control. Table 18.19 lists Timer S Interrupt Associated Registers.

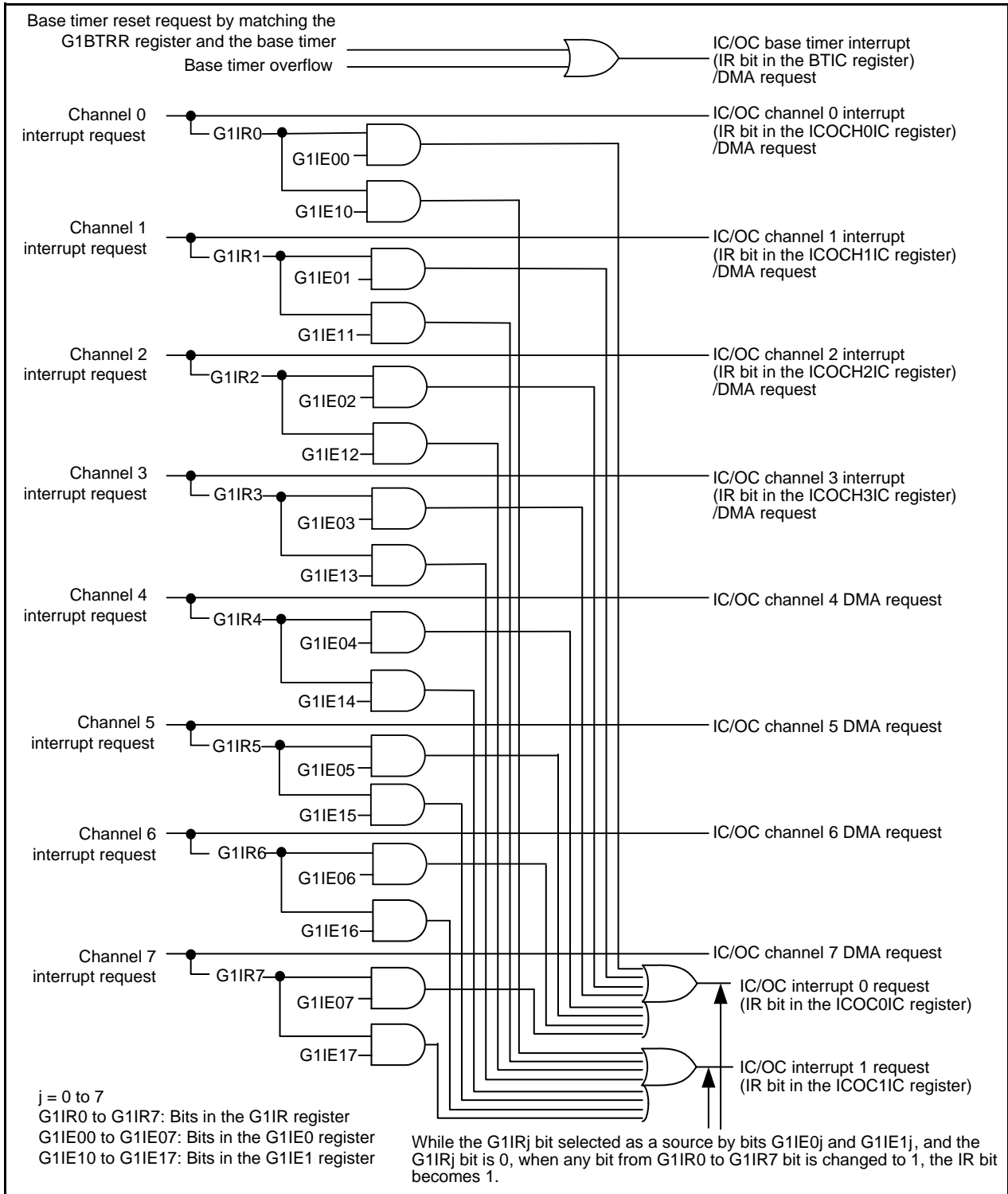


Figure 18.19 Timer S Interrupt and DMA Requests

**Table 18.19 Timer S Interrupt Associated Registers**

Address	Register	Symbol	Reset Value
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register	ICOC1IC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register	ICOCH1IC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b

#### 18.4.1 IC/OC Base Timer Interrupt

When the base timer reset request by matching the G1BTRR register and the base timer, or the base timer overflow is generated, the IR bit in the BTIC register becomes 1 (interrupt requested).

#### 18.4.2 IC/OC Channel 0 Interrupt to IC/OC Channel 3 Interrupt

When interrupt requests for channels 0 to 3 are generated, the corresponding IR bit in registers ICOCH0IC to ICOCH3IC becomes 1 (interrupt requested).

#### 18.4.3 IC/OC Interrupt 0 and IC/OC Interrupt 1

An interrupt request for IC/OC interrupt  $i$  ( $i = 0, 1$ ) is generated in combination with the channel  $j$  interrupt request ( $j = 0$  to  $7$ ). When the G1IE $ij$  bit in the G1IE $i$  register is set to 1 (IC/OC interrupt  $i$  request enabled), the interrupt request for channel  $j$  becomes the IC/OC interrupt  $i$  source.

When the channel  $j$  interrupt request is generated, the G1IR $j$  bit in the G1IR register becomes 1 (interrupt requested). While bits in the G1IR register corresponding to the channels selected as sources with the G1IE $i$  register are all 0 (interrupt not requested), when any bit in the G1IR register becomes 1, the IR bit in the ICOC $i$ IC register becomes 1 (interrupt requested).

The IR bit in the ICOC $i$ IC register becomes 0 automatically when an interrupt request is received (interrupt not requested). However, the G1IR $j$  bit does not become 0 automatically with an interrupt request reception. Thus, set the G1IR $j$  bit to 0 by a program. If the G1IR $j$  bit remains 1 when the IR bit is 0, the IR bit in the ICOC $i$ IC register does not become 1 anymore. This means the IC/OC interrupt  $i$  request is no longer generated.

## 18.5 Notes on Timer S

### 18.5.1 Register Access

The explanation for some bits and registers states, “the value written to this register or this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1)”. When writing these bits or registers, the written value is not reflected to the internal circuits immediately. After writing the value, prewrite operations are performed for up to one fBT1 cycle. When reading these bits or registers immediately after writing the value, the value before writing may be read.

### 18.5.2 Changing the G1IR Register

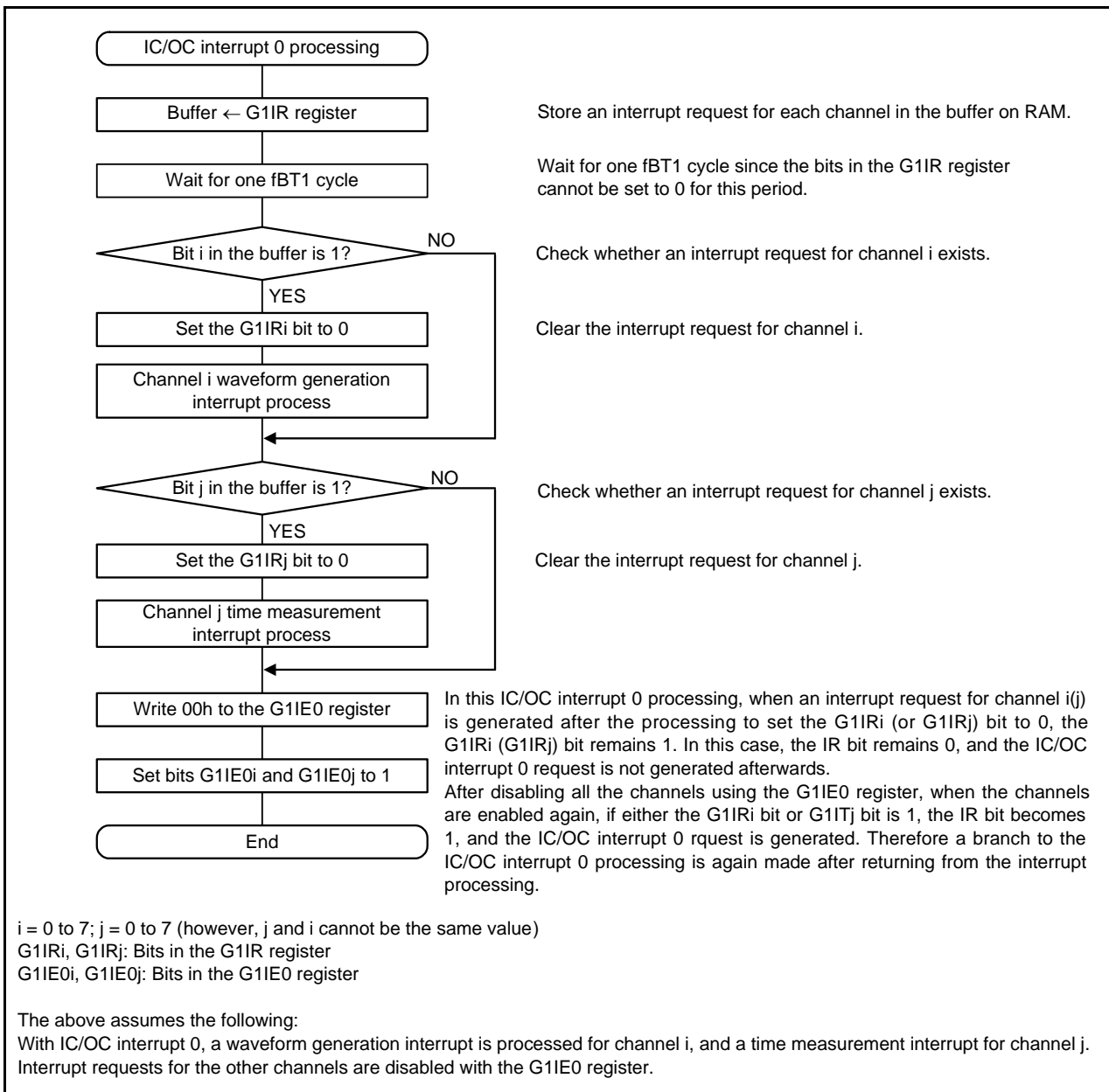
Set the G1IR<sub>j</sub> bit in the G1IR register (j = 0 to 7) to 0 by a program since it does not become 0 automatically with an interrupt request reception.

However, the G1IR<sub>j</sub> bit cannot be set to 0 for one fBT1 cycle after this bit becomes 1. Wait for one or more fBT1 cycles after the G1IR<sub>j</sub> bit becomes 1, then set this bit to 0.

To write 0 to the G1IR<sub>j</sub> bit, use the AND and BCLR instructions to avoid deleting requests for other channels.

Figure 18.20 shows “IC/OC Interrupt 0 Operation Example”. As shown in the operation example, disable interrupt requests for all channels once at the last part of an interrupt process, then enable them again.





**Figure 18.20 IC/OC Interrupt 0 Operation Example**

### 18.5.3 Changing Registers ICOCiIC (i = 0, 1)

While the G1IE<sub>j</sub> bit in the G1IE<sub>i</sub> register is 1 (IC/OC interrupt 1 request enabled), use the AND, OR, BCLR, or BSET instruction to change bits ILVL2 to ILVL0 in the ICOCiIC register at the point where a channel j interrupt request may be generated (j = 0 to 7). The IR bit becomes 1 (interrupt requested) if a channel j interrupt is generated while executing these instructions.

If the MOV instruction is used to perform the above, when a channel j interrupt request is generated while executing the MOV instruction, the IR bit does not become 1, and the interrupt request is ignored. The G1IR<sub>j</sub> bit in the G1IR register becomes 1 (interrupt requested) at this timing. If the G1IR<sub>j</sub> remains 1, subsequent IC/OC interrupt i requests are not generated.

When timer S is initialized, change registers ICOCiIC after registers ICOCiIC and G1IR are both set to 00h.

### 18.5.4 Output Waveform During the Base Timer Reset with the BTS bit

When the BTS bit in the G1BCR1 register is set to 0 (base timer reset), the waveform output pin level remains as it is at that point. This output level is held until the base timer value matches the G1PO<sub>j</sub> register value after the BTS bit is set to 1 (base timer starts counting).

### 18.5.5 OUTC1\_0 Pin Output During the Base Timer Reset with the G1PO0 register

While the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset when the base timer matches the G1PO0 register), when the base timer matches the G1PO0 register, the base timer is reset after two fBT1 cycles. During the two fBT1 cycles from when the base timer value matches the G1PO0 register value to the base timer being reset, the OUTC1\_0 pin is driven high. Thus set the EOC0 bit in the G1OER register to 1 (output disabled).

### 18.5.6 Interrupt Request When Selecting Time Measurement Function

When the FSC<sub>j</sub> bit (j = 0 to 7) in the G1FS register is set to 1, and the IFE<sub>j</sub> bit in the G1FE register is also set to 1, the G1IR<sub>j</sub> bit in the G1IR register, or the IR bits in registers ICOCiIC (i = 0, 1) or ICOCHjIC (j = 0 to 3) may become 1 (interrupt requested) after a maximum of two fBT1 cycles.

When using IC/OC interrupt i or IC/OC channel j interrupt, set bits FSC<sub>j</sub> and IFE<sub>j</sub> to 1, then perform the following:

- (1) Wait for two or more fBT1 cycles.
- (2) Set the IR bit in the ICOCiIC register and/or the ICOCHjIC register to 0.
- (3) Wait for three or more fBT1 cycles after the time measurement function is selected. Set the G1IR register to 00h after setting the IR bit in the ICOCiIC register to 0.

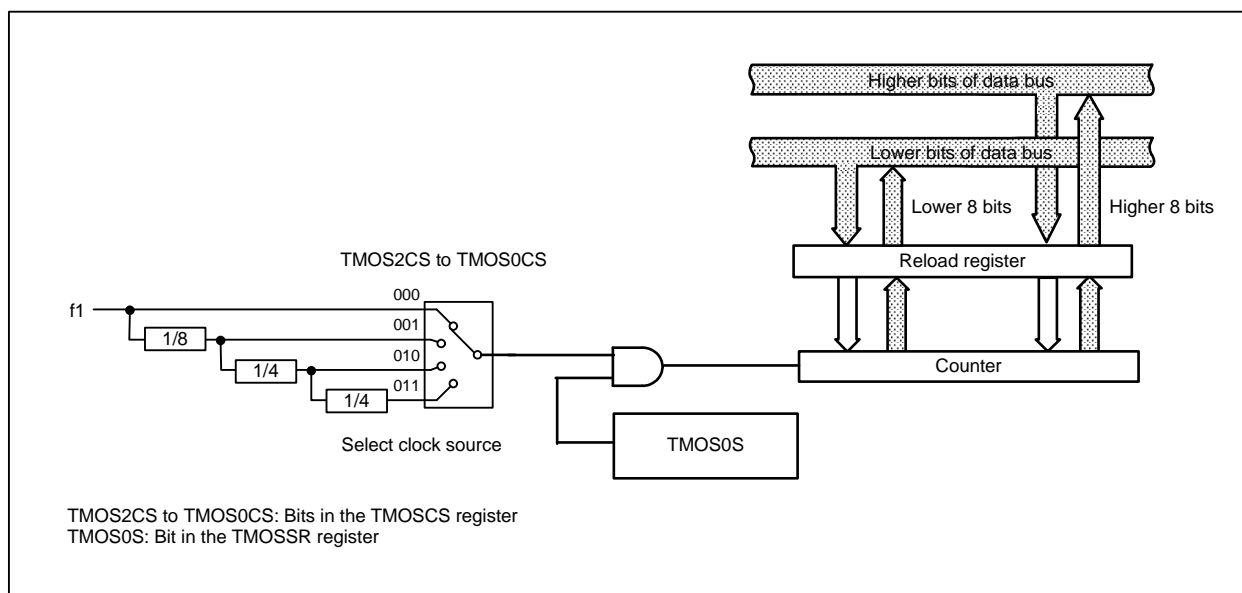
## 19. Task Monitor Timer

### 19.1 Introduction

The task monitor timer has one 16-bit timer to count internal count sources. The TMOSPR register (task monitor timer protect register) has the ability to protect other task monitor timer associated registers.

**Table 19.1 Task Monitor Timer Specifications**

Item	Specification
Count sources	f1, f1 divided-by-8, f1 divided-by-32, f1 divided-by-128
Count operations	<ul style="list-style-type: none"> <li>• Decrement</li> <li>• Reloads the value in the reload register and continues counting when the timer underflows.</li> </ul>
Counter cycle	$(n+1)/f_j$ n: TMOS register setting 0000h to FFFFh, f <sub>j</sub> : count source frequency
Count start condition	Set the TMOS0S bit in the TMOSSR register to 1 (start counting)
Count stop condition	Set the TMOS0S bit to 0 (stop counting)
Interrupt request generation timing	At timer underflow
Read from timer	The timer's count value is read by reading the TMOS register
Write to task monitor timer	<ul style="list-style-type: none"> <li>• When the value is written to the TMOS register while the task monitor timer counter stops, the value is written to both the reload register and the counter.</li> <li>• When the value is written to the TMOS register while the task monitor timer is counting (after setting the TMOS0S bit in the TMOSSR register to 1 (start counting)), the value is written to the reload register and transferred at the next reload timing.</li> </ul>



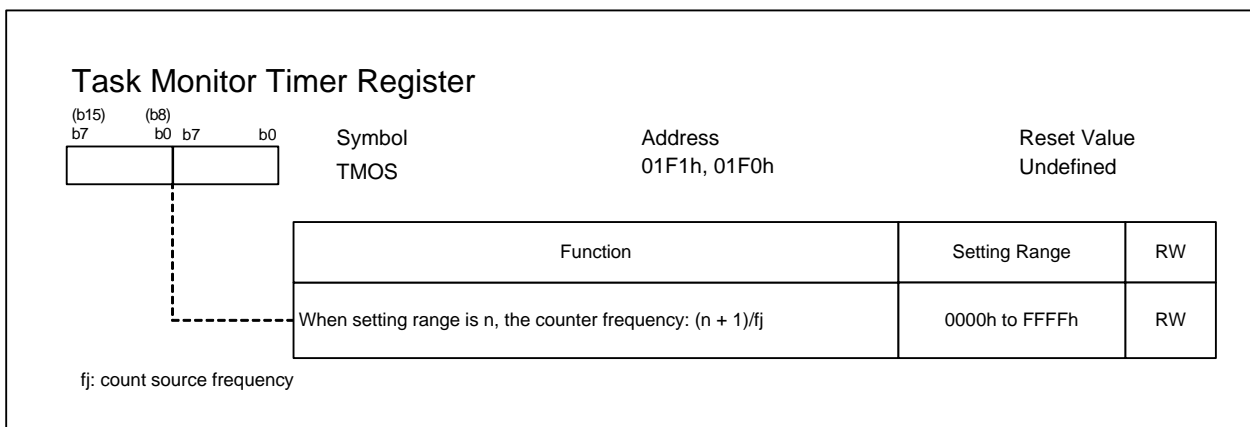
**Figure 19.1 Task Monitor Timer Block Diagram**

## 19.2 Registers

**Table 19.2 Registers**

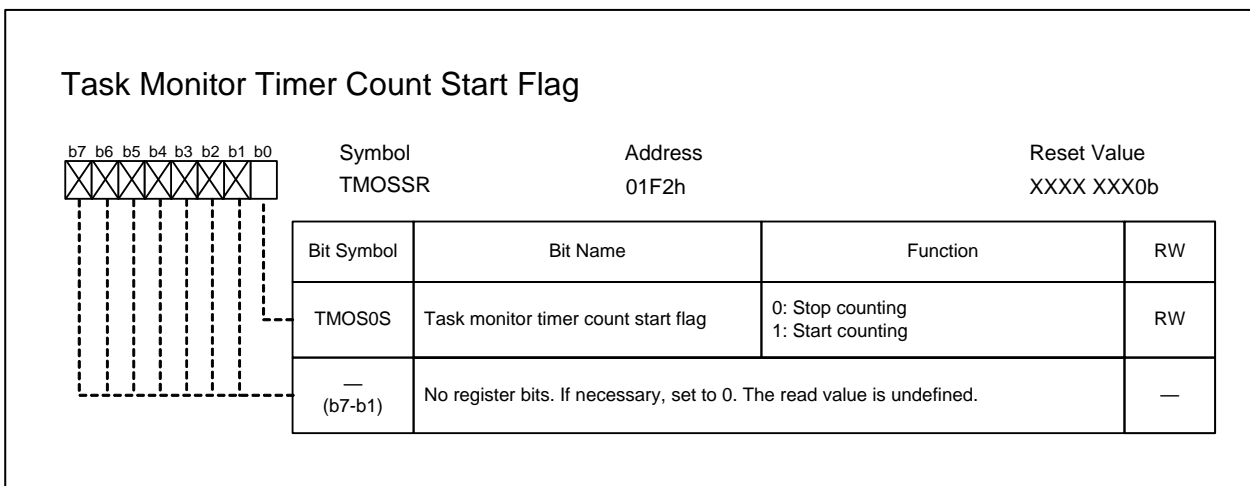
Address	Register Name	Register symbol	Reset Value
01F0h	Task Monitor Timer Register	TMOS	XXh
01F1h			XXh
01F2h	Task Monitor Timer Count Start Flag	TMOSSR	XXXX XXX0b
01F3h	Task Monitor Timer Count Source Select Register	TMOSCS	XXXX 0000b
01F4h	Task Monitor Timer Protect Register	TMOSPR	00h

### 19.2.1 Task Monitor Timer Register (TMOS)

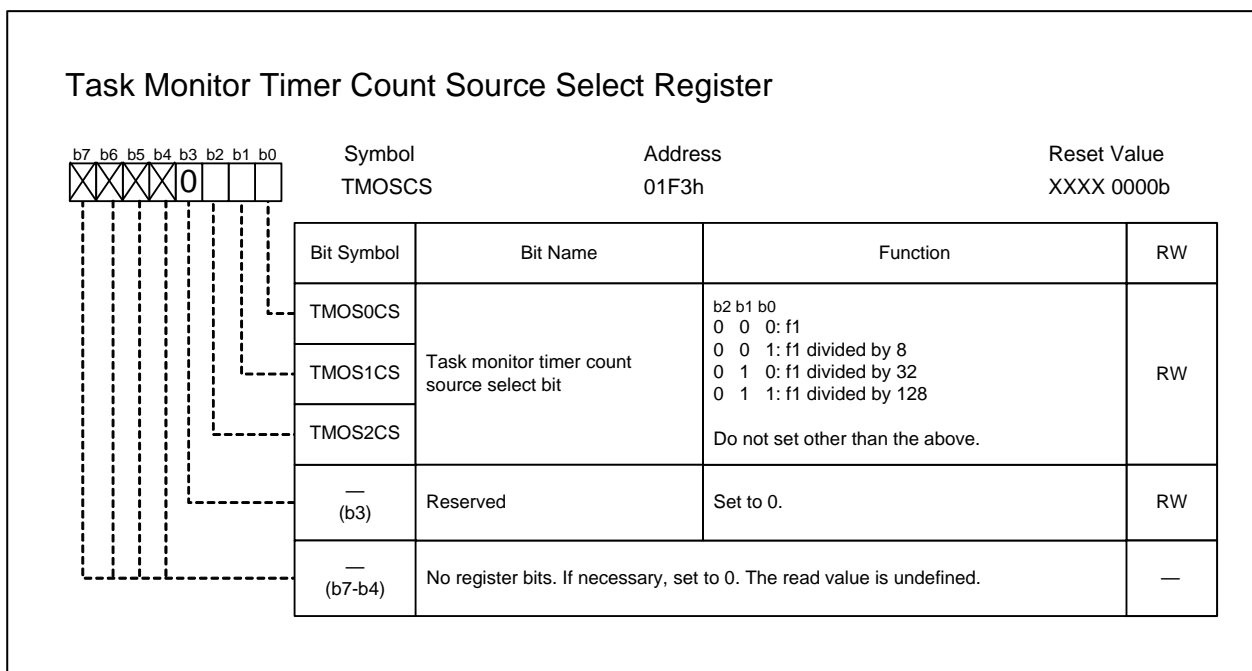


Access the TMOS register in 16-bit units.

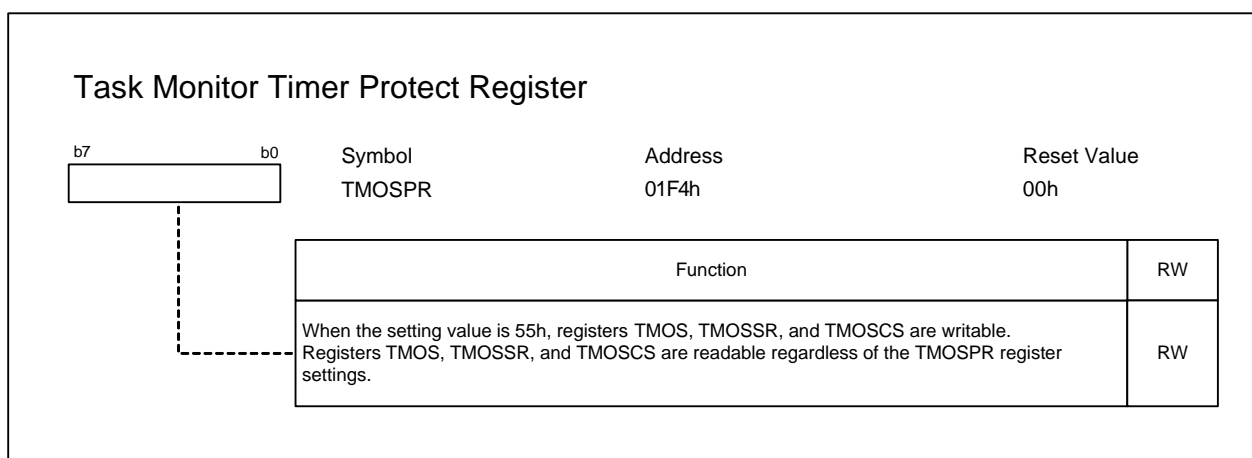
### 19.2.2 Task Monitor Timer Count Start Flag (TMOSSR)



### 19.2.3 Task Monitor Timer Count Source Select Register (TMOSCS)



### 19.2.4 Task Monitor Timer Protect Register (TMOSPR)

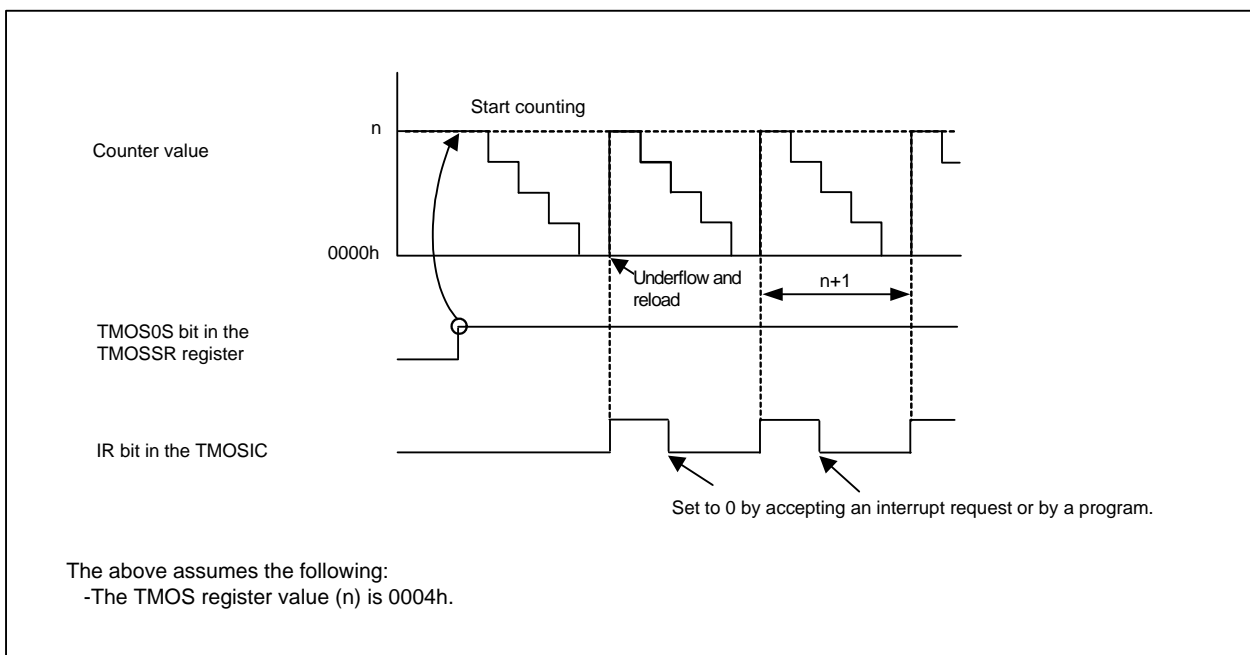


When changing the TMOS, TMOSSR, or TMOSCS register, follow the steps below:

- (1) Write 55h (write enabled) to the TMOSPR register.
- (2) Write a value to the TMOS, TMOSSR, or TMOSCS register as required.
- (3) Write a value other than 55h to the TMOSPR register (write disabled)

### 19.3 Operation

Figure 19.2 shows the Task Monitor Timer Operation.



**Figure 19.2 Task Monitor Timer Operation**

## 19.4 Interrupt

Table 19.3 lists the Task Monitor Timer Interrupt Associated Register.

**Table 19.3 Task Monitor Timer Interrupt Associated Register**

Address	Register Name	Register Symbol	Reset Value
004Ah	Task Monitoring Timer Interrupt Control Register	TMOSIC	XXXX X000b

Task monitor timer shares the interrupt vectors and interrupt control registers with other peripheral functions. When using task monitor timer interrupt, set the IFSR20 bit in the IFSR2A register to 1 (task monitor timer).

## 19.5 Notes on Task Monitor Timer

### 19.5.1 Register Settings

After reset, the task monitor timer counter is stopped. After setting the counter value and count source by setting registers TMOS register and TMOSCS, set the TMOS0S bit in the TMOSSR register to 1 (start counting).

Change the TMOSCS register value when the TMOS0S bit is 0 (stop counting).

### 19.5.2 Reading the Timer

While the task monitor timer is counting, the counter value can be read at any given time by reading the TMOS register. However, when reading the counter at its reload timing, the value is read as FFFFh. When the task monitor timer stops counting and after setting the value to the TMOS register, the setting value can be read until the counter starts counting.



## 20. Real-Time Clock

### 20.1 Introduction

The real-time clock generates a 1-second signal from a count source and counts seconds, minutes, hours, a.m./p.m., a day, and a week. It also detects matches with specified seconds, minutes, and hours. Table 20.1 lists Real-Time Clock Specifications, Figure 20.1 shows a Real-Time Clock Block Diagram, and Table 20.2 lists the I/O Port.

**Table 20.1 Real-Time Clock Specifications**

Item	Specification
Count source	f1, fC
Count operation	<ul style="list-style-type: none"> <li>• Increment</li> <li>• Compare mode 1 or not using compare mode The count value is continuously used, and the count continues.</li> <li>• Compare mode 2 When a compare match is detected, the count value is set to 0 and the count continues.</li> <li>• Compare mode 3 When a compare match is detected, the count value is set to 0 and the count stops.</li> </ul>
Count start condition	1 (count started) is written to the TSTART bit in the RTCCR1 register.
Count stop condition	0 (count stopped) is written to the TSTART bit in the RTCCR1 register.
Interrupt request generation timing	Select one of the following: <ul style="list-style-type: none"> <li>• Update second data</li> <li>• Update minute data</li> <li>• Update hour data</li> <li>• Update day data</li> <li>• When day data is set to 000b</li> <li>• When time data and compare data match</li> </ul>
RTCOUT pin function	Programmable I/O port or compare output
Read from timer	When the RTCSEC, RTCMIN, RTCHR, or RTCWK register is read, the count value can be read. The values read from registers RTCSEC, RTCMIN, and RTCHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the RTCCR1 register are 0 (count stopped), the RTCSEC, RTCMIN, RTCHR, and RTCWK registers are write enabled. Values written to registers RTCSEC, RTCMIN, and RTCHR are represented by the BCD code.
Selectable functions	<ul style="list-style-type: none"> <li>• 12-/24-hour mode switch function</li> <li>• Compare output</li> </ul>

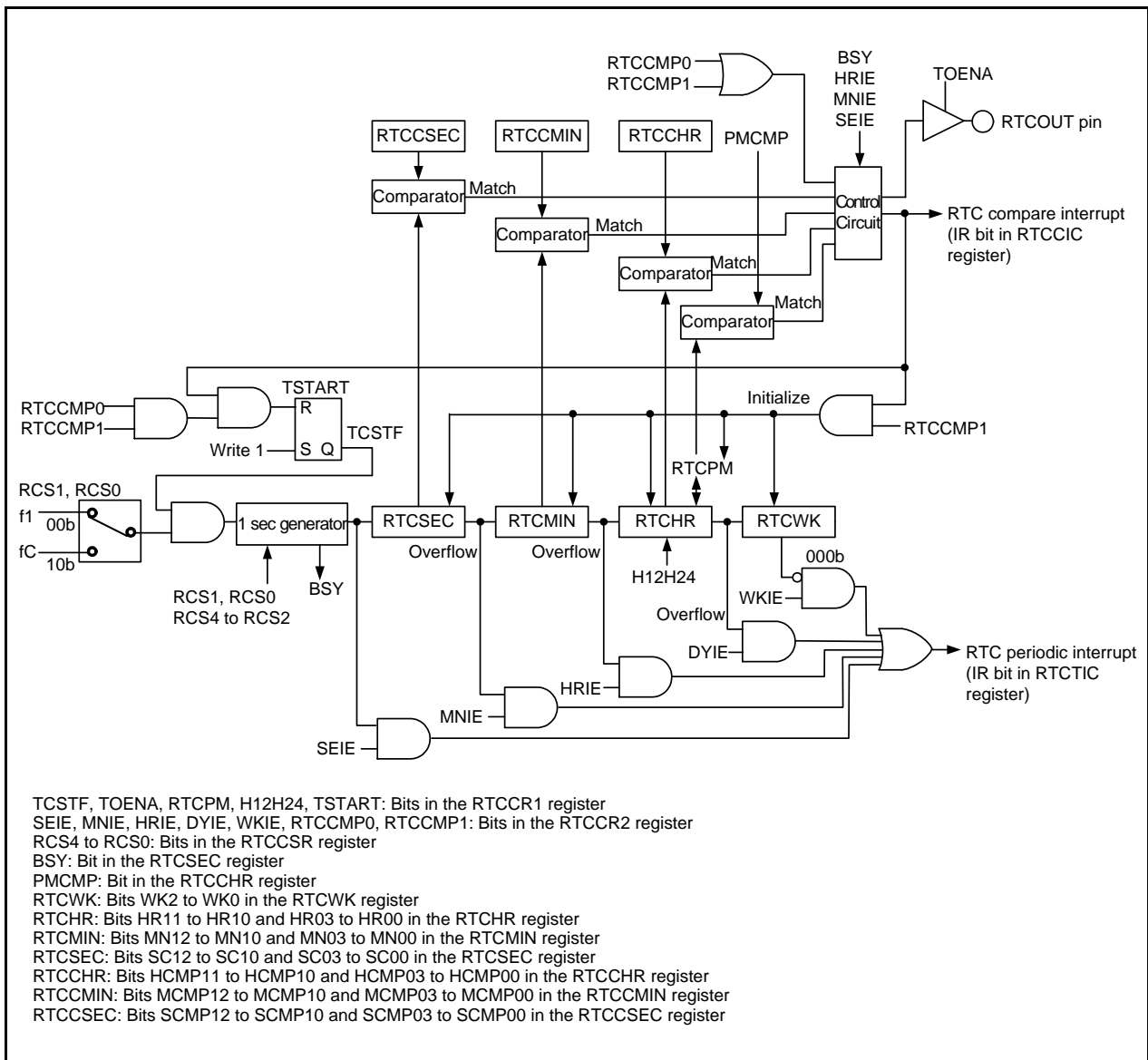


Figure 20.1 Real-Time Clock Block Diagram

Table 20.2 I/O Port

Pin Name	I/O	Function
RTCOUT	Output	Compare output

## 20.2 Registers

**Table 20.3 Registers**

Address	Register	Symbol	Reset Value
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b

### 20.2.1 Real-Time Clock Second Data Register (RTCSEC)

Real-Time Clock Second Data Register		Symbol RTCSEC	Address 0340h	Reset Value 00h								
b7	b6	b5	b4	b3	b2	b1	b0	Bit Symbol	Bit Name	Function	Setting Range	RW
								SC00	First digit of second count bit	Count 0 to 9 every second. When the digit increments, 1 is added to the 2nd digit of second.	0 to 9	RW
							SC01	RW				
							SC02	RW				
							SC03	RW				
								SC10	Second digit of second count bit	When counting 0 to 5, 60 seconds are counted.	0 to 5	RW
							SC11	RW				
							SC12	RW				
								BSY	Real-time clock busy flag	This bit is 1 while registers RTCSEC, RTCMIN, RTCHR or RTCWK are updated.		RO

SC03 to SC00 (First digit of second count bit) (b3-b0)

SC12 to SC10 (Second digit of second count bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.

These bits become 00 at compare match in compare mode 2 and compare mode 3.

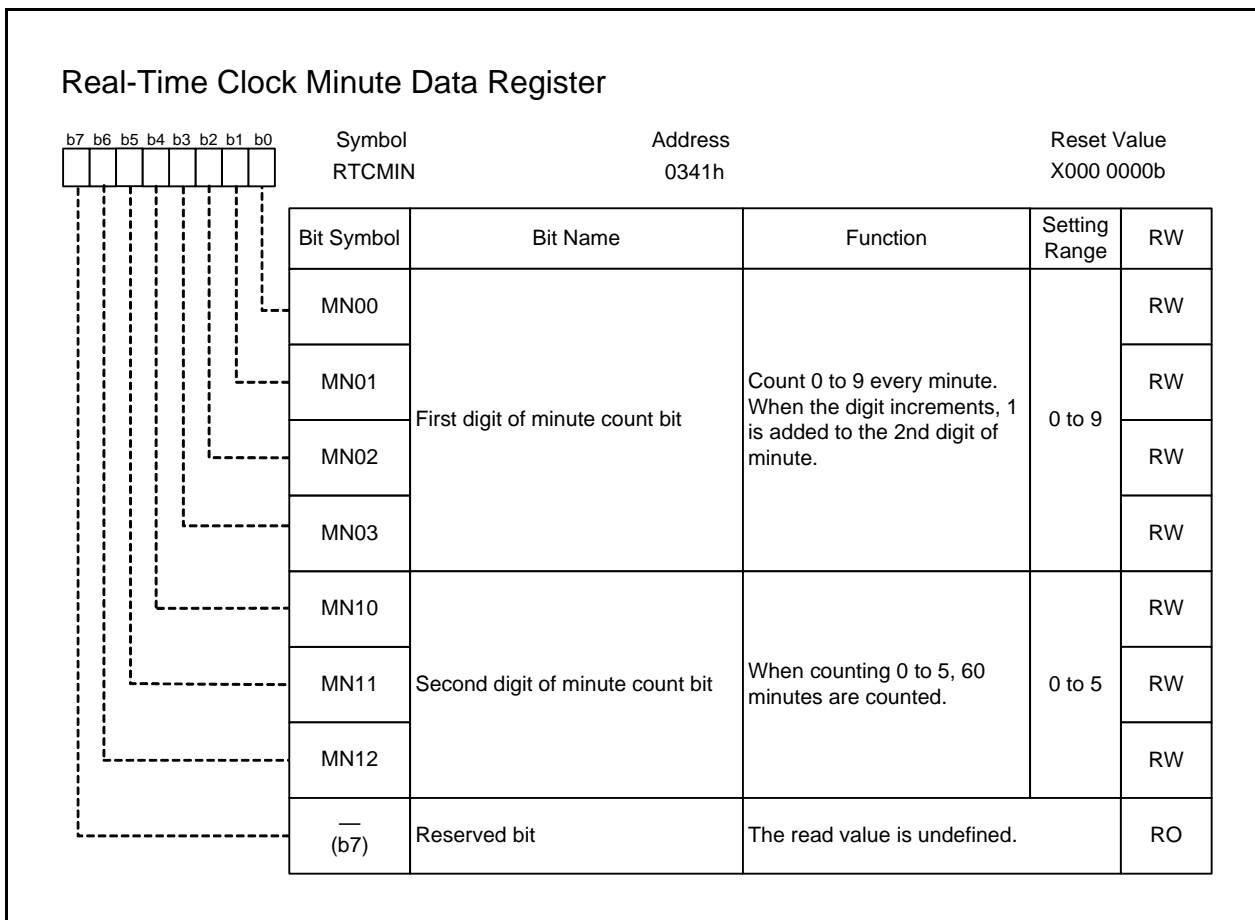
Write to bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit is 0 (not while data is updated).

BSY (Real-time clock busy flag) (b7)

This bit is 1 while data is updated. Read the following bits when the BSY bit is 0 (not while data is updated):

- Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
- Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
- Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
- Bits WK2 to WK0 in the RTCWK register
- The RTCPM bit in the RTCCR1 register

### 20.2.2 Real-Time Clock Minute Data Register (RTCMIN)



MN03 to MN00 (First digit of minute count bit) (b3-b0)

MN12 to MN10 (Second digit of minute count bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.

When the digit increments from the RTCSEC register, 1 is added.

These bits become 00 at compare match in compare mode 2 and compare mode 3.

Write to bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit in the RTCSEC is 0 (not while data is updated).

### 20.2.3 Real-Time Clock Hour Data Register (RTCHR)

Real-Time Clock Hour Data Register				
	Symbol RTCHR	Address 0342h	Reset Value XX00 0000b	
Bit Symbol	Bit Name	Function	Setting Range	RW
HR00	First digit of hour count bit	Count 0 to 9 every hour. When the digit increments, 1 is added to the 2nd digit of hour.	0 to 9	RW
HR01				RW
HR02				RW
HR03				RW
HR10	Second digit of hour count bit	Count 0 to 1 when the H12H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12H24 bit is set to 1 (24-hour mode).	0 to 2	RW
HR11				RW
$\bar{\text{b6}}$	No register bit. If necessary, set to 0. The read value is undefined.			—
$\bar{\text{b7}}$	Reserved bit	The read value is undefined.		RO

HR03 to HR00 (First digit of hour count bit) (b3-b0)

HR11 and HR10 (Second digit of hour count bit) (b5-b4)

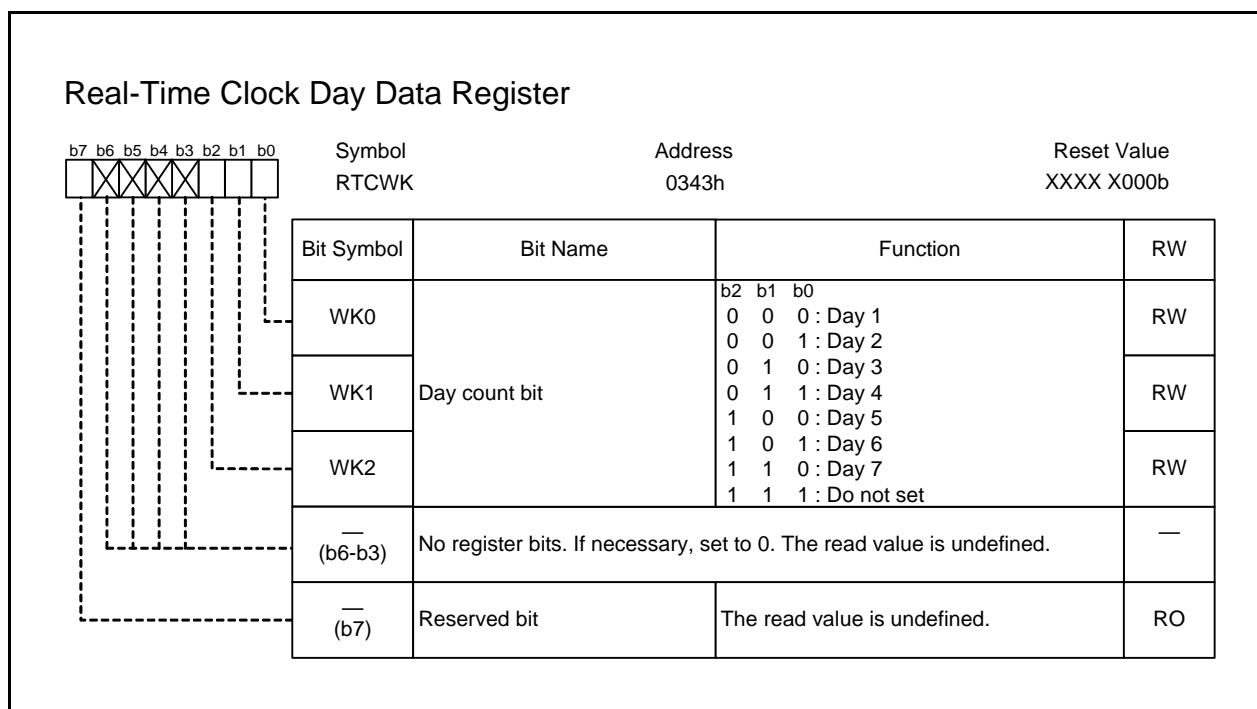
When the H12H24 bit in the RTCCR1 register is 0 (12-hour mode), set a value between 00 and 11 by BCD code. When the H12H24 bit in the RTCCR1 register is 1 (24-hour mode), set a value between 00 and 23 by the BCD code.

When the digit increments from the RTCMIN register, 1 is added.

These bits become 00 at compare match in compare mode 2 and compare mode 3.

Write to bits HR11 to HR10 and HR03 to HR00 in the RTCHR register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

## 20.2.4 Real-Time Clock Day Data Register (RTCWK)



### WK2 to WK0 (Day count bit) (b2-b0)

A week is counted by counting from 000b (Day 1) to 110b (Day 7) repeatedly. Do not set these bits to 111b.

When the digit increments from the RTCHR register, 1 is added.

These bits become 000b at compare match in compare mode 2 and compare mode 3.

Write to bits WK2 to WK0 in the RTCWK register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

## 20.2.5 Real-Time Clock Control Register 1 (RTCCR1)

Real-Time Clock Control Register 1											
b7	b6	b5	b4	b3	b2	b1	b0	Symbol RTCCR1	Address 0344h	Reset Value 0000 X00Xb	
				0			0	Bit Symbol	Bit Name	Function	RW
								$\bar{\text{b0}}$	Reserved bit	Set to 0	RW
								TCSTF	Real-time clock count status flag	0 : Count stopped 1 : Counting	RO
								TOENA	RTCOUT pin output bit	0 : Compare output disabled 1 : Compare output enabled	RW
								$\bar{\text{b3}}$	Reserved bit	Set to 0	RW
								RTCRST	Real-time clock reset bit	Setting this bit to 0 after setting it to 1 resets the real-time clock.	RW
								RTCPM	a.m./p.m. bit	0 : a.m. 1 : p.m.	RW
								H12H24	Operating mode select bit	0 : 12-hour mode 1 : 24-hour mode	RW
								TSTART	Real-time clock count start bit	0 : Count stopped 1 : Count started	RW

TCSTF (Real-time clock count status flag) (b1)

TSTART (Real-time clock count start bit) (b7)

The real-time clock uses the TSTART bit to instruct the count to start or stop, and use the TCSTF bit to indicate count start or stop.

The real-time clock starts counting and the TCSTF bit becomes 1 (count started) when the TSTART bit is set to 1 (count started). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock <sup>(1)</sup> other than the TCSTF bit.

Also, when setting the TSTART bit to 0 (count stopped), the real-time clock stops counting and the TCSTF bit becomes 0 (count stopped). It takes the time for up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock <sup>(1)</sup> other than the TCSTF bit.

Note:

1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.



**RTCRST (Real-Time clock reset bit) (b4)**

When setting this bit to 0 after setting it to 1, the following are set automatically:

- The values are reset in registers RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.
- Bits TCSTF, RTCPM, H12H24, and TSTART in the RTCCR1 register become 0.

**RTCPM (a.m./p.m. bit) (b5)**

Write to the RTCPM bit when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped). Read this bit when the BSY bit in the RTCSEC register is 0 (not while data is updated).

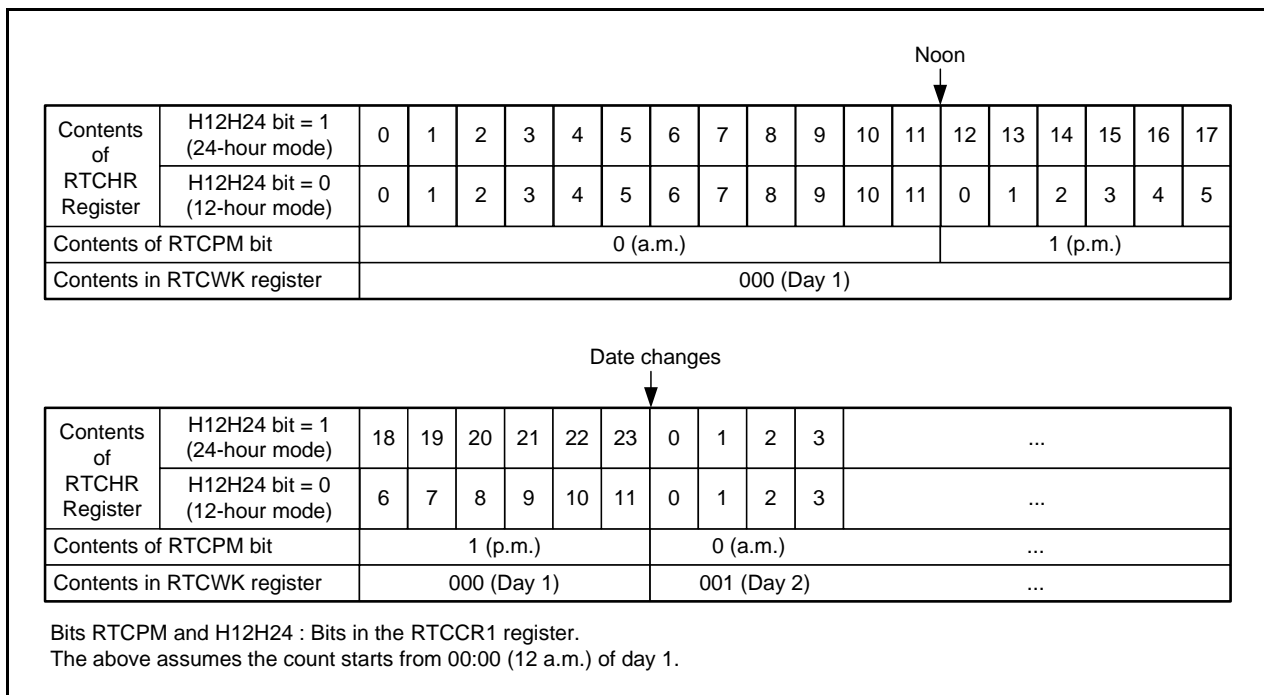
The RTCPM bit is enabled when the H12H24 bit is 0 (12-hour mode) or 1 (24-hour mode). Set the RTCPM bit as shown below to set the time while the H12H24 bit is 1:

- Set the RTCPM bit to 0 when bits HR11 to HR10 and HR03 to HR00 in the RTCHR register are 00 to 11.
- Set the RTCPM bit to 1 when bits HR11 to HR10 and HR03 to HR00 in the RTCHR register are 12 to 23.

The RTCPM bit changes as follows while counting:

- Becomes 0 when the RTCPM bit is 1 (p.m.) while the clock increments from 11:59:59 (23:59:59 for 24-hour mode) to 00:00:00.
- Becomes 1 when the RTCPM bit is 0 (a.m.) while the clock increments from 11:59:59 to 00:00:00 (12:00:00 for 24-hour mode).

Figure 20.2 shows Time Representation.



**Figure 20.2 Time Representation**

**H12H24 (Operating mode select bit) (b6)**

Write to the H12H24 bit when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped).

## 20.2.6 Real-Time Clock Control Register 2 (RTCCR2)

Real-Time Clock Control Register 2			
	Symbol RTCCR2	Address 0345h	Reset Value X000 0000b
b7	b6	b5	b4
b3	b2	b1	b0
Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit	0 : Disable periodic interrupt triggered every second 1 : Enable periodic interrupt triggered every second	RW
MNIE	Periodic interrupt triggered every minute enable bit	0 : Disable periodic interrupt triggered every minute 1 : Enable periodic interrupt triggered every minute	RW
HRIE	Periodic interrupt triggered every hour enable bit	0 : Disable periodic interrupt triggered every hour 1 : Enable periodic interrupt triggered every hour	RW
DYIE	Periodic interrupt triggered every day enable bit	0 : Disable periodic interrupt triggered every day 1 : Enable periodic interrupt triggered every day	RW
WKIE	Periodic interrupt triggered every week enable bit	0 : Disable periodic interrupt triggered every week 1 : Enable periodic interrupt triggered every week	RW
RTCCMP0	Compare mode select bit	b6 b5 0 0 : No compare mode 0 1 : Compare mode 1 1 0 : Compare mode 2 1 1 : Compare mode 3	RW
RTCCMP1			RW
— (b7)	No register bit. If necessary, set to 0. The read value is undefined.		—

Write to the RTCCR2 register when bits TSTART and TCSTF in the RTCCR1 register are both 0 (count stopped).

While bits RTCCMP1 to RTCCMP0 are 00b (no compare mode), an interrupt request can be generated every second, minute, hour, day, or week. To generate an interrupt request, set one of the following bits to 1 (interrupt enabled): SEIE, MNIE, HRIE, DAYIE, or WKIE. (Do not set more than one bit to 1.) Table 20.4 lists Periodic Interrupt Sources.

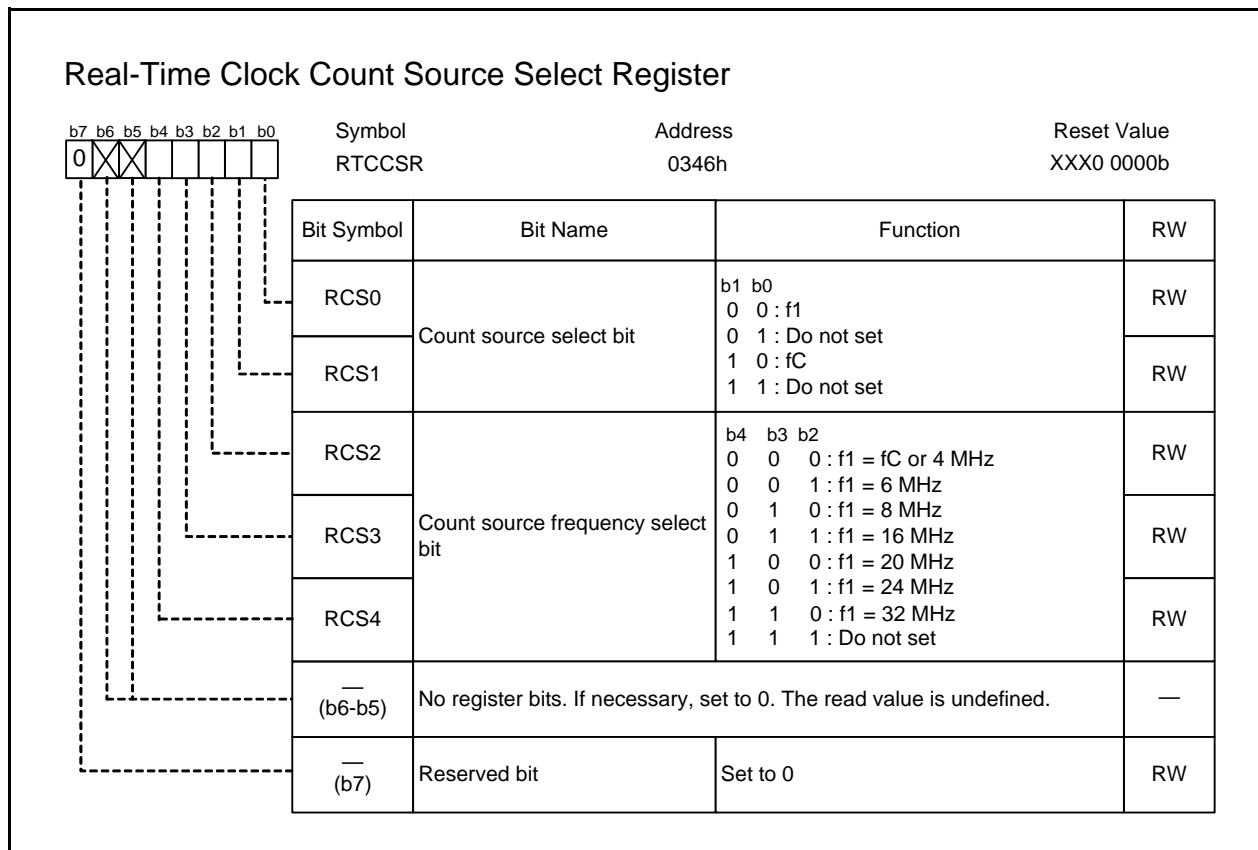
**Table 20.4** Periodic Interrupt Sources

Factor	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	Value in RTCWK register is set to 000b (1-week period)	WKIE
Periodic interrupt triggered every day	RTCWK register is updated (1-day period)	DYIE
Periodic interrupt triggered every hour	RTCHR register is updated (1-hour period)	HRIE
Periodic interrupt triggered every minute	RTCCMIN register is updated (1-minute period)	MNIE
Periodic interrupt triggered every second	RTCCSEC register is updated (1-second period)	SEIE

When bits RTCCMP1 to RTCCMP0 are 01b, 10b, or 11b (any compare mode), set the following according to which registers are compared:

- When comparing to the RTCCSEC register, set the SEIE bit to 1 (interrupt enabled).
- When comparing to the RTCCMIN register, set bits SEIE and MNIE to 1.
- When comparing to the RTCCCHR register, set bits SEIE, MNIE, and HRIE to 1.

### 20.2.7 Real-Time Clock Count Source Select Register (RTCCSR)



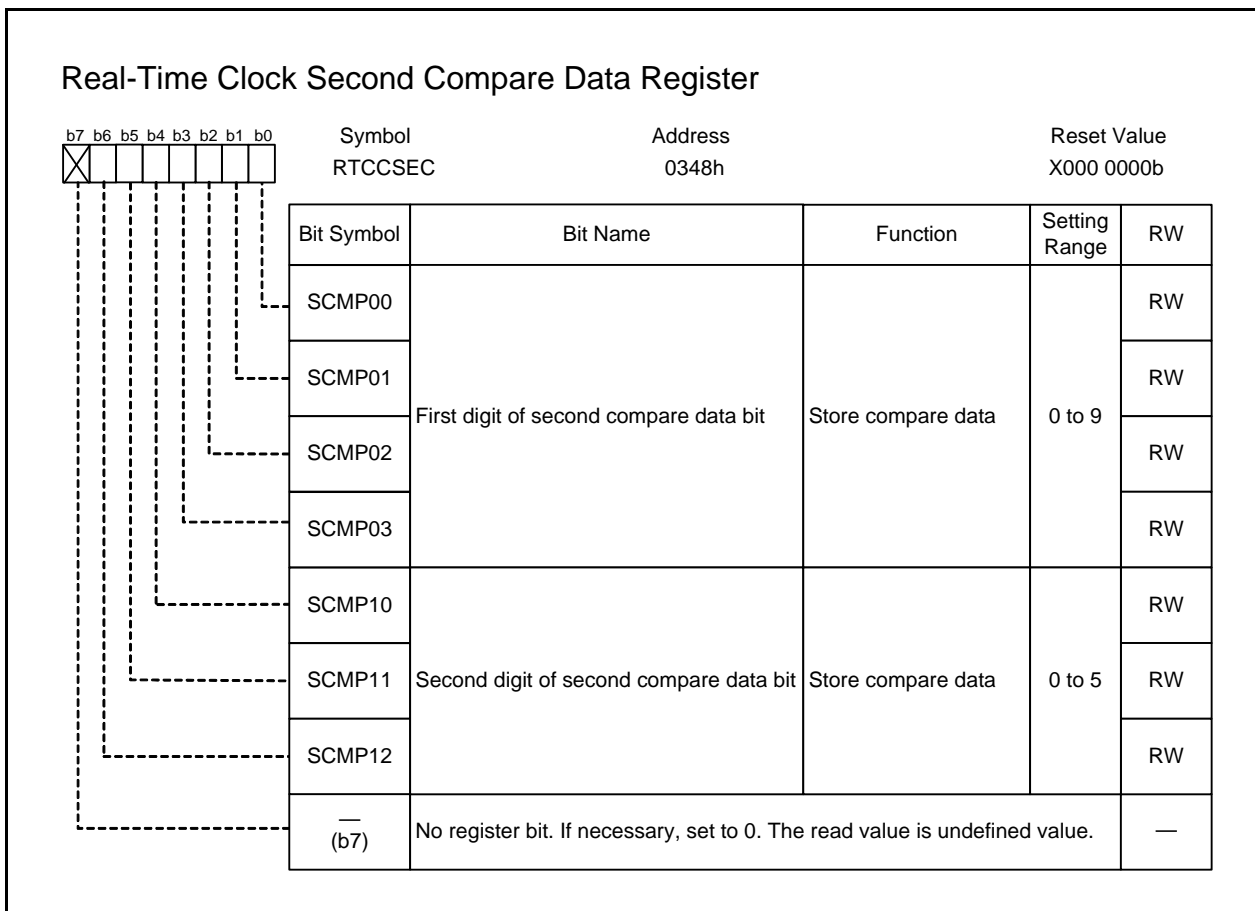
When bits RCS1 to RCS0 are 10b (fC), set bits RCS4 to RCS2 to 000b.

When bits RCS1 to RCS0 are 00b (f1), select a frequency matched to f1 by bits RCS4 to RCS2.

Write to the RTCCSR register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (count stopped).

When using fC, set the PM25 bit in the PM2 register to 1 (peripheral clock fC provided). Refer to 8. "Clock Generator" for details on fC.

### 20.2.8 Real-Time Clock Second Compare Data Register (RTCCSEC)



The RTCCSEC register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

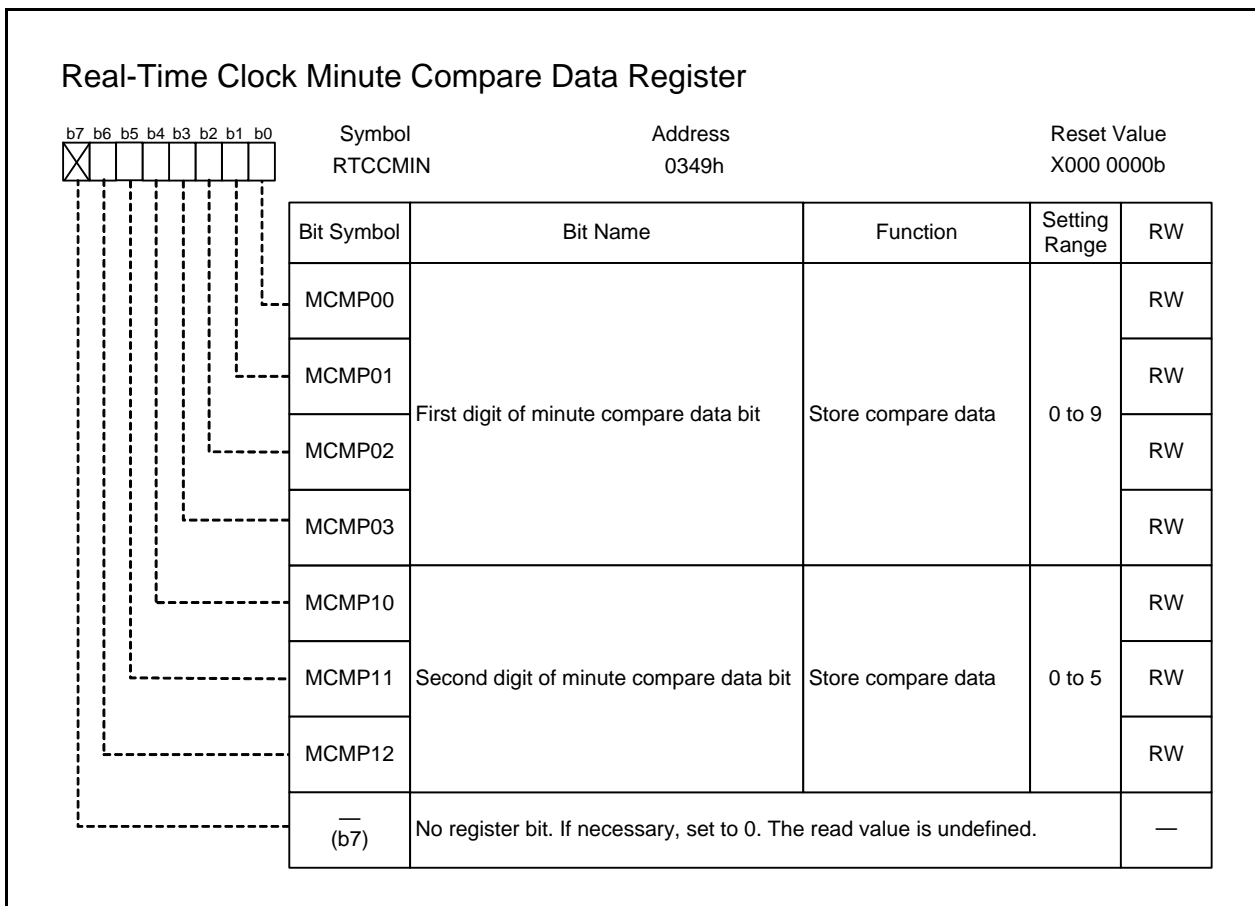
SCMP03 to SCMP00 (First digit of second compare data bit) (b3-b0)

SCMP12 to SCMP10 (Second digit of second compare data bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.

Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

### 20.2.9 Real-Time Clock Minute Compare Data Register (RTCCMIN)



The RTCCMIN register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

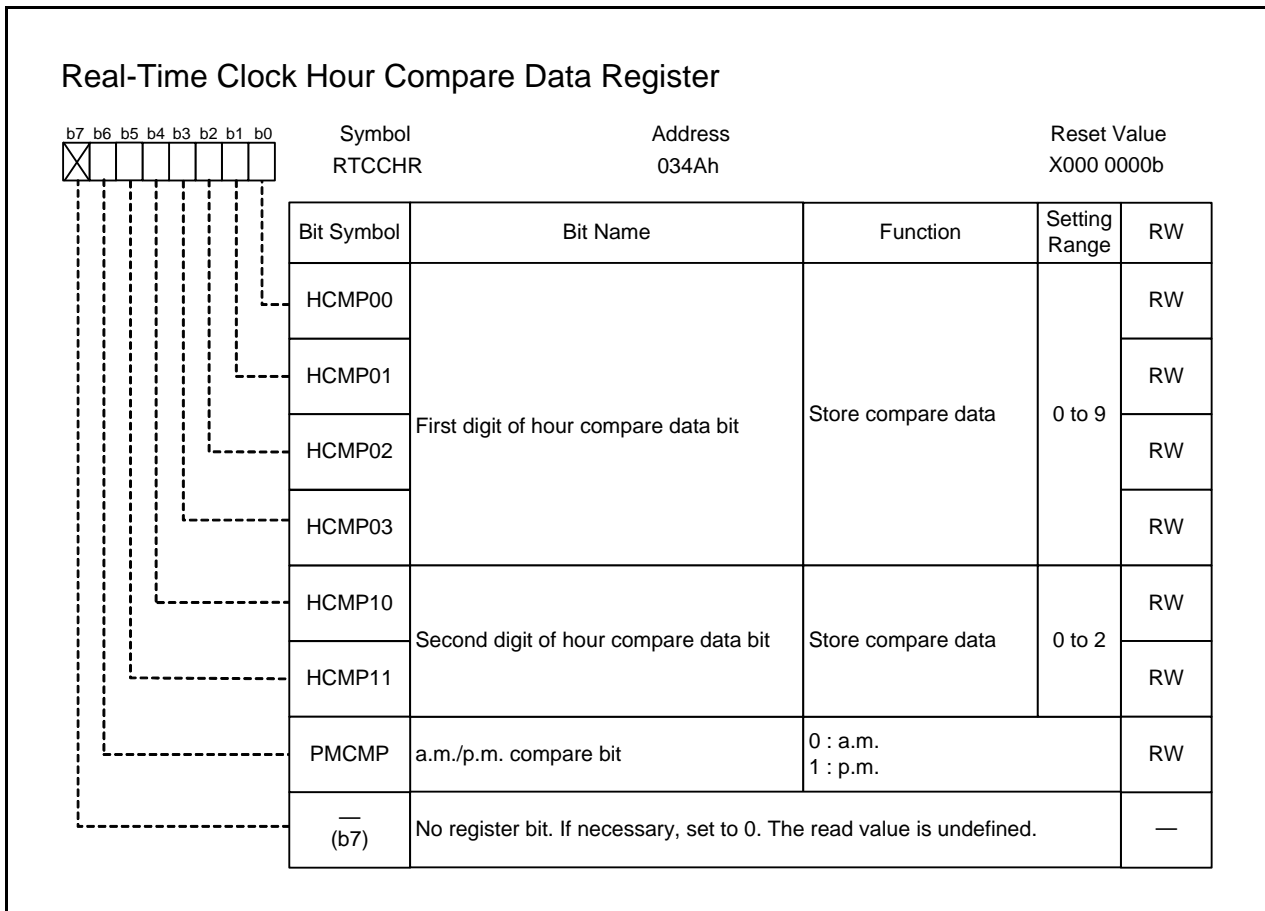
MCMP03 to MCMP00 (First digit of minute compare data bit) (b3-b0)

MCMP12 to MCMP10 (Second digit of minute compare data bit) (b6-b4)

Set a value between 00 and 59 by the BCD code.

Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

### 20.2.10 Real-Time Clock Hour Compare Data Register (RTCCHR)



The RTCCHR register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

**HCMP03-HCMP00 (First digit of hour compare data bit) (b3-b0)**

**HCMP11-HCMP10 (Second digit of hour compare data bit) (b5-b4)**

When the H12H24 bit in the RTCCR1 register is 0 (12-hour mode), set a value between 00 and 11 by the BCD codes. When the H12H24 bit in the RTCCR1 register is 1 (24-hour mode), set a value between 00 and 23 by the BCD codes.

Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

**PMCMP (a.m./p.m compare bit) (b6)**

This bit is enabled when the H12H24 bit in the RTCCR1 register is either 0 (12-hour mode) or 1 (24-hour mode). When the H12H24 bit is 1, set the following:

- When bits HCMP11 to HCMP10 and HCMP03 to HCMP00 are 00 to 11, set the PMCMP bit to 0.
- When bits HCMP11 to HCMP10 and HCMP03 to HCMP00 are 12 to 23, set the PMCMP bit to 1.

Write to this bit when the BSY bit in the RTCSEC register is 0 (not while data is updated).

## 20.3 Operations

### 20.3.1 Basic Operation

The real-time clock generates a 1-second signal from the count source selected in the RTCCSR register and counts seconds, minutes, hours, a.m./p.m., a day, and a week.

The day and time to start the count can be set using registers RTCSEC, RTCMIN, RTCHR, RTCWK, and the RTCPM bit in the RTCCR1 register. Current time and day are read from registers RTCSEC, RTCMIN, RTCHR, RTCWK, and the RTCPM bit in the RTCCR1 register. However, do not read these registers when the BSY bit in the RTCSEC register is 1 (while data is updated).

An interrupt request can be generated every second, minute, hour, day, or week. While bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 00b (no compare mode), use the RTCCR2 register to enable one of the periodic interrupts triggered every second, minute, hour, day and week. When a periodic interrupt is generated, the IR bit in the RTCTIC register becomes 1 (interrupt request).

Figure 20.3 shows Real-Time Clock Basic Operating Example, Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare Mode 1), and Figure 20.5 shows Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3).

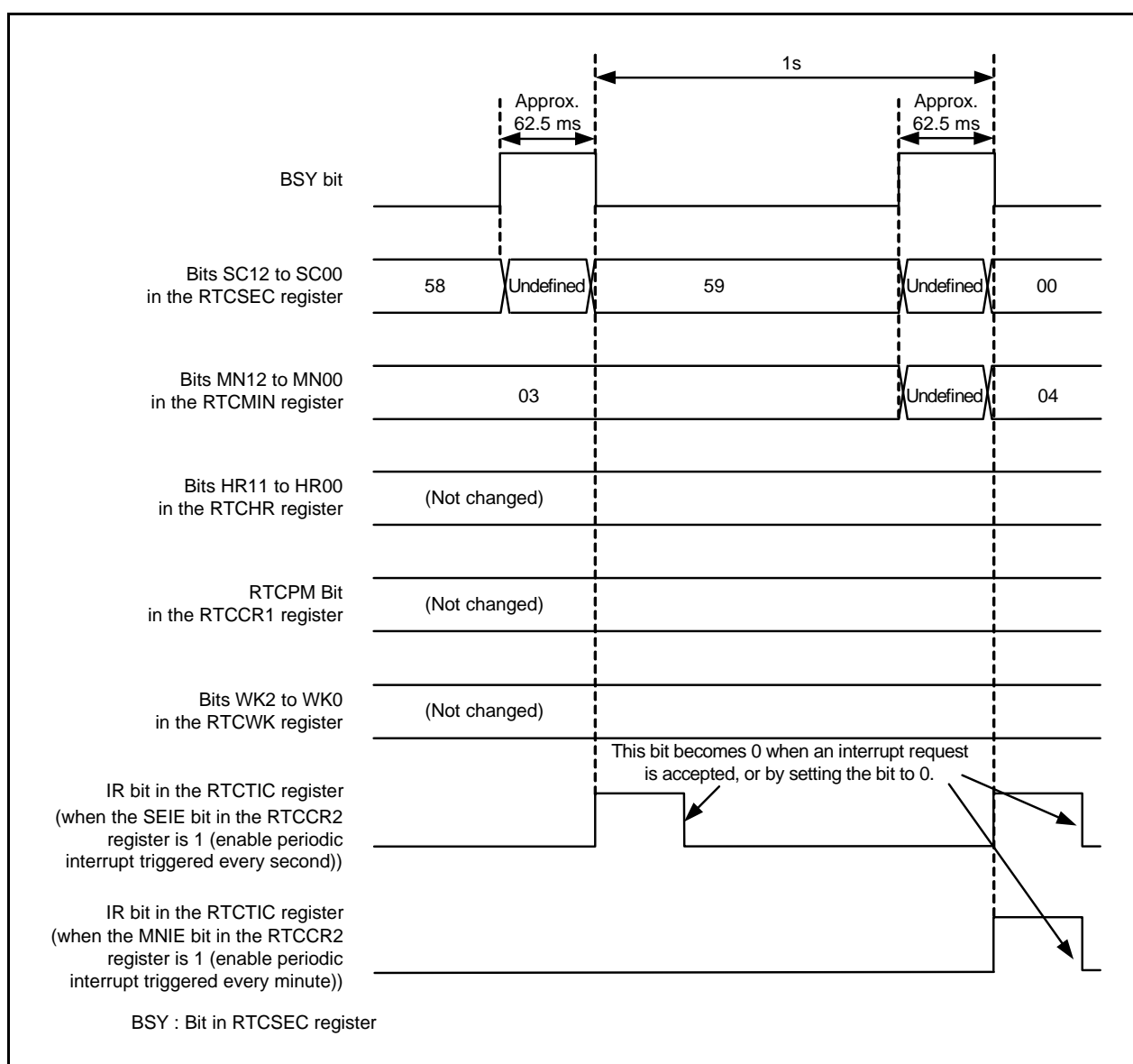


Figure 20.3 Real-Time Clock Basic Operating Example



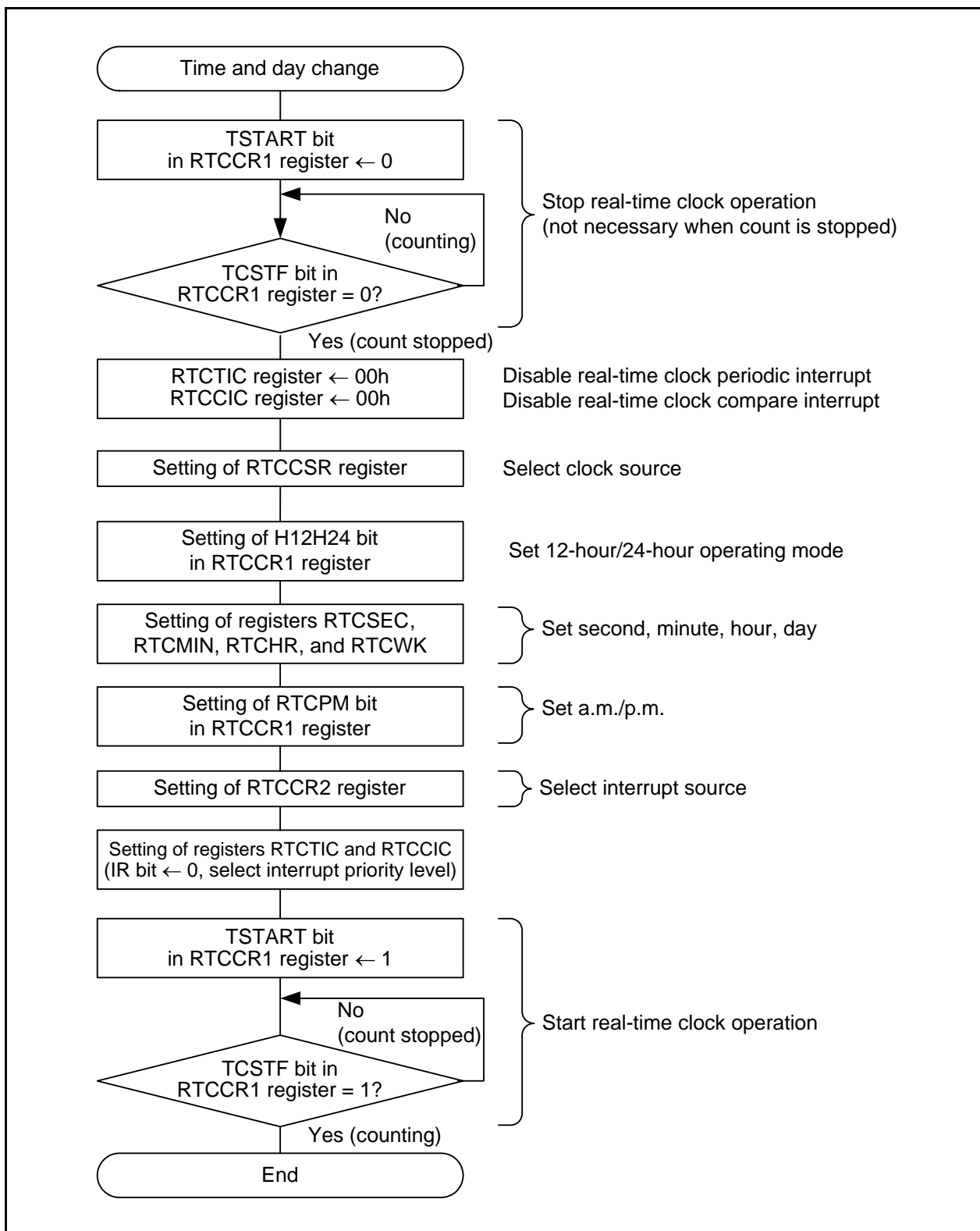


Figure 20.4 Time and Day Change Procedure (No Compare Mode or Compare Mode 1)

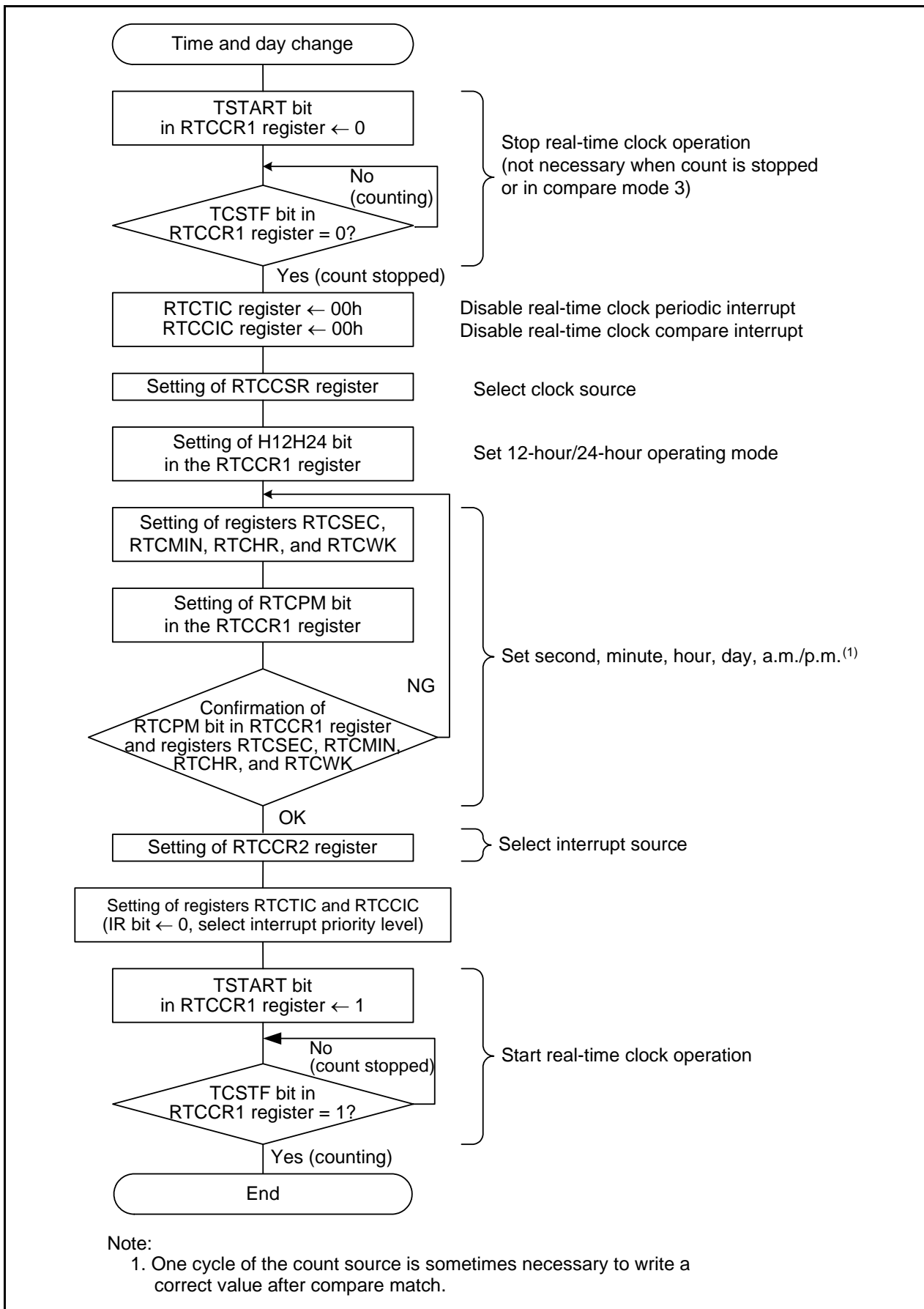


Figure 20.5 Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3)

### 20.3.2 Compare Mode

In compare mode, time data <sup>(1)</sup> and compare data <sup>(2)</sup> are compared, and a compare match is detected.

When a match is detected, the following occur:

- Compare interrupt request  
Refer to 20.4 “Interrupts” for details.
- RTCOUT pin output level inversion  
When the TOENA bit in the RTCCR1 register is 1 (compare output enabled), if a compare match is detected, the RTCOUT pin output level is inverted.

Notes:

1. Bits for time data are as follows:  
Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register  
Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register  
Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register  
The RTCPM bit in the RTCCR1 register
2. Bits for compare data are as follows:  
Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register  
Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register  
Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register  
The PMCMP bit in the RTCCHR register

In compare mode, set the SEIE, MNIE, or HRIE bit in the RTCCR2 register to 1 (interrupt enabled) according to compare data (second, minute, or hour). Refer to 20.2.6 “Real-Time Clock Control Register 2 (RTCCR2)” for details.

Compare mode has three modes: compare mode 1, compare mode 2, and compare mode 3. Operation after a compare match differs depending on the compare mode.

- Compare mode 1  
The time data is used continuously and counting continues.
- Compare mode 2  
The reset value is used as the time data and counting continues.
- Compare mode 3  
The reset value is used as the time data and counting stops.

Figure 20.6 shows Difference between Compare Modes, Figure 20.7 shows Count Start/Stop Operating Example, Figure 20.8 shows Compare Mode 1 Operating Example, Figure 20.9 shows Compare Mode 2 Operating Example, and Figure 20.10 shows Compare Mode 3 Operating Example.

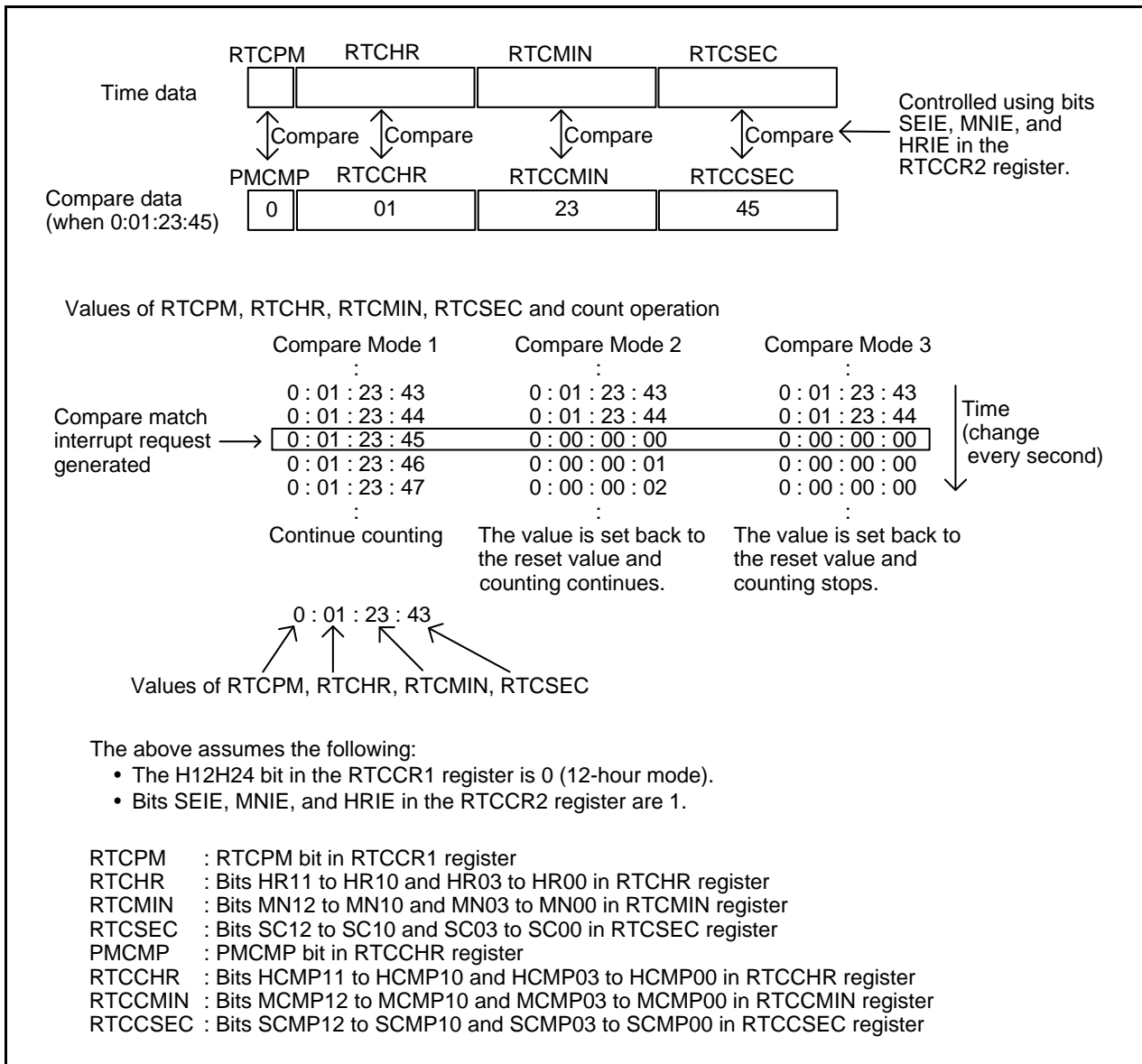


Figure 20.6 Difference between Compare Modes

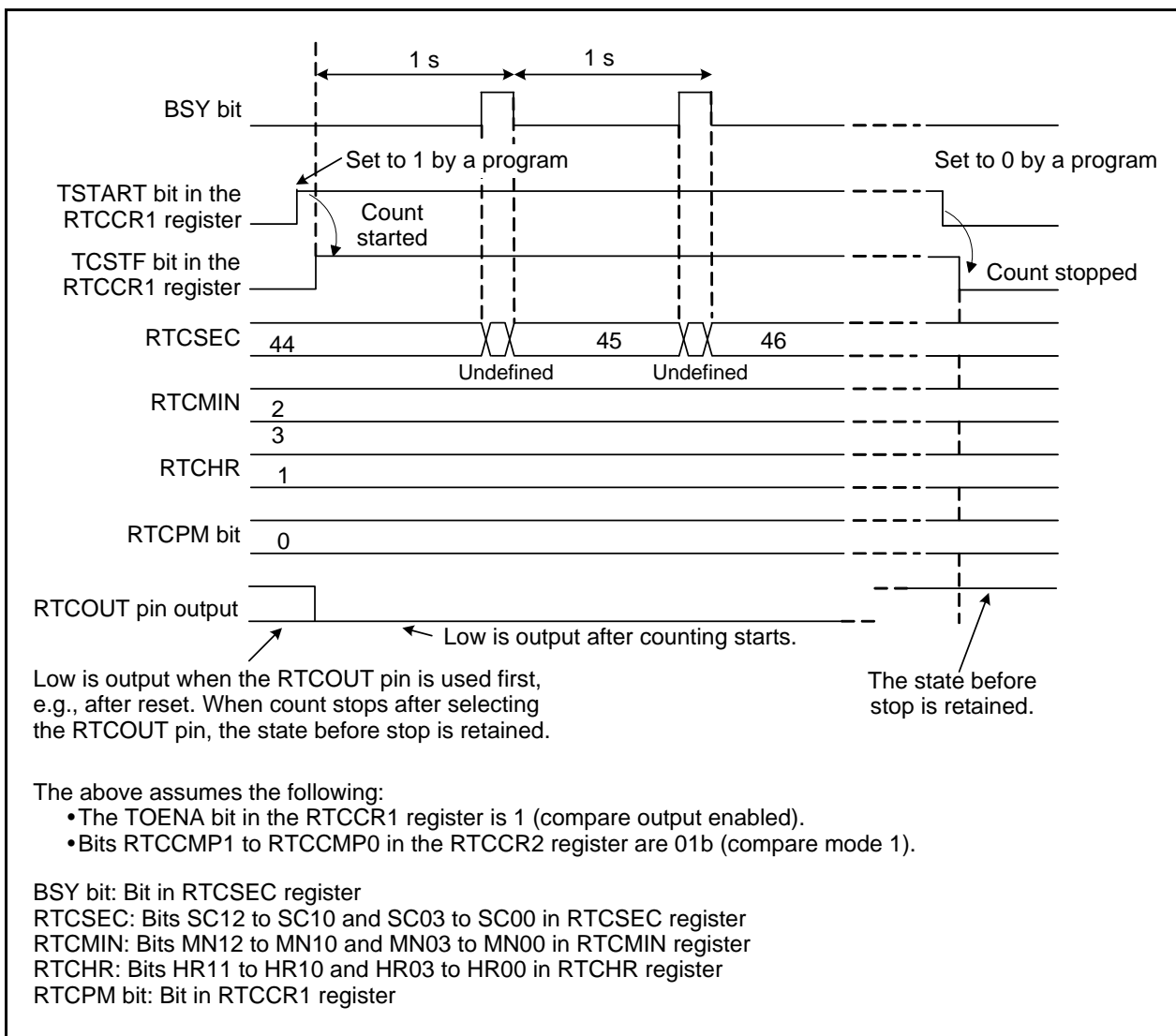


Figure 20.7 Count Start/Stop Operating Example

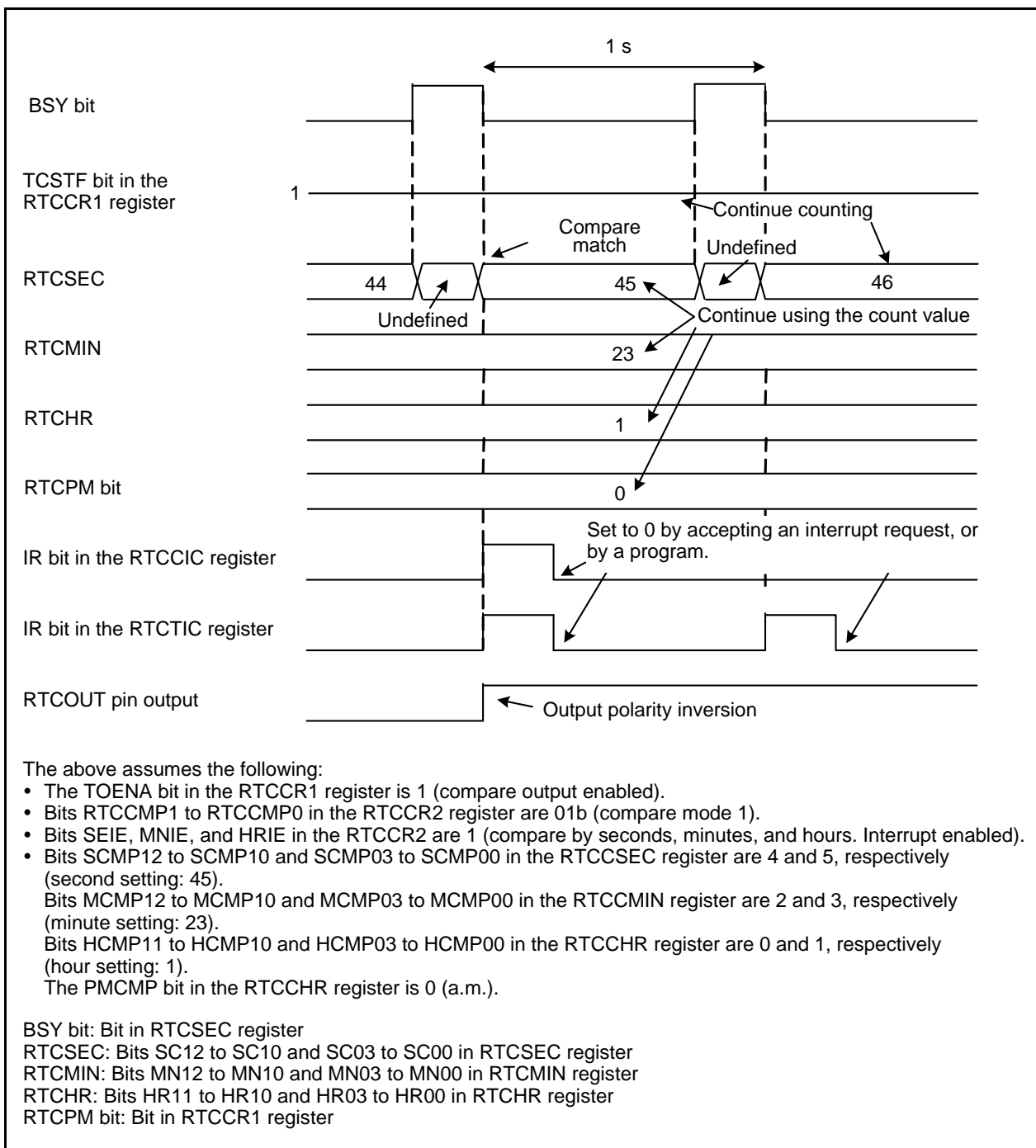


Figure 20.8 Compare Mode 1 Operating Example

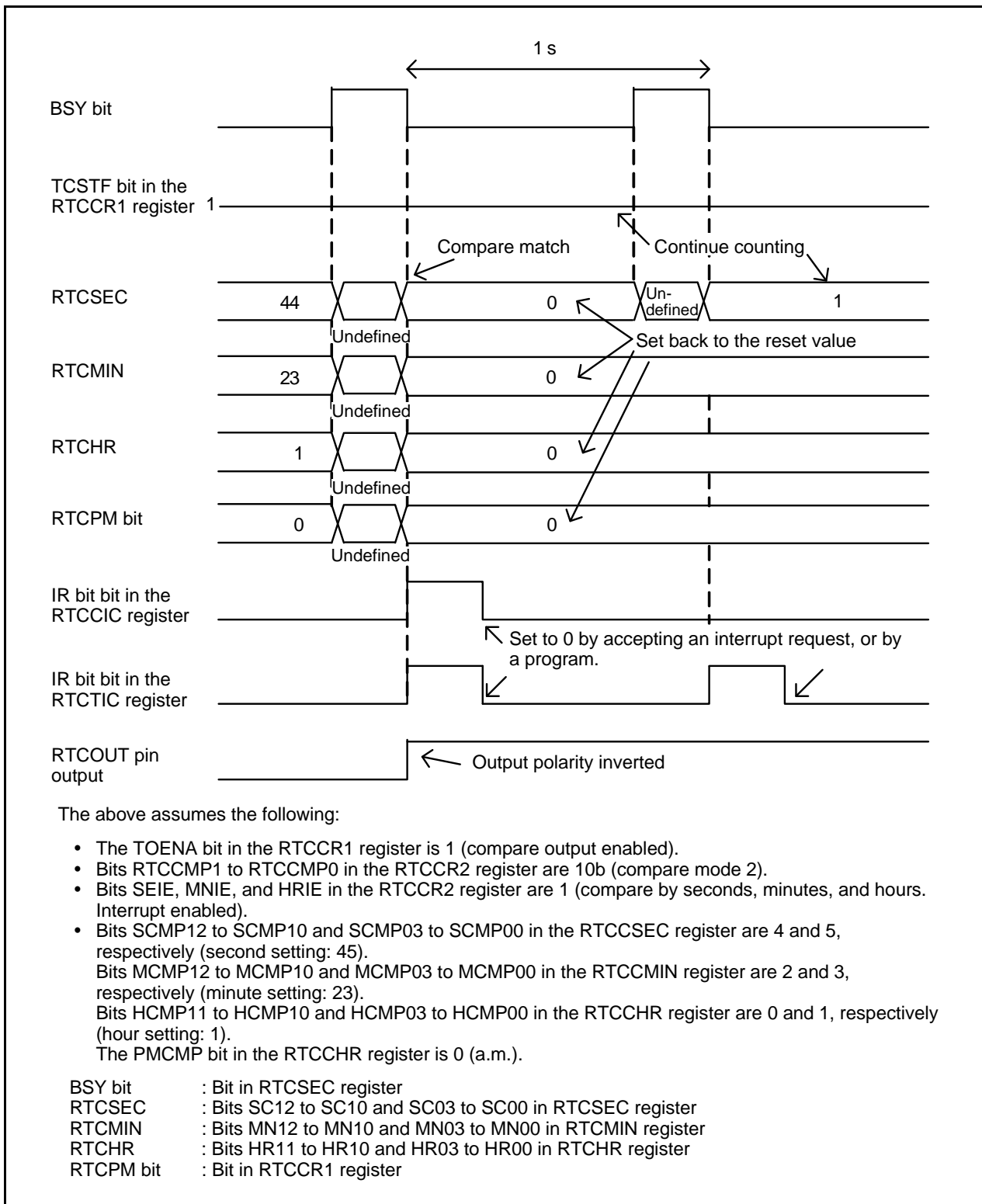
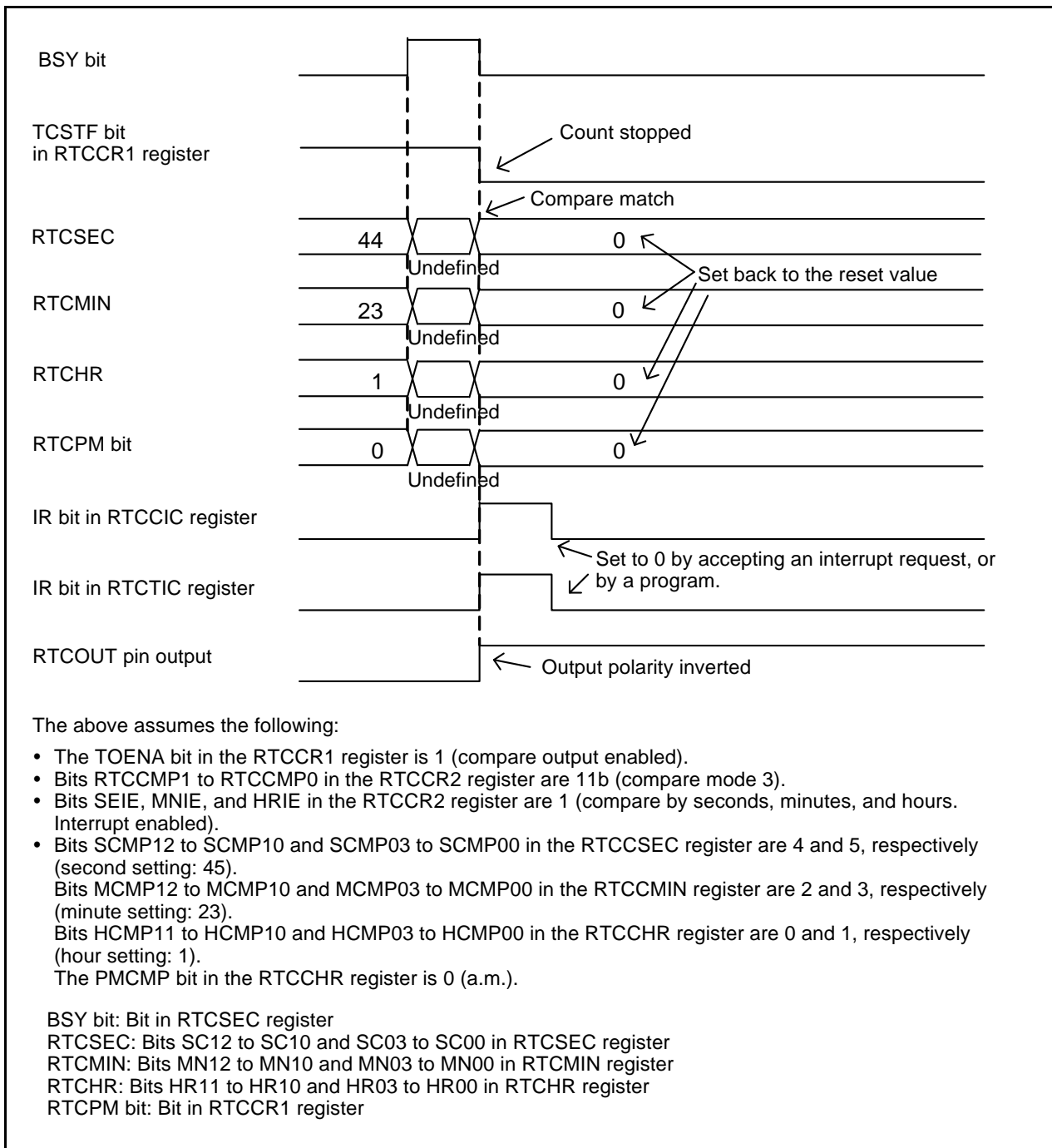


Figure 20.9 Compare Mode 2 Operating Example



**Figure 20.10 Compare Mode 3 Operating Example**



## 20.4 Interrupts

The real-time clock generates two types of interrupt:

- Periodic interrupts triggered every second, minute, hour, day, and week
- Compare match interrupt

See Table 20.4 Periodic Interrupt Sources for details on periodic interrupt sources, individual mode specifications and an operating example for the interrupt request generating timing. Refer to 12.7 “Interrupt Control” for details of interrupt control. Table 20.5 lists Real-Time Clock Interrupt-Associated Registers.

**Table 20.5 Real-Time Clock Interrupt-Associated Registers**

Address	Register	Symbol	Reset Value
006Fh	Real-Time Clock Compare Interrupt Control Register	RTCCIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register	RTCTIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h

The real-time clock shares interrupt vectors and interrupt control registers with other peripheral functions. To use compare interrupts, set the IFSR36 bit in the IFSR3A register to 1 (real-time clock compare).

## 20.5 Notes on Real-Time Clock

### 20.5.1 Starting and Stopping the Count

The real-time clock uses the TSTART bit for instructing the count to start or stop, and the TCSTF bit which indicates count started or stopped. Bits TSTART and TCSTF are in the RTCCR1 register.

The real-time clock starts counting and the TCSTF bit becomes 1 (count started) when the TSTART bit is set to 1 (count started). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock <sup>(1)</sup> other than the TCSTF bit.

Similarly, when setting the TSTART bit to 0 (count stopped), the real-time clock stops counting and the TCSTF bit becomes 0 (count stopped). It takes up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock other than the TCSTF bit.

Note:

1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

### 20.5.2 Register Settings (Time Data, etc.)

Write to the following registers/bits when the real-time clock is stopped:

- Registers RTCSEC, RTCMIN, RTCHR, RTCWK, and RTCCR2
- Bits H12H24 and RTCPM in the RTCCR1 register
- Bits RCS0 to RCS4 in the RTCCSR register

The real-time clock is stopped when bits TSTART and TCSTF in the RTCCR1 register are 0 (real-time clock stopped).

Set the RTCCR2 register after setting the registers and bits mentioned above (immediately before the real-time clock count starts).

Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare Mode 1), and Figure 20.5 shows Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3).

### 20.5.3 Register Settings (Compare Data)

Write to the following registers when the BSY bit in the RTCSEC register is 0 (not while data is updated).

- Registers RTCCSEC, RTCCMIN, and RTCCHR

### 20.5.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read time data bits <sup>(1)</sup> when the BSY bit in the RTCSEC register is 0 (not while data is updated).

When reading multiple registers, if data is rewritten between reading registers, an errant time will be read. To prevent this, use one of the following steps when reading:

- Using an interrupt

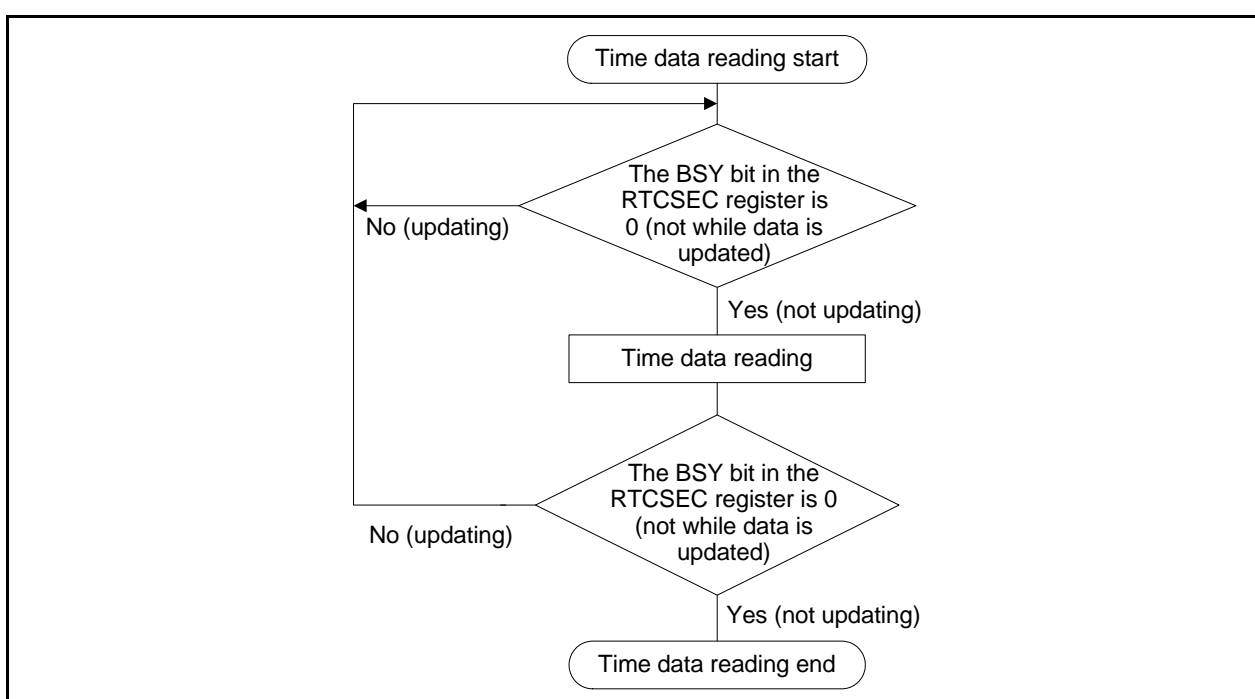
In the real-time clock periodic interrupt routine, read the values necessary from the appropriate time data bits.

- Monitoring by a program 1

Monitor the IR bit in the RTCTIC register by a program and read necessary values of time data bits after the IR bit becomes 1 (periodic interrupt requested).

- Monitoring by a program 2

Read the time data according to Figure 20.11 “Time Data Reading”.



**Figure 20.11 Time Data Reading**

Also, when reading multiple registers, read them as continuously as possible.

**Note:**

1. Time data bits are as follows:  
 Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register  
 Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register  
 Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register  
 Bits WK2 to WK0 in the RTCWK register  
 The RTCPM bit in the RTCCR1 register

## 21. Serial Interface UARTi (i = 0 to 4)

### Note

Pins CLK4, RXD4, and TXD4 do not exist in the 64-pin package. Do not access the UART4 associated registers.

### 21.1 Introduction

Serial interfaces consist of five channels: UART0 to UART4.

Each UART has a dedicated timer to generate a transmit/receive clock, and operates independently of the others.

Table 21.1 lists UARTi Specifications (i = 0 to 4). Table 21.2 lists Specification Differences between UART0 to UART4. Figure 21.1 shows the block diagram of UARTi. Figure 21.2 shows UARTi Transmit/Receive Unit Block Diagram.

**Table 21.1 UARTi Specifications (i = 0 to 4)**

Item	Specification
Operational mode	<ul style="list-style-type: none"> <li>• Clock synchronous serial I/O mode</li> <li>• Clock asynchronous serial I/O mode (UART mode)</li> <li>• Special mode 1 (I<sup>2</sup>C mode) Can be used with UART2. The simplified I<sup>2</sup>C-bus interface is supported.</li> <li>• Special mode 2 Can be used with UART2. The transmit/receive clock polarity and phase are selectable.</li> <li>• Special mode 3 (bus collision detection function, IE mode) Can be used with UART2. A 1-byte wave of the UART mode approximates 1-bit of the IEBus.</li> <li>• Special mode 4 (SIM mode) Can be used with UART2. The SIM interface is supported.</li> </ul>

**Table 21.2 Specification Differences between UART0 to UART4**

Mode	UART0	UART1	UART2	UART3	UART4
Clock synchronous serial I/O mode	Available		Available	Available	
Clock asynchronous serial I/O mode (UART mode)	Available		Available	Available	
Special mode 1 (I <sup>2</sup> C mode)	Not available		Available	Not available	
Special mode 2	Not available		Available	Not available	
Special mode 3 (IE mode)	Not available		Available	Not available	
Special mode 4 (SIM mode)	Not available		Available	Not available	
CTS/RTS pin	Available		Available	Available	Not available

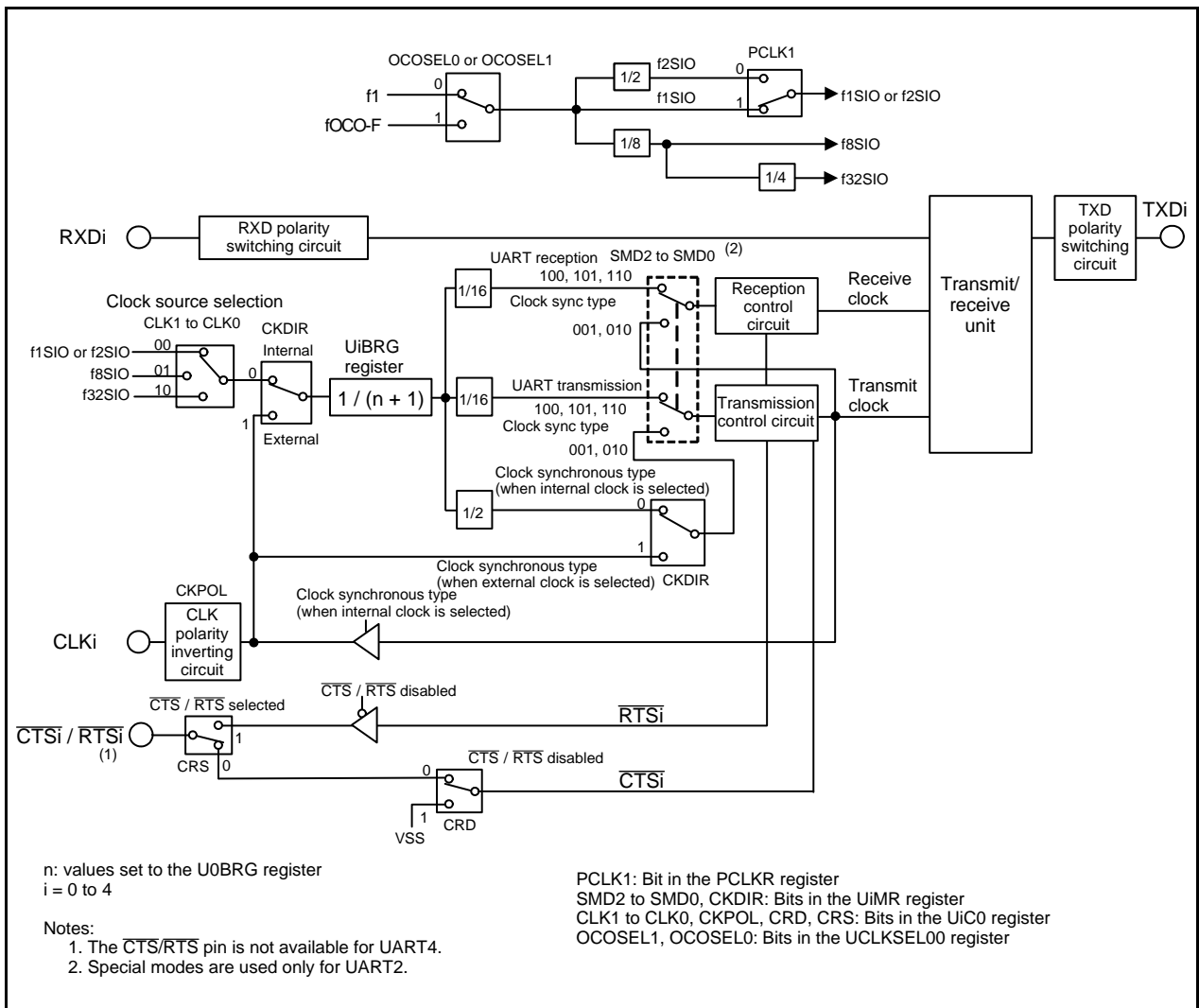


Figure 21.1 UARTi Block Diagram

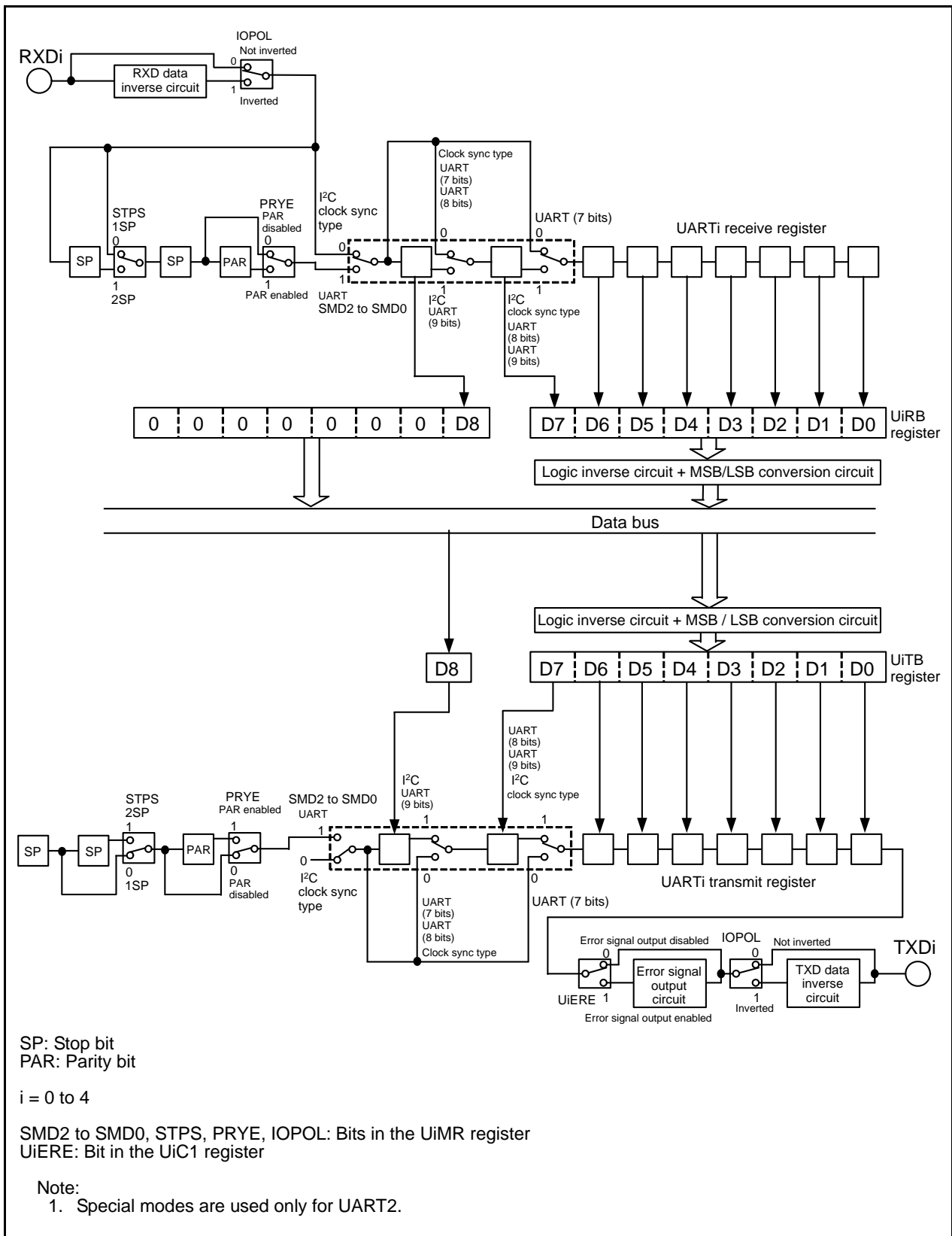


Figure 21.2 UARTi Transmit/Receive Unit Block Diagram

## 21.2 Registers

Table 21.3 and Table 21.4 list registers associated with UART0 to UART4.

Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART4 again.

Refer to “Registers Used and Settings” in each mode for the settings of registers and bits.

**Table 21.3 Registers (1/2)**

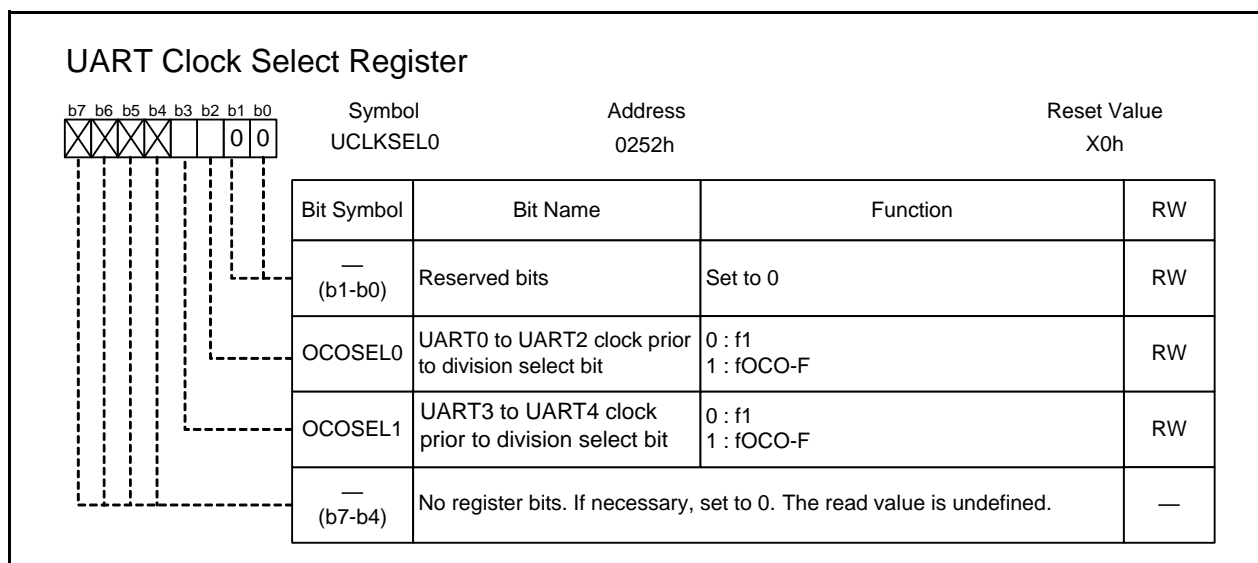
Address	Register	Symbol	Reset Value
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0252h	UART Clock Select Register	UCLKSEL0	X0h
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b

**Table 21.4 Registers (2/2)**

Address	Register	Symbol	Reset Value
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
0370h	Pin Assignment Control Register	PACR	0XXX X000b



### 21.2.1 UART Clock Select Register (UCLKSEL0)



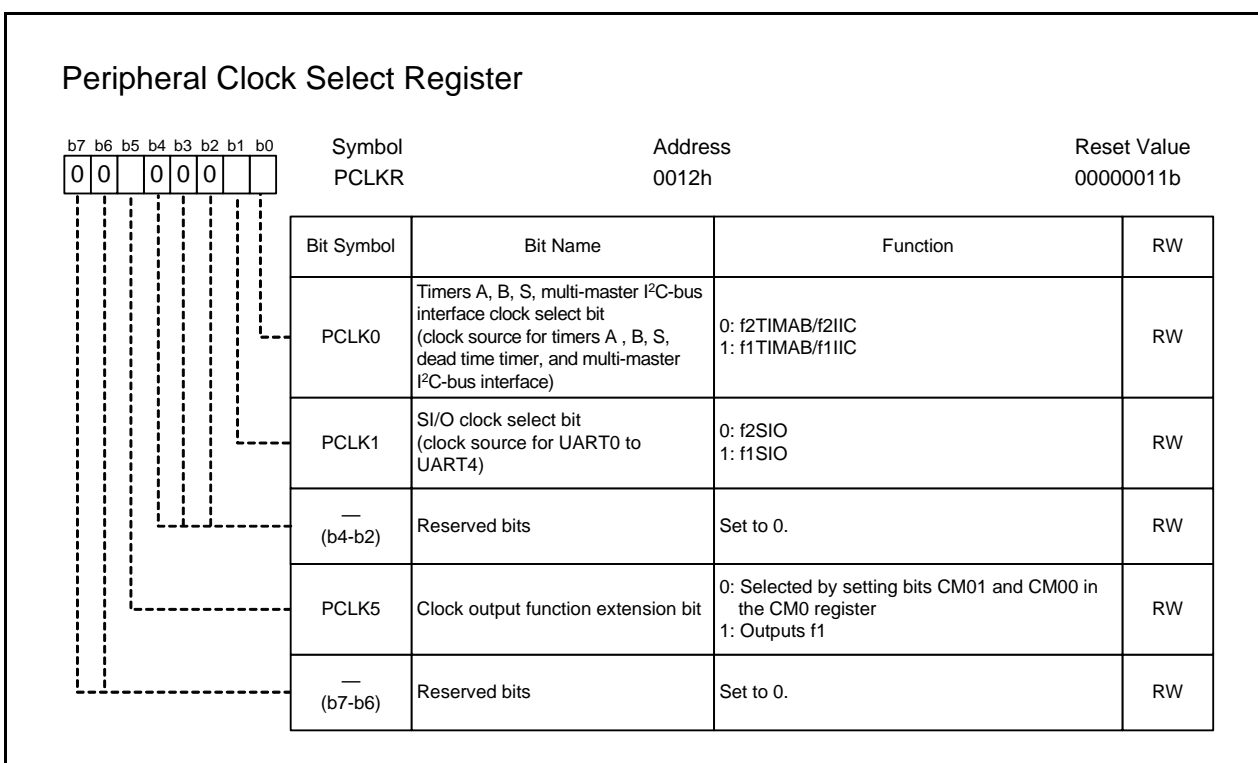
OCOSEL0 (UART0 to UART2 clock prior to division select bit) (b2)

OCOSEL1 (UART3 to UART4 clock prior to division select bit) (b3)

Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART3 to UART4 stops.

Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART3 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART3 to UART4 again.

### 21.2.2 Peripheral Clock Select Register (PCLKR)



Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting this register.

### 21.2.3 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 to 4)

UARTi Transmit/Receive Mode Register (i = 0 to 4)			
Symbol		Address	Reset Value
U0MR, U1MR, U2MR		0248h, 0258h, 0268h	00h
U4MR, U3MR		0298h, 02A8h	00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0 : Serial interface disabled	RW
SMD1		0 0 1 : Clock synchronous serial I/O mode	RW
SMD2		0 1 0 : I <sup>2</sup> C mode 1 0 0 : UART mode character bit length is 7 bits 1 0 1 : UART mode character bit length is 8 bits 1 1 0 : UART mode character bit length is 9 bits Only set the values listed above.	RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bit	RW
PRY	Odd/even parity select bit	Enabled when PRYE is 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TXD, RXD I/O polarity inverse bit	0 : Not inverted 1 : Inverted	RW

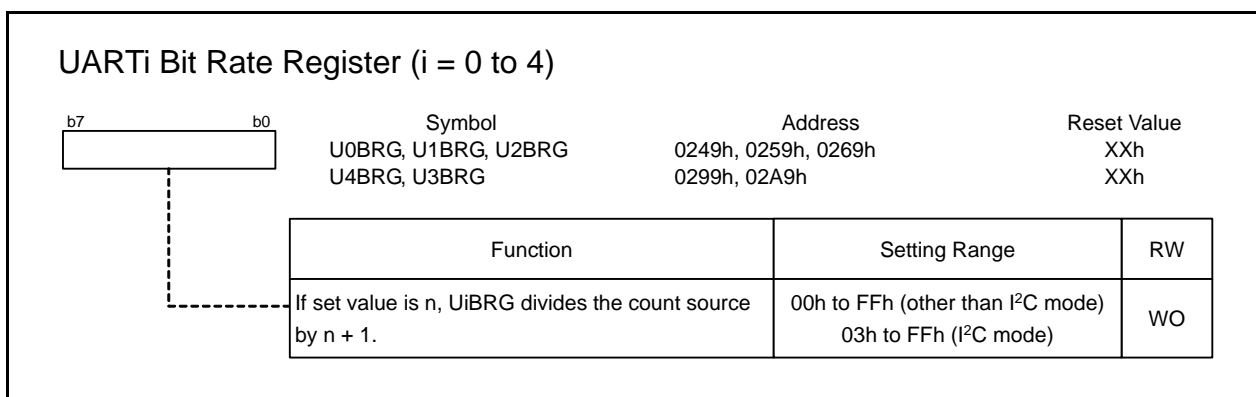
Write to the U4MR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled)

#### SMD2 to SMD0 (Serial I/O mode select bit) (b2 to b0)

When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).

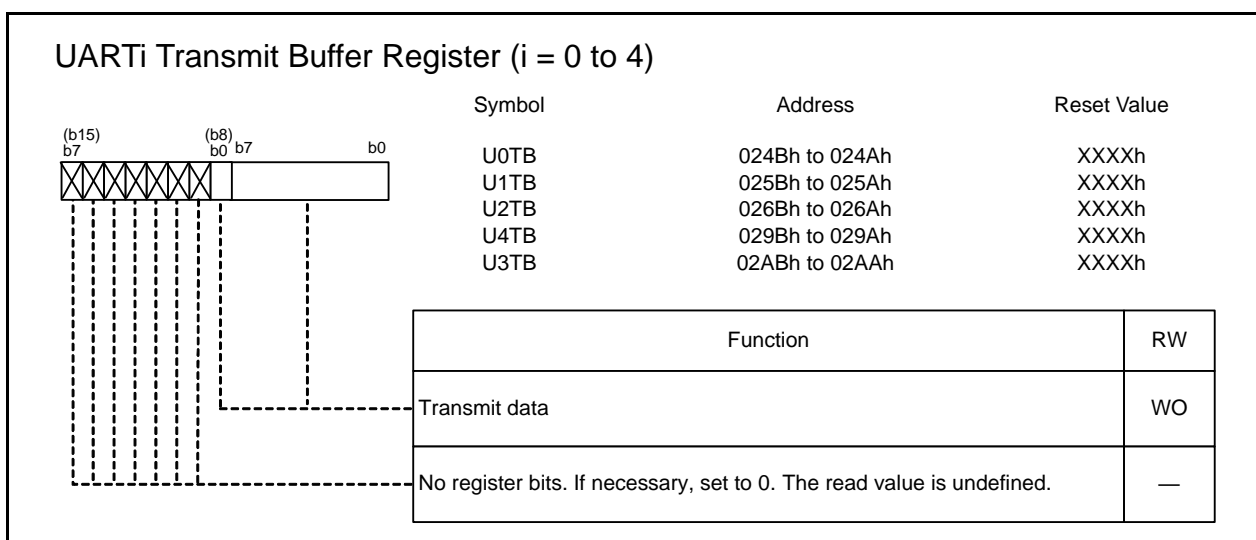
010b (I<sup>2</sup>C mode) is selected by the U2MR register. Do not select 010b by the U0MR, U1MR, U3MR, or U4MR register.

### 21.2.4 UARTi Bit Rate Register (UiBRG) (i = 0 to 4)



Write to the UiBRG register while the serial interface is neither transmitting nor receiving.  
 Use the MOV instruction to write to the UiBRG register.  
 Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.

### 21.2.5 UARTi Transmit Buffer Register (UiTB) (i = 0 to 4)



Use the MOV instruction to write to this register.  
 When character length is 9 bits long or I<sup>2</sup>C mode, write to this register in 16-bit units, or in 8-bit units from upper byte to lower byte.

### 21.2.6 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 4)

UARTi Transmit/Receive Control Register 0 (i = 0 to 4)		Symbol	Address	Reset Value
		U0C0, U1C0, U2C0 U4C0, U3C0	024Ch, 025Ch, 026Ch 029Ch, 02ACh	0000 1000b 0000 1000b
Bit Symbol	Bit Name	Function	RW	
CLK0	UiBRG count source select bit	b1 b0 0 0 : f1SIO or f2SIO selected 0 1 : f8SIO selected 1 0 : f32SIO selected 1 1 : Do not set	RW	
CLK1		RW		
CRS	$\overline{\text{CTS}}/\overline{\text{RTS}}$ function select bit	Enabled when CRD is 0 0 : $\overline{\text{CTS}}$ function selected 1 : $\overline{\text{RTS}}$ function selected	RW	
TXEPT	Transmit register empty flag	0 : Data present in transmit register (transmission in progress) 1 : No data present in transmit register (transmission completed)	RO	
CRD	$\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit	0 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ function enabled 1 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled	RW	
NCH	Data output select bit	0 : Pins TXDi/SDAi and SCLi are CMOS output 1 : Pins TXDi/SDAi and SCLi are N-channel open drain output	RW	
CKPOL	CLK polarity select bit	0 : Transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge 1 : Transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge	RW	
UFORM	Bit order select bit	0 : LSB first 1 : MSB first	RW	

#### CLK1 to CLK0 (UiBRG count source select bit) (b1-b0)

When bits CLK1 to CLK0 are 00b (f1SIO or f2SIO selected), select f1SIO or f2SIO by the PCLK1 bit in the PCLKR register.

Set bits CLK1 to CLK0 after setting registers UCLKSEL0 and PCLKR.

If bits CLK1 to CLK0 are changed, set the UiBRG register.

#### CRD ( $\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit) (b4)

When the CRD bit is 1 ( $\overline{\text{CTS}}/\overline{\text{RTS}}$  function disabled), the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  pin can be used as an I/O port.

Set the CRD bit in the U4C0 register to 1 ( $\overline{\text{CTS}}/\overline{\text{RTS}}$  function disabled).

### NCH (Data output select bit) (b5)

When the clock synchronous serial I/O mode, the I<sup>2</sup>C mode, or the UART mode is selected by setting the bits SMD2 to SMD0 in the UiMR register, the output method of pins TXDi/SDAi can be selected with the NCH bit. When bits SMD2 to SMD0 is 000b (serial interface disabled), the output method of pins TXDi/SDAi is CMOS.

When the IICM bit in the U2SMR register is 1 (I<sup>2</sup>C mode) and bits SMD2 to SMD0 is 010b (I<sup>2</sup>C mode), the output method of the SCL2 pin is N-channel open drain with the NCH bit set to 1. When the IICM bit is 0 (other than I<sup>2</sup>C mode), or bits SMD2 to SMD0 is other than 010b, the output method of the SCL2 pin is CMOS.

This function is used to set the P-channel transistor of the CMOS output buffer always off, but not to change pins TXDi, SDA2 and SCL2 to open drain output completely.

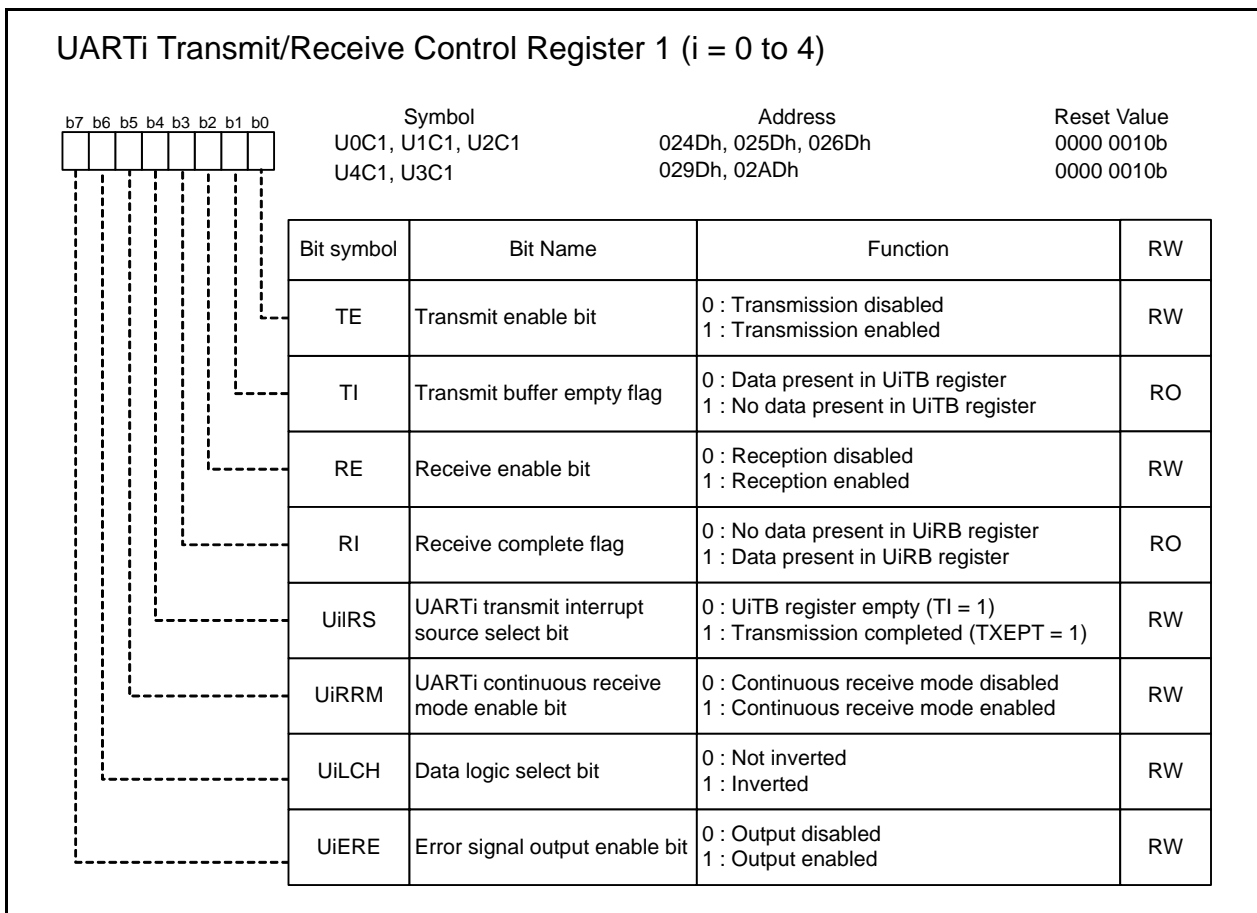
Refer to the electrical characteristics for the input voltage range.

### UFORM (Bit order select bit) (b7)

The UFORM bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), or 101b (UART mode, 8-bit character data).

Set the UFORM bit to 1 when bits SMD2 to SMD0 are 010b (I<sup>2</sup>C mode), and to 0 when bits SMD2 to SMD0 are 100b (UART mode, 7-bit character data) or 110b (UART mode, 9-bit character data).

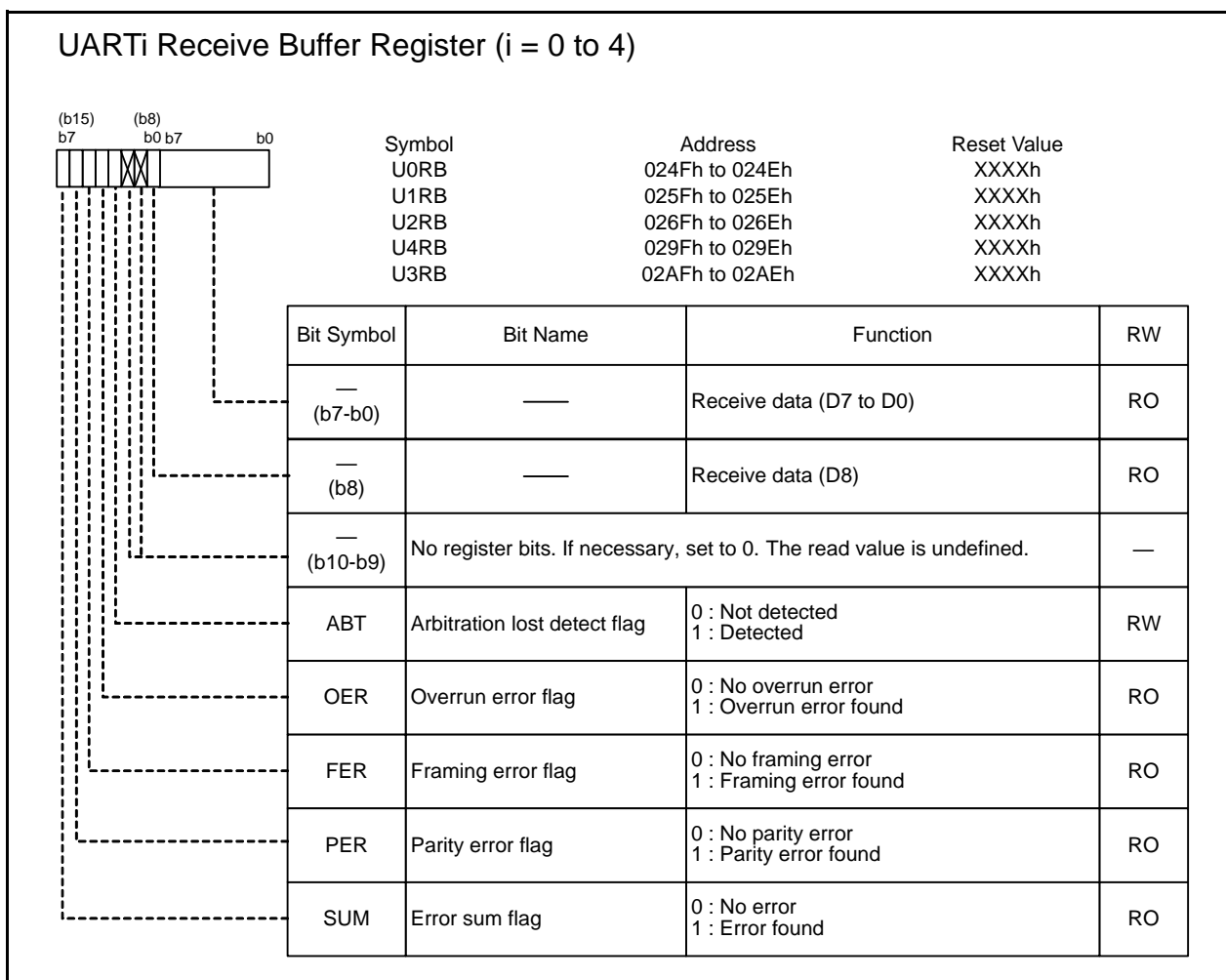
### 21.2.7 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 to 4)



#### UiLCH (Data logic select bit) (b6)

The UiLCH bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), 100b (UART mode, 7-bit character), or 101b (UART mode, 8-bit character). Set this bit to 0 when bits SMD2 to SMD0 are set to 010b (I<sup>2</sup>C mode) or 110b (UART mode, 9-bit character).

## 21.2.8 UARTi Receive Buffer Register (UiRB) (i = 0 to 4)



When bits SMD2 to SMD0 in the UiMR register are 100b, 101b, or 110b, read this register in 16-bit units, or in 8-bit units from upper byte to lower byte.

Bits FER and PER in the upper byte become 0 when the lower byte of the UiRB register is read.

If an overrun error occurs, the receive data of the UiRB register is undefined.

### ABT (Arbitration lost detect flag) (b11)

The ABT bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

### OER (Overrun error flag) (b12)

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).

Condition to become 1:

- The RI bit in the UiC1 register is 1 (data present in UiRB register), and the last bit of the next data is received.

### FER (Framing error flag) (b13)

The FER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I<sup>2</sup>C mode). The read value is undefined.

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The set number of stop bits is not detected.  
(detected when the received data is transferred from the UARTi receive register to the UiRB register.)

### PER (Parity error flag) (b14)

The PER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I<sup>2</sup>C mode). The read value is undefined.

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The number of 1's of the parity bit and character bits do not match the set value of the PRY bit in the UiMR register.  
(detected when the received data is transferred from the UARTi receive register to the UiRB register.)

### SUM (Error sum flag) (b15)

The SUM bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I<sup>2</sup>C mode). The read value is undefined.

Conditions to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- Bits PER, FER and OER are all 0 (no error).

Condition to become 1:

- At least two bits out of PER, FER, or OER are 1 (error found).



### 21.2.9 UART2 Special Mode Register 4 (U2SMR4)

UART2 Special Mode Register 4		Symbol	Address	Reset Value
		U2SMR4	0264h	00h
Bit Symbol	Bit Name	Function	RW	
STAREQ	Start condition generate bit	0 : Clear 1 : Start	RW	
RSTAREQ	Restart condition generate bit	0 : Clear 1 : Start	RW	
STPREQ	Stop condition generate bit	0 : Clear 1 : Start	RW	
STSPSEL	SCL, SDA output select bit	0 : Select serial I/O circuit 1 : Select start condition/stop condition generate circuit	RW	
ACKD	ACK data bit	0 : ACK 1 : NACK	RW	
ACKC	ACK data output enable bit	0 : Serial data output 1 : ACK data output	RW	
SCLHI	SCL output stop bit	If stop condition is detected, 0 : Do not stop SCL2 output 1 : Stop SCL2 output	RW	
SWC9	SCL wait auto insert bit 3	0 : No wait-state/wait-state cleared 1 : Hold the SCL2 pin low after the ninth bit of the SCL2 is received	RW	

#### STAREQ (Start condition generate bit) (b0)

The STAREQ bit becomes 0 when a start condition is generated.

This bit is used in master mode of I<sup>2</sup>C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I<sup>2</sup>C mode). Do not set this bit to 1 when the IICM bit is 0.

#### RSTAREQ (Restart condition generate bit) (b1)

The RSTAREQ bit becomes 0 when a restart condition is generated.

This bit is used in master mode of I<sup>2</sup>C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I<sup>2</sup>C mode). Do not set this bit to 1 when the IICM bit is 0.

#### STPREQ (Stop condition generate bit) (b2)

The STPREQ bit becomes 0 when a stop condition is generated.

This bit is used in master mode of I<sup>2</sup>C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I<sup>2</sup>C mode). Do not set this bit to 1 when the IICM bit is 0.

#### STSPSEL (SCL, SDA output select bit) (b3)

This bit is used in master mode of I<sup>2</sup>C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I<sup>2</sup>C mode). Do not set this bit to 1 when the IICM bit is 0.

Set the STSPSEL bit to 1 (select start condition/stop condition generate circuit) after setting the STAREQ, RSTAREQ, or STPREQ bit to 1 (start).

ACKD (ACK data bit) (b4)

ACKC (ACK data output enable bit) (b5)

SWC9 (SCL wait auto insert bit 3) (b7)

This bit is used in slave mode of I<sup>2</sup>C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I<sup>2</sup>C mode). Do not set this bit to 1 when the IICM bit is 0.

SCLHI (SCL output stop bit) (b6)

This bit is used in master mode of I<sup>2</sup>C mode. To set this bit to 1, preset the IICM bit in the U2SMR register to 1 (I<sup>2</sup>C mode). Do not set this bit to 1 when the IICM bit is 0.

### 21.2.10 UART2 Special Mode Register 3 (U2SMR3)

UART2 Special Mode Register 3				
		Symbol U2SMR3	Address 0265h	Reset Value 000X 0X0Xb
Bit Symbol	Bit Name	Function	RW	
— (b0)	No register bit. If necessary, set to 0. The read value is undefined.		—	
CKPH	Clock phase set bit	0 : No clock delay 1 : With clock delay	RW	
— (b2)	No register bit. If necessary, set to 0. The read value is undefined.		—	
NODC	Clock output select bit	0 : CLK2 is CMOS output 1 : CLK2 is N-channel open drain output	RW	
— (b4)	No register bit. If necessary, set to 0. The read value is undefined.		—	
DL0	SDA2 digital delay setup bit	b7 b6 b5 0 0 0 : No delay 0 0 1 : 1 to 2 cycles of U2BRG count source 0 1 0 : 2 to 3 cycles of U2BRG count source 0 1 1 : 3 to 4 cycles of U2BRG count source 1 0 0 : 4 to 5 cycles of U2BRG count source 1 0 1 : 5 to 6 cycles of U2BRG count source 1 1 0 : 6 to 7 cycles of U2BRG count source 1 1 1 : 7 to 8 cycles of U2BRG count source	RW	
DL1		RW		
DL2		RW		

#### NODC (Clock output select bit) (b3)

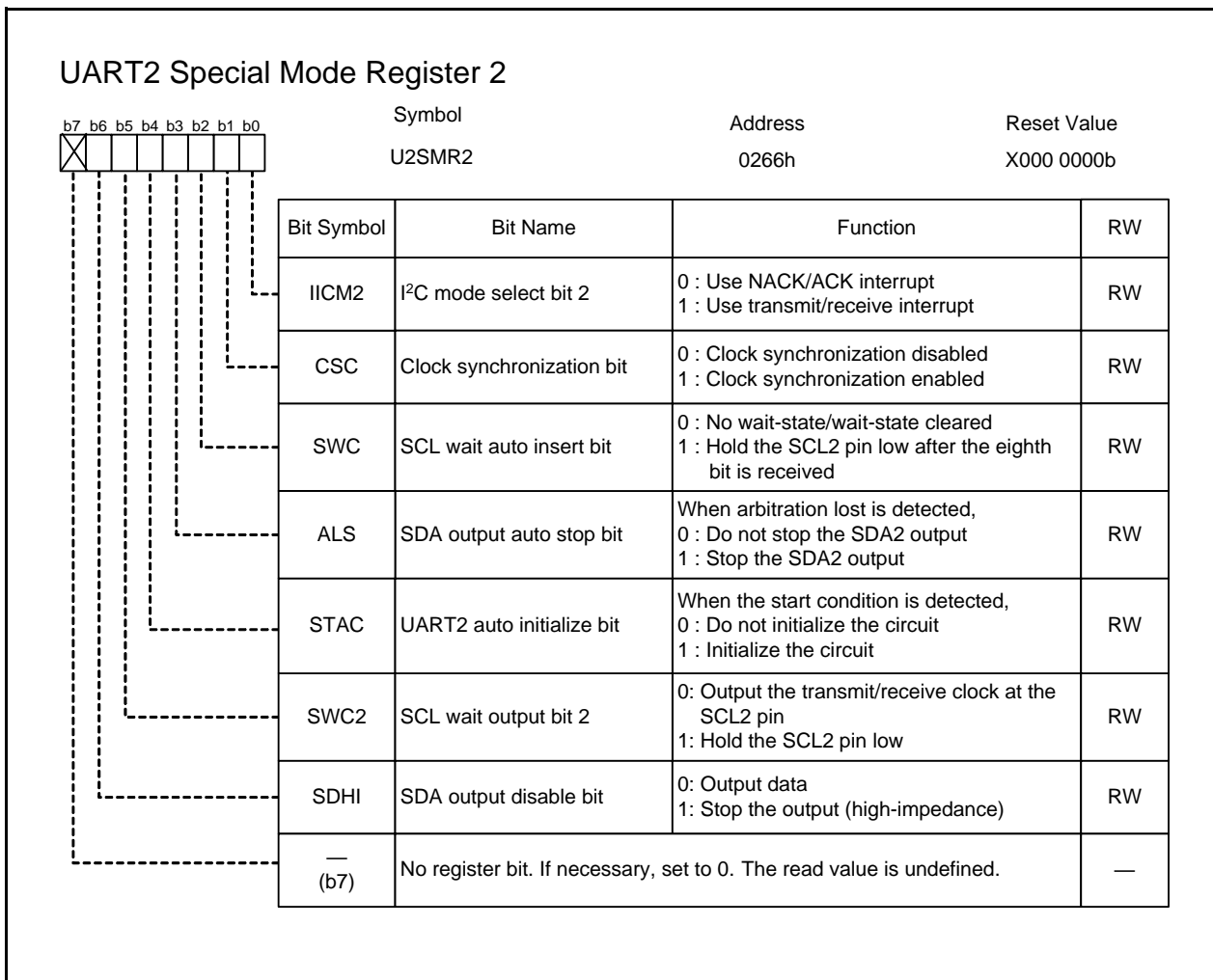
This function is used to set P-channel transistor of the CMOS output buffer always off, but not to change the CLK2 pin to open drain output completely. Refer to the electrical characteristics for the input voltage range.

#### DL2-DL0 (SDA2 digital delay setup bit) (b7-b5)

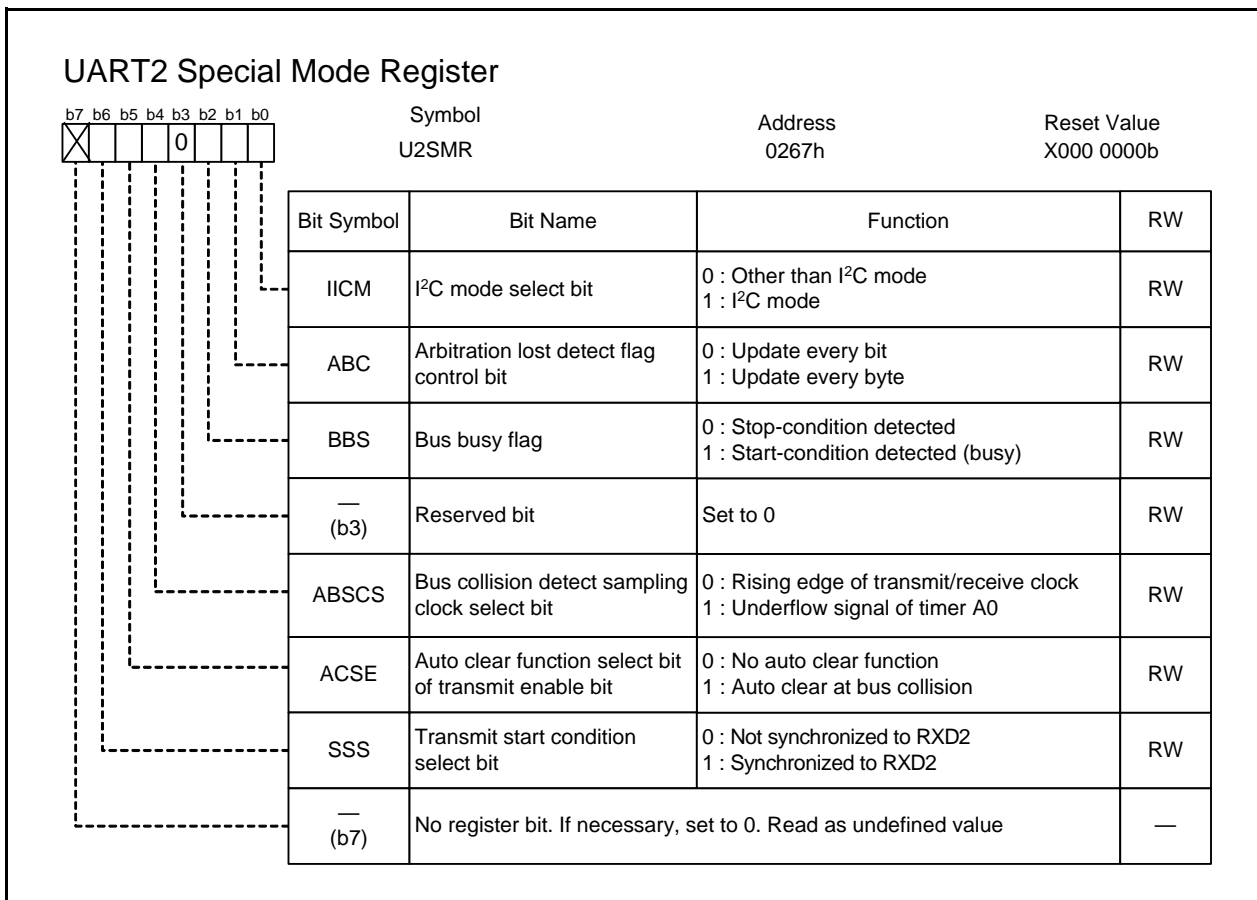
Bits DL2 to DL0 are used to generate a digital delay in SDA2 output in I<sup>2</sup>C mode. Except in I<sup>2</sup>C mode, set these bits to 000b (no delay).

The delay length varies with the load on pins SCL2 and SDA2. Also, when using an external clock, the delay length increases by about 100 ns.

### 21.2.11 UART2 Special Mode Register 2 (U2SMR2)



### 21.2.12 UART2 Special Mode Register (U2SMR)



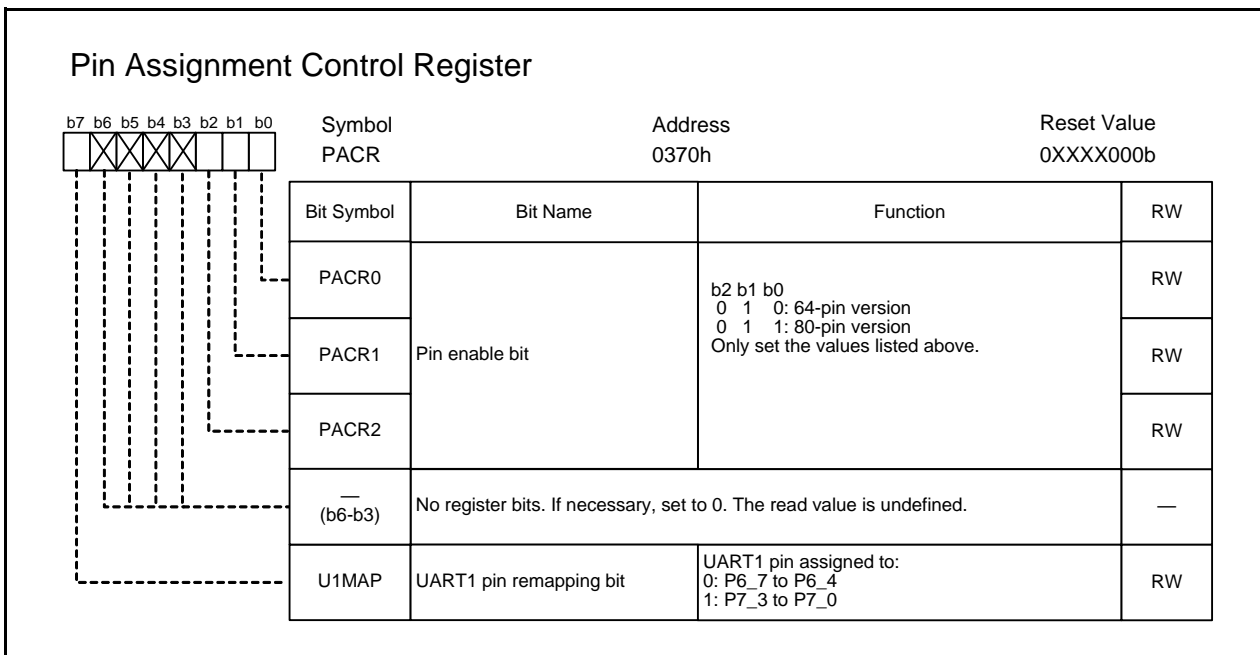
#### BBS (Bus busy flag) (b2)

The BBS bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

#### SSS (Transmit start condition select bit) (b6)

When a transmission starts, the SSS bit becomes 0 (not synchronized to RXD2).

### 21.2.13 Pin Assignment Control Register (PACR)



Write to the PACR register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

## 21.3 Operations

### 21.3.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transmit/receive clock to transmit/receive data. Table 21.5 lists the Clock Synchronous Serial I/O Mode Specifications.

**Table 21.5 Clock Synchronous Serial I/O Mode Specifications**

Item	Specification
Data format	Character length: 8 bits
Transmit/receive clock	<ul style="list-style-type: none"> <li>CKDIR bit in the UiMR register = 0 (internal clock): <math>\frac{f_j}{2(n+1)}</math></li> <li><math>f_j = f1SIO, f2SIO, f8SIO, f32SIO</math></li> <li><math>n =</math> setting value of UiBRG register (00h to FFh)</li> <li>CKDIR bit = 1 (external clock): input from CLKi pin</li> </ul>
Transmit/receive control	Selectable from $\overline{CTS}$ , $\overline{RTS}$ , or $\overline{CTS/RTS}$ function disabled (UART0 to UART3)
Transmission start conditions	To start transmission, satisfy the following requirements <sup>(1)</sup> <ul style="list-style-type: none"> <li>The TE bit in the UiC1 register is 1 (transmission enabled)</li> <li>The TI bit in the UiC1 register is 0 (data presents in UiTB register)</li> <li>When <math>\overline{CTS}</math> function is selected, input on the <math>\overline{CTS_i}</math> pin is low</li> </ul>
Reception start conditions	To start reception, satisfy the following requirements <sup>(1)</sup> <ul style="list-style-type: none"> <li>The RE bit in the UiC1 register is 1 (reception enabled)</li> <li>The TE bit in the UiC1 register is 1 (transmission enabled)</li> <li>The TI bit in the UiC1 register is 0 (data presents in the UiTB register)</li> </ul>
Interrupt request generation timing	For transmission, one of the following conditions can be selected <ul style="list-style-type: none"> <li>The UiIRS bit in the UiC1 register is 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission)</li> <li>The UiIRS bit is 1 (transfer completed): When the serial interface completes sending data from the UARTi transmit register</li> </ul> For reception <ul style="list-style-type: none"> <li>When transferring data from the UARTi receive register to the UiRB register (at completion of reception)</li> </ul>
Error detection	Overrun error <sup>(2)</sup> This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receiving the seventh bit of the next unit of data
Selectable functions	<ul style="list-style-type: none"> <li>CLK polarity selection Data input/output can be selected to occur synchronously with the rising or falling edge of the transmit/receive clock</li> <li>LSB first, MSB first selection Whether to start transmitting/receiving the data from bit 0 or from bit 7 can be selected</li> <li>Continuous receive mode selection Reception is enabled immediately by reading the UiRB register</li> <li>Switching serial data logic This function inverts the logic value of the transmit/receive data</li> </ul>

i = 0 to 4

Notes:

- These requirements do not have to be set in any particular order. If transmission/reception is started while an external clock is selected and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement at either of the following timings:
  - The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
  - The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.
- If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 21.6 lists Pin Functions in Clock Synchronous Serial I/O Mode.

Note that for a period from when UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open drain output is selected, this pin is high-impedance.)

**Table 21.6 Pin Functions in Clock Synchronous Serial I/O Mode**

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(Outputs dummy data only when receiving)
RXDi	Input	Serial data input	Set the port direction bit sharing pin to 0.
	Input	Input port	Set the port direction bit sharing pin to 0. (can be used as an input port only when transmitting)
CLKi	Output	Transmit/receive clock output	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bit sharing pin to 0.
$\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bit sharing pin to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	I/O	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 4

Note:

1. The CTS/RTS pin is not available for UART4.



**Table 21.7 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)**

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART4.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 7	Set transmission data.
	8	- (does not need to be set) If necessary, set to 0.
UiRB	0 to 7	Reception data can be read.
	8, 11, 13 to 15	When read, the read value is undefined.
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select internal clock or external clock.
	4 to 6	Set to 0.
	IOPOL	Set to 0.
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the CTS or RTS function. Set this bit to 1 (disabled) when using UART4.
	NCH	Select TXDi pin output mode.
	CKPOL	Select the transmit/receive clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select source of UARTi transmit interrupt.
	UiRRM	Set to 1 to use continuous receive mode.
	UiLCH	Set to 1 to use inverted data logic.
	UiERE	Set to 0.
U2SMR (2)	0 to 7	Set to 0.
U2SMR2 (2)	0 to 7	Set to 0.
U2SMR3 (2)	0 to 2	Set to 0.
	NODC	Select clock output mode.
	4 to 7	Set to 0.
U2SMR4 (2)	0 to 7	Set to 0.

i = 0 to 4

Notes:

1. This table does not describe a procedure.
2. In case of UART2

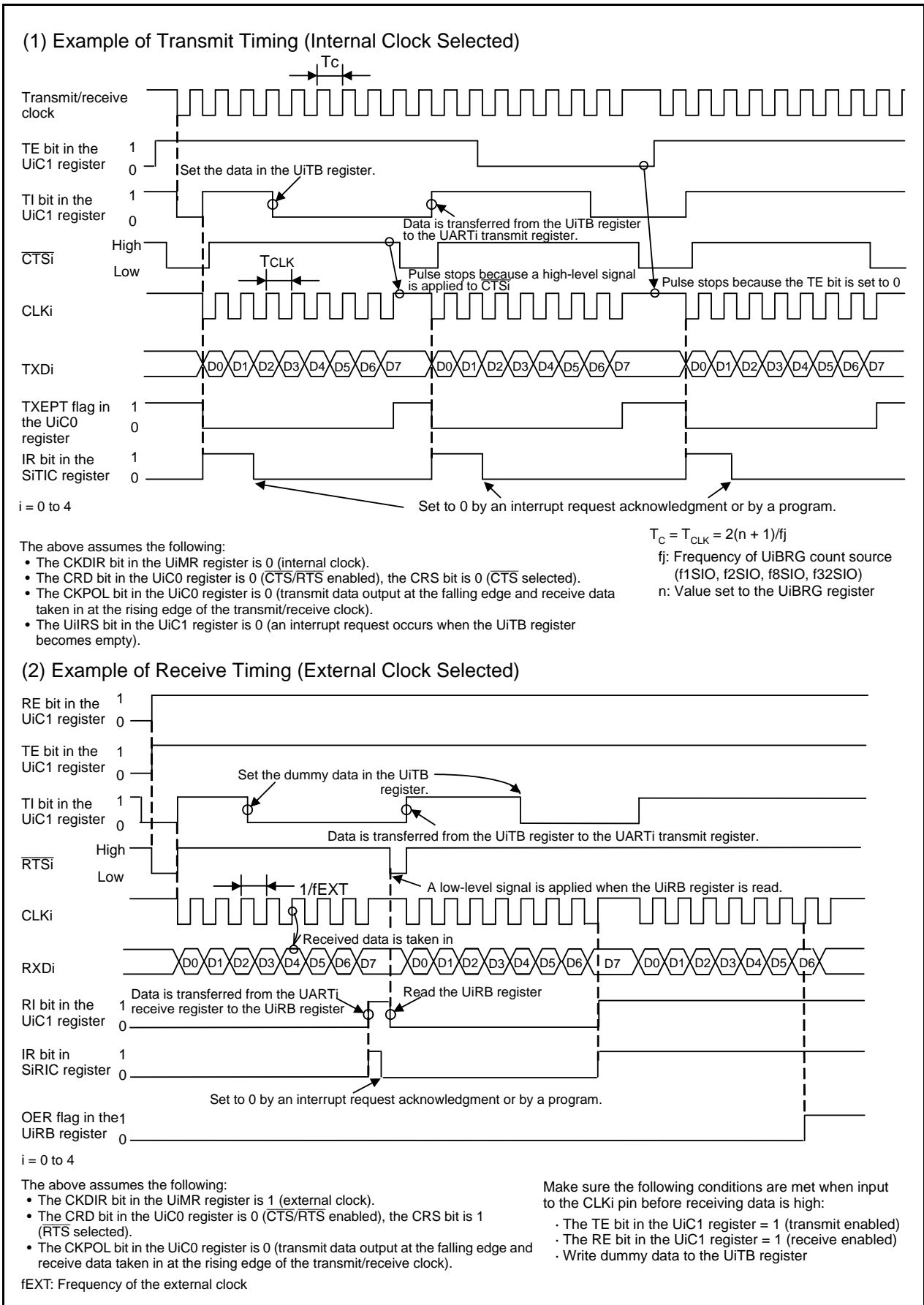


Figure 21.3 Transmit and Receive Operation during Clock Synchronous Serial I/O Mode

### 21.3.1.1 CLK Polarity Select Function

Use the CKPOL bit in the UiC0 register (i = 0 to 4) to select the transmit/receive clock polarity. Figure 21.4 shows the Transmit/Receive Clock Polarity.

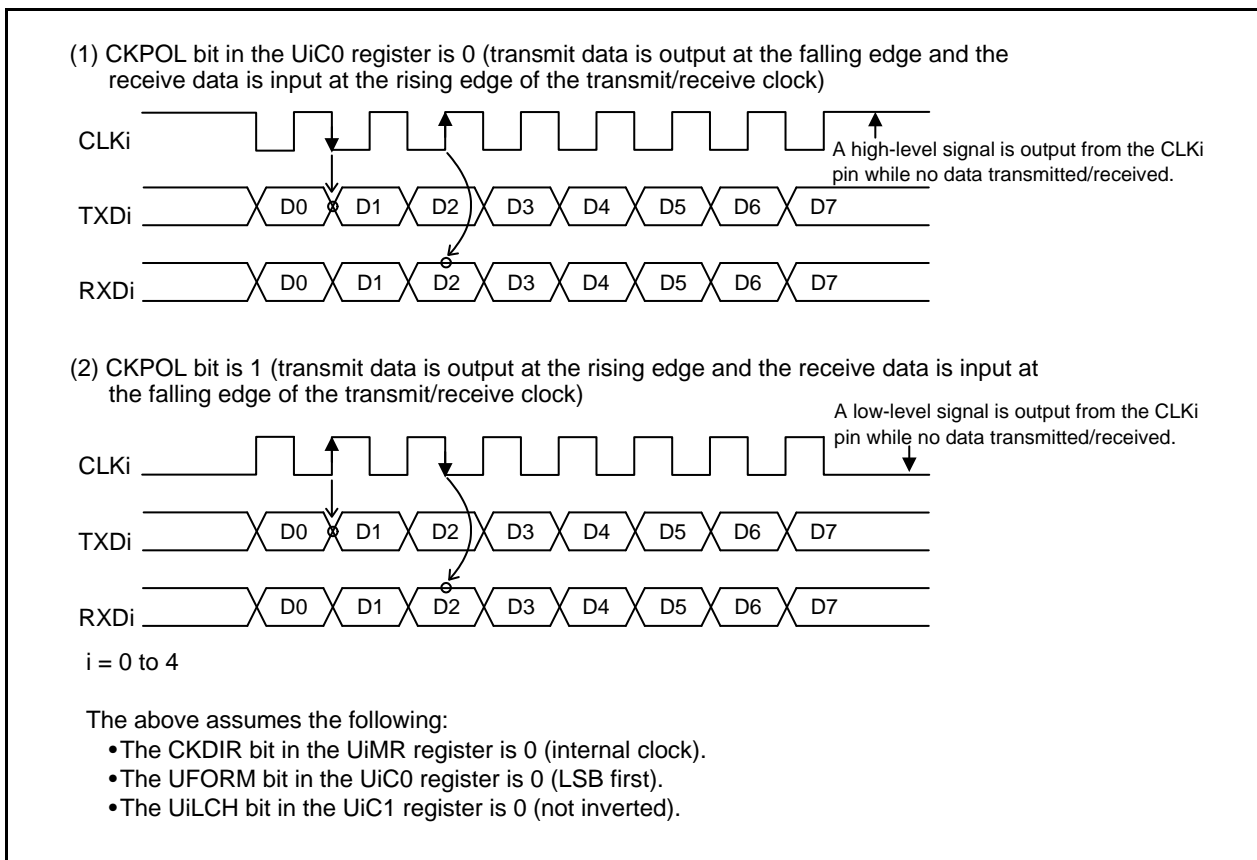


Figure 21.4 Transmit/Receive Clock Polarity

### 21.3.1.2 LSB First/MSB First Select Function

Use the UFORM bit in the UiC0 register (i = 0 to 4) to select the bit order. Figure 21.5 shows the Bit Order.

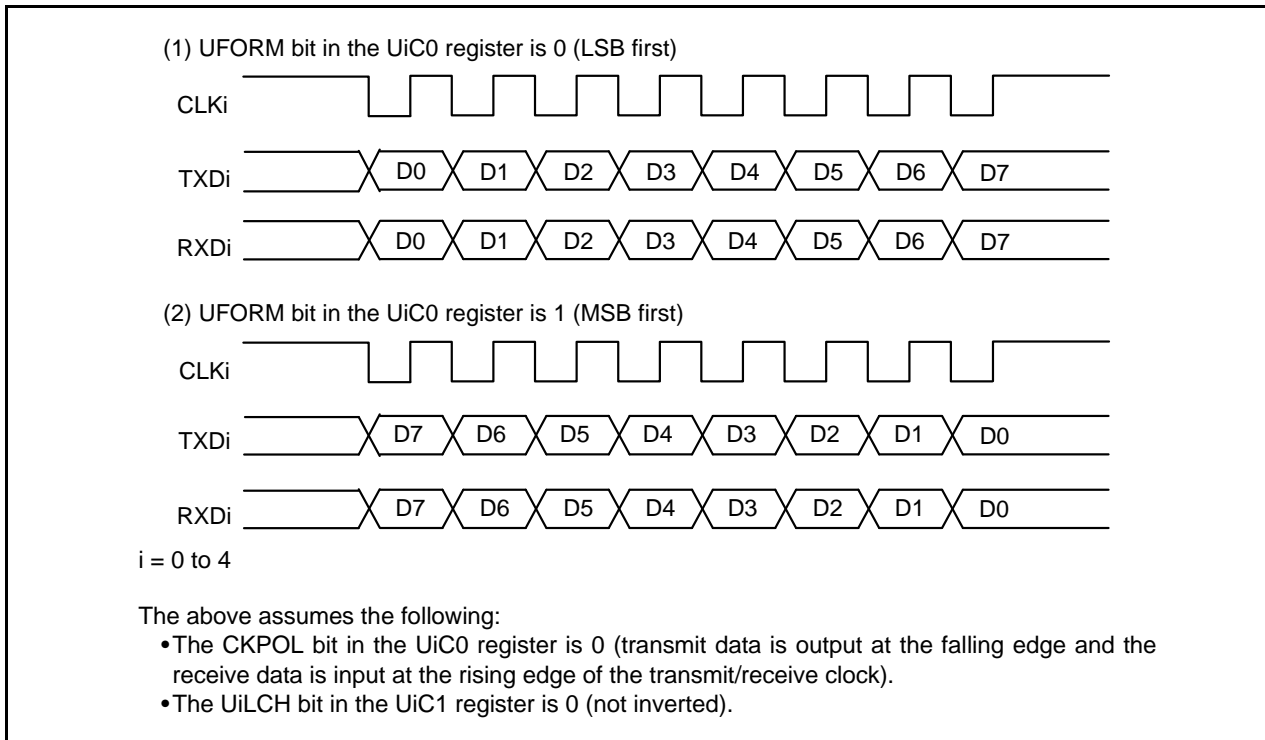


Figure 21.5 Bit Order

### 21.3.1.3 Continuous Receive Mode

In continuous receive mode, the receive operation is enabled when the receive buffer register is read. Thus, a dummy write to the transmit buffer register to enable the receive operation is unnecessary in this mode. However, a dummy read of the receive buffer register is required when start receiving. When setting the UiRRM bit in the UiC1 (i = 0 to 4) to 1 (continuous receive mode), the TI bit in the UiC1 register is set to 0 (data present in the UiTB register) by reading the UiRB register. When the UiRRM bit is 1, do not write dummy data to the UiTB register by a program. When using an external clock, read the UiRB register between receiving the eighth bit of data and starting the next transmission.

Figure 21.6 shows Operation Example in Continuous Receive Mode.

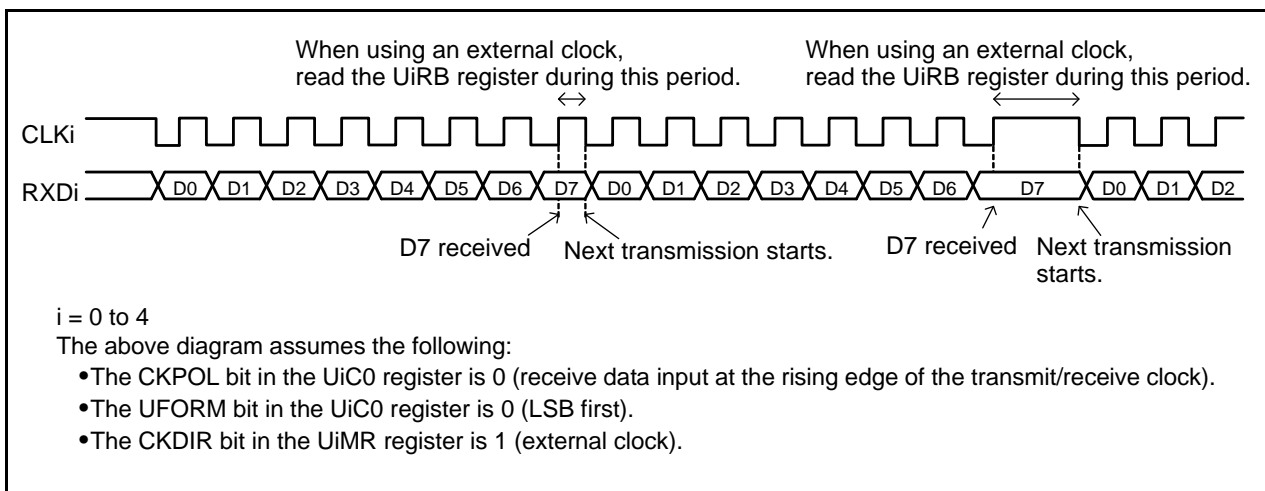


Figure 21.6 Operation Example in Continuous Receive Mode

### 21.3.1.4 Serial Data Logic Switching Function

When the UiLCH bit in the UiC1 register (i = 0 to 4) is 1 (inverted), the data written to the UiTB register has its logic inverted before being transmitted. Similarly, the inverted data has its logic inverted when read from the UiRB register. Figure 21.7 shows Serial Data Logic.

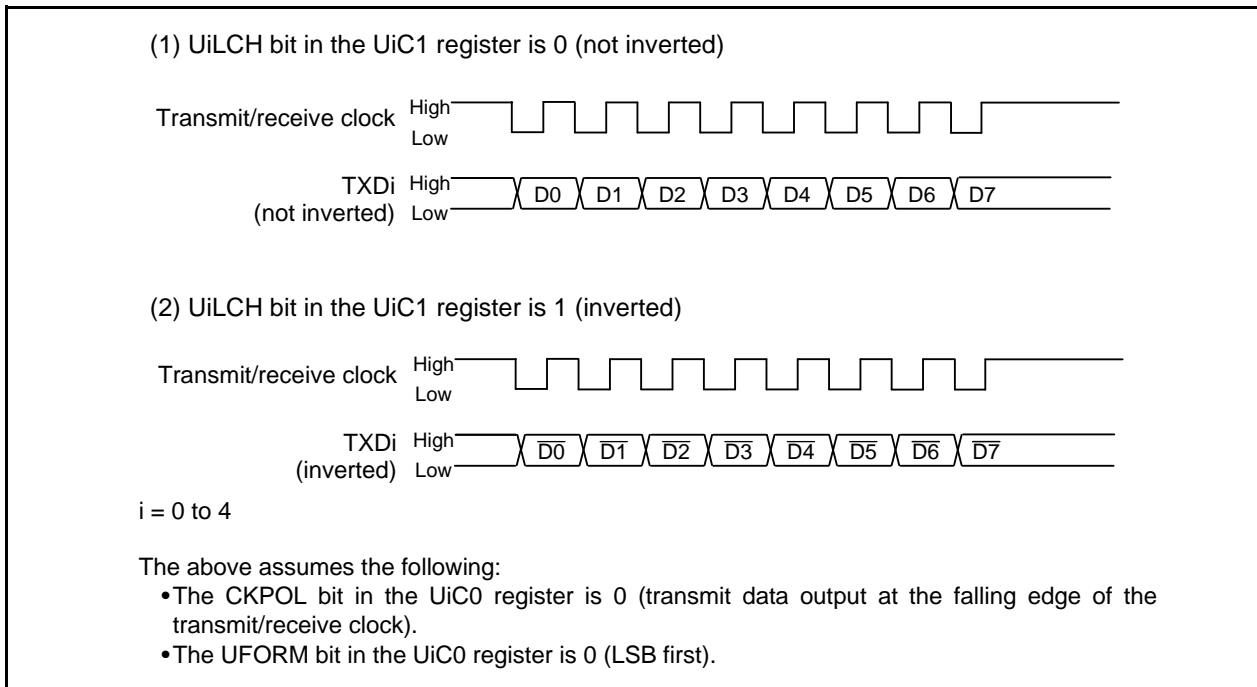


Figure 21.7 Serial Data Logic

### 21.3.1.5 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The  $\overline{\text{CTS}}$  function is used to start transmit/receive operation when a low signal is applied to the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  (i = 0 to 3) pin. Transmit/receive operation begins when input to the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  pin becomes low. If the low signal is switched to high during a transmit or receive operation, the operation stops before the next data.

For the  $\overline{\text{RTS}}$  function, the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  pin outputs a low signal when the MCU is ready to receive. The output level becomes high at the detection of the start bit.

See Table 21.6 "Pin Functions in Clock Synchronous Serial I/O Mode".

### 21.3.1.6 Processing When Terminating Communication or When an Error Occurs

When communication is terminated in clock synchronous serial I/O mode, or when a communication error occurs, use the following procedure to reset communication:

- (1) Set the TE bit in the UiC1 (i = 0 to 4) register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
- (3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
- (4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

### 21.3.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data to be transmitted/received after setting the desired bit rate and bit order. Table 21.8 lists the UART Mode Specifications.

**Table 21.8 UART Mode Specifications**

Item	Specification
Data format	<ul style="list-style-type: none"> <li>• Character bit: selectable from 7, 8, or 9 bits</li> <li>• Start bit: 1 bit</li> <li>• Parity bit: selectable from odd, even, or none</li> <li>• Stop bit: selectable from 1 bit or 2 bits</li> </ul>
Transmit/receive clock	<ul style="list-style-type: none"> <li>• The CKDIR bit in the UiMR register = 0 (internal clock): <math>\frac{f_j}{16(n+1)}</math>  <math>f_j = f1SIO, f2SIO, f8SIO, f32SIO</math> n: Setting value of UiBRG register 00h to FFh</li> <li>• CKDIR bit = 1 (external clock): <math>\frac{fEXT}{16(n+1)}</math>  <math>fEXT</math>: Input from CLKi pin n: Setting value of UiBRG register 00h to FFh</li> </ul>
Transmit/receive control	Selectable from $\overline{CTS}$ , $\overline{RTS}$ , or $\overline{CTS/RTS}$ function disabled (UART0 to UART3)
Transmission start conditions	To start transmission, satisfy the following requirements: <ul style="list-style-type: none"> <li>• The TE bit in the UiC1 register is 1 (transmission enabled)</li> <li>• The TI bit in the UiC1 register is 0 (data present in the UiTB register)</li> <li>• If <math>\overline{CTS}</math> function is selected, input on the <math>\overline{CTS_i}</math> pin = low</li> </ul>
Reception start conditions	To start reception, satisfy the following requirements: <ul style="list-style-type: none"> <li>• The RE bit in the UiC1 register is 1 (reception enabled)</li> <li>• Start bit detection</li> </ul>
Interrupt request generation timing	For transmission, one of the following conditions can be selected: <ul style="list-style-type: none"> <li>• The UiIRS bit in the UiC1 register is 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission)</li> <li>• The UiIRS bit is 1 (transmission completed): When the serial interface completes sending data from the UARTi transmit register</li> </ul> For reception: <ul style="list-style-type: none"> <li>• When transferring data from the UARTi receive register to the UiRB register (at completion of reception)</li> </ul>
Error detection	<ul style="list-style-type: none"> <li>• Overrun error <sup>(1)</sup> This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the bit before the last stop bit of the next unit of data.</li> <li>• Framing error This error occurs when the number of stop bits set is not detected.</li> <li>• Parity error This error occurs when the number of 1's of the parity bit and character bit does not match the set value of the PRY bit in the UiMR register.</li> <li>• Error sum flag This flag becomes 1 when any of the overrun, framing, or parity errors occur.</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>• LSB first, MSB first selection Whether to start transmitting/receiving the data from bit 0 or from bit 7 can be selected.</li> <li>• Serial data logic switch This function inverts the logic of the transmit/receive data. The start and stop bits are not inverted.</li> <li>• TXD, RXD I/O polarity switch This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted.</li> </ul>

i = 0 to 4

Note:

1. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 21.9 lists I/O Pin Functions in UART Mode. Note that for a period from when the UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open drain output is selected, this pin becomes high-impedance.)

**Table 21.9 I/O Pin Functions in UART Mode**

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(High-level output only when receiving.)
RXDi	Input	Serial data input	Set the port direction bit sharing pin to 0.
CLKi	I/O	Input/output port	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bit sharing pin to 0.
$\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$ (1)	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bit sharing pin to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	I/O	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 4

Note:

1. The  $\overline{\text{CTS}}/\overline{\text{RTS}}$  pin is not available for UART4.



**Table 21.10 Registers Used and Settings in UART Mode (1)**

Register	Bits	Function
UCLKSELO	OCOSEL0	Select clock prior to division for UART0 to UART2.
	OCOSEL1	Select clock prior to division for UART3 to UART4.
PCLKR	PCLK1	Select the count source for the UiBRG register.
UiTB	0 to 8	Set transmission data. (2)
UiRB	0 to 8	Reception data can be read. (2, 4)
	OER, FER, PER, SUM	Error flag
	11	When read, the read value is undefined.
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 100b when character bit length is 7 bits.
		Set to 101b when character bit length is 8 bits.
		Set to 110b when character bit length is 9 bits.
	CKDIR	Select the internal clock or external clock.
	STPS	Select number of stop bits.
	PRY, PRYE	Select whether parity is included and whether odd or even.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
		If CTS or RTS is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the CTS or RTS function. Set this bit to 1 (disabled) when using UART4.
	NCH	Select TXDi pin output mode.
	CKPOL	Set to 0.
	UFORM	LSB first or MSB first can be selected when character bit length is 8 bits. Set to 0 when character bit length is 7 or 9 bits.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UiIRS	Select source of UARTi transmit interrupt.
	UiRRM	Set to 0.
	UiLCH	Set to 1 to use reversed data logic.
UiERE	Set to 0.	
U2SMR (3)	0 to 7	Set to 0.
U2SMR2 (3)	0 to 7	Set to 0.
U2SMR3 (3)	0 to 7	Set to 0.
U2SMR4 (3)	0 to 7	Set to 0.

i = 0 to 4

Notes:

1. This table does not describe a procedure.
2. The bits used for transmit/receive data are as follows: Bits 0 to 6 when character bit length is 7 bits; bits 0 to 7 when character bit length is 8 bits; bits 0 to 8 when character bit length is 9 bits.
3. In case of UART2.
4. The values of bits 7 and 8 are undefined when character bit length is 7 bits.  
The values of bit 8 is undefined when character bit length is 8 bits.

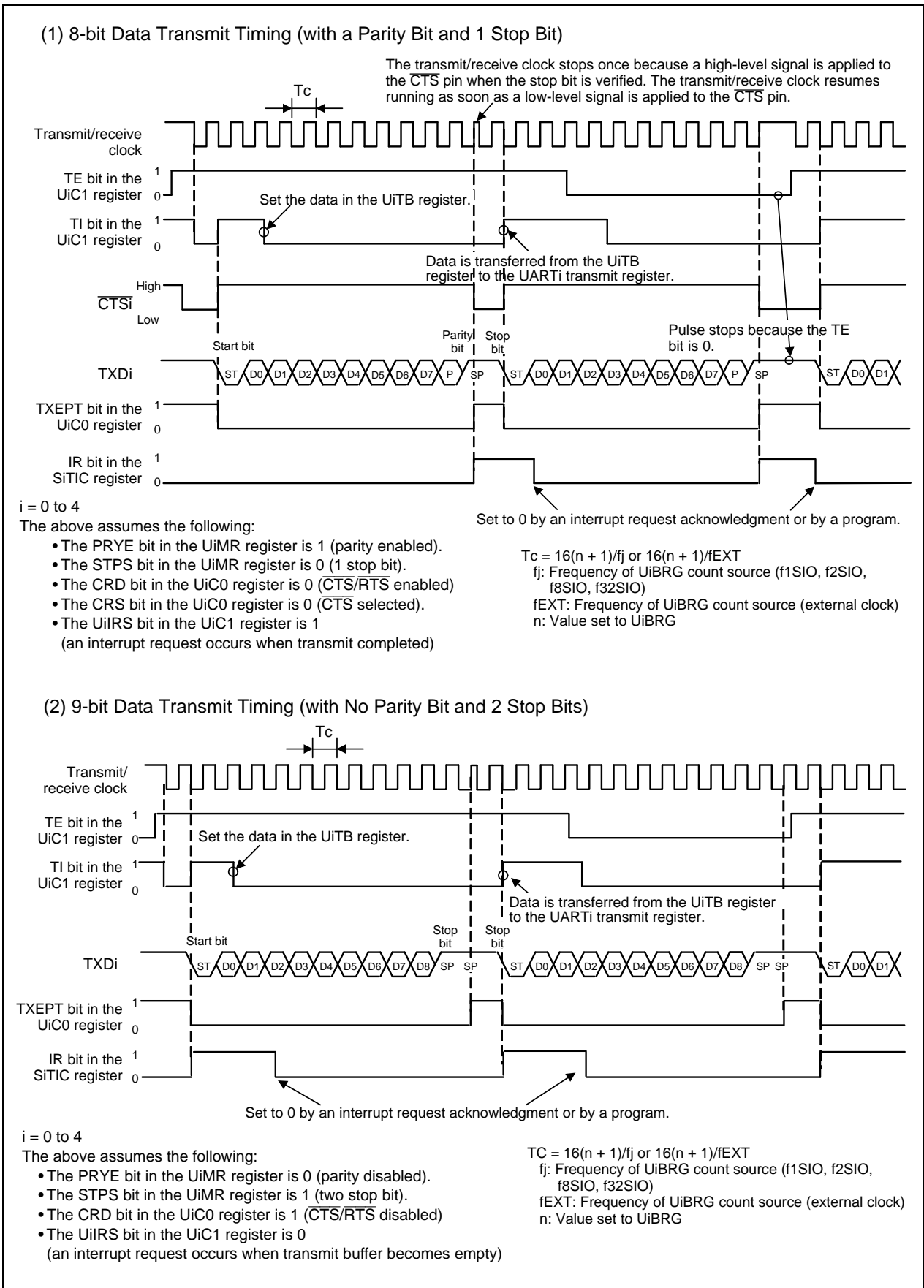
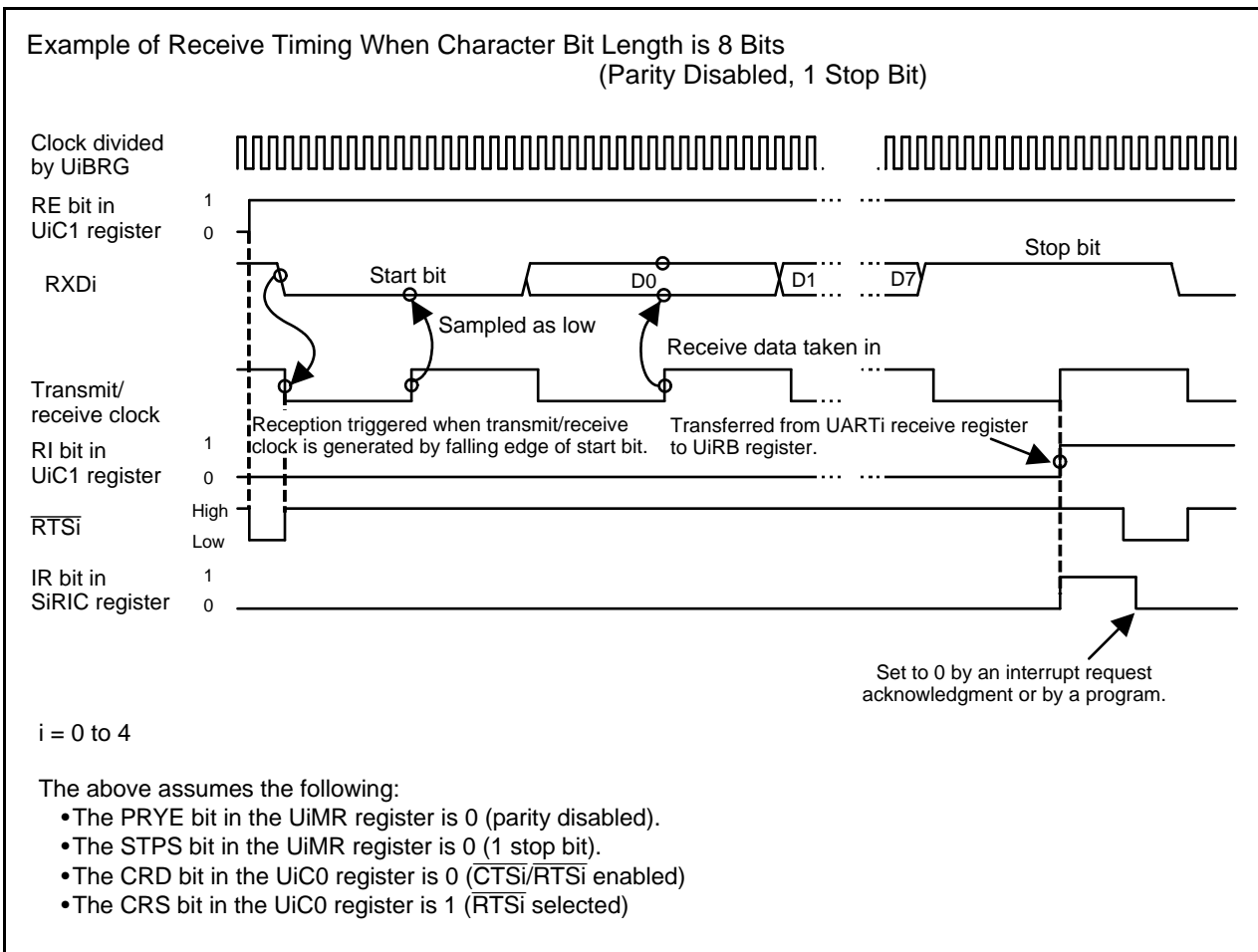


Figure 21.8 Transmit Timing in UART Mode



**Figure 21.9 Receive Timing in UART Mode**

### 21.3.2.1 Bit Rate

In UART mode, the frequency set by the UiBRG register (i = 0 to 4) divided by 16 becomes a bit rate.

The setting value (n) of the UiBRG register is calculated by the following formula:

$$n = \frac{f_j}{\text{bitrate}(\text{bps}) \times 16} - 1$$

$f_j = f1SIO, f2SIO, f8SIO, f32SIO$

$n = 00h \text{ to } FFh$

Table 21.11 lists Example Bit Rates and Settings.

**Table 21.11 Example of Bit Rates and Settings (1)**

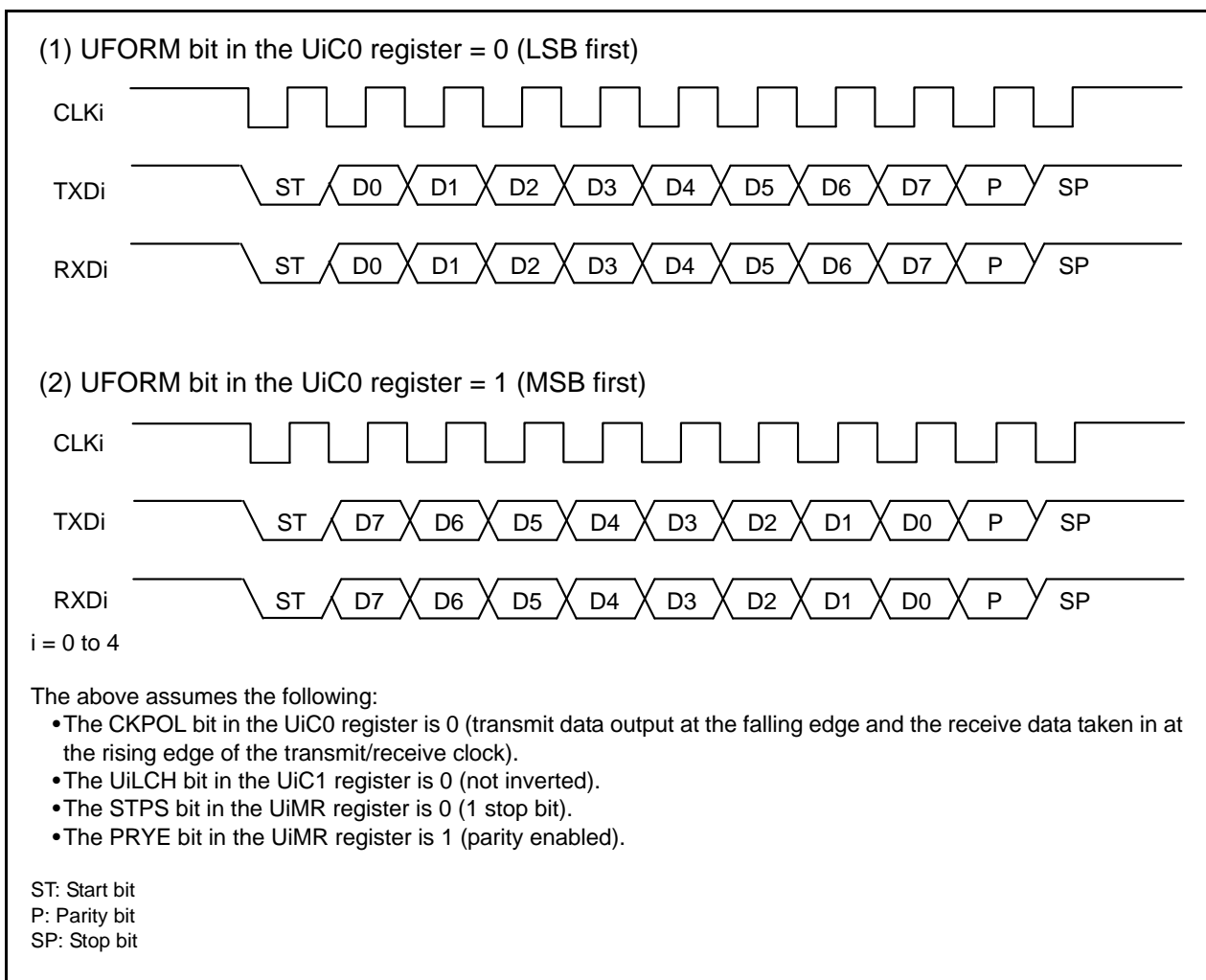
Bit Rate (bps)	Count Source of UiBRG	Peripheral Function Clock f1: 16 MHz		Peripheral Function Clock f1: 24 MHz	
		Set Value of UiBRG: n	Bit Rate (bps)	Set value of UiBRG: n	Bit Rate (bps)
1200	f8SIO	103 (67h)	1202	155 (9Bh)	1202
2400	f8SIO	51 (33h)	2404	77 (4Dh)	2404
4800	f8SIO	25 (19h)	4808	38 (26h)	4808
9600	f1SIO	103 (67h)	9615	155 (9Bh)	9615
14400	f1SIO	68 (44h)	14493	103 (67h)	14423
19200	f1SIO	51 (33h)	19231	77 (4Dh)	19231
28800	f1SIO	34 (22h)	28571	51 (33h)	28846
31250	f1SIO	31 (1Fh)	31250	47 (2Fh)	31250
38400	f1SIO	25 (19h)	38462	38 (26h)	38462
51200	f1SIO	19 (13h)	50000	28 (1Ch)	51724

Note:

1. Assumed that either the OCOSEL0 bit or OCOSEL1 bit in the UCLKSEL0 register is 0 (f1).

### 21.3.2.2 LSB First/MSB First Select Function

As shown in Figure 21.10, the bit order can be selected by setting the UFORM bit in the UiC0 register. This function is enabled when the character bit length is 8 bits.



**Figure 21.10 Bit Order**

### 21.3.2.3 Serial Data Logic Switching Function

The logic of the data written to the UiTB register is inverted and then transmitted. Similarly, the inverted logic of the received data is read when the UiRB register is read.

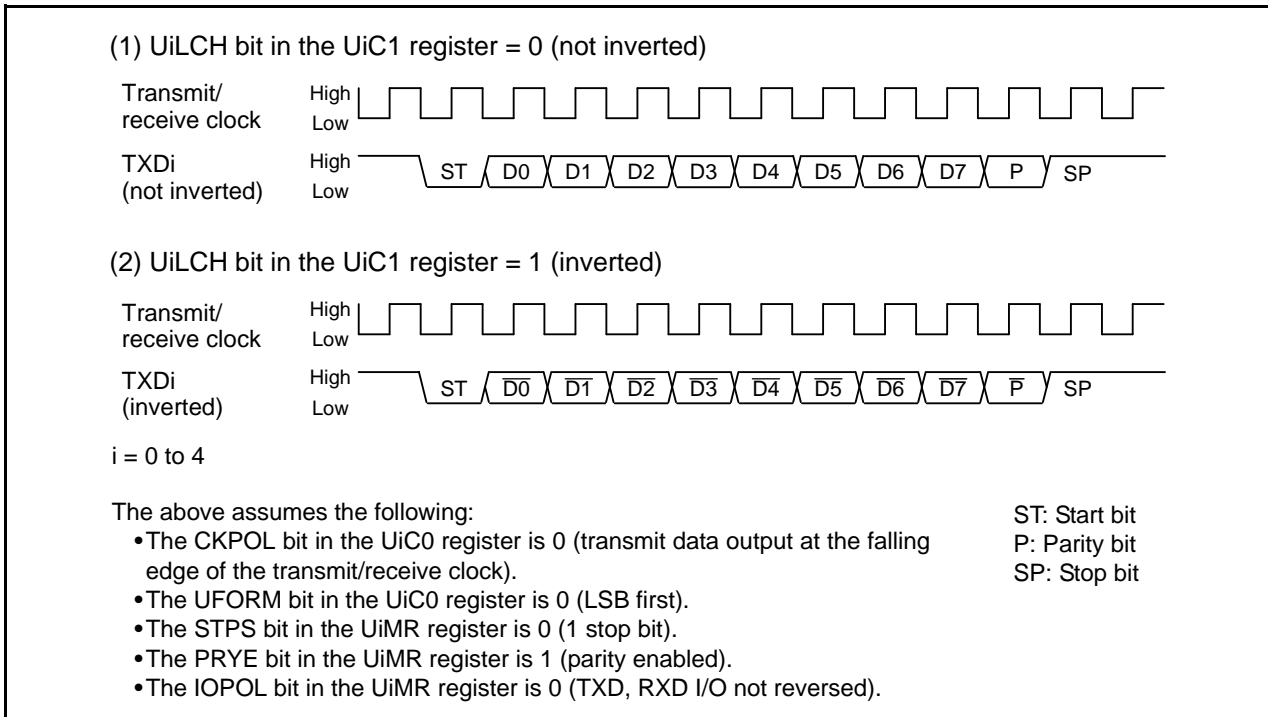


Figure 21.11 Serial Data Logic Switching

### 21.3.2.4 TXD and RXD I/O Polarity Reverse Function

This function reverses the polarities of the TXDi pin output and RXDi pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted.

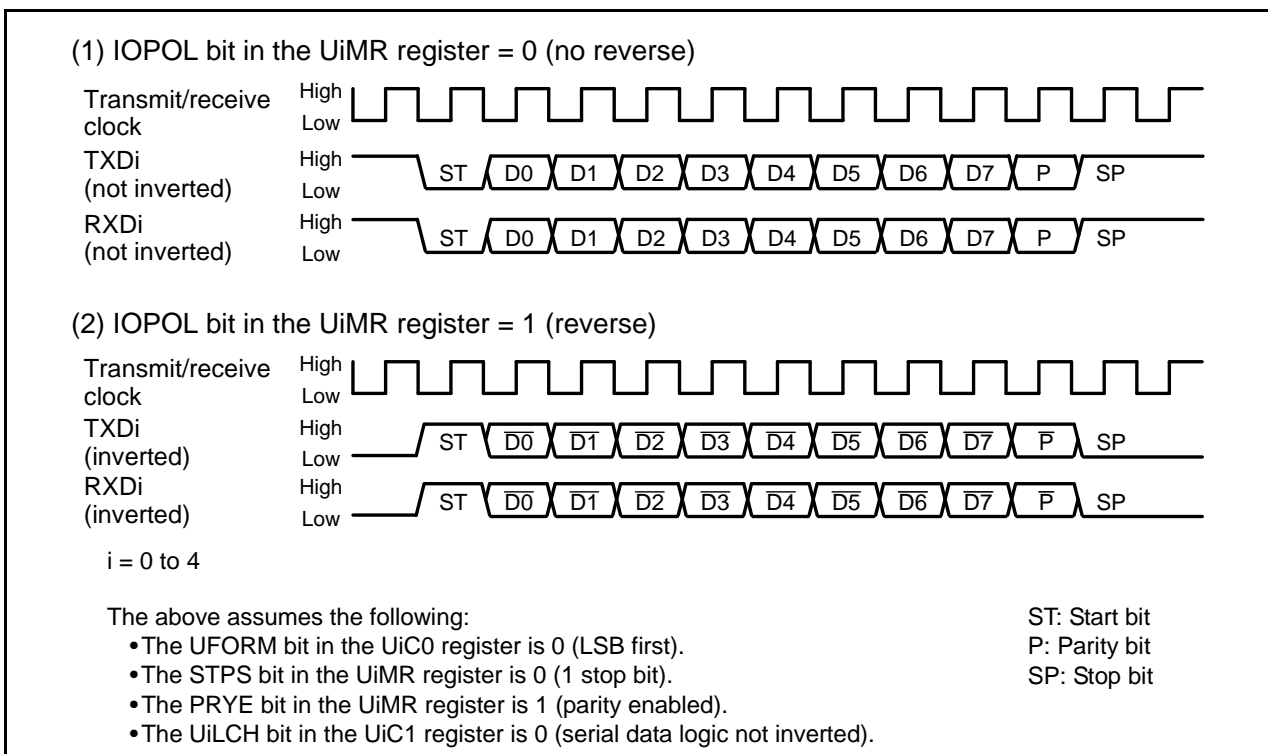


Figure 21.12 TXD and RXD I/O Polarity Inversion

### 21.3.2.5 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The  $\overline{\text{CTS}}$  function is used to start transmit operation when a low signal is applied to the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  (i = 0 to 3) pin. Transmit operation begins when input to the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  pin becomes low. If the input level is switched from low to high during transmit operation, the operation stops after the ongoing transmit/receive operation is completed.

When the  $\overline{\text{RTS}}$  function is selected, the  $\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$  pin outputs a low signal when the MCU is ready to receive. The output level becomes high when a start bit is detected.

See Table 21.9 "I/O Pin Functions in UART Mode".

### 21.3.2.6 Processing When Terminating Communication or When an Error Occurs

If communication is terminated in UART mode, or a communication error occurs, use following procedure reset communication:

- (1) Set the TE bit in the UiC1 (i = 0 to 4) register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
- (3) Set bits SMD2 to SMD0 in the UiMR register to 100b (UART mode character bit length is 7 bits), 101b (UART mode character bit length is 8 bits), and 110b (UART mode character bit length is 9 bits).
- (4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

### 21.3.3 Special Mode 1 (I<sup>2</sup>C Mode) (UART2)

I<sup>2</sup>C mode is compatible with the simplified I<sup>2</sup>C interface. Table 21.12 lists the I<sup>2</sup>C Mode Specifications. Table 21.14 and Table 21.15 list the Registers Used and Settings in I<sup>2</sup>C Mode. Table 21.16 lists the I<sup>2</sup>C Mode Functions. Figure 21.13 shows the I<sup>2</sup>C Mode Block Diagram.

As shown in Table 21.16, the MCU is placed in I<sup>2</sup>C mode by setting bits SMD2 to SMD0 in the U2MR register to 010b and the IICM bit in the U2SMR register to 1. Because SDA2 transmit output has a delay circuit attached, SDA2 output does not change state until SCL2 goes low and remains stably low.

**Table 21.12 I<sup>2</sup>C Mode Specifications**

Item	Specification
Data format	Character bit length: 8 bits
Transfer clock	<ul style="list-style-type: none"> <li>• Master mode The CKDIR bit in the U2MR register is 0 (internal clock): <math>f_j / (2(n+1))</math> <math>f_j = f1SIO, f2SIO, f8SIO, f32SIO</math> <math>n =</math> setting value of the U2BRG register (03h to FFh)</li> <li>• Slave mode The CKDIR bit is 1 (external clock): input from the SCL2 pin</li> </ul>
Transmit/receive clock	To start transmission, satisfy the following requirements <sup>(1)</sup> <ul style="list-style-type: none"> <li>• The TE bit in the U2C1 register is 1 (transmission enabled)</li> <li>• The TI bit in the U2C1 register is 0 (data present in U2TB register)</li> </ul>
Reception start conditions	To start reception, satisfy the following requirements <sup>(1)</sup> <ul style="list-style-type: none"> <li>• The RE bit in the U2C1 register is 1 (reception enabled)</li> <li>• The TE bit in the U2C1 register is 1 (transmission enabled)</li> <li>• The TI bit in the U2C1 register is 0 (data present in the U2TB register)</li> </ul>
Interrupt request generation timing	When a start condition, stop condition, ACK (acknowledge), or NACK (not-acknowledge) is detected.
Error detection	Overrun error <sup>(2)</sup> This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the eighth bit of the unit of next data.
Selectable functions	<ul style="list-style-type: none"> <li>• Arbitration lost Timing at which the ABT bit in the U2RB register is updated can be selected.</li> <li>• SDA2 digital delay No digital delay or a delay of 2 to 8 U2BRG count source clock cycles can be selected.</li> <li>• Clock phase setting With or without clock delay can be selected.</li> </ul>

Notes:

1. These requirements do not have to be set in any particular order. When transmission/reception is started as a slave and the TXEPT bit in the U2C0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.
2. If an overrun error occurs, the received data of the U2RB register will be undefined.



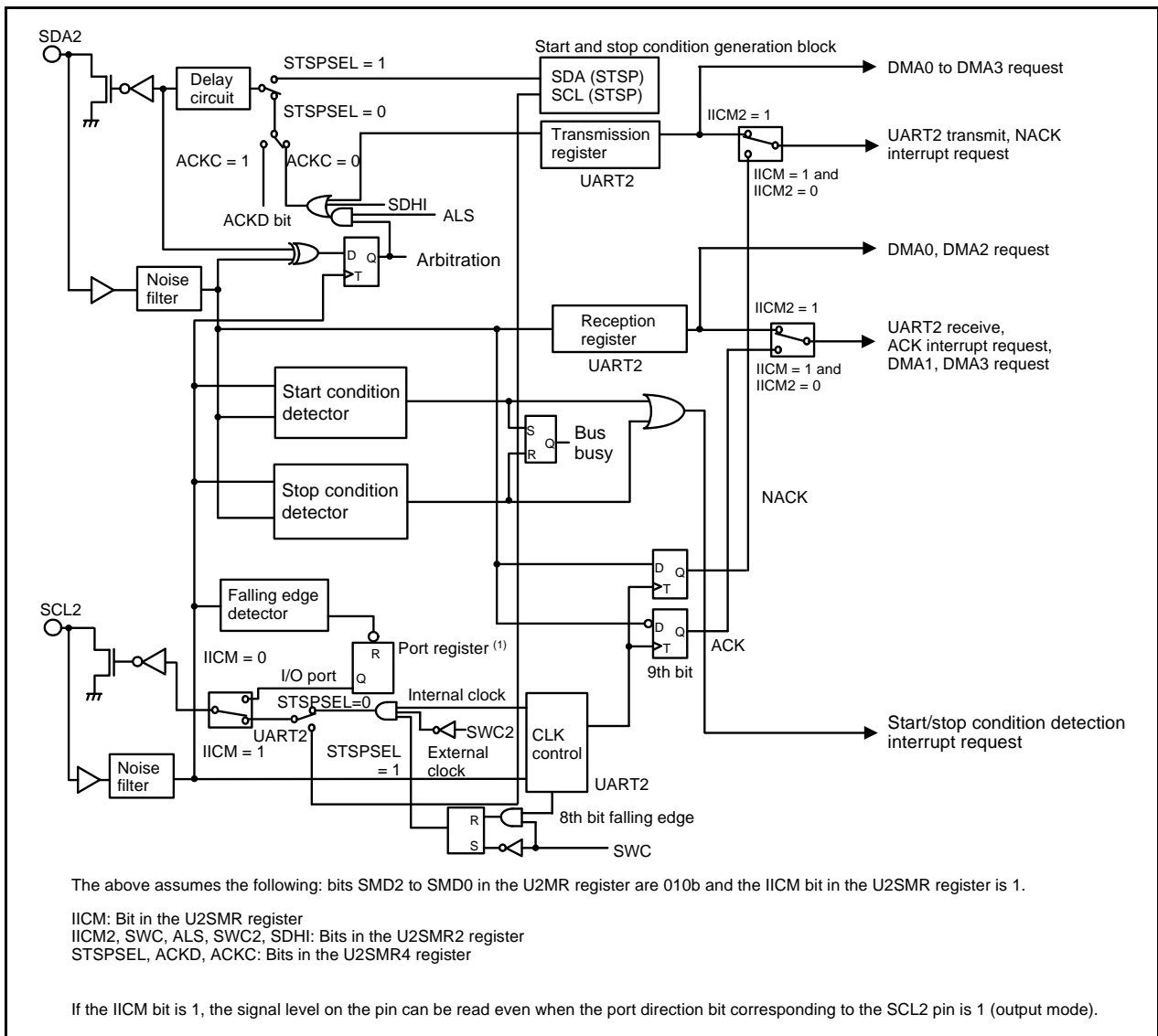


Figure 21.13 I<sup>2</sup>C Mode Block Diagram

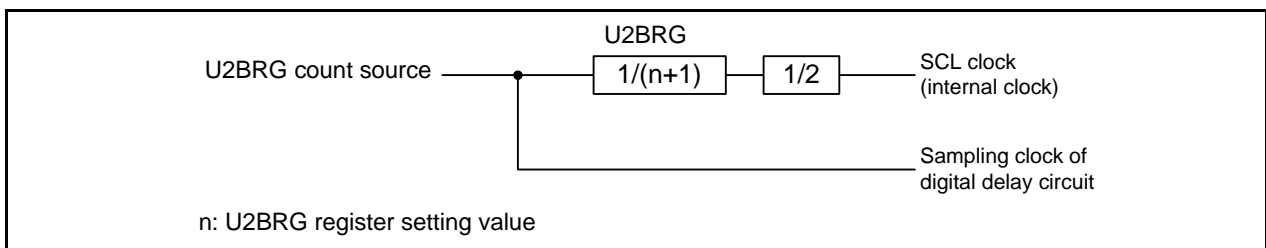


Figure 21.14 Internal Clock Configuration

Table 21.13 I/O Pin Functions in I<sup>2</sup>C Mode

Pin Name	I/O	Function
SCL2 (1, 2)	I/O	Clock input or output
SDA2 (1, 2)	I/O	Data input or output

Note:

1. Set the port direction bit sharing pin to 0.
2. Pins CLK2 and CTS2/RTS2 are not used (they can be used as I/O ports).

**Table 21.14 Registers Used and Settings in I<sup>2</sup>C Mode (1/2) (1)**

Register	Bits	Function	
		Master	Slave
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.	Select clock prior to division for UART0 to UART2.
PCLKR	PCLK1	Select the count source for the U2BRG register.	Select the count source for the U2BRG register.
U2TB	0 to 7	When transmitting, set the transmission data. When receiving, set FFh.	When transmitting, set the transmission data. When receiving, set FFh.
	8	When transmitting, set to 1. When receiving, set the value in the ACK bit.	When transmitting, set to 1. When receiving, set the value in the ACK bit.
U2RB	0 to 7	Reception data can be read.	Reception data can be read.
	8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	ABT	Arbitration lost detection flag	Disabled
	OER	Overrun error flag	Overrun error flag
	13 to 15	When read, the read value is undefined.	When read, the read value is undefined.
U2BRG	0 to 7	Set a bit rate.	Disabled
U2MR	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	4 to 6	Set to 0.	Set to 0.
	IOPOL	Set to 0.	Set to 0.
U2C0	CLK1, CLK0	Select the count source for the UiBRG register.	Disabled
	CRS	Disabled because CRD is 1	Disabled because CRD is 1
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD	Set to 1.	Set to 1.
	NCH	Set to 1.	Set to 1.
	CKPOL	Set to 0.	Set to 0.
U2C1	UFORM	Set to 1.	Set to 1.
	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Reception complete flag	Reception complete flag
	UjIRS	Set to 1.	Set to 1.
U2SMR	UjRRM, UiLCH, UiERE	Set to 0.	Set to 0.
	IICM	Set to 1.	Set to 1.
	ABC	Select the timing that arbitration lost is detected.	Disabled
	BBS	Bus busy flag	Bus busy flag
	3 to 7	Set to 0.	Set to 0.

Note:

1. This table does not describe a procedure.

**Table 21.15 Registers Used and Settings in I<sup>2</sup>C Mode (2/2) (1)**

Register	Bits	Function	
		Master	Slave
U2SMR2	IICM2	See Table 21.16 "I <sup>2</sup> C Mode Functions".	See Table 21.16 "I <sup>2</sup> C Mode Functions".
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCL2 output to low after receiving the eighth bit of the clock.	Set to 1 to fix SCL2 output to low after receiving the eighth bit of the clock.
	ALS	Set to 1 to stop SDA2 output when arbitration lost is detected.	Set to 0.
	STAC	Set to 0.	Set to 1 to initialize UART2 at start condition detection.
	SWC2	Set to 1 to forcibly pull SCL2 output low.	Set to 1 to forcibly pull SCL2 output low.
	SDHI	Set to 1 to disable SDA2 output.	Set to 1 to disable SDA2 output.
	7	Set to 0.	Set to 0.
U2SMR3	0, 2, 4 NODC	Set to 0.	Set to 0.
	CKPH	Set to 1.	Set to 1.
	DL2 to DL0	Set the amount of SDA2 digital delay.	Set the amount of SDA2 digital delay.
U2SMR4	STAREQ	Set to 1 to generate start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate restart condition.	Set to 0.
	STPREQ	Set to 1 to generate stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCL2 output when stop condition is detected.	Set to 0.
SWC9	Set to 0.	Set to 1 to set SCL2 to remain low at the falling edge of the ninth bit of clock.	

Note:

1. This table does not describe a procedure.

In I<sup>2</sup>C mode, functions and timings vary depending on the IICM2 bit setting in the U2SMR2 register. Figure 21.15 shows Transfer to U2RB Register and Interrupt Timing. See Figure 21.15 for the timing of transferring data to the U2RB register, the bit position of the data stored in the U2RB register, types of interrupts, interrupt requests, and DMA request generation timing.

Table 21.16 lists a comparison of other functions in clock synchronous serial I/O mode with I<sup>2</sup>C mode.

**Table 21.16 I<sup>2</sup>C Mode Functions**

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I <sup>2</sup> C Mode (SMD2 to SMD0 = 010b, IICM = 1)	
		IICM2 = 0 (NACK/ACK interrupt)	IICM2 = 1 (UART transmit/receive interrupt)
		CKPH = 1 (Clock delay)	CKPH = 1 (Clock delay)
Start and stop condition detect interrupts (3)	-	Start condition or stop condition detection (See Figure 21.17 "STSPSEL Bit Functions")	
Transmission, NACK interrupt (2, 3)	UART2 transmission Transmission started or completed (selected by U2IRS)	No acknowledgment detection (NACK) Rising edge of the 9th bit of SCL2	UART2 transmission Falling edge of the 9th bit of SCL2
Reception, ACK interrupt (2, 3)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of the 9th bit of SCL2	UART2 reception Falling edge of the 9th bit of SCL2
Timing for transferring data from UART reception shift register to U2RB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of the 9th bit of SCL2	Falling edges of the 8th bit of SCL2 and rising edges of the 9th bit of SCL2
UART2 transmission output delay	Not delayed	Delayed	Delayed
Read RXD2 and SCL2 pin levels	Possible when the corresponding port direction bit = 0	Always possible no matter how the corresponding port direction bit is set	Always possible no matter how the corresponding port direction bit is set
Initial value of TXD2 and SDA2 outputs	CKPOL = 0 (high) CKPOL = 1 (low)	The value set in the port register before setting I <sup>2</sup> C mode (1)	The value set in the port register before setting I <sup>2</sup> C mode (1)
Initial and end values of SCL2	-	Low	Low
DMA1, DMA3 factor (2)	UART2 reception	Acknowledgment detection (ACK)	UART2 reception Falling edge of the 9th bit of SCL2
Read received data	1st to 8th bits of the received data are stored in bits 0 to 7 in the U2RB register.	1st to 8th bits of the received data are stored in bits 7 to 0 in the U2RB register.	Refer to Figure 21.15 "Transfer to U2RB Register and Interrupt Timing".

SMD2 to SMD0: Bits in the U2MR register

CKPOL: Bit in the U2C0 register

IICM: Bit in the U2SMR register

IICM2: Bit in the U2SMR2 register

CKPH: Bit in the U2SMR3 register

U2IRS: Bit in the U2C1 register

Notes:

- Set the initial value of SDA2 output while bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- See Figure 21.15 "Transfer to U2RB Register and Interrupt Timing".
- The procedure to change interrupt sources is as follows:
  - Disable the interrupt to be changed the source.
  - Change the source of interrupt.
  - Set the IR bit in the interrupt control register of that interrupt to 0 (no interrupt requested).
  - Set bits ILVL2 to ILVL0 in the interrupt control register of that interrupt.

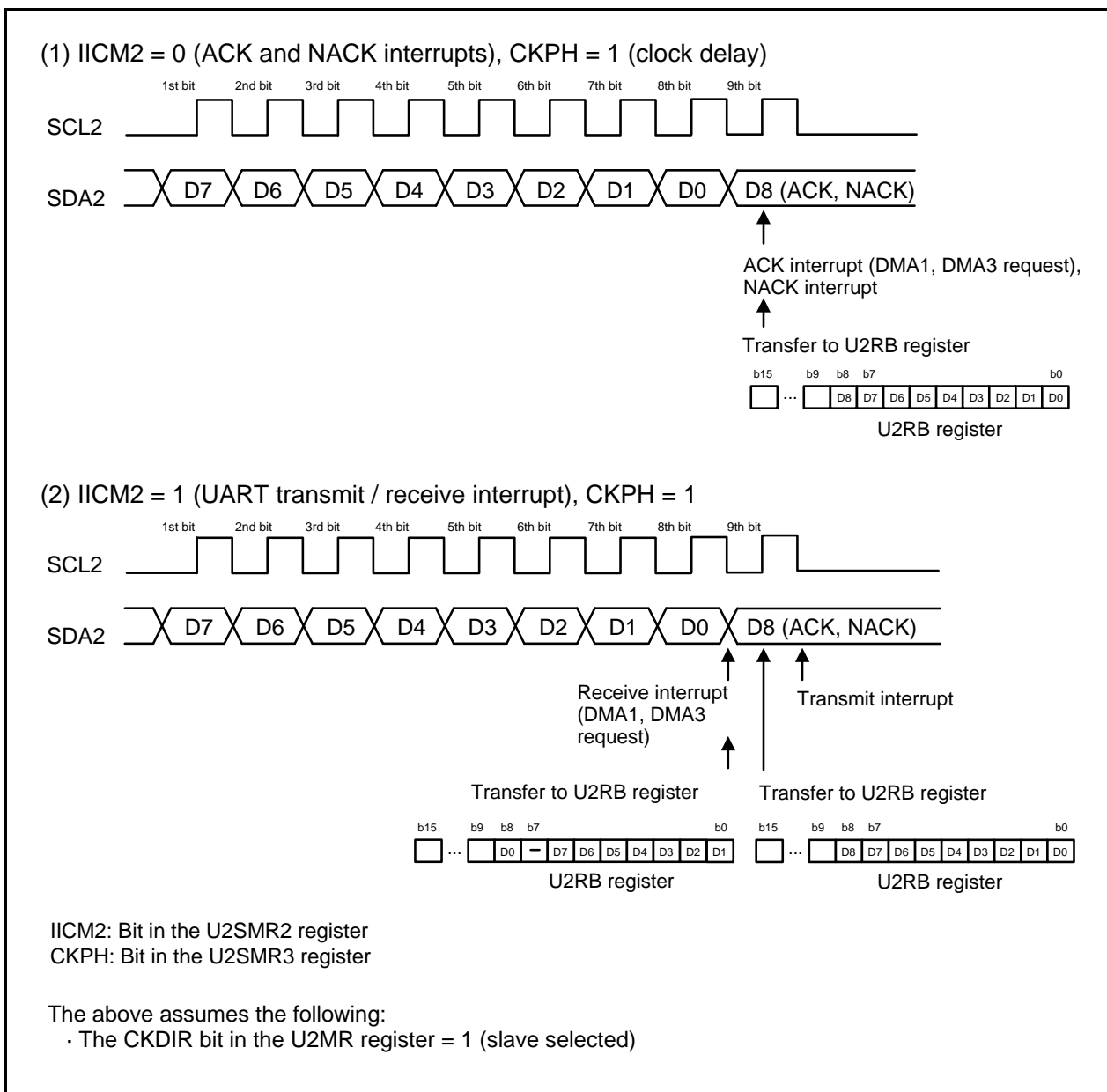


Figure 21.15 Transfer to U2RB Register and Interrupt Timing

### 21.3.3.1 Detecting Start and Stop Conditions

Start and stop conditions are detected by their respective detectors.

Whether a start or a stop condition has been detected is determined.

A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.

Because the start and stop condition detect interrupts share the interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt. To detect a start or stop condition, both the set-up and hold times require at least six cycles of the BRG2 count source as shown in Figure 21.16. To meet the condition for the Fast-mode specification, the BRG2count source must be at least 10 MHz.

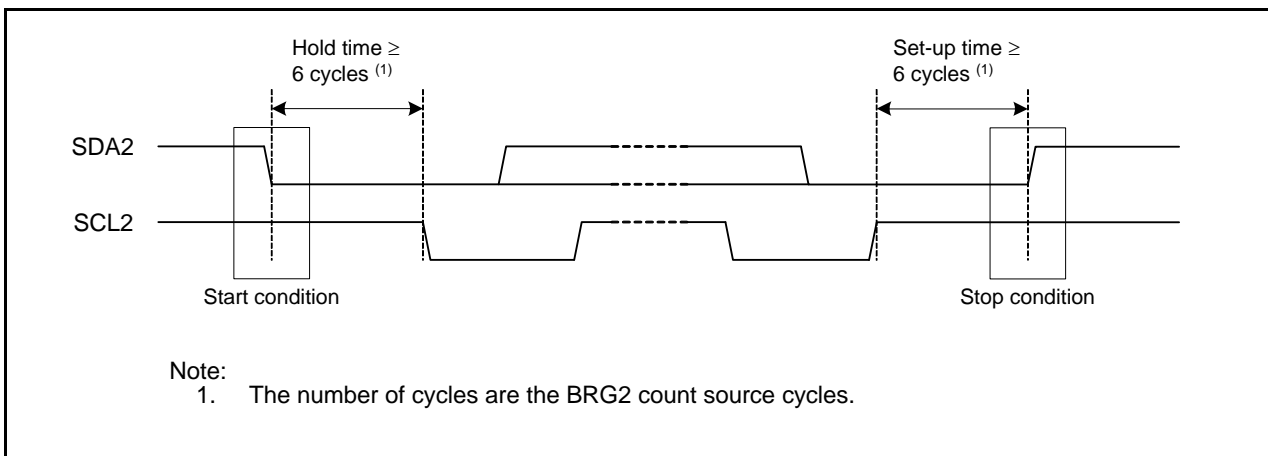


Figure 21.16 Detecting Start and Stop Conditions

### 21.3.3.2 Generating Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).

A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).

A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is described below.

- (1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).
- (2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).

The functions of the STSPSEL bit are shown in Table 21.17 and Figure 21.17.

Table 21.17 STSPSEL Bit Functions

Function	STSPSEL = 0	STSPSEL = 1
Output of pins SCL2 and SDA2	Output of transmit/receive clock and data Output of start/stop condition is accomplished by a program using ports (not automatically generated in hardware)	Output of a start/stop condition according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition Interrupt request generation timing	Detection of start/stop condition	Completion of generating start/stop condition

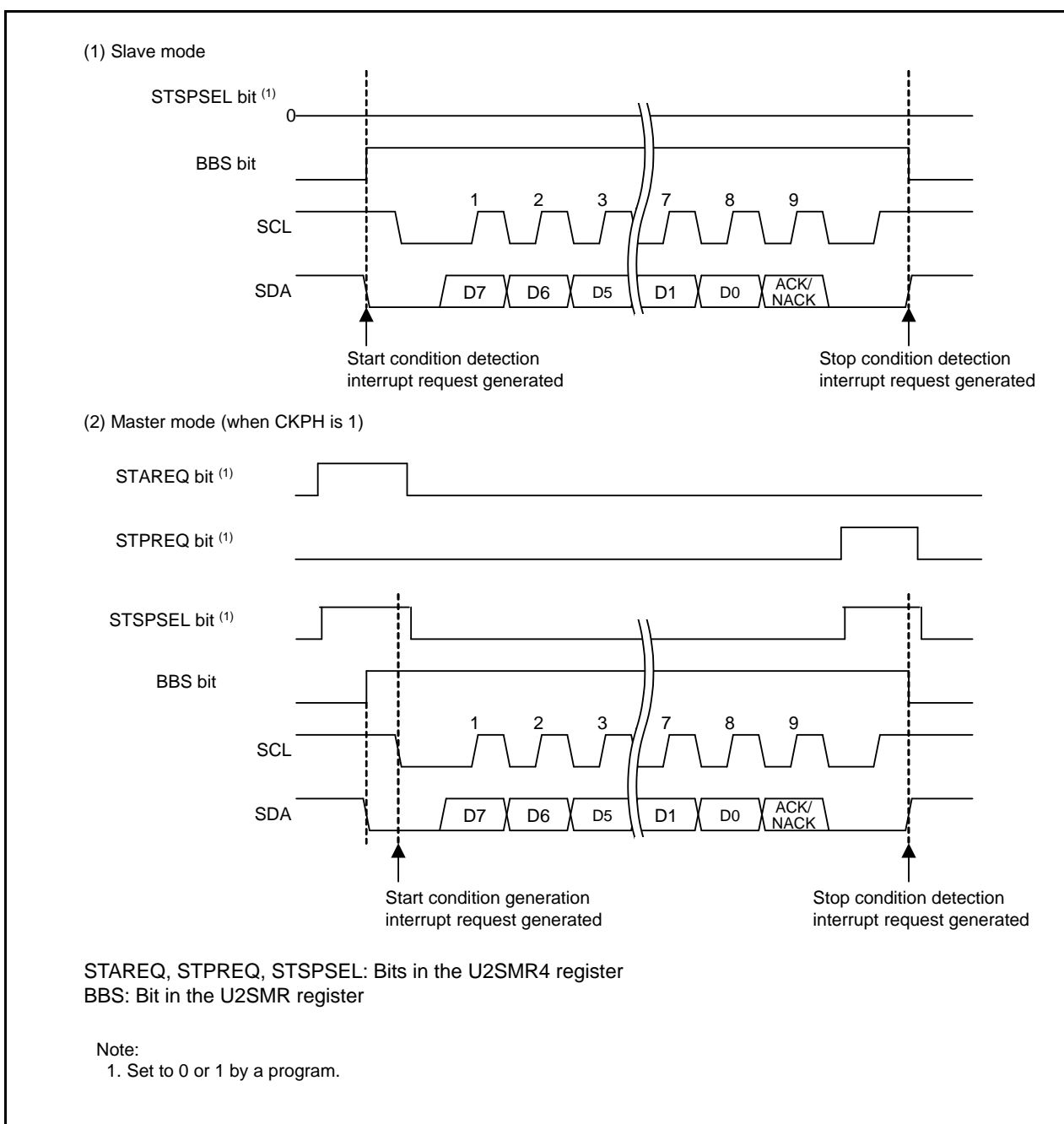
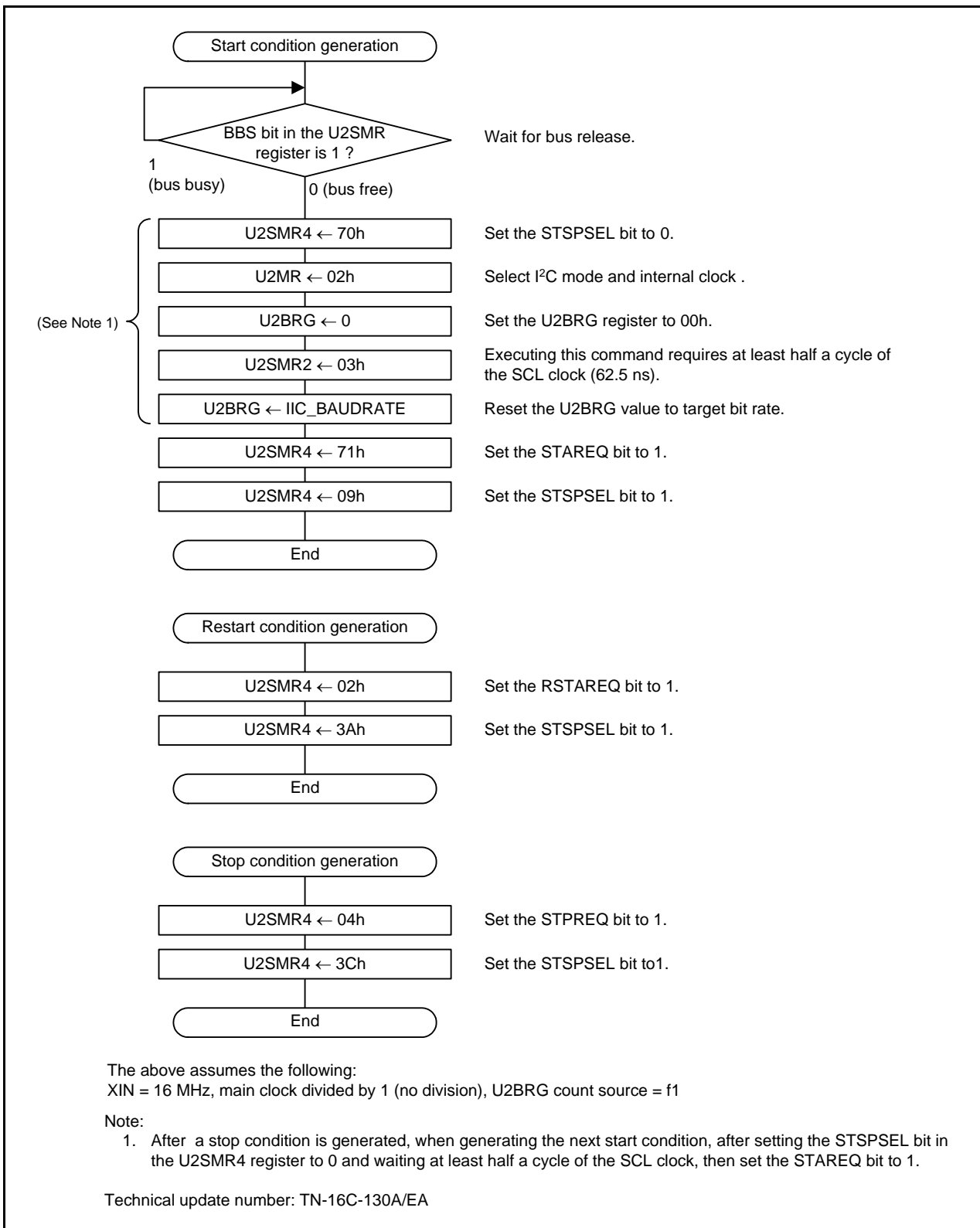


Figure 21.17 STSPSEL Bit Functions



**Figure 21.18 Register Setting Procedures for Condition Generation**



### 21.3.3.3 Arbitration

The MCU determines whether the transmit data matches data input to the SDA2 pin on the rising edge of SCL2. If it does not match the input data, arbitration takes place at the SDA2 pin by stopping data output.

The ABC bit in the U2SMR register determines the update timing for the ABT bit in the U2RB register. When the ABC bit is 0 (update per bit), the ABT bit becomes 1 as soon as a data discrepancy is detected. If not detected, the ABT bit becomes 0. When the ABC bit is 1 (update per byte), the ABT bit becomes 1 on the falling edge of the eighth bit of SCL2 if any discrepancy is detected. In this ABC bit setting, the ABT bit should be set to 0 after ACK detection of 1-byte is completed to start the next 1-byte transmission/reception.

When the ALS bit in the U2SMR2 register is set to 1 (SDA output stop enabled), an arbitration lost occurs. As soon as the ABT bit becomes 1, the SDA2 pin becomes high-impedance.

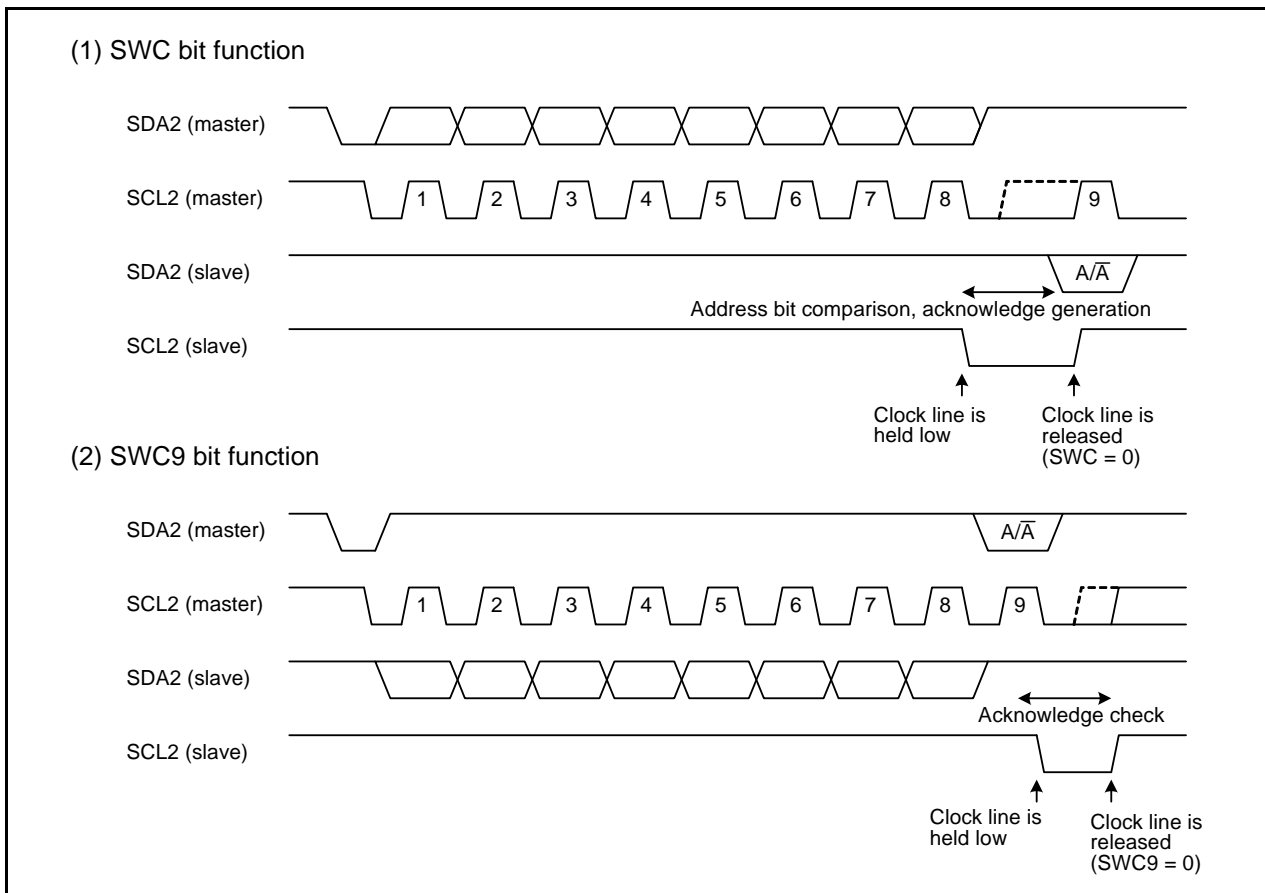
### 21.3.3.4 SCL Control and Clock Synchronization

Data transmission/reception in I<sup>2</sup>C mode uses the transmit/receive clock as shown in Figure 21.15 "Transfer to U2RB Register and Interrupt Timing". The clock speed increase makes it difficult to secure the required time for ACK generation and data transmit procedure. The I<sup>2</sup>C mode supports a function of wait-state insertion to secure this required time and a function of clock synchronization with a wait-state inserted by other devices.

The SWC bit in the U2SMR2 register is used to insert a wait-state for ACK generation. When the SWC bit is set to 1 (the SCL2 pin is held low after the eighth bit of SCL2 is received), the SCL2 pin is held low on the falling edge of the eighth bit of SCL2. When the SWC bit is set to 0 (no wait-state/wait-state cleared), the SCL2 line is released.

When the SWC2 bit in the U2SMR2 register is set to 1 (the SCL2 pin is held low), the SCL2 pin is forced low even during transmission or reception. When the SWC2 bit is set to 0 (transmit/receive clock is output at the SCL2 pin), the SCL2 line is released to output the transmit/receive clock.

The SWC9 bit in the U2SMR4 register is used to insert a wait-state for checking received acknowledge bits. While the CKPH bit in the U2SMR3 register is 1 (clock delayed), when the SWC9 bit is set to 1 (the SCL2 pin is held low after the ninth bit of the SCL2 is received), the SCL2 pin is held low on the falling edge of the ninth bit of SCL2. When the SWC9 bit is set to 0 (no wait-state/wait-state cleared), the SCL2 line is released.



**Figure 21.19** Inserting Wait-States Using Bits SWC and SWC9

The CSC bit in the U2SMR2 register synchronizes an internally generated clock with the clock applied to the SCL2 pin. For example, if a wait-state is inserted from other devices, the two clocks are not synchronized. While the CSC bit is 1 (clock synchronization enabled) and the internal clock is held high, when a high at the SCL2 pin changes to low, the internal clock becomes low in order to reload the U2BRG register value and resume counting. While the SCL2 pin is held low, when the internal clock changes from low to high, the count is stopped until the SCL2 pin becomes high. That is, the UART2 transmit/receive clock is the logical AND of the internal clock and SCL2. The synchronized period starts from one clock prior to an internally generated clock and ends when the ninth clock is completed. The CSC bit can be set to 1 only when the CKDIR bit in the U2MR register is set to 0 (internal clock selected).

The SCLHI bit in the U2SMR4 register is used to leave the SCL2 pin open when another master generates a stop condition while the master is performing a transmit/receive operation. While the SCLHI bit is set to 1 (output stopped), the SCL2 pin is open (the pin is high-impedance) when a stop condition is detected and the clock output is stopped.

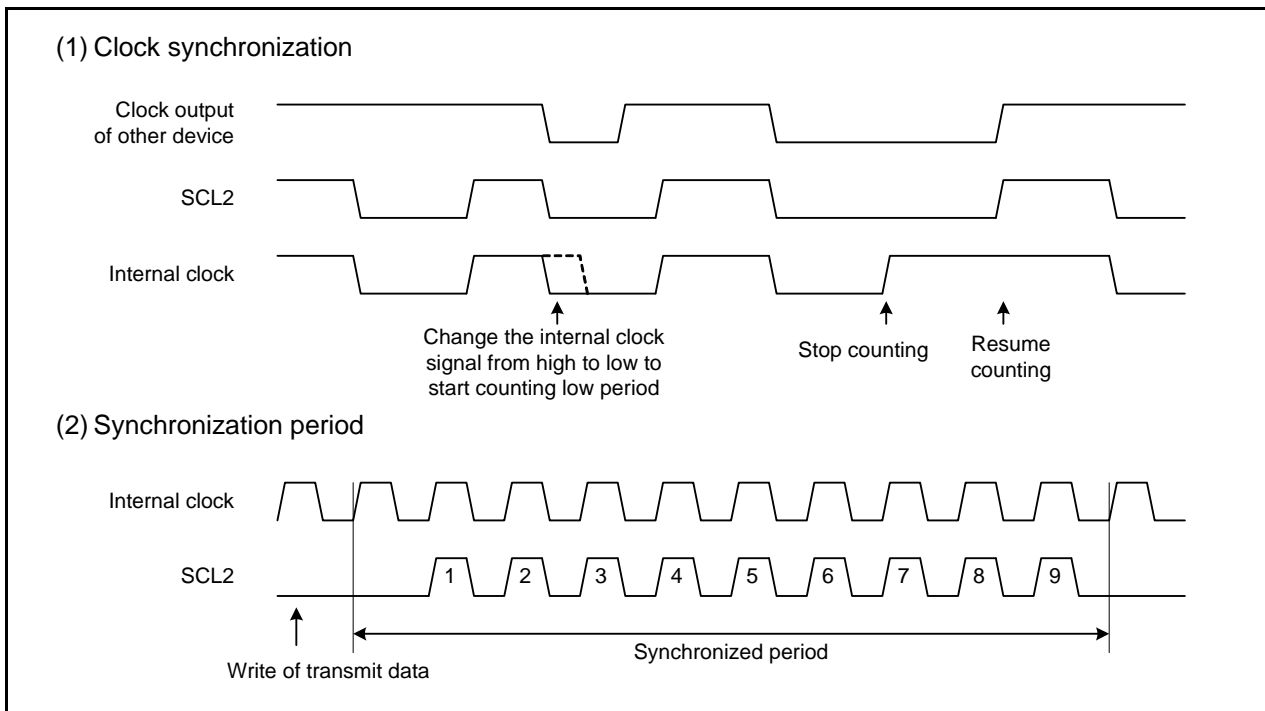


Figure 21.20 Clock Synchronization

### 21.3.3.5 SCL Clock Frequency

The SCL clock duty generated in I<sup>2</sup>C mode is 50%. The low-level width of the SCL clock is 1.25  $\mu$ s when the I<sup>2</sup>C-bus setting is Fast-mode maximum SCL clock (400 kbps). This value does not satisfy the Fast-mode I<sup>2</sup>C-bus specification ( $f_{LOW}$  = minimum 1.3  $\mu$ s). Set the SCL clock to 384.6 kbps or less to satisfy the SCL clock low-level width of 1.3  $\mu$ s or more.

When the clock synchronous function (Figure 21.20 “Clock Synchronization”) is enabled, there is a sampling delay of the noise filter plus 1 to 1.5 cycles of U2BRG count source.

There is also a delay of the SCL clock when high is determined and the SCL clock high width is extended. Therefore, the actual SCL clock becomes slower than SCL clock bit rate setting.

To calculate the effective value of SCL clock, take the SCL clock rise time ( $t_R$ ) into consideration.

The following is an example of an SCL clock calculation.

Example of an effective value of SCL clock calculation at 384.6 kbps

- U2BRG count source:  $f_1 = 20$  MHz
- U2BRG register setting value:  $n = 26 - 1$
- SCL clock rise time:  $t_R = 100$  ns
- SCL clock fall time:  $t_F = 0$  ns
- Noise filter width:  $t_{NF} = 100$  ns (1)
- Sampling delay:  $t_{SD} = 1$  cycle

$$f_{SCL} \text{ (theoretical value)} = f_1 / (2(n + 1)) = 20 \text{ MHz} / (2(25 + 1)) = 384.6 \text{ kbps}$$

$$t_{LOW} = 1 / (2f_{SCL} \text{ (theoretical value)}) = 1 / (2 \times 384.6 \text{ kbps}) = 1.3 \mu\text{s}$$

$$\begin{aligned} t_{HIGH} &= 1 / (2f_{SCL} \text{ (theoretical value)}) + t_{NF} + (t_{SD} \times 1 / f_1) \\ &= 1 / (2 \times 384.6 \text{ kbps}) + 100 \text{ ns} + (1 \times 1 / 20 \text{ MHz}) \\ &= 1.45 \mu\text{s} \end{aligned}$$

$$f_{SCL} \text{ (actual value)} = 1 / (t_F + t_{LOW} + t_R + t_{HIGH}) = 1 / (0 \text{ ns} + 1.3 \mu\text{s} + 100 \text{ ns} + 1.45 \mu\text{s}) \approx 350.8 \text{ kbps}$$

Note:

1. Maximum 200 ns.

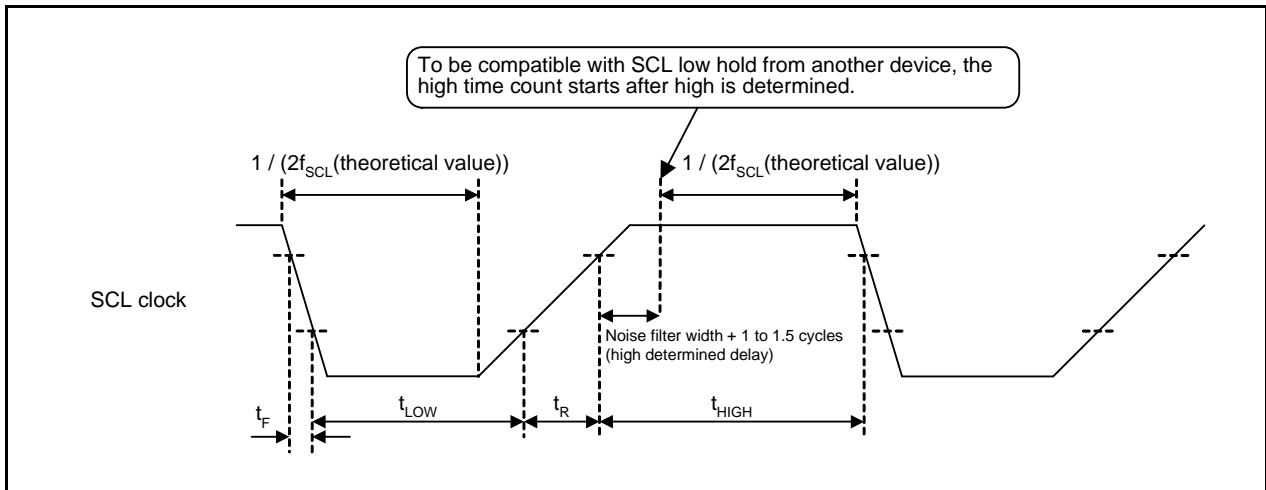


Figure 21.21 SCL Clock

### 21.3.3.6 SDA Output Control

When transmitting byte data, the SDA2 pin outputs transmit data for the first to eighth bits, and it is released to receive an acknowledgment for the ninth bit.

In I<sup>2</sup>C mode, set 9-bit data to the U2TB register. In 9-bit data, set the transmit data to bits b7 to b0 and set b8 to 1. By setting the UFORM bit in the U2C0 register to 1 (MSB first) and 9-bit data to the U2TB register, transmit data is output from the SDA2 pin in the following order: b7, b6, b5, b4, b3, b2, b1, b0 and b8. As b8 is 1, the SDA2 pin becomes high-impedance at the ninth bit and an acknowledgment can be received.

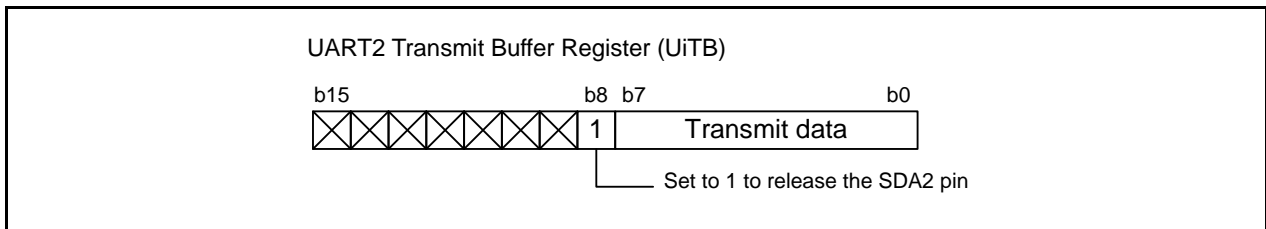


Figure 21.22 U2TB Register Setting (SDA Output)

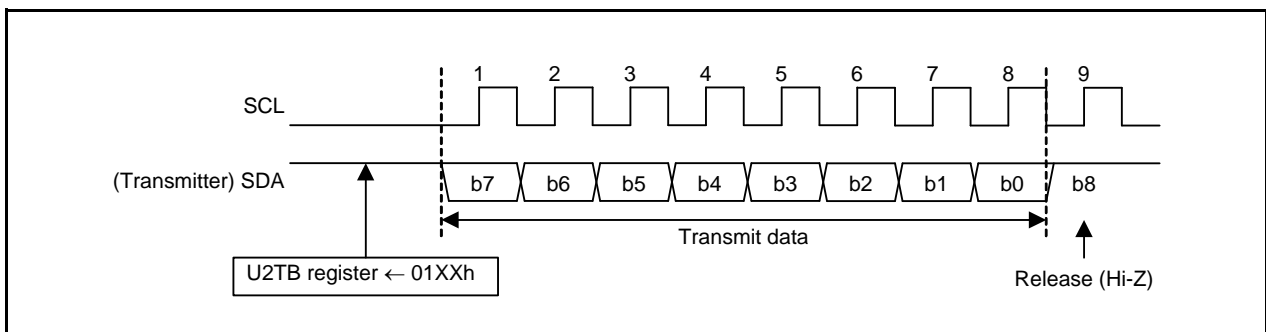


Figure 21.23 Byte Data Transmission

Set bits DL2 to DL0 in the U2SMR3 register to add no delays or a delay of one to eight U2BRG count source clock cycles to SDA2 output.

Setting the SDHI bit in the U2SMR2 register to 1 (SDA output disabled) forcibly places the SDA2 pin in a high-impedance state. Do not write to the SDHI bit at the rising edge of the UART2 transmit/receive clock as the ABT bit in the U2RB register may inadvertently become 1 (detected).

### 21.3.3.7 SDA Digital Delay

When transferring data with the I<sup>2</sup>C-bus, change the data while the SCL clock is low. When SDA is changed while the SCL clock is a high, the change is recognized as one of the corresponding conditions (see 21.5.3.3 “Setup and Hold Times When Generating a Start/Stop Condition”).

This function delays output from the SDA2 pin. By delaying the change of the SDA, the data can be changed while the SCL clock is low. This function is enabled by setting bits DL2 to DL0 in the U2SMR3 register to 001b to 111b, and disabled by setting them to 000b.

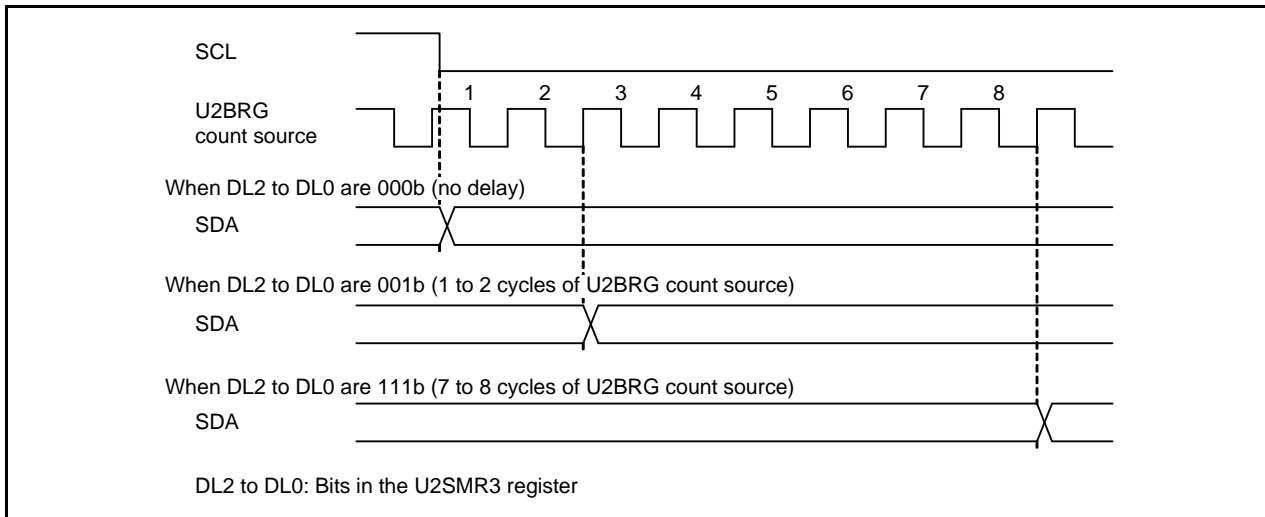


Figure 21.24 SDA Output Selection by Setting Bits DL2 to DL0

### 21.3.3.8 SDA Input

When the IICM2 bit in the U2SMR2 register is set to 0, the first 8 bits of received data (D7 to D0) are stored in bits 7 to 0 in the U2RB register and the ninth bit (ACK/NACK) is stored in bit 8.

When the IICM2 bit is 1, the first to seventh bits (D7 to D1) of the received data are stored in bits 6 to 0 in the U2RB register and the eighth bit (D0) is stored in bit 8 in the U2RB register. Even when the IICM2 bit is 1, if the CKPH bit in the U2SMR3 register is 1, the same data as when the IICM2 bit is 0 can be read. To read the data, read the U2RB register after the rising edge of ninth bit of the corresponding clock pulse.

When receiving byte data, the SDA2 pin is released for the first to eighth bits to receive data, and an acknowledgment is generated for the ninth bit. NACK is generated when the last byte data is received in master mode, or when the slave address does not match in slave mode. In all other cases, ACK is generated.

In I<sup>2</sup>C mode, set 9-bit data to the U2TB register. In 9-bit data, set FFh to b7 to b0 to release the SDA2 pin and set b8 to 0 to generate ACK or 1 to generate NACK.

By setting 00FFh or 01FFh as 9-bit data to the U2TB register, the SDA2 pin becomes high-impedance for the first to eighth bits, and data can be received. ACK or NACK is generated at the ninth bit.

Read the received data from the U2RB register. When the clock delay function is used, data transfer to the U2RB register occurs twice and each U2RB register value is different. Refer to Figure 21.15 “Transfer to U2RB Register and Interrupt Timing” for details.

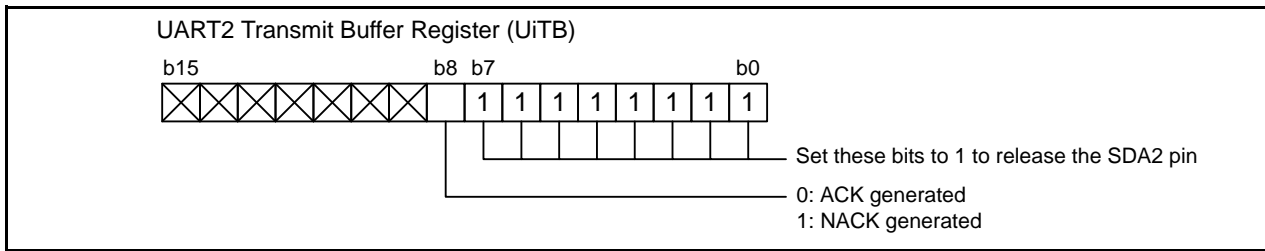


Figure 21.25 UiTB Register Setting (SDA Input)

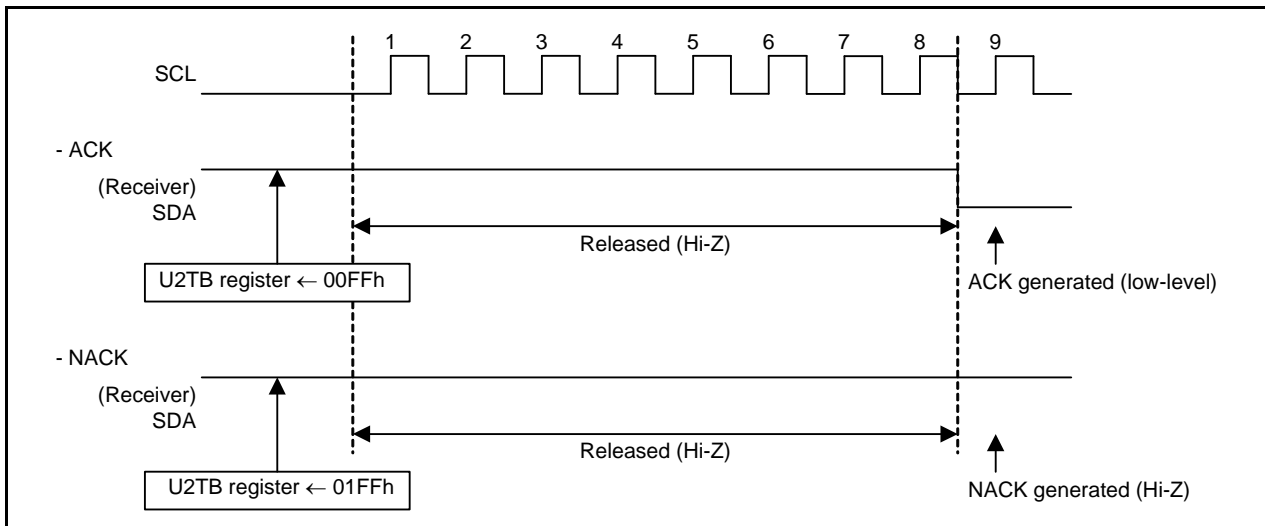


Figure 21.26 Byte Data Reception

### 21.3.3.9 ACK and NACK

When data is to be received, ACK is output after 8 bits are received by setting the U2TB register to 00FFh as dummy data. When the STSPSEL bit in the U2SMR4 register is set to 0 (serial I/O circuit selected) and the ACKC bit is set to 1 (ACK data output), the value of the ACKD bit is output at the SDA2 pin.

If the IICM2 bit is 0, a NACK interrupt request is generated when the SDA2 pin is held high at the rising edge of the ninth bit of SCL2. An ACK interrupt request is generated when the SDA2 pin is held low.

If the DMA request source is "UART2 receive interrupt request or ACK interrupt request", the DMA transfer is activated when ACK is detected.

### 21.3.3.10 Initialization of Transmission/Reception

Select the external clock as the transmit/receive clock when using this function.

If a start condition is detected while the STAC bit in the U2SMR2 register is 1 (initialize the circuit if the start condition is detected), the serial interface operates as follows:

- The transmit shift register is initialized, and the U2TB register value is transferred to the transmit shift register. Doing so starts the data transmission when the next clock pulse is applied. However, the UART2 output value does not change until the first bit of data is output synchronously with the input clock. It remains the same as when a start condition was detected.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit becomes 1 (hold the SCL2 pin low after the eighth bit of SCL2 is received).

Consequently, the SCL2 pin is pulled low at the falling edge of the ninth clock pulse.

When UART2 transmission/reception is started using this function, the TI bit does not change.

When the UART2 initializing function is used in slave mode, UART2 is initialized automatically when a start condition is detected. Therefore, an interrupt is unnecessary for detecting a start condition.

### 21.3.4 Special Mode 2 (UART2)

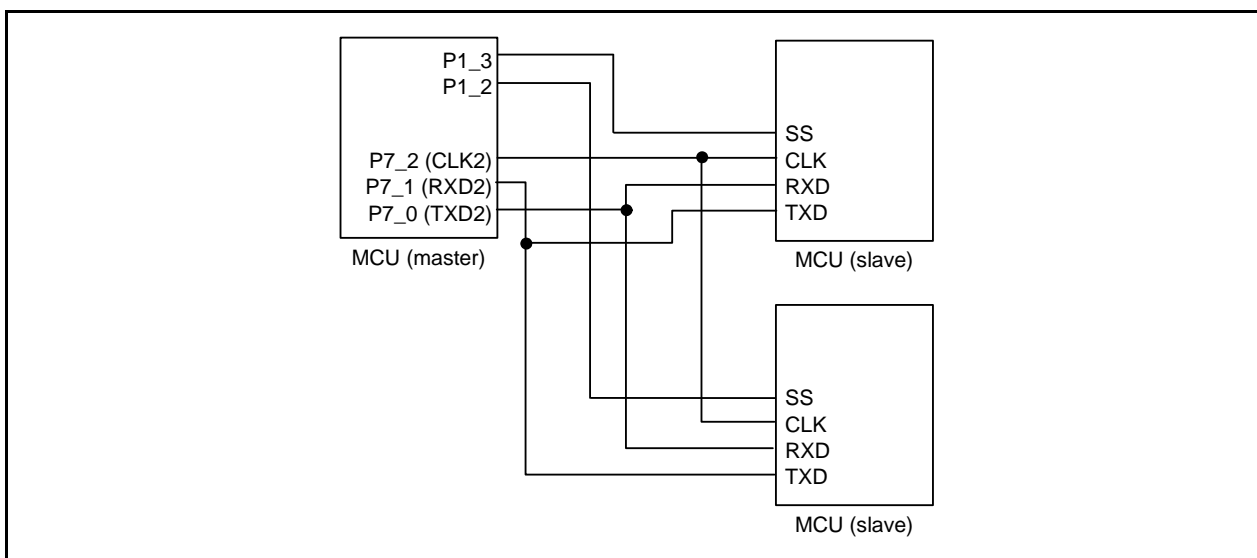
In special mode 2, the serial interface module allows serial communication between one master and multiple slaves. The transmit/receive clock polarity and phase are selectable. Table 21.18 lists Special Mode 2 Specifications.

**Table 21.18 Special Mode 2 Specifications**

Item	Specification
Data format	Character data length: 8 bits
Transmit/receive clock	<ul style="list-style-type: none"> <li>Master mode</li> </ul> The CKDIR bit in the U2MR register = 0 (internal clock): $\frac{f_j}{2(n+1)}$ $f_j = f1SIO, f2SIO, f8SIO, f32SIO$ $n$ : Setting value of U2BRG register 00h to FFh
Transmit/receive control	Controlled by I/O ports
Transmission start conditions	To start transmission, satisfy the following requirements: <ul style="list-style-type: none"> <li>The TE bit in the U2C1 register is 1 (transmission enabled)</li> <li>The TI bit in the U2C1 register is 0 (data present in U2TB register)</li> </ul>
Reception start conditions	To start reception, satisfy the following requirements: <ul style="list-style-type: none"> <li>The RE bit in the U2C1 register is 1 (reception enabled)</li> <li>The TE bit is 1 (transmission enabled)</li> <li>The TI bit is 0 (data present in the U2TB register)</li> </ul>
Interrupt request generation timing	For transmit interrupt, one of the following conditions can be selected <ul style="list-style-type: none"> <li>The U2IRS bit in the U2C1 register is 0 (transmit buffer empty): When transferring data from the U2TB register to the UART2 transmit register (at start of transmission)</li> <li>The U2IRS bit is 1 (transfer completed): When the serial interface completed sending data from the UART2 transmit register</li> </ul> For receive interrupt <ul style="list-style-type: none"> <li>When transferring data from the UART2 receive register to the U2RB register (at completion of reception)</li> </ul>
Error detection	Overrun error <sup>(1)</sup> This error occurs if the serial interface starts receiving the next data before reading the U2RB register and receives the 7th bit of the next data
Selectable functions	<ul style="list-style-type: none"> <li>CLK polarity selection Whether transfer data is output/input at the rising or falling edge of the transfer clock can be selected.</li> <li>LBS first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7.</li> <li>Continuous receive mode selection Reception is enabled by reading the U2RB register</li> <li>Serial data logic switching Function to invert the logic value of the transmit/receive data.</li> <li>Clock phase setting Selectable from four combinations of transmit/receive clock polarities and phases.</li> </ul>

Note:

1. If an overrun error occurs, the received data of the U2RB register will be undefined. The IR bit in the S2RIC register does not change.



**Figure 21.27 Serial Bus Communication Control Example in Special Mode 2**

**Table 21.19 I/O Pin Functions in Special Mode 2**

Pin Name	I/O	Function	Method of Selection
CLK2	Output	Clock output	The CKDIR bit in the U2MR register = 0
TXD2	Output	Serial data output	(Dummy data is output when performing reception only.)
RXD2	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits sharing pins to 0. (can be used as an input port only when transmitting)

Pins CTS2/RTS2 are not used. (They can be used as I/O ports.)



**Table 21.20 Registers Used and Settings in Special Mode 2 (1)**

Register	Bits	Function
UCLKSEL0	OCOSEL0	Select clock prior to division for UART0 to UART2.
PCLKR	PCLK1	Select the count source for the U2BRG register.
U2TB	0 to 7	Set transmission data.
	8	- (does not need to be set) If necessary, set to 0.
U2RB	0 to 7	Reception data can be read.
	OER	Overrun error flag
	8, 11, 13 to 15	When read, the read value is undefined.
U2BRG	0 to 7	Set bit rate.
U2MR	SMD2 to SMD0	Set to 001b.
	CKDIR	Set to 0.
	4 to 6	Set to 0.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Disabled because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXD2 pin output format.
	CKPOL	Clock phases can be set in combination with the CKPH bit in the U2SMR3 register.
	UFORM	Select the LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select UART2 transmit interrupt source.
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	0 to 7	Set to 0.
U2SMR2	0 to 7	Set to 0.
U2SMR3	CKPH	Clock phases can be set in combination with the CKPOL bit in the U2C0 register.
	NODC	Set to 0.
	0, 2, 4 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

## Notes:

1. This table does not describe a procedure.

### 21.3.4.1 Clock Phase Setting Function

One of four combinations of transmit/receive clock phases and polarities can be selected using the CKPH bit in the U2SMR3 register and the CKPOL bit in the U2C0 register.

Make sure the transmit/receive clock polarity and phase are the same for the master and slaves to be used for communication.

Figure 21.28 shows the Transmit and Receive Timing in Master Mode (Internal Clock).

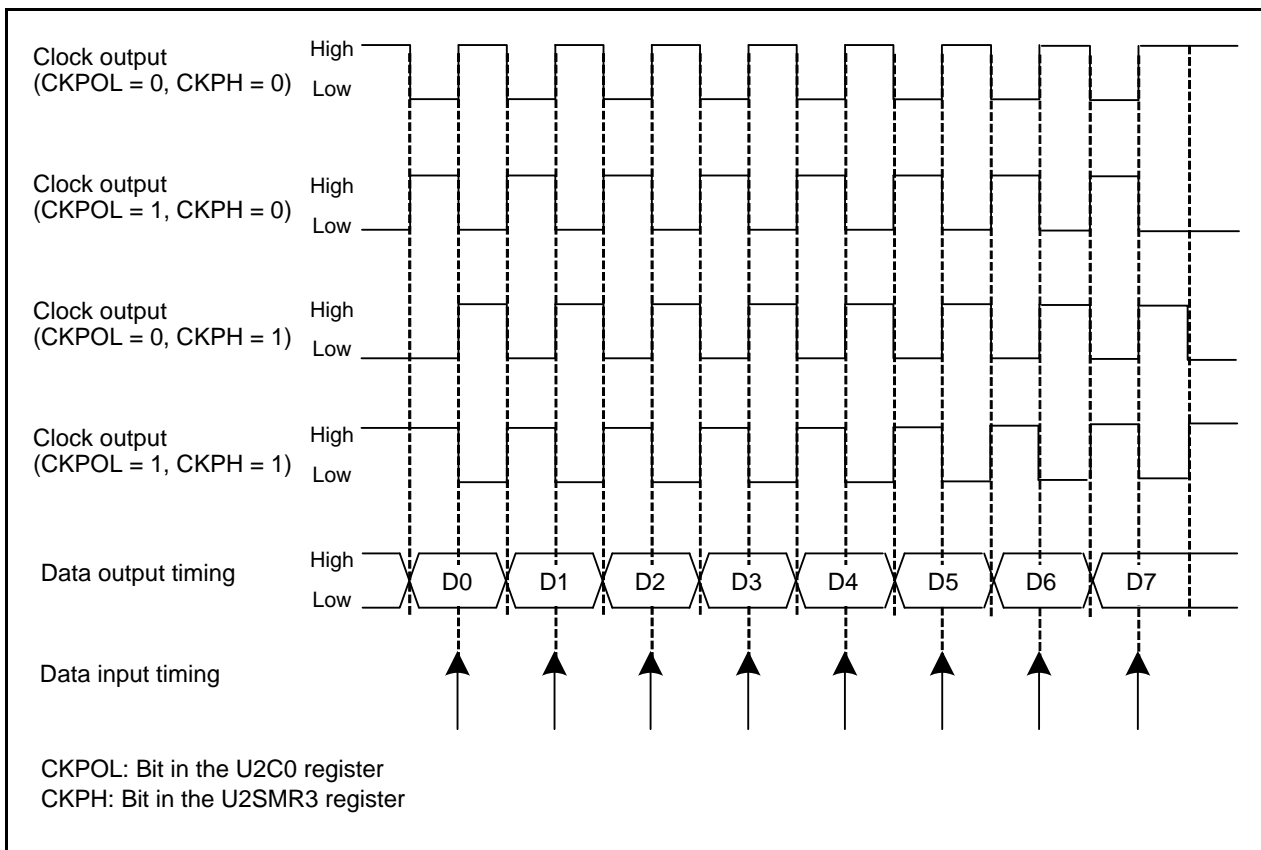


Figure 21.28 Transmit and Receive Timing in Master Mode (Internal Clock)

### 21.3.5 Special Mode 3 (IE Mode) (UART2)

In this mode, 1 bit of IEBus is approximated by 1 byte of UART mode waveform.

Table 21.21 lists the Registers Used and Settings in IE Mode. Figure 21.29 shows the Bus Collision Detect Function-Related Bits.

If the TXD2 pin output level and RXD2 pin input level do not match, a UART2 bus collision detect interrupt request is generated.

**Table 21.21 Registers Used and Settings in IE Mode (1)**

Register	Bits	Function
U2TB	0 to 8	Set transmission data.
U2RB (2)	0 to 8	Reception data can be read.
	OER, FER, PER, SUM	Error flag
U2BRG	0 to 7	Set bit rate.
U2MR	SMD2 to SMD0	Set to 110b.
	CKDIR	Select internal clock or external clock.
	STPS	Set to 0.
	PRY	Disabled because PRYE is 0
	PRYE	Set to 0.
U2C0	IOPOL	Select the TXD and RXD input/output polarity.
	CLK1, CLK0	Select the count source for the U2BRG register.
	CRS	Disabled because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXD2 pin output format.
U2C1	CKPOL	Set to 0.
	UFORM	Set to 0.
	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
U2SMR	U2IRS (2)	Select the source of UART transmit interrupt.
	U2RRM (2), U2LCH, U2ERE	Set to 0.
	0 to 3, 7	Set to 0.
	ABSCS	Select the sampling timing to detect a bus collision.
U2SMR2	ACSE	Set to 1 to use the auto clear function of the transmit enable bit.
	SSS	Select the transmit start condition.
	U2SMR3	Set to 0.
U2SMR4	Set to 0.	

Notes:

1. This table does not describe a procedure.
2. Set the bits not listed above to 0 when writing to registers in IE mode.

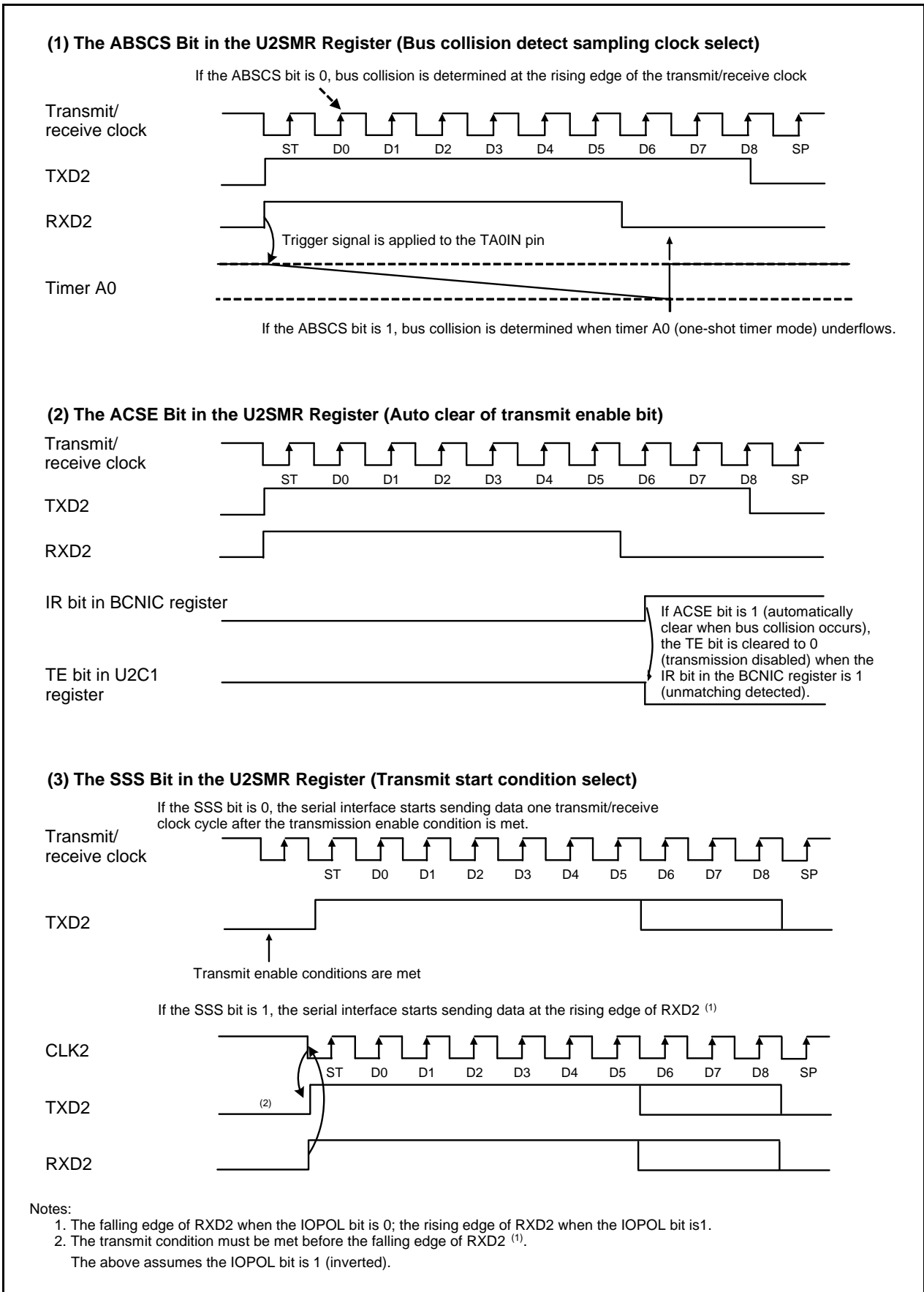


Figure 21.29 Bus Collision Detect Function-Related Bits

### 21.3.6 Special Mode 4 (SIM Mode) (UART2)

In this mode, the serial interface module allows SIM interface devices to communicate in UART mode. Both direct and inverted formats are available. The TXD2 pin outputs a low-level signal when a parity error is detected.

Table 21.22 lists the specifications of SIM mode. Table 21.23 lists the related registers and their settings.

**Table 21.22 SIM Mode Specifications**

Item	Specification
Data formats	<ul style="list-style-type: none"> <li>• Direct format</li> <li>• Inverted format</li> </ul>
Transmit/receive clock	<ul style="list-style-type: none"> <li>• The CKDIR bit in the U2MR register is 0 (internal clock): <math>f_i/(16(n + 1))</math>  <math>f_i = f_{1SIO}, f_{2SIO}, f_{8SIO}, f_{32SIO}</math>  <math>n =</math> setting value of the U2BRG register 00h to FFh</li> <li>• The CKDIR bit is 1 (external clock): <math>f_{EXT}/(16(n + 1))</math>  <math>f_{EXT} =</math> input from the CLK2 pin  <math>n =</math> setting value of the U2BRG register 00h to FFh</li> </ul>
Transmission start conditions	<p>To start transmission, satisfy the following requirements:</p> <ul style="list-style-type: none"> <li>• The TE bit in the U2C1 register is 1 (transmission enabled)</li> <li>• The TI bit in the U2C1 register is 0 (data present in the U2TB register)</li> </ul>
Reception start conditions	<p>To start reception, satisfy the following requirements:</p> <ul style="list-style-type: none"> <li>• The RE bit in the U2C1 register is 1 (reception enabled)</li> <li>• Start bit detection</li> </ul>
Interrupt request generation timing <sup>(2)</sup>	<ul style="list-style-type: none"> <li>• While transmitting When the serial interface completes transmitting data from the UART2 transmit register (the U2IRS bit is 1)</li> <li>• While receiving When transferring data from the UART2 receive register to the U2RB register (at completion of reception)</li> </ul>
Error detection	<ul style="list-style-type: none"> <li>• Overrun error <sup>(1)</sup> This error occurs if the serial interface starts receiving the next data before reading the U2RB register and receives the bit before the last stop bit of the next data.</li> <li>• Framing error <sup>(3)</sup> This error occurs when the number of stop bits set is not detected.</li> <li>• Parity error <sup>(3)</sup> During reception, if a parity error is detected, a parity error signal is output from the TXD2 pin. During transmission, a parity error is detected by the level of input to the RXD2 pin when a transmission interrupt occurs.</li> <li>• Error sum flag This flag becomes 1 when an overrun, framing, or parity errors occurs.</li> </ul>

Notes:

1. If an overrun error occurs, the received data of the U2RB register will be undefined. The IR bit in the S2RIC register does not change.
2. After reset is deasserted, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.
3. The timing at which the framing error flag and the parity error flag are set is detected when data is transferred from the UART2 receive register to the U2RB register.

**Table 21.23 Registers Used and Settings in SIM Mode (1)**

Register	Bit	Function
U2TB (2)	0 to 7	Set transmit data.
U2RB (2)	0 to 7	Received data can be read.
	OER, FER, PER, SUM	Error flag
U2BRG	0 to 7	Set a bit rate.
U2MR	SMD2 to SMD0	Set to 101b.
	CKDIR	Select the internal clock or external clock.
	STPS	Set to 0.
	PRY	Set to 1 in direct format or 0 in inverted format.
	PRYE	Set to 1.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Disabled because CRD is 1.
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Set to 1.
	CKPOL	Set to 0.
	UFORM	Set to 0 in direct format or 1 in inverted format.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Set to 1.
	U2RRM	Set to 0.
	U2LCH	Set to 0 in direct format or 1 in inverted format.
	U2ERE	Set to 1.
U2SMR (2)	0 to 3	Set to 0.
U2SMR2	0 to 7	Set to 0.
U2SMR3	0 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

## Notes:

1. This table does not describe a procedure.
2. Set bits not listed above to 0 when writing to the registers in SIM mode.

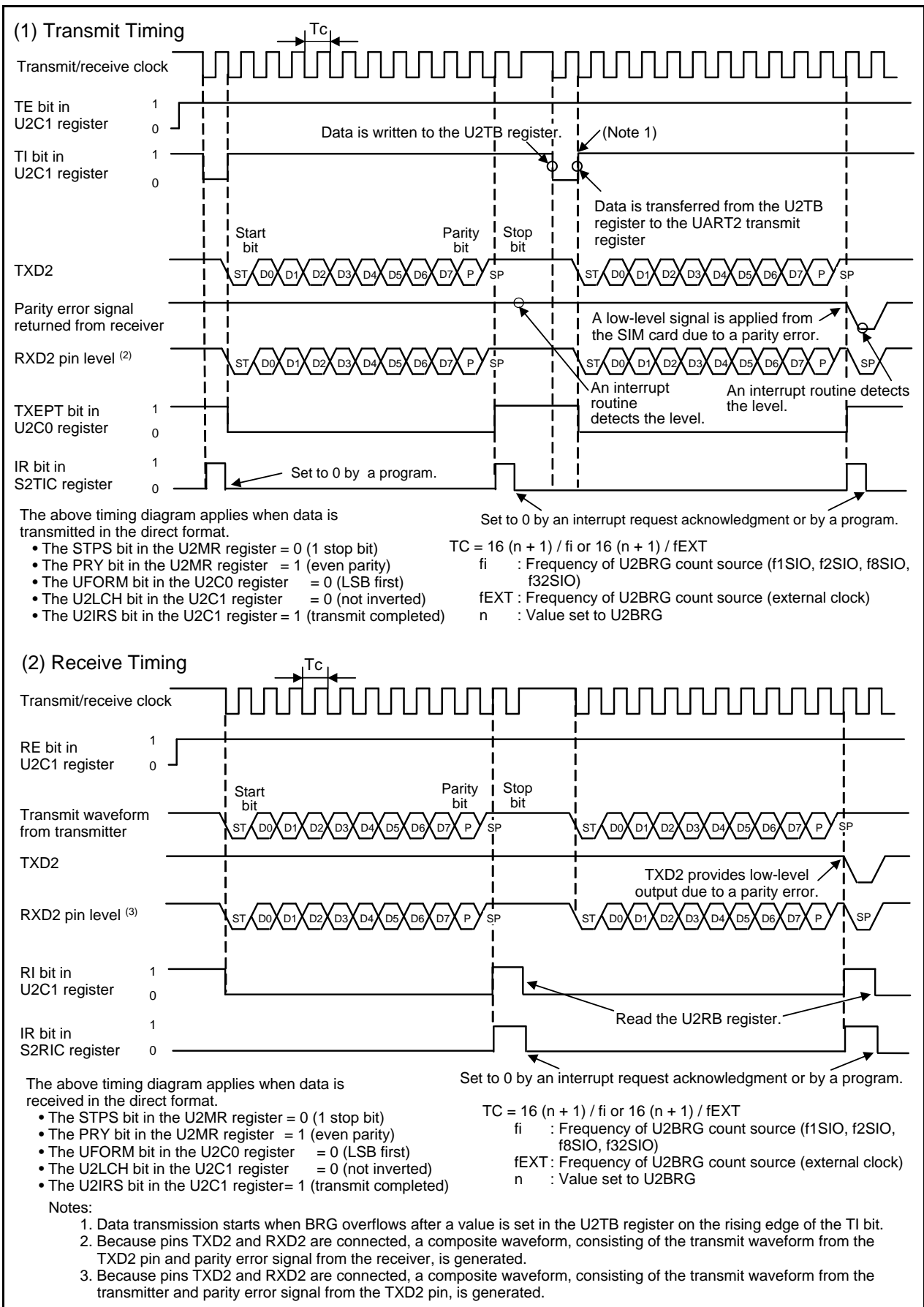


Figure 21.30 Transmit/Receive Timing in SIM Mode

Figure 21.31 shows the Example of SIM Interface Connection. Connect pins TXD2 and RXD2, and then place a pull-up resistance.

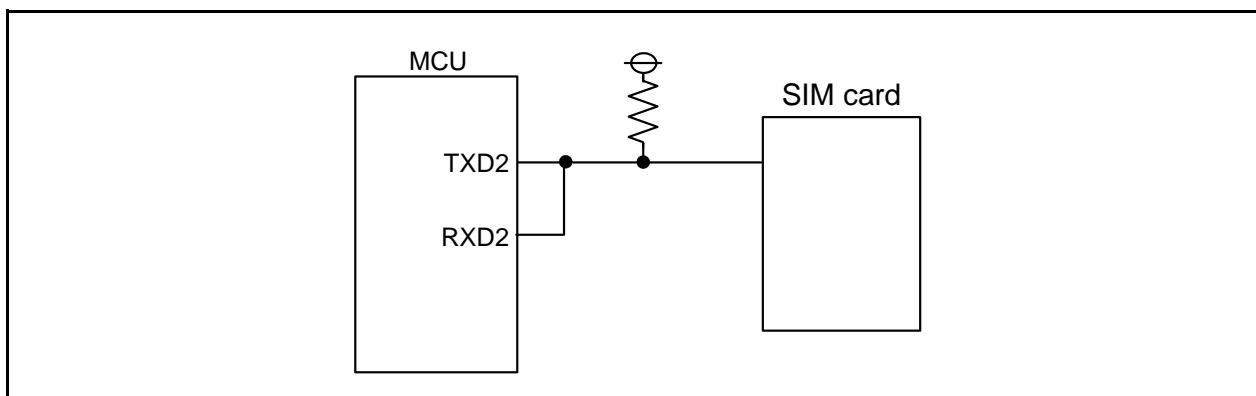


Figure 21.31 Example of SIM Interface Connection

### 21.3.6.1 Parity Error Signal Output

The parity error signal is enabled by setting the U2ERE bit in the U2C1 register to 1 (error signal output).

The parity error signal is output when a parity error is detected while receiving data. A low-level signal is output from the TXD2 pin in the timing shown in Figure 21.32. If the U2RB register is read while outputting a parity error signal, the PER bit is cleared to 0 (no parity error) and at the same time the TXD2 output again goes high.

When transmitting, a transmission complete interrupt request is generated at the falling edge of the transmit/receive clock pulse that immediately follows the stop bit. Therefore, whether a parity error signal has been returned can be determined by reading the port that shares the RXD2 pin in a transmission complete interrupt routine.

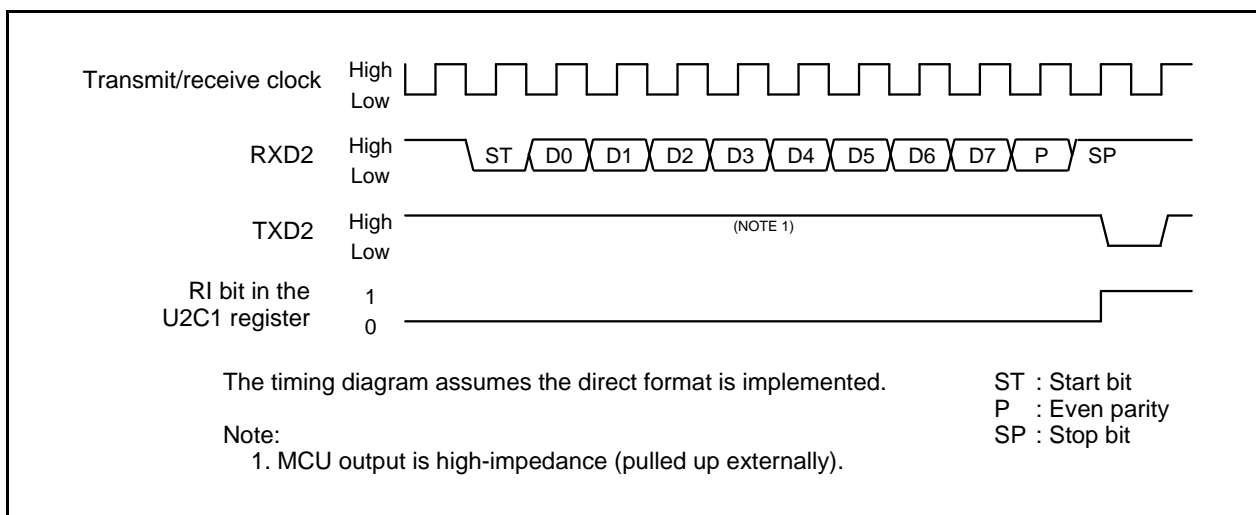


Figure 21.32 Parity Error Signal Output Timing



### 21.3.6.2 Formats

Two formats are available: direct format and inverse format.

For direct format, set the PRYE bit in the U2MR register to 1 (parity enabled), the PRY bit to 1 (even parity), the UFORM bit in the U2C0 register to 0 (LSB first), and the U2LCH bit in the U2C1 register to 0 (not inverted). When data is transmitted, data set in the U2TB register are transmitted with the even-numbered parity, starting from D0. When data is received, the received data is stored in the U2RB register, starting from D0. The even-numbered parity is used to determine whether a parity error occurs. For inverted format, set the PRYE bit to 1, the PRY bit to 0 (odd parity), the UFORM bit to 1 (MSB first), and the U2LCH bit to 1 (inverted). When data is transmitted, values set in the U2TB register are logically inverted and are transmitted with the odd-numbered parity, starting from D7. When data is received, the received data is logically inverted to be stored in the U2RB register, starting from D7. The odd-numbered parity is used to determine whether a parity error occurs.

Figure 21.33 shows the SIM Interface Format.

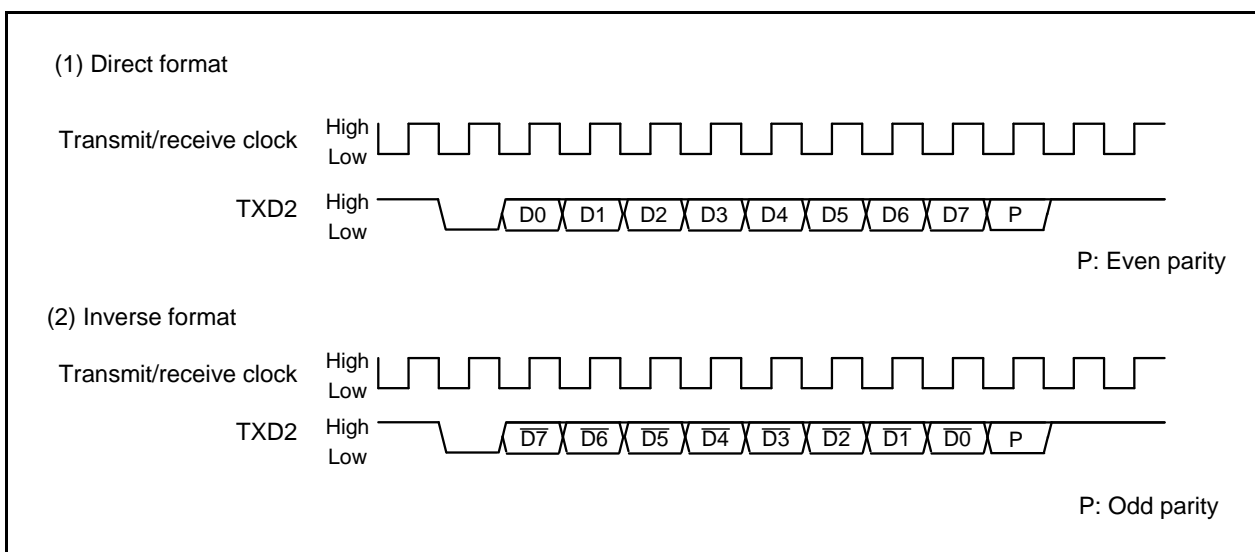


Figure 21.33 SIM Interface Format

## 21.4 Interrupts

UART0 to UART4 include interrupts by transmission, reception, ACK, NACK, start/stop condition detection, and bus collision detection.

### 21.4.1 Interrupt Related Registers

Refer to operation examples in each mode for interrupt sources and interrupt request generation timing. For details of interrupt control, refer to 12.7 "Interrupt Control". Table 21.24 lists UART0 to UART4 Interrupt Related Registers.

**Table 21.24 UART0 to UART4 Interrupt Related Registers**

Address	Register	Symbol	Reset Value
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
006Fh	UART4 Transmit Interrupt Control Register	S4TIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h

Some interrupts of UART0 to UART4 share interrupt vectors and interrupt control registers with other peripheral functions. When using these interrupts, select them by interrupt source select registers. Table 21.25 lists Interrupt Selection in UART0 to UART4.

**Table 21.25 Interrupt Selection in UART0 to UART4**

Interrupt Source	Interrupt Source Select Register Settings		
	Register	Bit	Setting Value
UART2 start/stop condition detection, bus collision detection	IFSR2A	IFSR20	0
UART3 transmission	IFSR2A	IFSR25	0
UART4 transmission	IFSR3A	IFSR36	0
UART0 transmission	IFSR4A	IFSR43	0

In the following modes, an interrupt request can be generated by rewriting bit values.

- Special mode 1 (I<sup>2</sup>C mode)

Set the IR bit in the interrupt control register of UART2 to 0 (interrupt not requested), when the following bits are changed:

Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, the CKPH bit in the U2SMR3 register

- Special mode 4 (SIM mode)

After reset, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

## 21.4.2 Reception Interrupt

- The case that bits SMD2 to SMD0 in the U2MR register are not set to 010b (I<sup>2</sup>C mode)

When the RI bit in the U2C1 register is changed from 0 (no data in the U2RB register) to 1 (data present in the U2RB register), the IR bit in the S2RIC register is automatically set to 1 (interrupt requested).

If an overrun error occurs (when the RI bit is 1, the next data is received), the RI bit remains 1, and therefore, the IR bit in the S2RIC register remains unchanged.

- The case that bits SMD2 to SMD0 in the U2MR register are set to 010b (I<sup>2</sup>C mode)

When the RI bit in the U2C1 register is changed from 0 (no data in the U2RB register) to 1 (data present in the U2RB register), the IR bit in the S2RIC register is automatically set to 1 (interrupt requested).

When an overrun error occurs, the IR bit in the S2RIC register also becomes 1.

## 21.5 Notes on Serial Interface UARTi (i = 0 to 4)

### 21.5.1 Common Notes on Multiple Modes

#### 21.5.1.1 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/ $\overline{CTS2}$ / $\overline{RTS2}$ /TA1IN/ $\overline{V}$ /TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/ $\overline{W}$ , P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/ $\overline{U}$ /TSUDB

#### 21.5.1.2 Register Setting

Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART4 again.

### 21.5.2 Clock Synchronous Serial I/O Mode

#### 21.5.2.1 Transmission/Reception

When the  $\overline{RTS}$  function is used with an external clock, the  $\overline{RTSi}$  pin (i = 0 to 3) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The  $\overline{RTSi}$  pin outputs a high-level signal when a receive operation starts. Therefore, transmit timing and receive timing can be synchronized by connecting the  $\overline{RTSi}$  pin to the  $\overline{CTS}$  pin on the transmitting side. The  $\overline{RTS}$  function is disabled when an internal clock is selected.

#### 21.5.2.2 Transmission

If the transmission is started while an external clock is selected and the TXEPT bit in the UiC0 register (i = 0 to 4) is 1 (no data present in transmit register), meet the last requirement at either of the following timings:

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start transmission (in no particular order):

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When the  $\overline{CTS}$  function is selected, input on the  $\overline{CTS}$  pin is low.

### 21.5.2.3 Reception

In clock synchronous serial I/O mode, a shift clock is generated by activating a transmitter. Set the UARTi-associated registers for a transmit operation even if the MCU is used for a receive operations only. Dummy data is output from the TXDi pin (i = 0 to 4) while receiving.

When an internal clock is selected, a shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), set dummy data in the UiTB register, and input an external clock to the CLKi pin to generate a shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is 1 (data present in the UiRB register) and the next receive data is received in the UARTi receive register. Then, the OER bit in the UiRB register becomes 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs again, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register for each receive operation.

If the reception is started while an external clock is selected and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement at either of the timings below.

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start reception (in no particular order):

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

## 21.5.3 Special Mode 1 (I<sup>2</sup>C Mode)

### 21.5.3.1 Generating Start and Stop Conditions

(Technical update number: TN-16C-130A/EA)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than a half cycle of the transmit/receive clock. Then set each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

### 21.5.3.2 IR Bit

Set the following bits first, and then set the IR bit in each UART2 interrupt control register to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, the CKPH bit in the U2SMR3 register

### 21.5.3.3 Setup and Hold Times When Generating a Start/Stop Condition

When generating a start condition, the hold time ( $t_{HD:STA}$ ) is a half cycle of the SCL clock. When generating a stop condition, the setup time ( $t_{SU:STO}$ ) is a half cycle of the SCL clock.

When the SDA digital delay function is enabled, take delay time into consideration (see 21.3.3.7 "SDA Digital Delay").

The following shows a calculation example of hold and setup times when generating a start/stop condition.

Calculation example when setting 100 kbps

- U2BRG count source:  $f_1 = 20$  MHz
- U2BRG register setting value:  $n = 100 - 1$
- SDA digital delay setting value: DL2 to DL0 are 101b (5 or 6 cycles of U2BRG count source)

$$f_{SCL} \text{ (theoretical value)} = f_1 / (2(n+1)) = 20 \text{ MHz} / (2 \times (99 + 1)) = 100 \text{ kbps}$$

$$t_{DL} = \text{delay cycle count} / f_1 = 6 / 20 \text{ MHz} = 0.3 \mu\text{s}$$

$$t_{HD:STA} \text{ (theoretical value)} = 1 / (2f_{SCL} \text{ (theoretical value)}) = 1 / (2 \times 100 \text{ kbps}) = 5 \mu\text{s}$$

$$t_{SU:STO} \text{ (theoretical value)} = 1 / (2f_{SCL} \text{ (theoretical value)}) = 1 / (2 \times 100 \text{ kbps}) = 5 \mu\text{s}$$

$$t_{HD:STA} \text{ (actual value)} = t_{HD:STA} \text{ (theoretical value)} - t_{DL} = 5 \mu\text{s} - 0.3 \mu\text{s} = 4.7 \mu\text{s}$$

$$t_{SU:STO} \text{ (actual value)} = t_{SU:STO} \text{ (theoretical value)} + t_{DL} = 5 \mu\text{s} + 0.3 \mu\text{s} = 5.3 \mu\text{s}$$

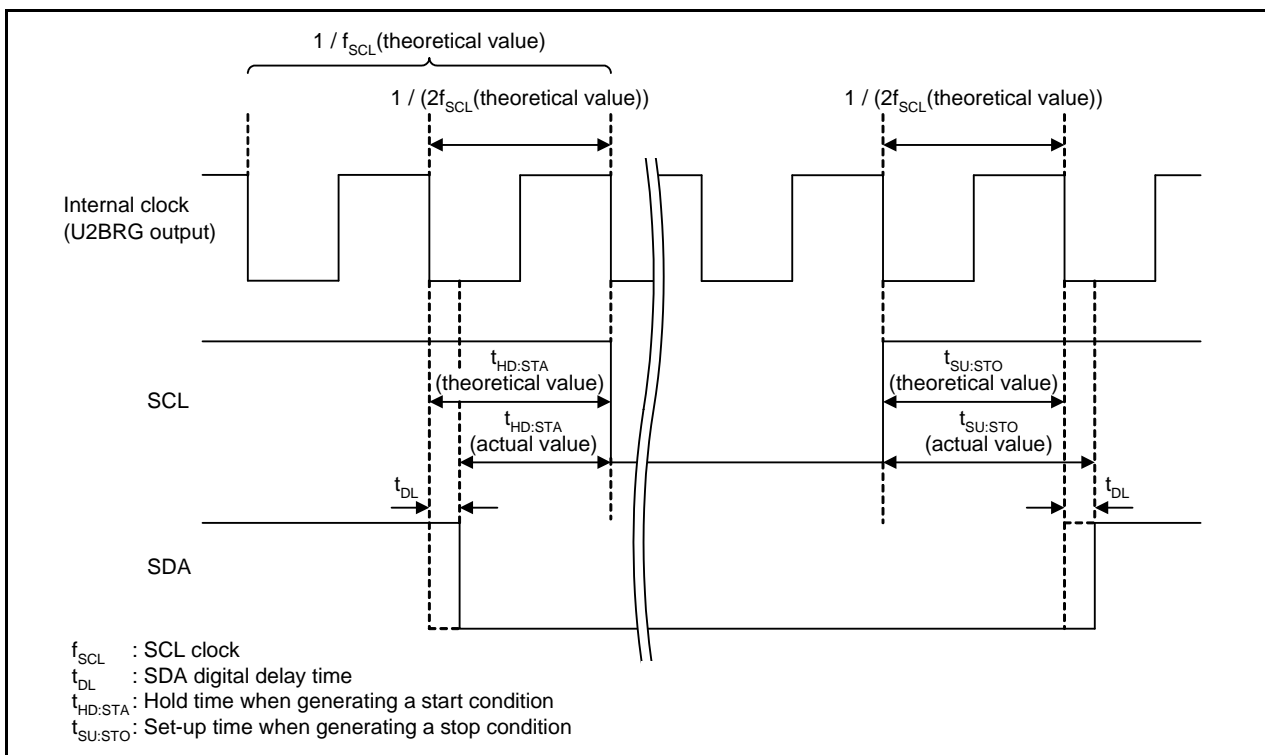


Figure 21.34 Setup and Hold Times When Generating Start and Stop Conditions

### 21.5.3.4 Restrictions on the Bit Rate When Using the U2BRG Count Source

In I<sup>2</sup>C mode, set the U2BRG register to a value of 03h or greater.

A maximum of three U2BRG count source cycles are necessary until the internal circuit acknowledges the SCL clock level. The connectable I<sup>2</sup>C-bus bit rate is one-third or less than the U2BRG count source speed. If a value between 00h to 02h is set to the U2BRG register, bit slippage may occur.

### 21.5.3.5 Restart Condition in Slave Mode

When a restart condition is detected in slave mode, the successive processes may not be executed correctly. In slave mode, do not use a restart condition.

### 21.5.3.6 Requirements to Start Transmission/Reception in Slave Mode

When transmission/reception is started in slave mode and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.

Requirements to start transmission (in no particular order):

- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

Requirements to start reception (in no particular order):

- The RE bit in the U2C1 register is 1 (reception enabled).
- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

### 21.5.4 Special Mode 4 (SIM Mode)

(Technical update number: TN-M16C-101-0309)

After reset is deasserted, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

## 22. Multi-master I<sup>2</sup>C-bus Interface

### 22.1 Introduction

The multi-master I<sup>2</sup>C-bus interface (I<sup>2</sup>C interface) is a serial communication circuit based on the I<sup>2</sup>C-bus data transmit/receive format, and is equipped with arbitration lost detect and clock synchronous functions. Table 22.1 lists the Multi-master I<sup>2</sup>C-bus Interface Specifications, Table 22.2 lists the I<sup>2</sup>C Interface Detection Function, Figure 22.1 shows the Multi-master I<sup>2</sup>C-bus Interface Block Diagram, and Table 22.3 lists the I/O Ports.

**Table 22.1 Multi-master I<sup>2</sup>C-bus Interface Specifications**

Item	Function
Formats	Based on I <sup>2</sup> C-bus standard: 7-bit addressing format Fast-mode Standard clock mode
Communication modes	Based on I <sup>2</sup> C-bus standard: Master transmission Master reception Slave transmission Slave reception
Bit rate	16.1 kbps to 400 kbps (fVIIC = 4 MHz)
I/O pins	Serial data line SDAMM (SDA) Serial clock line SCLMM (SCL)
Interrupt request generating sources	<ul style="list-style-type: none"> <li>• I<sup>2</sup>C-bus interrupt</li> <li>Completion of transmission</li> <li>Completion of reception</li> <li>Slave address match detection</li> <li>General call detection</li> <li>Stop condition detection</li> <li>Timeout detection</li> <li>• SDA/SCL interrupt</li> <li>Rising or falling edge of the signal of the SDAMM or SCLMM pin</li> </ul>
Selectable functions	<ul style="list-style-type: none"> <li>• I<sup>2</sup>C-bus interface pin input level select</li> <li>Selectable input level with I<sup>2</sup>C-bus input level or SMBus input level</li> <li>• Timeout detection</li> <li>A function that detects when the SCLMM pin is driven high over a certain period of time when the bus is busy.</li> <li>• Free data format select</li> <li>A function that generates an interrupt request when receiving the first byte of data, regardless of the slave address value.</li> </ul>

fVIIC: I<sup>2</sup>C-bus system clock



**Table 22.2 I<sup>2</sup>C Interface Detection Function**

Item	Function
Slave address match detection	A function to detect a slave address match when in slave transmission/reception. If slave address match is detected, an ACK is returned. If the slave address match is not detected, a NACK is returned, and no further data is transmitted/received. Up to three slave addresses can be set.
General call detection	A function to detect a general call in slave reception.
Arbitration lost detection	A function to detect arbitration lost and stop the output from pins SDAMM and SCLMM.
Bus busy detection	A function to detect a bus busy state and set/reset the BB bit.

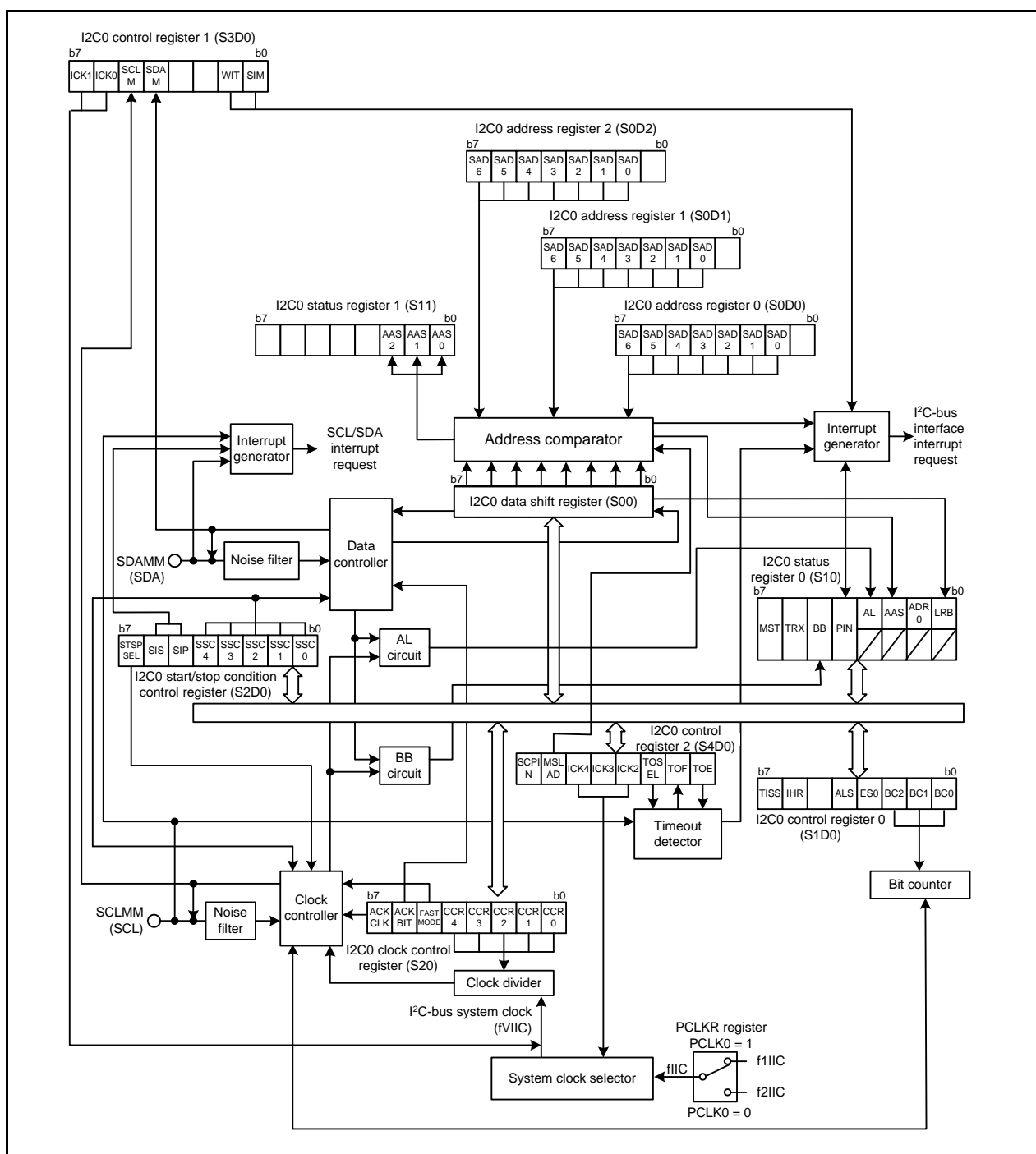


Figure 22.1 Multi-master I<sup>2</sup>C-bus Interface Block Diagram

Table 22.3 I/O Ports

Pin Name	I/O	Function
SDAMM	I/O	I/O pin for SDA (N-channel open drain output) (1)
SCLMM	I/O	I/O pin for SCL (N-channel open drain output) (1)

Note:

1. This function disables the P-channel transistor of CMOS output buffer for at all time. However, it does not make the SDAMM and SCLMM open drain output completely. Refer to electrical characteristics on input voltage range.

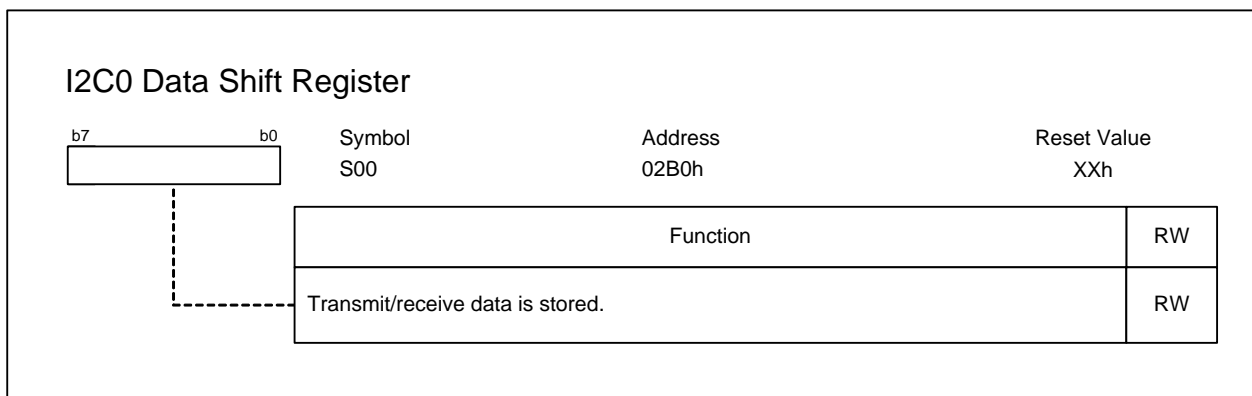
## 22.2 Registers Descriptions

Table 22.4 lists registers associated with multi-master I<sup>2</sup>C-bus interface. When the CM07 bit in the CM0 register is set to 1 (sub clock is CPU clock), registers listed in Table 22.4 should not be accessed. Set them after the CM07 bit is set to 0 (main clock, PLL clock, or on-chip oscillator clock).

**Table 22.4 Registers**

Address	Register	Symbol	Reset Value
02B0h	I2C0 Data Shift Register	S00	XXh
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb

### 22.2.1 I<sup>2</sup>C0 Data Shift Register (S00)



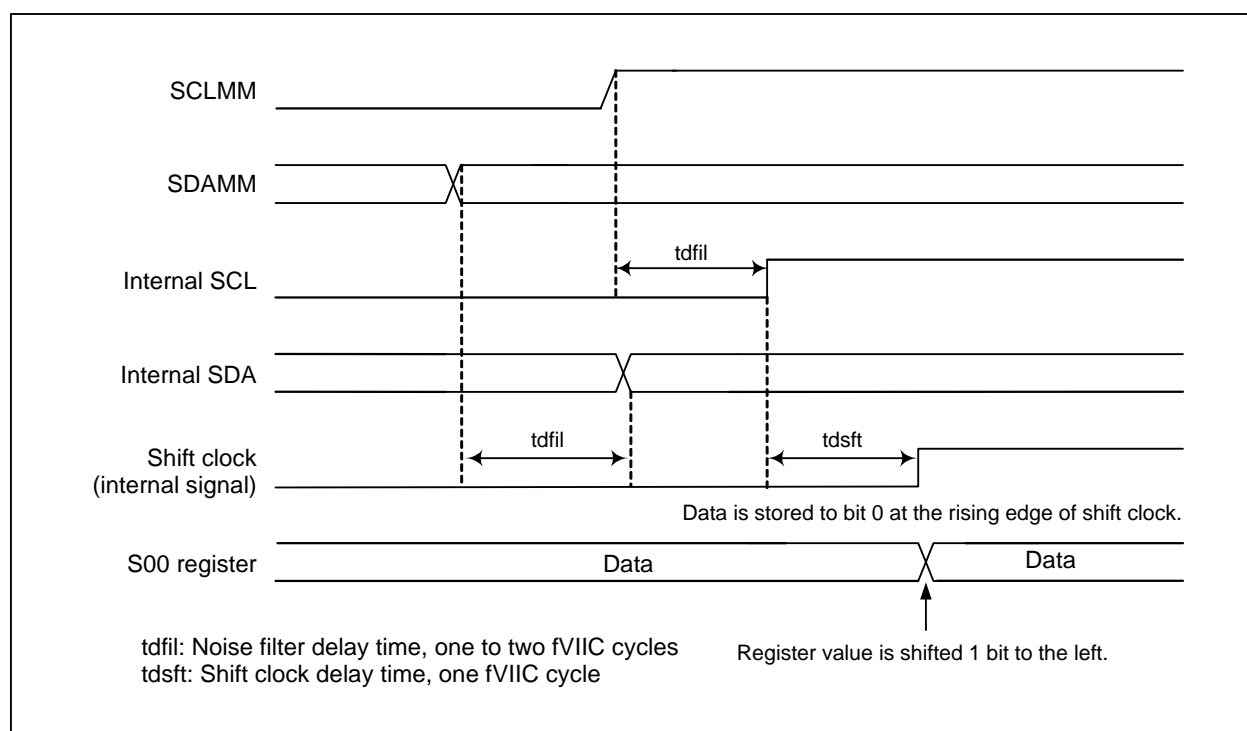
When the I<sup>2</sup>C interface is a transmitter, write transmit data to the S00 register. When the I<sup>2</sup>C interface is a receiver, received data can be read from the S00 register. In master mode, this register is also used to generate a start condition or stop condition on a bus. (Refer to 22.3.2 “Generating a Start Condition” and 22.3.3 “Generating a Stop Condition”.)

Write to the S00 register when the ES0 bit in the S1D0 register is 1 (I<sup>2</sup>C interface enabled).

Do not write to the S00 register when transmitting/receiving data.

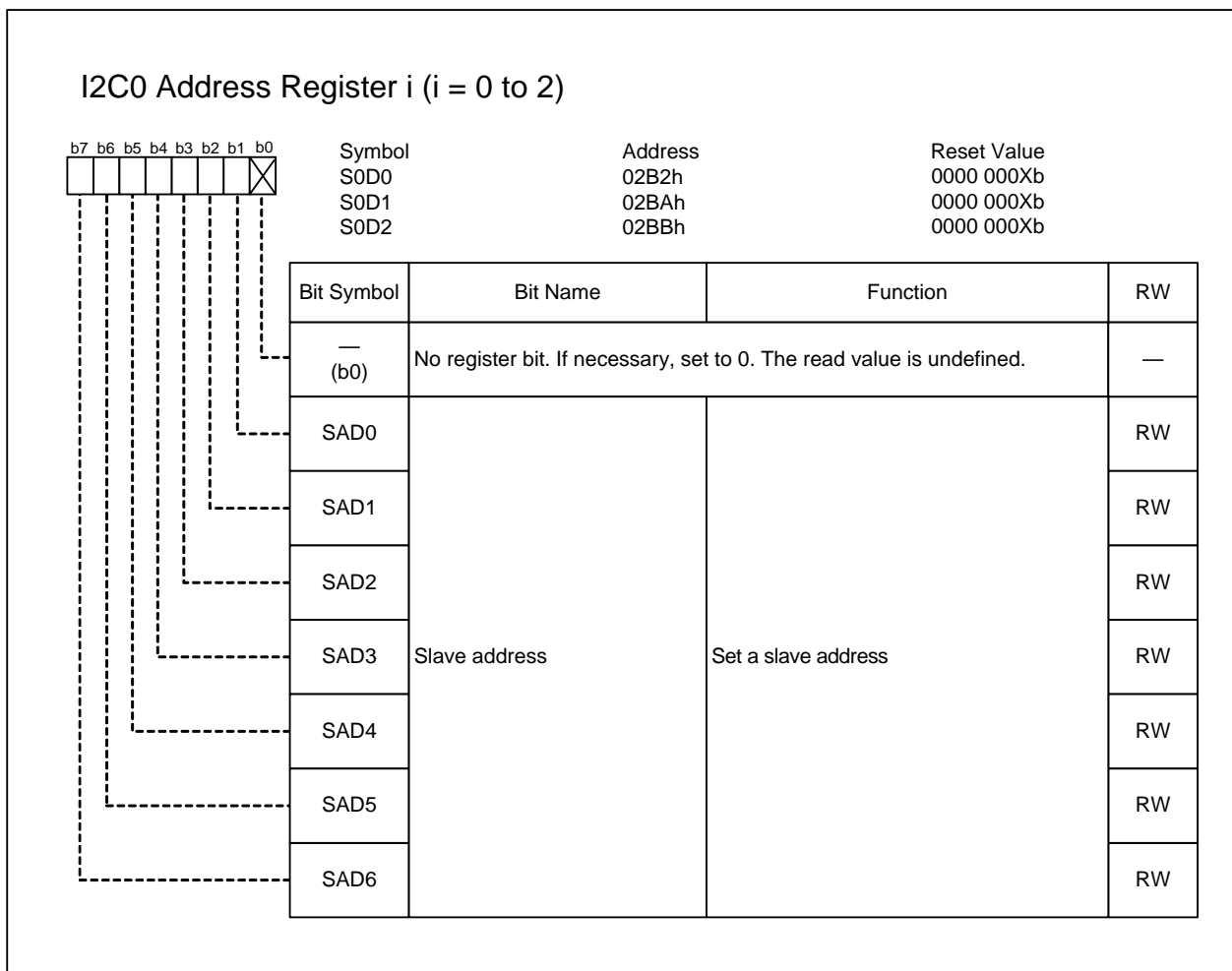
When the I<sup>2</sup>C interface is a transmitter, the data in the S00 register is transmitted to other devices. The MSB (bit 7) is transmitted first, synchronizing with the SCLMM clock. Every time 1-bit data is output, the S00 register value is shifted 1 bit to the left.

When the I<sup>2</sup>C interface is a receiver, data is transferred to the S00 register from other devices. The LSB (bit 0) is input first, synchronizing with the SCLMM clock. Every time 1-bit data is output, the S00 register value is shifted 1 bit to the left. Figure 22.2 shows Timing to Store Received Data to the S00 Register.



**Figure 22.2 Timing to Store Received Data to the S00 Register**

### 22.2.2 I<sup>2</sup>C0 Address Register i (S0Di) (i = 0 to 2)



#### SAD6 to SAD0 (Slave address) (b7-b1)

Bits SAD6 to SAD0 indicate a slave address to be compared for a slave address match detection in slave mode. Up to three slave addresses can be set. Set the S0Di register to 00h when not setting the slave address.

However, when the MSLAD bit in the S4D0 register is 0, registers S0D1 and S0D2 are disabled. Only the slave address set to the S0D0 register is compared with address the data received.

### 22.2.3 I<sup>2</sup>C0 Control Register 0 (S1D0)

I <sup>2</sup> C0 Control Register 0											
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Reset Value	
		0						S1D0	02B3h	00h	
								Bit Symbol	Bit Name	Function	RW
								BC0	Bit counter (number of transmitted/received bits)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	RW
								BC1		RW	
								BC2		RW	
								ES0		I <sup>2</sup> C-bus interface enable bit	0: Disabled 1: Enabled
								ALS	Data format select bit	0: Addressing format 1: Free data format	RW
								— (b5)	Reserved bit	Set to 0.	RW
								IHR	I <sup>2</sup> C-bus interface reset bit	0: Reset is deasserted (automatically) 1: Reset	RW
								TISS	I <sup>2</sup> C-bus interface pin input level select bit	0: I <sup>2</sup> C-bus input 1: SMBus input	RW

#### BC2 to BC0 (Bit counter) (b2-b0)

Bits BC2 to BC0 become 000b (8 bits) when a start condition is detected.

When the ACKCLK bit in the S20 register is 0 (no ACK clock), and data for the number of bits selected by bits BC2 to BC0 is transmitted or received, bits BC2 to BC0 become 000b again.

When the ACKCLK bit in the S20 register is 1 (ACK clock), and data for the number of bits selected and an ACK is transmitted or received, bits BC2 to BC0 become 000b again.

#### ES0 (I<sup>2</sup>C-bus interface enable bit) (b3)

The ES0 bit enables the I<sup>2</sup>C interface.

When the ES0 bit is set to 0, the I<sup>2</sup>C interface becomes as follows:

- Pins SDAMM and SCLMM: I/O ports or other peripheral pins
- The S00 register is write disabled.
- The I<sup>2</sup>C-bus system clock (hereinafter called fVIIC) stops.
- S10 register
  - ADRO bit: 0 (general call not detected)
  - AAS bit: 0 (slave address not matched)
  - AL bit: 0 (arbitration lost not detected)
  - PIN bit: 1 (no I<sup>2</sup>C-bus interrupt request)
  - BB bit: 0 (bus free)
  - TRX bit: 0 (receive mode)
  - MST bit: 0 (slave mode)

- Bits AAS2 to AAS0 in the S11 register: 0 (slave address not matches)
- The TOF bit in the S4D0 register: 0 (timeout not detected)

### ALS (Data format select bit) (b4)

The ALS bit is enabled in slave mode. When the ALS bit is 0 (addressing format), the slave address match detection is performed.

When a slave address stored to bits SAD6 to SAD0 in the S0Di register ( $i = 0$  to 2) is compared and matched with the calling address by a master, or when a general call address is received, the IR bit in the IICIC register becomes 1 (interrupt requested).

When the ALS bit is 1 (free data format), the slave address match detection is not performed. Therefore, the IR bit in the IICIC register becomes 1 (interrupt requested), regardless of the calling address by a master.

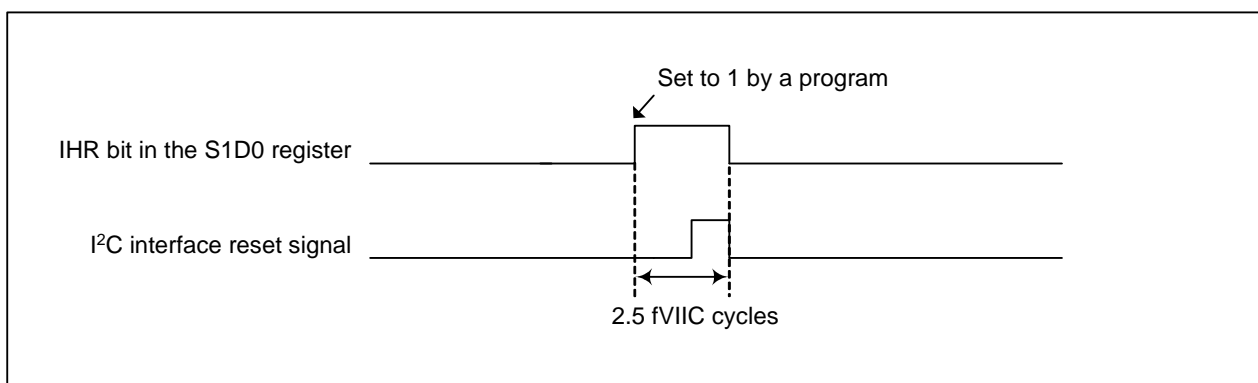
### IHR (I<sup>2</sup>C-bus interface reset bit) (b6)

The IHR bit resets the I<sup>2</sup>C interface if there is an anomaly during transmission/reception. When the ES0 bit in the S1D0 register is 1 (I<sup>2</sup>C interface enabled) and then the IHR bit is set to 1 (reset), the I<sup>2</sup>C interface becomes as follows:

- S10 register
  - ADR0 bit: 0 (general call not detected)
  - AAS bit: 0 (slave address not matched)
  - AL bit: 0 (arbitration lost not detected)
  - PIN bit: 1 (No I<sup>2</sup>C-bus interrupt request)
  - BB bit: 0 (bus free)
  - TRX bit: 0 (receive mode)
  - MST bit: 0 (slave mode)
- Bits AAS2 to AAS0 in the S11 register: 0 (slave address not matches)
- TOF bit in the S4D0 register: 0 (timeout not detected)

When the IHR bit is set to 1, the I<sup>2</sup>C interface is reset and the IHR bit becomes 0 automatically. It takes a maximum of 2.5 fVIIC cycles to complete the reset sequence.

Figure 22.3 shows the I<sup>2</sup>C Interface Reset Timing.

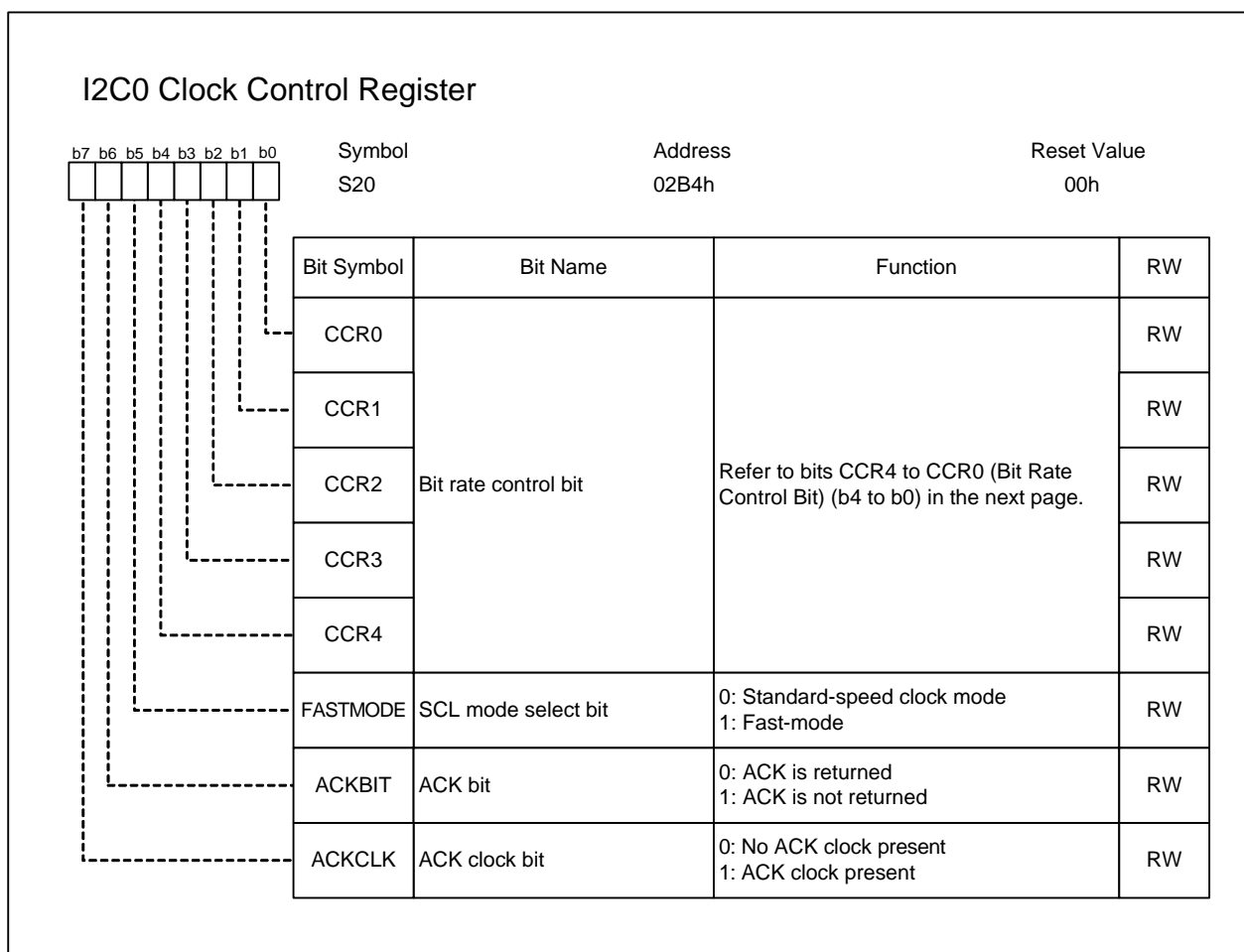


**Figure 22.3 I<sup>2</sup>C Interface Reset Timing**

### TISS (I<sup>2</sup>C-bus interface pin input level select bit) (b7)

Set the TISS bit to select the input level of the SCLMM pin and SDAMM pin for the I<sup>2</sup>C interface.

## 22.2.4 I<sup>2</sup>C0 Clock Control Register (S20)



### CCR4 to CCR0 (Bit rate control bit) (b4-b0)

Assuming the CCR value (3 to 31) is the value set to bits CCR4 to CCR0, the bit rate can be calculated using the following equation:

Refer to 22.3.1.2 “Bit Rate and Duty Cycle” for more details.

In standard-speed clock mode,

$$\text{Bit rate} = \frac{f_{\text{VIIC}}}{8 \times \text{CCR value}} \leq 100 \text{ kbps}$$

When the CCR value is other than 5 in fast-mode,

$$\text{Bit rate} = \frac{f_{\text{VIIC}}}{4 \times \text{CCR value}} \leq 400 \text{ kbps}$$

When the CCR value is 5 in fast-mode, the bit rate is assumed to reach 400 kbps, the maximum bit rate in fast-mode.

$$\text{Bit rate} = \frac{f_{\text{VIIC}}}{2 \times \text{CCR value}} = \frac{f_{\text{VIIC}}}{10} \leq 400 \text{ kbps}$$

Do not set the CCR value from 0 to 2 regardless of the f<sub>VIIC</sub> frequency.

Rewrite bits CCR4 to CCR0 when the ES0 bit in the S1D0 register is 0 (disabled).



**FASTMODE (SCL mode select bit) (b5)**

When using the fast-mode I<sup>2</sup>C-bus standard (maximum 400 kbps), set the FASTMODE bit to 1 (fast-mode) and set fVIIC to 4 MHz or more.

Rewrite the FASTMODE bit when the ES0 bit in the S1D0 register is 0 (disabled).

**ACKBIT (ACK bit) (b6)**

The ACK bit is enabled in master reception, slave reception, or slave address reception. When receiving a slave address, the SDAMM pin level during the ACK clock pulse is determined by a combination of bits ALS and ACKBIT in the S1D0 register and the received slave address.

When receiving data, the SDAMM pin level during the ACK clock pulse is determined by the ACKBIT bit. Table 22.5 lists the SDAMM Pin Level during the ACK Clock Pulse.

**Table 22.5 SDAMM Pin Level during the ACK Clock Pulse**

Received Content	ALS Bit in the S1D0 Register	ACKBIT Bit in the S20 Register	Slave Address Content	SDAMM Pin Level at ACK Clock
Slave Address	0	0	When the MSLAD bit in the S4D0 register is 0: Matched with bits SAD6 to SAD0 in the S0D0 register.	Low (ACK)
			When the MSLAD bit is 1: Matched with bits SAD6 to SAD0 in any of registers S0D0 to S0D2.	
			0000000b	
			Others	High (NACK)
		1	—	High (NACK)
	1	0	—	Low (ACK)
		1	—	High (NACK)
Data	—	0	—	Low (ACK)
		1	—	High (NACK)

**ACKCLK (ACK clock bit) (b7)**

When the ACKCLK bit is 1 (ACK clock present), an ACK clock is generated immediately after 1-byte data is transmitted or received (8 clocks).

When the ACKCLK bit is 0 (no ACK clock), no ACK clock is generated after 1-byte data is transmitted or received (8 clocks). At the falling edge of data transmission/reception (the falling edge of the eighth clock), the IR bit in the IICIC register becomes 1 (interrupt requested).

Do not write to this bit when transmitting/receiving data.

### 22.2.5 I<sup>2</sup>C0 Start/Stop Condition Control Register (S2D0)

I <sup>2</sup> C0 Start/Stop Condition Control Register			
	Symbol S2D0	Address 02B5h	Reset Value 0001 1010b
Bit Symbol	Bit Name	Function	RW
SSC0	Start/stop condition setting bit	Refer to SSC4 to SSC0 (Start/Stop Condition Setting Bit) (b4 to b0) in the same page	RW
SSC1			RW
SSC2			RW
SSC3			RW
SSC4			RW
SIP	SCL/SDA interrupt pin polarity select bit	0: Falling edge 1: Rising edge	RW
SIS	SCL/SDA interrupt pin select bit	0: SDAMM 1: SCLMM	RW
STSPSEL	Start/stop condition generation select bit	0: Short setup/hold time mode 1: Long setup/hold time mode	RW

#### SSC4 to SSC0 (Start/stop condition setting bit) (b4-b0)

Set bits SSC4 to SSC0 to select the start/stop condition detect parameter (SCL open time, setup time, hold time) in standard-speed clock mode. Refer to 22.3.7 “Detecting Start/Stop Conditions”.

Do not set an odd value or 00000b to these bits.

#### SIP (SCL/SDA interrupt pin polarity select bit) (b5)

#### SIS (SCL/SDA interrupt pin select bit) (b6)

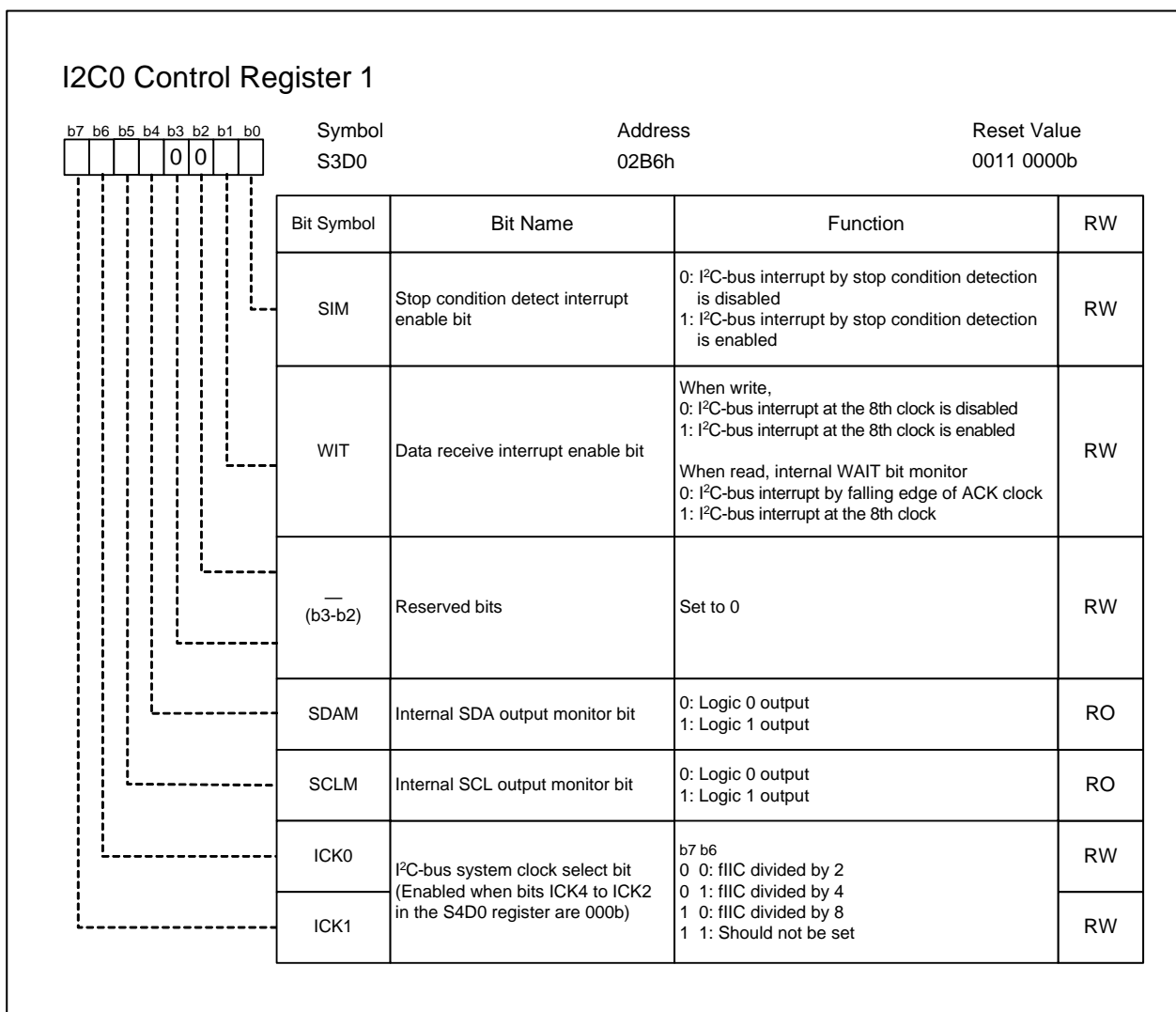
The IR bit in the SCLDAIC register becomes 1 (interrupt requested) when the I<sup>2</sup>C interface detects the edge selected by the SIP bit for the pin signal selected by the SIS bit. Refer to 22.4 “Interrupts”.

#### STSPSEL (Start/stop condition generation select bit) (b7)

See Table 22.12 “Setup/Hold Time for Generating a Start/Stop Condition”.

If the fVIIC frequency is more than 4 MHz, set the STSPSEL bit to 1 (long mode).

### 22.2.6 I<sup>2</sup>C0 Control Register 1 (S3D0)



Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use the MOV instruction to write to the S3D0 register.

#### SIM (Stop condition detect interrupt enable bit) (b0)

When the SIM bit is 1 (I<sup>2</sup>C-bus interrupt by stop condition detection enabled) and a stop condition is detected, the SCPIN bit in the S4D0 register becomes 1 (stop condition detect interrupt requested) and the IR bit in the IICIC register becomes 1 (interrupt requested).

**WIT (Data receive interrupt enable bit) (b1)**

The WIT bit is enabled in master reception or slave reception.

The WIT bit has two functions:

- Selects the I<sup>2</sup>C-bus interrupt timing when data is received. (write)
- Monitors the state of the internal WAIT flag. (read)

The WIT bit can select whether to generate an I<sup>2</sup>C-bus interrupt request at eighth clock (before ACK clock) during the data reception.

When the ACKCLK bit in the S20 register is 1 (ACK clock presents) and the WIT bit is set to 1 (enable I<sup>2</sup>C-bus interrupt at 8th clock), an I<sup>2</sup>C-bus interrupt request is generated at the eighth clock (before the ACK clock). Then, the PIN bit in the S10 register becomes 0 (interrupt requested).

When the ACKCLK bit in the S20 register is 0 (no ACK clock presents), write 0 to the WIT bit to disable the I<sup>2</sup>C-bus interrupt by data reception.

When transmitting data and receiving a slave address, no interrupt requests are generated at the eighth clock (before the ACK clock) regardless of the value written to the WIT bit.

Reading the WIT bit returns the internal WAIT flag status.

An I<sup>2</sup>C-bus interrupt request is generated at the falling edge of the ninth clock (ACK clock) regardless of the value written to the WIT bit. Then, the PIN bit in the S10 register becomes 0 (interrupt requested).

Therefore, read the internal WAIT flag status to determine whether the I<sup>2</sup>C-bus interrupt request is generated at the eighth clock (before the ACK clock) or at the falling edge of the ACK clock.

When the WIT bit is set to 1 (I<sup>2</sup>C-bus interrupt enabled by receiving data), the internal WAIT flag changes under the following conditions:

Condition to become 0:

- The S20 register (ACKBIT bit) is written.

Condition to become 1:

- The S00 register is written during data reception.

When transmitting data and receiving a slave address, the internal WAIT flag is 0 and the I<sup>2</sup>C-bus interrupt request will be generated only at the falling edge of the ninth clock (ACK clock), regardless of the value written to the WIT bit.

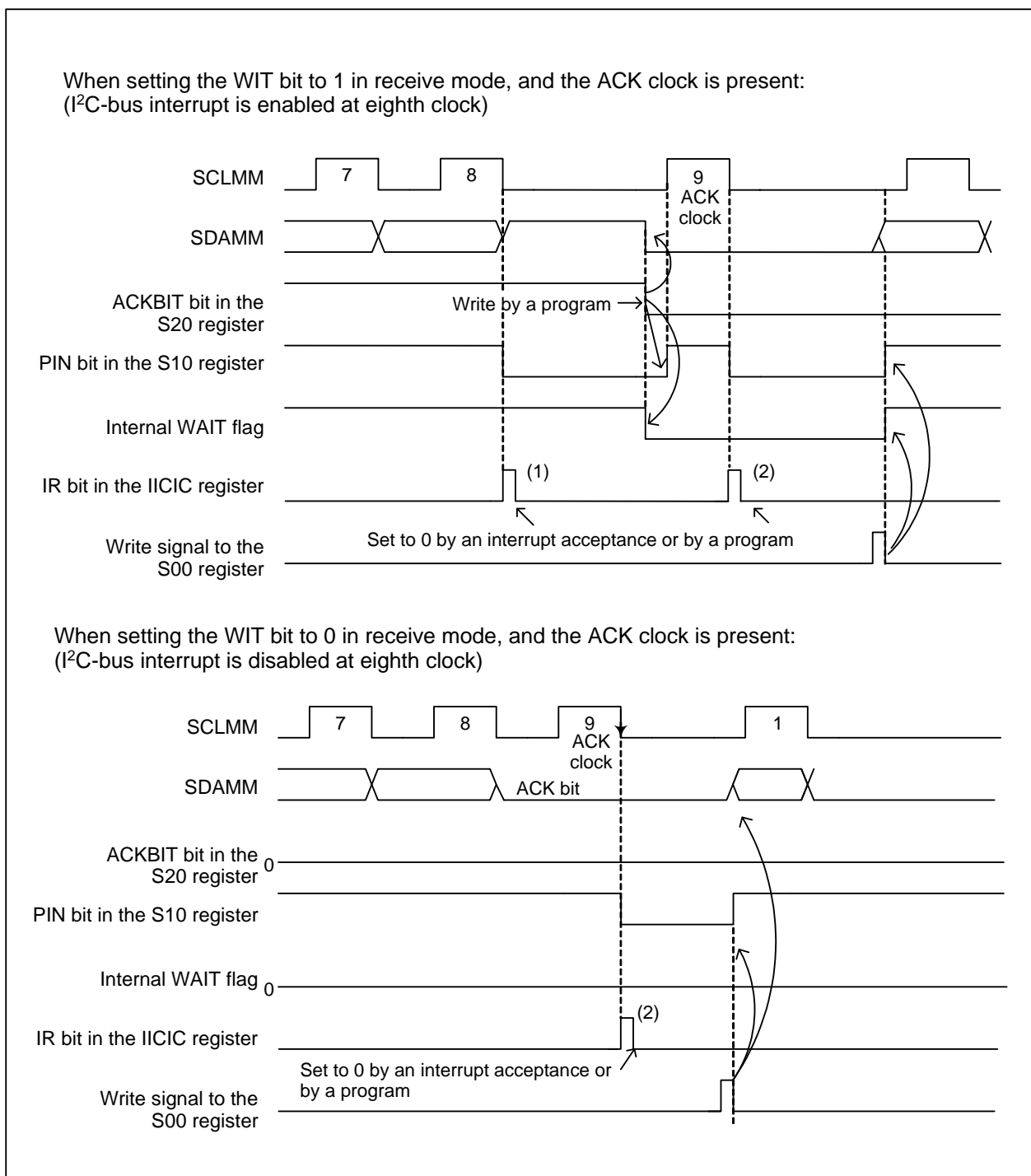
Table 22.6 lists interrupt request generation timing and the conditions to restart transmission/reception when receiving data. Figure 22.4 shows Interrupt Request Generation Timing in Receive Mode.

**Table 22.6 Generating an Interrupt Request and Restarting Transmission/Reception When Receiving Data**

I <sup>2</sup> C-bus Interrupt Request Generation Timing	Internal WAIT Flag Status	Conditions to Restart Transmission/Reception
At the falling edge of the eighth clock (before the ACK clock) <sup>(1)</sup>	1	Write to the ACKBIT bit in the S20 register <sup>(3)</sup>
At the falling edge of the ninth clock (ACK clock) <sup>(2)</sup>	0	Write to the S00 register

Notes:

1. See the timing of (1) on the IR bit in the IICIC register in Figure 22.4.
2. See the timing of (2) on the IR bit in the IICIC register in Figure 22.4.
3. When setting the ACKBIT bit, do not rewrite any other bits and do not set the S00 register.



**Figure 22.4 Interrupt Request Generation Timing in Receive Mode**

SDAM (Internal SDA output monitor bit) (b4)  
SCLM (Internal SCL output monitor bit) (b5)

The internal SDA and SCL output signal levels are the same as the output level of the I<sup>2</sup>C interface before it has any effect from the external device output. Bits SDAM and SCLM are read only bits. If necessary, set these bits to 0.

**ICK1 and ICK0 (I<sup>2</sup>C-bus system clock select bit) (b7-b6)**

Rewrite these bits when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled). fVIIC is selected by setting all the bits ICK1 to ICK0, bits ICK4 to ICK2 in the S4D0 register, and the PCLK0 bit in the PCLKR register. Refer to 22.3.1.2 "Bit Rate and Duty Cycle".

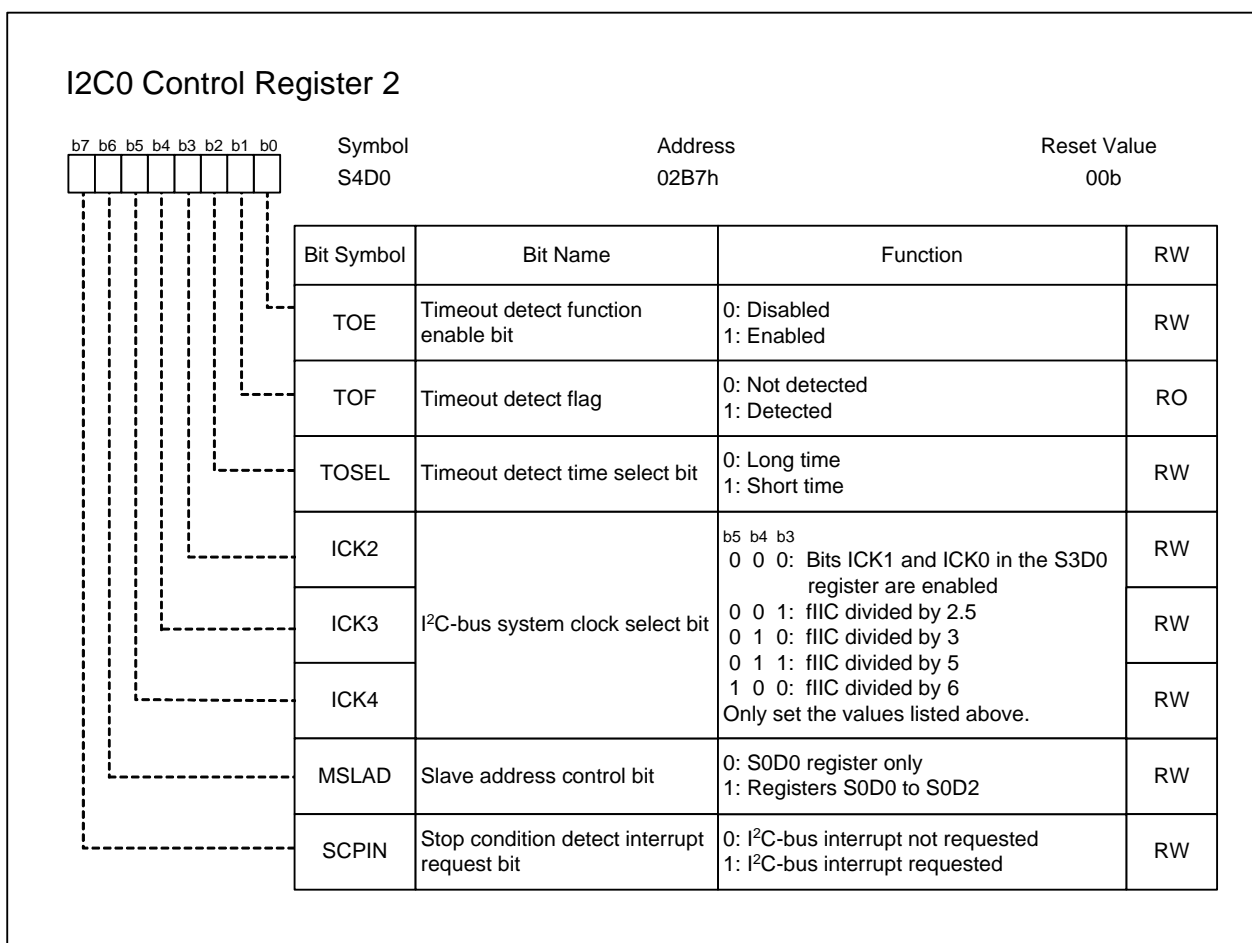
**Table 22.7 I<sup>2</sup>C-bus System Clock Select Bits**

S4D0 Register			S3D0 Register		fVIIC
ICK4 Bit	ICK3 Bit	ICK2 Bit	ICK1 Bit	ICK0 Bit	
0	0	0	0	0	fIIC divided-by-2
0	0	0	0	1	fIIC divided-by-4
0	0	0	1	0	fIIC divided-by-8
0	0	1	–	–	fIIC divided-by-2.5
0	1	0	–	–	fIIC divided-by-3
0	1	1	–	–	fIIC divided-by-5
1	0	0	–	–	fIIC divided-by-6

–: 0 or 1

Only set the values listed above.

## 22.2.7 I<sup>2</sup>C0 Control Register 2 (S4D0)



### TOE (Timeout detect function enable bit) (b0)

The TOE bit enables the timeout detect function. Refer to 22.3.9 “Timeout Detection” for details.

### TOF (Timeout detect flag) (b1)

The TOF bit is enabled when the TOE bit is set to 1. When the TOF bit becomes 1 (detected), the IR bit in the IICIC register becomes 1 (interrupt requested) at the same time.

Conditions to become 0:

- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

Condition to become 1:

- The BB bit in the S10 register is set to 1 (bus busy) and the SCLMM high period is greater than the timeout detect period.

**TOSEL (Timeout detect time select bit) (b2)**

Set the TOSEL bit to select a timeout detection period. The TOSEL bit is enabled when the TOE bit is 1 (timeout detect function enabled).

When long time is selected, the internal counter increments fVIIC as a 16-bit counter. When short time is selected, the internal counter increments fVIIC as a 14-bit counter. Therefore, the timeout detect time is as follows:

When the TOSEL bit is set to 0 (long time)

$$65536 \times \frac{1}{fVIIC}$$

When the TOSEL bit is set to 1 (short time)

$$16384 \times \frac{1}{fVIIC}$$

Table 22.8 lists Timeout Detect Time.

**Table 22.8 Timeout Detect Time**

fVIIC	Timeout Detect	
	TOSEL bit: 0 (Long time)	TOSEL bit: 1 (Short time)
4 MHz	16.4 ms	4.1 ms
2 MHz	32.8 ms	8.2 ms
1 MHz	65.6 ms	16.4 ms

Rewrite this bit when the TOE bit is 0.

**ICK4-ICK2 (I<sup>2</sup>C-bus system clock select bit) (b5-b3)**

Rewrite bits ICK4 to ICK2 when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).

fVIIC is selected by setting all the bits ICK4 to ICK2, bits ICK1 to ICK0 in the S3D0 register, and the PCLK0 bit in the PCLKR register. Refer to Table 22.7 "I<sup>2</sup>C-bus System Clock Select Bits" and 22.3.1.2 "Bit Rate and Duty Cycle".

**MSLAD (Slave address control bit) (b6)**

The MSLAD bit is enabled when the ALS bit in the S1D0 register is set to 0 (addressing format). The MSLAD bit is used to select the S0Di register (i = 0 to 2) used for slave address match detection.

**SCPIN (Stop condition detect interrupt request bit) (b7)**

The SCPIN bit is enabled when the SIM bit in the S3D0 register is set to 1 (enable I<sup>2</sup>C-bus interrupt by stop condition detection).

Condition to become 0:

- Writing 0 by a program.

Condition to become 1:

- Stop condition is detected  
(This bit cannot be set to 1 by a program.)



## 22.2.8 I<sup>2</sup>C0 Status Register 0 (S10)

I <sup>2</sup> C0 Status Register 0		Symbol	Address	Reset Value
		S10	02B8h	0001 000Xb
Bit Symbol	Bit Name	Function	RW	
LRB	Last receive bit	When read, 0: Last bit = 0 1: Last bit = 1  When write, see Table 22.9 "Functions Enabled by Writing to the S10 Register"	RW	
ADR0	General call detect flag	When read, 0: Not detected 1: Detected  When write, see Table 22.9 "Functions Enabled by Writing to the S10 Register"	RW	
AAS	Slave address compare flag	When read, 0: Address not matched 1: Address matched  When write, see Table 22.9 "Functions Enabled by Writing to the S10 Register"	RW	
AL	Arbitration lost detect flag	When read, 0: Not detected 1: Detected  When write, see Table 22.9 "Functions Enabled by Writing to the S10 Register"	RW	
PIN	I <sup>2</sup> C-bus interface interrupt request bit	When read, 0: Interrupt requested 1: Interrupt not requested  When write, see Table 22.9 "Functions Enabled by Writing to the S10 Register"	RW	
BB	Bus busy flag	When read, 0: Bus free 1: Bus busy  When write, see Table 22.9 "Functions Enabled by Writing to the S10 Register"	RW	
TRX	Communication mode select bit 0	0: Receive mode 1: Transmit mode	RW	
MST	Communication mode select bit 1	0: Slave mode 1: Master mode	RW	

Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use the MOV instruction to write to the S10 register.

Bit 5 to bit 0 in the S10 register (6 lower bits) monitor the state of the I<sup>2</sup>C interface. The bit values cannot be changed by a program. However, writing to the S10 register, including the 6 lower bits, generates a start/stop condition.

Bits MST and TRX are read and write bits. To change bits MST or TRX without generating a start/stop condition, set 1111b to the 4 lower bits in the S10 register.

Table 22.9 lists Functions Enabled by Writing to the S10 Register. Only set the values listed in Table 22.9. If the values listed in Table 22.9 are written to the S10 register, the 6 lower bits in the S10 register will not be changed.

**Table 22.9 Functions Enabled by Writing to the S10 Register**

Bit Setting of the S10 Register								Function
MST	TRX	BB	PIN	AL	AAS	ADR0	LRB	
1	1	1	0	0	0	0	0	Sets the I <sup>2</sup> C interface to start condition standby state in master transmit/receive mode
1	1	0	0	0	0	0	0	Sets the I <sup>2</sup> C interface to stop condition standby state in master transmit/receive mode
0	0	–	0	1	1	1	1	Slave receive mode
0	1	–	0	1	1	1	1	Slave transmit mode
1	0	–	0	1	1	1	1	Master receive mode
1	1	–	0	1	1	1	1	Master transmit mode

–: 0 or 1

Refer to 22.3.2 “Generating a Start Condition” and 22.3.3 “Generating a Stop Condition” for start/stop conditions.

#### LRB (Last receive bit) (b0)

When read, the LRB bit functions as described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

The LRB bit stores the value of the last bit of the received data. It is used to check if ACK is received.

The bit becomes 0 after writing to the S00 register.

#### ADR0 (General call detect flag) (b1)

The ADR0 bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- Stop condition is detected.
- Start condition is detected.
- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

Condition to become 1:

- The ALS bit in the S1D0 register is set to 0 (addressing format) and the received slave address is 0000000b (general call) in slave mode.

### AAS (Slave address compare flag) (b2)

The AAS bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- The S00 register is written.
- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

Conditions to become 1:

- In slave receive mode, the MSLAD bit in the S4D0 register is 1 (registers S0D0 to S0D2), the ALS bit in the S1D0 register is 0 (addressing format), and the received slave address is matched with bits SAD6 to SAD0 in any registers from S0D0 to S0D2.
- In slave receive mode, the MSLAD bit is 0, the ALS bit in the S1D0 register is 0 (addressing format), and the received slave address is matched with bits SAD6 to SAD0 in the S0D0 register.
- In slave receive mode, the ALS bit in the S1D0 register is 0 (addressing format) and the received slave address is 0000000b (general call).

### AL (Arbitration lost detect flag) (b3)

The AL bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- The S00 register is written.
- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

Conditions to become 1:

- In master transmit mode or master receive mode, the SDAMM pin level changes to low by an external device, not by the ACK clock, when slave address is transmitted.
- The SDAMM pin level changes to low by an external device for other than the ACK clock when data is transmitted in master transmit mode.
- In master transmit mode or master receive mode, the SDAMM pin level changes to low by an external device when start condition is transmitted.
- In master transmit mode or master receive mode, the SDAMM pin level changes to low by an external device when stop condition is transmitted.
- The function to prevent start condition overlaps is activated.

### PIN (I<sup>2</sup>C-bus interface interrupt request bit) (b4)

The PIN bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Conditions to become 0:

- Slave address transmission is completed in master mode (including a case of detecting arbitration lost).
- 1-byte data transmission is completed (including a case of detecting arbitration lost).
- 1-byte data reception is completed (the falling edge of eighth clock is detected when the ACKCLK bit in the S20 register is 0, or the falling edge of ACK clock when the ACKCLK bit is 1).
- The WIT bit in the S3D0 register is 1 (I<sup>2</sup>C-bus interrupt enabled at 8th clock) and 1-byte data reception is completed (before ACK clock).
- In slave receive mode, the MSLAD bit in the S4D0 register is 1, the ALS bit in the S1D0 register is 0 (addressing format), and any of the slave address stored in bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is matched with the received slave address (slave address match).
- In slave receive mode, the MSLAD bit is 0, the ALS bit is 0 (addressing format), and the slave address stored in bits SAD6 to SAD0 in the S0D0 register is matched with the received slave address (slave address match).
- In slave receive mode, the ALS bit in the S1D0 register is 0 (addressing format) and the received slaved address is 0000000b (general call).
- In slave receive mode, the ALS bit in the S1D0 register is 1 (free data format) and the slave address reception is completed.

Conditions to become 1:

- The S00 register is written.
- The S20 register is written (when the WIT bit is 1 and the internal WAIT flag is 1).
- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

The IR bit in the IICIC register becomes 1 (interrupt requested) as soon as the PIN bit becomes 0 (I<sup>2</sup>C-bus interrupt requested). When the PIN bit is 0, the SCLMM pin output level is low.

However, when all of the following conditions are met, the SCLMM pin does not output a low level signal:

- In master mode, arbitration lost is detected by a slave address or data
- The ALS bit in the S1D0 register is 0 (addressing format)
- The slave address is not 0000000b (general call) and does not match any of the bits from SAD6 to SAD0 in registers S0D0 to S0D2.

### BB (Bus busy flag) (b5)

The BB bit function in read access is described below. See Table 22.9 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

The BB bit indicates the state of the bus system, whether the bus is free or not. The BB bit changes depending on the SCLMM and SDAMM input signals, regardless of master mode or slave mode.

Conditions to become 0:

- Stop condition is detected.
- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

Condition to become 1:

- Start condition is detected.

### TRX (Communication mode select bit 0) (b6)

Set the TRX bit to select transmit mode or receive mode.

Conditions to become 0:

- The TRX bit is set to 0 by a program.
- Arbitration lost is detected.
- Stop condition is detected.
- Start condition overlap protect function is enabled.
- Start condition is detected when the MST bit in the S10 register is 0 (slave mode).
- No ACK is detected from a receiver when the MST bit in the S10 register is 0 (slave mode).
- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).

Conditions to become 1:

- The TRX bit is set to 1 by a program.
- In slave mode, the ALS bit in the S1D0 register is 0 (addressing format), the AAS bit in the S10 register becomes 1 (address matched) after receiving the slave address, and the received R/W bit is 1.

### MST (Communication mode select bit 1) (b7)

Set the MST bit to select master mode or slave mode.

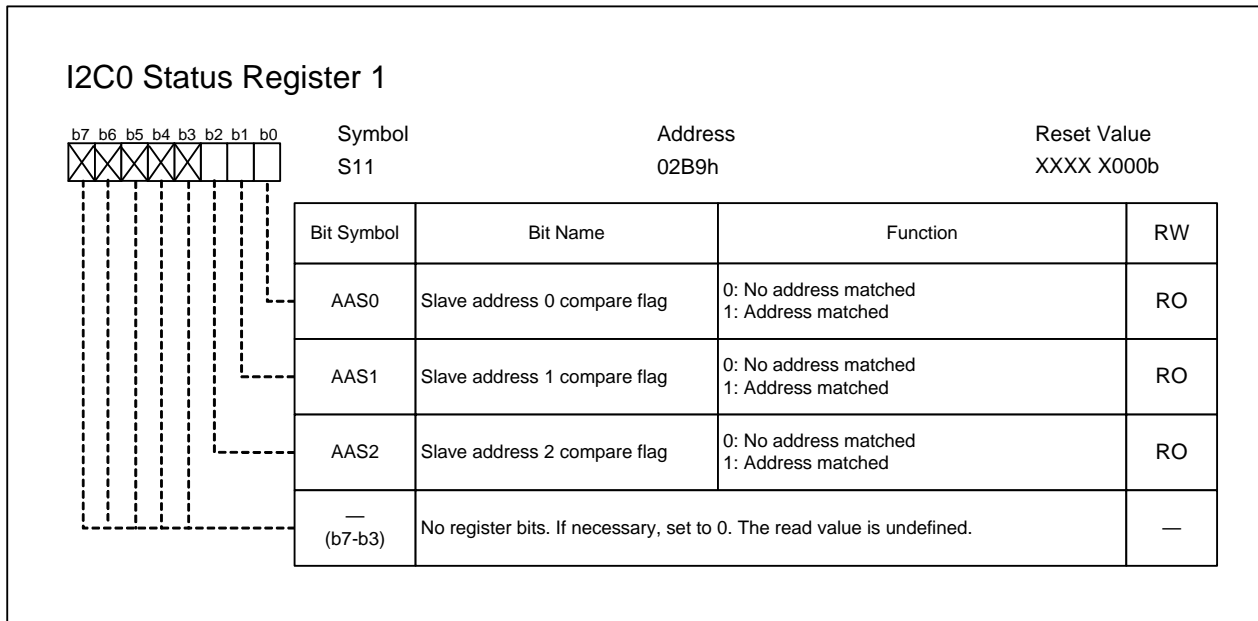
Conditions to become 0:

- The MST bit is set to 0 by a program.
- The 1-byte data that lost arbitration is completed transmitting/receiving when arbitration lost is detected.
- Stop condition is detected.
- Start condition overlap protect function is enabled.
- The ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is 1 (I<sup>2</sup>C interface reset).

Conditions to become 1:

- The MST bit is set to 1 by a program.

### 22.2.9 I<sup>2</sup>C0 Status Register 1 (S11)



AAS0 (Slave address 0 compare flag) (b0)

AAS1 (Slave address 1 compare flag) (b1)

AAS2 (Slave address 2 compare flag) (b2)

When the ALS bit in the S1D0 register is 0 (addressing format), any slave address stored in bits SAD6 to SAD0 in the S0Di register ( $i = 0$  to 2) is compared with the received slave address. The compare result is shown in the AASi bit. The AASi bit becomes 1 when there is an address match or when a general call address is received.

The AAS0 bit is enabled when the MSLAD bit in the S4D0 register is 0 (S0D0 register only). Bits AAS2 to AAS0 are enabled when the MSLAD bit is 1 (registers S0D0 to S0D2).

Conditions to become 0:

- The ES0 bit in the S1D0 register is set to 0 (I<sup>2</sup>C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I<sup>2</sup>C interface reset).
- The S00 register is written.

## 22.3 Operations

### 22.3.1 Clock

Figure 22.5 shows the I<sup>2</sup>C-bus Interface Clock.

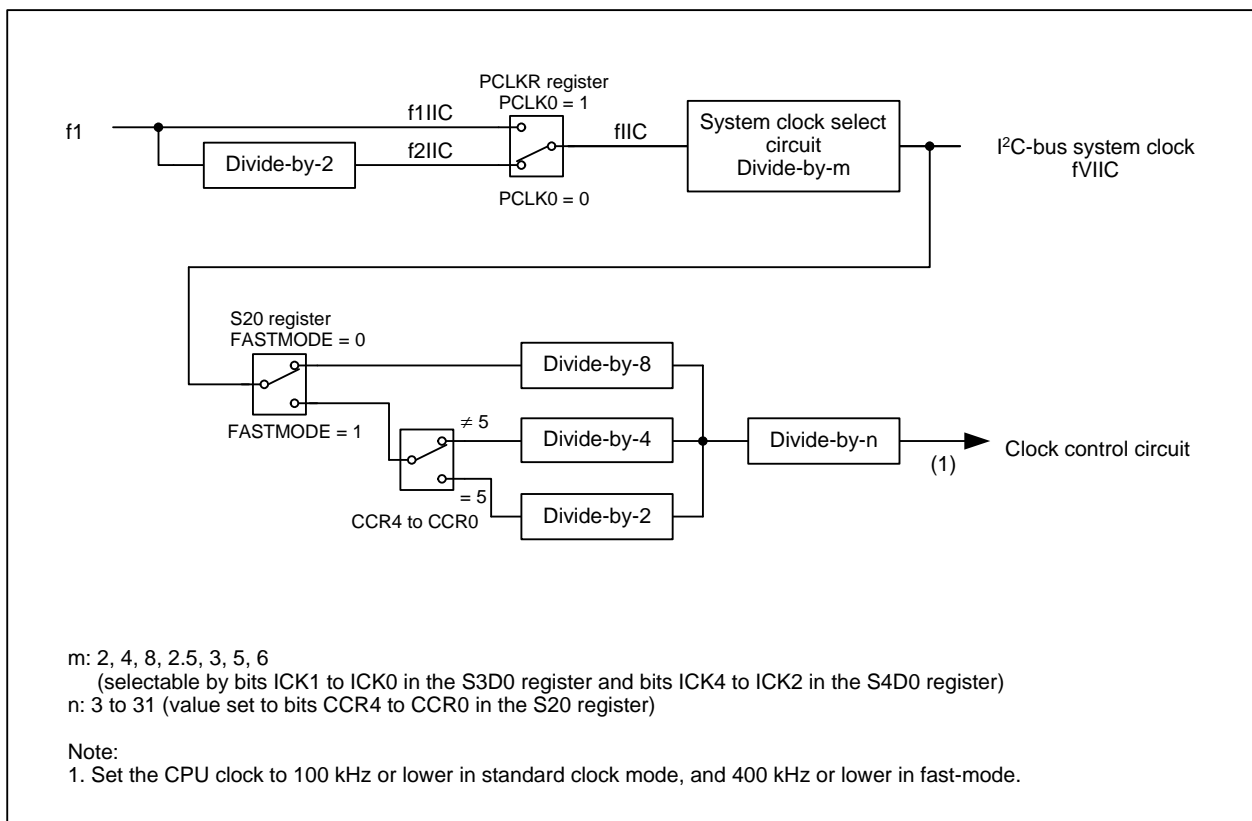


Figure 22.5 I<sup>2</sup>C-bus Interface Clock

#### 22.3.1.1 fVIIC

fVIIC is determined by setting a combination of the following:

- The frequency of peripheral clock  $f_1$
- The PCLK0 bit in the PCLKR register
- Bits ICK1 to ICK0 in the S3D0 register
- Bits ICK4 to ICK2 in the S4D0 register

fVIIC stops when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).

See Table 22.7 "I<sup>2</sup>C-bus System Clock Select Bits" for details.

### 22.3.1.2 Bit Rate and Duty Cycle

Bit rate is determined by a combination of fVIIC, the FASTMODE bit in the S20 register, and bits CCR4 to CCR0 in the S20 register.

Table 22.10 lists the Bit Rate of Internal SCL Output and Duty Cycle. When the change in the internal SCL output high level is a negative value, although the low period increases the amount that the high periods decreases, the bit rate does not increase. The values described in the following table are the values of the internal SCL output before being effected by the SCL output of an external device.

**Table 22.10 Bit Rate of Internal SCL Output and Duty Cycle**

Item	Standard Clock Mode (FASTMODE = 0)	Fast-mode (FASTMODE = 1) (CCR value = other than 5)	Fast-mode (FASTMODE = 1) (CCR value = 5)
Bit rate (bps)	$\frac{fVIIC}{8 \times CCR \text{ value}}$	$\frac{fVIIC}{4 \times CCR \text{ value}}$	$\frac{fVIIC}{2 \times CCR \text{ value}} = \frac{fVIIC}{10}$
Duty cycle	50% Fluctuation of high level: -4 to +2 fVIIC cycles	50% Fluctuation of high level: -2 to +2 fVIIC cycles	35 to 45%

CCR value: Value set to bits CCR4 to CCR0

When the CCR value (setting value of bits CCR4 to CCR0) is 5 (00101b) in fast-mode, the bit rate is assumed to reach 400 kbps, the maximum bit rate in fast-mode.

The bit rate and duty cycle are as follows.

- Bit rate:

$$\frac{fVIIC}{2 \times CCR \text{ value}} = \frac{fVIIC}{10}$$

When fVIIC is 4 MHz, the bit rate is 400 kbps.

- Duty cycle is 35 to 45%

Even if the bit rate is 400 kbps, the 1.3 μs minimum low period of the SCLMM clock (I<sup>2</sup>C-bus standard) is allocated. Table 22.11 lists the Bit Setting for Bits CCR4 to CCR0 and Bit Rate (fVIIC = 4 MHz).

**Table 22.11 Bit Setting for Bits CCR4 to CCR0 and Bit Rate (fVIIC = 4 MHz)**

Bits CCR4 to CCR0 in the S20 Register					Bit Rate (kbps)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard Clock Mode	Fast-mode
0	0	0	0	0	Do not set (1)	Do not set (1)
0	0	0	0	1	Do not set (1)	Do not set (1)
0	0	0	1	0	Do not set (1)	Do not set (1)
0	0	0	1	1	Do not set (2)	333
0	0	1	0	0	Do not set (2)	250
0	0	1	0	1	100	400
0	0	1	1	0	83.3	166
:	:	:	:	:	:	:
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes:

1. Do not set bits CCR4 to CCR0 to 0 to 2 regardless of the fVIIC frequency.
2. Do not exceed the maximum bit rates of 100 kbps in standard clock mode and 400 kbps in fast-mode.



### 22.3.1.3 Receiving a Slave Address in Wait Mode and Stop Mode

When the CM02 bit in the CM0 register is set to 0 (peripheral clock f1 does not stop in wait mode) and transition is made to wait mode, the I<sup>2</sup>C interface can receive the slave address even in wait mode.

When the CM02 bit in the CM0 register is set to 1 (peripheral clock f1 stops in wait mode) and transition is made to wait mode, the I<sup>2</sup>C interface stops operating because fVIIC supply is stopped in stop mode and low-power consumption mode.

The SCL/SDA interrupt can be used in either wait mode or stop mode.

### 22.3.2 Generating a Start Condition

Follow the procedure below when the ES0 bit in the S1D0 register is 1 (I<sup>2</sup>C interface enabled) and the BB bit in the S10 register is set to 0 (bus free). Figure 22.6 shows the Procedure to Generate a Start Condition.

(1) Write E0h to the S10 register.

The I<sup>2</sup>C interface enters the start condition standby state and the SDAMM pin is released.

(2) Write a slave address to the S00 register.

A start condition is generated. Then, the bit counter becomes 000b, the SCL clock signal is output for 1 byte, and the slave address is transmitted.

After a stop condition is generated and the BB bit becomes 0 (bus free), a write to the S10 register is disabled for 1.5 fVIIC cycles. Therefore, even if the S00 register is subsequently written to, a start condition is not generated. When generating a start condition shortly after changing the BB bit from 1 to 0, confirm that both bits TRX and MST are 1 after executing step (1), then execute step (2).

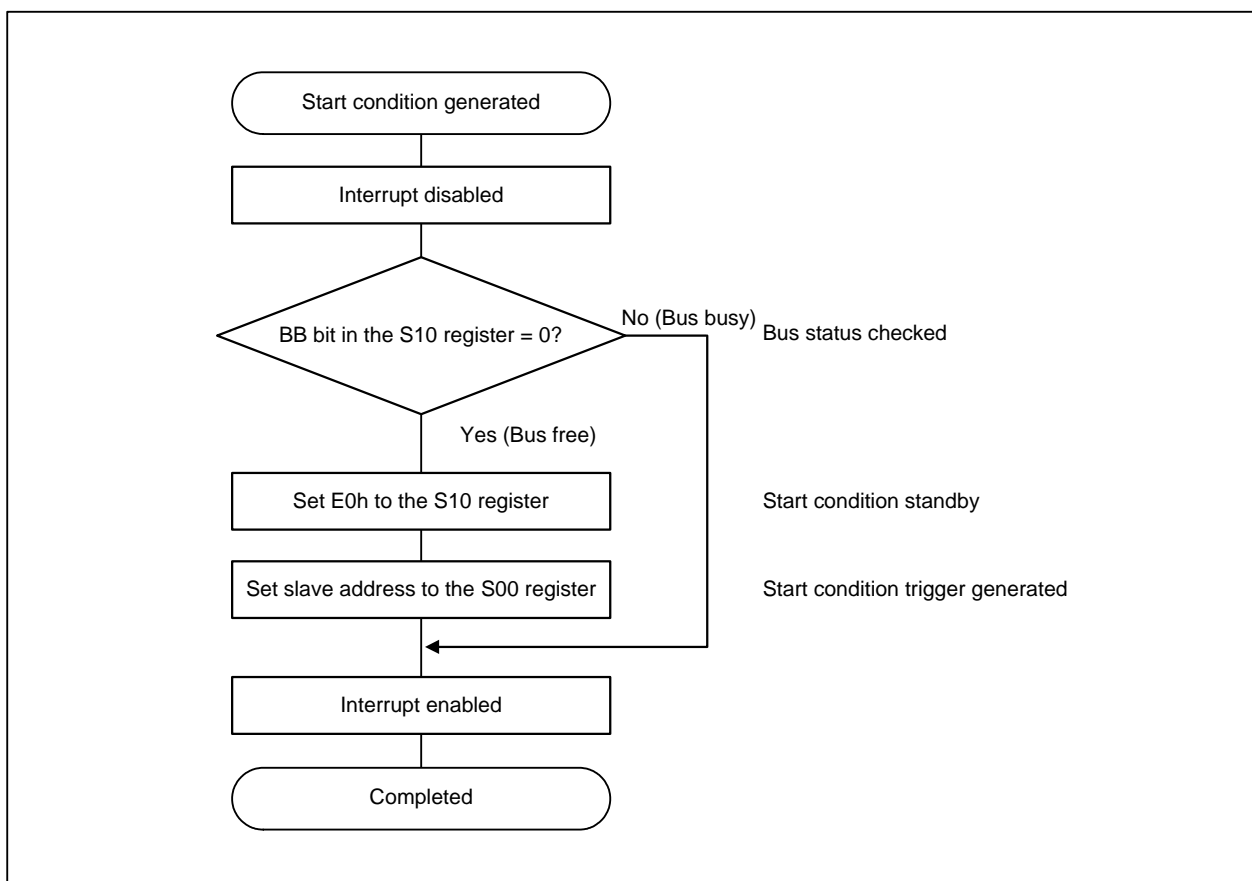
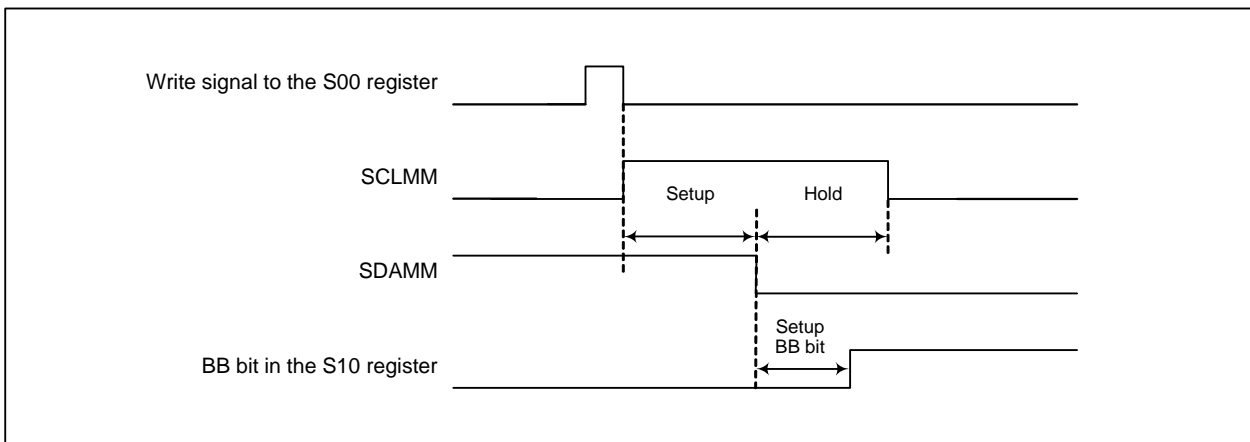


Figure 22.6 Procedure to Generate a Start Condition

The start condition generation timing depends on the modes - standard clock mode or fast-mode. Figure 22.7 shows the Start Condition Generation Timing. Table 22.12 lists the Setup/Hold Time for Generating a Start/Stop Condition.



**Figure 22.7 Start Condition Generation Timing**

**Table 22.12 Setup/Hold Time for Generating a Start/Stop Condition**

Item	STSPSEL Bit	Standard Clock Mode		Fast-mode	
		fVIIC cycles	fVIIC = 4 MHz	fVIIC cycles	fVIIC = 4 MHz
Setup time	0 (short mode)	20	5.0 μs	10	2.5 μs
	1 (long mode)	52	13.0 μs	26	6.5 μs
Hold time	0 (short mode)	20	5.0 μs	10	2.5 μs
	1 (long mode)	52	13.0 μs	26	6.5 μs
BB bit set/reset time	-	$\frac{SSC\ value - 1}{2} + 2$	3.375 μs (1)	3.5	0.875 μs

-: 0 or 1

STSPSEL: Bit in the S2D0 register

SSC value: Value of bits SSC4 to SSC0 in the S2D0 register

Note:

1. Example value when bits SSC4 to SSC0 are 11000b.

### 22.3.3 Generating a Stop Condition

Use the following procedure when the ES0 bit in the S1D0 register is 1 (I<sup>2</sup>C interface enabled).

(1) Write C0h to the S10 register.

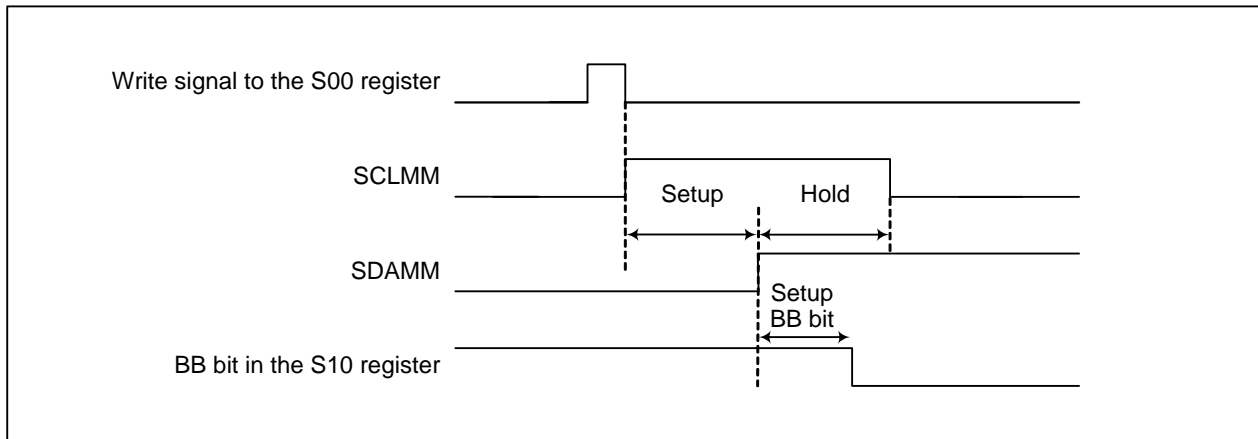
The I<sup>2</sup>C interface enters the stop condition standby state and the SDAMM pin is driven low.

(2) Write dummy data to the S00 register.

A stop condition is generated.

The stop condition generation timing depends on the modes - standard clock mode or fast-mode.

Figure 22.8 shows the Stop Condition Generation Timing. See Table 22.12 "Setup/Hold Time for Generating a Start/Stop Condition" for setup/hold time.



**Figure 22.8 Stop Condition Generation Timing**

Do not write to the S10 register or S00 register until the BB bit in the S10 register becomes 0 (bus free) after the instructions to generate a stop condition (refer to above (2)) are executed.

If the SCLMM pin input signal becomes low until the BB bit in the S10 register becomes 0 (bus free) from the instruction to generate a stop condition is executed and the SCLMM pin becomes high-level, the internal SCL output becomes low. In this case, perform one of the steps below to stop the low signal output from the SCLMM pin (release the SCLMM pin).

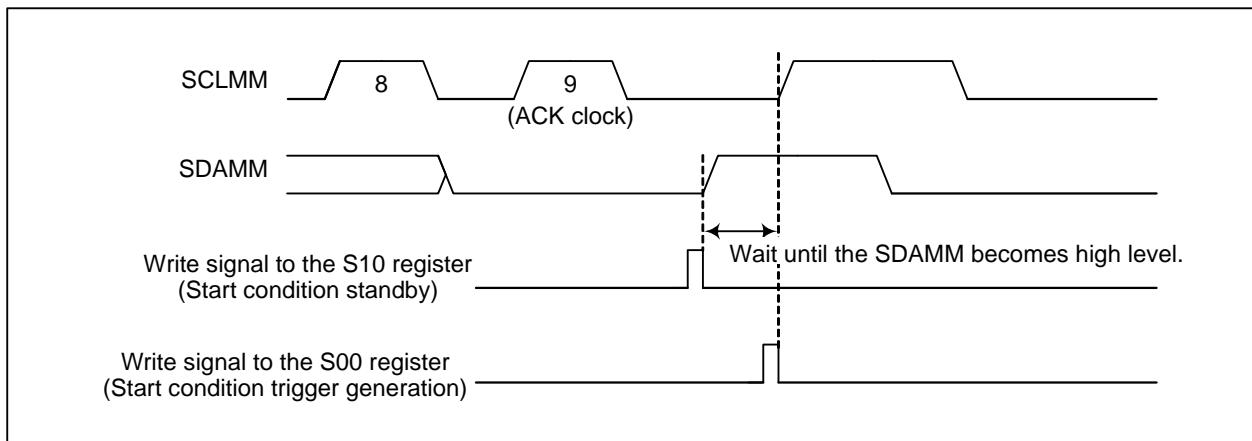
- Generate a stop condition (perform steps (1) and (2) above).
- Set the ES0 bit in the S1D0 register to 0 (I<sup>2</sup>C interface disabled).
- Write 1 to the IHR bit (I<sup>2</sup>C interface reset).

### 22.3.4 Generating a Restart Condition

Use the following procedure to generate a restart condition when 1-byte data is transmitted/received.

- (1) Write E0h to the S10 register. (Start condition standby state. The SDAMM pin released.)
- (2) Wait until the SDAMM pin level becomes high.
- (3) Write a slave address to the S00 register (a start condition trigger is generated)

Figure 22.9 shows the Restart Condition Generation Timing.



**Figure 22.9 Restart Condition Generation Timing**

### 22.3.5 Start Condition Overlap Protect

The I<sup>2</sup>C interface generates a start condition by setting registers S10 and S00 by a program. The bus system must be free before setting these registers. Check whether the bus is free with the BB bit in the S10 register by a program before setting the registers.

However, even after confirming that the bus is free, other master devices may generate a start condition before setting registers S10 and S00. In this case, when the I<sup>2</sup>C interface detects a start condition, the BB bit becomes 1 (bus busy) and the start condition overlap protect function is activated.

The start condition overlap protect function operates as follows:

- The multi-master I<sup>2</sup>C-bus interface does not enter start condition standby state even if the S10 register is set to E0h.
- If the I<sup>2</sup>C interface is in a start condition standby state, exit the state.
- A start condition trigger is not generated even if a data is written to the S00 register by program.
- Bits MST and TRX in the S10 register become 0 (slave receive mode).
- The AL bit in the S10 register becomes 1 (arbitration lost detected).

Figure 22.10 shows the Start Condition Overlap Protect Operation.

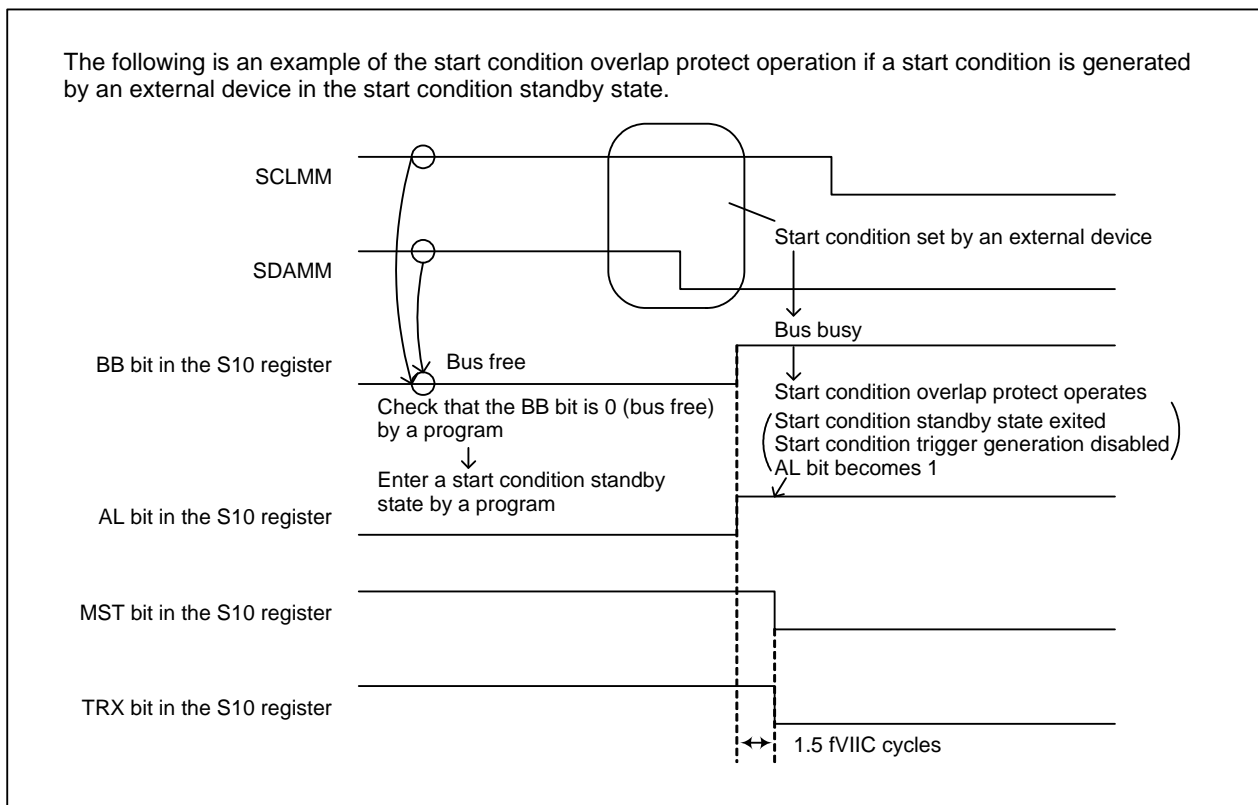
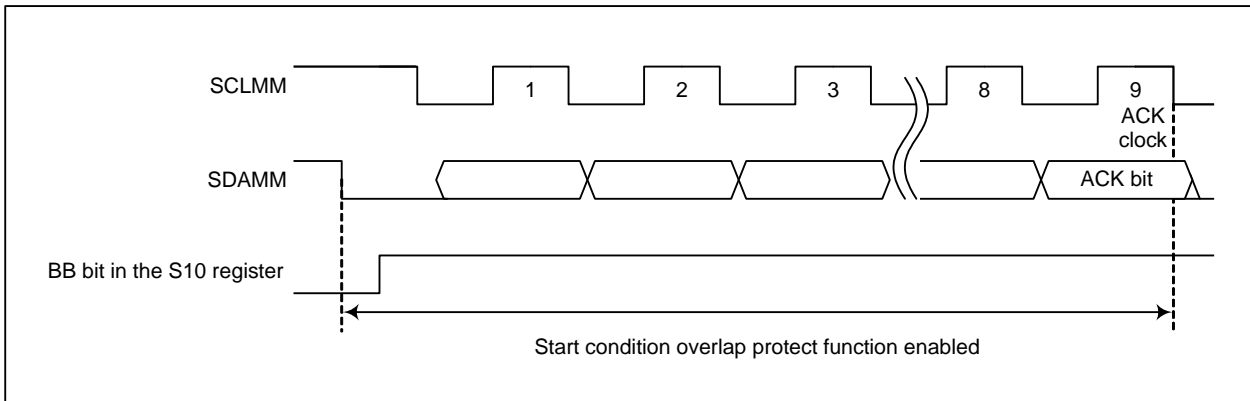


Figure 22.10 Start Condition Overlap Protect Operation

The start condition overlap protect is enabled from the falling edge of SDAMM (start condition) to the completion of the slave address receive. If data is written to registers S10 and S00 during that period, the above operation is performed. Figure 22.11 shows the Start Condition Overlap Protect Function Enable Period.



**Figure 22.11 Start Condition Overlap Protect Function Enable Period**

### 22.3.6 Arbitration Lost

When all of the conditions below are met, the SDAMM pin signal level becomes low by an external device and the I<sup>2</sup>C interface determines that it has lost arbitration.

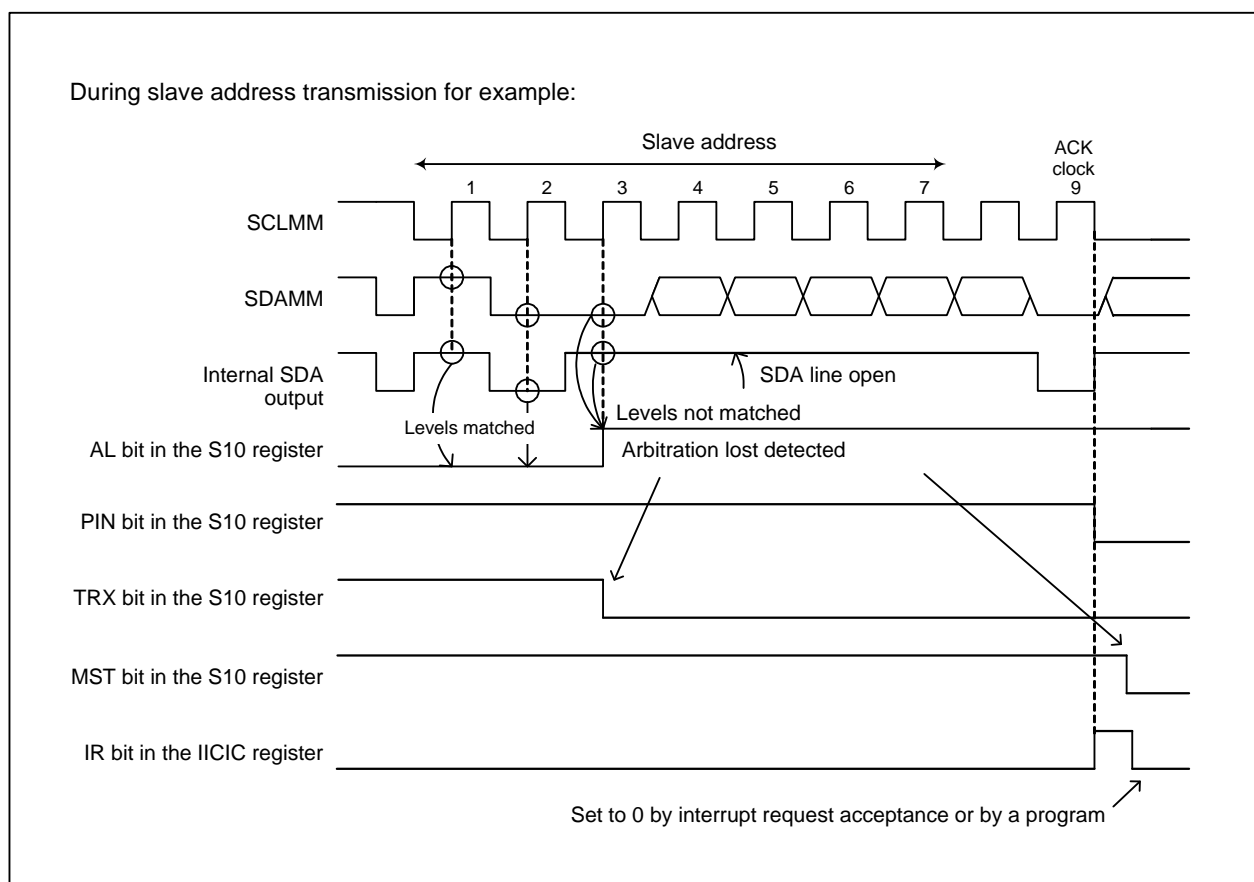
(a) Transmit/receive (one of the following)

- Slave address transmit (not an ACK clock) in master transmit mode or master receive mode
- Data transmit (not an ACK clock) in master transmit mode
- Start condition generated in master transmit mode or master receive mode
- Stop condition generated in master transmit mode or master receive mode

(b) Internal SDA output: High

(c) SDAMM pin level: Low (sampling at the rising edge of the clock of SCLMM pin.)

Figure 22.12 shows Operation Example When Arbitration Lost is Detected.



**Figure 22.12 Operation Example When Arbitration Lost is Detected**



When arbitration lost is detected:

- The AL bit in the S10 register becomes 1 (arbitration lost detected)
- Internal SDA output becomes high. (SDAMM released)
- The I<sup>2</sup>C interface enters the slave receive mode
  - The TRX bit in the S10 register is 0 (receive mode).
  - The MST bit in the S10 register is 0 (slave mode).

In order to set the AL bit to 0 again after arbitration lost is detected, set a value to the S00 register.

When arbitration lost is detected during slave address transmission, the I<sup>2</sup>C interface automatically enters slave receive mode and receives the slave address sent from another master. When the ALS bit in the S1D0 register is 0 (addressing format), the slave address comparison result is determined by reading bits ADR0 and AAS in the S10 register.

When arbitration lost is detected during data transmission, the I<sup>2</sup>C interface automatically enters slave receive mode.

Also, when arbitration lost is detected, the TRX bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, read the S00 register after arbitration lost is detected. When bit 0 in the S00 register is 1, write 4Fh (slave transmit mode) to the S10 register and execute slave transmission.

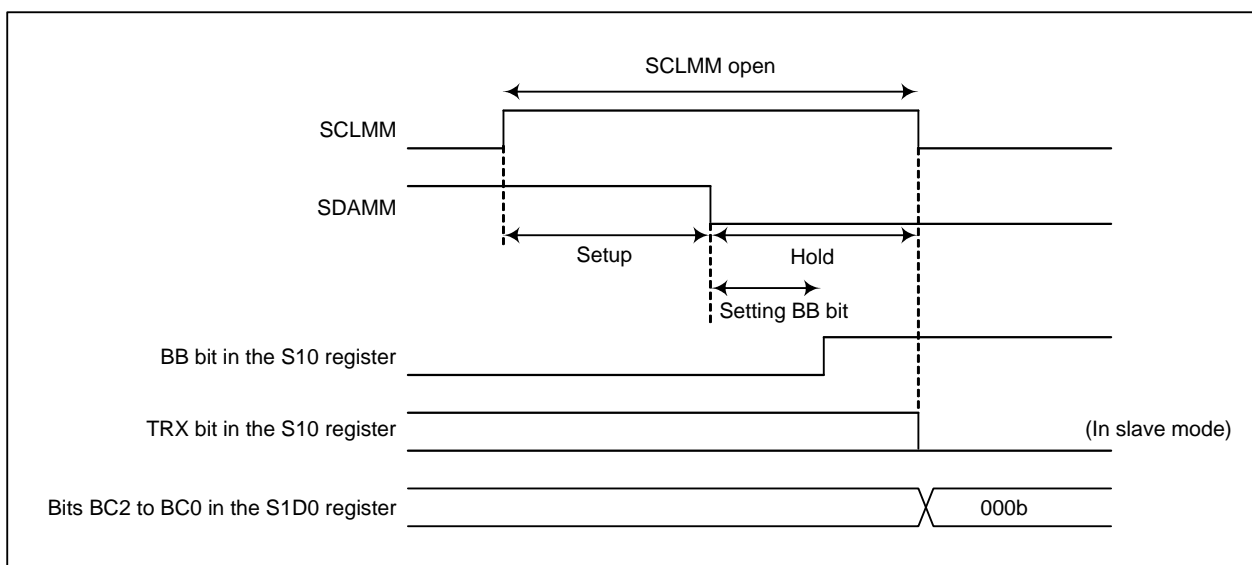
### 22.3.7 Detecting Start/Stop Conditions

Figure 22.13 shows Start Condition Detection, Figure 22.14 shows Stop Condition Detection, and Table 22.13 lists Conditions to Detect Start/Stop Condition.

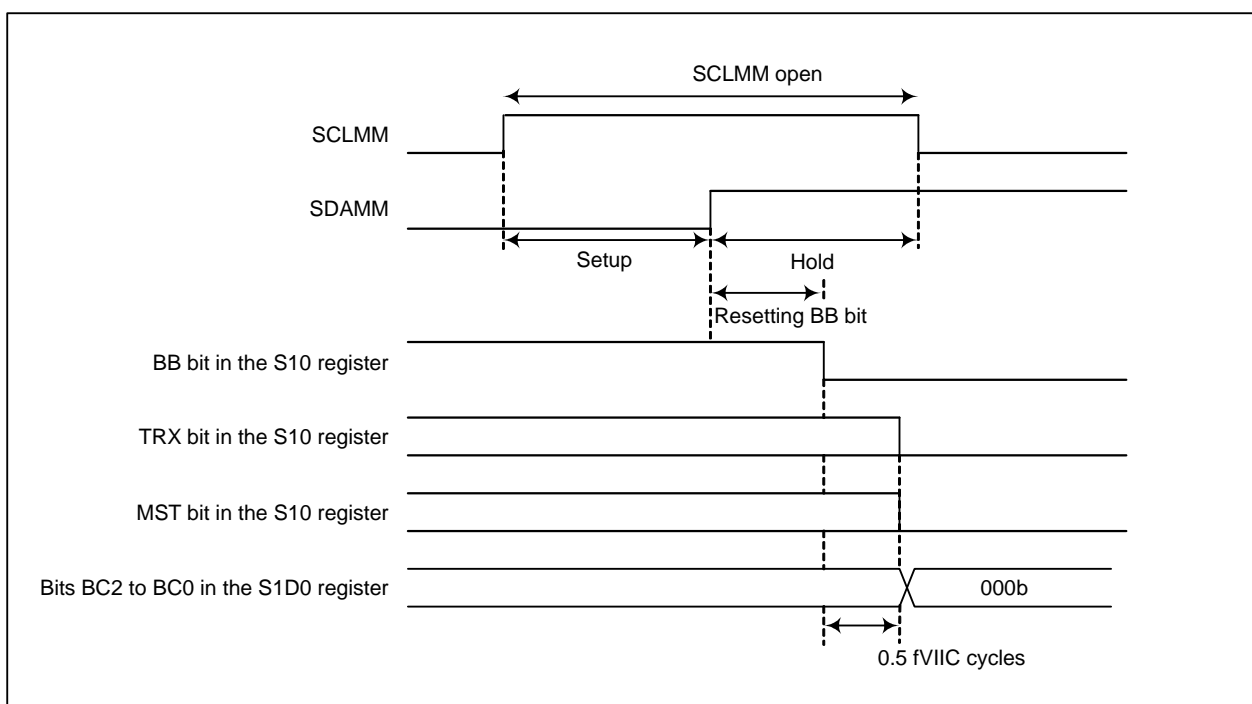
A start/stop condition can be detected only when the start/stop condition detect parameters are selected by setting bits SSC4 to SSC0 in the S2D0 register, and the signals input to pins SCLMM and SDAMM meet all three conditions (SCLMM release time, setup time, and hold time) listed in Table 22.13.

The BB bit in the S10 register becomes 1 when a start condition is detected, and becomes 0 when a stop condition is detected. The set timing and reset timing of the BB bit depends on whether the mode is standard mode or fast-mode. Refer to the BB bit set/reset times in Table 22.14.

Table 22.14 lists the Recommended Values of Bits SSC4 to SSC0 in Standard Clock Mode.



**Figure 22.13 Start Condition Detection**



**Figure 22.14 Stop Condition Detection**

**Table 22.13 Conditions to Detect Start/Stop Condition**

	Standard Clock Mode	Fast-Mode
SCLMM open time	SSC value + 1 cycle	4 cycles
Setup time	$\frac{\text{SSC value}}{2} + 1$ cycle	2 cycles
Hold time	$\frac{\text{SSC value}}{2}$ cycles	2 cycles
BB bit setting/resetting time	$\frac{\text{SSC value} - 1}{2} + 2$ cycles	3.5 cycles

Unit: Number of fVIIC cycles

SSC value: Value of bits SSC4 to SSC0 in the S2D0 register

**Table 22.14 Recommended Values of Bits SSC4 to SSC0 in Standard Clock Mode**

fVIIC	SSC Value (recommended)	Start/Stop Condition Detect Parameter			BB Bit Setting/Resetting Time
		SCLMM open time	Setup time	Hold time	
5 MHz	11110b	6.2 μs (31)	3.2 μs (16)	3.0 μs (15)	3.3 μs (16.5)
4 MHz	11010b	6.75 μs (27)	3.5 μs (14)	3.25 μs (13)	3.625 μs (14.5)
	11000b	6.25 μs (25)	3.25 μs (13)	3.0 μs (12)	3.375 μs (13.5)
2 MHz	01100b	6.5 μs (13)	3.5 μs (7)	3.0 μs (6)	3.75 μs (7.5)
	01010b	5.5 μs (11)	3.0 μs (6)	2.5 μs (5)	3.25 μs (6.5)
1 MHz	00100b	5.0 μs (5)	3.0 μs (3)	2.0 μs (2)	3.5 μs (3.5)

SSC value: Value of bits SSC4 to SSC0 in the S2D0 register

( ): Number of fVIIC cycles

### 22.3.8 Operation after Transmitting/Receiving a Slave Address or Data

After a slave address or 1-byte data has been transmitted/received, the PIN bit in the S10 register becomes 0 (interrupt requested) at the falling edge of the ACK clock. The IR bit in the IICIC register becomes 1 (interrupt requested) at the same time. The value in the S10 register or other register changes depending on the state of the transmit/receive data, and the level of pins SCLMM and SDAMM. Figure 22.15 shows Operation When Transmitted/Received a Slave Address or Data.

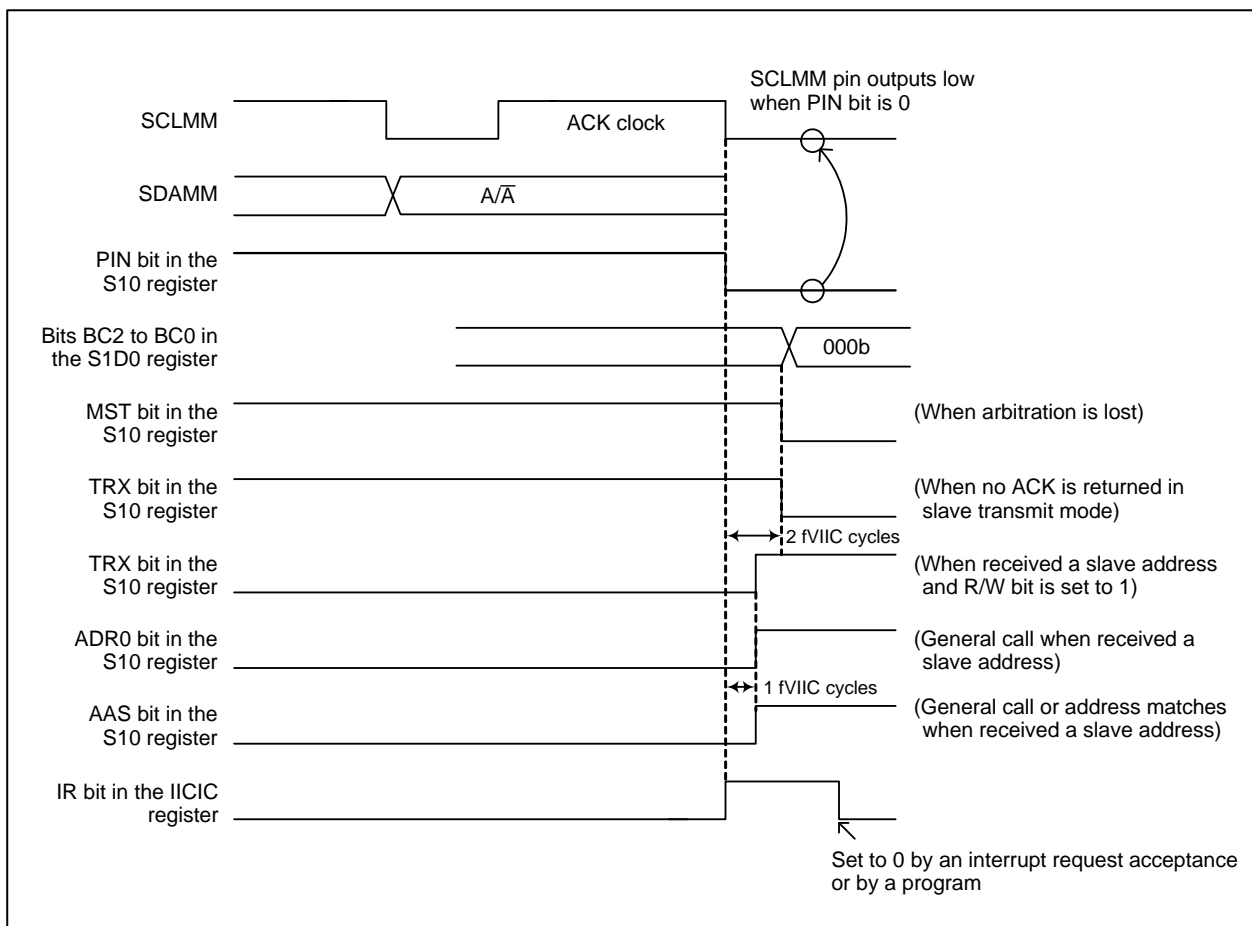
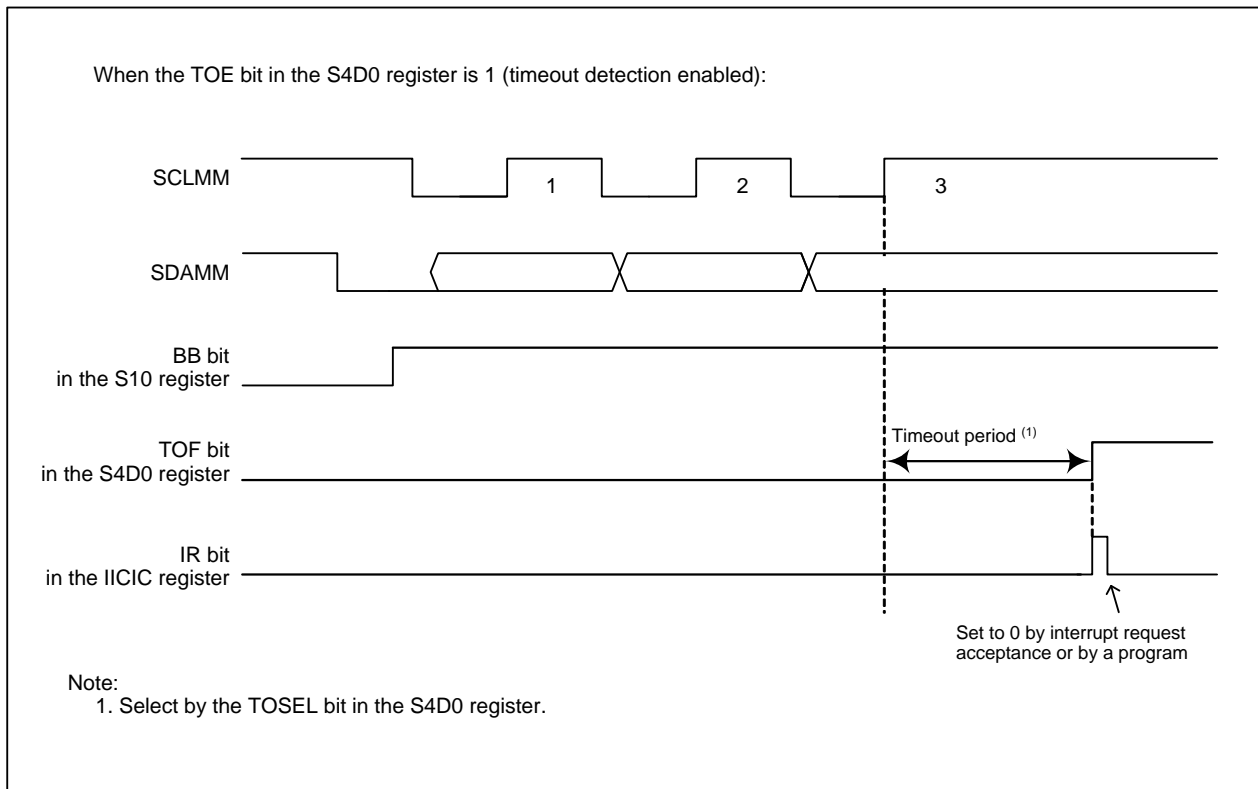


Figure 22.15 Operation When Transmitted/Received a Slave Address or Data

### 22.3.9 Timeout Detection

When the SCL clock is stopped during transmission/reception, each device stops operating, keeping the communication state. To avoid this, the I<sup>2</sup>C interface incorporates a function to detect timeouts and generate an I<sup>2</sup>C-bus interrupt request when the SCLMM pin is driven high for more than the selected timeout detection period during transmission/reception. Figure 22.16 shows the Timeout Detection Timing. Refer to “TOSEL (Timeout Detection Period Select Bit) (b2)” in 22.2.7 “I<sup>2</sup>C0 Control Register 2 (S4D0)” for the timeout detection period.



**Figure 22.16 Timeout Detection Timing**

A timeout is detected when the all of the following conditions are met:

- The TOE bit in the S4D0 register is 1 (timeout detection enabled)
- The BB bit in the S10 register is 1 (bus busy)
- The SCLMM pin is driven high for more than the timeout detect period

When a timeout is detected:

- The TOF bit in the S4D0 register becomes 1 (timeout detected)
- The IR bit in the IICIC register becomes 1 (I<sup>2</sup>C-bus interrupt requested)

When the timeout is detected, perform one of the following:

- Set the ES0 bit in the S1D0 register to 0 (disabled).
- Set the IHR bit in the S1D0 register to 1 (I<sup>2</sup>C interface reset).

### 22.3.10 Data Transmit/Receive Examples

The data transmit/receive examples are described in this section. The conditions for the examples are as follows:

- Slave address: 7 bits
- Data: 8 bits
- ACK clock
- Standard clock mode, bit rate: 100 kbps (fIIC: 20 MHz; fVIIC: 4 MHz)  
20 MHz (fIIC) divided-by-5 = 4 MHz (fVIIC),  
4 MHz (fVIIC) divided-by-8 and further divided-by-5 = 100 kbps (bit rate)
- In receive mode, an ACK is returned for received data other than the last data. NACK is returned after the last data is received.
- When receiving data, I<sup>2</sup>C-bus interrupt at the eighth clock (just before ACK clock): disabled
- Stop condition interrupt: enabled
- Timeout detect interrupt: disabled
- Set an own slave address to the S0D0 register (registers S0D1 or S0D2 should not be used)

When enabling an I<sup>2</sup>C-bus interrupt at the eighth clock (just before ACK clock) during data reception, a receiver can determine whether to generate ACK or NACK after checking the received data each byte.

#### 22.3.10.1 Initial Settings

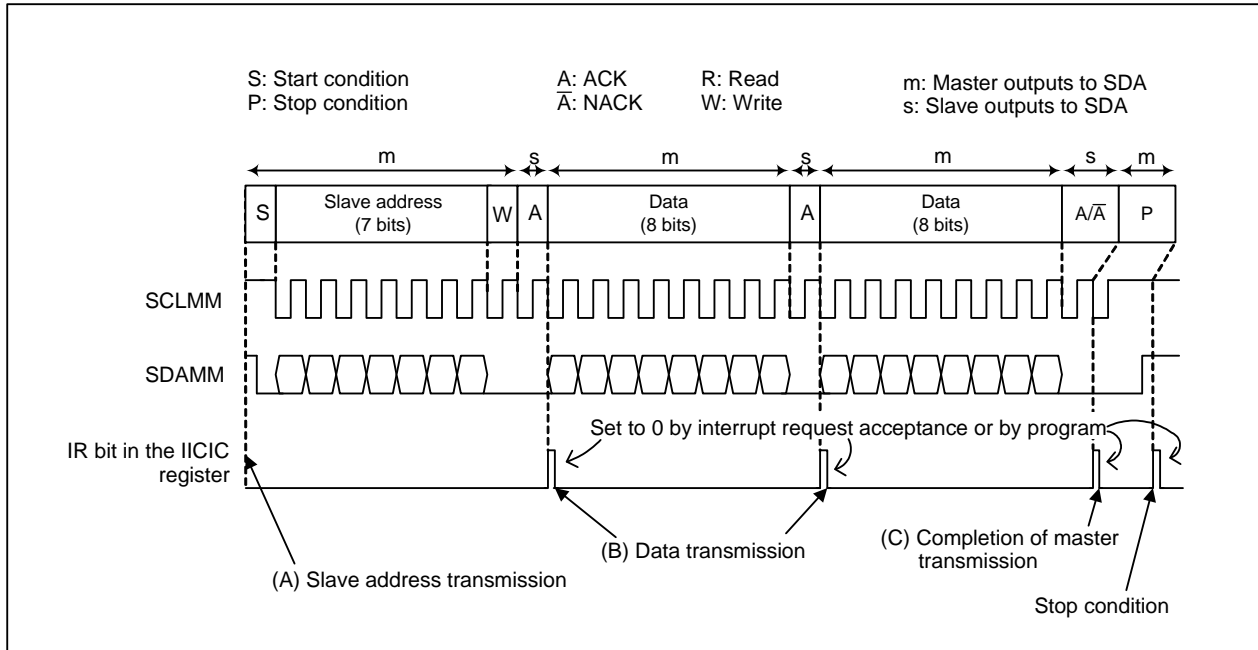
Follow the initial setting procedures below for 22.3.10.2 to 22.3.10.5.

- (1) Write an own slave address to bits SAD6 to SAD0 in the S0D0 register.
- (2) Write 85h to the S20 register. (CCR value: 5, standard clock mode, ACK clock presents)
- (3) Write 18h to the S4D0 register. (fVIIC: fIIC divided-by-5, timeout interrupt disabled)
- (4) Write 01h to the S3D0 register. (stop condition detect interrupt enabled and I<sup>2</sup>C-bus interrupt at eighth clock is disabled when receiving data)
- (5) Write 0Fh to the S10 register. (slave receive mode)
- (6) Write 98h to the S2D0 register (SSC value: 18h; start/stop condition generation timing: long mode)
- (7) Write 08h to the S1D0 register (bit counter: 8, I<sup>2</sup>C interface enabled, addressing format, input level: I<sup>2</sup>C-bus input)

If the MCU uses a single-master system and it is a master, start the initial setting procedures from step (2).

### 22.3.10.2 Master Transmission

Master transmission is described in this section. The initial settings described in 22.3.10.1 "Initial Settings" are assumed to be completed. Figure 21.17 shows master transmission operation. The following programs (A) to (C) are executed at (A) to (C) in Figure 22.17, respectively.



**Figure 22.17 Example of Master Transmission**

#### (A) Slave address transmission

- (1) The BB bit in the S10 register must be 0 (bus free).
- (2) Write E0h to the S10 register. (start condition standby)
- (3) Write a slave address to the upper 7 bits and set the least significant bit (LSB) to 0. (start condition generated, then slave address transmitted)

#### (B) Data transmission

- (in I<sup>2</sup>C-bus interrupt routine)
- (1) Write transmit data to the S00 register. (data transmission)

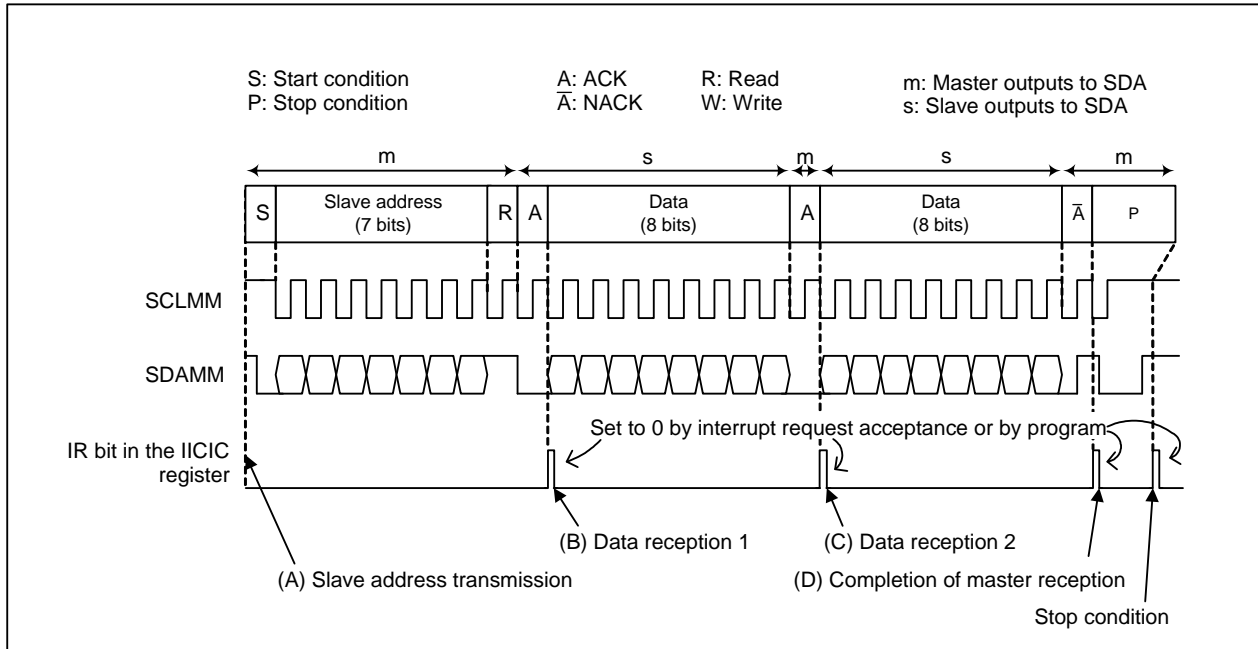
#### (C) Completion of Master transmission

- (in I<sup>2</sup>C-bus interrupt routine)
- (1) Write C0h to the S10 register. (Stop condition standby state)
  - (2) Write dummy data to the S00 register. (stop condition generated)

When transmission is completed or ACK is not returned from a slave device (NACK returned), master transmission should be completed as shown in the example above.

### 22.3.10.3 Master Reception

Master reception is described in this section. The initial settings described in 22.3.10.1 “Initial Settings” are assumed to be completed. Figure 22.18 shows the operation example of master reception. The following programs (A) to (D) are executed at (A) to (D) in Figure 22.18, respectively.



**Figure 22.18 Example of Master Reception**

#### (A) Slave address transmission

- (1) The BB bit in the S10 register must be 0 (bus free).
- (2) Write E0h to the S10 register. (Start condition standby)
- (3) Write a slave address to the upper 7 bits and a set the least significant bit (LSB) to 1. (Start condition generated, then slave address transmitted)

#### (B) Data reception 1 (after slave address transmission)

- (In I<sup>2</sup>C-bus interrupt routine)
- (1) Write AFh to the S10 register. (Master receive mode)
  - (2) Set the ACKBIT bit in the S20 register to 0 (ACK presents) because the data is not the last one.
  - (3) Write dummy data to the S00 register

#### (C) Data reception 2 (data reception)

- (In I<sup>2</sup>C-bus interrupt routine)
- (1) Read the received data from the S00 register
  - (2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
  - (3) Write dummy data to the S00 register

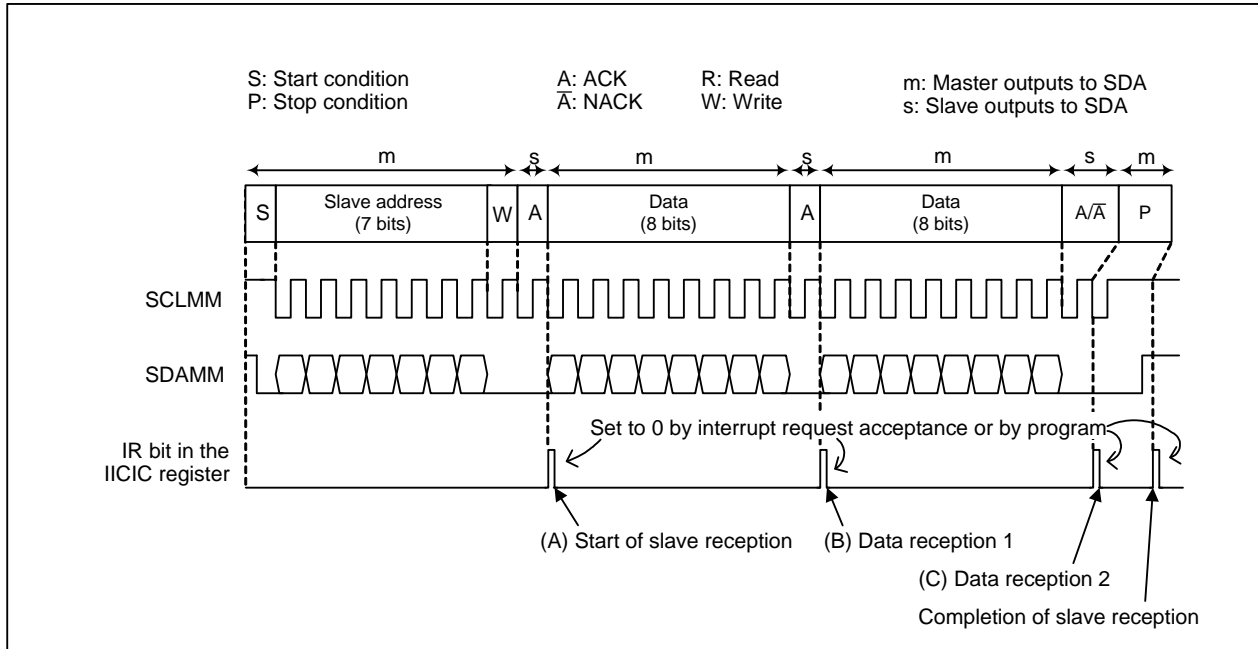
#### (D) Completion of master reception

- (In I<sup>2</sup>C-bus interrupt routine)
- (1) Read the received data from the S00 register
  - (2) Write C0h to the S10 register. (Stop condition standby state)
  - (3) Write dummy data to the S00 register (stop condition generated)



### 22.3.10.4 Slave Reception

The slave reception is described in this section. The initial settings described in 22.3.10.1 "Initial Settings" are assumed to be completed. Figure 22.19 shows the example of slave reception. The following programs (A) to (C) are executed at (A) to (C) in Figure 22.19, respectively.



**Figure 22.19 Example of Slave Reception**

(A) Slave receive is started.

(In I<sup>2</sup>C-bus interrupt routine)

- (1) Check the value of the S10 register. When the TRX bit is 0, the I<sup>2</sup>C interface is in slave receive mode.
- (2) Write dummy data to the S00 register.

(B) Data reception 1

(In I<sup>2</sup>C-bus interrupt routine)

- (1) Read the received data from the S00 register.
- (2) Set the ACKBIT bit in the S20 register to 0 (ACK presents) because the data is not the last one.
- (3) Write dummy data to the S00 register.

(C) Data reception 2

(In I<sup>2</sup>C-bus interrupt routine)

- (1) Read the received data from the S00 register.
- (2) Set the ACKBIT bit in the S20 register to 1 (no ACK presents) because the data is the last one.
- (3) Write dummy data to the S00 register.

### 22.3.10.5 Slave Transmission

Slave transmission is described in this section. The initial settings described in 22.3.10.1 "Initial Settings" are assumed to be completed. Figure 22.20 shows the example of slave transmission. The following programs (A) to (B) are executed at (A) and (B) in Figure 22.20, respectively.

When arbitration lost is detected, the TRX bit becomes 0 (receive mode) even when the bit after the slave address is 1 (read). Therefore, after arbitration lost is detected, read the S00 register. When the bit 0 in the S00 register is 1, write 4Fh (slave transmit mode) to the S10 register and execute slave transmission.

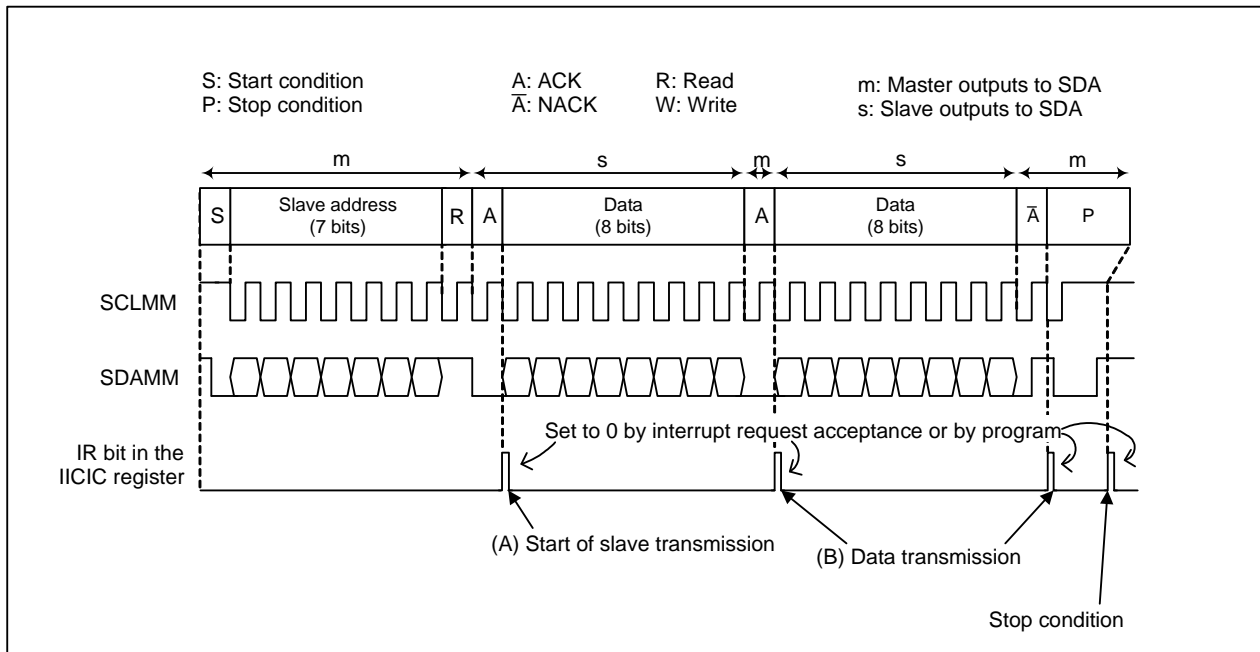


Figure 22.20 Example of Slave Transmission

#### (A) Start of slave transmission

(In I<sup>2</sup>C-bus interrupt routine)

- (1) Check the value of the S10 register. When the TRX bit is 1, the I<sup>2</sup>C interface is in slave transmit mode.
- (2) Write transmit data to the S00 register

#### (B) Data transmission

(In I<sup>2</sup>C-bus interrupt routine)

- (1) Write transmit data to the S00 register

Write dummy data to the S00 register even if an interrupt occurs at an ACK clock of the last transmit data. After writing to the S00 register, the SCLMM pin is released.

### 22.4 Interrupts

The I<sup>2</sup>C interface generates interrupt requests. Figure 22.21 shows I<sup>2</sup>C Interface Interrupts, and Table 22.15 lists I<sup>2</sup>C-bus Interrupts.

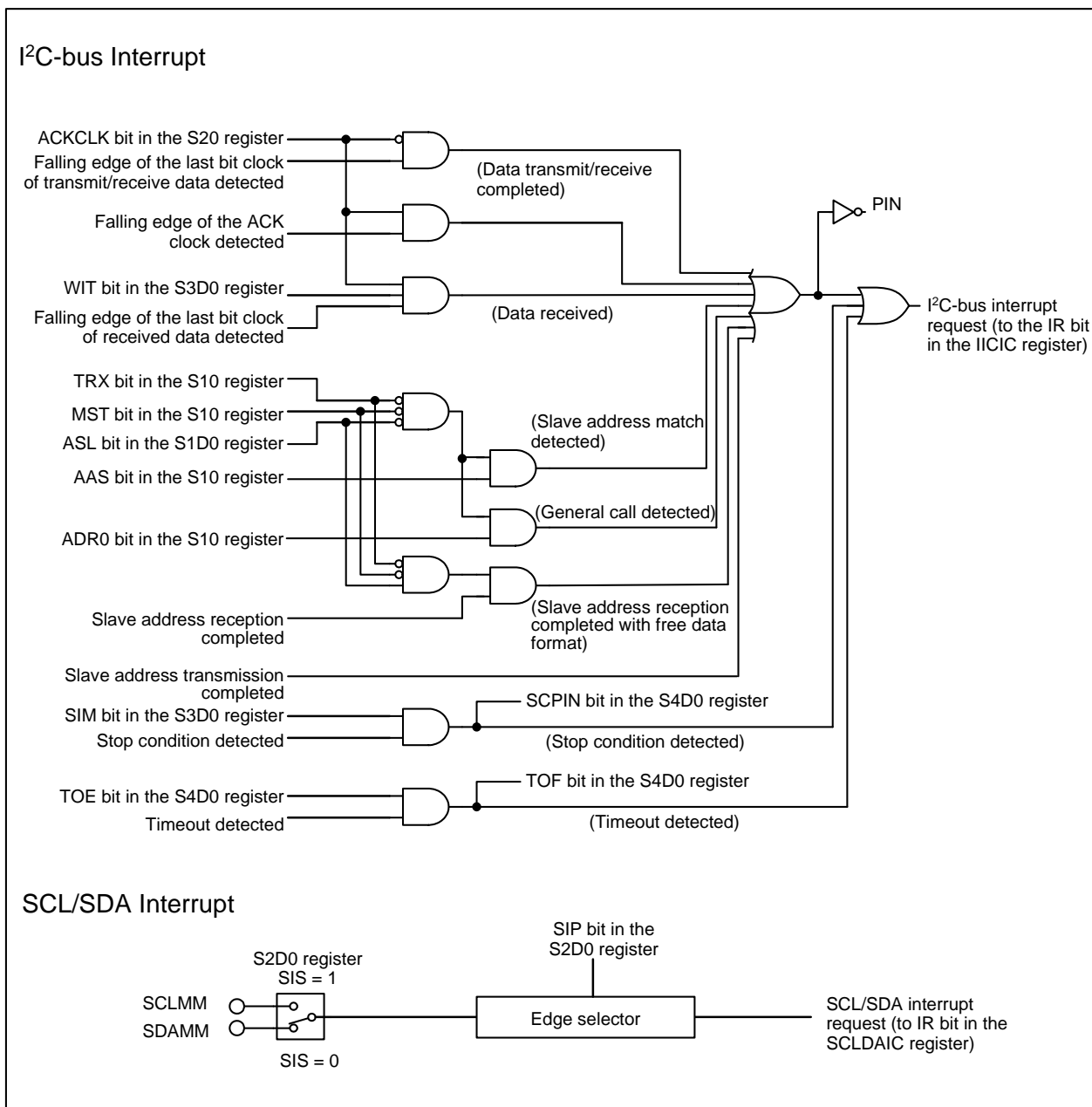


Figure 22.21 I<sup>2</sup>C Interface Interrupts

**Table 22.15 I<sup>2</sup>C-bus Interrupts**

Interrupt	Interrupt Source	Associated Bits (Register)		Interrupt Control Register	
		Interrupt enabled	Interrupt request		
I <sup>2</sup> C-bus Interrupt	Completion of data transmit/receive When the ACKCLK bit in the S20 register is 0: Detection of the falling edge of the last clock of transmit/receive data through the SCLMM pin When the ACKCLK bit is 1: Detection of the falling edge of ACK clock through the SCLMM pin	—	PIN (S10)	IICIC	
	Data reception (before ACK clock) Detection of the falling edge of the last clock of transmit/receive data through the SCLMM pin	WIT (S3D0)			
	Detection of slave address match Received slave address matches bits SAD6 to SAD0 in registers S0D0 to S0D2 in slave receive mode with addressing format (AAS bit in the S10 register = 1)	—			
	Detection of general call General call in slave receive mode with addressing format (ADR0 bit in the S10 register = 1)	—			
	Completion of receiving slave address in slave receive mode with free data format	—			
	Stop condition detected	SIM (S3D0)			SCPIN (S4D0)
	Timeout detected	TOE (S4D0)			TOF (S4D0)
	SCL/SDA interrupt	Detection of the falling edge or rising edge of input/output signal for the SCLMM or SDAMM pin			—

Refer to 12.7 "Interrupt Control". Table 22.16 lists Registers Associated with I<sup>2</sup>C Interface Interrupts.

**Table 22.16 Registers Associated with I<sup>2</sup>C Interface Interrupts**

Address	Register	Symbol	Reset Value
007Bh	I <sup>2</sup> C-bus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
0206h	Interrupt Source Select Register 2	IFSR2A	00h

When using the I<sup>2</sup>C-bus interface interrupt, set the IFSR22 bit in the IFSR2A register to 1 (I<sup>2</sup>C-bus interrupt). When using the SCL/SDA interrupt, set the IFSR23 bit in the IFSR2A register to 1 (SCL/SDA interrupt).

The SCL/SDA interrupt is enabled even in wait mode and stop mode.

The IR bit in the SCLDAIC register may become 1 (interrupt requested) when the ES0 bit in the S1D0 register, the SIP bit in the S2D0 register, or the SIS bit in the S2D0 register is changed. Therefore, follow the procedure below to change these bits. Refer to 12.13 "Notes on Interrupts".

- (1) Set bits ILVL2 to ILVL0 in the SCLDAIC register to 000b (interrupt disabled).
- (2) Set the ES0 bit in the S1D0 register and bits SIP and SIS in the S2D0 register.
- (3) Set the IR bit in the SCLDAIC register to 0 (no interrupt request).

## 22.5 Notes on Multi-master I<sup>2</sup>C-bus Interface

### 22.5.1 Limitation on CPU Clock

When the CM07 bit in the CM0 register is 1 (CPU clock is a sub clock), do not access the registers listed in Table 22.4 "Registers". Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock) to access these registers.

### 22.5.2 Register Access

Refer to the notes below when accessing the I<sup>2</sup>C interface control registers. The period from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of an ACK clock is considered to be the transmission/reception period. When the ACKCLK bit is 0 (no ACK clock), the transmission/reception period is from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of the eighth clock.

#### 22.5.2.1 S00 Register

Do not write to the S00 register during transmission/reception.

#### 22.5.2.2 S1D0 Register

Do not change bits other than the IHR bit in the S1D0 register during transmission/reception.

#### 22.5.2.3 S20 Register

Do not change bits other than the ACKBIT bit in the S20 register during transmission/reception.

#### 22.5.2.4 S3D0 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use the MOV instruction to write to this register.
- Rewrite bits ICK1 and ICK0 when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).

#### 22.5.2.5 S4D0 Register

Rewrite bits ICK4 to ICK2 when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).

#### 22.5.2.6 S10 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use the MOV instruction to write to this register.
  - Do not write to the S10 register when bits MST and TRX change their values.
- Refer to operation examples in 22.3 "Operations" for bits MST and TRX change.

## 23. CAN Module

### Note

Do not use CAN function in the M16C/56 Group.

The M16C/5L Group implements one channel (referred to as CAN0) of the Controller Area Network (CAN) module that complies with the ISO11898-1 Specifications. The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier hereafter referred to as ID) and extended ID (29 bits).

Tables 23.1 and 23.2 list the CAN module specifications, and Figure 23.1 shows the CAN module block diagram.

Connect the CAN bus transceiver externally.

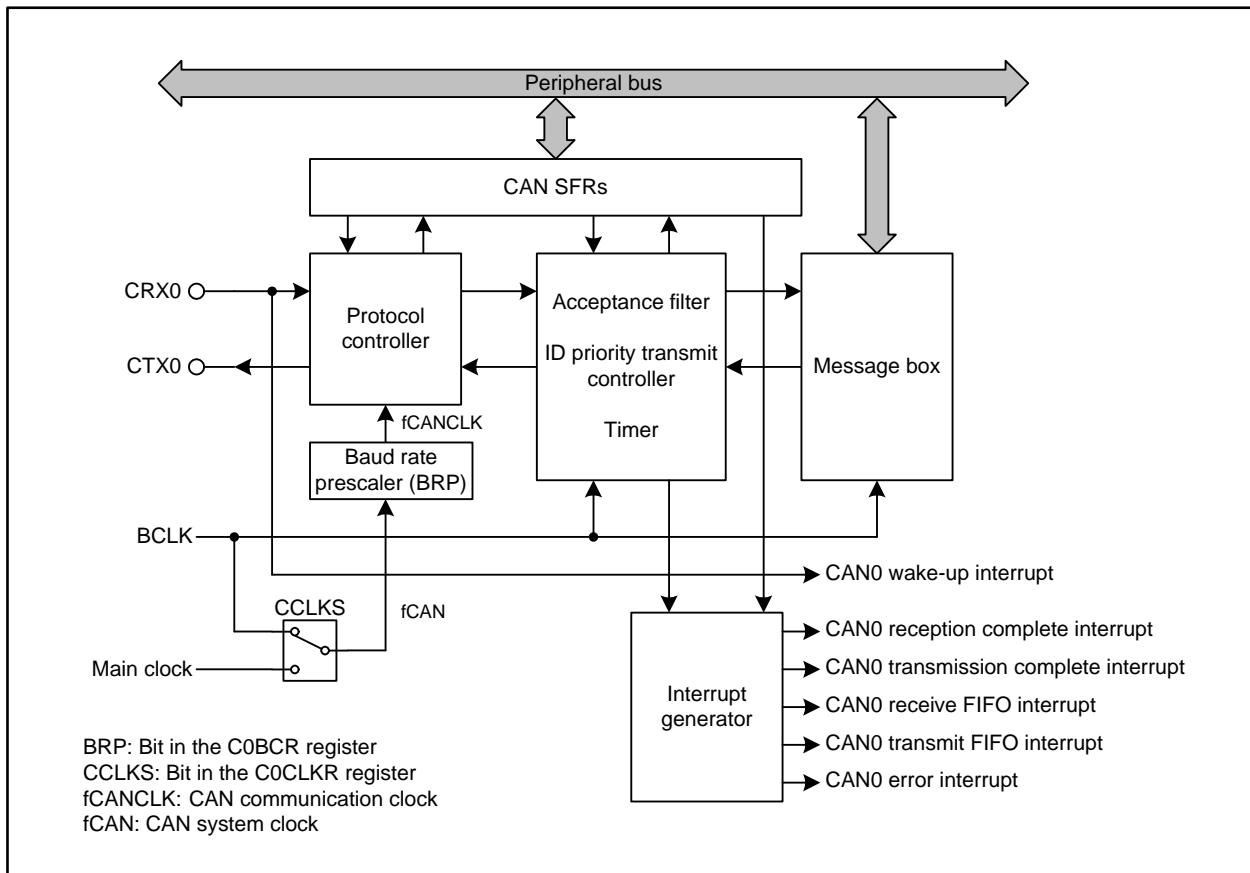
**Table 23.1 CAN Module Specifications (1)**

Item	Specification
Protocol	ISO11898-1 compliant
Bit rate	Up to 1 Mbps
Message boxes	32 mailboxes: Two selectable mailbox modes: • Normal mailbox mode All 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as 4-stage FIFO for transmission and 4-stage FIFO for reception.
Reception	<ul style="list-style-type: none"> <li>• Data frames and remote frames can be received.</li> <li>• Selectable receiving ID format (only standard ID, only extended ID, or both ID)</li> <li>• Programmable one-shot reception function</li> <li>• Selectable overwrite mode (message overwritten) or overrun mode (message discarded)</li> <li>• The reception complete interrupt can be individually enabled or disabled for each mailbox.</li> </ul>
Acceptance filtering	8 acceptance masks: one mask every 4 mailboxes The mask can be individually enabled or disabled for each mailbox.
Transmission	<ul style="list-style-type: none"> <li>• Data frame and remote frame can be transmitted.</li> <li>• Selectable transmitting ID format (only standard ID, only extended ID, or both ID).</li> <li>• Programmable one-shot transmission function</li> <li>• Selectable ID priority transmit mode or mailbox number priority transmit mode</li> <li>• Transmission request can be aborted. (The completion of abort can be confirmed with a flag.)</li> <li>• The transmission complete interrupt can be individually enabled or disabled for each mailbox.</li> </ul>
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state can be selected: <ul style="list-style-type: none"> <li>• ISO11898-1 compliant</li> <li>• Automatic entry to CAN halt mode at bus-off entry</li> <li>• Automatic entry to CAN halt mode at bus-off end</li> <li>• Entry to CAN halt mode by a program</li> <li>• Transition to the error-active state by a program</li> </ul>

**Table 23.2 CAN Module Specifications (2)**

Item	Specification
Error status monitoring	<ul style="list-style-type: none"> <li>• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored.</li> <li>• Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery).</li> <li>• The error counters can be read.</li> </ul>
Time stamp function	<p>Time stamp function using a 16-bit counter</p> <p>The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.</p>
Interrupt sources	<p>6 types:</p> <ul style="list-style-type: none"> <li>• Reception complete</li> <li>• Transmission complete</li> <li>• Receive FIFO</li> <li>• Transmit FIFO</li> <li>• Error</li> <li>• Wake-up</li> </ul>
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.
Software support units	<p>3 software support units:</p> <ul style="list-style-type: none"> <li>• Acceptance filter support</li> <li>• Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search)</li> <li>• Channel search support</li> </ul>
CAN clock source	Selectable BCLK or main clock
Test mode	<p>3 test modes available for user evaluation:</p> <ul style="list-style-type: none"> <li>• Listen-only mode</li> <li>• Self-test mode 0 (external loop back)</li> <li>• Self-test mode 1 (internal loop back)</li> </ul>





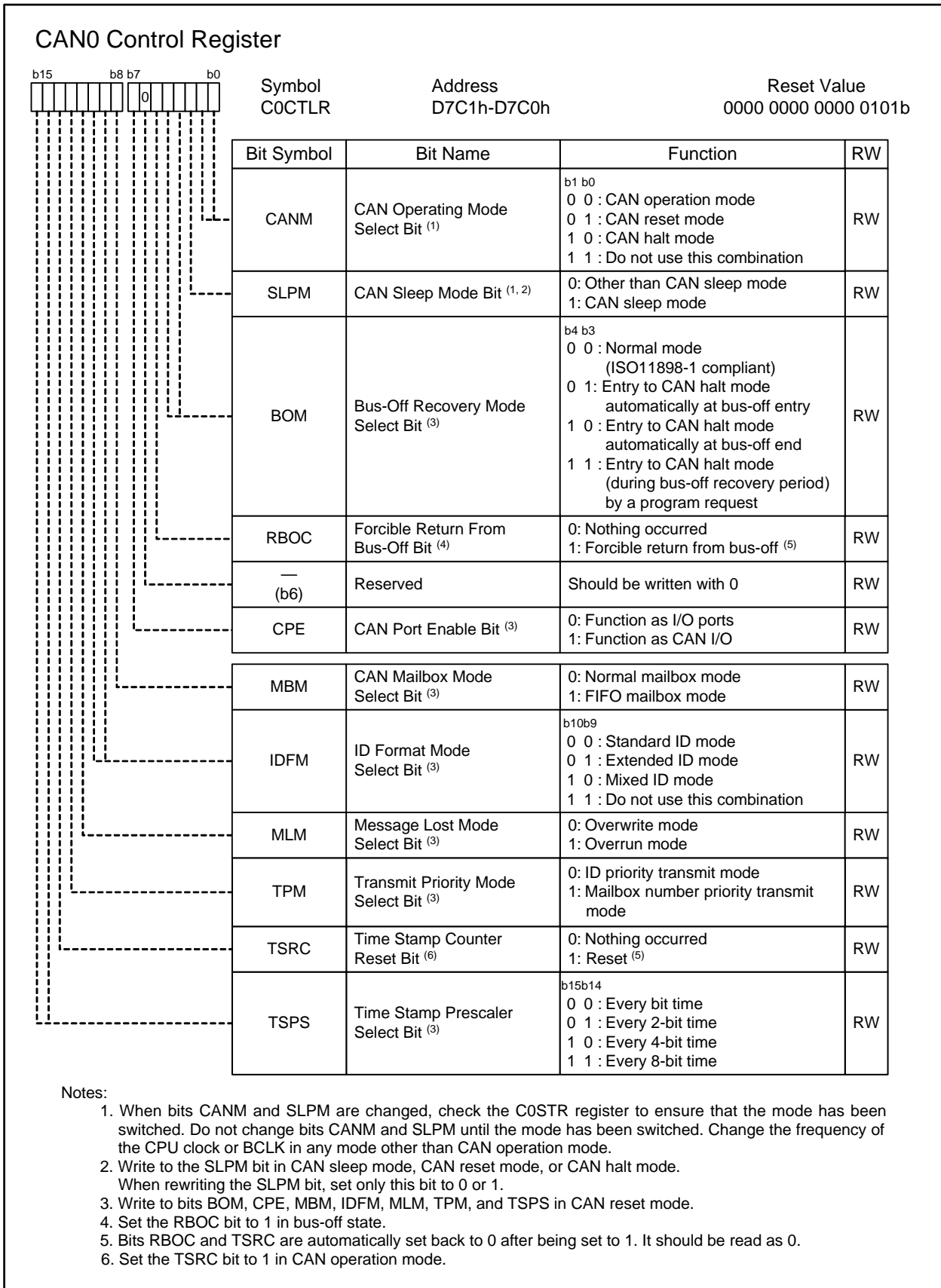
**Figure 23.1 CAN Module Block Diagram**

- CRX0/CTX0: CAN input/output pins
- Protocol controller: Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box: Consists of 32 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter: Performs filtering of received messages. Registers C0MKR0 to C0MKR7 are used for the filtering process.
- Timer: Used for the time stamp function. The timer value when storing a message into the mailbox is written as the time stamp value.
- Wake-up function: Generates a CAN0 wake-up interrupt request when a message is detected on the CAN bus.
- Interrupt generator: Generates the following five types of interrupts:
  - CAN0 reception complete interrupt
  - CAN0 transmission complete interrupt
  - CAN0 receive FIFO interrupt
  - CAN0 transmit FIFO interrupt
  - CAN0 error interrupt
- CAN SFRs: CAN-associated registers. Refer to 23.1 "CAN SFRs" for details.

### 23.1 CAN SFRs

The CAN-associated registers are shown in Figures 23.2 to 23.11, 23.13, 23.14, 23.16 to 23.20, 23.22, and 23.24 to 23.30.

### 23.1.1 CAN0 Control Register (C0CTLR)



**Figure 23.2 C0CTLR Register**

### 23.1.1.1 CANM Bit

The CANM bit selects one of the following modes for the CAN module: CAN operation mode, CAN reset mode, or CAN halt mode. Refer to 23.2 “Operating Mode” for details.

CAN sleep mode is set by the SLPM bit.

Do not set the CANM bit to 11b.

When the CAN module enters CAN halt mode according to the setting of the BOM bit, the CANM bit is automatically set to 10b.

### 23.1.1.2 SLPM Bit

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode.

When this bit is set to 0, the CAN module exits CAN sleep mode.

Refer to 23.2 “Operating Mode” for details.

### 23.1.1.3 BOM Bit

The BOM bit is used to select bus-off recovery mode.

When the BOM bit is 00b, the recovery from bus-off is compliant with ISO11898-1, i.e. the CAN module reenters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.

When the BOM bit is 01b, as soon as the CAN module reaches the bus-off state, the CANM bit in the C0CTLR register is set to 10b (CAN halt mode) and the CAN module enters CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off and registers C0TECR and C0RECR are set to 00h.

When the BOM bit is 10b, the CANM bit is set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off and registers C0TECR and C0RECR are set to 00h.

When the BOM bit is 11b, the CAN module enters CAN halt mode by setting the CANM bit to 10b while the CAN module is still in bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and registers C0TECR and C0RECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM bit is set to 10b, a bus-off recovery interrupt request is generated.

If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM bit is 01b, or at bus-off end when the BOM bit is 10b), then the CPU request to enter CAN reset mode has higher priority.

### 23.1.1.4 RBOC Bit

When the RBOC bit is set to 1 (force return from bus-off) in bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active.

When the RBOC bit is set to 1, registers C0RECR and C0TECR are set to 00h and the BOST bit in the C0STR register is set to 0 (the CAN module is not in bus-off state). The other registers remain unchanged. No bus-off recovery interrupt request is generated by this recovery from the bus-off state. Use the RBOC bit only when the BOM bit is 00b (normal mode).

### 23.1.1.5 CPE Bit

When the CPE bit is set to 1, the function of the CAN I/O pins (CRX0 and CTR0) is enabled. To use the CAN module, set this bit to 1.

To set the CPE bit to 1, set the port direction bit corresponding to the CRX0 pin to 0.

When the CPE bit is set to 0, the function of the port I/O pins is enabled.

Write to the CPE bit only in CAN reset mode.

To use a CAN wake-up interrupt, set the CPE bit to 1.

### 23.1.1.6 MBM Bit

When the MBM bit is 0 (normal mailbox mode), mailboxes [0] to [31] are configured as transmit or receive mailboxes.

When this bit is 1 (FIFO mailbox mode), mailboxes [0] to [23] are configured as transmit or receive mailboxes. Mailboxes [24] to [27] are configured as a transmit FIFO and mailboxes [28] to [31] as a receive FIFO.

Transmit data is written into mailbox [24] (mailbox [24] is a window mailbox for the transmit FIFO).

Receive data is read from mailbox [28] (mailbox [28] is a window mailbox for the receive FIFO).

Table 23.3 lists the mailbox configuration.

**Table 23.3 Mailbox Configuration**

Mailbox	MBM = 0 (Normal Mailbox Mode)	MBM = 1 (1) (FIFO Mailbox Mode)
Mailboxes [0] to [23]	Normal mailbox	Normal mailbox
Mailboxes [24] to [27]		Transmit FIFO
Mailboxes [28] to [31]		Receive FIFO

Note:

- When the MBM bit is set to 1, note the following:
  - Transmit FIFO is controlled by the C0TFCR register.  
The C0MCTLj register (j = 0 to 31) for mailboxes [24] to [27] is disabled.  
Registers C0MCTL24 to C0MCTL27 cannot be used.
  - Receive FIFO is controlled by the C0RFCR register.  
The C0MCTLj register for mailboxes [28] to [31] is disabled.  
Registers C0MCTL28 to C0MCTL31 cannot be used.
  - Refer to the C0MIER register about the FIFO interrupts.
  - The corresponding bits in the C0MKIVLR register for mailboxes [24] to [31] are disabled. Set 0 to these bits.
  - Transmit/receive FIFOs can be used for both data frames and remote frames.

### 23.1.1.7 IDFM Bit

The IDFM bit specifies the ID format.

When this bit is 00b, all mailboxes (including FIFO mailboxes) handle only standard IDs.

When this bit is 01b, all mailboxes (including FIFO mailboxes) handle only extended IDs.

When this bit is 10b, all mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mailbox mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [23], the IDE bit in registers C0FIDCR0 and C0FIDCR1 is used for the receive FIFO, and the IDE bit in mailbox [24] is used for the transmit FIFO.

Do not set 11b to the IDFM bit.

### 23.1.1.8 MLM Bit

The MLM bit specifies the operation when a new message is captured in the unread mailbox. Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode.

When the MLM bit is 0, all mailboxes are set to overwrite mode and the new message is overwriting the old message.

When this bit is 1, all mailboxes are set to overrun mode and the new message is discarded.

### 23.1.1.9 TPM Bit

The TPM bit specifies the priority of modes when transmitting messages. ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO 11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [31] (in normal mailbox mode), and mailboxes [0] to [23] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [23]).

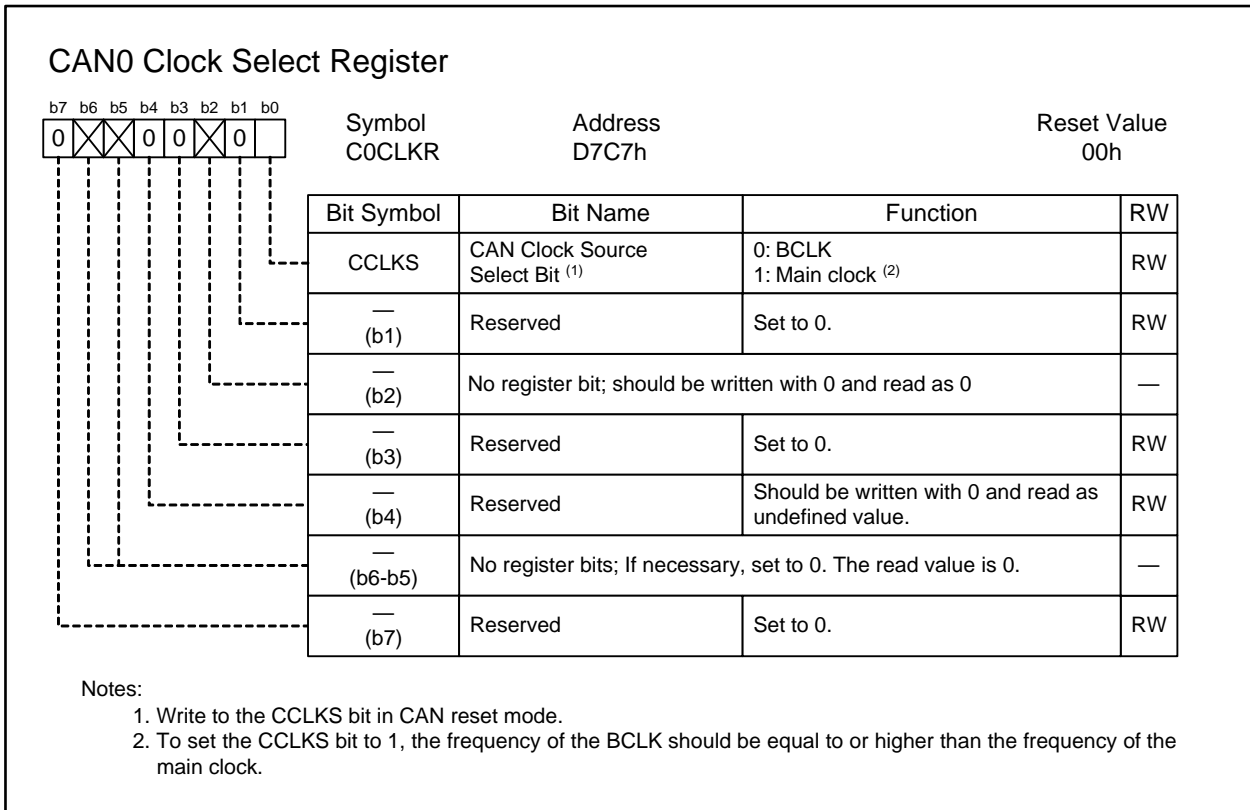
### 23.1.1.10 TSRC Bit

The TSRC bit is used to reset the time stamp counter.  
When this bit is set to 1, the C0TSR register is set to 0000h. It is automatically set to 0.

### 23.1.1.11 TSPS Bit

The TSPS bit selects the prescaler for the time stamp.  
The reference clock for the time stamp can be selected from 1-, 2-, 4- or 8-bit time periods.

### 23.1.2 CAN0 Clock Select Register (C0CLKR)



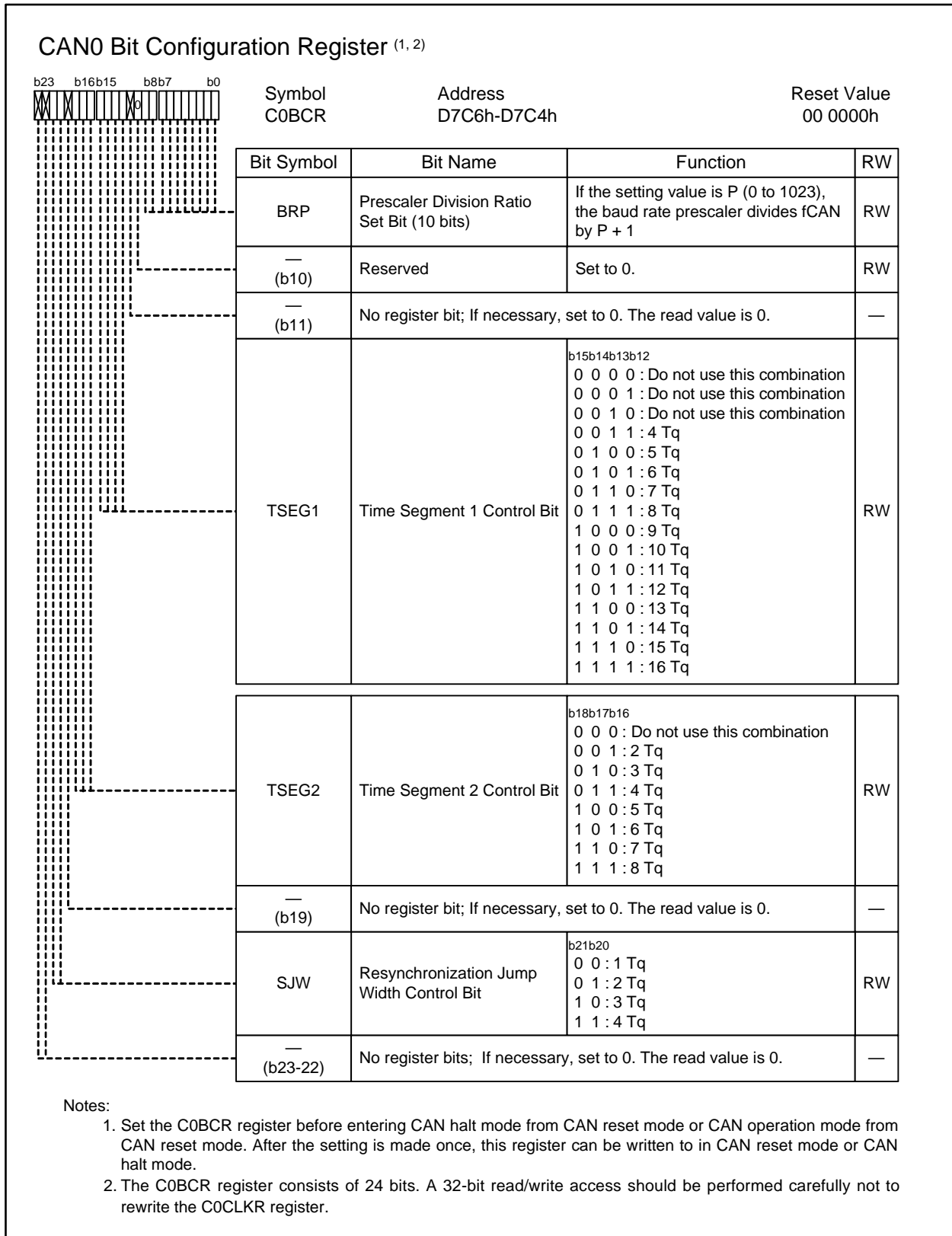
**Figure 23.3 C0CLKR Register**

#### 23.1.2.1 CCLKS Bit

When the CCLKS bit is set to 0, the CAN clock source (fCAN) originates from the PLL.

When this bit is set to 1, fCAN originates directly from the external XIN pin bypassing the PLL.

### 23.1.3 CAN0 Bit Configuration Register (C0BCR)



**Figure 23.4 C0BCR Register**

Refer to 23.3 “CAN Communication Speed Configuration” about the bit timing configuration.



### 23.1.3.1 BRP Bit

The BRP bit is used to set the frequency of the CAN communication clock (fCANCLK).  
The cycle of fCANCLK is set to be 1 Time Quantum (Tq).

### 23.1.3.2 TSEG1 Bit

The TSEG1 bit is used to specify the total length of the propagation time segment (PROP\_SEG) and phase buffer segment 1 (PHASE\_SEG1) with the value of Tq.  
A value from 4 to 16 time quanta can be set.

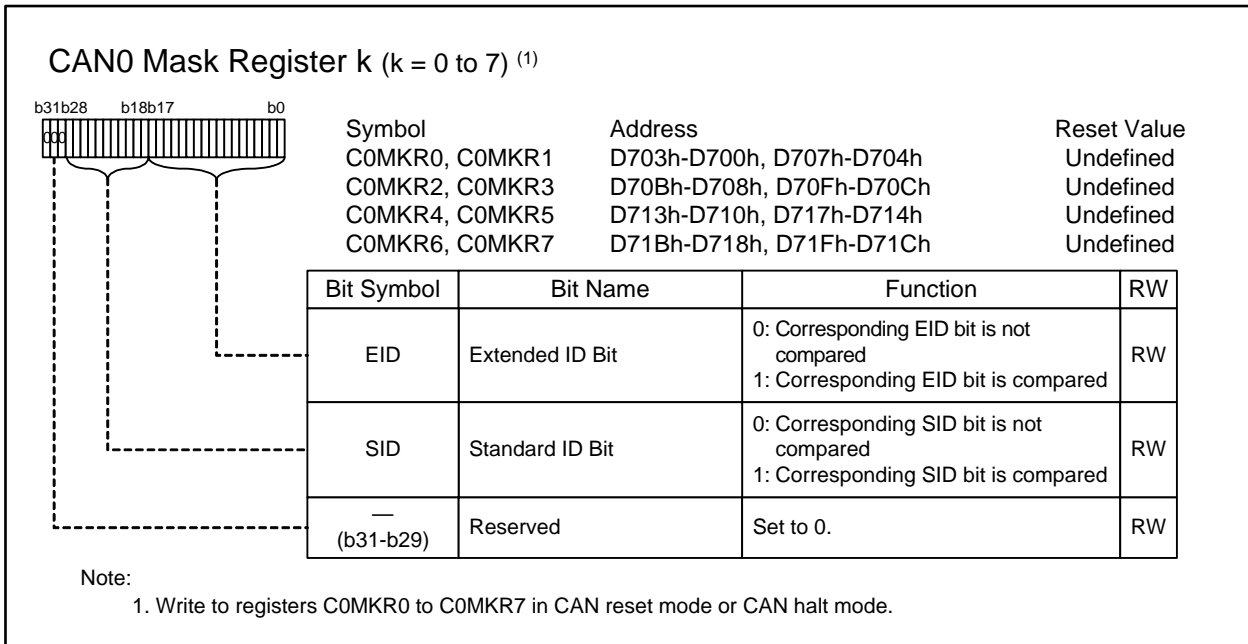
### 23.1.3.3 TSEG2 Bit

The TSEG2 bit is used to specify the length of phase buffer segment TSEG2 (PHASE\_SEG2) with the value of Tq.  
A value from 2 to 8 time quanta can be set.  
Set the value smaller than that of the TSEG1 bit.

### 23.1.3.4 SJW Bit

The SJW bit is used to specify the resynchronization jump width with the value of Tq.  
A value from 1 to 4 time quanta can be set.  
Set the value smaller than or equal to that of the TSEG2 bit.

### 23.1.4 CAN0 Mask Register k (COMKRk) (k = 0 to 7)



**Figure 23.5 Registers C0MKR0 to C0MKR7**

Refer to 23.5 “Acceptance Filtering and Masking Function” about the masking function in FIFO mailbox mode.

#### 23.1.4.1 EID Bit

The EID bit is the filter mask bit corresponding to the CAN extended ID bit. This bit is used to receive extended ID messages.

When the EID bit is 0, the corresponding EID bit is not compared for the received ID and the mailbox ID.

When this bit is 1, the corresponding EID bit is compared for the received ID and the mailbox ID.

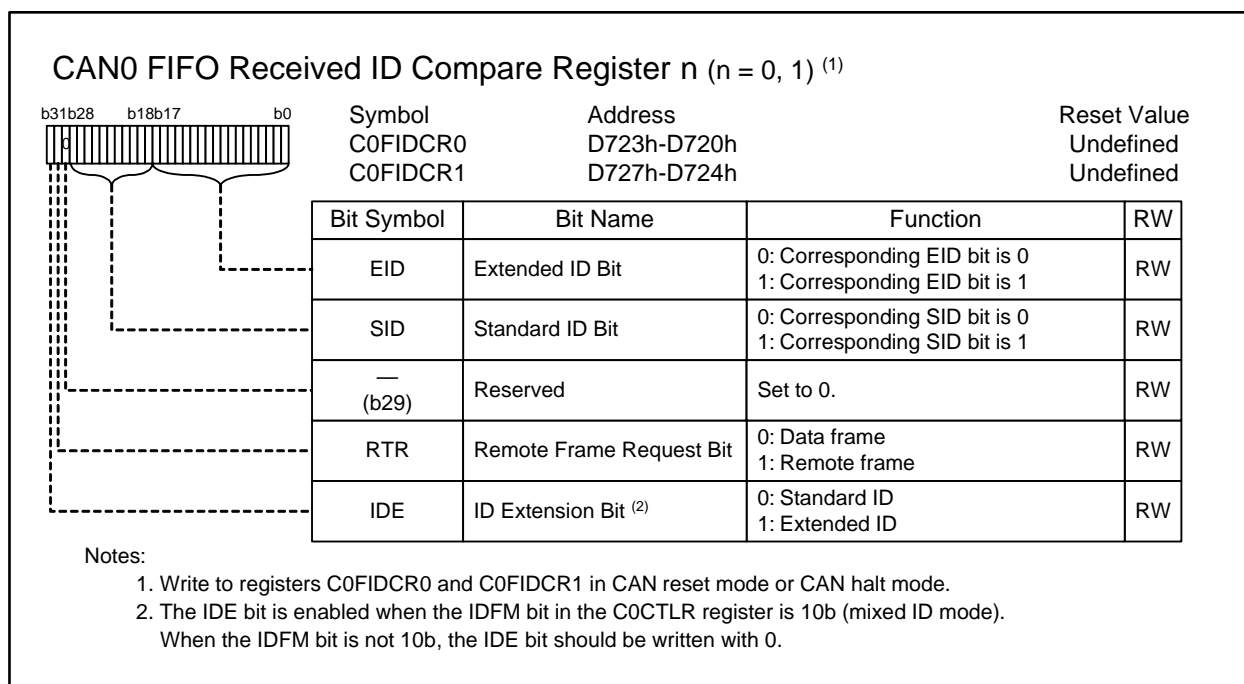
#### 23.1.4.2 SID Bit

The SID bit is the filter mask bit corresponding to the CAN standard ID bit. This bit is used to receive both standard ID and extended ID messages.

When the SID bit is 0, the corresponding SID bit is not compared for the received ID and the mailbox ID.

When this bit is 1, the corresponding SID bit is compared for the received ID and the mailbox ID.

### 23.1.5 CAN0 FIFO Received ID Compare Register n (C0FIDCR0 to C0FIDCR1) (n = 0, 1)



**Figure 23.6 Registers C0FIDCR0 to C0FIDCR1**

Registers C0FIDCR0 and C0FIDCR1 are enabled when the MBM bit in the C0CTLR register is set to 1 (FIFO mailbox mode). Bits EID, SID, RTR, and IDE in registers C0MB28 to C0MB31 are disabled. Refer to 23.5 “Acceptance Filtering and Masking Function” about the usage of these registers.

#### 23.1.5.1 EID Bit

The EID bit sets the extended ID of data frames and remote frames. This bit is used to receive extended ID messages.

#### 23.1.5.2 SID Bit

The SID bit sets the standard ID of data frames and remote frames. This bit is used to receive both standard ID and extended ID messages.

### 23.1.5.3 RTR Bit

The RTR bit sets the specified frame format of data frames or remote frames.

This bit specifies the following operation:

- When both RTR bits in registers C0FIDCR0 and C0FIDCR1 are set to 0, only data frames can be received.
- When both RTR bits in registers C0FIDCR0 and C0FIDCR1 are set to 1, only remote frames can be received.
- When the RTR bits in registers C0FIDCR0 and C0FIDCR1 are set to 0 or 1 individually, both data frames and remote frames can be received.

### 23.1.5.4 IDE bit

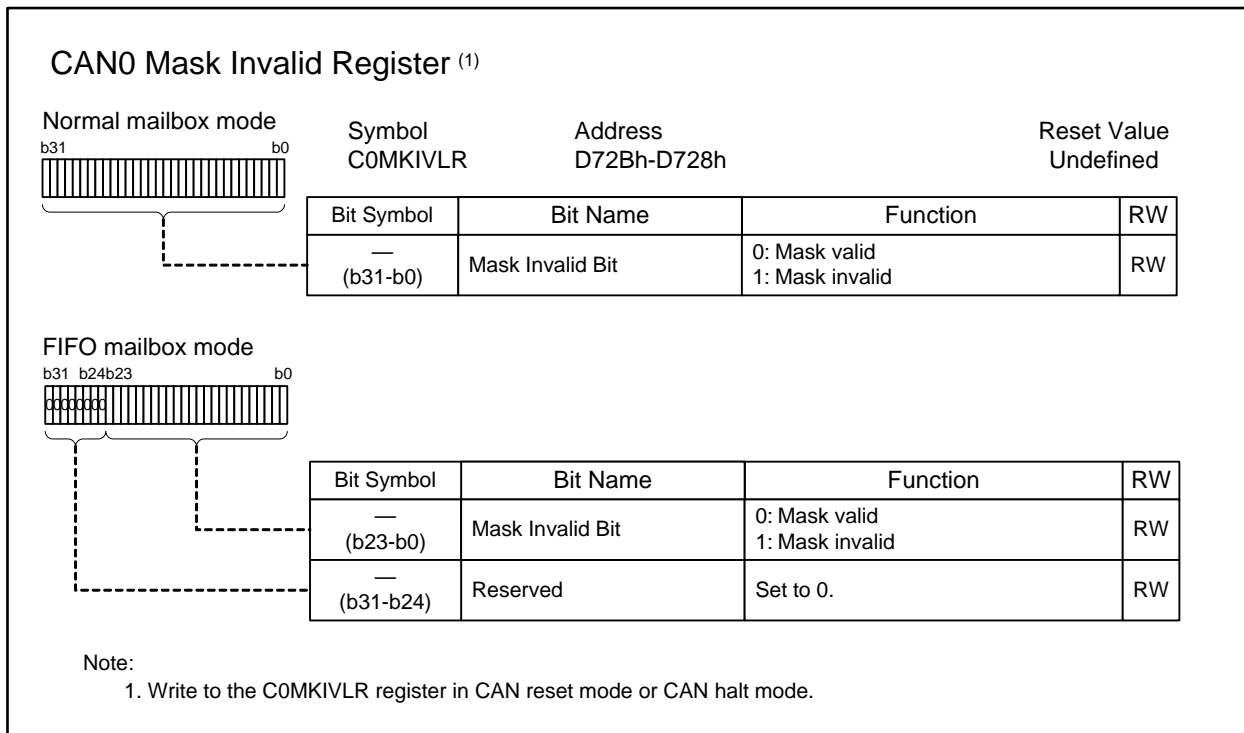
The IDE bit sets the ID format of standard ID or extended ID.

This bit is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode).

When the IDFM bit is 10b, the IDE bit specifies the following operation:

- When both IDE bits in registers C0FIDCR0 and C0FIDCR1 are set to 0, only standard ID frames can be received.
- When both IDE bits in registers C0FIDCR0 and C0FIDCR1 are set to 1, only extended ID frames can be received.
- When the IDE bits in registers C0FIDCR0 and C0FIDCR1 are set to 0 or 1 individually, both standard ID and extended ID frames can be received.

### 23.1.6 CAN0 Mask Invalid Register (C0MKIVLR)



**Figure 23.7 C0MKIVLR Register**

Each bit corresponds to the mailbox with the same number. When each bit is 1, the acceptance mask for the mailbox corresponding to the bit number is disabled. In this case, a receiving message is stored into the mailbox only if its ID matches bits SID and EID in the C0MBj register (j = 0 to 31).

### 23.1.7 CAN0 Mailbox Register j (C0MBj) (j = 0 to 31)

Table 23.4 lists the CAN0 mailbox memory mapping, and Table 23.5 lists the CAN data frame structure. The value after reset of CAN0 mailbox is undefined.

**Table 23.4 CAN0 Mailbox Memory Mapping**

Address	Message Content
CAN0	Memory Mapping
D500h + j * 16 + 0	EID7 to EID0
D500h + j * 16 + 1	EID15 to EID8
D500h + j * 16 + 2	SID5 to SID0, EID17, EID16
D500h + j * 16 + 3	IDE, RTR, SID10 to SID6
D500h + j * 16 + 4	—
D500h + j * 16 + 5	Data length code (DLC)
D500h + j * 16 + 6	Data byte 0
D500h + j * 16 + 7	Data byte 1
⋮	⋮
⋮	⋮
⋮	⋮
D500h + j * 16 + 13	Data byte 7
D500h + j * 16 + 14	Time stamp lower byte
D500h + j * 16 + 15	Time stamp upper byte

j: Mailbox number (j = 0 to 31)

**Table 23.5 CAN Data Frame Structure**

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	.....	DATA7
------------------	-----------------	-------------------	------------------	-----------------	-----------------	-------	-------	-------	-------

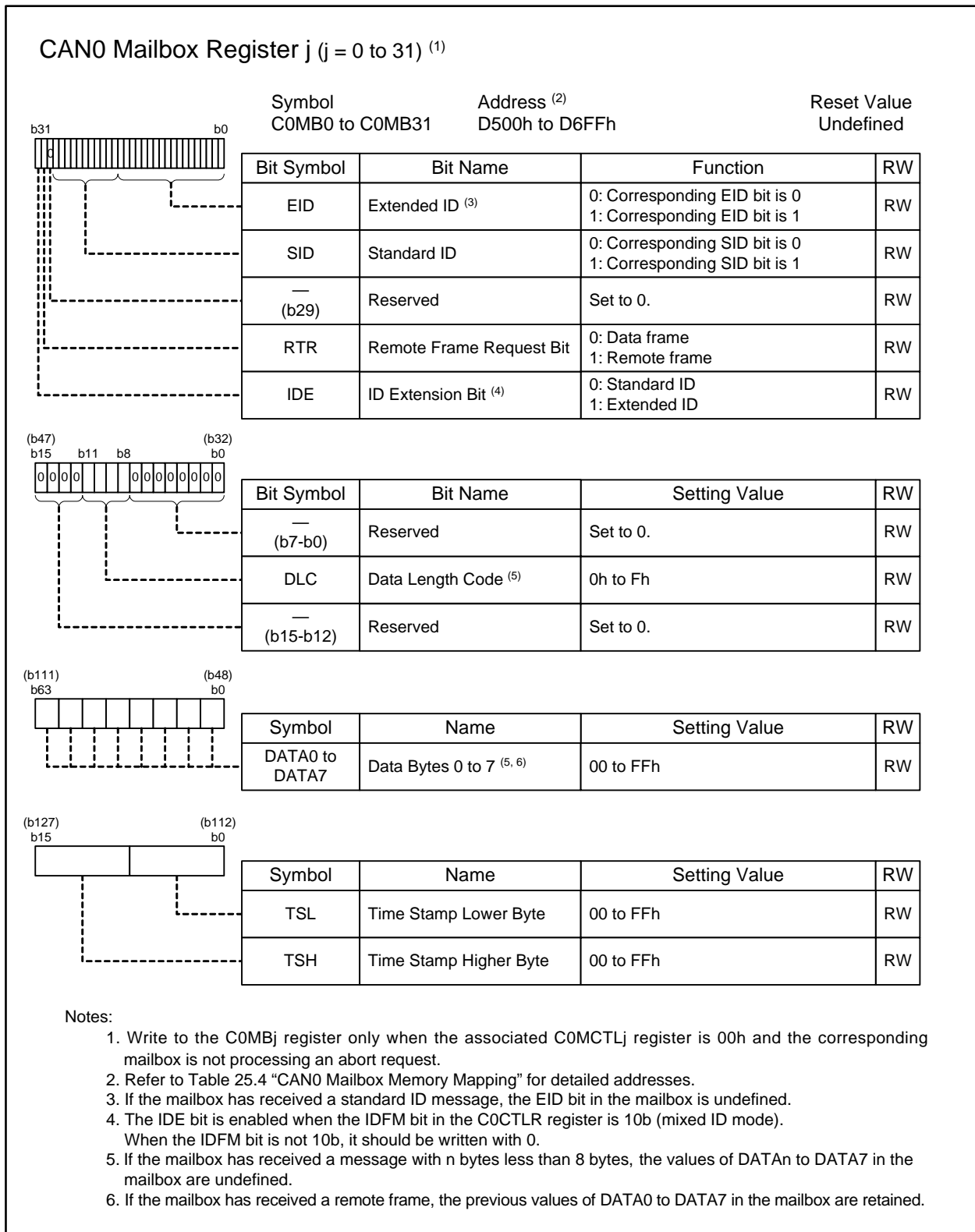


Figure 23.8 C0MBj Register

The previous value of each mailbox is retained unless a new message is received.

#### 23.1.7.1 EID Bit

The EID bit sets the extended ID of data frames and remote frames. This bit is used to transmit or receive extended ID messages.

#### 23.1.7.2 SID Bit

The SID bit sets the standard ID of data frames and remote frames. This bit is used to transmit or receive both standard ID and extended ID messages.

#### 23.1.7.3 RTR Bit

The RTR bit sets the frame format of data frames or remote frames.

This bit specifies the following operation:

- Receive mailbox receives only frames with the format specified by the RTR bit.
- Transmit mailbox transmits according to the frame format specified by the RTR bit.
- Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in registers C0FIDCR0 and C0FIDCR1.
- Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmitting message.

#### 23.1.7.4 IDE Bit

The IDE bit sets the ID format of standard IDs or extended IDs.

This bit is enabled when the IDFM bit in the C0CTRL register is 10b (mixed ID mode).

When the IDFM bit is 10b, the IDE bit specifies the following operation:

- Receive mailbox receives only the ID format specified by the IDE bit.
- Transmit mailbox transmits according to the ID format specified by the IDE bit.
- Receive FIFO mailbox receives messages with the standard ID, extended ID, or both IDs specified by the IDE bit in registers C0FIDCR0 and C0FIDCR1.
- Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmitting message.



### 23.1.7.5 DLC (Data Length Code)

The DLC is used to set the number of data bytes to be transmitted in a data frame. When data is requested using a remote frame, the number of data bytes to be requested is set.

When a data frame is received, the number of received data bytes is stored. When a remote frame is received, the number of requested data bytes is stored.

Table 23.6 lists the data length corresponding DLC.

**Table 23.6 Data Length Corresponding DLC**

DLC[3]	DLC[2]	DLC[1]	DLC[0]	Data Length
0	0	0	0	0 byte
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	-	-	-	8 bytes

-: Any value

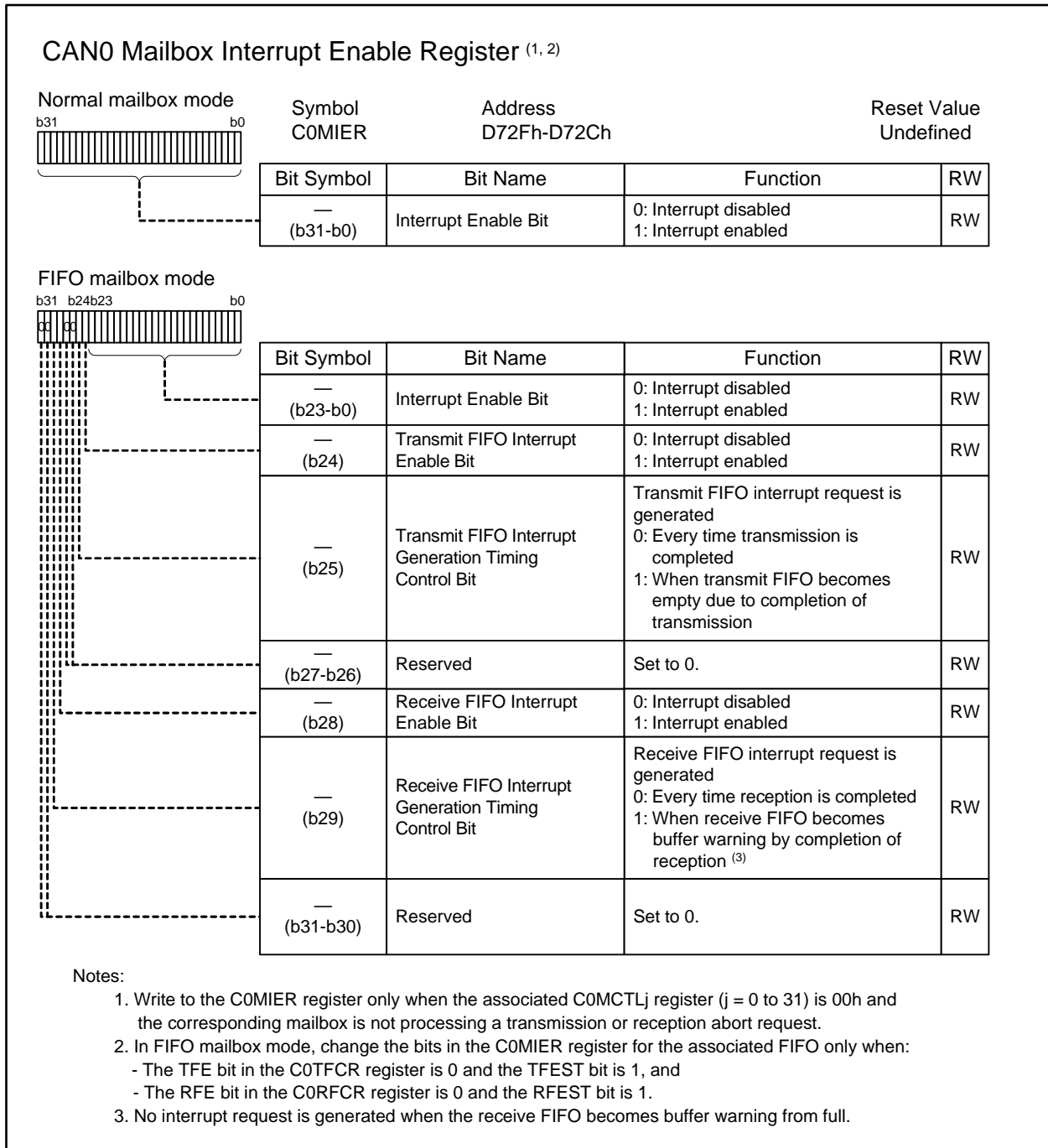
### 23.1.7.6 DATA0 to DATA7

DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.

### 23.1.7.7 TSL and TSH

TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.

### 23.1.8 CAN0 Mailbox Interrupt Enable Register (COMIER)



**Figure 23.9 COMIER Register**

Interrupts can be enabled individually for each mailbox.

In normal mailbox mode (bits 0 to 31) and in FIFO mailbox mode (bits 0 to 23), each bit corresponds to the mailbox with the same number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.

In FIFO mailbox mode, bits 24, 25, 28, and 29 specify whether transmit/receive FIFO interrupts are enabled/disabled and timing when interrupt requests are generated.

“Buffer warning” indicates a state in which the third unread message is stored in the receive FIFO.

### 23.1.9 CAN0 Message Control Register (C0MCTLj) (j = 0 to 31)

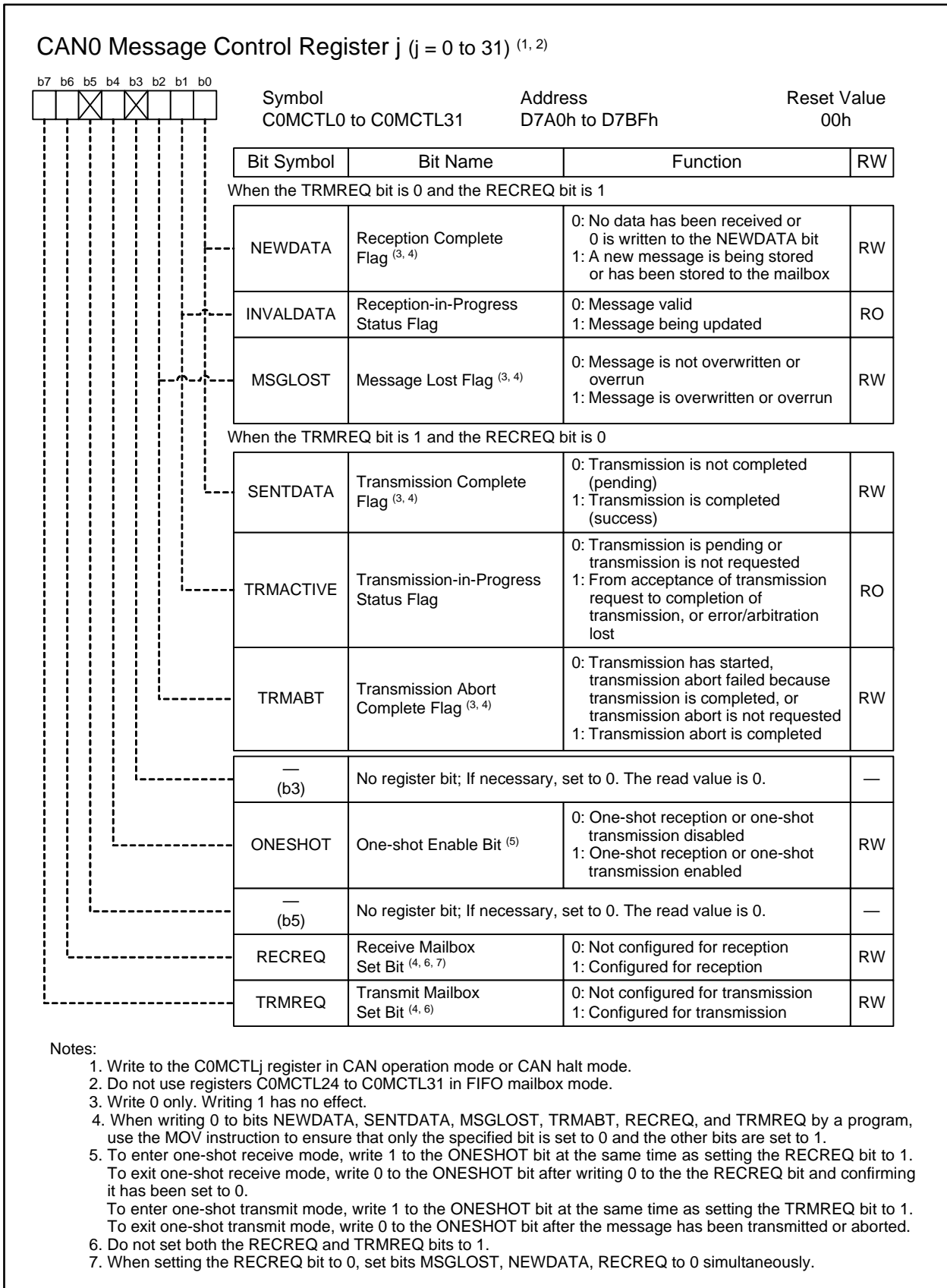


Figure 23.10 C0MCTLj Register

### 23.1.9.1 NEWDATA Bit

The NEWDATA bit is set to 1 when a new message is being stored or has been stored to the mailbox. The timing for setting this bit to 1 is simultaneous with the INVALIDDATA bit.

The NEWDATA bit is set to 0 by writing 0 by a program.

This bit cannot be set to 0 by writing 0 by a program while the related INVALIDDATA bit is 1.

### 23.1.9.2 SENTDATA Bit

The SENTDATA bit is set to 1 when data transmission from the corresponding mailbox is completed.

This bit is set to 0 by writing 0 by a program.

To set the SENTDATA bit to 0, first set the TRMREQ bit to 0.

Bits SENTDATA and TRMREQ cannot be set to 0 simultaneously.

To transmit a new message from the corresponding mailbox, set the SENTDATA bit to 0.

### 23.1.9.3 INVALIDDATA Bit

After the completion of a message reception, the INVALIDDATA bit is set to 1 while the received message is being updated into the corresponding mailbox.

This bit is set to 0 immediately after the message has been stored. If the mailbox is read while this bit is 1, the data is undefined.

### 23.1.9.4 TRMACTIVE Bit

The TRMACTIVE bit is set to 1 when the corresponding mailbox of the CAN module begins transmitting a message.

This bit is set to 0 when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed.

### 23.1.9.5 MSGLOST Bit

The MSGLOST bit is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA bit is 1. The MSGLOST bit is set to 1 at the end of the sixth bit of EOF.

This bit is set to 0 by writing 0 by a program.

In both overwrite and overrun modes, this bit cannot be set to 0 by writing 0 by a program during five cycles of fCAN (CAN system clock) following the sixth bit of EOF.

### 23.1.9.6 TRMABT Bit

The TRMABT bit is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is completed before starting transmission.
- Following a transmission abort request, when the CAN module detects CAN bus arbitration lost or a CAN bus error.
- In one-shot transmission mode (RECREQ bit = 0, TRMREQ bit = 1, and ONESHOT bit = 1), when the CAN module detects CAN bus arbitration lost or a CAN bus error.

The TRMABT bit is not set to 1 when data transmission is completed. In this case, the SENTDATA bit is set to 1.

The TRMABT bit is set to 0 by writing 0 by a program.

### 23.1.9.7 ONESHOT Bit

The ONESHOT bit can be used in the following two ways, receive mode and transmit mode:

#### (1) One-Shot Receive Mode

When the ONESHOT bit is set to 1 in receive mode (RECREQ bit = 1 and TRMREQ bit = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of bits NEWDATA and INVALIDDATA is the same as in normal reception mode. In one-shot receive mode, the MSGLOST bit is not set to 1. To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it has been set to 0.

#### (2) One-Shot Transmit Mode

When the ONESHOT bit is set to 1 in transmit mode (RECREQ bit = 0 and TRMREQ bit = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration lost occurs. When transmission is completed, the SENTDATA bit is set to 1. If transmission is not completed due to a CAN bus error or CAN bus arbitration lost, the TRMABT bit is set to 1.

Set the ONESHOT bit to 0 after the SENTDATA or TRMABT bit is set to 1.

### 23.1.9.8 RECREQ Bit

The RECREQ bit selects receive modes shown in Table 23.11.

When the RECREQ bit is set to 1, the corresponding mailbox is configured for reception of a data frame or a remote frame.

When this bit is set to 0, the corresponding mailbox is not configured for reception of a data frame or a remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 by writing 0 by a program during the following period:

Hardware protection is started

- From the acceptance filter procedure (the beginning of the CRC field)

Hardware protection is released

- For the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs (i.e. a maximum period of hardware protection is from the beginning of the CRC field to the end of the seventh bit of EOF).
- For the other mailboxes, after the acceptance filter procedure.
- If no mailbox is specified to receive the message, after the acceptance filter procedure.

When setting the RECREQ bit to 1, do not set 1 to the TRMREQ bit.

To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to 0 before changing to reception.

### 23.1.9.9 TRMREQ Bit

The TRMREQ bit selects transmit modes shown in Table 23.11.

When this bit is set to 1, the corresponding mailbox is configured for transmission of a data frame or a remote frame.

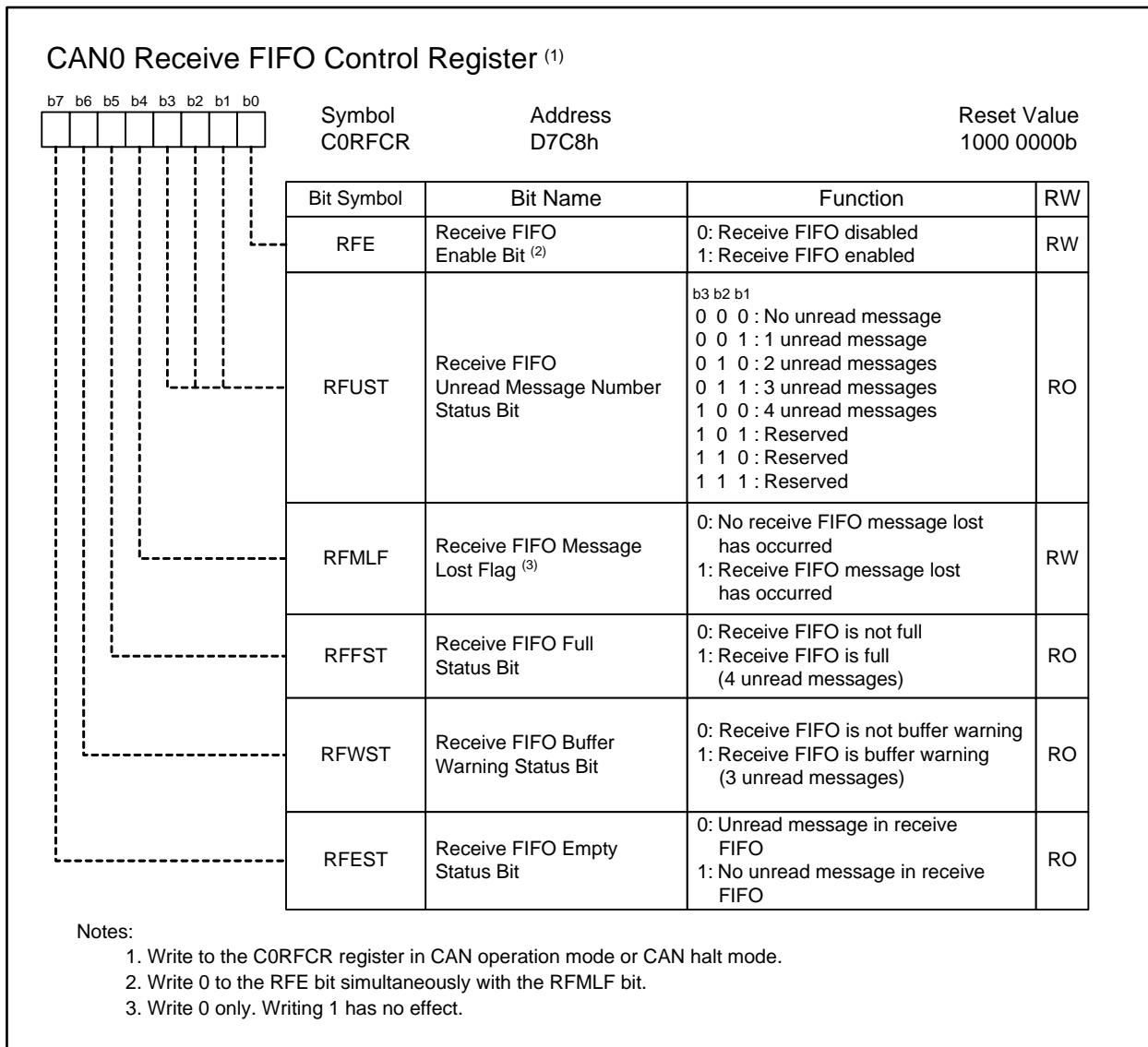
When this bit is set to 0, the corresponding mailbox is not configured for transmission of a data frame or a remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the corresponding transmission request, either the TRMABT or SENTDATA bit is set to 1.

When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1.

To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to 0 before changing to transmission.

### 23.1.10 CAN0 Receive FIFO Control Register (C0RFCR)



**Figure 23.11 C0RFCR Register**

### 23.1.10.1 RFE Bit

When the RFE bit is set to 1, the receive FIFO is enabled.

When this bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST bit = 1).

Do not set this bit to 1 in normal mailbox mode (MBM bit in the C0CTLR register = 0).

Due to hardware protection, the RFE bit is not set to 0 by writing 0 by a program during the following period:

Hardware protection is started

- From the acceptance filter procedure (the beginning of the CRC field)

Hardware protection is released

- If the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. (i.e. a maximum period of hardware protection is from the beginning of the CRC field to the end of the seventh bit of EOF.)
- If the receive FIFO is not specified to receive the message, after the acceptance filter procedure.

### 23.1.10.2 RFUST Bit

The RFUST bit indicates the number of unread messages in the receive FIFO.

The value of this bit is initialized to 000b when the RFE bit is set to 0.

### 23.1.10.3 RFMLF Bit

The RFMLF bit is set to 1 (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to 1 is at the end of the sixth bit of EOF.

The RFMLF bit is set to 0 by writing 0 by a program.

In both overwrite and overrun modes, this bit cannot be set to 0 (receive FIFO message lost has not occurred) by writing 0 by a program due to hardware protection during the five cycles of fCAN following the sixth bit of EOF, if the receive FIFO is full and determined to receive the message.

### 23.1.10.4 RFFST Bit

The RFFST bit is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. This bit is set to 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. This bit is set to 0 when the RFE bit is 0.

### 23.1.10.5 RFWST Bit

The RFWST bit is set to 1 (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. This bit is set to 0 (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. This bit is set to 0 when the RFE bit is 0.

### 23.1.10.6 RFEST Bit

The RFEST bit is 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. This bit is set to 1 when the RFE bit is set to 0. The RFEST bit is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 23.12 shows the receive FIFO mailbox operation.



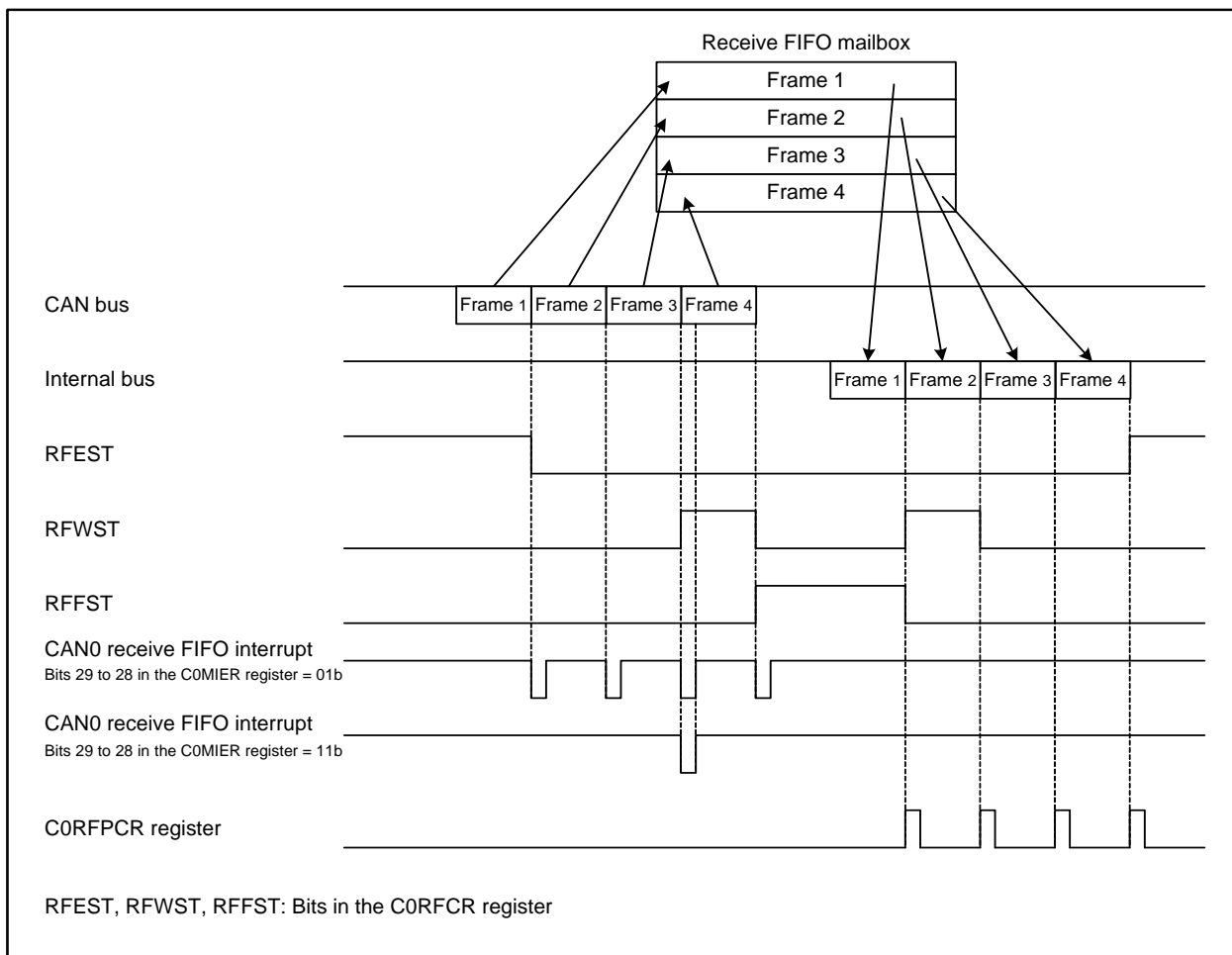
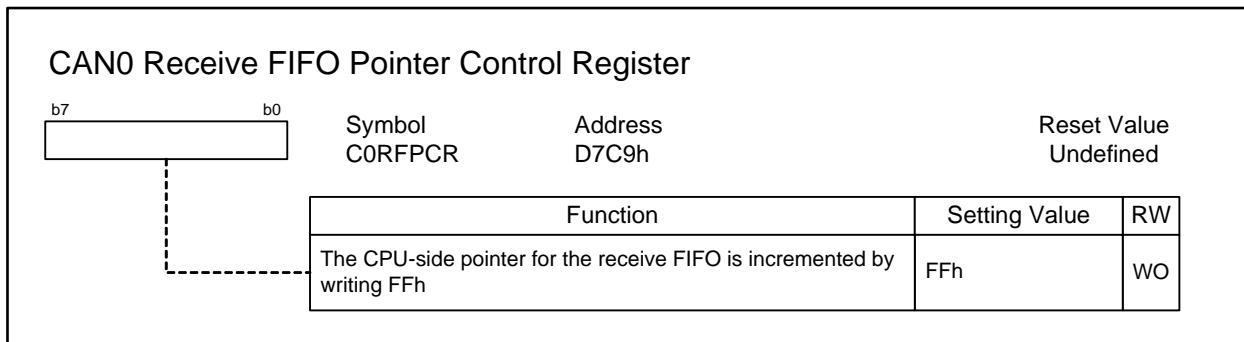


Figure 23.12 Receive FIFO Mailbox Operation (Bits 29 and 28 in C0MIER Register = 01b and 11b)

### 23.1.11 CAN0 Receive FIFO Pointer Control Register (C0RFPCR)



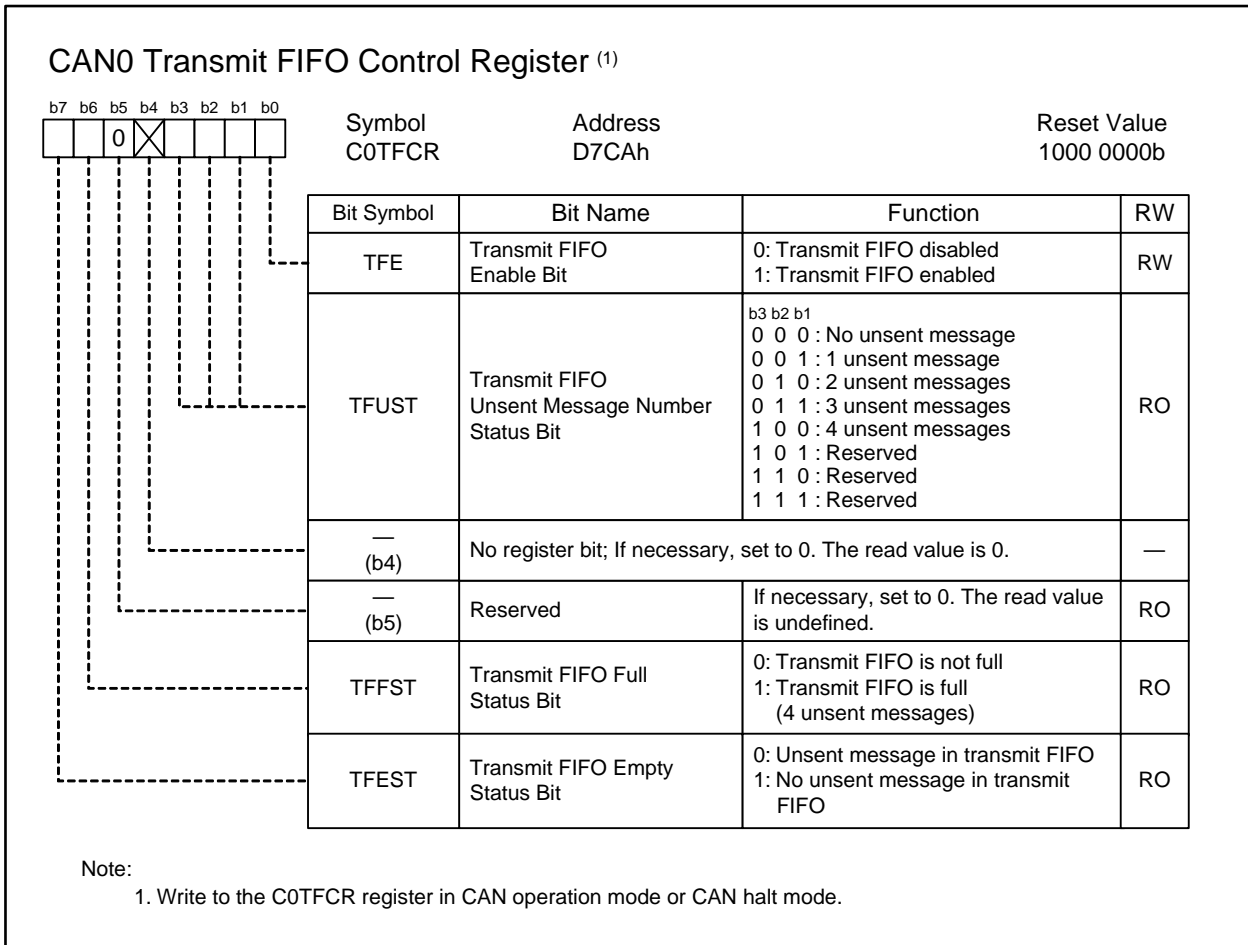
**Figure 23.13 C0RFPCR Register**

When the receive FIFO is not empty, write FFh to the C0RFPCR register by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.

Do not write to the C0RFPCR register when the RFE bit in the C0RFPCR register is 0 (receive FIFO disabled).

Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit is 1 (receive FIFO is full) in overwrite mode. When the RFMLF bit is 1 in this condition, the CPU-side pointer cannot be incremented by writing to the C0RFPCR register by a program.

### 23.1.12 CAN0 Transmit FIFO Control Register (C0TFCR)



**Figure 23.14 C0TFCR Register**

#### 23.1.12.1 TFE Bit

When the TFE bit is set to 1, the transmit FIFO is enabled.

When this bit is set to 0, the transmit FIFO becomes empty (TFEST bit = 1) and then unsent messages from the transmit FIFO are lost as described below:

- If a message from the transmit FIFO is not scheduled for the next transmission or during transmission.
- Following the completion of transmission, a CAN bus error, CAN bus arbitration lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission.

Before setting the TFE bit to set to 1 again, ensure that the TFEST bit has been set to 1.

After setting the TFE bit to 1, write transmit data into the COMB24 register.

Do not set this bit to 1 in normal mailbox mode (MBM bit in the C0CTRL register = 0).

#### 23.1.12.2 TFUST Bit

The TFUST bit indicates the number of unsent messages in the transmit FIFO.

After the TFE bit is set to 0, the value of the TFUST bit is initialized to 000b when transmission abort or transmission is completed.

### 23.1.12.3 TFFST Bit

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsend messages in the transmit FIFO is 4. This bit is set to 0 (transmit FIFO is not full) when the number of unsend messages in the transmit FIFO is less than 4. This bit is set to 0 when transmission from the transmit FIFO has been aborted.

### 23.1.12.4 TFEST Bit

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsend messages in the transmit FIFO is 0. This bit is set to 1 when transmission from the transmit FIFO has been aborted. The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsend messages in the transmit FIFO is not 0.

Figure 23.15 shows the transmit FIFO mailbox operation.

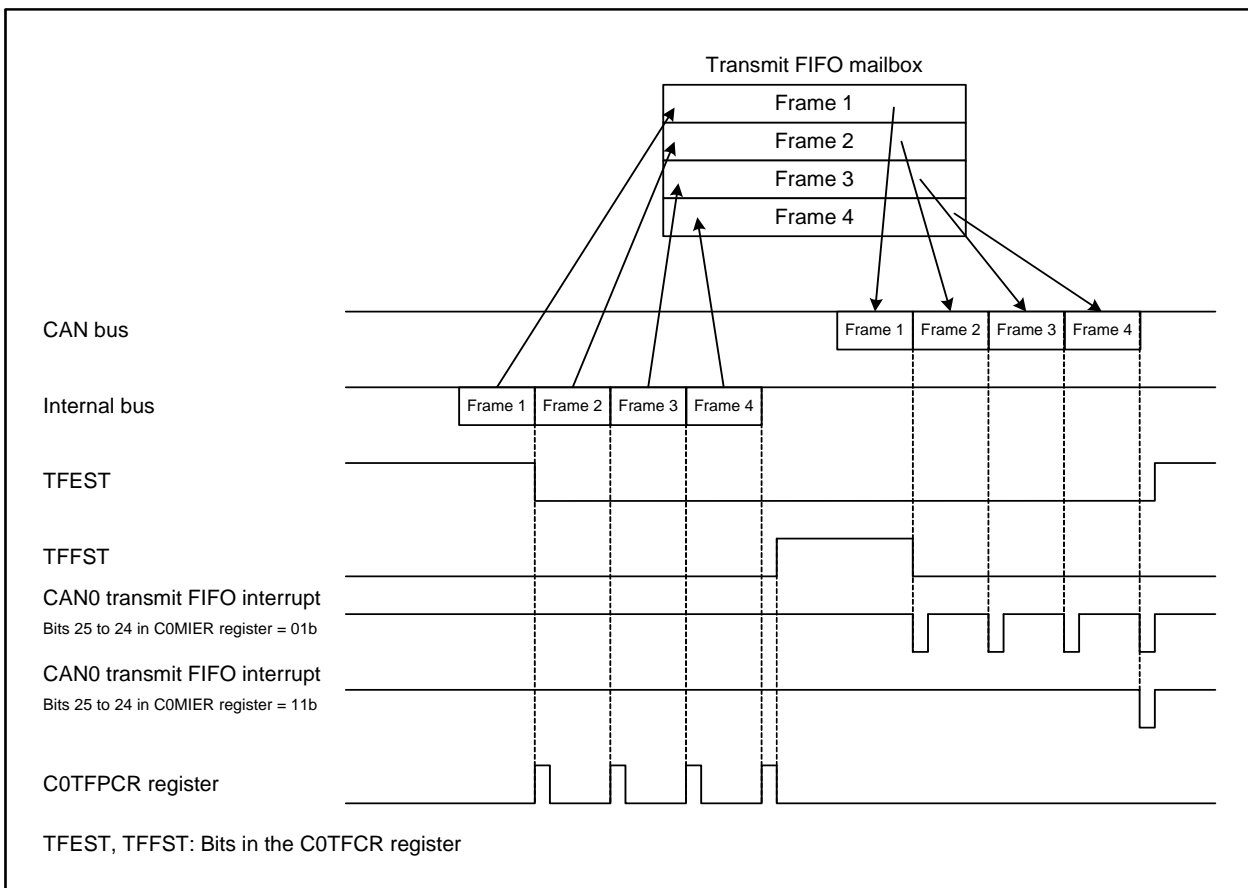
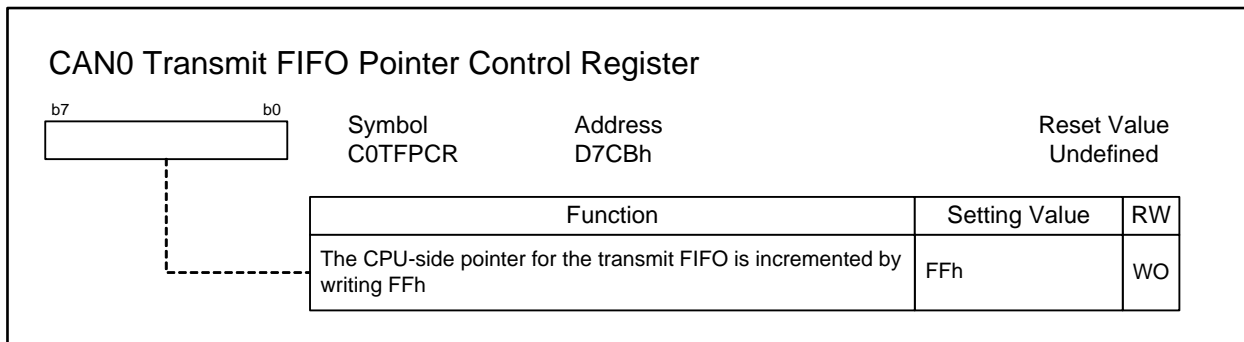


Figure 23.15 Transmit FIFO Mailbox Operation (Bits 25 and 24 in C0MIER Register = 01b and 11b)

### 23.1.13 CAN0 Transmit FIFO Pointer Control Register (C0TFPCR)



**Figure 23.16 C0TFPCR Register**

When the transmit FIFO is not full, write FFh to the C0TFPCR register by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.

Do not write to the C0TFPCR register when the TFE bit in the C0TFPCR register is 0 (transmit FIFO disabled).

### 23.1.14 CAN0 Status Register (C0STR)

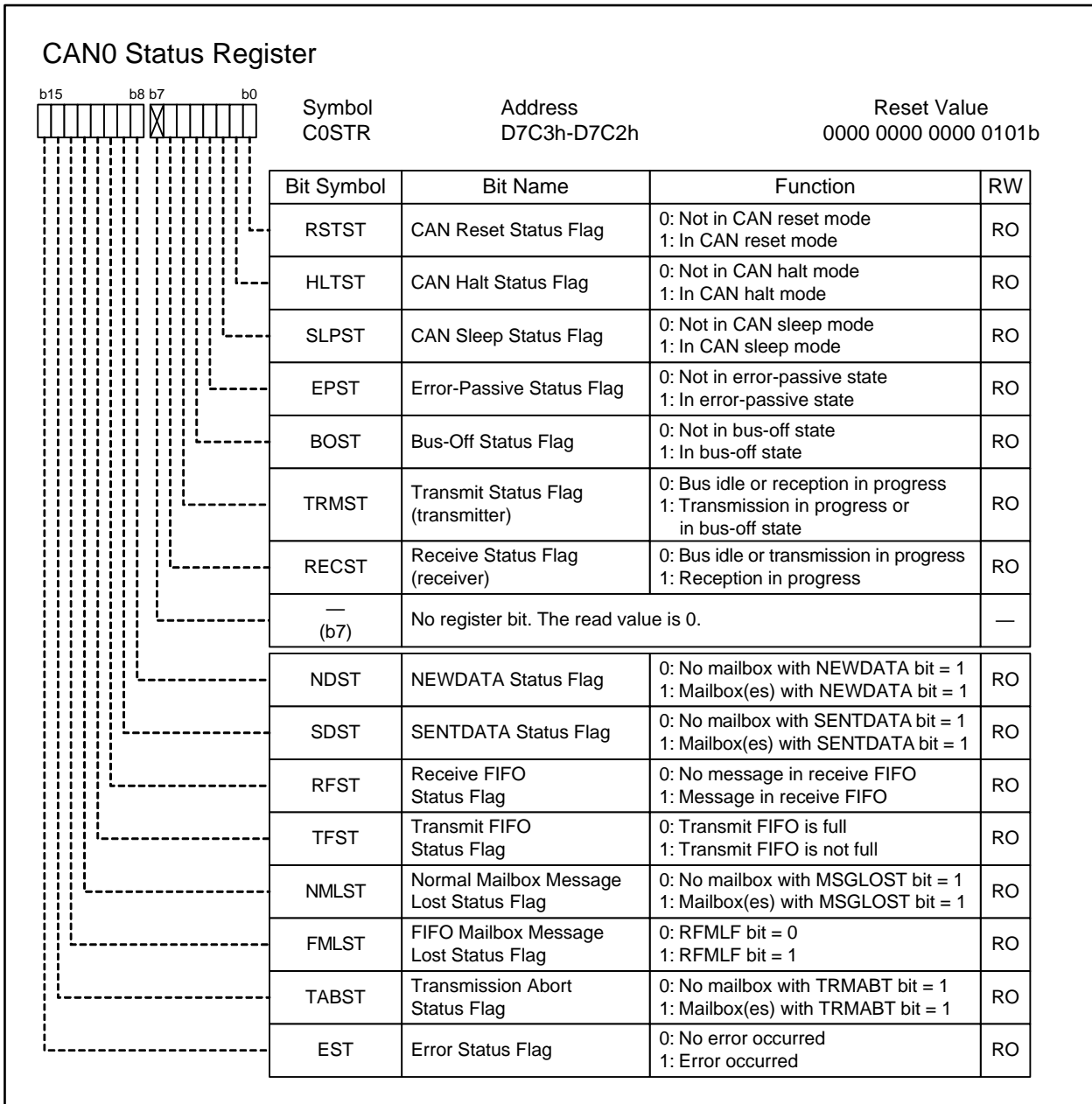


Figure 23.17 C0STR Register

#### 23.1.14.1 RSTST Bit

The RSTST bit is set to 1 when the CAN module is in CAN reset mode.

This bit is set to 0 when the CAN module is not in CAN reset mode.

Even when the state is changed from CAN reset mode to CAN sleep mode, the RSTST bit remains 1.

#### 23.1.14.2 HLTST Bit

The HLTST bit is set to 1 when the CAN module is in CAN halt mode.

This bit is set to 0 when the CAN module is not in CAN halt mode.

Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST bit remains 1.

#### 23.1.14.3 SLPST Bit

The SLPST bit is set to 1 when the CAN module is in CAN sleep mode.

This bit is set to 0 when the CAN module is not in CAN sleep mode.

#### 23.1.14.4 EPST Bit

The EPST bit is set to 1 when the value of the C0TECR or C0RECR register exceeds 127 and the CAN module is in error-passive state ( $128 \leq \text{TEC} < 256$  or  $128 \leq \text{REC} < 256$ ). This bit is set to 0 when the CAN module is not in error-passive state.

TEC indicates the value of the transmit error counter (C0TECR register) and REC indicates the value of the receive error counter (C0RECR register).

#### 23.1.14.5 BOST Bit

The BOST bit is set to 1 when the value of the C0TECR register exceeds 255 and the CAN module is in bus-off state ( $\text{TEC} \geq 256$ ). This bit is set to 0 when the CAN module is not in bus-off state.

#### 23.1.14.6 TRMST Bit

The TRMST bit is set to 1 when the CAN module performs as a transmitter node or is in bus-off state.

This bit is set to 0 when the CAN module performs as a receiver node or is in bus-idle state.

#### 23.1.14.7 RECST Bit

The RECST bit is set to 1 when the CAN module performs as a receiver node.

This bit is set to 0 when the CAN module performs as a transmitter node or is in bus-idle state.

#### 23.1.14.8 NDST Bit

The NDST bit is set to 1 when at least one NEWDATA bit in the C0MCTLj register ( $j = 0$  to 31) is 1 regardless of the value of the C0MIER register.

The NDST bit is set to 0 when all NEWDATA bits are 0.

### 23.1.14.9 SDST Bit

The SDST bit is set to 1 when at least one SENTDATA bit in the COMCTLj register (j = 0 to 31) is 1 regardless of the value of the COMIER register.

The SDST bit is set to 0 when all SENTDATA bits are 0.

### 23.1.14.10 RFST Bit

The RFST bit is set to 1 when the receive FIFO is not empty.

This bit is set to 0 when the receive FIFO is empty.

This bit is set to 0 when normal mailbox mode is selected.

### 23.1.14.11 TFST Bit

The TFST bit is set to 1 when the transmit FIFO is not full.

This bit is set to 0 when the transmit FIFO is full.

This bit is set to 0 when normal mailbox mode is selected.

### 23.1.14.12 NMLST Bit

The NMLST bit is set to 1 when at least one MSGLOST bit in the COMCTLj register is 1 regardless of the value of the COMIER register.

The NMLST bit is set to 0 when all MSGLOST bits are 0.

### 23.1.14.13 FMLST Bit

The FMLST bit is set to 1 when the RFMLF bit in the CORFCR register is 1 regardless of the value of the COMIER register.

The FMLST bit is set to 0 when the RFMLF bit is 0.

### 23.1.14.14 TABST Bit

The TABST bit is set to 1 when at least one TRMABT bit in the COMCTLj register is 1 regardless of the value of the COMIER register.

The TABST bit is set to 0 when all TRMABT bits are 0.

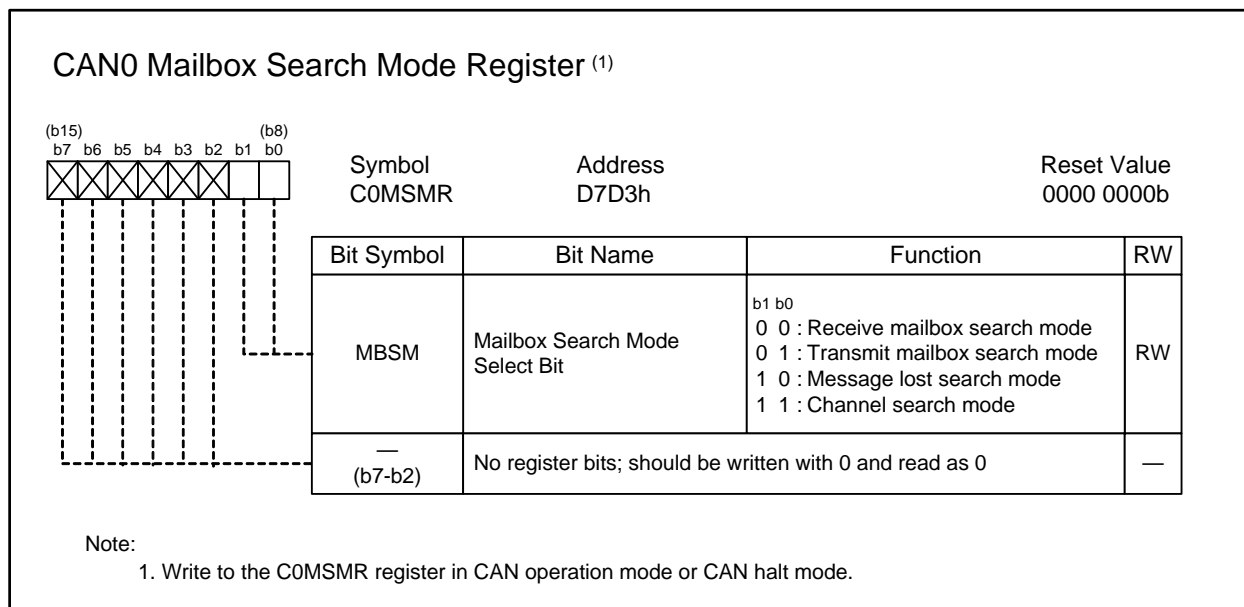
### 23.1.14.15 EST Bit

The EST bit is 1 when at least one error is detected by the COEIFR register regardless of the value of the COEIER register.

This bit is set to 0 when no error is detected by the COEIFR register.



### 23.1.15 CAN0 Mailbox Search Mode Register (C0MSMR)



**Figure 23.18 C0MSMR Register**

#### 23.1.15.1 MBSM Bit

The MBSM bit selects the search mode for the mailbox search function.

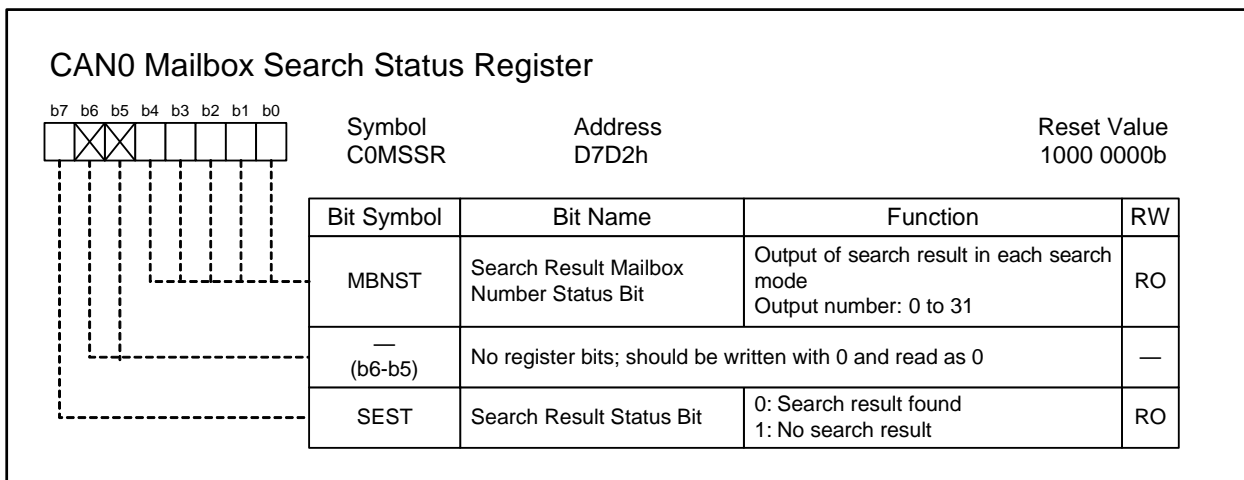
When this bit is 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in the C0MCTLj register (j = 0 to 31) for the normal mailbox and the RFEST bit in the C0RFCR register.

When the MBSM bit is 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA bit in the C0MCTLj register.

When the MBSM bit is 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST bit in the C0MCTLj register for the normal mailbox and the RFMLF bit in the C0RFCR register.

When the MBSM bit is 11b, channel search mode is selected. In this mode, the search target is the C0CSSR register. Refer to 23.1.17 "CAN0 Channel Search Support Register (C0CSSR)".

### 23.1.16 CAN0 Mailbox Search Status Register (C0MSSR)



**Figure 23.19 C0MSSR Register**

### 23.1.16.1 MBNST Bit

The MBNST bit outputs the smallest mailbox number that is searched in each mode of the COMSMR register.

In receive mailbox, transmit mailbox, and message lost search modes, the value of the mailbox i.e., the search result to be output, is updated as described below:

- When the NEWDATA, SENTDATA, or MSGLOST bit for the output mailbox is set to 0.
- When the NEWDATA, SENTDATA, or MSGLOST bit for a higher-priority mailbox is set to 1.

In receive mailbox search and message lost search modes, the receive FIFO (mailbox [28]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [23]).

In transmit mailbox search mode, the transmit FIFO (mailbox [24]) is not output.

Table 23.7 lists the behavior of MBNST bit in FIFO mailbox mode.

**Table 23.7 Behavior of MBNST Bit in FIFO Mailbox Mode**

MBSM Bit	Mailbox [24] (Transmit FIFO)	Mailbox [28] (Receive FIFO)
00b	Mailbox [24] is not output.	Mailbox [28] is output when no NEWDATA bit for the normal mailbox is set to 1 and the receive FIFO is not empty.
01b		Mailbox [28] is not output.
10b		Mailbox [28] is output when no MSGLOST bit for the normal mailbox is set to 1 and the RFMLF bit is set to 1 in the receive FIFO.
11b		Mailbox [28] is not output.

In channel search mode, the MBNST bit outputs the corresponding channel number. After the COMSSR register is read by a program, the next target channel number is output.

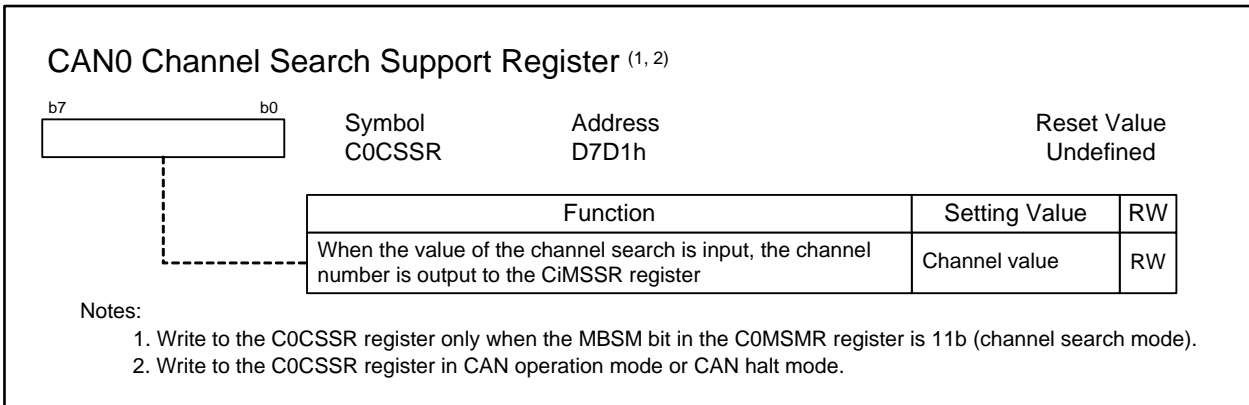
### 23.1.16.2 SEST Bit

The SEST bit is set to 1 when no corresponding mailbox is found after searching all mailboxes.

For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA bit for mailboxes is 1. The SEST bit is set to 0 when at least one SENTDATA bit is 1.

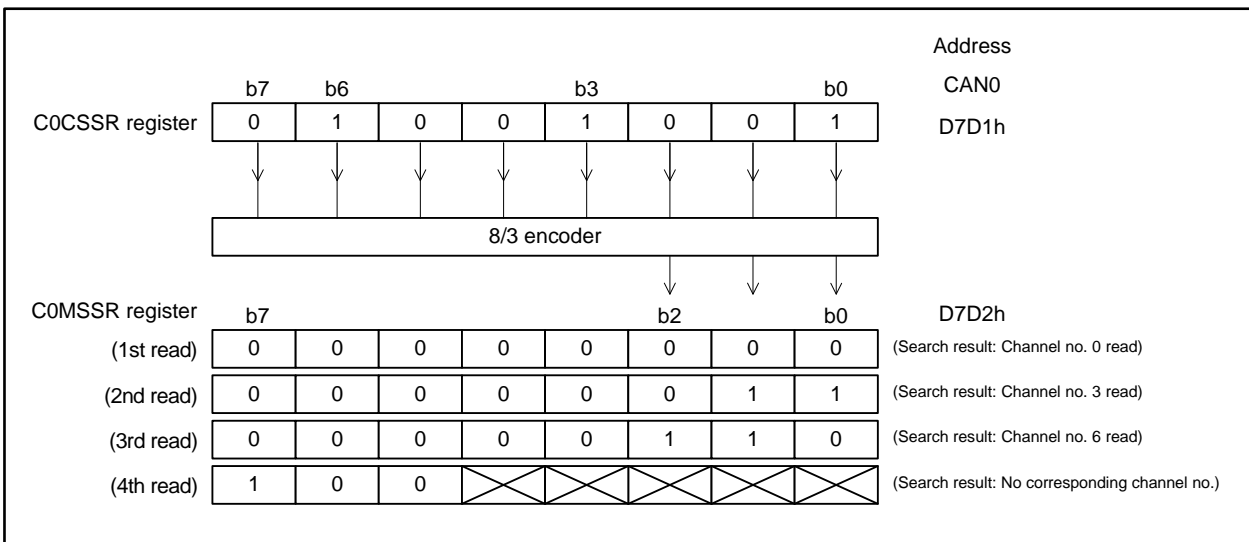
When the SEST bit is 1, the value of the MBNST bit is undefined.

### 23.1.17 CAN0 Channel Search Support Register (C0CSSR)



**Figure 23.20 C0CSSR Register**

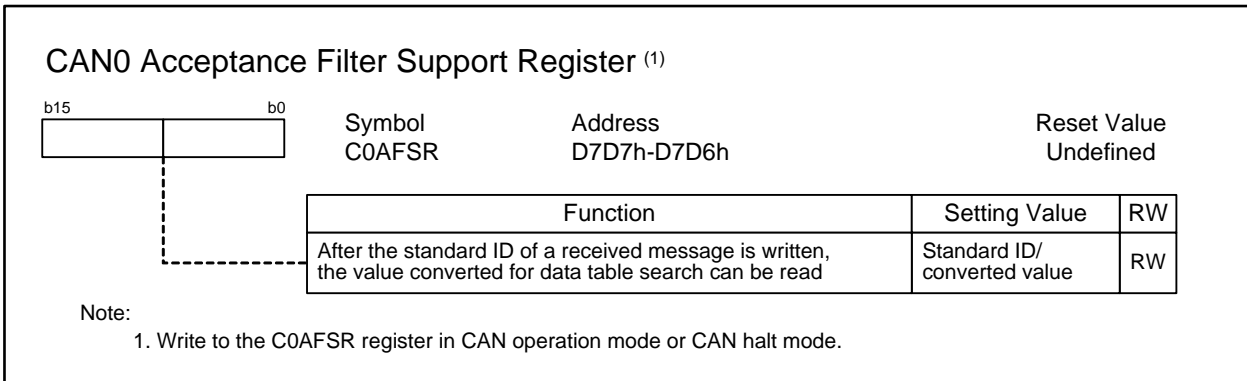
The bits in the C0CSSR register, which are set to 1, are encoded by an 8/3 encoder (the lower bit position, the higher priority) and output to the MBNST bits in the C0MSSR register. The C0MSSR register outputs the updated value whenever the C0MSSR register is read by a program. Figure 23.21 shows the write and read of registers C0CSSR and C0MSSR.



**Figure 23.21 Write and Read of Registers C0CSSR and C0MSSR**

The value of the C0CSSR register is also updated whenever the C0MSSR register is read. When the C0CSSR register is read, the value before the 8/3 encoder conversion is read.

### 23.1.18 CAN0 Acceptance Filter Support Register (C0AFSR)



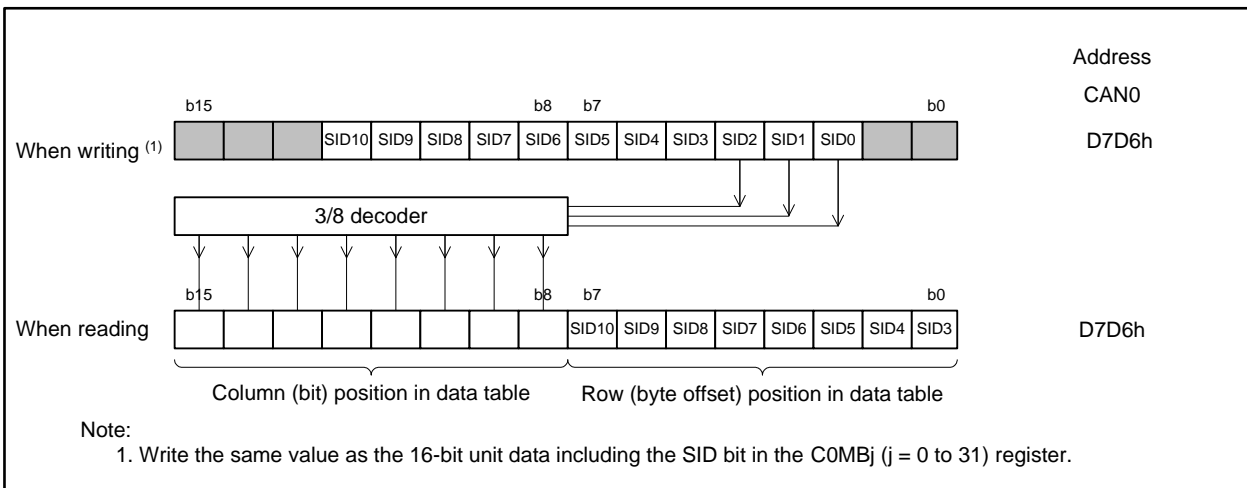
**Figure 23.22 C0AFSR Register**

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When the C0AFSR register is written with the 16-bit unit data including the SID bit in the C0MBj register (j = 0 to 31), in which a received ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

The ASU is enabled in the following cases:

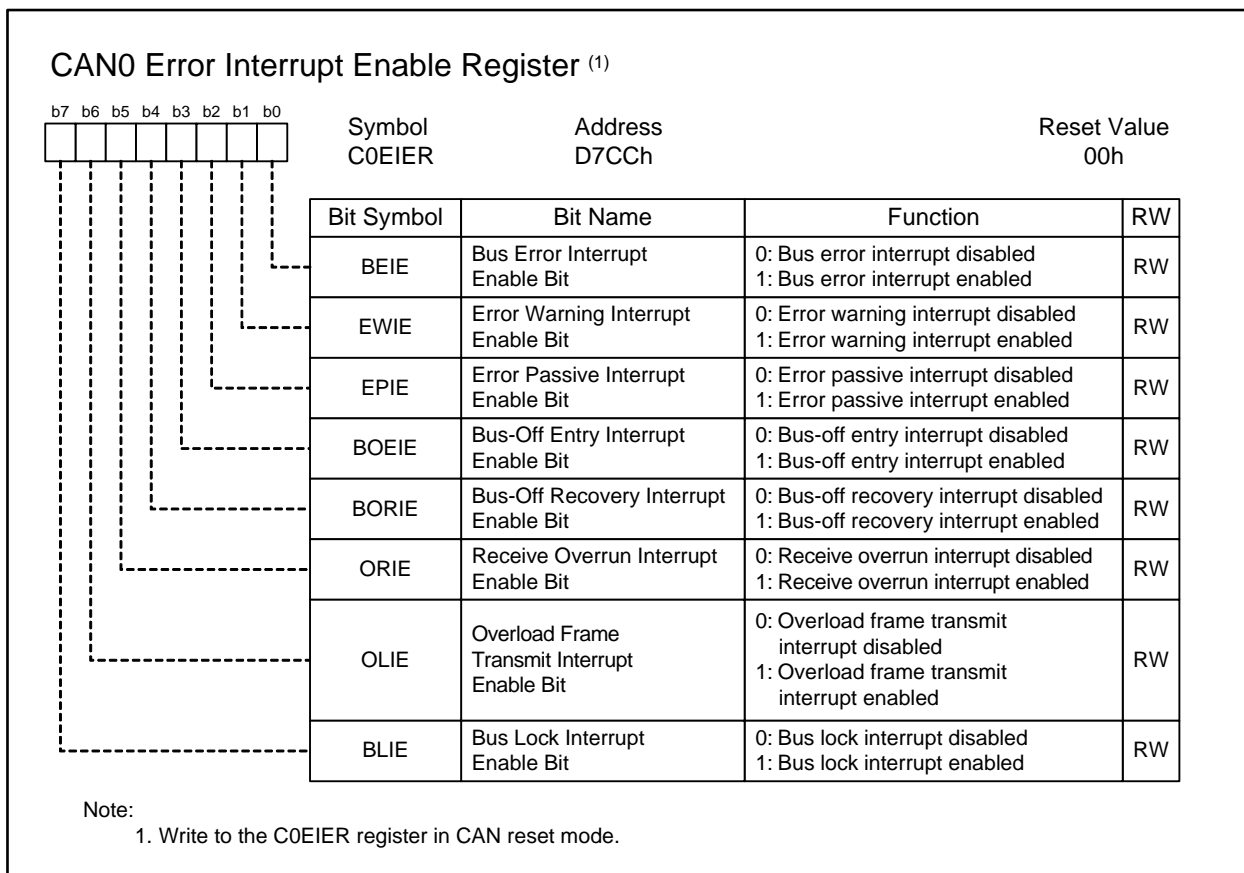
- When the ID to receive cannot be masked by the acceptance filter.  
Example) IDs to receive: 078h, 087h, 111h
- When there are too many IDs to receive and software filtering time is expected to be shortened.

Figure 23.23 shows the write and read of C0AFSR register.



**Figure 23.23 Write and Read of C0AFSR Register**

### 23.1.19 CAN0 Error Interrupt Enable Register (C0EIER)



**Figure 23.24 C0EIER Register**

The C0EIER register is used to set the error interrupt enabled/disabled individually for each error interrupt source in the C0EIFR register.

**23.1.19.1 BEIE Bit**

When the BEIE bit is 0, no error interrupt request is generated even if the BEIF bit in the C0EIFR register is set to 1.

When the BEIE bit is 1, an error interrupt request is generated if the BEIF bit is set to 1.

**23.1.19.2 EWIE Bit**

When the EWIE bit is 0, no error interrupt request is generated even if the EWIF bit in the C0EIFR register is set to 1.

When the EWIE bit is 1, an error interrupt request is generated if the EWIF bit is set to 1.

**23.1.19.3 EPIE Bit**

When the EPIE bit is 0, no error interrupt request is generated even if the EPIF bit in the C0EIFR register is set to 1.

When the EPIE bit is 1, an error interrupt request is generated if the EPIF bit is set to 1.

**23.1.19.4 BOEIE Bit**

When the BOEIE bit is 0, no error interrupt request is generated even if the BOEIF bit in the C0EIFR register is set to 1.

When the BOEIE bit is 1, an error interrupt request is generated if the BOEIF bit is set to 1.

**23.1.19.5 BORIE Bit**

When the BORIE bit is 0, an error interrupt request is not generated even if the BORIF bit in the C0EIFR register is set to 1.

When the BORIE bit is 1, an error interrupt request is generated if the BORIF bit is set to 1.

**23.1.19.6 ORIE Bit**

When the ORIE bit is 0, no error interrupt request is generated even if the ORIF bit in the C0EIFR register is set to 1.

When the ORIE bit is 1, an error interrupt request is generated if the ORIF bit is set to 1.

**23.1.19.7 OLIE Bit**

When the OLIE bit is 0, no error interrupt request is generated even if the OLIF bit in the C0EIFR register is set to 1.

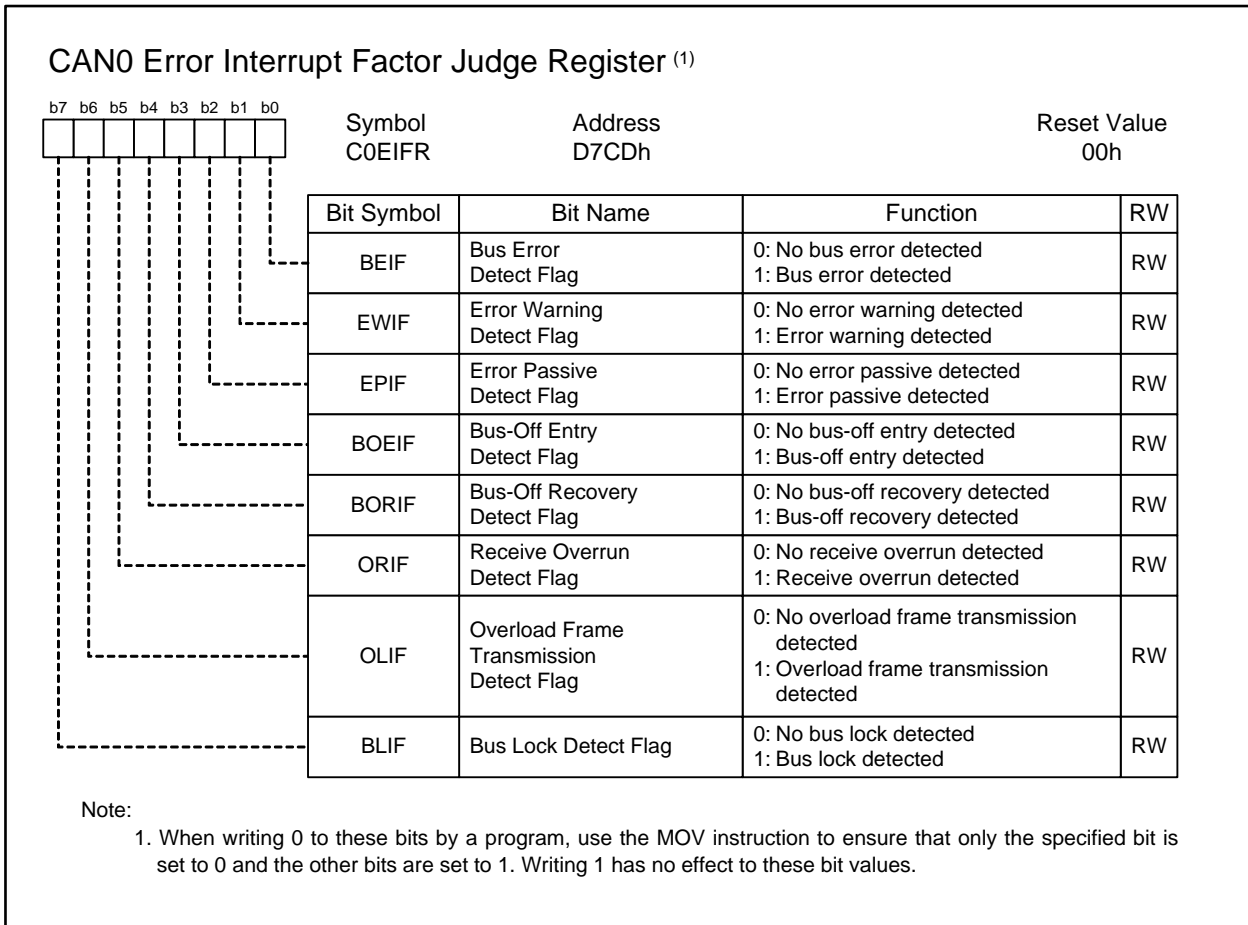
When the OLIE bit is 1, an error interrupt request is generated if the OLIF bit is set to 1.

**23.1.19.8 BLIE Bit**

When the BLIE bit is 0, no error interrupt request is generated even if the BLIF bit in the C0EIFR register is set to 1.

When the BLIE bit is 1, an error interrupt request is generated if the BLIF bit is set to 1.

### 23.1.20 CAN0 Error Interrupt Factor Judge Register (C0EIFR)



**Figure 23.25 C0EIFR Register**

If an event corresponding to each bit occurs, the corresponding bit in the C0EIFR register is set to 1 regardless of the setting of the C0EIER register.

To set each bit to 0, write 0 by a program. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes 1.

#### 23.1.20.1 BEIF Bit

The BEIF bit is set to 1 when a bus error is detected.

#### 23.1.20.2 EWIF Bit

The EWIF bit is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95.

This bit is set to 1 only when the REC or TEC initially exceeds 95. Thus, if 0 is written to the EWIF bit by a program while the REC or TEC remains greater than 95, this bit is not set to 1 until the REC and the TEC go below 95 and then exceed 95 again.



### 23.1.20.3 EPIF Bit

The EPIF bit is set to 1 when the CAN error state becomes error-passive (the REC or TEC value exceeds 127).

This bit is set to 1 only when the REC or TEC initially exceeds 127. Thus, if 0 is written by a program while the REC or TEC remains greater than 127, this bit is not set to 1 until the REC and the TEC go below 127 and then exceed 127 again.

### 23.1.20.4 BOEIF Bit

The BOEIF bit is set to 1 when the CAN error state becomes bus-off (the TEC value exceeds 255).

This bit is also set to 1 when the BOM bit in the C0CTLR register is 01b (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state.

### 23.1.20.5 BORIF Bit

The BORIF bit is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions:

- (1) When the BOM bit in the C0CTLR register is 00b.
- (2) When the BOM bit is 10b.
- (3) When the BOM bit is 11b.

The BORIF bit is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:

- (1) When the CANM bit in the C0CTLR register is set to 01b (CAN reset mode).
- (2) When the RBOC bit in the C0CTLR register is set to 1 (forcible return from bus-off).
- (3) When the BOM bit is 01b.
- (4) When the BOM bit is 11b and the CANM bit is set to 10b (CAN halt mode) before normal recovery occurs.

Table 23.8 lists the behavior of bits BOEIF and BORIF according to BOM bit setting value.

**Table 23.8 Behavior of Bits BOEIF and BORIF according to BOM Bit Setting Value**

BOM Bit	BOEIF Bit	BORIF Bit
00b	Set to 1 on entry to the bus-off state.	Set to 1 on exit from the bus-off state.
01b		Do not set to 1.
10b		Set to 1 on exit from the bus-off state.
11b		Set to 1 if normal bus-off recovery occurs before the CANM bit is set to 10b (CAN halt mode).

### 23.1.20.6 ORIF Bit

The ORIF bit is set to 1 when a receive overrun occurs.

This bit is not to set to 1 in overwrite mode. In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and this bit is not set to 1.

In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [31] in overrun mode, this bit is set to 1.

In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [23] or the receive FIFO in overrun mode, this bit is set to 1.

### 23.1.20.7 OLIF Bit

The OLIF bit is set to 1 if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception.

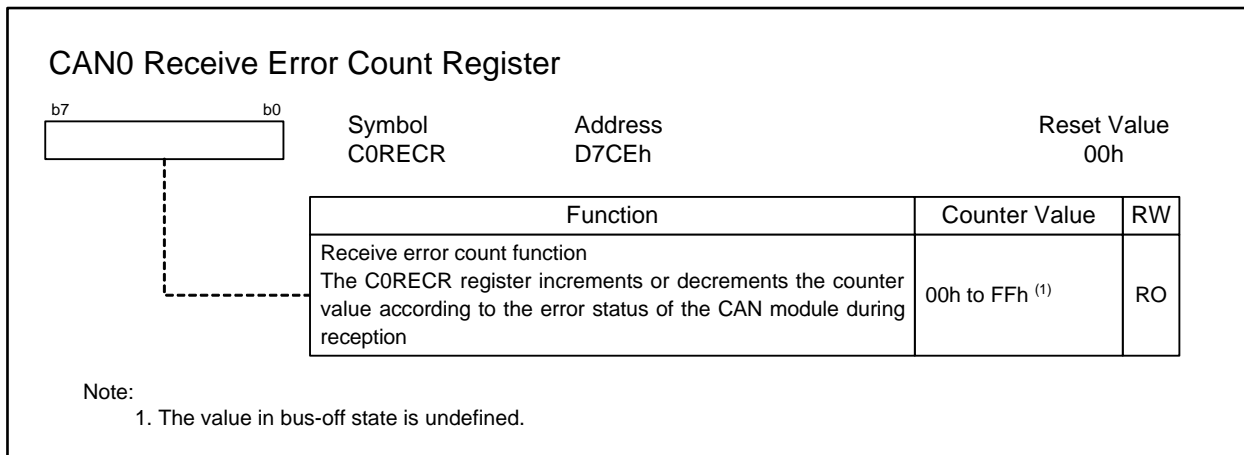
### 23.1.20.8 BLIF Bit

The BLIF bit is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.

After the BLIF bit is set to 1, 32 consecutive dominant bits are detected again under either of the following conditions:

- After this bit is set to 0 from 1, recessive bits are detected.
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

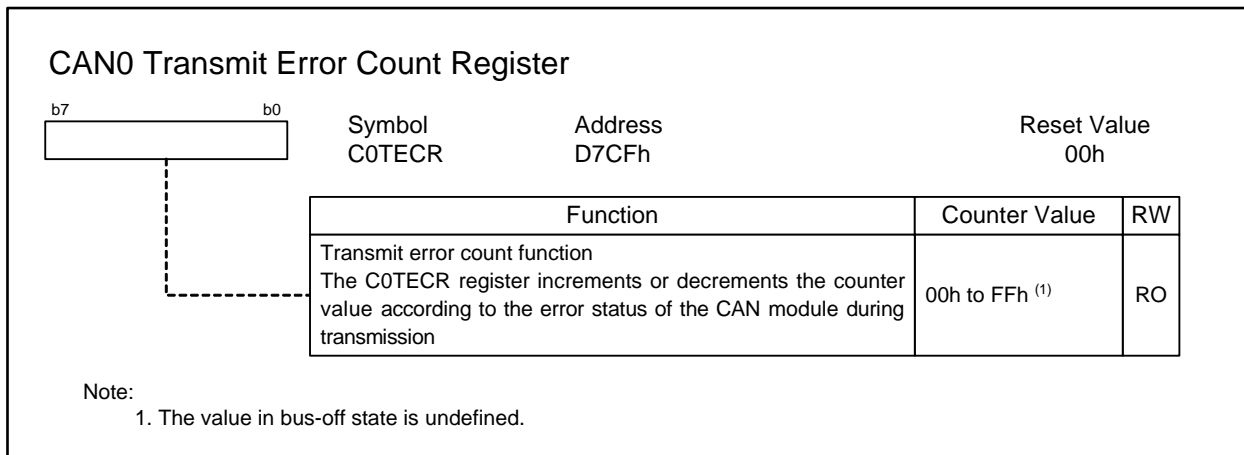
### 23.1.21 CAN0 Receive Error Count Register (C0RECR)



**Figure 23.26 C0RECR Register**

The C0RECR register indicates the value of the receive error counter. Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the receive error counter.

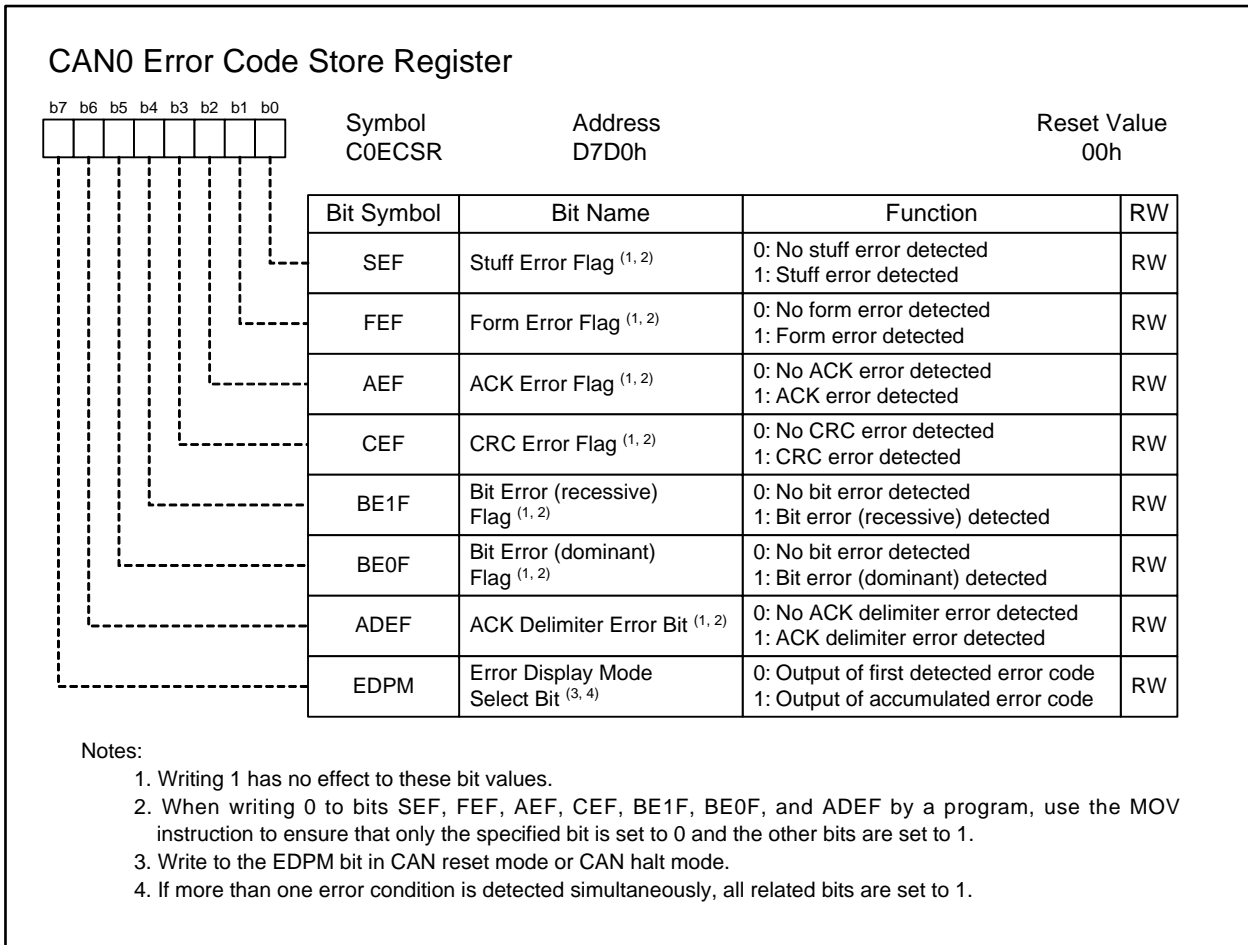
### 23.1.22 CAN0 Transmit Error Count Register (C0TECR)



**Figure 23.27 C0TECR Register**

The C0TECR register indicates the value of the TEC error counter. Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the transmit error counter.

### 23.1.23 CAN0 Error Code Store Register (C0ECSR)



**Figure 23.28 C0ECSR Register**

The C0ECSR register can be used to monitor whether an error has occurred on the CAN bus. Refer to the CAN Specifications (ISO11898-1) to check the generation conditions of each error.

To set each bit except the EDPM bit to 0, write 0 by a program. If the timing at which each bit is set to 1 and the timing at which is written by a program are the same, the relevant bit is set to 1.

#### 23.1.23.1 SEF Bit

The SEF bit is set to 1 when a stuff error is detected.

#### 23.1.23.2 FEF Bit

The FEF bit is set to 1 when a form error is detected.

#### 23.1.23.3 AEF Bit

The AEF bit is set to 1 when an ACK error is detected.

**23.1.23.4 CEF Bit**

The CEF bit is set to 1 when a CRC error is detected.

**23.1.23.5 BE1F Bit**

The BE1F bit is set to 1 when a recessive bit error is detected.

**23.1.23.6 BE0F Bit**

The BE0F bit is set to 1 when a dominant bit error is detected.

**23.1.23.7 ADEF Bit**

The ADEF bit is set to 1 when a form error is detected with the ACK delimiter during transmission.

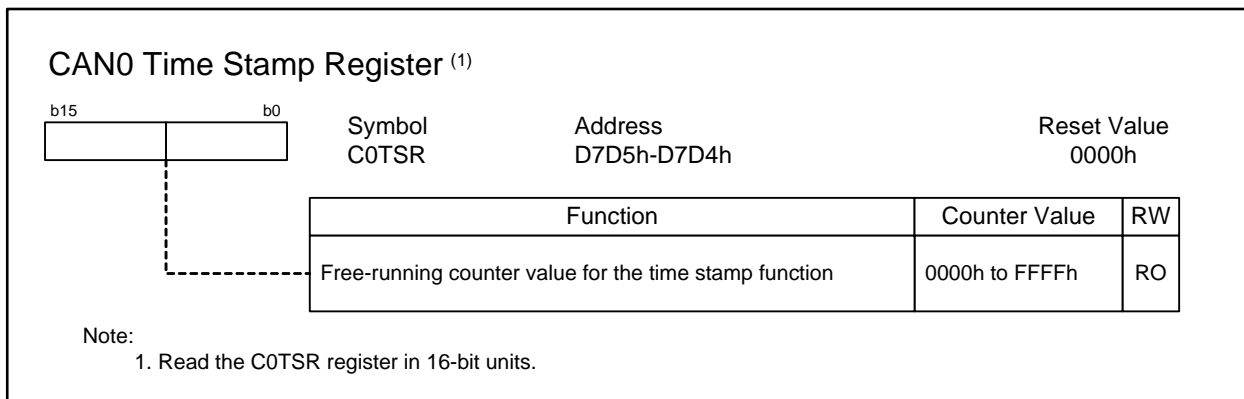
**23.1.23.8 EDPM Bit**

The EDPM bit selects the output mode of the C0ECSR register.

When this bit is set to 0, the C0ECSR register outputs the first error code.

When this bit is set to 1, the C0ECSR register outputs the accumulated error code.

### 23.1.24 CAN0 Time Stamp Register (C0TSR)



**Figure 23.29 C0TSR Register**

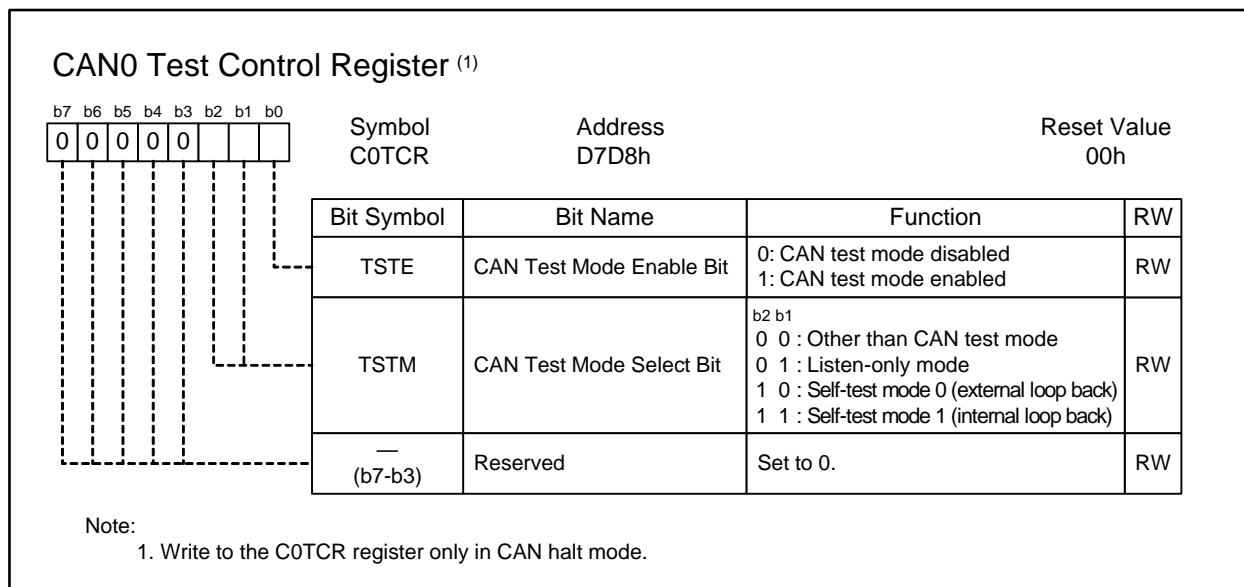
When the C0TSR register is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.

The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by the TSPS bit in the C0CTLR register.

The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.

The time stamp counter value is stored to TSL and TSH in the C0MBj register (j = 0 to 31) when a received message is stored in a receive mailbox.

### 23.1.25 CAN0 Test Control Register (C0TCR)



**Figure 23.30 C0TCR Register**

#### 23.1.25.1 TSTE Bit

When the TSTE bit is set to 0, CAN test mode is disabled.  
When this bit is set to 1, CAN test mode is enabled.

#### 23.1.25.2 TSTM Bit

The TSTM bit selects the CAN test mode.  
The details of each CAN test mode is described below.



### 23.1.25.3 Listen-Only Mode

The ISO 11898-1 recommends an optional bus monitoring mode. In listen-only mode, the CAN node is able to receive valid data frames and valid remote frames. It sends only recessive bits on the CAN bus and the protocol controller is not required to send the ACK bit, overload flag, or active error flag.

Listen-only mode can be used for baud rate detection.

Do not request transmission from any mailboxes in this mode.

Figure 23.31 shows the connection when listen-only mode is selected.

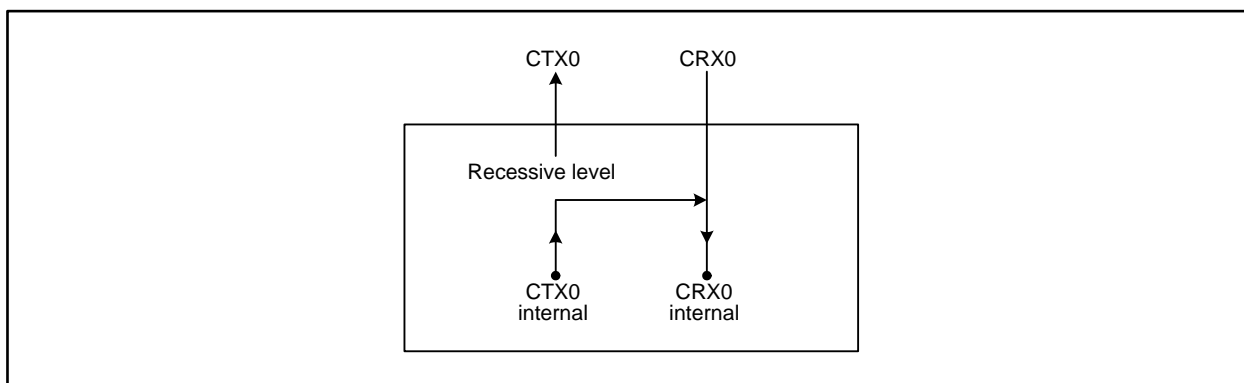


Figure 23.31 Connection when Listen-Only Mode is Selected

### 23.1.25.4 Self-Test Mode 0 (External Loop Back)

Self-test mode 0 is provided for CAN transceiver tests.

In this mode, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

Connect the CTX0/CRX0 pins to the transceiver.

Figure 23.32 shows the connection when self-test mode 0 is selected.

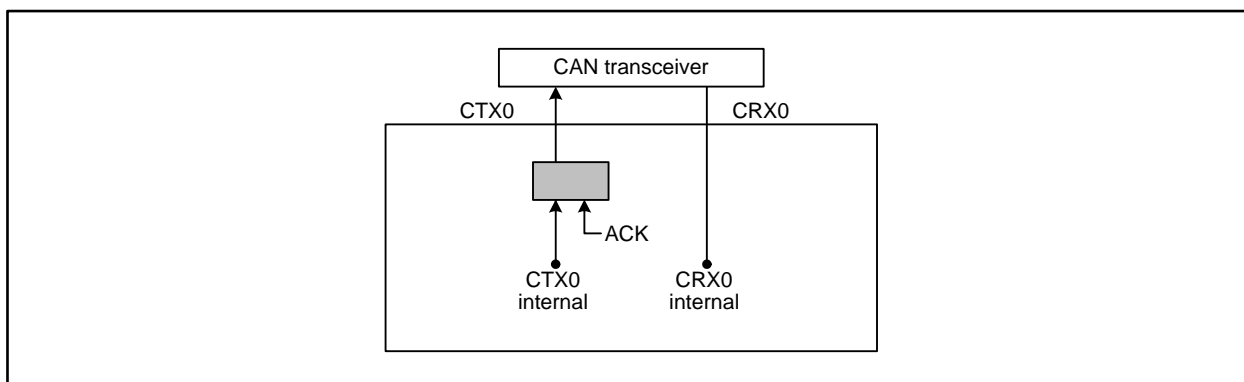


Figure 23.32 Connection when Self-Test Mode 0 is Selected

### 23.1.25.5 Self-Test Mode 1 (Internal Loop Back)

Self-test mode 1 is provided for self-test functions.

In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CTX0 pin to the internal CRX0 pin. The input value of the external CRX0 pin is ignored. The external CTX0 pin outputs only recessive bits. The CTX0/CRX0 pins do not need to be connected to the CAN bus or any external device.

Figure 23.33 shows the connection when self-test mode 1 is selected.

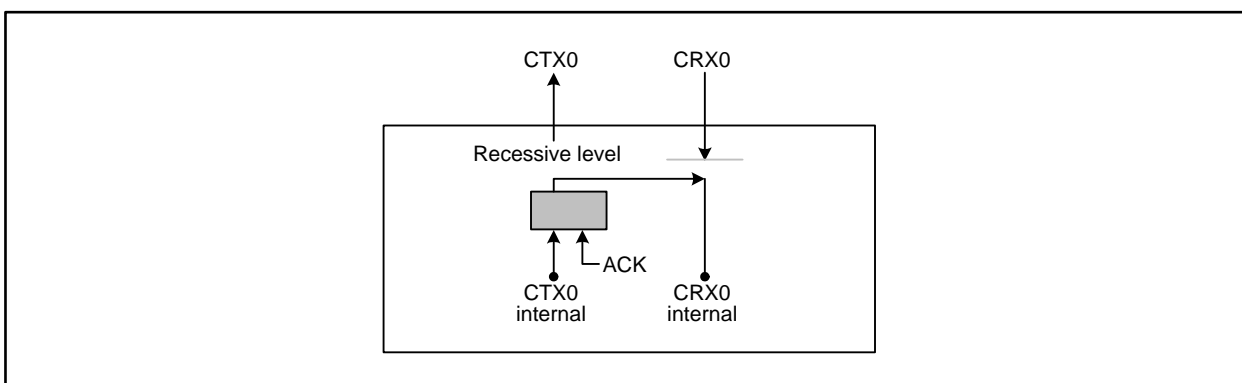


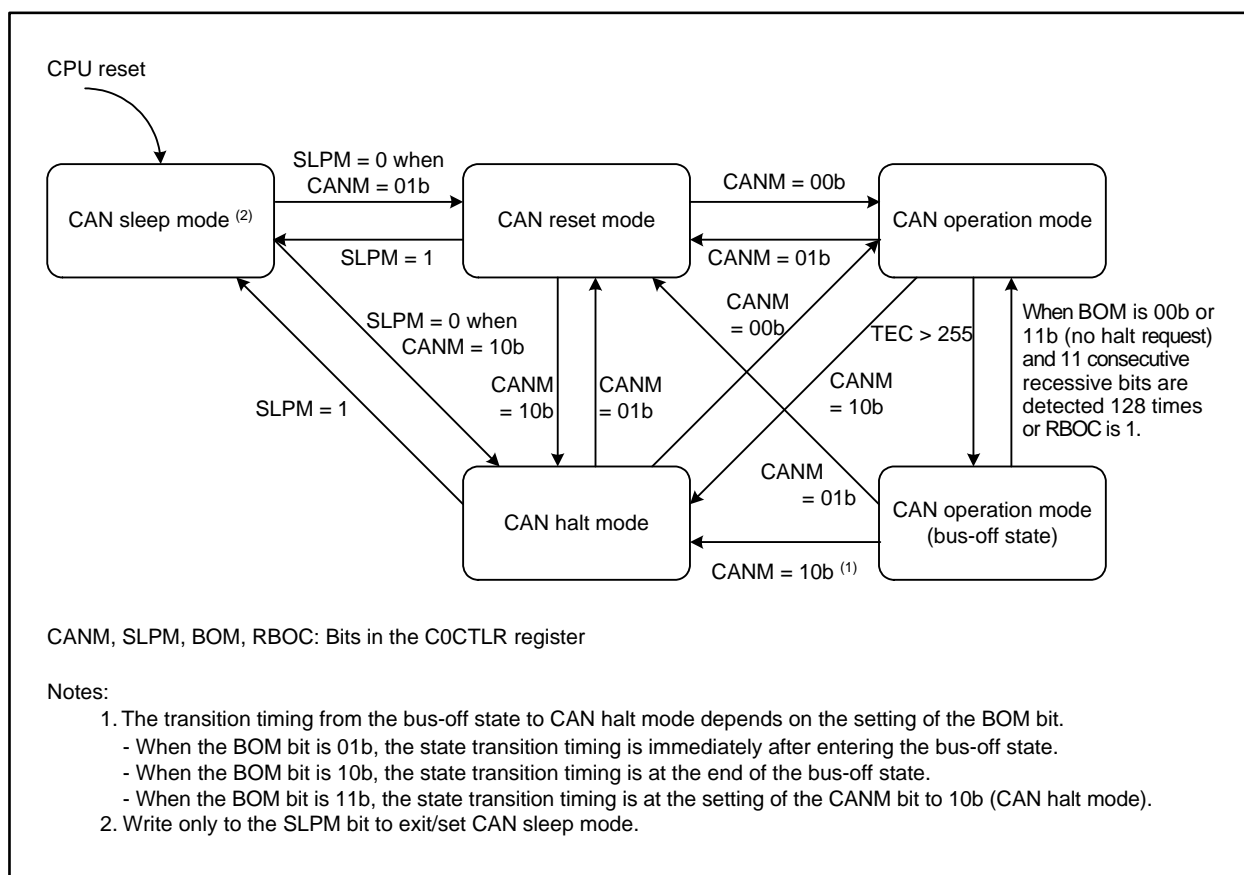
Figure 23.33 Connection when Self-Test Mode 1 is Selected

## 23.2 Operating Mode

The CAN module has the following four operating modes:

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 23.34 shows the transition between CAN operating modes.



**Figure 23.34 Transition between CAN Operating Modes**

### 23.2.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.

When the CANM bit in the C0CTLR register is set to 01b, the CAN module enters CAN reset. Then the RSTST bit in the C0STR register is set to 1. Do not change the CANM bit until the RSTST bit is set to 1. Configure the C0BCR register before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode and their initialized values are retained during CAN reset mode:

- C0MCTLj register (j = 0 to 31)
- C0STR register (except bits SLPST and TFST)
- C0EIFR register
- C0RECR register
- C0TECR register
- C0TSR register
- C0MSSR register
- C0MSMR register
- C0RFCR register
- C0TFPCR register
- C0TCR register
- C0ECSR register (except EDPM bit)

The previous values of the following registers are retained after entering CAN reset mode.

- C0CLKR register
- C0CTLR register
- C0STR register (bits SLPST and TFST)
- C0MIER register
- C0EIER register
- C0BCR register
- C0CSSR register
- C0ECSR register (EDPM bit only)
- C0MBj register
- Registers C0MKR0 to C0MKR7
- Registers C0FIDCR0 and C0FIDCR1
- C0MKIVLR register
- C0AFSR register
- C0RFPCR register
- C0TFPCR register

### 23.2.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.

When the CANM bit in the C0CTLR register is set to 10b, CAN halt mode is selected. Then the HLTST bit in the C0STR register is set to 1. Do not change the CANM bit until the HLTST bit is set to 1.

Refer to Table 23.9 Operation in CAN Reset Mode and CAN Halt Mode regarding the state transition conditions when transmitting or receiving.

All registers except bits RSTST, HLTST, and SLPST in the C0STR register remain unchanged when the CAN module enters CAN halt mode.

Do not change registers COCLKR, C0CTLR (except bits CANM and SLPM,) and COEIER in CAN halt mode. The COBCR register can be changed in CAN halt mode only when listen-only mode is selected to use for automatic bit rate detection.

**Table 23.9 Operation in CAN Reset Mode and CAN Halt Mode**

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission. (1, 4)	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. (2, 3)	CAN module enters CAN halt mode after waiting for the end of message transmission. (1, 4)	<p>[When the BOM bit is 00b] A halt request from a program will be acknowledged only after bus-off recovery.</p> <p>[When the BOM bit is 01b] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program).</p> <p>[When the BOM bit is 10b] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program).</p> <p>[When the BOM bit is 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.</p>

BOM bit: Bit in the C0CTLR register

Notes:

1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in the COEIFR register.
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN mode transits to CAN halt mode.
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN mode transits to the requested CAN mode.

### 23.2.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After MCU hardware reset or software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in the C0CTRL register is set to 1, the CAN module enters CAN sleep mode. Then the SLPST bit in the C0STR register is set to 1. Do not change the value of the SLPM bit until the bit is set to 1. The other registers remain unchanged when the MCU enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any other registers (except the SLPM bit) during CAN sleep mode. Read operation is still allowed.

When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

### 23.2.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.

When the CANM bit in the COCTRL register is set to 00b, the CAN module enters CAN operation mode. Then bits RSTST and HLTST in the C0STR register are set to 0. Do not change the value of the CANM bit until these bits are set to 0.

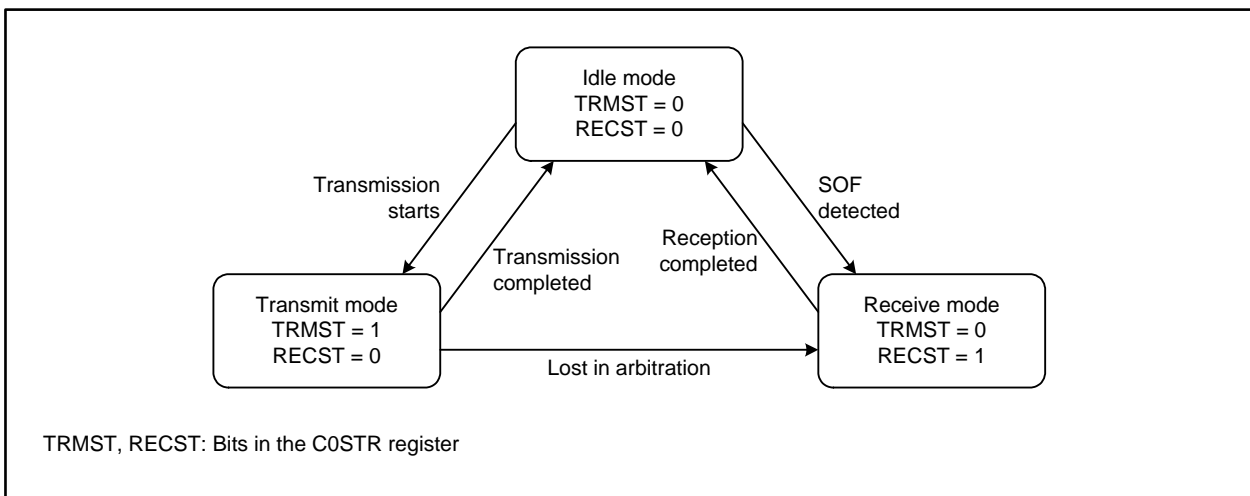
If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network that enables transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three submodes, depending on the status of the CAN bus:

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (TSTM bit in the C0STR register = 10b) or self-test mode 1 (TSTM bit = 11b) is selected.

Figure 23.35 shows the submode in CAN operation mode.



**Figure 23.35 Submode in CAN Operation Mode**

### 23.2.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/error counters in the CAN Specifications.

The following cases apply when recovering from the bus-off state. When the CAN module is in bus-off state, the values of the associated registers, except registers C0STR, C0EIFR, C0RECR, C0TECR and C0TSR, remain unchanged.

(1) When the BOM bit in the C0CTLR register is 00b (normal mode)

The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled. The BORIF bit in the C0EIFR register is set to 1 (bus-off recovery detected) at this time.

(2) When the RBOC bit in the C0CTLR register is set to 1 (forcible return from bus-off)

The CAN module enters the error-active state when it is in bus-off state and the RBOC bit is set to 1. CAN communication is enabled again after 11 consecutive recessive bits are detected. The BORIF bit is not set to 1 at this time.

(3) When the BOM bit is 01b (entry to CAN halt mode automatically at bus-off entry)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to 1 at this time.

(4) When the BOM bit is 10b (entry to CAN halt mode automatically at bus-off end)

The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to 1 at this time.

(5) When the BOM bit is 11b (entry to CAN halt mode by a program) and the CANM bit in the C0CTLR register is set to 10b (CAN halt mode) during the bus-off state

The CAN module enters CAN halt mode when it is in bus-off state and the CANM bit is set to 10b (CAN halt mode). The BORIF bit is not set to 1 at this time.

If the CANM bit is not set to 10b during bus-off, the same behavior as (1) applies.



## 23.3 CAN Communication Speed Configuration

The following description explains about the CAN communication speed configuration.

### 23.3.1 CAN Clock Configuration

This group has a CAN clock selector.

The CAN clock can be configured by setting the CCLKS bit in the C0CLKR register and the BRP bit in the C0BCR register.

Figure 23.36 shows the block diagram of CAN clock generator.

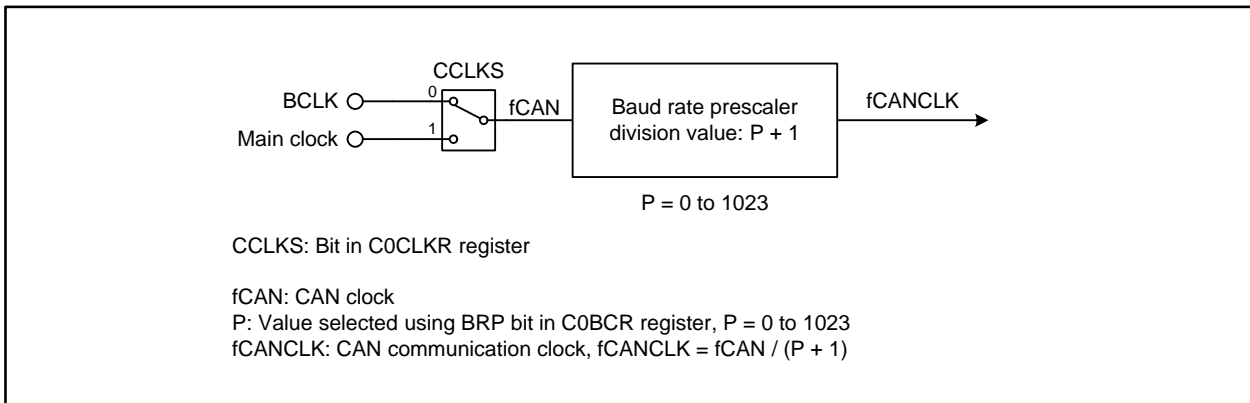


Figure 23.36 Block Diagram of CAN Clock Generator

### 23.3.2 Bit Timing Configuration

The bit time is a single bit time for transmitting/receiving a message and consists of the following three segments.

Figure 23.37 shows the bit timing.

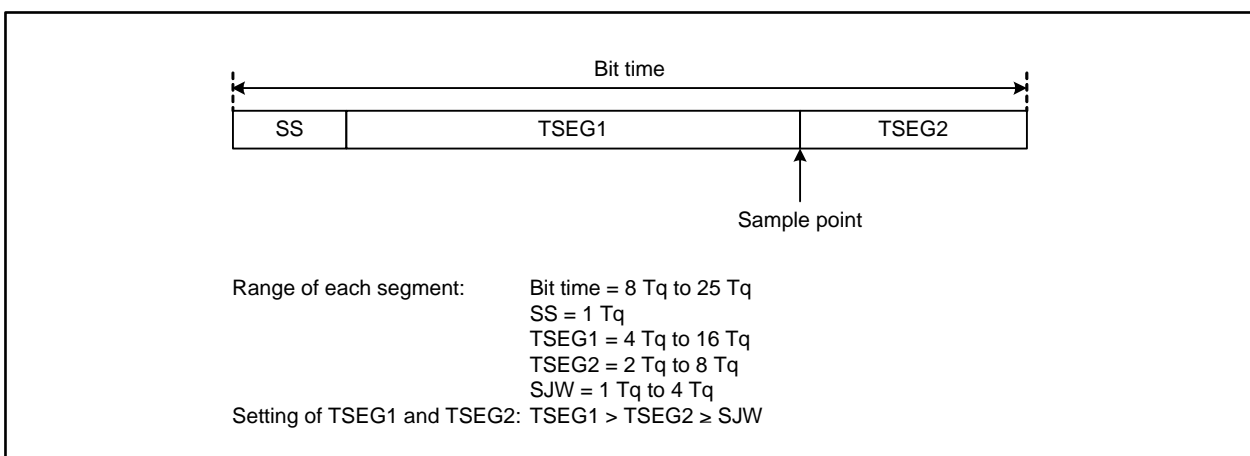


Figure 23.37 Bit Timing



### 23.4 Mailbox and Mask Register Structure

There are 32 mailboxes with the same structure.

Figure 23.38 shows the structure of C0MBj register (j = 0 to 31).

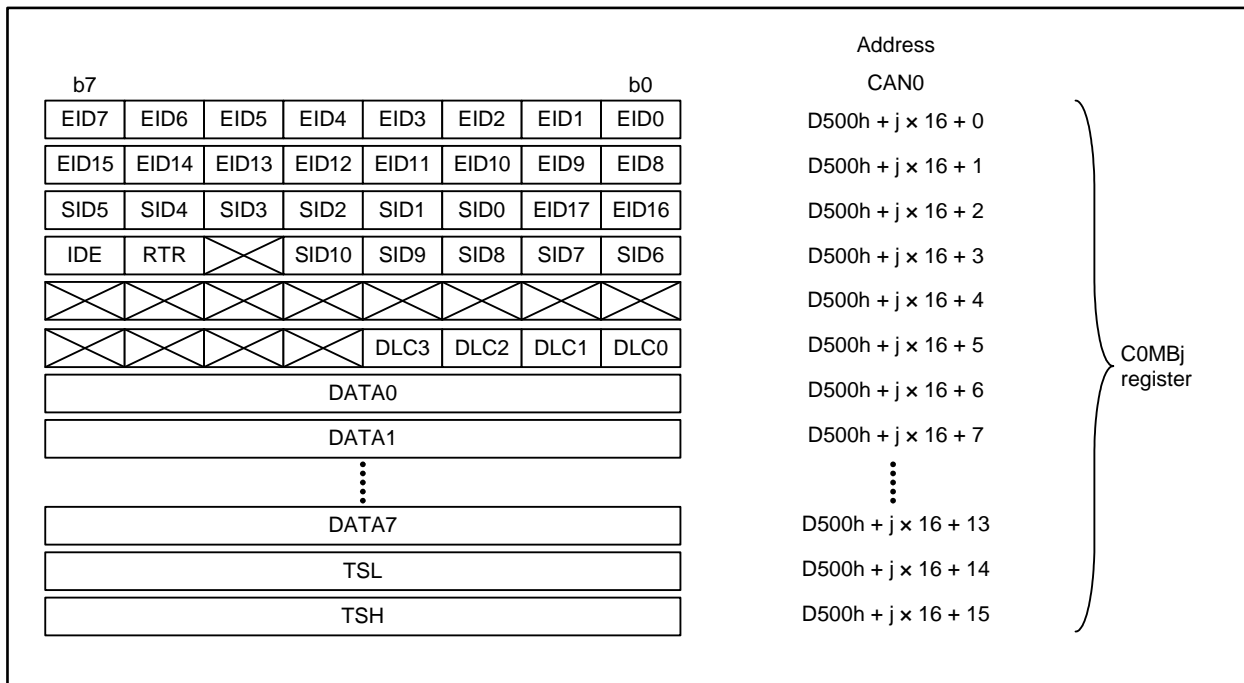


Figure 23.38 Structure of C0MBj Register (j = 0 to 31)

There are 8 mask registers with the same structure.

Figure 23.39 shows the structure of C0MKRk Register (k = 0 to 7).

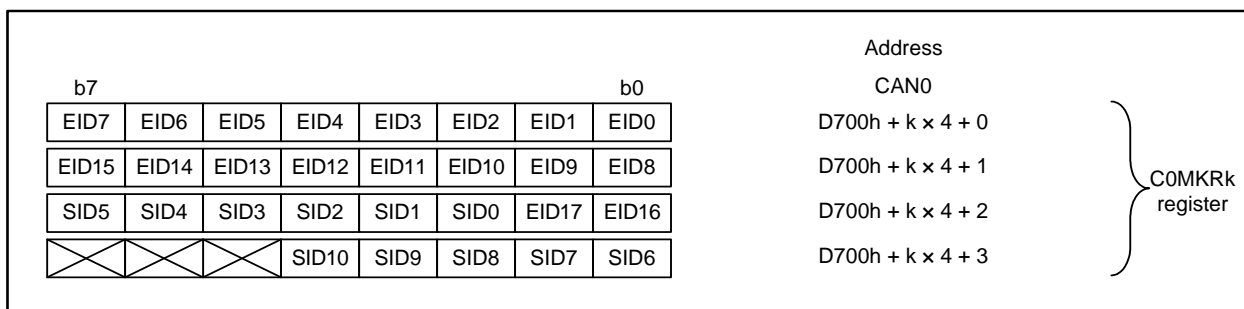
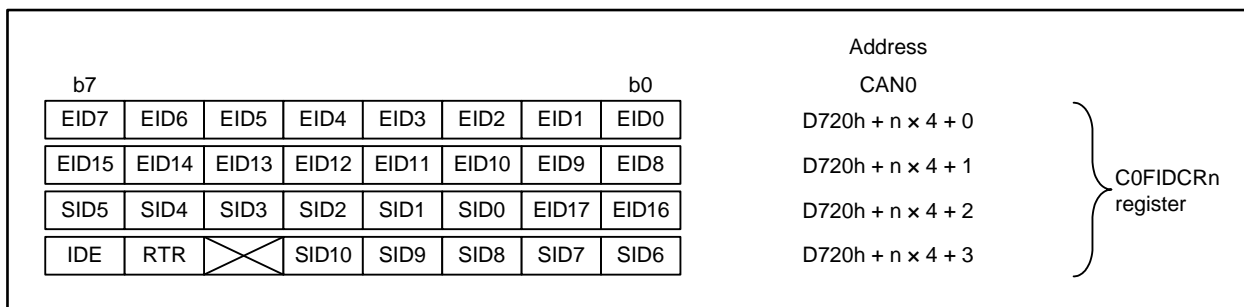


Figure 23.39 Structure of C0MKRk Register (k = 0 to 7)

There are 2 FIFO received ID compare registers with the same structure.  
 Figure 23.40 shows the structure of C0FIDCRn Register (n = 0, 1).



**Figure 23.40 Structure of C0FIDCRn Register (n = 0, 1)**

### 23.5 Acceptance Filtering and Masking Function

Acceptance filtering allows the user to receive messages with a specified range of multiple IDs for mailboxes.

Registers C0MKR0 to C0MKR7 can perform masking of the standard ID and the extended ID of 29 bits.

- The C0MKR0 register corresponds to mailboxes [0] to [3].
- The C0MKR1 register corresponds to mailboxes [4] to [7].
- The C0MKR2 register corresponds to mailboxes [8] to [11].
- The C0MKR3 register corresponds to mailboxes [12] to [15].
- The C0MKR4 register corresponds to mailboxes [16] to [19].
- The C0MKR5 register corresponds to mailboxes [20] to [23].
- The C0MKR6 register corresponds to mailboxes [24] to [27] in normal mailbox mode, and receive FIFO mailboxes [28] to [31] in FIFO mailbox mode.
- The C0MKR7 register corresponds to mailboxes [28] to [31] in normal mailbox mode, and receive FIFO mailboxes [28] to [31] in FIFO mailbox mode.

The C0MKIVLR register disables acceptance filtering individually for each mailbox.

The IDE bit in the C0MBj register (j = 0 to 31) is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode).

The RTR bit in the C0MBj register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [23]) use the single corresponding register among registers C0MKR0 to C0MKR5 for acceptance filtering. Receive FIFO mailboxes (mailboxes [28] to [31]) use two registers C0MKR6 and C0MKR7 for the acceptance filtering.

Also, the receive FIFO uses two registers C0FIDCR0 and C0FIDCR1 for ID comparison. Bits EID, SID, RTR, and IDE in registers C0MB28 to C0MB31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two ID-mask sets, two ranges of IDs can be received into the receive FIFO.

The C0MKIVLR register is disabled for the receive FIFO.

If both setting of standard ID and extended ID are set in the IDE bits in registers C0FIDCR0 and C0FIDCR1 individually, both ID formats are received.

If both setting of data frame and remote frame are set in the RTR bits in registers C0FIDCR0 and C0FIDCR1 individually, both data and remote frames are received.

When combination with two ranges of IDs is not necessary, set the same mask value and the same ID into both of the FIFO ID/mask register sets.

Figure 23.41 shows the correspondence of mask registers to mailboxes, and Figure 23.42 shows acceptance filtering.

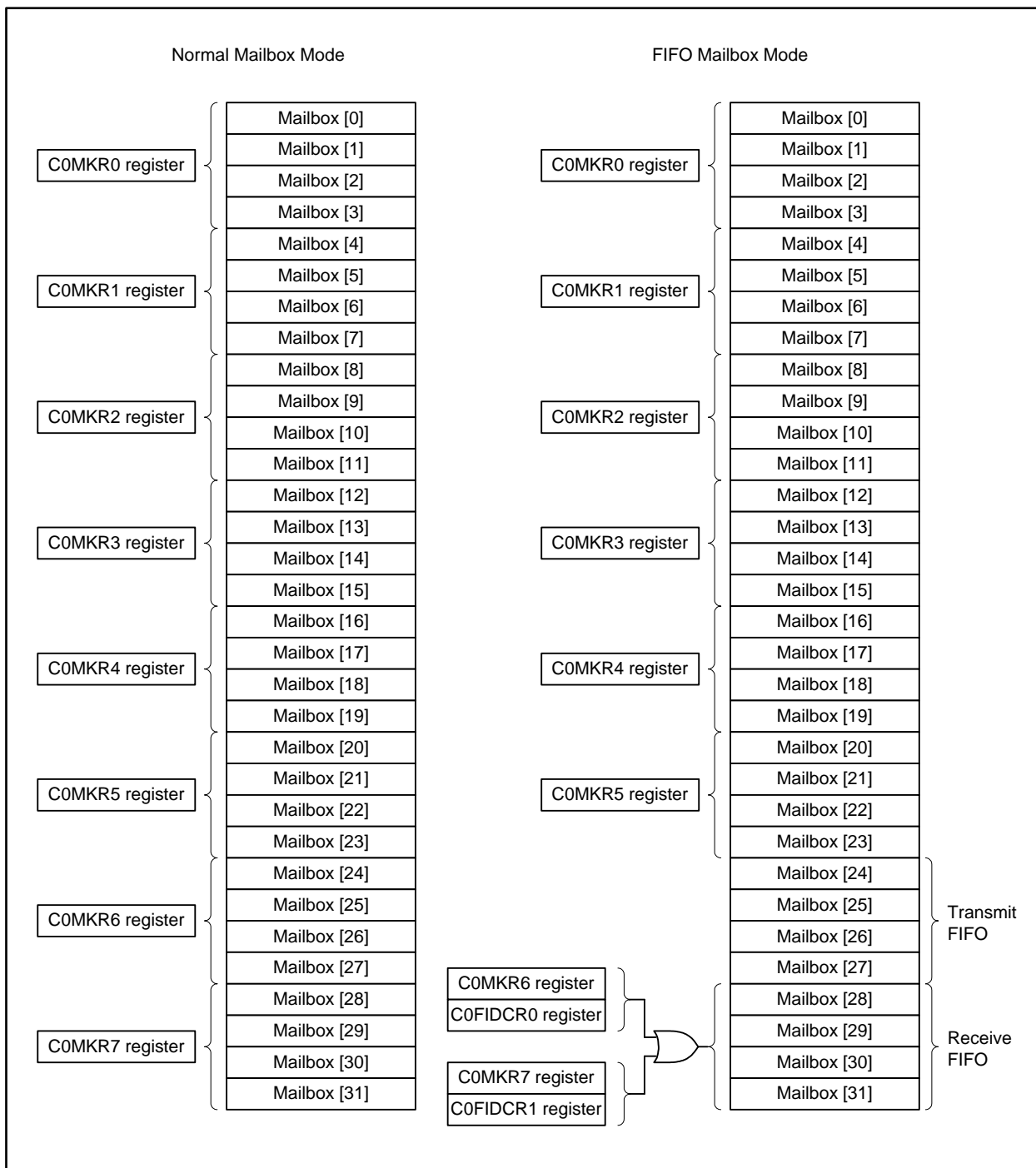


Figure 23.41 Correspondence of Mask Registers to Mailboxes

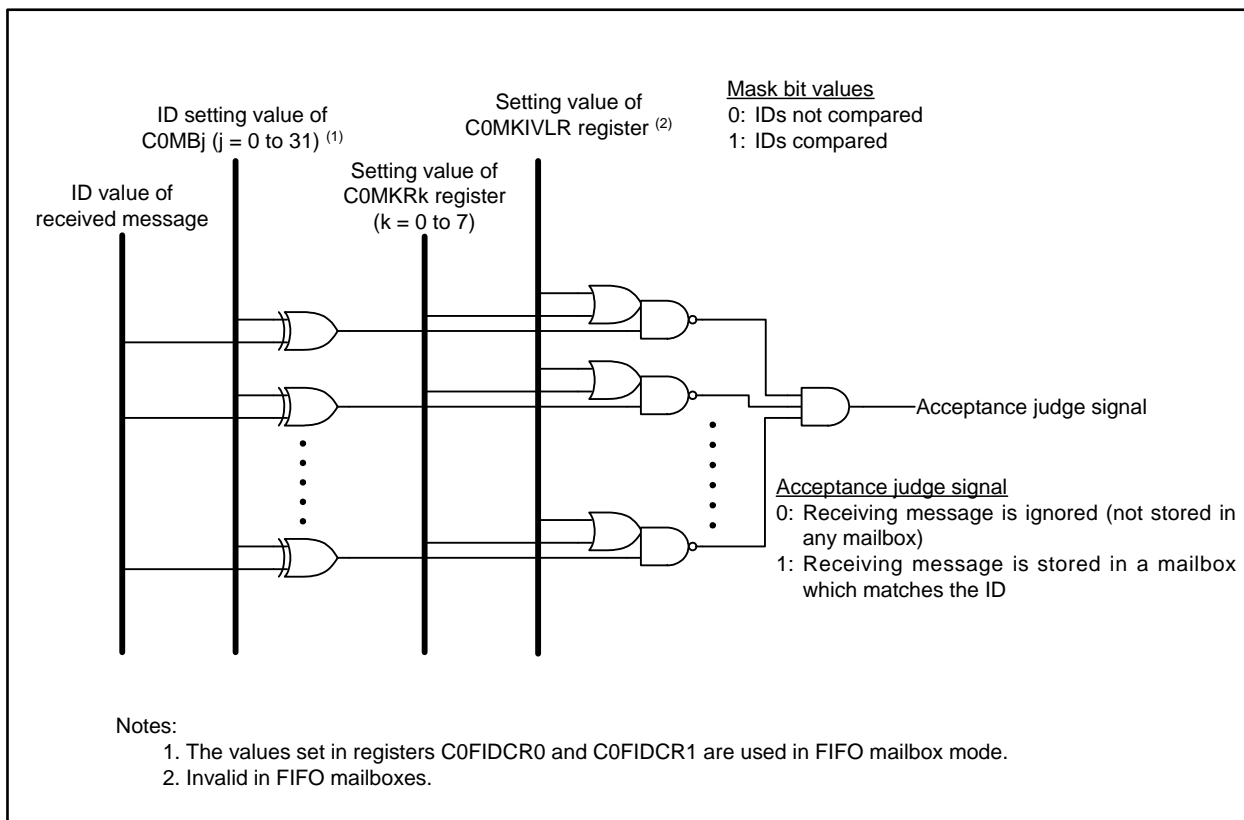


Figure 23.42 Acceptance Filtering

## 23.6 Reception and Transmission

Table 23.11 list the CAN communication mode configuration.

**Table 23.11 Configuration for CAN Reception Mode and Transmission Mode**

TRMREQ	RECREQ	ONESHOT	Communication Mode of Mailbox
0	0	0	Mailbox disabled or transmission being aborted.
0	0	1	Configurable only when transmission or reception from a mailbox (programmed in one-shot mode) is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

TRMREQ, RECREQ, ONESHOT: Bits in the COMCTLj register (j = 0 to 31)

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

- (1) Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set the COMCTLj register (j = 0 to 31) to 00h.
- (2) A received message is stored into the first mailbox that matches the condition according to the result of receive mode configuration and acceptance filtering. Upon deciding a mailbox which stores the received message, the mailbox with the smaller number has higher priority.
- (3) In CAN operation mode, when a CAN module transmits a message whose ID matches with the ID/mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module may receive its transmitted data. In this case, the CAN module sends an ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

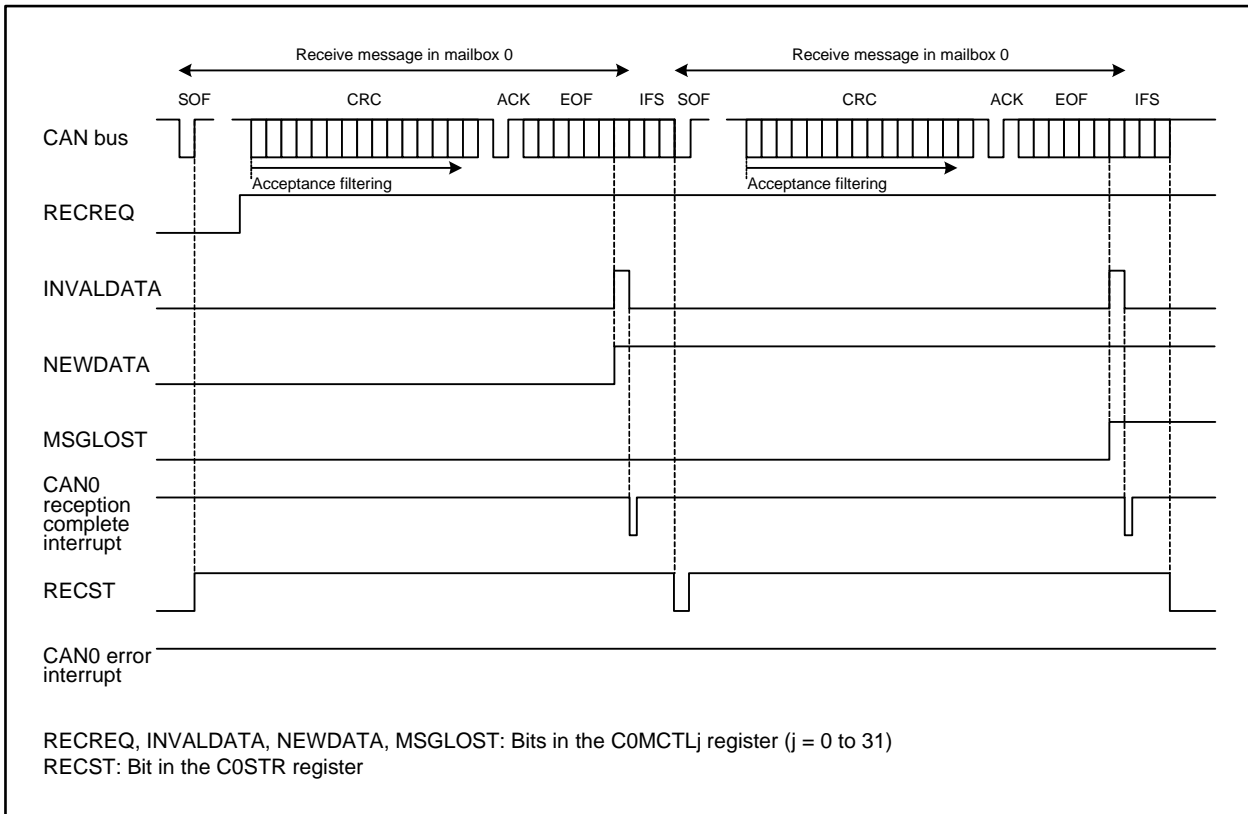
- (1) Before a mailbox is configured as a transmit mailbox or one-shot transmit mailbox, ensure that the COMCTLj register is 00h and that there is no pending abort process.



### 23.6.1 Reception

Figure 23.43 shows an operation example of data frame reception in overwrite mode.

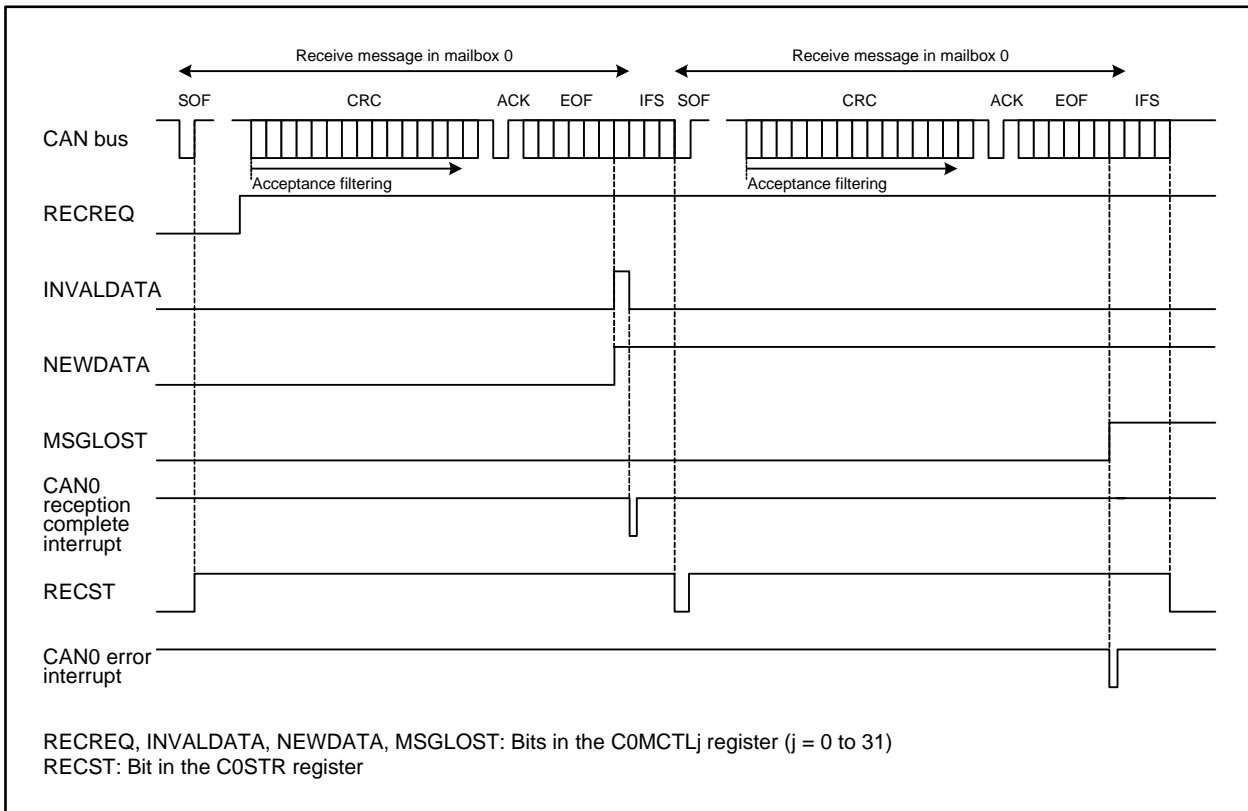
This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the COMCTL0 register.



**Figure 23.43 Operation Example of Data Frame Reception in Overwrite Mode**

- (1) When a SOF is detected on the CAN bus, the RECST bit in the C0STR register is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
- (2) The acceptance filter procedure starts at the beginning of the CRC field to select the receive mailbox.
- (3) After a message has been received, the NEWDATA bit in the COMCTLj register (j = 0 to 31) for the receive mailbox is set to 1 (new data being updated/stored in the mailbox). The INVALIDDATA bit in the COMCTLj register is set to 1 (message is being updated) at the same time, and then the INVALIDDATA bit is set to 0 (message valid) again after the complete message is transferred to the mailbox.
- (4) When the interrupt enable bit in the COMIER register for the receive mailbox is 1 (interrupt enabled), the CAN0 reception complete interrupt request is generated. This interrupt is generated when the INVALIDDATA bit is set to 0.
- (5) After reading the message from the mailbox, the NEWDATA bit needs to be set to 0 by a program.
- (6) In overwrite mode, if the next CAN message has been received into a mailbox whose NEWDATA bit is still set to 1, the MSGLOST bit in the COMCTLj register is set to 1 (message has been overwritten). The new received message is transferred to the mailbox. The CAN0 reception complete interrupt request is generated the same as in (4).

Figure 23.44 shows the operational example of data frame reception in overrun mode. This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the C0MCTL0 register.



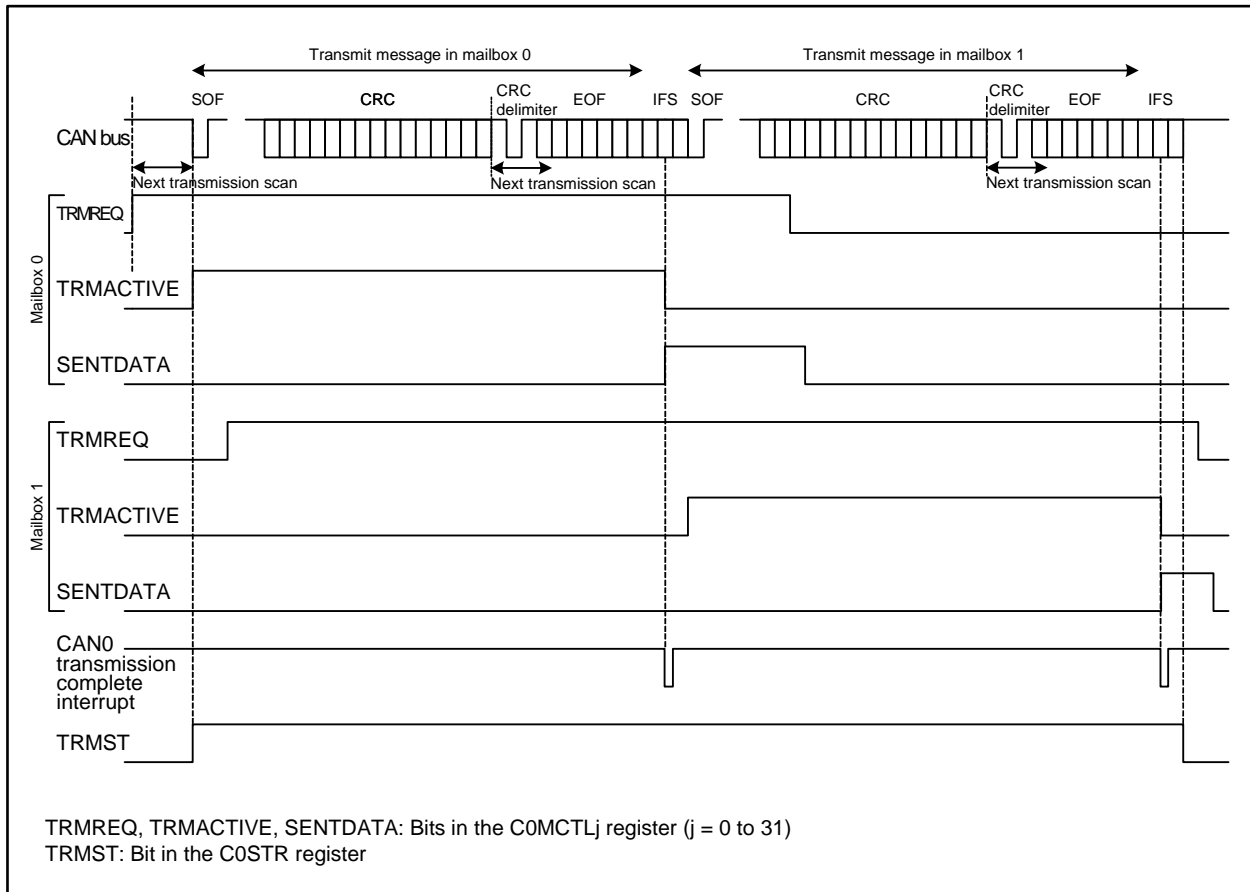
**Figure 23.44 Operation Example of Data Frame Reception in Overrun Mode**

(1) to (5) are the same as overwrite mode.

(6) In overrun mode, if the next message has been received before the NEWDATA bit is set to 0, the MSGLOST bit in the C0MCTLj register (j = 0 to 31) is set to 1 (message has been overrun). The new received message is discarded and a CAN0 error interrupt request is generated if the corresponding interrupt enable bit in the C0EIER register is set to 1 (interrupt enabled).

### 23.6.2 Transmission

Figure 23.45 shows an operation example of data frame transmission. This example shows the operation of transmitting messages that has been set in registers COMCTL0 and COMCTL1.



**Figure 23.45 Operation Example of Data Frame Transmission**

- (1) When a TRMREQ bit in the COMCTLj register (j = 0 to 31) is set to 1 (transmit mailbox) in bus-idle state, the mailbox scan procedure starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in the COMCTLj register is set to 1 (from when a transmission request is received until transmission is completed, or an error/arbitration lost has occurred), the TRMST bit in the COSTR register is set to 1 (transmission in progress), and the CAN module starts transmission. (1)
- (2) If other TRMREQ bits are set, the transmission scan procedure starts with the CRC delimiter for the next transmission.
- (3) If transmission is completed without losing arbitration, the SENTDATA bit in the COMCTLj register is set to 1 (transmission completed) and the TRMACTIVE bit is set to 0 (transmission is pending, or no transmission request). If the interrupt enable bit in the COMIER register is 1 (interrupt enabled), the CAN0 transmission complete interrupt request is generated.
- (4) When requesting the next transmission from the same mailbox, set bits SENTDATA and TRMREQ to 0, then set the TRMREQ bit to 1 after checking that bits SENTDATA and TRMREQ have been set to 0.

Note:

1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to 0. The transmission scan procedure is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the loss of arbitration, the transmission scan procedure is performed again from the start of the error delimiter to search for the highest-priority transmit mailbox.

## 23.7 CAN Interrupt

The CAN module provides the following CAN interrupts:

- CAN0 reception complete interrupt
- CAN0 transmission complete interrupt
- CAN0 receive FIFO interrupt
- CAN0 transmit FIFO interrupt
- CAN0 error interrupt

There are eight types of interrupt sources for the CAN0 error interrupts. These sources can be determined by checking the COEIFR register.

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock
- CAN0 wake-up interrupt

## 24. A/D Converter

### Note

The 64-pin package has no AN0\_4 to AN0\_7 (P0\_4 to P0\_7), AN2\_0 to AN2\_3 (P1\_0 to P1\_3), AN2\_5 to AN2\_7 (P9\_5 to P9\_7).

### 24.1 Introduction

The A/D converter consists of one 10-bit successive approximation A/D converter.

Table 24.1 lists the A/D Converter Specifications and Figure 24.1 shows an A/D Converter Block Diagram.

**Table 24.1 A/D Converter Specifications**

Item	Specification
A/D conversion method	Successive approximation
Analog input voltage	0 V to AVCC (VCC)
Operating clock $\phi_{AD}$	f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, f1 divided by 12, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, or fOCO40M divided by 12
Resolution	10 bits
Integral nonlinearity error	AVCC = VREF = 5 V ±3 LSB AVCC = VREF = 3.3 V ±5 LSB
Operation modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0
Analog input pins	8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7) + 3 pins (AN3_0 to AN3_2) (80-pin package) 8 pins (AN0 to AN7) + 4 pins (AN0_0 to AN0_3) + 1 pin (AN2_4) + 3 pins (AN3_0 to AN3_2) (64-pin package)
A/D conversion start conditions	<ul style="list-style-type: none"> <li>• Software trigger The ADST bit in the ADCON0 register is set to 1 (A/D conversion start).</li> <li>• External trigger (retrigger is enabled) Input to the <math>\overline{ADTRG}</math> pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).</li> </ul>
Conversion rate per pin	Minimum 43 $\phi_{AD}$ cycles

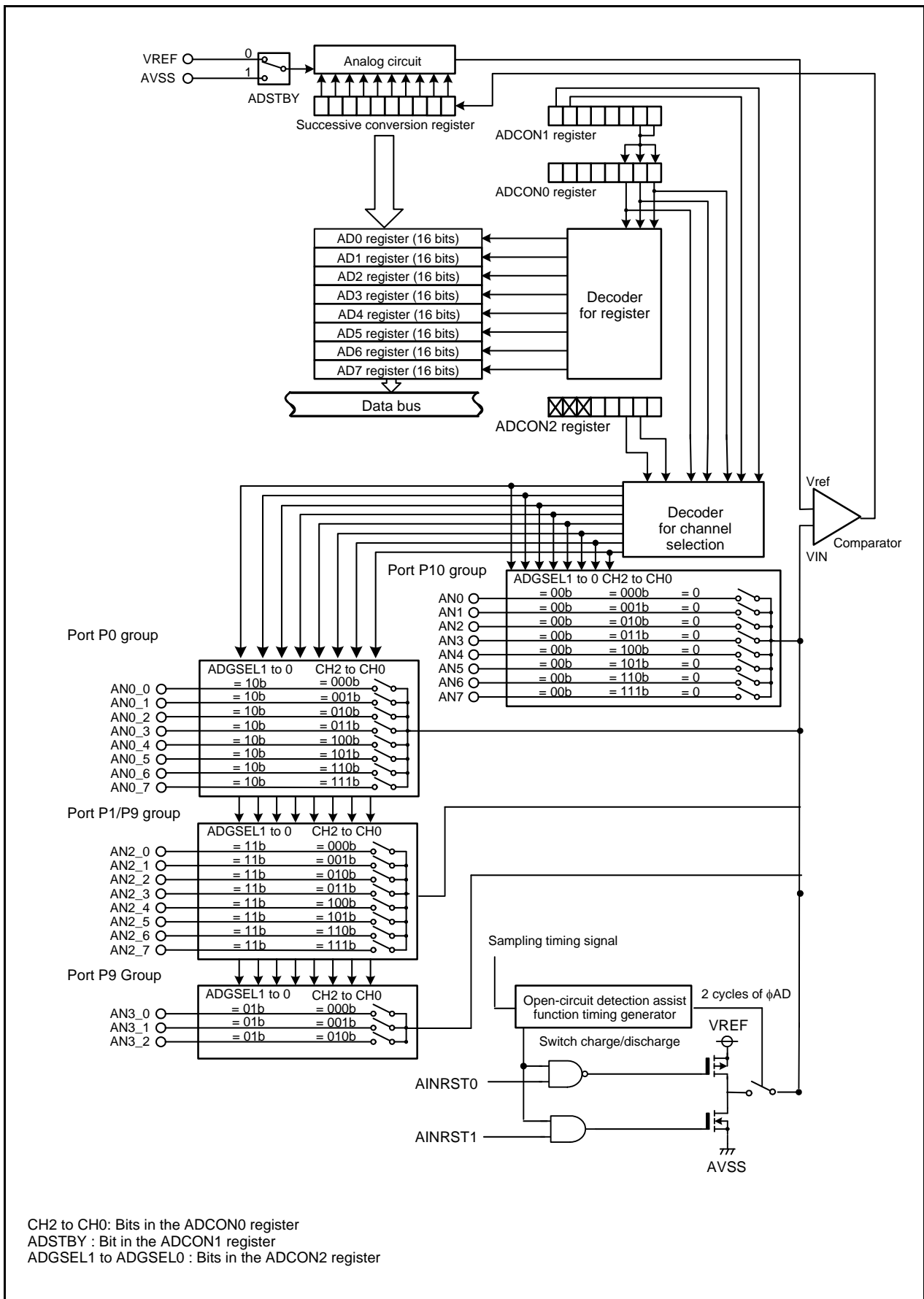


Figure 24.1 A/D Converter Block Diagram

**Table 24.2 I/O Ports**

Pin Name	I/O	Function
AN0 to AN7	Input	Analog input
AN0_0 to AN0_7	Input	Analog input
AN2_0 to AN2_7	Input	Analog input
AN3_0 to AN3_2	Input	Analog input
$\overline{\text{ADTRG}}$	Input	Trigger input

Note:

1. Set the direction bit of the ports sharing a port to 0 (input mode).

## 24.2 Registers

Table 24.3 lists registers associated with A/D converter. Set the CKS3 bit in the ADCON2 register before setting other registers associated with A/D converter. However, bits in the ADCON2 register and the CKS3 bit can be set simultaneously. After changing the CKS3 bit, set the registers in the same way again.

**Table 24.3 Registers**

Address	Register	Symbol	Reset Value
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 XXXXb
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b

### 24.2.1 Open-Circuit Detection Assist Function Register (AINRST)

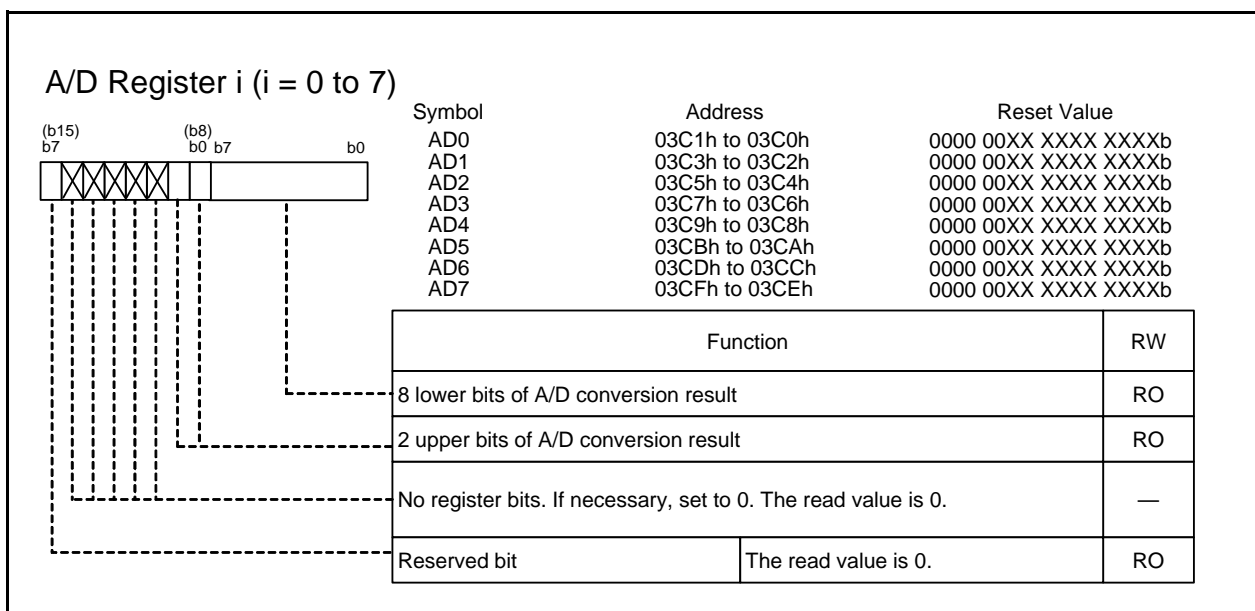
Open-Circuit Detection Assist Function Register			
	Symbol AINRST	Address 03A2h	Reset Value XX00 XXXXb
Bit Symbol	Bit Name	Function	RW
— (b3-b0)	No register bits. If necessary, set to 0. The read value is undefined.		—
AINRST0	Open-circuit detection assist function enable bit	b5 b4 0 0 : Open-circuit detection disabled 0 1 : Charge before conversion 1 0 : Discharge before conversion 1 1 : Do not set	RW
AINRST1			RW
— (b7-b6)	No register bits. If necessary, set to 0. The read value is undefined.		—

#### AINRST1-AINRST0 (Open-circuit detection assist function enable bit) (b5-b4)

To enable the A/D open-circuit detection assist function, set the AINRST0 bit or AINRST1 bit to 1, and then set the ADST bit in the ADCON0 register to 1 (A/D conversion) after waiting for one cycle of  $\phi_{AD}$ .



## 24.2.2 A/D Register i (ADi) (i = 0 to 7)

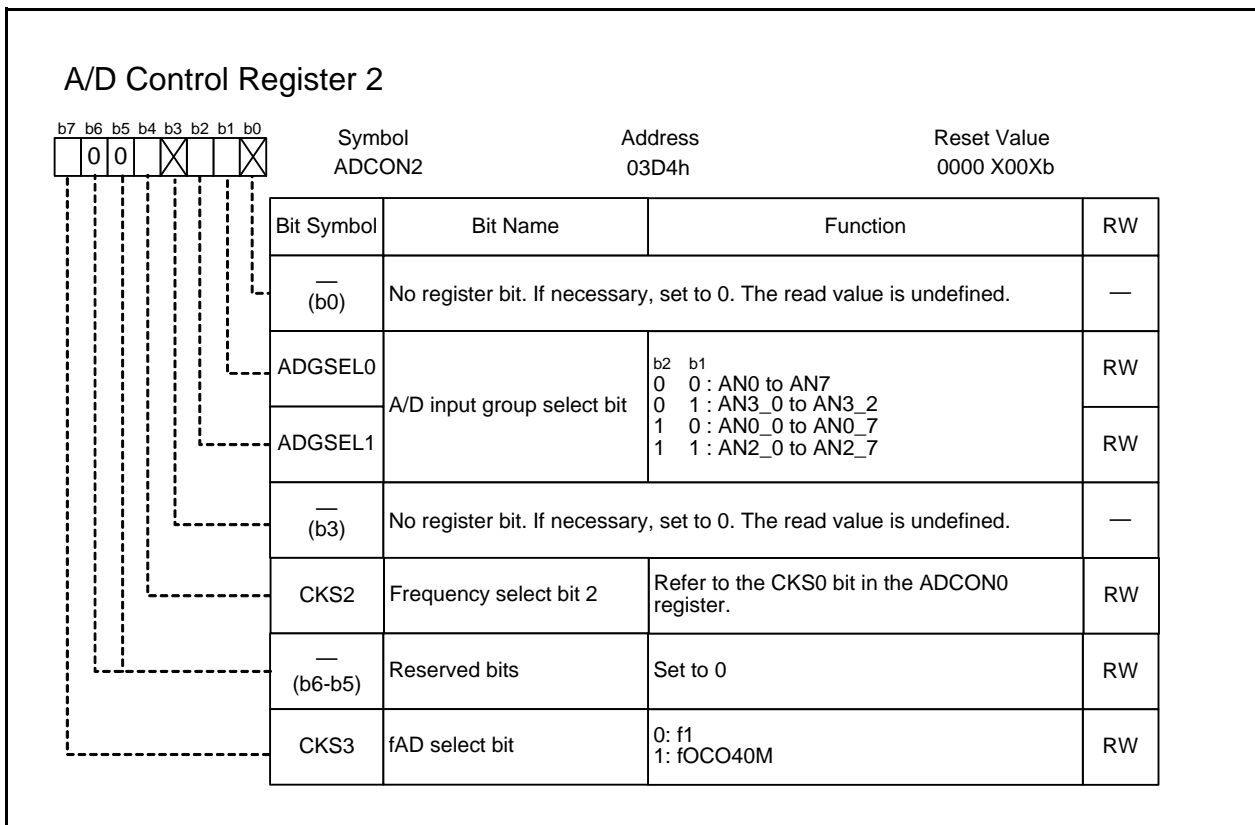


The A/D conversion result is stored in the ADi register corresponding to pins ANi, AN0\_i, AN2\_i, and AN3\_0 to AN3\_2. Read the ADi register in 16-bit units. Table 24.4 lists Analog Pin and A/D Conversion Result Storing Register.

**Table 24.4 Analog Pin and A/D Conversion Result Storing Register**

Analog Pin				A/D Conversion Result Storing Register
AN0	AN0_0	AN2_0	AN3_0	AD0 register
AN1	AN0_1	AN2_1	AN3_1	AD1 register
AN2	AN0_2	AN2_2	AN3_2	AD2 register
AN3	AN0_3	AN2_3	—	AD3 register
AN4	AN0_4	AN2_4	—	AD4 register
AN5	AN0_5	AN2_5	—	AD5 register
AN6	AN0_6	AN2_6	—	AD6 register
AN7	AN0_7	AN2_7	—	AD7 register

### 24.2.3 A/D Control Register 2 (ADCON2)



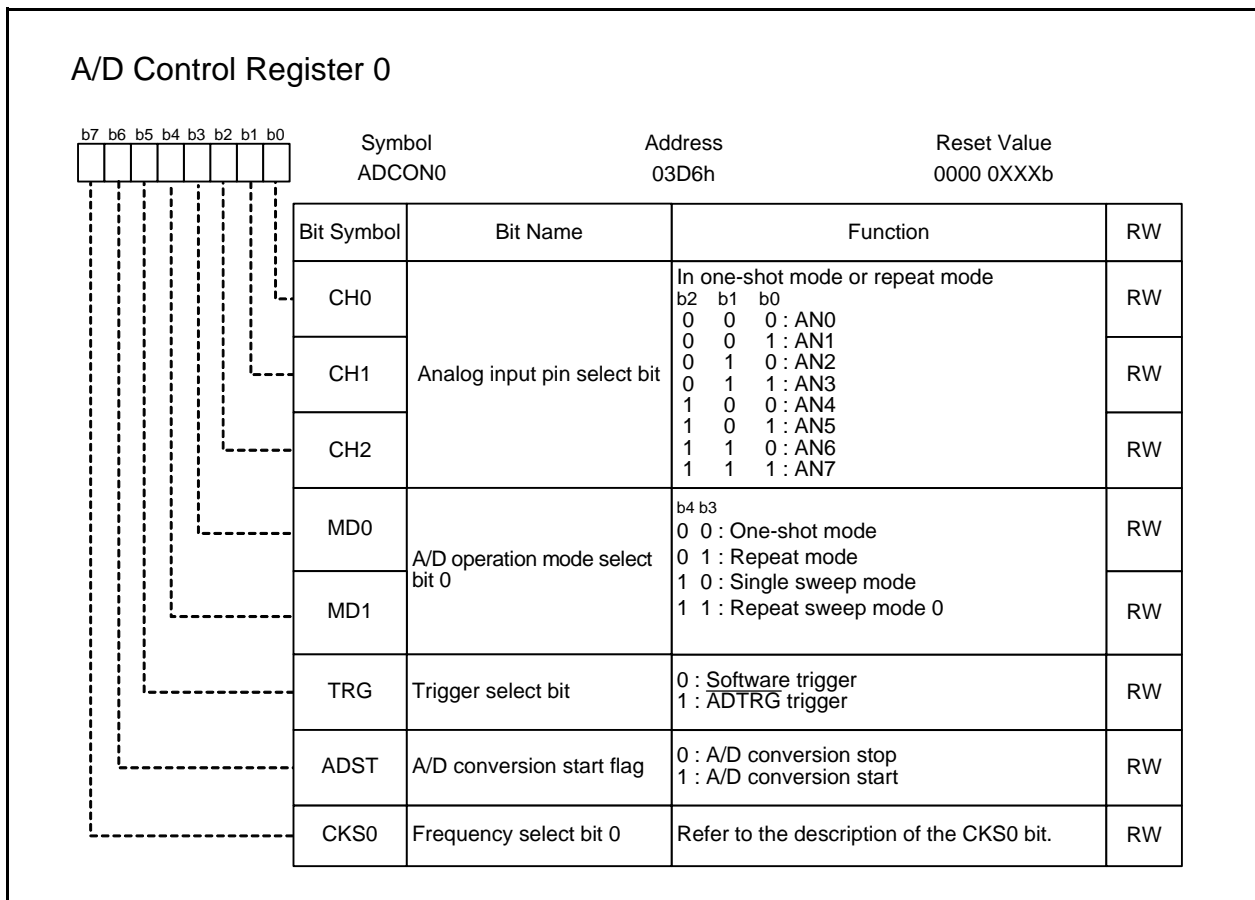
If the ADCON2 register is rewritten during A/D conversion, the conversion result is undefined.

#### CKS3 (fAD select bit) (b7)

Set the CKS3 bit while A/D conversion is stopped.

Set the CKS3 bit, and then set other A/D converter related registers. Also, after changing the CKS3 bit, set the A/D converter related registers again. Note that bits in the ADCON2 register and the CKS3 bit can be set simultaneously.

### 24.2.4 A/D Control Register 0 (ADCON0)



If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

**CKS0 (Frequency select bit 0) (b7)**

$\phi$ AD frequency is selected by a combination of the CKS0 bit in the ADCON0 register, the CKS1 bit in the ADCON1 register, and bits CKS3 and CKS2 in the ADCON2 register. Select bits CKS2 to CKS0 after setting the CKS3 bit in the ADCON2 register. Note that bits CKS3 and CKS2 can be set simultaneously. Table 24.5 lists  $\phi$ AD Frequency.

**Table 24.5**  $\phi$ AD Frequency

CKS3	CKS2	CKS1	CKS0	$\phi$ AD
0	0	0	0	fAD(f1) divided by 4
	0	0	1	fAD(f1) divided by 2
	0	1	0	fAD(f1)
	0	1	1	
	1	0	0	fAD(f1) divided by 12
	1	0	1	fAD(f1) divided by 6
	1	1	0	fAD(f1) divided by 3
	1	1	1	
1	0	0	0	fAD(fOCO40M) divided by 4
	0	0	1	fAD(fOCO40M) divided by 2
	1	0	0	fAD(fOCO40M) divided by 12
	1	0	1	fAD(fOCO40M) divided by 6
	1	1	0	fAD(fOCO40M) divided by 3
	1	1	1	

Only set the values listed above.

### 24.2.5 A/D Control Register 1 (ADCON1)

A/D Control Register 1				
		Symbol ADCON1	Address 03D7h	Reset Value 0000 X000b
Bit Symbol	Bit Name	Function	RW	
SCAN0	A/D sweep pin select bit	b1 b0 0 0: AN0 to AN1 (2 pins) 0 1: AN0 to AN3 (4 pins) 1 0: AN0 to AN5 (6 pins) 1 1: AN0 to AN7 (8 pins)	RW	
SCAN1		RW		
— (b2)	Reserved bit	Set to 0	RW	
— (b3)	No register bit. If necessary, set to 0. The read value is undefined		—	
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the registers, ADCON0 and AD1CON0	RW	
ADSTBY	A/D standby bit	0 : A/D operation stopped (standby) 1 : A/ operation enabled	RW	
— (b7-b6)	Reserved bit	Set to 0	RW	

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

#### ADSTBY (A/D standby bit) (b5)

If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for one  $\phi_{AD}$  cycle or more before starting A/D conversion.

When the A/D converter is not used, no current flows in the A/D converter by setting the ADSTBY bit to 0 (A/D operation stopped: standby). This helps reduce power consumption.

## 24.3 Operations

### 24.3.1 A/D Conversion Cycle

A/D conversion cycle is based on  $f_{AD}$  and  $\phi_{AD}$ . Divide  $f_{AD}$  so  $\phi_{AD}$  conforms the standard frequency. Figure 24.2 shows  $f_{AD}$  and  $\phi_{AD}$ .

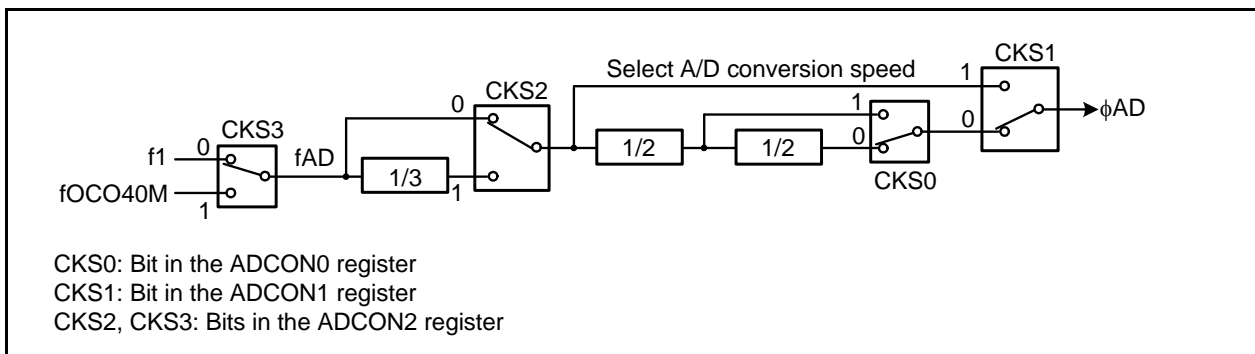


Figure 24.2  $f_{AD}$  and  $\phi_{AD}$

Figure 24.3 shows A/D Conversion Timing.

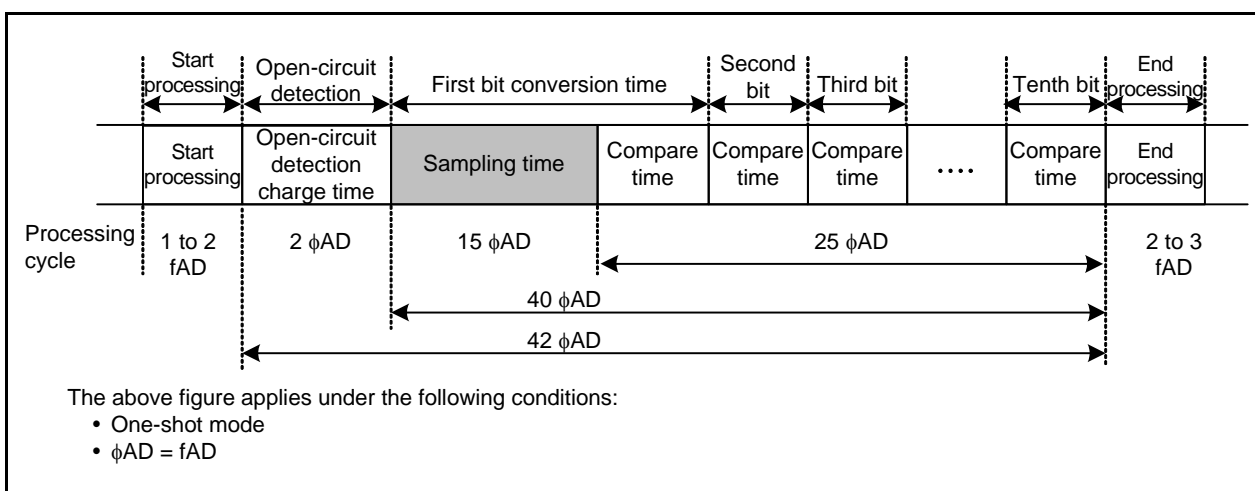


Figure 24.3 A/D Conversion Timing

Table 24.6 lists Cycles of A/D Conversion Item. A/D conversion time is described below.

Start processing time depends on which  $\phi_{AD}$  is selected.

A/D conversion starts after the start processing time elapses by setting the ADST bit in the ADCON0 register to 1 (A/D conversion start). When reading the ADST bit before starting A/D conversion, 0 (A/D conversion stop) is read.

When selecting multiple pins, or in a mode which performs A/D conversion multiple times, inter-execution processing time is inserted between A/D conversions.

In one-shot mode and single sweep mode, the ADST bit becomes 0 at the end processing time and the last A/D conversion result is stored in the ADi register.

One-shot mode:

Start processing time + A/D conversion execution time + end processing time

Two pins are selected in single sweep mode:

Start processing time + (A/D conversion execution time + inter-execution processing time + A/D conversion execution time) + end processing time

**Table 24.6 Cycles of A/D Conversion Item**

A/D Conversion Item		Number of Cycles
Start processing time	$\phi_{AD} = f_{AD}$	1 to 2 cycles of $f_{AD}$
	$\phi_{AD} = f_{AD}$ divided by 2	2 to 3 cycles of $f_{AD}$
	$\phi_{AD} = f_{AD}$ divided by 3	3 to 4 cycles of $f_{AD}$
	$\phi_{AD} = f_{AD}$ divided by 4	3 to 4 cycles of $f_{AD}$
	$\phi_{AD} = f_{AD}$ divided by 6	4 to 5 cycles of $f_{AD}$
	$\phi_{AD} = f_{AD}$ divided by 12	7 to 8 cycles of $f_{AD}$
A/D conversion execution time	Open-circuit detection disabled	40 cycles of $\phi_{AD}$
	Open-circuit detection enabled	42 cycles of $\phi_{AD}$
Inter-execution processing time		1 cycle of $\phi_{AD}$
End processing time		2 to 3 cycles of $f_{AD}$

### 24.3.2 A/D Conversion Start Conditions

An A/D conversion start trigger has a software trigger and an external trigger. Figure 24.4 shows A/D Conversion Start Trigger.

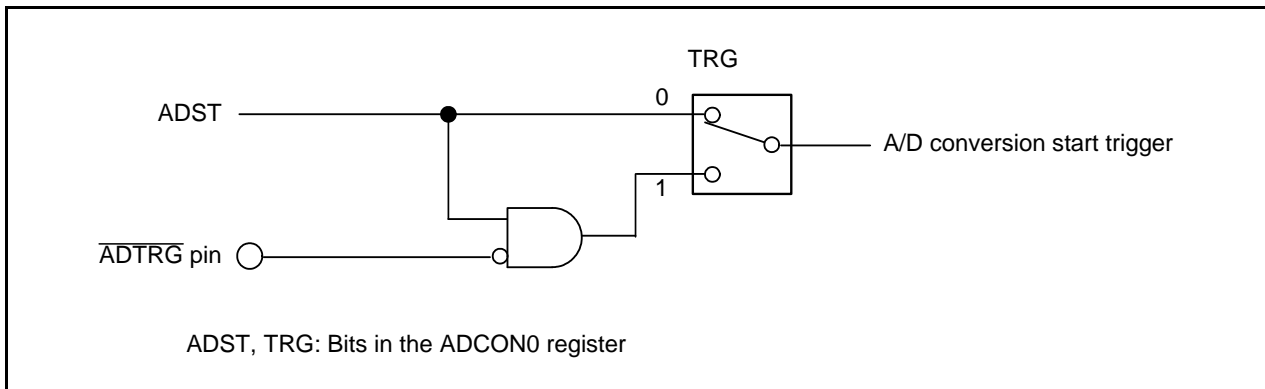


Figure 24.4 A/D Conversion Start Trigger

#### 24.3.2.1 Software Trigger

The software trigger is enabled when the TRG bit in the ADCON0 register is 0 (software trigger). A/D conversion starts by setting the ADST bit in the ADCON0 register to 1 (A/D conversion start).

#### 24.3.2.2 External Trigger

The external trigger is enabled when the TRG bit in the ADCON0 register is 1 ( $\overline{\text{ADTRG}}$  trigger). To use this trigger, set the following:

- The direction bit of the port which shares a pin with  $\overline{\text{ADTRG}}$  is 0 (input mode).
- The TRG bit in the ADCON0 register is 1 ( $\overline{\text{ADTRG}}$  trigger).
- The ADST bit in the ADCON0 register is 1 (A/D conversion start).

Under the above conditions, when input to the  $\overline{\text{ADTRG}}$  pin is changed from high to low, A/D conversion starts.

Set the high- and low-level durations of the pulse input to the  $\overline{\text{ADTRG}}$  pin to two or more cycles of fAD.

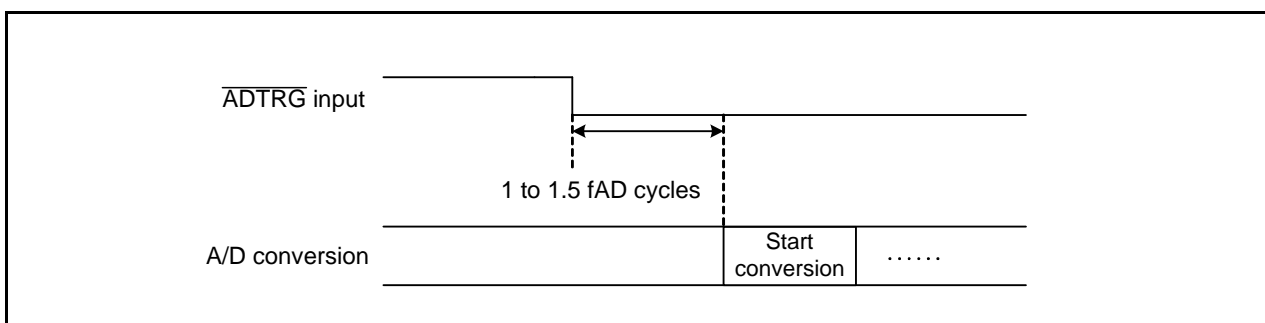


Figure 24.5 A/D Conversion Start Timing When External Trigger Input



### 24.3.3 A/D Conversion Result

When reading the ADi register before A/D conversion is completed, the undefined value is read. Read the ADi register after completing A/D conversion. Use the following procedure to detect the completion of A/D conversion.

- In one-shot mode and single sweep mode:

The IR bit in the ADIC register becomes 1 (interrupt requested) at a completion of A/D conversion. Ensure that the IR bit becomes 1 to read the ADi register.

When not using an A/D interrupt, set the IR bit to 0 (interrupt not requested) by a program after reading the ADi register.

- In repeat mode, repeat sweep mode 0:

The IR bit remains unchanged (no interrupt request is generated). At first, read the ADi register after one A/D conversion time elapses (refer to 24.3.1 "A/D Conversion Cycle"). After that, whenever the ADi register is read, the conversion result which has been obtained before reading is read.

The ADi register is overwritten after every A/D conversion. Read the value before the ADi register is overwritten.

### 24.3.4 Current Consumption Reduce Function

When the A/D converter is not in use, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stopped: standby) to shut off any analog circuit current flow.

To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for one  $\phi_{AD}$  cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion start). Do not set bits ADST and ADSTBY to 1 at the same time.

Also, do not set the ADSTBY bit to 0 (A/D operation stopped: standby) during A/D conversion.

### 24.3.5 Open-Circuit Detection Assist Function

The A/D converter has a function to set the charge of the sampling capacitor to a predefined state (AVCC or AVSS) before A/D conversion starts. This helps prevent the influence of analog input voltage from the previous conversion and more reliably detect an open-circuit of a trace connected to an analog input pin.

Figure 24.6 shows A/D Open-Circuit Detection Example on AVCC (Preconversion Charge) and Figure 24.7 shows A/D Open-Circuit Detection Example on AVSS (Preconversion discharge).

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation of the system.

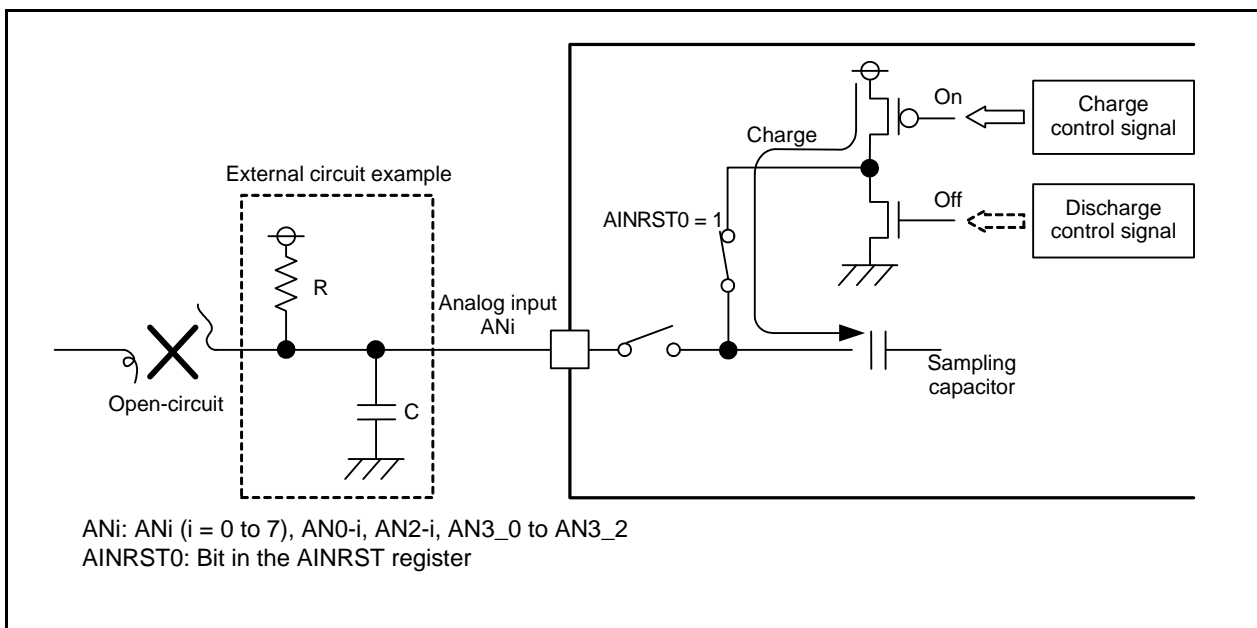


Figure 24.6 A/D Open-Circuit Detection Example on AVCC (Preconversion Charge)

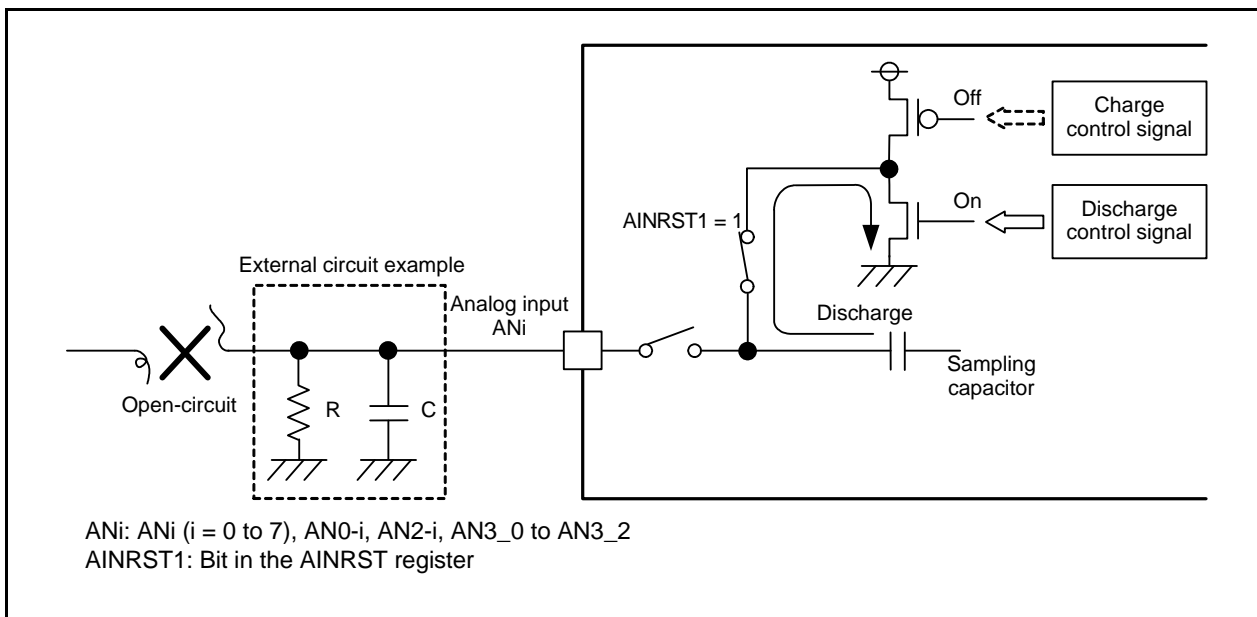


Figure 24.7 A/D Open-Circuit Detection Example on AVSS (Preconversion discharge)

## 24.4 Operational Modes

### 24.4.1 One-Shot Mode

In one-shot mode, the analog voltage applied to a selected pin is converted to a digital code once. Table 24.7 lists One-Shot Mode Specifications.

**Table 24.7 One-Shot Mode Specifications**

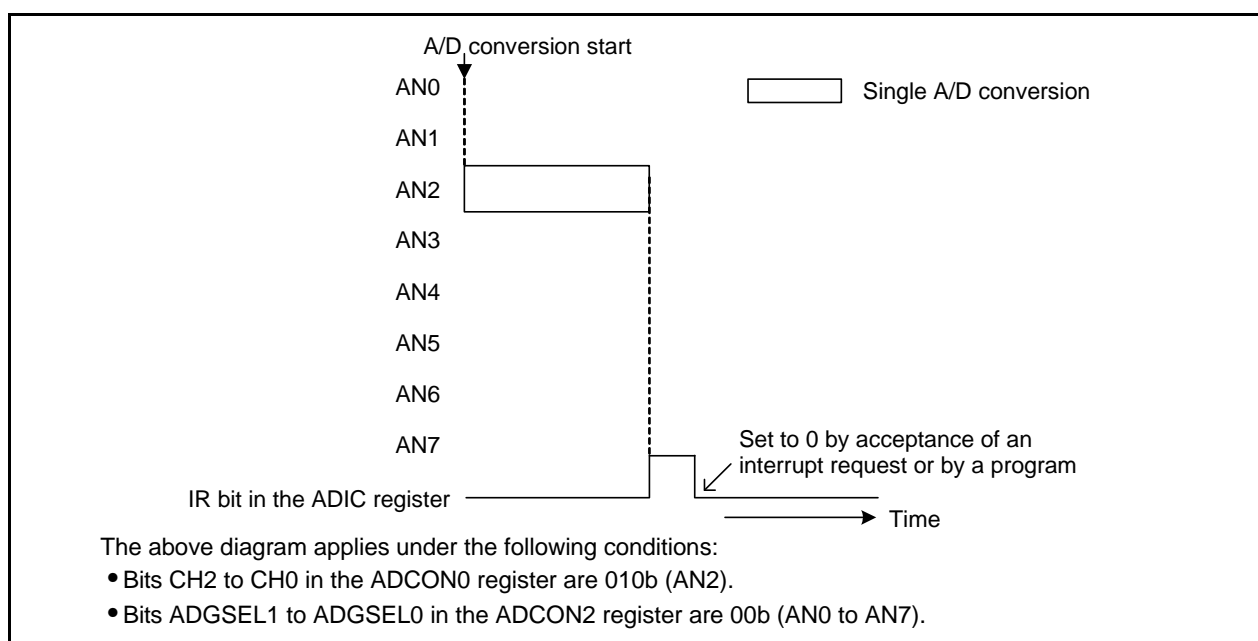
Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select a pin. The analog voltage applied to the pin is converted to a digital code once.
A/D conversion start conditions	<ul style="list-style-type: none"> <li>• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).</li> <li>• When the TRG bit is 1 (<math>\overline{\text{ADTRG}}</math> trigger) the input level at the <math>\overline{\text{ADTRG}}</math> pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).</li> </ul>
A/D conversion stop conditions	<ul style="list-style-type: none"> <li>• Completion of A/D conversion (if a software trigger is selected, the ADST bit becomes 0 (A/D conversion stop)).</li> <li>• Set the ADST bit to 0.</li> </ul>
Interrupt request generation timing	Completion of A/D conversion.
Analog input pin	Select one pin from AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, or AN3_0 to AN3_2.
Reading of A/D conversion result	Read the register among AD0 to AD7 that corresponds to the selected pin.

**Table 24.8 Registers and Settings in One-Shot Mode (1)**

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select $\phi$ AD frequency.
ADCON0	CH2 to CH0	Select analog input pin.
	MD1 to MD0	Set to 00b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select $\phi$ AD frequency.
ADCON1	SCAN1, SCAN0	Disabled
	CKS1	Select $\phi$ AD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:

1. This table does not describe a procedure.

**Figure 24.8 Operation Example in One-Shot Mode**

### 24.4.2 Repeat Mode

In repeat mode, the analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 24.9 lists Repeat Mode Specifications.

**Table 24.9 Repeat Mode Specifications**

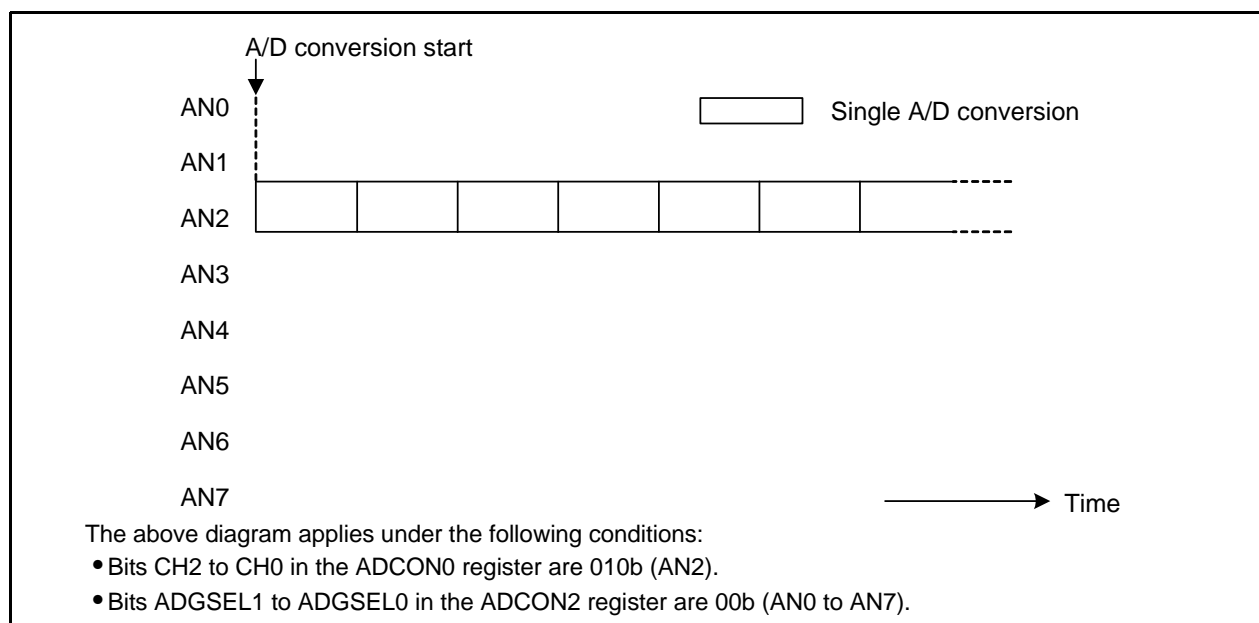
Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select a pin. The analog voltage applied to the pin is repeatedly converted to a digital code.
A/D conversion start conditions	<ul style="list-style-type: none"> <li>• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start).</li> <li>• When the TRG bit is 1 (<math>\overline{\text{ADTRG}}</math> trigger) the input level at the <math>\overline{\text{ADTRG}}</math> pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).</li> </ul>
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pin	Select one pin from among AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, or AN3_0 to AN3_2.
Reading of A/D conversion result	Read the register among AD0 to AD7 that corresponds to the selected pin.

**Table 24.10 Registers and Settings in Repeat Mode (1)**

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select $\phi$ AD frequency.
ADCON0	CH2 to CH0	Select analog input pin.
	MD1 to MD0	Set to 01b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select $\phi$ AD frequency.
ADCON1	SCAN1, SCAN0	Disabled
	CKS1	Select $\phi$ AD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:

1. This table does not describe a procedure.

**Figure 24.9 Operation Example in Repeat Mode**

### 24.4.3 Single Sweep Mode

In single sweep mode, the analog voltage applied to selected pins is converted one-by-one to a digital code. Table 24.11 lists the Single Sweep Mode Specifications.

**Table 24.11 Single Sweep Mode Specifications**

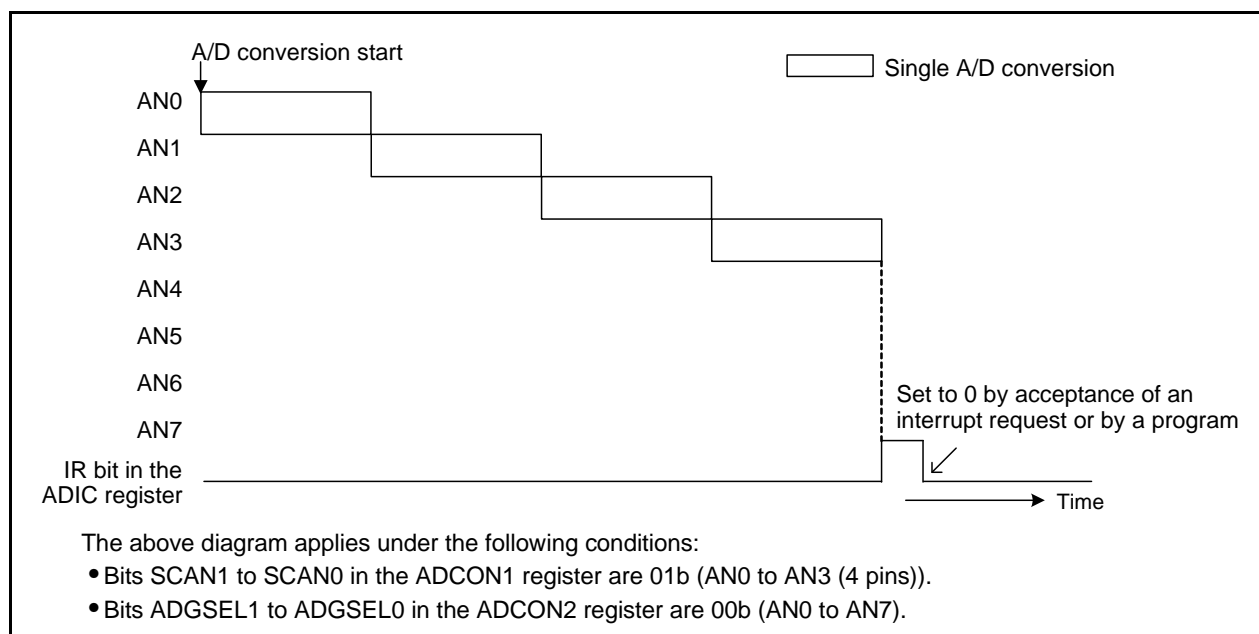
Item	Specification
Function	Bits SCAN1 to SCAN0 in the ADCON1 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select pins. The analog voltage applied to the pins is converted one-by-one to a digital code.
A/D conversion start conditions	<ul style="list-style-type: none"> <li>• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start).</li> <li>• When the TRG bit is 1 (<math>\overline{\text{ADTRG}}</math> trigger) the input level at the <math>\overline{\text{ADTRG}}</math> pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).</li> </ul>
A/D conversion stop conditions	<ul style="list-style-type: none"> <li>• Completion of A/D conversion (if a software trigger is selected, the ADST bit is set to 0 (A/D conversion stop)).</li> <li>• Set the ADST bit to 0.</li> </ul>
Interrupt request generation timing	Completion of A/D conversion
Analog input pin	Select one of the following groupings from AN0 to AN7: 2 pins: AN0 and AN1 4 pins: AN0 to AN3 6 pins: AN0 to AN5 8 pins: AN0 to AN7 AN0_0 to AN0_7, AN2_0 to AN2_7, and AN3_0 to AN3_2 can also be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that corresponds to the selected pin.

**Table 24.12 Registers and Settings in Single Sweep Mode (1)**

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select $\phi$ AD frequency.
ADCON0	CH2 to CH0	Disabled
	MD1 to MD0	Set to 10b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select $\phi$ AD frequency.
ADCON1	SCAN1, SCAN0	Select analog input pin.
	CKS1	Select $\phi$ AD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:

1. This table does not describe a procedure.

**Figure 24.10 Operation Example in Single Sweep Mode**



#### 24.4.4 Repeat Sweep Mode 0

In repeat sweep mode 0, the analog voltage applied to selected pins is repeatedly converted to a digital code. Table 24.13 lists the Repeat Sweep Mode 0 Specifications.

**Table 24.13 Repeat Sweep Mode 0 Specifications**

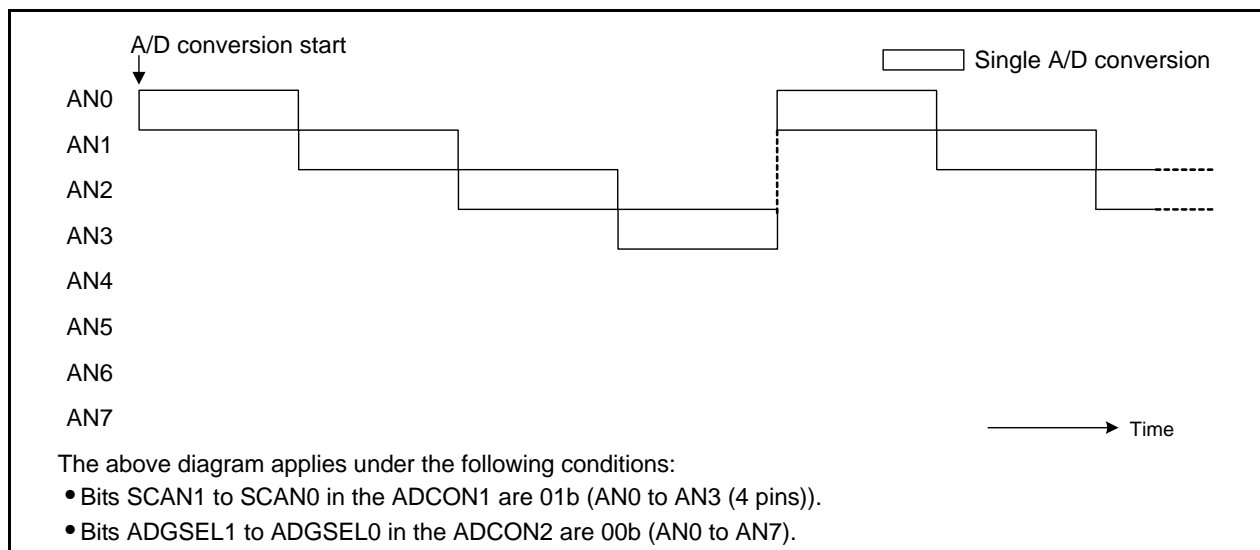
Item	Specification
Function	Bits SCAN1 to SCAN0 in the ADCON1 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select pins. Analog voltage applied to the pins is repeatedly converted to a digital code.
A/D conversion start conditions	<ul style="list-style-type: none"> <li>• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start).</li> <li>• When the TRG bit is 1 (ADTRG trigger) the input level at the ADTRG pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).</li> </ul>
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pin	Select one of the following groupings from AN0 to AN7: 2 pins: AN0 and AN1 4 pins: AN0 to AN3 6 pins: AN0 to AN5 8 pins: AN0 to AN7 AN0_0 to AN0_7, AN2_0 to AN2_7, and AN3_0 to AN3_2 can also be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that correspond to the selected pins.

**Table 24.14 Registers and Settings in Repeat Sweep Mode 0 (1)**

Register	Bit	Setting
AINRST	AINRST1, AINRST0	Select whether open-circuit detection assist function is used or not.
AD0 to AD7	b9 to b0	A/D conversion result can be read.
ADCON2	ADGSEL1, ADGSEL0	Select analog input pin group.
	CKS2	Select $\phi$ AD frequency.
ADCON0	CH2 to CH0	Disabled
	MD1 to MD0	Set to 11b.
	TRG	Select a trigger.
	ADST	Set to 1 to start A/D conversion and set to 0 to stop it.
	CKS0	Select $\phi$ AD frequency.
ADCON1	SCAN1, SCAN0	Select analog input pin.
	CKS1	Select $\phi$ AD frequency.
	ADSTBY	Set to 1 when performing A/D conversion.

Note:

1. This table does not describe a procedure.



**Figure 24.11 Operation Example in Repeat Sweep Mode 0**

## 24.5 External Sensor

To perform A/D conversion accurately, charging the internal capacitor C shown in Figure 24.12 must be completed within a specified period of time.

T: Specified period of time (sampling time)

R0: Output impedance of sensor equivalent circuit

R: Internal resistance of the MCU

X: Precision (error) of the A/D converter

Y: Resolution of the A/D converter by Y (Y is 1024)

$$\text{Generally, } VC = VIN \left\{ 1 - e^{-\frac{1}{C(R0+R)}t} \right\}$$

$$\text{When } t = T, VC = VIN - \frac{X}{Y}VIN = VIN \left( 1 - \frac{X}{Y} \right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln \frac{X}{Y}$$

$$\text{Therefore, } R0 = -\frac{T}{C \cdot \ln \frac{X}{Y}} - R$$

Figure 24.12 shows Analog Input Pin and External Sensor Equivalent Circuit. Impedance R0 by which voltage VC between pins of the capacitor C changes from 0 to VIN - (0.1/1024)VIN in time T when the difference between VIN and VC is 0.1LSB is obtained. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is kept to 0.1LSB in A/D conversion. However, the actual error is the value of absolute accuracy added to 0.1LSB.

When  $\phi_{AD}$  is 20 MHz, T is 0.75  $\mu$ s. Output impedance R0 for charging capacitor C sufficiently within time T is obtained as follows.

T = 0.75  $\mu$ s, R = 10 k $\Omega$ , C = 6.0 pF, X = 0.1, and Y = 1024. Therefore,

$$R0 = -\frac{0.75 \times 10^{-6}}{6.0 \times 10^{-12} \cdot \ln \frac{0.1}{1024}} - 10 \times 10^3 \approx 3.5 \times 10^3$$

Thus, the output impedance R0 of the sensor equivalent circuit, making the A/D converter precision (error) 0.1LSB or less, is up to 3.5 k $\Omega$ .

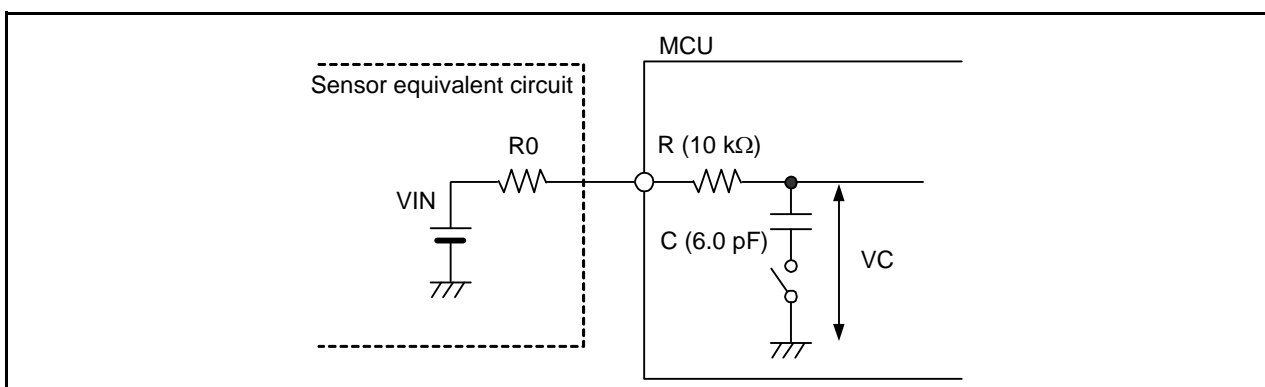


Figure 24.12 Analog Input Pin and External Sensor Equivalent Circuit

## 24.6 Interrupt

Refer to the operation examples for timing of generating interrupt requests.

Also, refer to 12.7 "Interrupt Control" for details. Table 24.15 lists Registers Associated with A/D Converter Interrupt.

**Table 24.15 Registers Associated with A/D Converter Interrupt**

Address	Register	Symbol	Reset Value
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b

## 24.7 Notes on A/D Converter

### 24.7.1 Analog Input Pin

Do not use any pin from AN4 to AN7 as analog input pin if any pin from  $\overline{KI0}$  to  $\overline{KI3}$  is used as a key input interrupt.

### 24.7.2 Pin Configuration

To prevent operation errors due to noise or latchup, and to reduce conversion errors, place capacitors between the AVSS pin and the AVCC pin, the VREF pin, and analog inputs (AN<sub>i</sub> (i = 0 to 7), AN0<sub>i</sub>, AN2<sub>i</sub>, and AN3<sub>0</sub> to AN3<sub>2</sub>). Also, place a capacitor between the VCC pin and VSS pin.

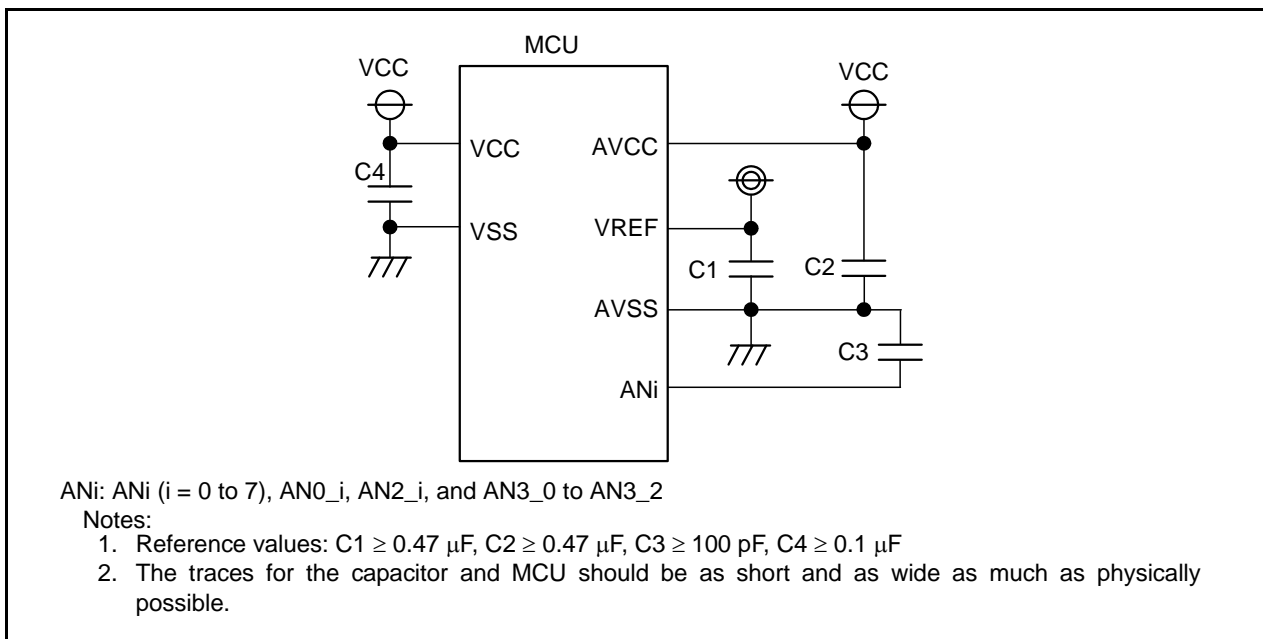


Figure 24.13 Example of Pin Configuration

### 24.7.3 Register Access

Set registers associated with A/D converter after setting the CKS3 bit in the ADCON2 register. However the other bits in the ADCON2 register and the CKS3 bit can be set at the same time. After changing the CKS3 bit, set the others in the same way.

Write registers ADCON0 (excluding the ADST bit), ADCON1, and ADCON2 when A/D conversion stops (before a trigger is generated).

After A/D conversion stops, set the ADSTBY bit in the ADCON1 register from 1 to 0.

### 24.7.4 A/D Conversion Start

When rewriting the ADSTBY bit in the ADCON1 register from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for one φ<sub>AD</sub> cycle or more before starting A/D conversion.

### 24.7.5 A/D Operation Mode Change

When the A/D operation mode has been changed, reselect analog input pins by using bits CH2 to CH0 in the ADCON0 register or bits SCAN1 to SCAN0 in the ADCON1 register.

### 24.7.6 State When Forcibly Terminated

If A/D conversion in progress is halted by setting the ADST bit in the ADCON0 register to 0 (A/D conversion stopped), the conversion result is undefined. In addition, the unconverted AD<sub>i</sub> register

( $i = 0$  to  $7$ ) may also become undefined. Do not use any value in AD $i$  registers when setting the ADST bit to 0 by a program during A/D conversion.

### 24.7.7 A/D Open-Circuit Detection Assist Function

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation of the system.

When A/D conversion starts after changing the AINRST register, follow these steps:

- (1) Change bits AINRST1 to AINRST0 in the AINRST register.
- (2) Wait for one cycle of  $\phi_{AD}$ .
- (3) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started).

### 24.7.8 Detecting Completion of A/D Conversion

In one-shot mode and single sweep mode, use the IR bit in the ADIC register to detect completion of A/D conversion. When not using an interrupt, set the IR bit to 0 by a program after detection.

When 1 is written to the ADST bit in the ADCON0 register, the ADST bit becomes 1 (A/D conversion start) after start processing time elapses (see Table 24.6 "Cycles of A/D Conversion Item"). Therefore when reading the ADST bit immediately after writing 1, 0 (A/D conversion stop) may be read.

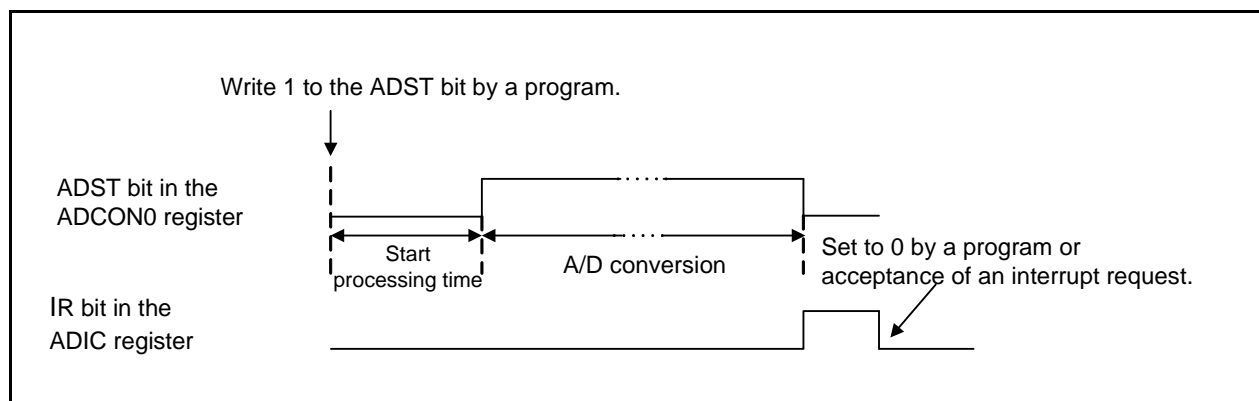


Figure 24.14 ADST Bit Operation

### 24.7.9 $\phi_{AD}$

Divide  $f_{AD}$  so  $\phi_{AD}$  conforms to the standard frequency.

In particular, consider the maximum and minimum values of  $f_{OCO40M}$  when the CKS3 bit in the ADCON2 register is 1 ( $f_{OCO40M}$  is  $f_{AD}$ ).

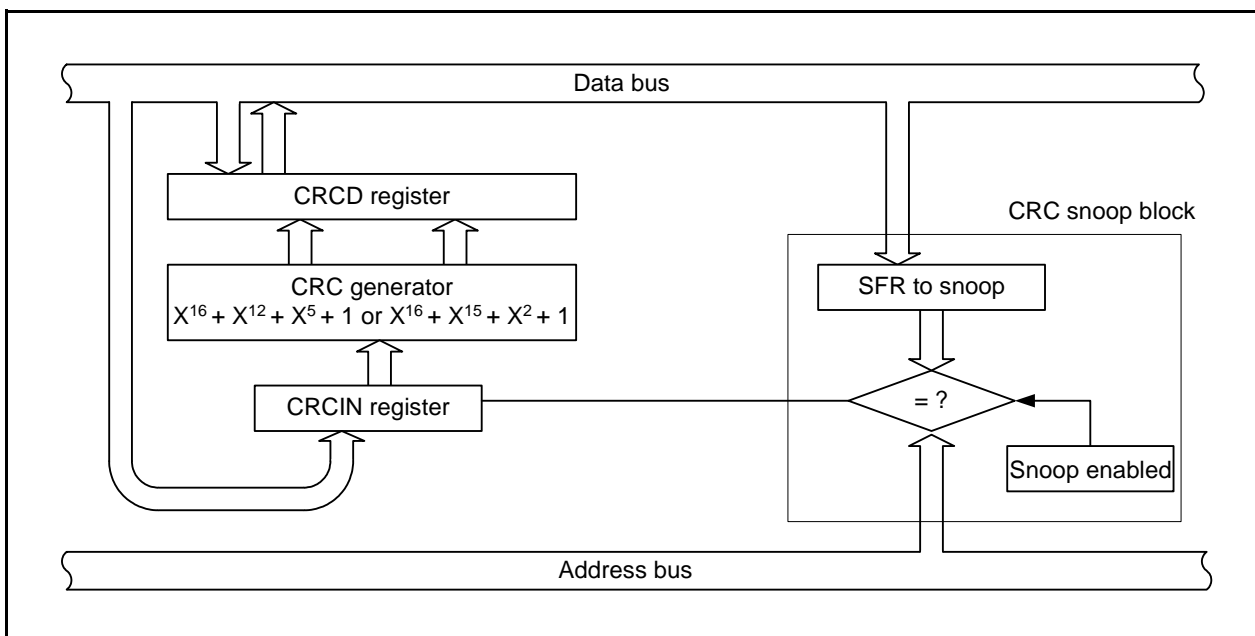
## 25. CRC Calculator

### 25.1 Introduction

The cyclic redundancy check (CRC) calculator detects errors in data blocks. This CRC calculator is enhanced by an additional feature, the CRC snoop, in order to monitor reads from and writes to a certain SFR address, and perform CRC calculations automatically on the data read from and data written to the aforementioned SFR address.

**Table 25.1 CRC Calculator Specifications**

Item	Specification
Generator polynomial	CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ ) or CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ )
Selectable functions	<ul style="list-style-type: none"> <li>• MSB/LSB selectable</li> <li>• CRC snoop</li> </ul>



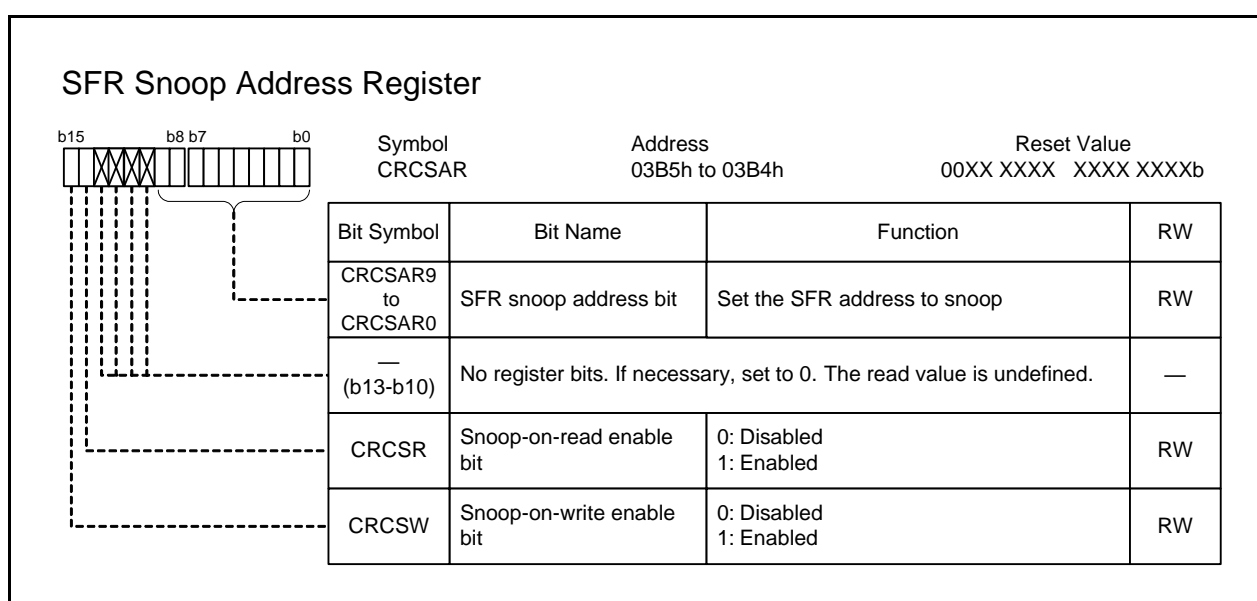
**Figure 25.1 CRC Calculator Block Diagram**

## 25.2 Registers

**Table 25.2 Registers**

Address	Register	Symbol	Reset Value
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh

### 25.2.1 SFR Snoop Address Register (CRCSAR)



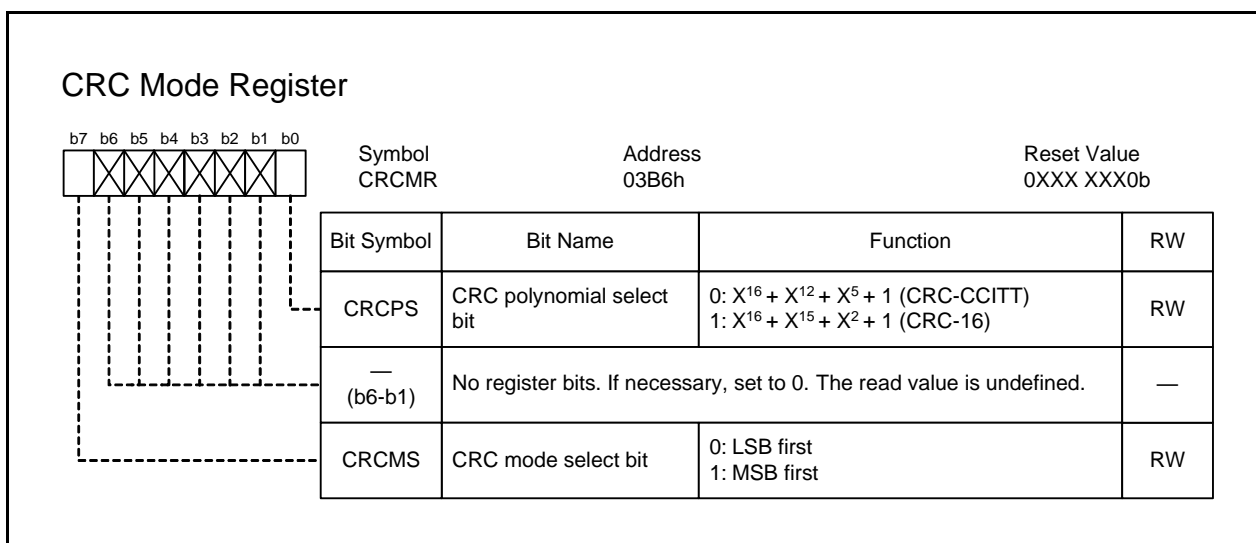
CRCSR (Snoop-on-read enable bit) (b14)

CRCSW (Snoop-on-write enable bit) (b15)

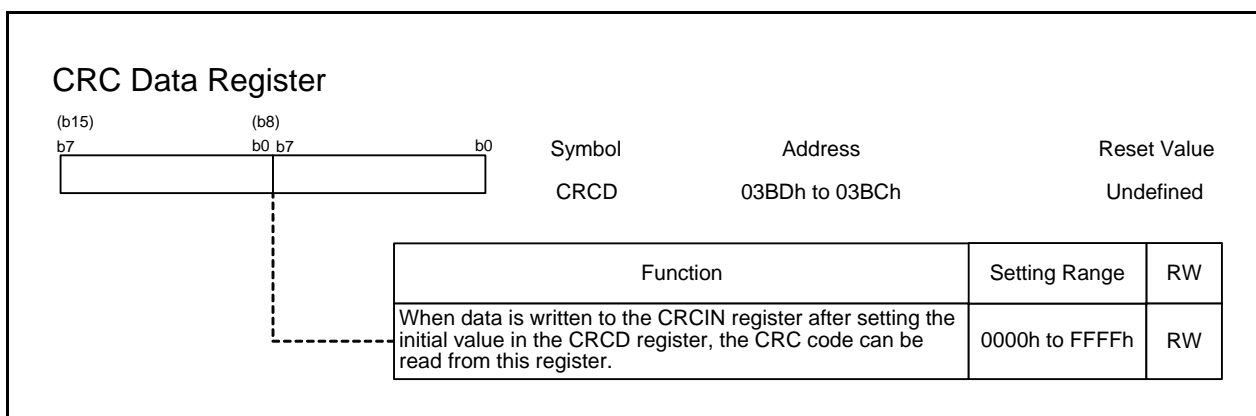
Do not set bits CRCSR and CRCSW to 1 at the same time. Set the CRCSR bit to 0 when the CRCSW bit is 1. Set the CRCSW bit to 0 when the CRCSR bit is 1.



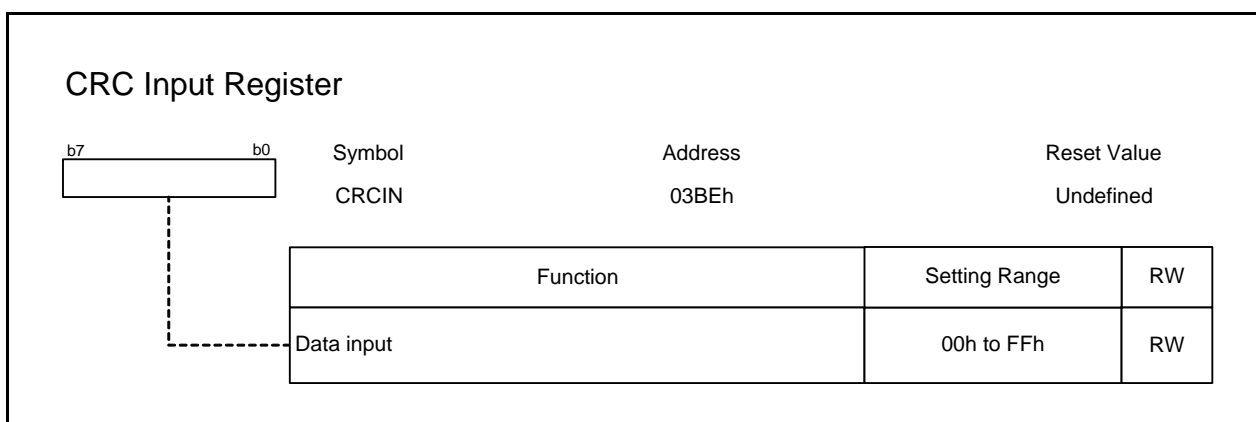
### 25.2.2 CRC Mode Register (CRCMR)



### 25.2.3 CRC Data Register (CRCD)



### 25.2.4 CRC Input Register (CRCIN)



## 25.3 Operations

### 25.3.1 Basic Operation

The CRC (Cyclic Redundancy Check) calculator detects errors in data blocks. The MCU uses two generator polynomials to generate CRC: CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ ) and CRC-16 ( $X^{16} + X^{15} + X^2 + 1$ ).

The CRC code is 16-bit code generated for a given length of a data block in 8-bit units. After setting the default value in the CRCD register, the CRC code is stored in the CRCD register every time 1-byte of data is written to the CRCIN register. CRC code generation for 1-byte data is completed in two CPU clock cycles.

### 25.3.2 CRC Snoop

The CRC snoop monitors reads from and writes to a certain SFR address and performs CRC calculation on the data read from and written to the aforementioned SFR address automatically. Because the CRC snoop recognizes writes to and reads from a certain SFR address as a trigger to automatically perform CRC calculation, there is no need to write data to the CRCIN register. All SFR addresses from 0020h to 03FFh are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the UART transmit buffer, and reads from the UART receive buffer.

To use this function, write a target SFR address to bits CRCSAR9 to CRCSAR0 in the CRCSAR register. Then, set the CRCSW bit in the CRCSAR register to 1 to enable snooping on writes to the target, or set the CRCSR bit in the CRCSAR register to 1 to enable snooping on reads from the target.

When setting the CRCSW bit to 1 and writing data to a target SFR address by CPU or DMA, the CRC calculator stores the data in the CRCIN register and performs CRC calculation. Similarly, when setting the CRCSR bit to 1 and reading data in a target SFR address by CPU or DMA, the CRC calculator stores the data in the CRCIN register and performs CRC calculation.

CRC calculation is performed 1-byte at a time. When the target SFR address is accessed in words (16 bits), CRC code is generated on the lower byte (1 byte) of data.

### CRC calculation and setting procedure to generate CRC, 80C4h, with CRC-CCITT (LSB first selected)

• CRC calculator specification

CRC: remainder of a division,  $\frac{\text{inverted value of the CRCIN register}}{\text{generator polynomial}}$

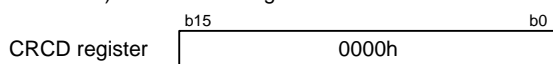
Generator polynomial:  $X^{16} + X^{12} + X^5 + 1$  (1 0001 0000 0010 0001b)

• Setting procedures

(1) Invert the bit position of the value 80C4h by a program in 1-byte units.

80h → 01h, C4h → 23h

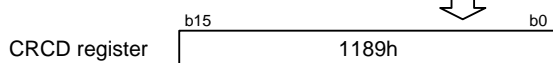
(2) Write 0000h (initial value) to the CRCD register.



(3) Write 01h (inverted value of 80h) to the CRCIN register.



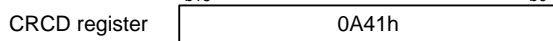
After two cycles, 1189h, which is a bit-position-inverse value of 9188h (CRC for 80h) is stored in the CRCD register.



(4) Write 23h (inverted value of C4h) to the CRCIN register.

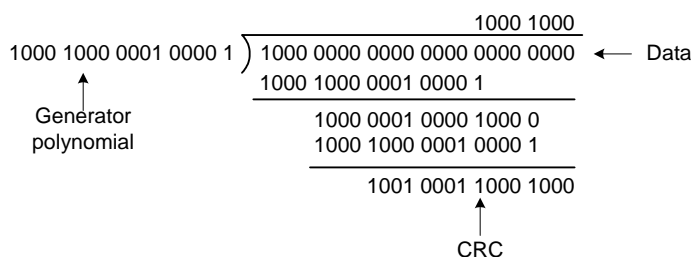


After two cycles, 0A41h, which is a bit-position-inverse value of 8250h (CRC for 80C4h) is stored in the CRCD register.



• Details on CRC calculation

As shown in (3) above, bit position of 01h (0000 0001b) written to the CRCIN register is reversed and becomes 80h (1000 0000b). Add 1000 0000 0000 0000 0000 0000b, as 1000 0000b plus 16 digits, to 0000 0000 0000 0000 0000b, as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register to perform the modulo-2 division.



Modulo-2 operation is operation that complies with the law given below.

0 + 0 = 0  
 0 + 1 = 1  
 1 + 0 = 1  
 1 + 1 = 0  
 -1 = 1

0001 0001 1000 1001b (1189h), the remainder 1001 0001 1000 1000b (9188h) with inversed bit position, can be read from the CRCD register.

When going on to (4) above, 23h (0010 0011b) written in the CRCIN register is inverted and becomes C4h (1100 0100b). Add 1100 0100 0000 0000 0000 0000b, as 1100 0100b plus 16 digits, to 1001 0001 1000 1000 0000 0000b, as 1001 0001 1000 1000b plus 8 digits as a remainder of (3) left in the CRCD register to perform the modulo-2 division. 0000 1010 0100 0001b (0A41h), the remainder 1000 0010 0101 0000b (8250h) with inversed bit position, can be read from the CRCD register.

Figure 25.2 CRC Calculation When Using CRC-CCITT

### CRC calculation and setting procedure to generate CRC, 80C4h with CRC-16 (MSB first selected)

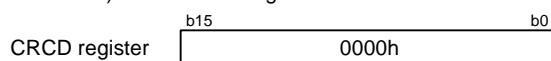
- CRC operation specification

CRC: remainder of a division,  $\frac{\text{the CRCIN register}}{\text{generator polynomial}}$

Generator polynomial:  $X^{16} + X^{15} + X^2 + 1$  (1 1000 0000 0000 0101b)

- Setting procedures

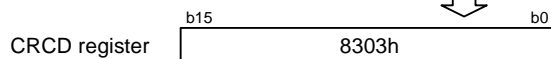
(1) Write 0000h (initial value) to the CRCD register.



(2) Write 80h to the CRCIN register.



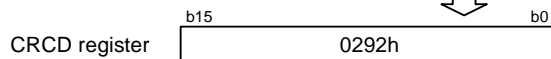
After two cycles, 8303h (CRC for 80h) is stored in the CRCD register.



(3) Write C4h to the CRCIN register.



After two cycles, 0292h (CRC for 80C4h) is stored in the CRCD register.



- Details on CRC calculation

As shown in (2) above, add 1000 0000 0000 0000 0000 0000b, as 80h (1000 0000b) written in the CRCIN register plus 16 digits, to 0000 0000 0000 0000 0000 0000b, as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register. Perform the modulo-2 division on the result. The remainder, 1000 0011 0000 0011b (8303h) can be read from the CRCD register.

When going on to (3) above, add 1100 0100 0000 0000 0000 0000b, as C4h (1100 0100b) written in the CRCIN register plus 16 digits, to 1000 0011 0000 0011 0000 0000b, as 8303h (1000 0011 0000 0011b) plus 8 digits as a remainder of (2) left in the CRCD register to perform the modulo-2 division.

The remainder, 0000 0010 1001 0010b (0292h) can be read from the CRCD register.

**Figure 25.3 CRC Calculation When Using CRC-16**

## 26. Flash Memory

### Note

Pins P0\_4 to P0\_7, P1\_0 to P1\_4, P3\_4 to P3\_7, P9\_5 to P9\_7 cannot be used in the 64-pin package. For the 64-pin package, do not use these pins for the entry of user boot function.

### 26.1 Introduction

This product uses flash memory as ROM. In this chapter, flash memory refers to the flash memory inside the MCU.

In this product, the flash memory can perform in three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

Table 26.1 lists Flash Memory Specifications (see Table 1.1 to Table 1.4 “Specifications” for the items not listed in Table 26.1).

**Table 26.1 Flash Memory Specifications**

Item		Specification
Flash memory rewrite modes		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Erase block	Program ROM 1	See Figure 26.1 “Flash Memory Block Diagram”.
	Program ROM 2	1 block (16 KB)
	Data flash	2 blocks (4 KB each)
Program method		In 2-word (4-byte) units
Erase method		Block erase
Program and erase control method		Program and erase controlled by software commands
Suspend function		Program suspend and erase suspend
Protect method		A lock bit protects each block.
Number of commands		8
Program and erase cycles	Program ROM 1 and program ROM 2	1,000 times <sup>(1)</sup>
	Data flash	10,000 times <sup>(1)</sup>
Data retention		20 years
Flash memory rewrite disable function		Parallel I/O mode ROM code protect function Standard serial I/O mode ID code check function, forced erase function, and standard serial I/O mode disable function
User boot function		User boot mode

#### Note:

1. Definition of program and erase cycles:

The program and erase cycles is the number of erase operations performed on a per-block basis. For example, assume that a 4 KB block is programmed in 1,024 operations, writing 2 words at a time, and erased thereafter. In this case, the block is considered to have been programmed and erased once.

If the program and erase cycles are 1,000 times, each block can be erased up to 1,000 times.

**Table 26.2 Flash Memory Rewrite Modes Overview**

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	The flash memory is rewritten when the CPU executes software commands. EW0 mode: Rewritable in RAM EW1 mode: Rewritable in the flash memory	The flash memory is rewritten using a dedicated serial programmer. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: 2-wire clock asynchronous serial I/O	The flash memory is rewritten using a dedicated parallel programmer.
Areas which can be rewritten	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash
CPU operating mode	Single-chip mode	Boot mode	Parallel I/O mode
ROM programmer	None	Serial programmer	Parallel programmer
On-board rewrite	Available	Available	Unavailable

## 26.2 Memory Map

The flash memory is used as ROM in this product. The flash memory is comprised of program ROM 1, program ROM 2, and data flash. Figure 26.1 shows the Flash Memory Block Diagram.

The flash memory is divided into several blocks, each of which can be protected (locked) from being programmed or erased. The flash memory can be rewritten in CPU rewrite, standard serial I/O, and parallel I/O modes.

Program ROM 2 can be used when the PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled).

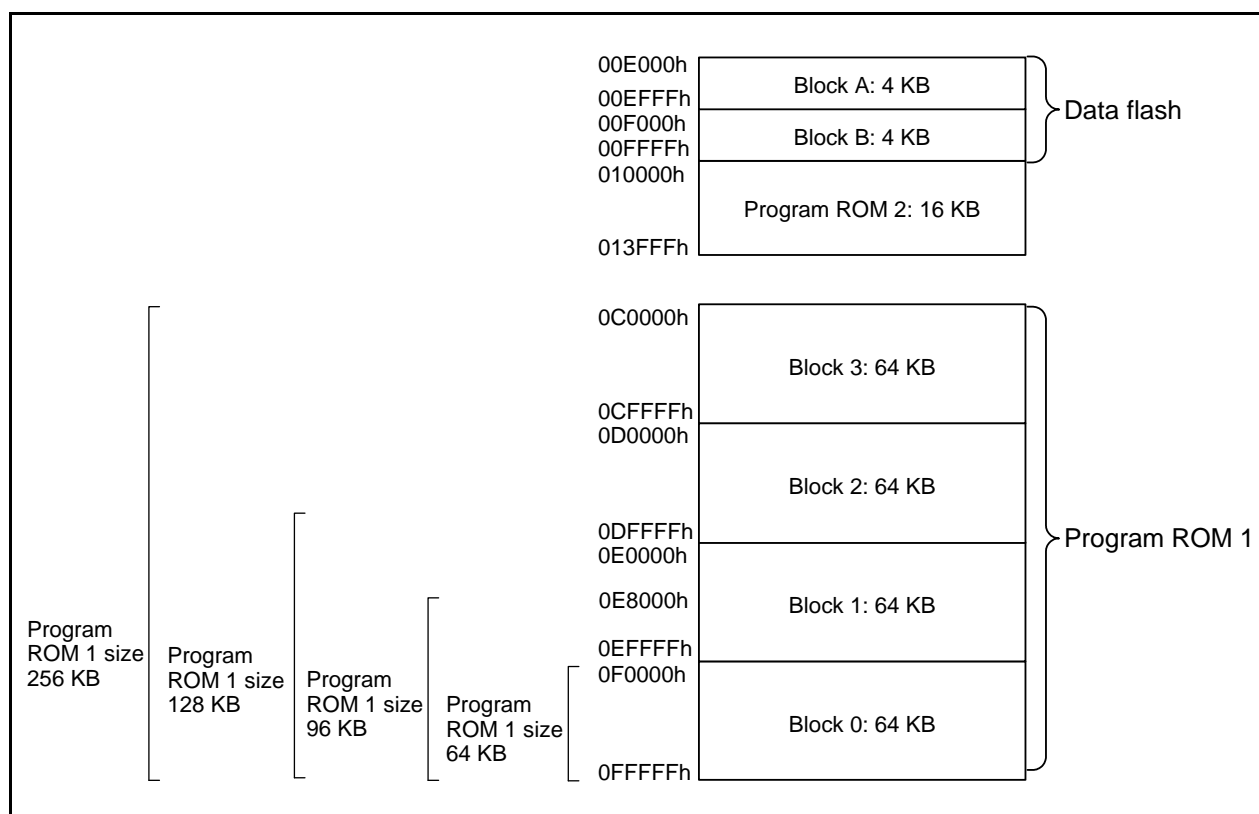
Data flash can be used when the PM10 bit in the PM1 register is set to 1 (0E000h to 0FFFFh: data flash). Data flash is divided into block A and block B.

Table 26.3 lists the differences among program ROM 1, program ROM 2, and data flash.

In single-chip mode, program can be allocated in either program ROM 1, program ROM 2, or data flash.

**Table 26.3 Program ROM 1, Program ROM 2, and Data Flash**

Item	Flash Memory		
	Program ROM 1	Program ROM 2	Data flash
Program and erase cycles	1,000 times		10,000 times
Forced erase function	Enabled		Disabled
Frequency limit when reading	No		Yes
User boot program	Do not allocate	Allocatable	Do not allocate



**Figure 26.1 Flash Memory Block Diagram**

## 26.3 Registers

**Table 26.4 Registers**

Address	Register	Symbol	Reset Value
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b

### 26.3.1 Flash Memory Control Register 0 (FMR0)

Flash Memory Control Register 0		Symbol	Address	Reset Value
		FMR0	0220h	0000 0001b (other than user boot mode) 0010 0001b (user boot mode)
Bit Symbol	Bit Name	Function	RW	
FMR00	RY/ $\overline{\text{BY}}$ status flag	0 : Busy (being written or erased) 1 : Ready	RO	
FMR01	CPU rewrite mode select bit	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW	
FMR02	Lock bit disable select bit	0 : Lock bit enabled 1 : Lock bit disabled	RW	
FMSTP	Flash memory stop bit	0 : Flash memory operation enabled 1 : Flash memory operation stopped (low power-mode, flash memory initialized)	RW	
— (b4)	Reserved bit	Set to 0	RW	
— (b5)	Reserved bit	Set to 0 in other than user boot mode Set to 1 in user boot mode	RW	
FMR06	Program status flag	0 : Completed as expected 1 : Completed in error	RO	
FMR07	Erase status flag	0 : Completed as expected 1 : Completed in error	RO	

#### FMR00 (RY/ $\overline{\text{BY}}$ status flag) (b0)

This bit indicates the flash memory operating state.

Conditions to become 0:

- When executing the following commands:  
Program, block erase, lock bit program, read lock bit status, and block blank check
- When the flash memory stops (the FMSTP bit is 1)
- During the wake up operation when the FMSTP bit is changed from 1 to 0

Condition to become 1:

- Other than those above.



### FMR01 (CPU rewrite mode select bit) (b1)

Commands can be accepted by setting the FMR01 bit to 1 (CPU rewrite mode enabled).

To set the FMR01 bit to 1, write 0 and then 1 in succession. Do not generate any interrupts or DMA transfers between setting 0 and 1.

Change the FMR01 bit when the PM24 bit in the PM2 register is 0 ( $\overline{\text{NMI}}$  interrupt disabled) or high is input to the  $\overline{\text{NMI}}$  pin.

While in EW0 mode, write to this bit from a program in RAM.

Enter read array mode, and then set this bit to 0.

### FMR02 (Lock bit disable select bit) (b2)

The lock bit is disabled by setting the FMR02 bit to 1 (lock bit disabled) (Refer to 26.8.4 “Data Protect Function”).

The FMR02 bit does not change the lock bit data, but disables the lock bit function. If an erase command is executed when the FMR02 bit is set to 1, the lock bit data status changes from 0 (locked) to 1 (unlocked) after command execution is completed.

To set the FMR02 bit to 1, write 0 and then 1 to the FMR02 bit in succession when the FMR01 bit is 1.

Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.

Do not change the FMR02 bit while programming, erasing or suspending.

### FMSTP (Flash memory stop bit) (b3)

The FMSTP bit resets the flash memory control circuits and minimizes current consumption in the flash memory. Access to the internal flash memory is disabled when the FMSTP bit is set to 1 (flash memory operation stopped). Set the FMSTP bit by a program located in RAM.

Set the FMSTP bit to 1 under the following condition:

- A flash memory access error occurs while erasing or programming in EW0 mode (the FMR00 bit does not revert to 1 (ready)).

Use the following steps to rewrite the FMSTP bit.

To stop the flash memory:

- (1) Set the FMSTP bit to 1.
- (2) Wait the wait time to stabilize the flash memory circuit (tps).

To restart the flash memory:

- (1) Set the FMSTP bit to 0.
- (2) Wait the wait time to stabilize the flash memory circuit (tps).

The FMSTP bit is enabled when the FMR01 bit is 1 (CPU rewrite mode). When the FMR01 bit is 0, although the FMSTP bit can be set to 1 by writing 1, the flash memory is neither placed in low-power mode nor initialized.

When the FMR22 bit is 1 (slow read mode enabled) or the FMR23 bit is 1 (low-current consumption read mode enabled), do not set the FMSTP bit in the FMR0 register to 1 (flash memory operation stopped). Also, when the FMSTP bit is 1, do not set the FMR22 or FMR23 bit to 1.

**FMR06 (Program status flag) (b6)**

This bit indicates the auto-program operation state.

Condition to become 0:

- Execute the clear status command.

Condition to become 1:

- Refer to 26.8.7.1 "Full Status Check".

Do not execute the following commands when the FMR06 bit is 1:

Program, block erase, lock bit program, and block blank check.

**FMR07 (Erase status flag) (b7)**

This bit indicates the auto-erase operation state.

Condition to become 0:

- Execute the clear status command

Condition to become 1:

- Refer to 26.8.7.1 "Full Status Check".

Do not execute the following commands when the FMR07 bit is 1:

Program, block erase, lock bit program, and block blank check.

### 26.3.2 Flash Memory Control Register 1 (FMR1)

Flash Memory Control Register 1			
	Symbol FMR1	Address 0221h	Reset Value 00X0 XX0Xb
Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	The read value is undefined.	RO
FMR11	Write to FMR6 register enable bit	0 : Disabled 1 : Enabled	RW
— (b3-b2)	Reserved bits	The read value is undefined.	RO
— (b4)	Reserved bit	Set to 0	RW
— (b5)	No register bit. If necessary, set to 0. The read value is undefined.		—
FMR16	Lock bit status flag	0 : Lock 1 : Unlock	RO
FMR17	Data flash wait bit	0 : 1 wait 1 : Follow the setting of the PM17 bit in the PM1 register	RW

#### FMR11 (Write to FMR6 register enable bit) (b1)

Change FMR11 bit when the PM24 bit in the PM2 register is 0 ( $\overline{\text{NMI}}$  interrupt disabled) or high is input to the  $\overline{\text{NMI}}$  pin.

#### FMR16 (Lock bit status flag) (b6)

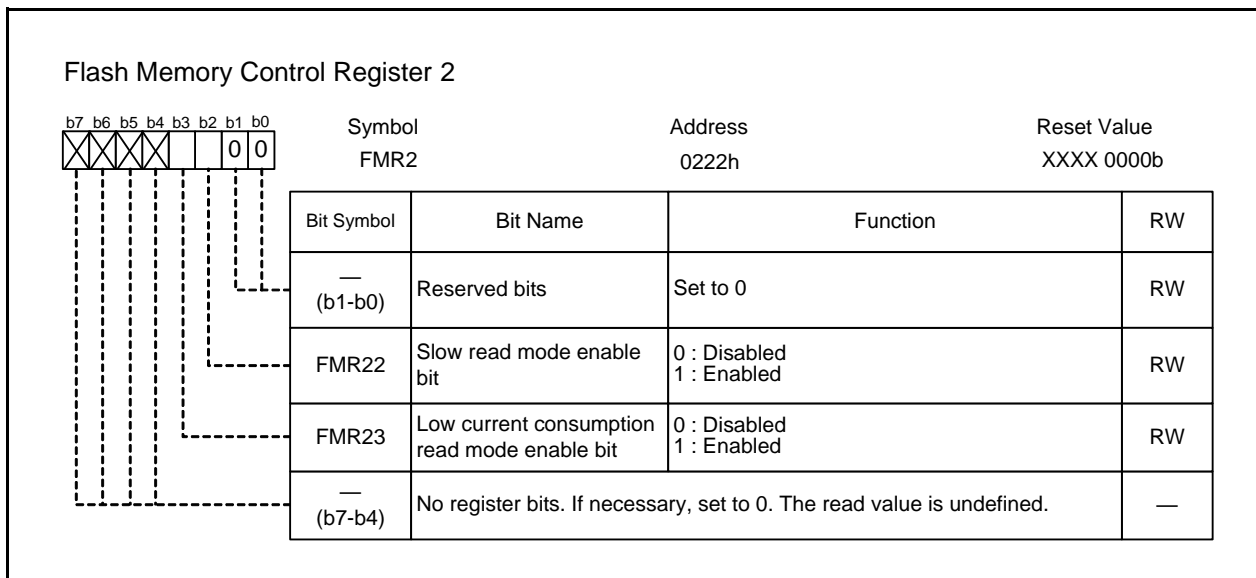
This bit indicates the execution result of the read lock bit status command.

#### FMR17 (Data flash wait bit) (b7)

This bit is used to select the number of waits for data flash.

When setting this bit to 0, one wait is inserted to the read cycle of the data flash. The write cycle is not affected.

### 26.3.3 Flash Memory Control Register 2 (FMR2)

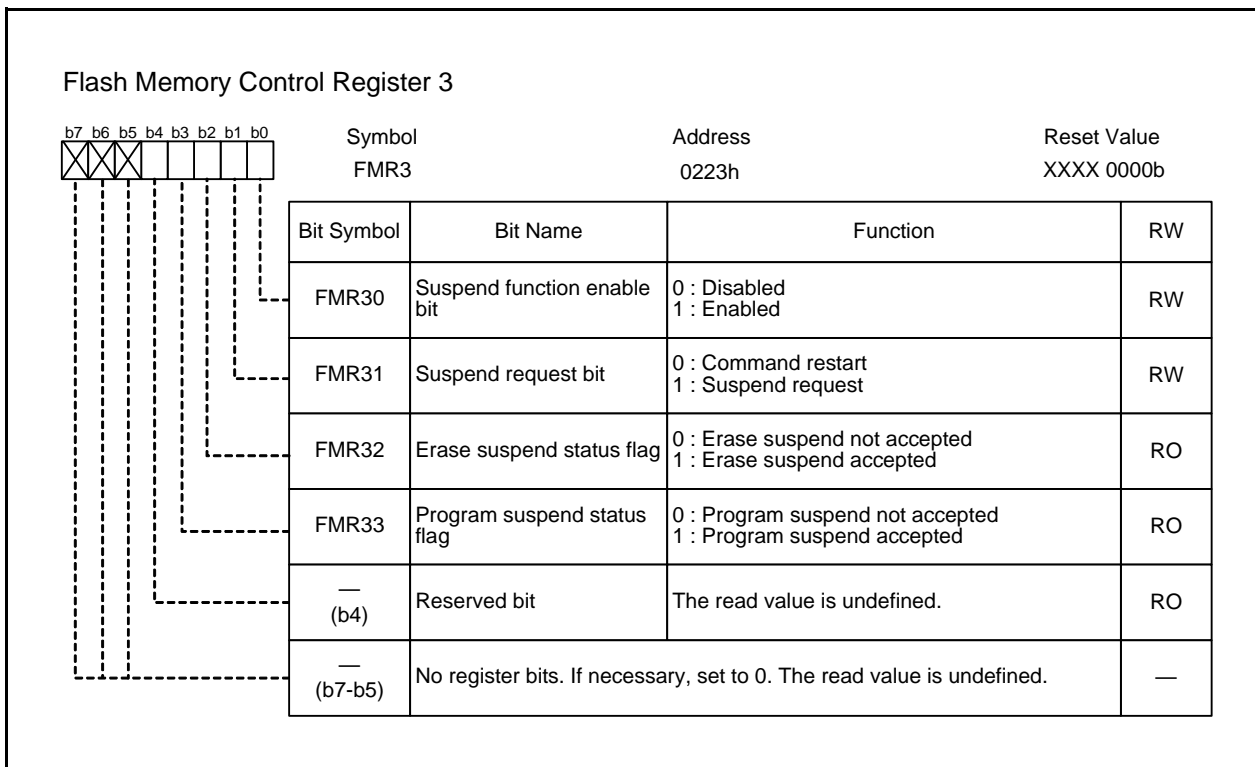


FMR22 (Slow read mode enable bit) (b2)

FMR23 (Low-current consumption read mode enable bit) (b3)

Refer to 9.4 “Power Control in Flash Memory”.

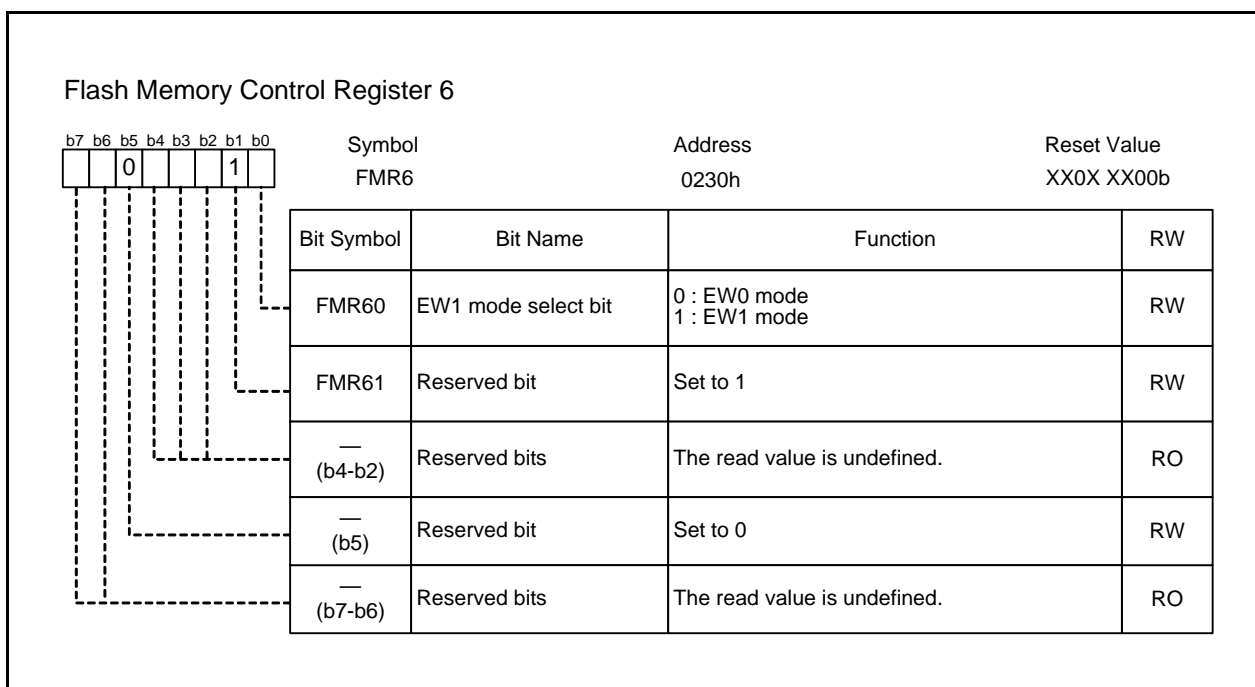
### 26.3.4 Flash Memory Control Register 3 (FMR3)



#### FMR30 (Suspend function enable bit) (b0)

To set the FMR30 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.

### 26.3.5 Flash Memory Control Register 6 (FMR6)



When accessing the FMR6 register, select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register. Also, set the PM17 bit in the PM1 register to 1 (wait state).

#### FMR60 (EW1 mode select bit) (b0)

To set the FMR60 bit to 1, write 1 when both FMR01 bit in the FMR0 register and FMR11 bit in the FMR1 register are 1.

Change the FMR60 bit when the PM24 bit in the PM2 register is 0 ( $\overline{\text{NMI}}$  interrupt disabled) or high is input to the  $\overline{\text{NMI}}$  pin. Also, change this bit when the FMR00 bit in the FMR0 register is 1 (ready).

#### FMR61 (b1)

Set the FMR61 bit to 1 when using CPU rewrite mode.

## 26.4 Optional Function Select Area

In an option function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The option function select area is not an SFR, and therefore cannot be rewritten by a program. Set an appropriate value when writing a program to the flash memory. The entire option function select area becomes FFh when the block including the option function select area is erased.

In blank products, the OFS1 and OFS2 address values are FFh when shipped. After a value is written by the user, this address takes on the written value. In programmed products, the OFS1 and OFS2 addresses are the value set in the user program prior to shipping.

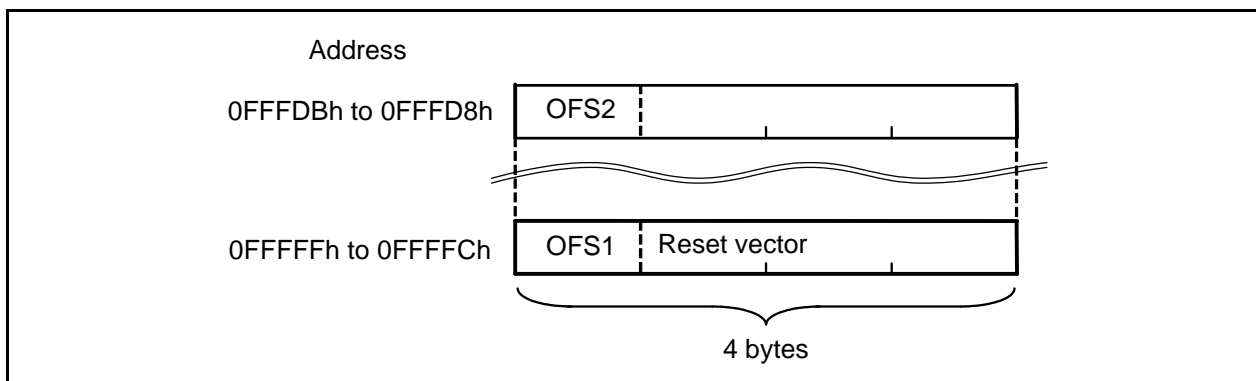
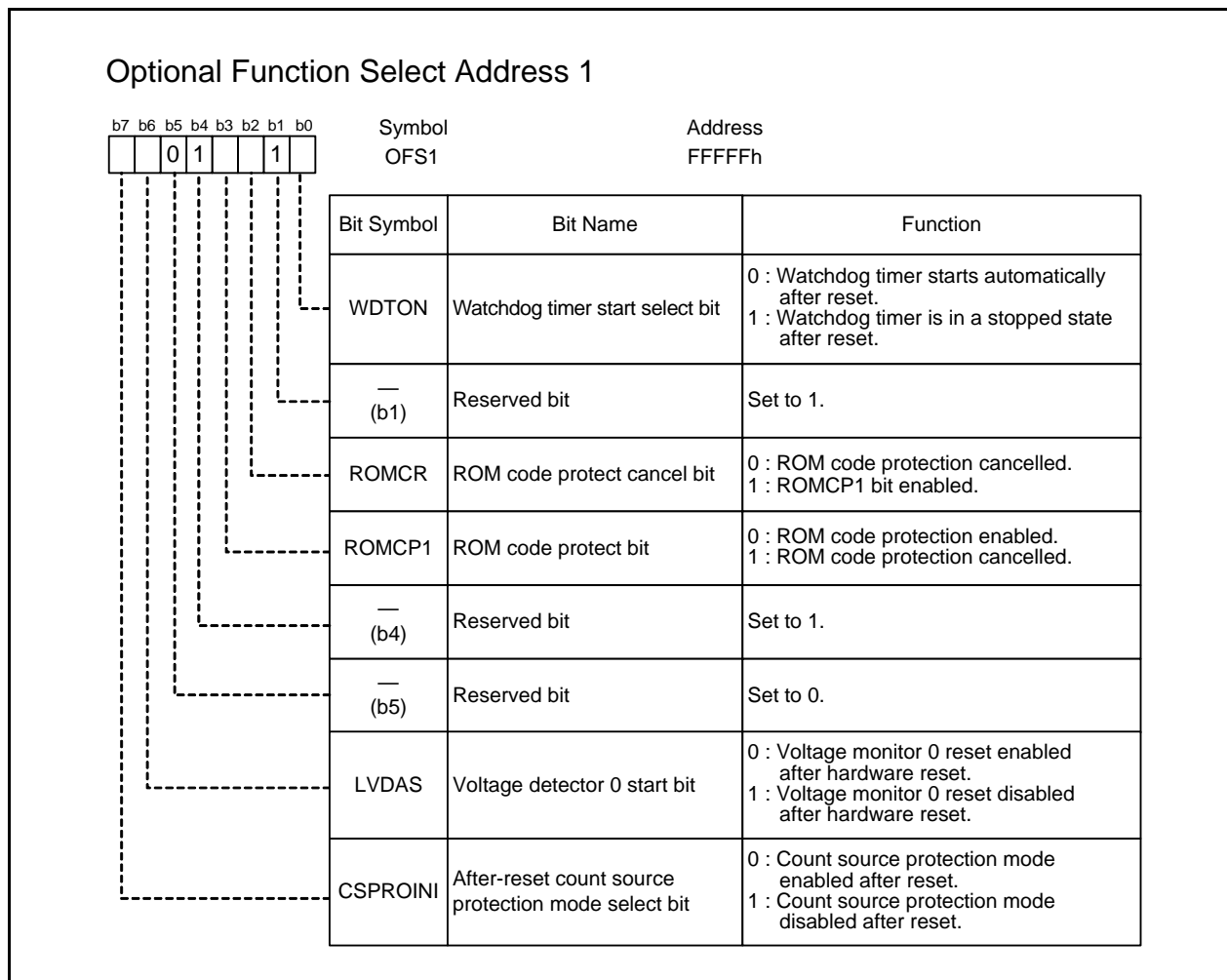


Figure 26.2 Option Function Select Area

### 26.4.1 Optional Function Select Address 1 (OFS1)



ROMCR (ROM code protect disable bit) (b2)

ROMCP1 (ROM code protect bit) (b3)

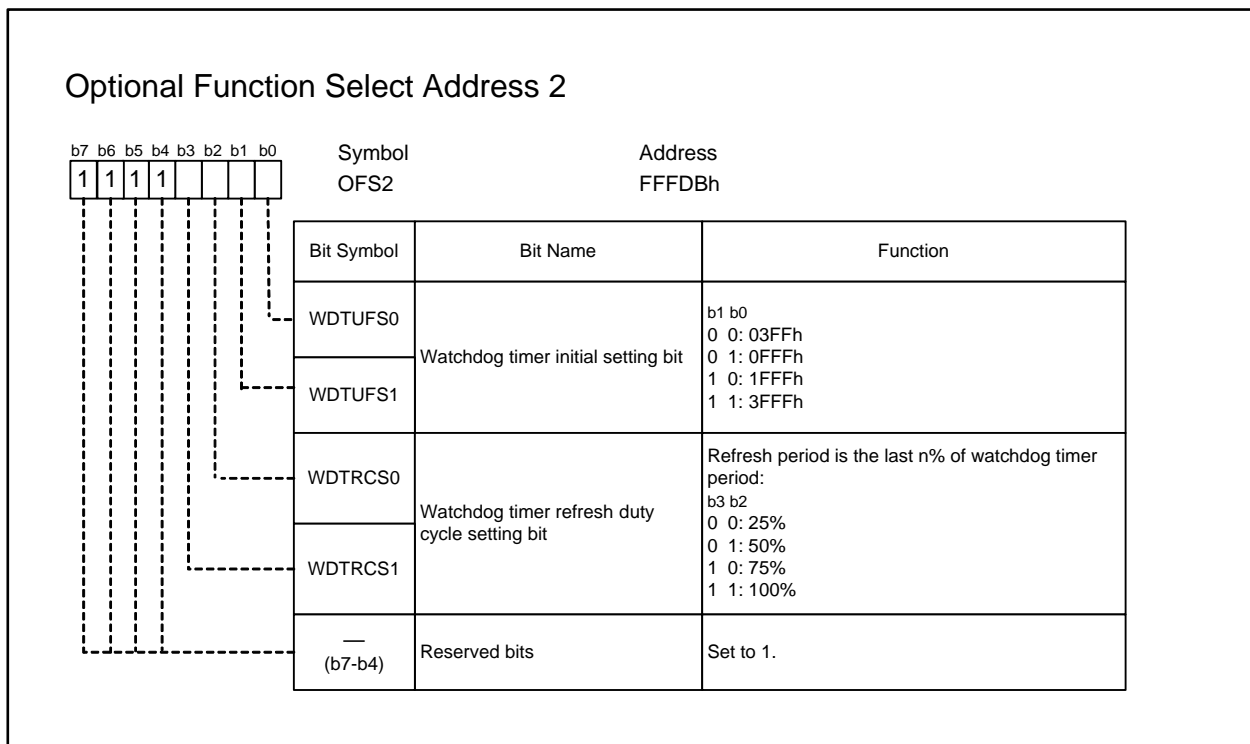
These bits are used to disable the flash memory from being read or rewritten in parallel I/O mode.

**Table 26.5 ROM Code Protect**

Bit Setting		ROM Code Protect
ROMCR bit	ROMCP1 bit	
0	0	Disabled
0	1	
1	0	Enabled
1	1	Disabled



### 26.4.2 Optional Function Select Address 2 (OFS2)



## 26.5 Flash Memory Rewrite Disable Function

This function disables the flash memory from being read, written, and erased. The following are details for each mode:

Parallel I/O mode

ROM code protect function

Standard serial I/O mode

ID code check function, forced erase function, and standard serial I/O mode disable function

## 26.6 Boot Mode

A hardware reset occurs while a high-level signal is applied to pins CNVSS. After reset, the MCU enters boot mode. In boot mode, user boot mode or standard serial I/O mode is selected in accordance with the content of the user boot code area. Refer to 26.9 "Standard Serial I/O Mode" for details.

The MCU does not enter boot mode in power-on reset and voltage monitor 0 reset.

## 26.7 User Boot Mode

This mode is used for starting the flash memory rewrite program programmed by a user.

Allocate the flash memory rewrite program to program ROM 2. In user boot mode, the program is executed from address 10000h (starting address of program ROM 2). After starting the program, the flash memory is rewritten according to the program in EW0 or EW1 mode.

### 26.7.1 User Boot Function

User boot mode can be selected by the status of a port when the MCU starts in boot mode. Table 26.6 lists the User Boot Function Specifications.

**Table 26.6 User Boot Function Specifications**

Item	Specification
Entry pin	None or select a port from P0 to P3, P6 to P10
User boot start level	Select high or low
User boot start address	Address 10000h (program ROM 2 start address)

Set "UserBoot" in ASCII code to addresses 13FF0h to 13FF7h in the user boot code area, select a port for entry from addresses 13FF8h to 13FF9h and 13FFAh, and select the start level with address 13FFBh. After starting boot mode, user boot mode or standard serial I/O mode is selected in accordance with the input level of the selected port.

In addition, if addresses 13FF0h to 13FF7h are set to "UserBoot" in ASCII code and addresses 13FF8h to 13FFBh are set to 00h, user boot mode is selected.

In user boot mode, the program of address 10000h (program ROM 2 start address) is executed.

Figure 26.3 shows the User Boot Code Area, Table 26.7 lists Start Mode (When Port Pi\_j is Selected for Entry), Table 26.8 lists "UserBoot" in ASCII Code, and Table 26.9 lists Addresses of Selectable Ports for Entry.

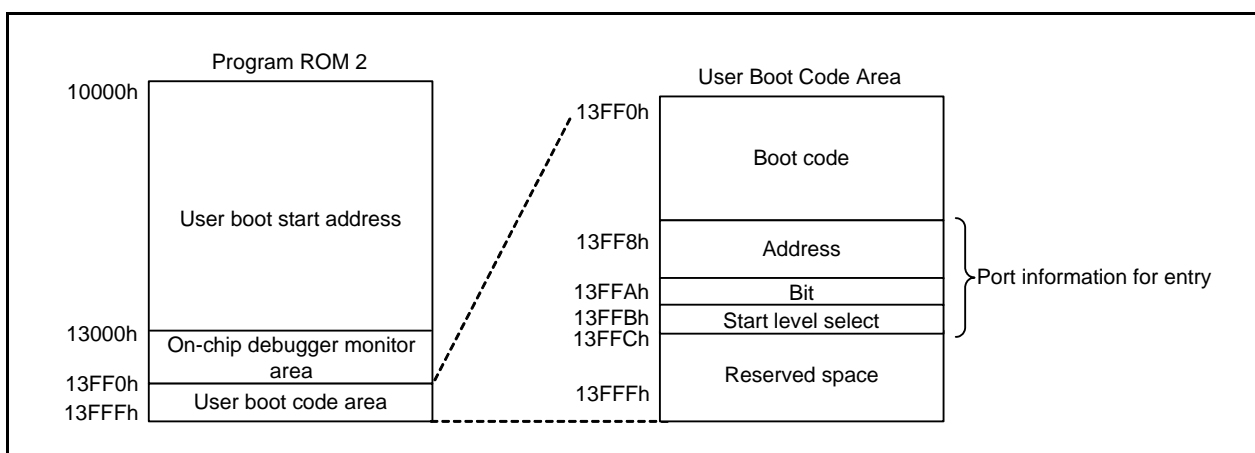


Figure 26.3 User Boot Code Area

Table 26.7 Start Mode (When Port Pi\_j is Selected for Entry) (1)

Boot Code (13FF0h to 13FF7h)	Port Information for Entry			Port Pi_j Input Level	Start Mode
	Address (13FF8h to 13FF9h)	Bit (13FFAh)	Start level select (13FFBh)		
"UserBoot" in ASCII code (2)	0000h	00h	00h	–	User boot mode
	Pi register address (3)	00h to 07h (value of j)	00h	High	Standard serial I/O mode
				Low	User boot mode
	Pi register address (3)	00h to 07h (value of j)	01h	High	User boot mode
Low				Standard serial I/O mode	
Other than "UserBoot" in ASCII code	–	–	–	–	Standard serial I/O mode

i = 0 to 3, 6 to 10; j = 0 to 7

Notes:

1. Only use the values listed in Table 26.7.
2. See Table 26.8 "UserBoot" in ASCII Code.
3. See Table 26.9 "Addresses of Selectable Ports for Entry".

Table 26.8 "UserBoot" in ASCII Code

Address	ASCII Code
13FF0h	55h (upper-case U)
13FF1h	73h (lower-case s)
13FF2h	65h (lower-case e)
13FF3h	72h (lower-case r)
13FF4h	42h (upper-case B)
13FF5h	6Fh (lower-case o)
13FF6h	6Fh (lower-case o)
13FF7h	74h (lower-case t)

**Table 26.9** Addresses of Selectable Ports for Entry

Port	Address	
	13FF9h	13FF8h
P0	03h	E0h
P1	03h	E1h
P2	03h	E4h
P3	03h	E5h
P6	03h	ECh
P7	03h	EDh
P8	03h	F0h
P9	03h	F1h
P10	03h	F4h

**Table 26.10** Example Settings of User Boot Code Area

When starting up in user boot mode while input level of the port P1\_5 is low:

Address	Setting Value	Meaning
13FF0h	55h	Upper-case U
13FF1h	73h	Lower-case s
13FF2h	65h	Lower-case e
13FF3h	72h	Lower-case r
13FF4h	42h	Upper-case B
13FF5h	6Fh	Lower-case o
13FF6h	6Fh	Lower-case o
13FF7h	74h	Lower-case t
13FF8h	E1h	Port P1_5
13FF9h	03h	
13FFAh	05h	
13FFBh	00h	Low level

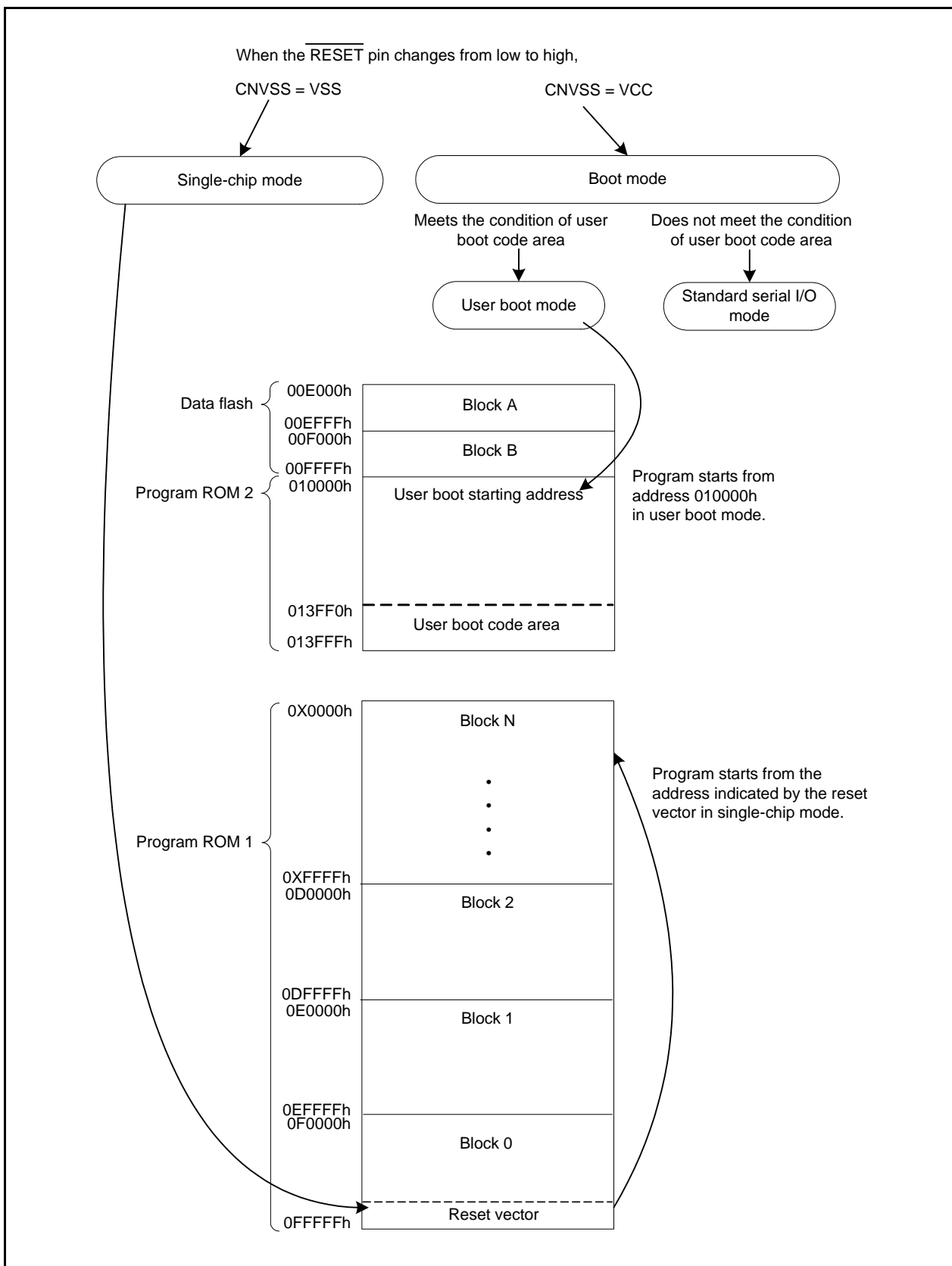


Figure 26.4 Program Starting Address in User Boot Mode

## 26.8 CPU Rewrite Mode

In CPU rewrite mode, the flash memory can be rewritten when the CPU executes software commands. Program ROM 1, program ROM 2, and data flash can be rewritten with the MCU mounted on the board and without using a ROM programmer.

The program and block erase commands are executed only in individual block areas of program ROM 1, program ROM 2, and data flash.

The flash memory has a suspend function to temporarily suspend operation when erasing or programming in CPU rewrite mode. Refer to 26.8.5 “Suspend Function” for details of the suspend function.

EW0 mode and EW1 mode are available in CPU rewrite mode. Table 26.11 lists the differences between EW0 mode and EW1 mode.

Refer to 26.8.1 “EW0 Mode” and 26.8.2 “EW1 Mode” for details.

**Table 26.11 EW0 Mode and EW1 Mode**

Item	EW0 Mode	EW1 Mode
Operating mode	• Single-chip mode	Single-chip mode
Rewrite control program allocatable area	• Program ROM 1 • Program ROM 2	• Program ROM 1 • Program ROM 2
Rewrite control program executable area	The rewrite control program must be transferred to RAM before being executed.	The rewrite control program can be executed in program ROM 1 and program ROM 2.
Rewritable area	• Program ROM 1 • Program ROM 2 • Data flash	• Program ROM 1 • Program ROM 2 • Data flash Excluding blocks with the rewrite control program
Software command restriction	None	• Do not execute program and block erase commands in a block with the rewrite control program. • Read status register command Do not execute.
Mode after program/erase, or during program/erase suspend	Read status register mode	Read array mode
State during auto write and auto erase	Bus is not in a hold state.	Bus is in a hold state. <sup>(1)</sup>
Flash memory status detection	• Read bits FMR00, FMR06, and FMR07 in the FMR0 register, and bits FMR32 and FMR33 in the FMR3 register by a program. • Execute the read status register command, and then read bits SR7, SR5 and SR4 in the status register.	Read bits FMR00, FMR06, and FMR07 in the FMR0 register, and bits FMR32 and FMR33 in the FMR3 register by a program.

Note:

1. Refer to 10.4 “Bus Hold” for detail about the bus hold.

### 26.8.1 EW0 Mode

The MCU enters CPU rewrite mode when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled) and is ready to accept commands. EW0 mode is selected by setting the FMR60 bit in the FMR6 register to 0. Figure 26.5 shows Setting and Resetting of EW0 Mode

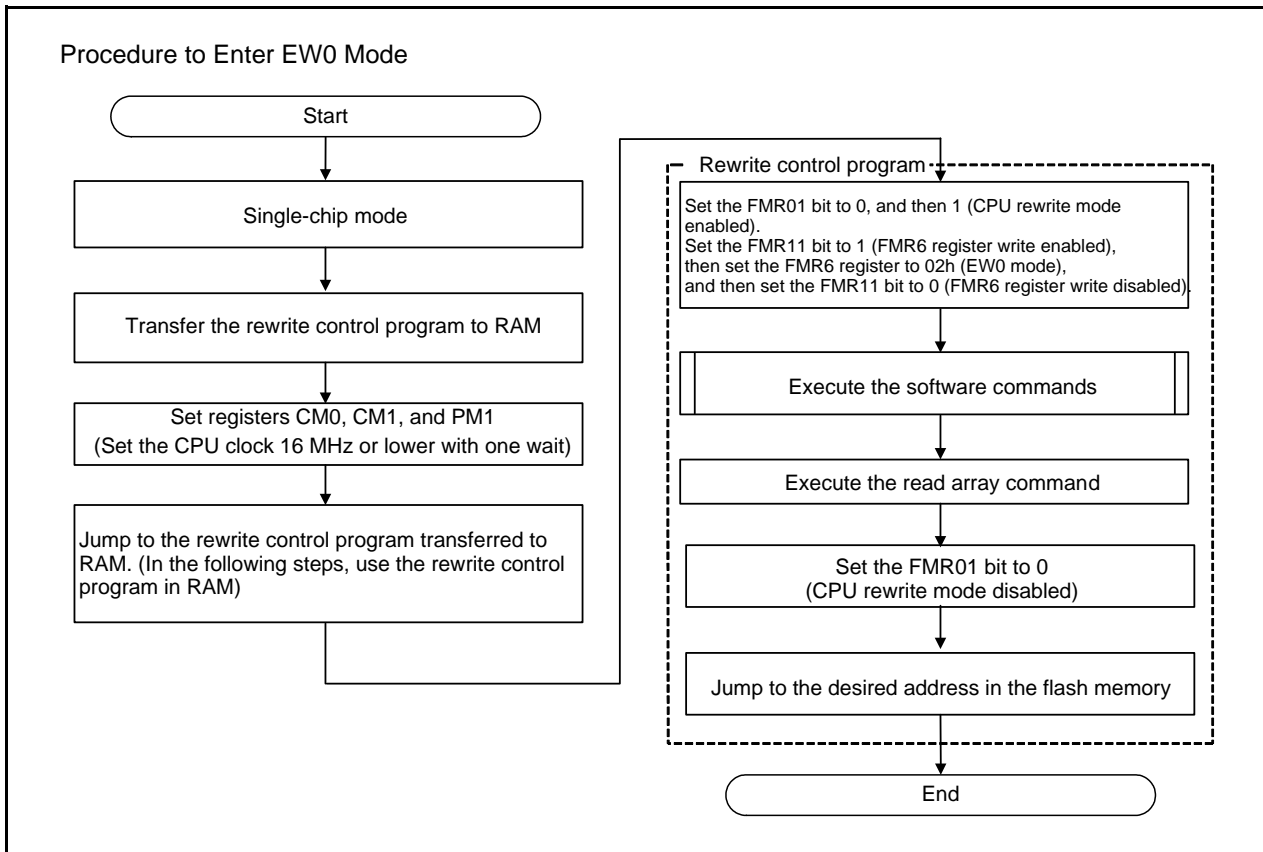


Figure 26.5 Setting and Resetting of EW0 Mode

Do not execute the following instructions in EW0 mode:

UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

The following are interrupts which can be used in EW0 mode and operations when the interrupts occur during auto-erase operation or auto-program operation:

- Maskable interrupt (suspend disabled)

To use the interrupt, allocate a variable vector table on RAM.

- Maskable interrupt (suspend enabled)

To use the interrupt, allocate a variable vector table on RAM.

When the FMR00 bit in the FMR0 register is checked in the interrupt routine and the result is 0 (being written or erased), auto-erase operation or auto-program operation suspends after  $t_d(SR-SUS)$  elapses by setting the FMR31 bit in the FMR3 register to 1 (suspend request). Auto-erase operation or auto-program operation restarts by setting the FMR31 bit to 0 (command restart) at the completion of the interrupt.

- $\overline{NMI}$ , watchdog timer, oscillator stop/restart detect, and voltage detect 2 interrupts

Auto-erase operation or auto-program operation is forcibly stopped as soon as the interrupt occurs, and then the interrupt process starts.

After the flash memory restart, execute auto-erase operation again and confirm that it is completed as expected in order to read the correct value.

The watchdog timer operates even in auto erasing or auto programming operation. Refresh the watchdog timer regularly.

**Table 26.12 Modes after Executing Commands (in EW0 Mode)**

Command	Mode after Executing Command
Read array	Read array mode
Clear status register	Read array mode
Program	Read status register mode <sup>(1)</sup>
Block erase	
Lock bit program	
Read lock bit status	Read lock bit status mode <sup>(1)</sup>
Block blank check	Read status register mode <sup>(1)</sup>

Note:

1. Flash memory can be read only in read array mode.



### 26.8.1.1 Suspend Function (EW0 Mode)

When using suspend function in EW0 mode, check the status of the flash memory in the interrupt routine and enter suspend mode. Program suspend or erase suspend is not accepted until  $t_d(SR-SUS)$  elapses after the FMR31 bit is set to 1. Access to the flash memory after confirming the acceptance of program suspend or erase suspend by the FMR33 or FMR32 bit. Set the FMR31 bit to 0 (command restart) to restart auto-program and auto-erase operations at the completion of the access to the flash memory. Figure 26.6 to Figure 26.8 show a flowchart in EW0 mode when the suspend function is enabled, and Figure 26.9 shows Suspend Operation Example in EW0 Mode.

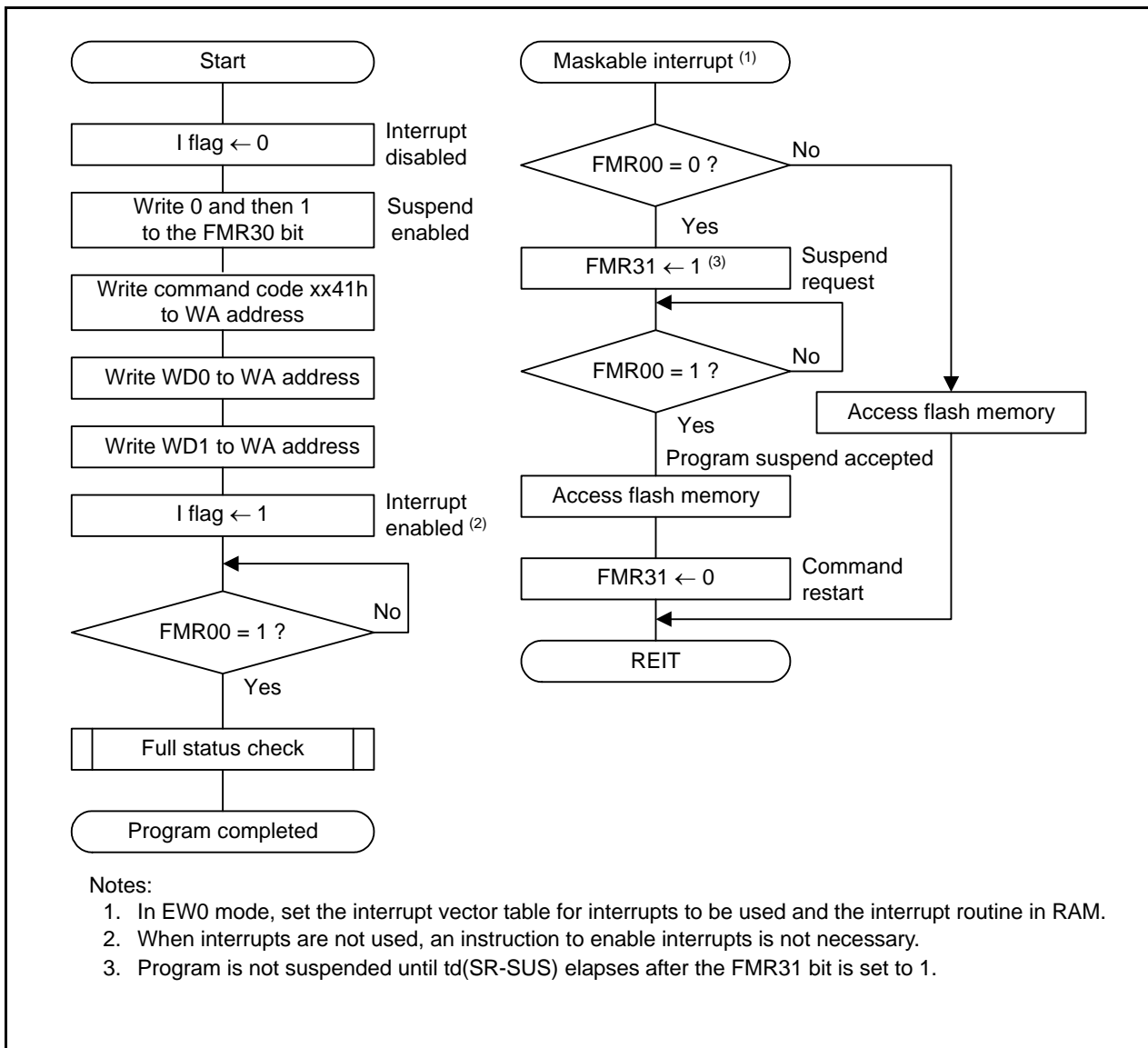


Figure 26.6 Program Flowchart in EW0 Mode (Suspend Function Enabled)

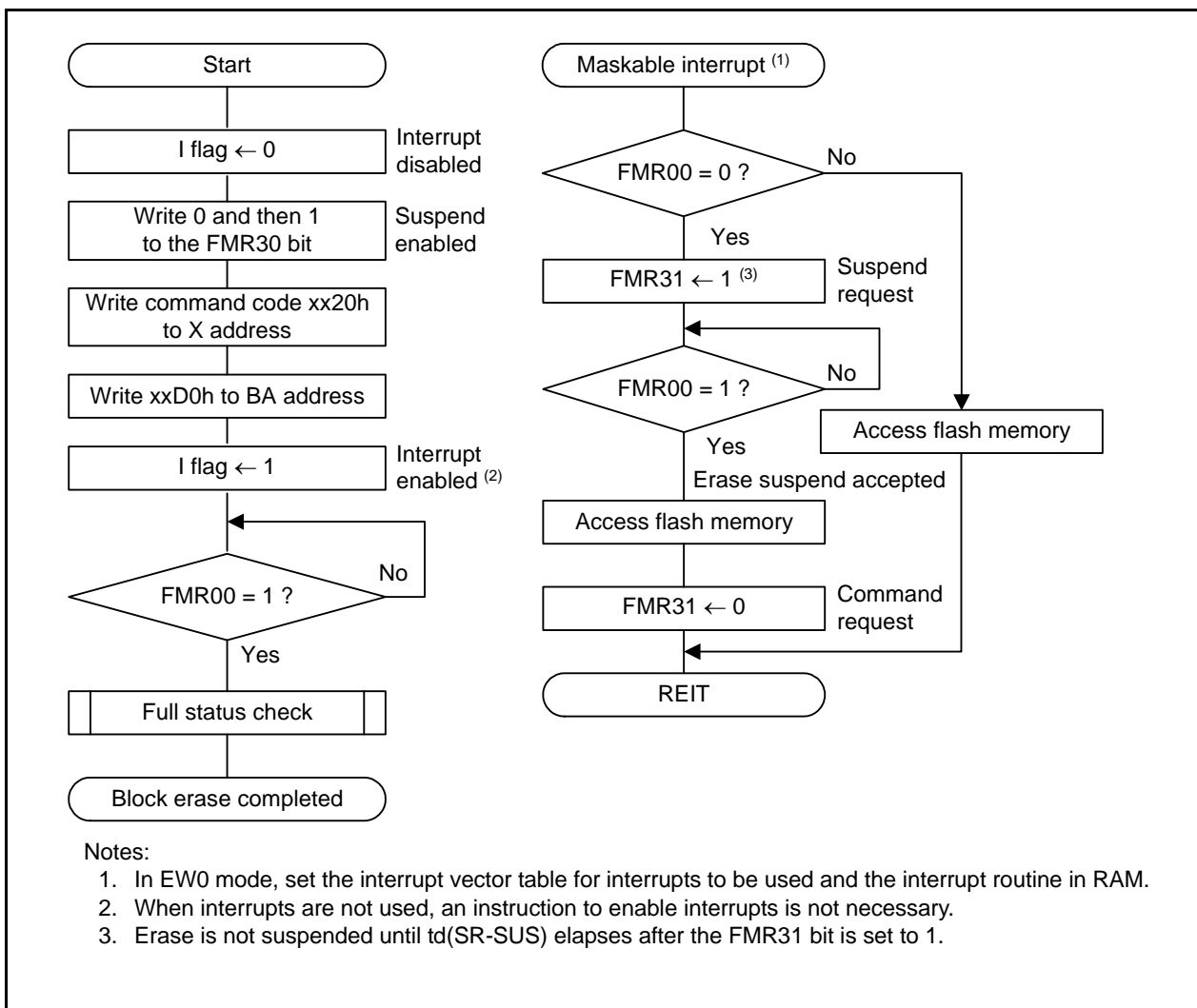


Figure 26.7 Block Erase Flowchart in EW0 Mode (Suspend Function Enabled)

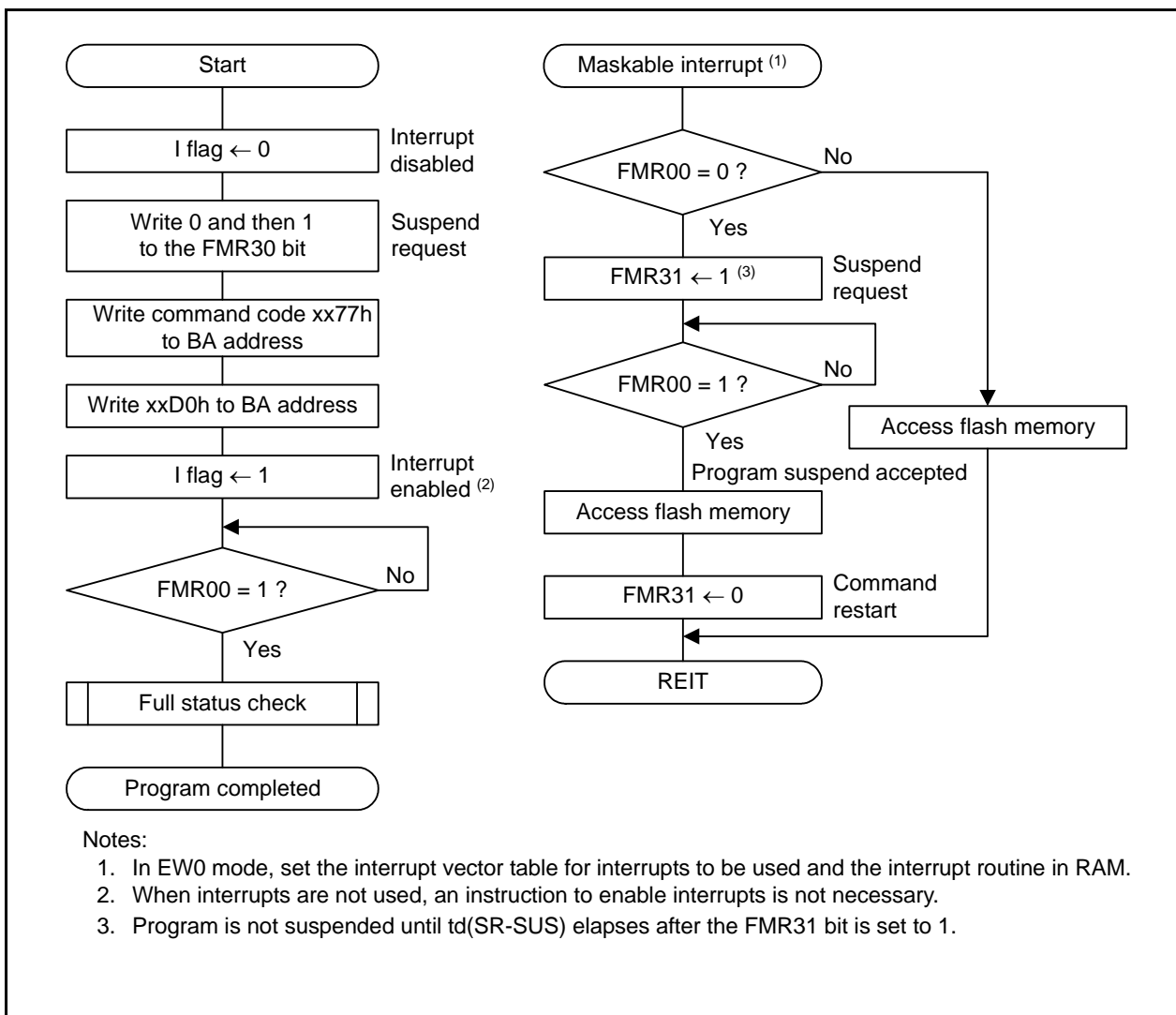


Figure 26.8 Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)

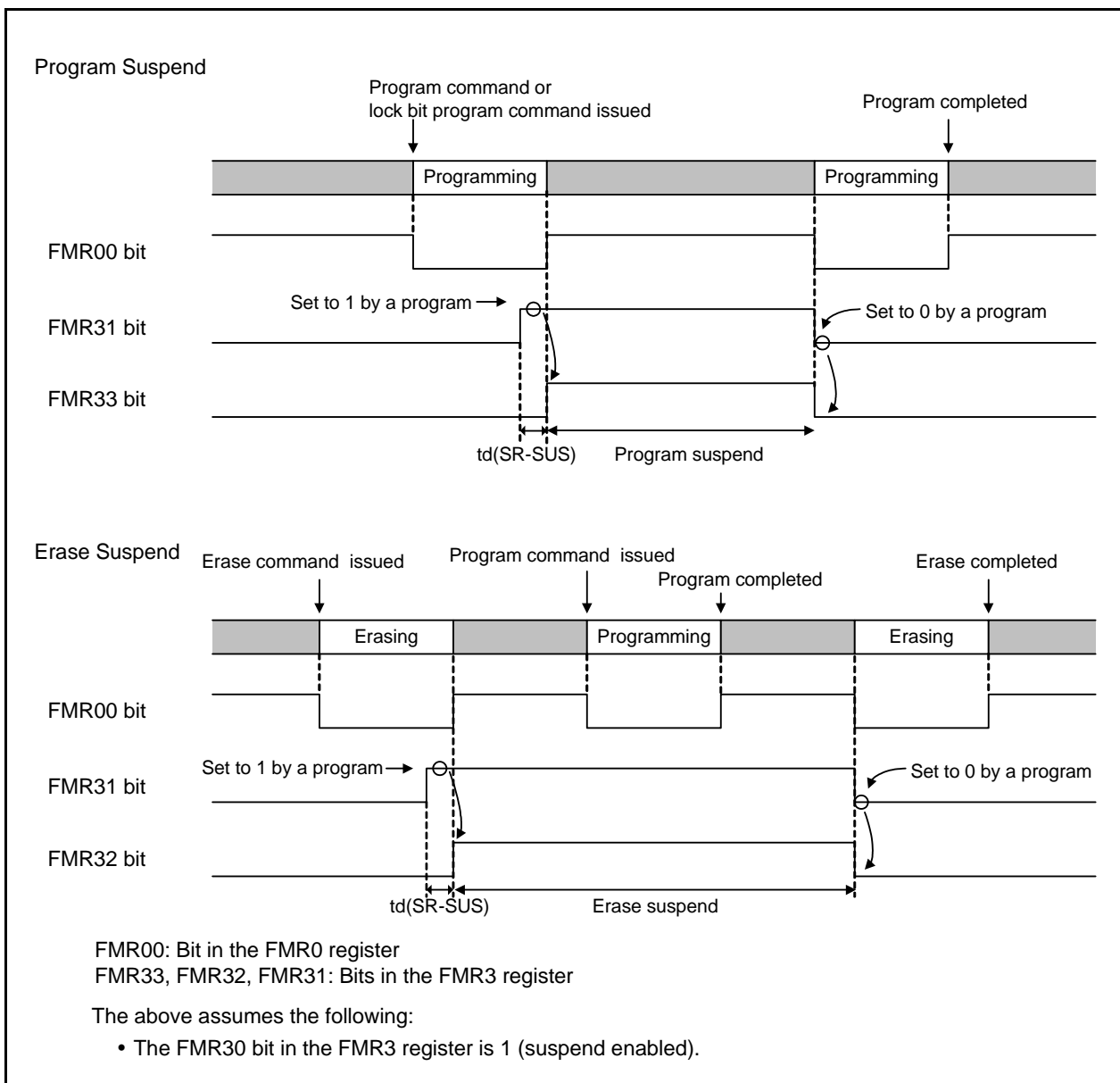
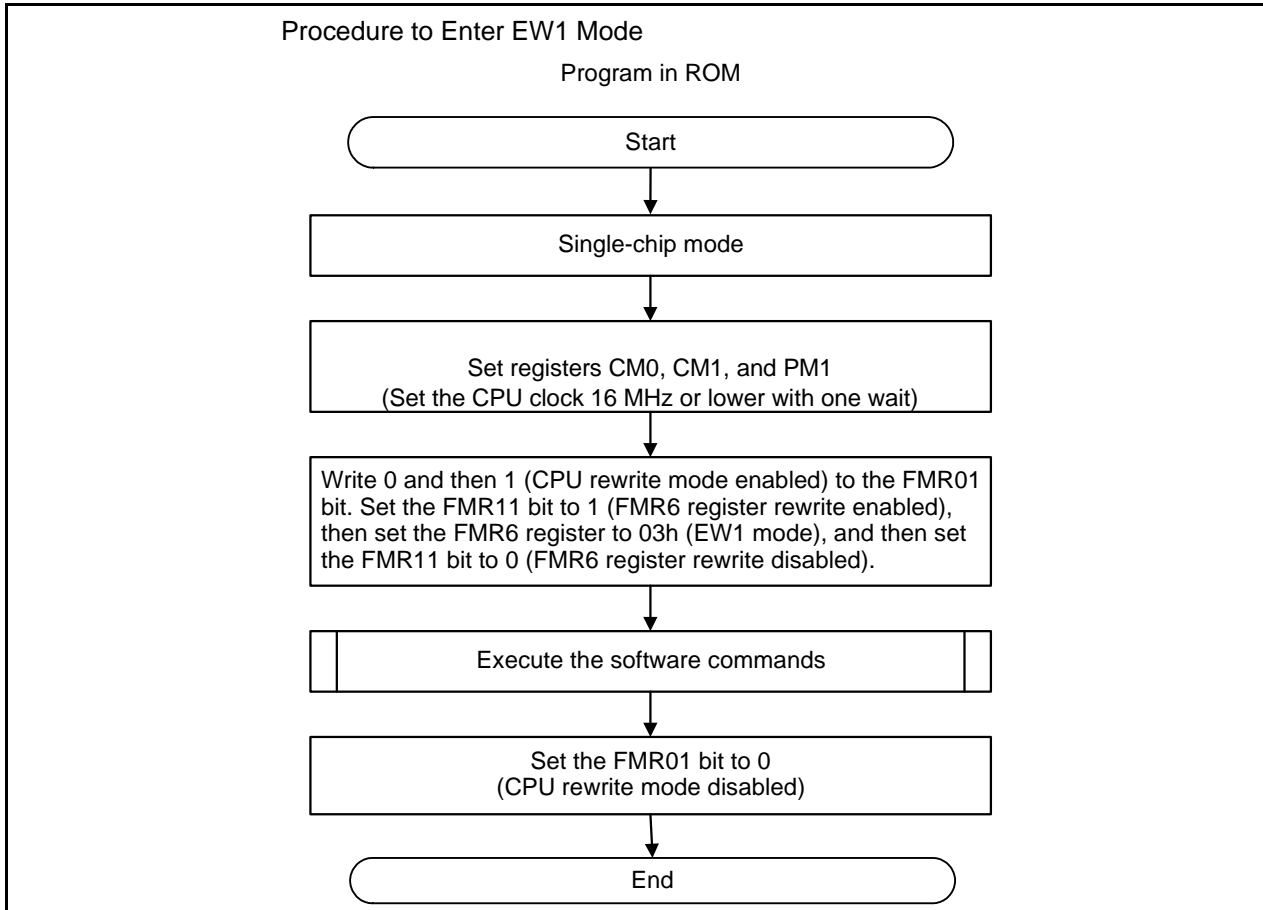


Figure 26.9 Suspend Operation Example in EW0 Mode

## 26.8.2 EW1 Mode

EW1 mode is selected by setting the FMR60 bit in the FMR6 register to 1 after setting the FMR01 bit in the FMR0 register to 1. Figure 26.10 shows Setting and Resetting of EW1 Mode.

When a program or erase operation is initiated, the CPU halts all program execution until the operation is completed.



**Figure 26.10 Setting and Resetting of EW1 Mode**

The following are interrupts which can be used in EW1 mode and operations when the interrupts occur during auto-erase operation or auto-program operation:

- Maskable interrupt (suspend function enabled)  
Auto-erase operation or auto-program operation suspends after  $t_d(SR-SUS)$  elapses and the interrupt process is executed. Auto-erase operation or auto-program operation restarts by setting the FMR31 bit in the FMR3 register to 0 (command restart) after the interrupt process is completed.
- Maskable interrupt (suspend function disabled)  
Auto-erase operation or auto-program operation has a higher priority level and the interrupt request has to wait. The interrupt process is executed after auto-erase operation or auto-program operation is completed.
- $\overline{NMI}$ , watchdog timer, oscillator stop/restart detect, and voltage detect 2 interrupts  
Auto-erase operation or auto-program operation forcibly stops as soon as the interrupt occurs, and then the interrupt process starts.  
After the flash memory restart, execute auto-erase operation again and confirm that it is completed as expected in order to read the correct value.

The watchdog timer stops its counting during auto-erase or auto-programming. Do not use EW1 mode while the CSPRO bit in the CSPR register is 1 (count source protection mode enabled). Use EW0 mode. However, counts does not stop during erase suspend or program suspend. As the interrupt request may be generated, initialize the watchdog timer regularly using the suspend function.

**Table 26.13 Modes after Executing Commands (in EW1 Mode)**

Command	Mode after Executing Command
Read array	Read array mode
Clear status register	
Program	
Block erase	
Lock bit program	
Read lock bit status	
Block blank check	

### 26.8.2.1 Suspend Function (EW1 Mode)

When using suspend function in EW1 mode, an interrupt request is not accepted until  $t_d(\text{SR-SUS})$  elapses after the interrupt request is generated. When the interrupt request is accepted, the flash memory enters erase suspend or program suspend. Set the FMR31 bit to 0 (command restart) to restart automatic program and erase operations at the completion of the interrupt. Figure 26.11 to Figure 26.13 show a flowchart in EW1 mode when the suspend function is enabled, and Figure 26.14 shows Suspend Operation Example in EW1 Mode.

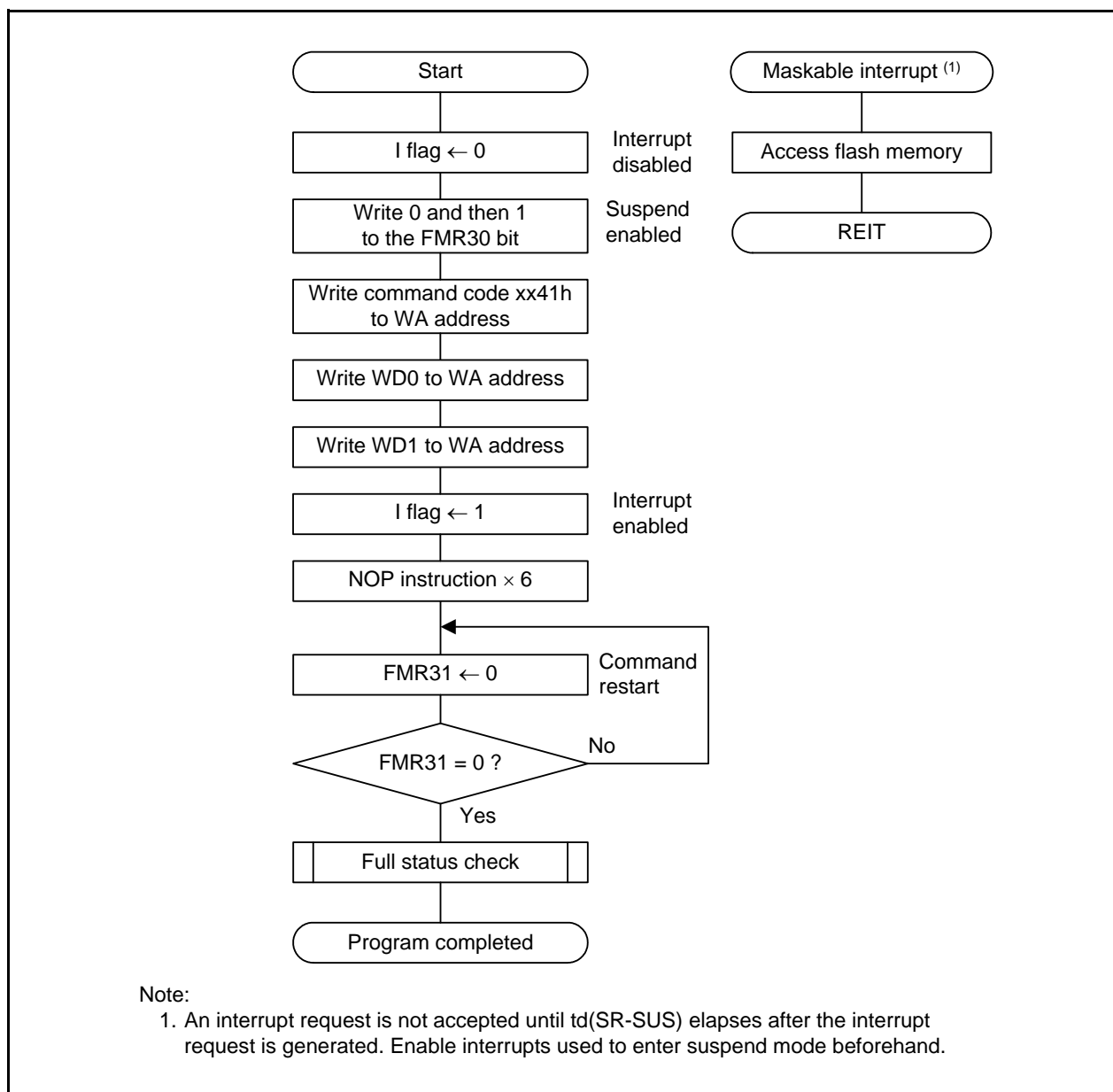
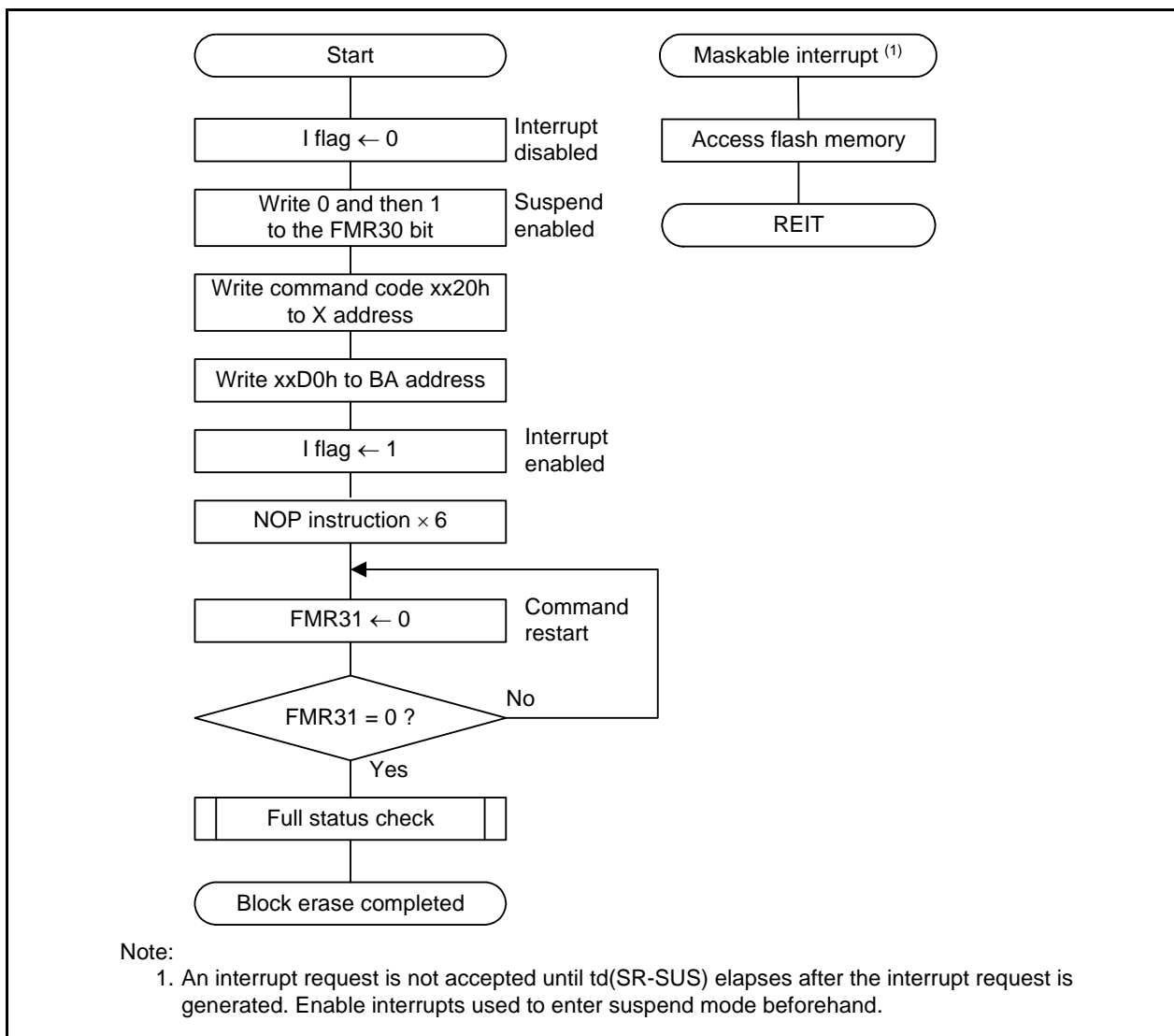


Figure 26.11 Program Flowchart in EW1 Mode (Suspend Function Enabled)



**Figure 26.12 Block Erase Flowchart in EW1 Mode (Suspend Function Enabled)**



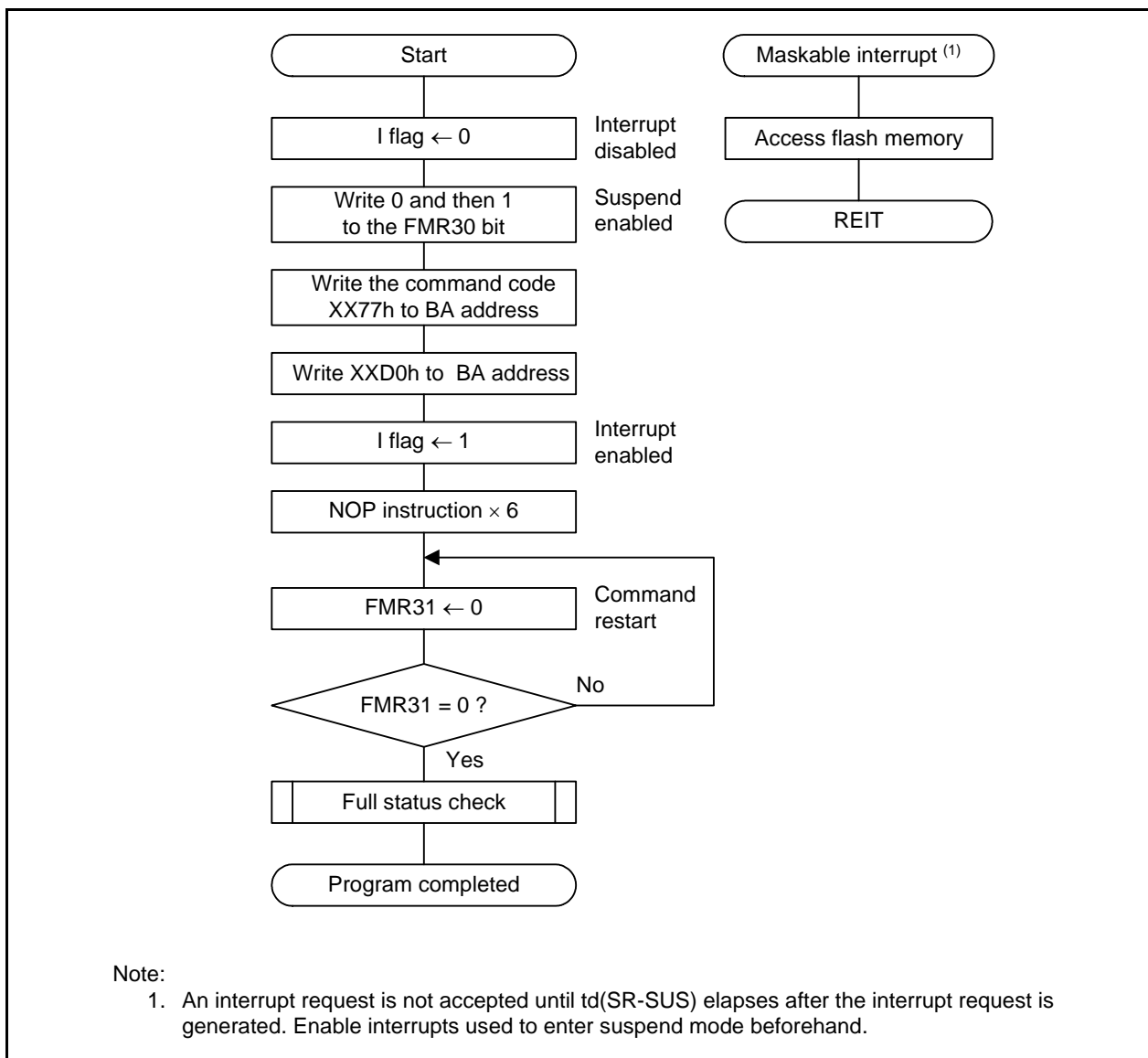


Figure 26.13 Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled)

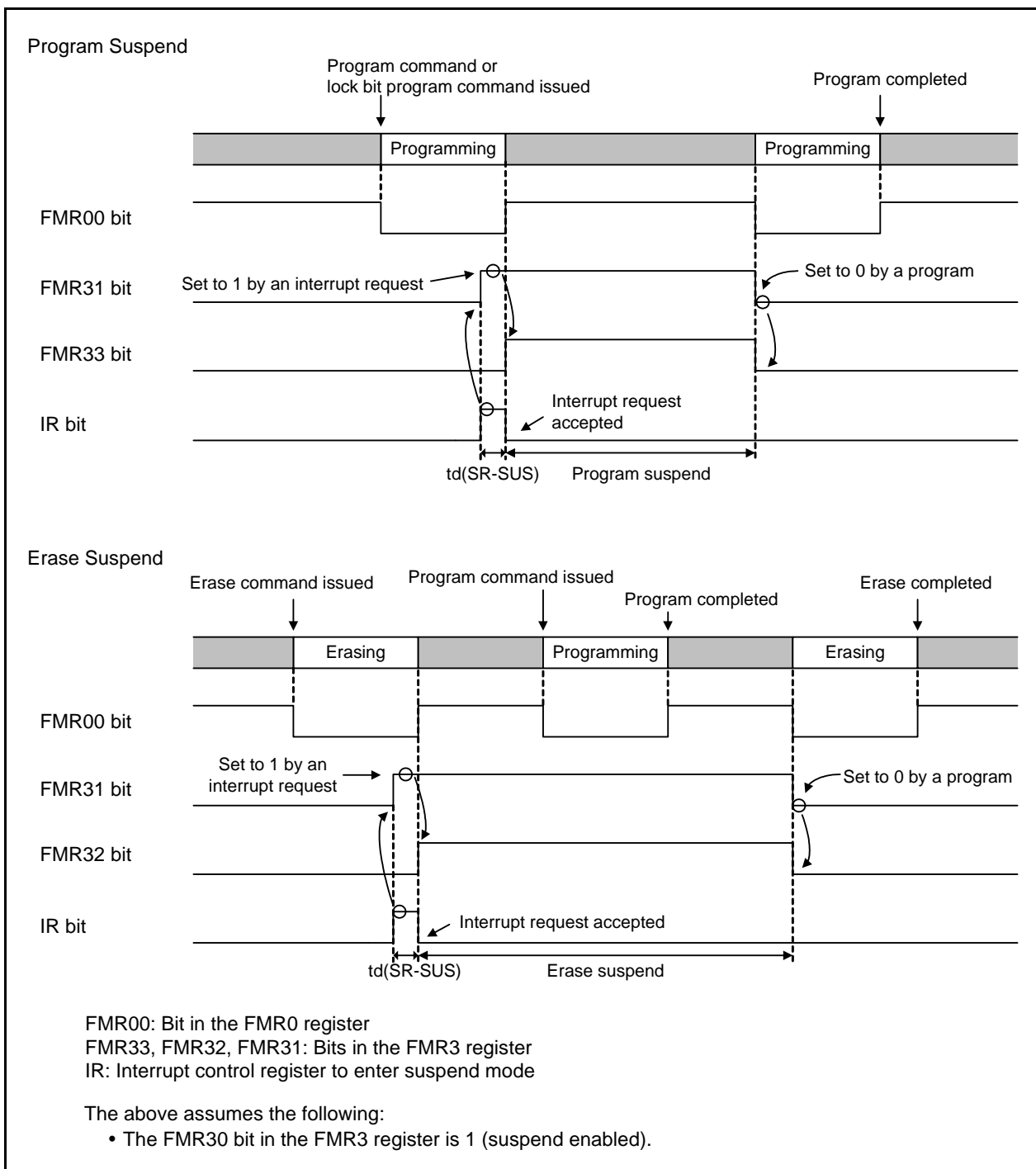


Figure 26.14 Suspend Operation Example in EW1 Mode

### 26.8.3 Operating Speed

Select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

### 26.8.4 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to 0 (lock bit enabled). The lock bit allows blocks to be individually protected (locked) against being programmed and erased. This prevents data from being inadvertently written to or erased from the flash memory. Table 26.14 lists Lock Bit and Block State.

**Table 26.14 Lock Bit and Block State**

FMR02 Bit in the FMR0 Register	Lock Bit	Block State
0 (enabled)	0 (locked)	Protected against being programmed and erased
	1 (unlocked)	Can be programmed or erased
1 (disabled)	0 (locked)	Can be programmed or erased
	1 (unlocked)	

Condition to become 0:

- Execute the lock bit program command

Condition to become 1:

- Execute the block erase command while the FMR02 bit in the FMR0 register is set to 1 (lock bit disabled).

If the block erase command is executed while the FMR02 bit is set to 1, the target block is erased regardless of lock bit status. The lock bit data can be read by the read lock bit status command.

Refer to 26.8.6 “Software Commands”, for details on each command.

### 26.8.5 Suspend Function

The suspend function suspends automatic programming and erasure. It can be used for an interrupt operation because program ROM 1, program ROM 2, and data flash can be read while automatic programming or erasure is suspended. Enable the interrupts used to enter suspend mode beforehand. The program command, erase command, and lock bit program command are subjects for suspend. Suspend operation is the same for the program command and lock bit program command, so both commands are described together as program suspend.

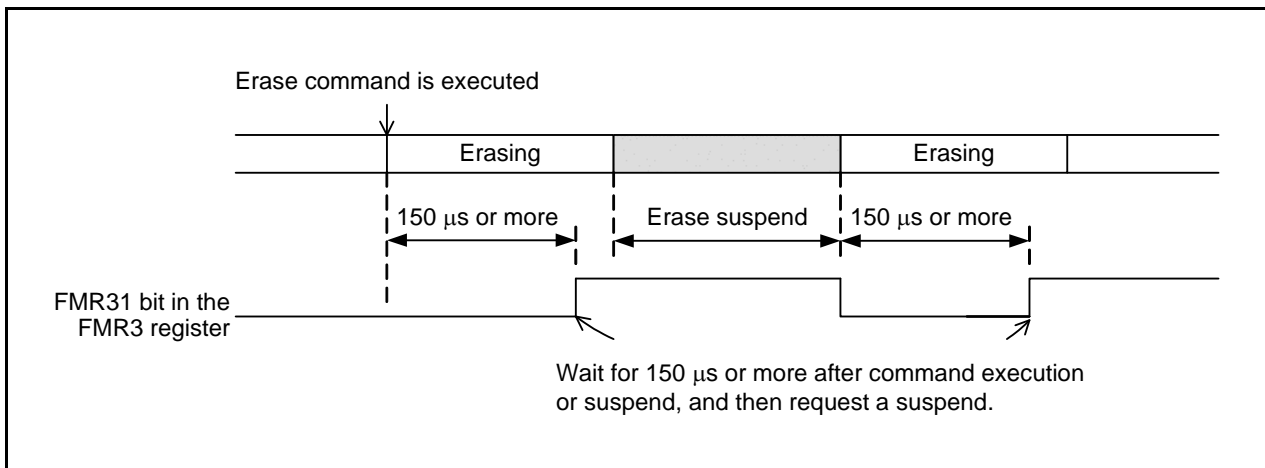
Do not suspend again in suspend mode. Table 26.15 lists Operation after Command is Issued during Suspend.

**Table 26.15 Operation after Command is Issued during Suspend**

Suspend	Command	Operation	
		Blocks erased or programmed before suspend	Other blocks
Erase suspend (Suspend while executing erase command)	Block erase	The command is not executed. A command sequence error occurs.	
	Program	The command is not executed. A command sequence error occurs.	The command can be executed. Program suspend does not start or an error does not occur even when setting the FMR31 bit to 1 (suspend request).
	Lock bit program	The command is not executed. A command sequence error occurs.	The command can be executed.
	Read array	The command can be executed.	
	Read status register		
	Clear status register		
	Read lock bit status	The command is not executed. A command sequence error occurs.	The command can be executed.
	Block blank check	Do not execute the command.	
Program suspend (Suspend while executing program or lock bit program command)	Block erase	The command is not executed. A command sequence error occurs. <sup>(1)</sup>	
	Program		
	Lock bit program		
	Read array	The command can be executed.	
	Read status register		
	Clear status register	Do not execute the command. <sup>(1)</sup>	
	Read lock bit status	Do not execute the command.	
	Block blank check		

**Note:**

1. If the command sequence error occurs after executing block erase, program, or lock bit program commands mistakenly during program suspend. execute the clear status register command, then restart suspend.

**Figure 26.15 Suspend Request**

## 26.8.6 Software Commands

Table 26.16 list Software Commands. Read or write commands and data in 16-bit units. When command code is written, the upper 8 bits (D15 to D8) are ignored.

**Table 26.16 Software Commands**

Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)
Read array	Write	x	xxFFh	–	–	–	–	–	–
Read status register	Write	x	xx70h	Read	x	SRD	–	–	–
Clear status register	Write	x	xx50h	–	–	–	–	–	–
Program	Write	WA	xx41h	Write	WA	WD0	Write	WA	WD1
Block erase	Write	x	xx20h	Write	BA	xxD0h	–	–	–
Lock bit program	Write	BA	xx77h	Write	BA	xxD0h	–	–	–
Read lock bit status	Write	x	xx71h	Write	BA	xxD0h	–	–	–
Block blank check <sup>(1)</sup>	Write	x	xx25h	Write	BA	xxD0h	–	–	–

SRD : Data in the status register (D7 to D0)

WA : Write address (set the end of the address to 0h, 4h, 8h, or Ch)

WD0 : Write data lower word (16 bits)

WD1 : Write data upper word (16 bits)

BA : Highest block address (even address)

x : Any even address in program ROM 1, program ROM 2, or data flash

xx : 8 upper bits of command code (ignored)

Note:

1. Block blank check command is designed for programmer manufacturer. Not for customers in general.

Software commands are described below.

For symbols shown in the flowcharts, refer to those in Table 26.16.

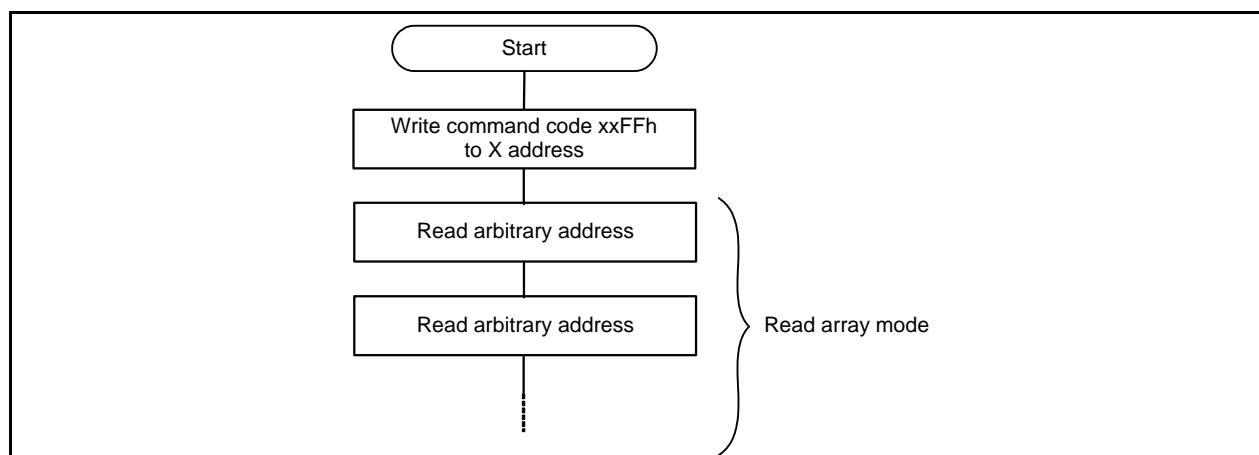
Refer to 26.8.5 “Suspend Function” for program, block erase, and lock bit program commands when using suspend function.

### 26.8.6.1 Read Array Command

The read array command is used to read the flash memory.

By writing the command code xxFFh in the first bus cycle, the flash memory enters read array mode. The value of the specified address can be read in 16-bit units by entering the address to be read after the next bus cycle.

The flash memory remains in read array mode until another command is written. Therefore, the values of multiple addresses can be read consecutively.



**Figure 26.16 Read Array Command**

### 26.8.6.2 Read Status Register Command

The read status register command is used to read the status register.

By writing the command code `xx70h` in the first bus cycle, the status register can be read in the second bus cycle. (Refer to 26.8.7 "Status Register"). To read the status register, read an even address in program ROM 1, program ROM 2, or the data flash.

Do not execute this command in EW1 mode.

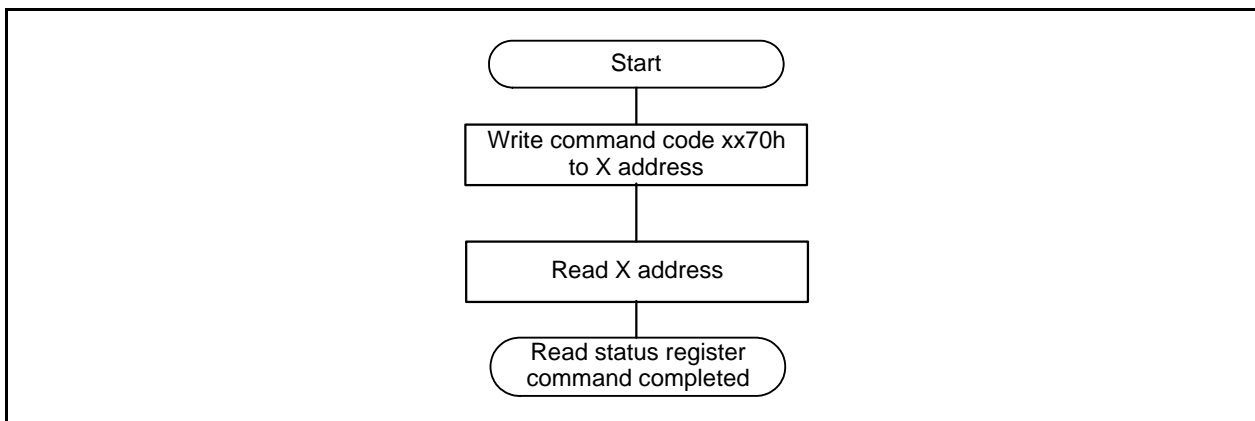


Figure 26.17 Read Status Register Command

### 26.8.6.3 Clear Status Register Command

The clear status register command is used to clear the status register.

By writing the command code `xx50h`, bits FMR07 and FMR06 in the FMR0 register (SR5 and SR4 in the status register) become 00b.

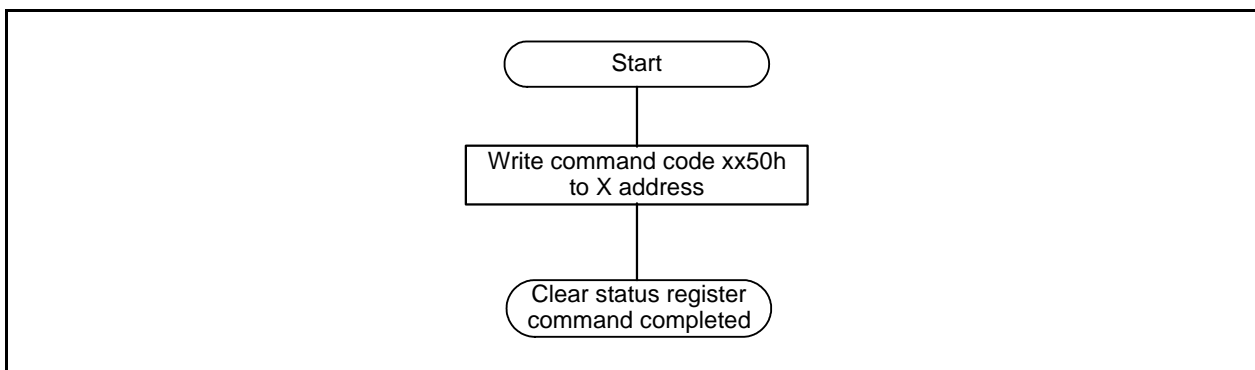


Figure 26.18 Clear Status Register Command

### 26.8.6.4 Program Command

The program command is used to write 2 words (4 bytes) of data to the flash memory.

By writing xx41h in the first bus cycle and data to the write address in the second and third bus cycles, an auto-program operation (data program and verify) is started. Set the end of the write address to 0h, 4h, 8h, or Ch.

The FMR00 bit in the FMR0 register indicates whether the auto-program operation has been completed. The FMR00 bit is 0 (busy) during the auto-program operation, and becomes 1 (ready) after the auto-program operation is completed. Do not execute other commands while the FMR00 bit is 0.

After the auto-program operation is completed, the FMR06 bit in the FMR0 register indicates whether or not the auto-program operation has been completed as expected. (Refer to 26.8.7.1 "Full Status Check").

Do not rewrite the addresses already programmed. Figure 26.19 shows a flowchart of the Program Command (Suspend Function Disabled).

The lock bit protects individual blocks from being programmed inadvertently. (Refer to 26.8.4 "Data Protect Function".)

In EW1 mode, do not execute this command on a block to which the rewrite control program is allocated.

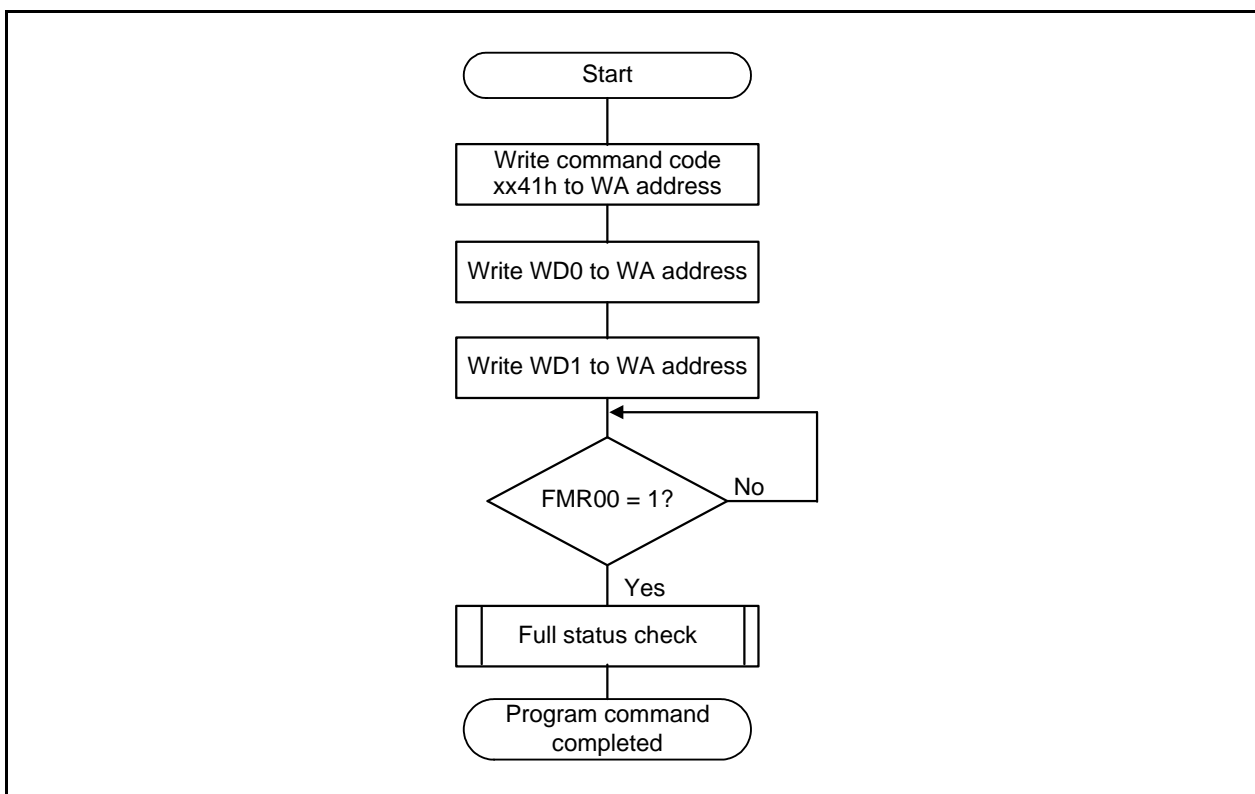


Figure 26.19 Program Command (Suspend Function Disabled)



### 26.8.6.5 Block Erase Command

By writing xx20h in the first bus cycle and xxD0h to the highest even address of a block in the second bus cycle, an auto-erase operation (erase and verify) is started on the specified block.

The FMR00 bit in the FMR0 register indicates whether the auto-erase operation has been completed. The FMR00 bit is 0 (busy) during the auto-erase operation, and becomes 1 (ready) when the auto-erase operation is completed. Do not execute other commands while the FMR00 bit is 0.

After the auto erase operation is completed, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected. (Refer to 26.8.7.1 “Full Status Check”).

Figure 26.20 shows a flowchart of the Block Erase Command (Suspend Function Disabled).

The lock bit protects individual blocks from being erased inadvertently. (Refer to 26.8.4 “Data Protect Function”).

In EW1 mode, do not execute this command on the block to which the rewrite control program is allocated.

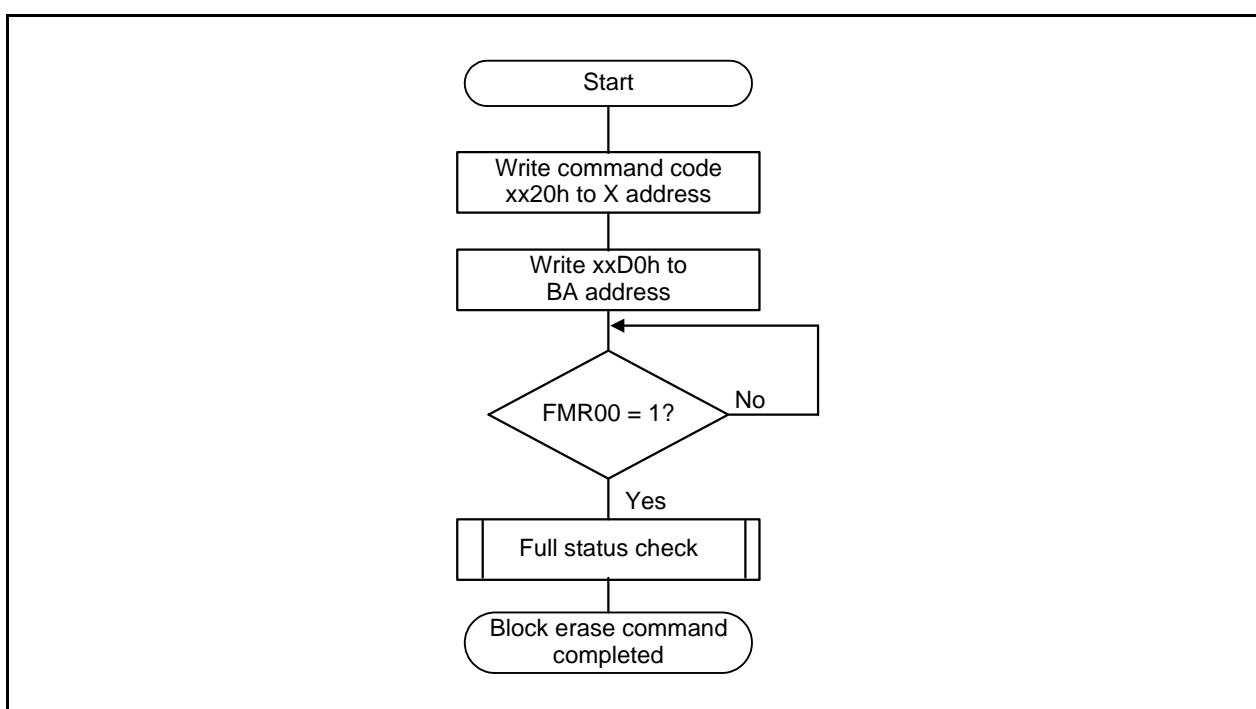


Figure 26.20 Block Erase Command (Suspend Function Disabled)

### 26.8.6.6 Lock Bit Program Command

The lock bit program command is used to set the lock bit for a specified block to 0 (locked). By writing xx77h in the first bus cycle and xxD0h to the highest even address of a block in the second bus cycle, the lock bit for the specified block is set to 0. The address value specified in the first bus cycle must be the same highest address of a block specified in the second bus cycle.

Figure 26.21 shows a flowchart of the Lock Bit Program Command (Suspend Function Disabled). Execute the read lock bit status command to read the lock bit state (lock bit data).

The FMR00 bit in the FMR0 register indicates whether a lock bit program operation has been completed. Do not execute other commands while the FMR00 bit is 0.

Refer to 26.8.4 “Data Protect Function”, for details on lock bit functions and how to set it to 1 (unlocked).

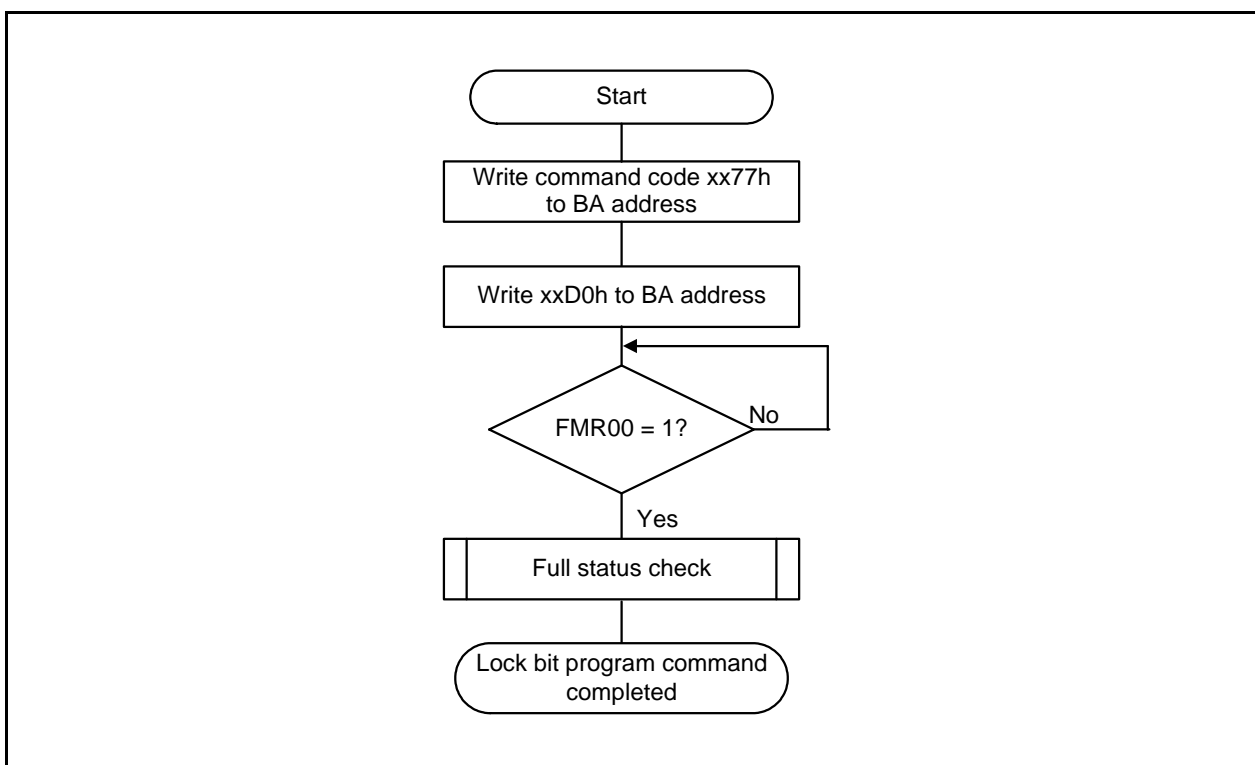


Figure 26.21 Lock Bit Program Command (Suspend Function Disabled)

### 26.8.6.7 Read Lock Bit Status

The read lock bit status command is used to read the lock bit state of a specified block. By writing xx71h in the first bus cycle and xxD0h to the highest even address of a block in the second bus cycle, the FMR16 bit in the FMR1 register stores information on the lock bit status of a specified block. Read the FMR16 bit after the FMR00 bit in the FMR0 register becomes 1 (ready). Do not execute other commands while the FMR00 bit is 0.

Figure 26.22 shows a flowchart of the Read Lock Bit Status Command.

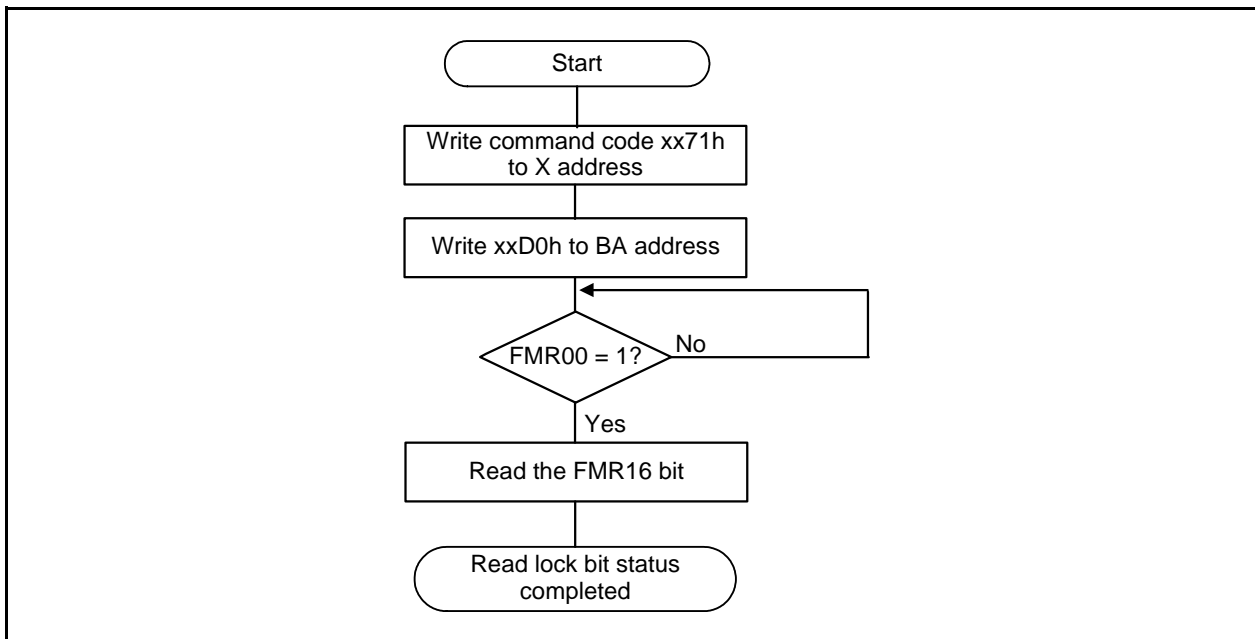


Figure 26.22 Read Lock Bit Status Command

### 26.8.6.8 Block Blank Check Command

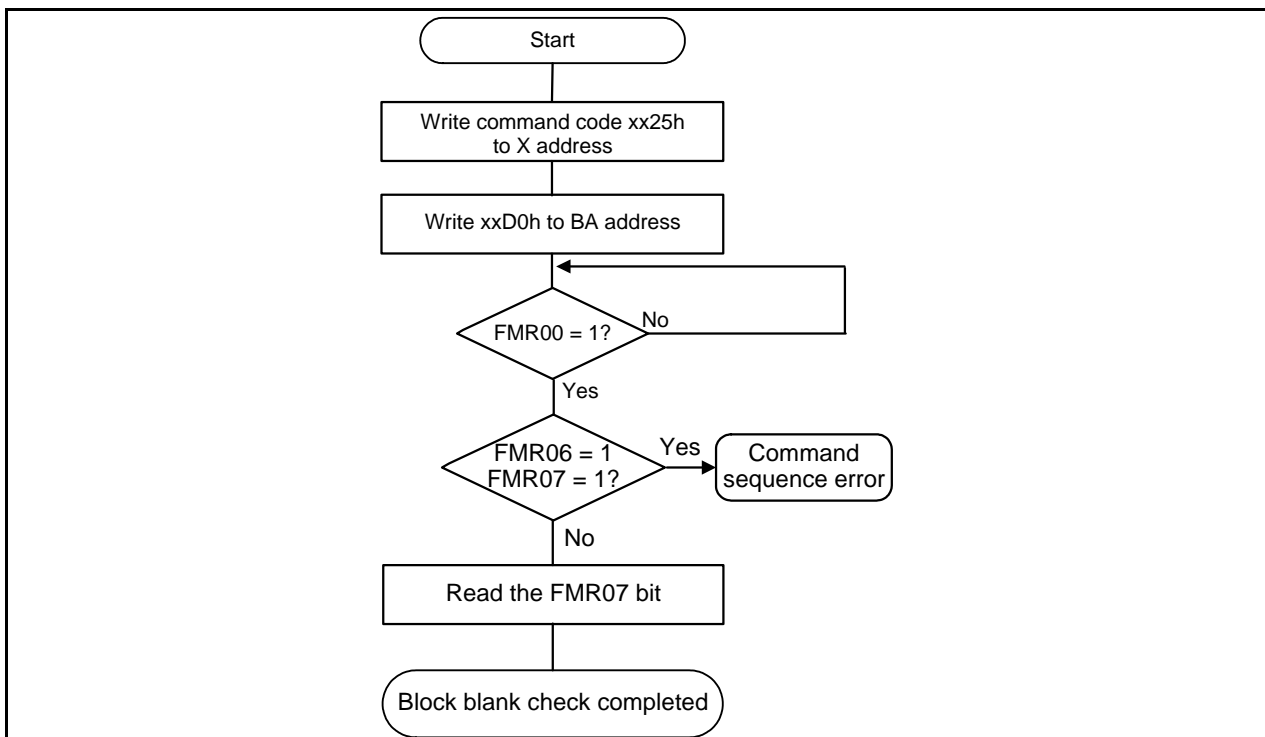
The block blank check command is used to check whether or not a specified block is blank (state after erase).

By writing xx25h in the first bus cycle and xxD0h in the second bus cycle to the highest even address of a block, the check result is stored in the FMR07 bit in the FMR0 register. Read the FMR07 bit after the FMR00 bit in the FMR0 register is set to 1 (ready). Do not execute other commands while the FMR00 bit is 0.

The block blank check command is valid for unlocked blocks.

If the block blank check command is executed on a block whose lock bit is 0 (locked), the FMR07 bit (SR5) is set to 1 (not blank) regardless of the FMR02 bit state.

Figure 26.23 shows a flowchart of the Block Blank Check Command.



**Figure 26.23 Block Blank Check Command**

As a result of block blank check, when the block is not blank, execute the clear status register command before executing other software commands.

The block blank check command is designated for use with a programmer. Use this command where instantaneous power failures do not occur. When an instantaneous power failure occurs while the block erase command is executed, execute the block erase command again. The block blank check command cannot be used to check whether the erase operation is successfully completed or not.

Do not execute the block blank check command during suspend.

### 26.8.7 Status Register

The status register indicates flash memory operating state and whether or not an erase or program operation has been completed as expected.

Bits FMR00, FMR06, and FMR07 in the FMR0 register indicate status register states. Refer to 26.3.1 “Flash Memory Control Register 0 (FMR0)” for a description of each bit.

**Table 26.17 Difference in Reading of Status Register**

Item	FMR0 register	Command
Condition	No limit	
Reading procedure	Read bits FMR00, FMR06, and FMR07 in the FMR0 register	<ul style="list-style-type: none"> <li>• Read any even address in program ROM 1, program ROM 2, or data flash after writing the read status register command.</li> <li>• Read any even address in program ROM 1, program ROM 2, or data flash after executing the program command, block erase command, lock bit program command, or block blank check command before executing the read array command.</li> </ul>

**Table 26.18 Status Register**

Bits in Status Register	Bit in FMR0 Register	Status	Status		Reset Value
			0	1	
SR0 (D0)	-	Reserved	-	-	-
SR1 (D1)	-	Reserved	-	-	-
SR2 (D2)	-	Reserved	-	-	-
SR3 (D3)	-	Reserved	-	-	-
SR4 (D4)	FMR06	Program status	Completed as expected	Completed in error	0
SR5 (D5)	FMR07	Erase status	Completed as expected	Completed in error	0
SR6 (D6)	-	Reserved	-	-	-
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1

D0 to D7: The data buses read when the read status register command is executed.

### 26.8.7.1 Full Status Check

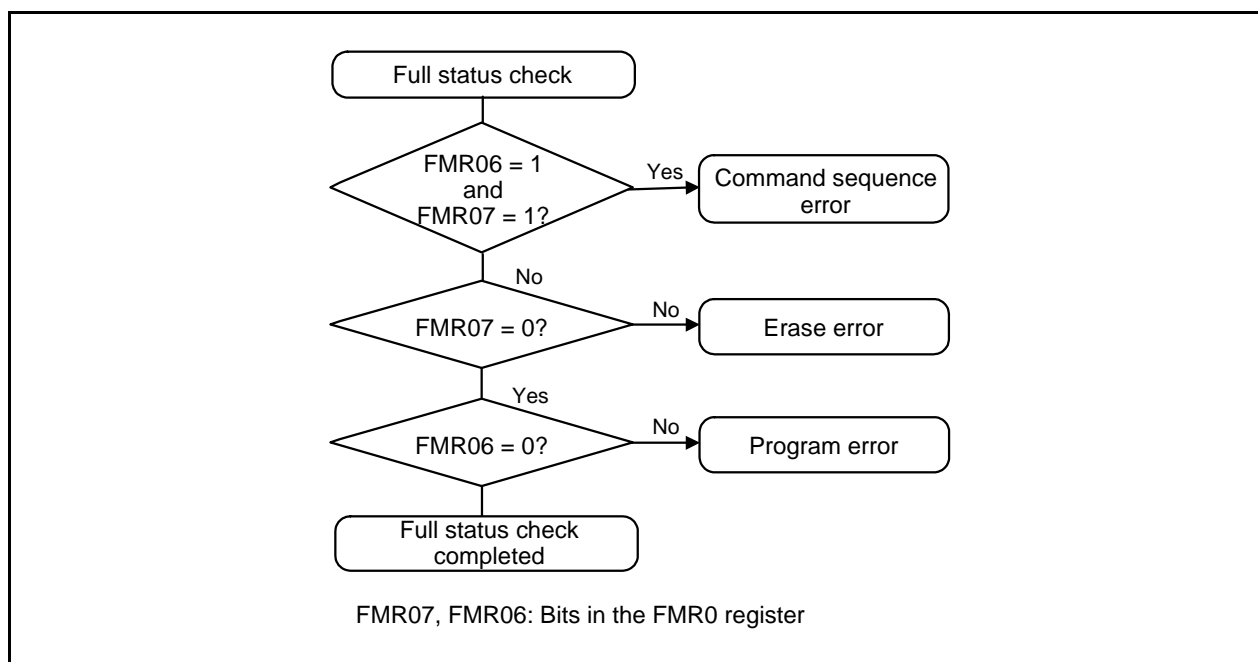
If an error occurs, bits FMR06 and FMR07 in the FMR0 register become 1, indicating the occurrence of an error. Therefore, the execution results can be confirmed by checking these status bits (full status check).

**Table 26.19 Errors and FMR0 Register States**

FMR00 Register		Error	Error Occurrence Conditions
FMR07 bit	FMR06 bit		
1	1	Command sequence error	<ul style="list-style-type: none"> <li>Command is written incorrectly.</li> <li>Data other than xxD0h and xxFFh is written in the second bus cycle of the lock bit program, block erase, block blank check, or read lock bit status command. <sup>(1)</sup></li> </ul>
1	0	Erase error	<ul style="list-style-type: none"> <li>The block erase command is executed on a locked block. <sup>(2)</sup></li> <li>The block erase command is executed on an unlocked block, but the auto-erase operation is not completed as expected.</li> <li>The block blank check command is executed, and the check result is not blank.</li> </ul>
0	1	Program error	<ul style="list-style-type: none"> <li>The program command is executed on a locked block. <sup>(2)</sup></li> <li>The program command is executed on an unlocked block, but the auto-program operation is not completed as expected.</li> <li>The lock bit program command is executed, but the lock bit is not written as expected.</li> </ul>

Notes:

- When writing xxFFh in the second bus cycle of the command, the flash memory becomes the state before executing the command, and the command code written in the first bus cycle is cancelled.
- When the FMR02 bit is 1 (lock bit disabled), no error occurs even under the conditions above.



**Figure 26.24 Full Status Check**

### 26.8.7.2 Handling Procedure for Errors

When errors occur, follow the procedures below.

Do not execute the program, block erase, lock bit program, and block blank check commands when either FMR06 or FMR07 bit is 1 (completed in error). Execute each command after executing the clear status register command.

Command sequence error

- (1) Execute the clear status register command and set bits FMR06 and FMR07 to 0 (completed as expected).
- (2) Check if the command is written correctly and execute the correct command.

Erase error

- (1) Execute the clear status register command and set the FMR07 bit to 0 (completed as expected).
- (2) Execute the read lock bit status command. Set the FMR02 bit in the FMR register to 1 (lock bit disabled) if the lock bit in the block where the error occurred is set to 0 (locked).
- (3) Execute the block erase command again.
- (4) Repeat (1) to (3) until an erase error is not generated.

If an error still occurs even after repeating three times, do not use that block.

When handling an erase error of the block blank check command and erasing is not necessary, execute (1) only.

Program error

[When a program operation is executed]

- (1) Execute the clear status register command and set the FMR06 bit to 0 (completed as expected).
- (2) Execute the read lock bit status command. Set the FMR02 bit in the FMR0 register to 1 if the lock bit in the block where the error occurred is set to 0.
- (3) Execute the program command again.

If the lock bit is set to 1 (unlocked), do not use the address in which error has occurred as it is. Execute the block erase command to erase the block, in which the error has occurred, before executing the program command to write to the same address again.

If an error still occurs, do not use that block.

[When a lock bit program operation is executed]

- (1) Execute the clear status register command and set the FMR06 bit to 0.
- (2) Set the FMR02 bit in the FMR0 register to 1.
- (3) Execute the block erase command to erase the block where the error occurred.
- (4) Execute the lock bit program command again after writing the data as needed.

If an error still occurs, do not use that block.

## 26.9 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer supporting the M16C/5L Group, M16C/56 Group can be used to rewrite program ROM 1, program ROM 2, and data flash while the MCU is mounted on a board.

Standard serial I/O mode has following modes:

- Standard serial I/O mode 1: The MCU is connected to the serial programmer by using clock synchronous serial I/O
- Standard serial I/O mode 2: The MCU is connected to the serial programmer by using 2-wire clock asynchronous serial I/O

For more information about the serial programmer, contact the serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.



### 26.9.1 ID Code Check Function

Use the ID code check function in standard serial I/O mode. This function determines whether the ID codes sent from the serial programmer match those written in the flash memory. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the 4 bytes of the reset vector are FFFFFFFFh, ID codes are not compared, allowing all commands to be accepted.

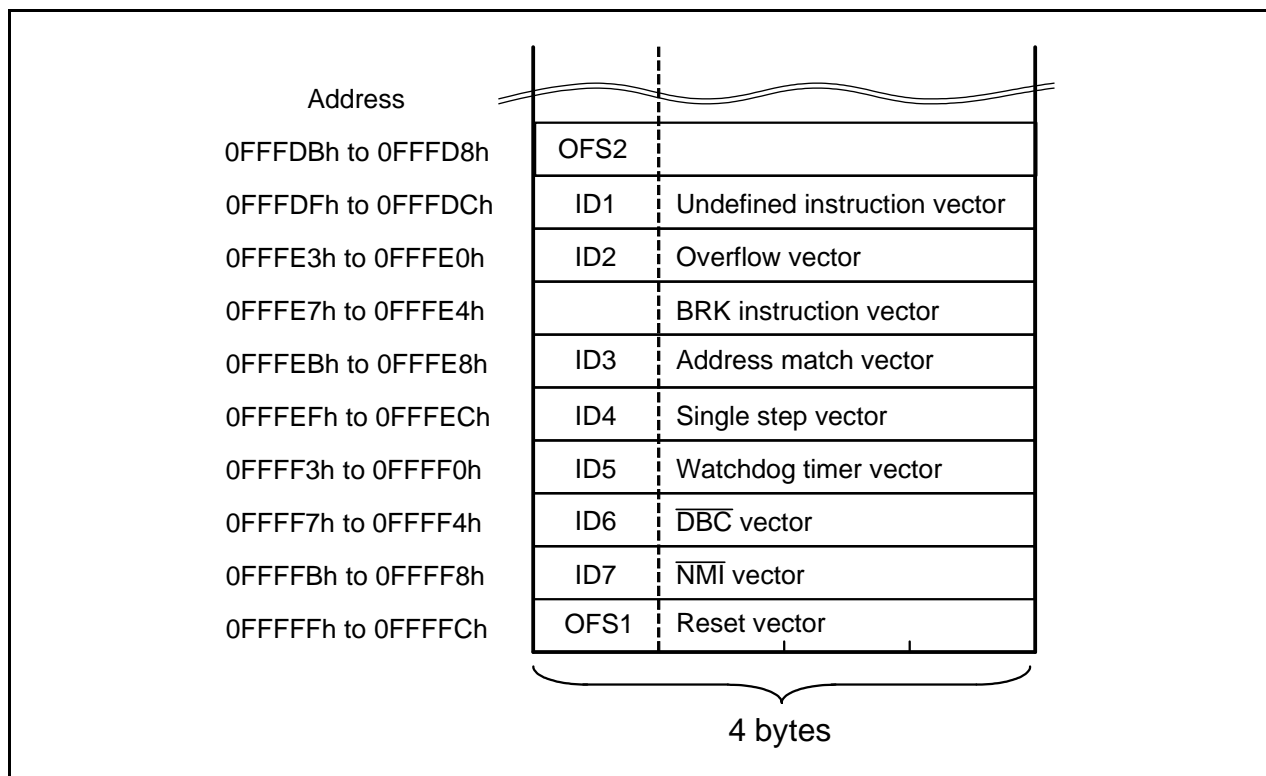
The ID codes are 7-byte data stored consecutively, starting with the first byte, at addresses 0FFFDf, 0FFFE3h, 0FFFEb, 0FFFEf, 0FFFF3h, 0FFFF7h, and 0FFFFb. The flash memory must have a program with the ID codes set in these addresses. Figure 26.25 shows ID Code Storage Addresses.

The ID code of "ALeRASE" in ASCII code is used for forced erase function. The ID code "Protect" in ASCII code is used for standard serial I/O mode disable function. Table 26.20 lists Reserved Word of ID Code. All ID code storage addresses and data must match the combinations listed in Table 26.20. When the forced erase function or standard serial I/O mode disable function is not used, use another combination of ID codes.

**Table 26.20 Reserved Word of ID Code**

ID Code Storage Address		Reserved Word of ID Code (ASCII)	
		ALeRASE	Protect
FFFDf	ID1	41h (upper-case A)	50h (upper-case P)
FFFE3h	ID2	4Ch (upper-case L)	72h (lower-case r)
FFFEb	ID3	65h (lower-case e)	6Fh (lower-case o)
FFFEf	ID4	52h (upper-case R)	74h (lower-case t)
FFFF3h	ID5	41h (upper-case A)	65h (lower-case e)
FFFF7h	ID6	53h (upper-case S)	63h (lower-case c)
FFFFb	ID7	45h (upper-case E)	74h (lower-case t)

All ID code storage addresses and data must match the combinations listed in Table 26.20.



**Figure 26.25 ID Code Storage Addresses**

### 26.9.2 Forced Erase Function

Use the forced erase function in standard serial I/O mode. When the reserved word, "ALeRASE" in ASCII code, is sent from the serial programmer as an ID code, the contents of program ROM 1 and program ROM 2 will all be erased. However, if the ID codes stored in the ID code storage addresses are set to a reserved word other than "ALeRASE" (other than the combination table listed in Table 26.20), the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled), and the ROMCP1 bit in the OFS1 address is 0 (ROM code protect enabled), the forced erase function is ignored and ID code check is executed by the ID code check function. Table 26.21 lists conditions and functions for forced erase function.

When both the ID codes sent from the serial programmer and the ID codes stored in the ID code storage addresses correspond to the reserved word "ALeRASE", program ROM 1 and program ROM 2 will be erased. However, when the serial programmer sends other than "ALeRASE", even if the ID codes stored in the ID code storage addresses are "ALeRASE", there is no ID match and no command is accepted. The flash memory cannot be operated.

**Table 26.21 Forced Erase Function**

Condition			Function
ID code from serial programmer	Code in ID code storage address	ROMCP1 bit in the OFS1 address	
ALeRASE	ALeRASE	–	Program ROM 1 and program ROM 2 all erase (forced erase function)
	Other than ALeRASE <sup>(1)</sup>	1 (ROM code protect disabled)	
		0 (ROM code protect enabled)	ID code check (ID code check function. No ID match)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID match)
	Other than ALeRASE <sup>(1)</sup>	–	ID code check (ID code check function)

Note:

1. When the combination of the stored addresses is "Protect", refer to 26.9.3 "Standard Serial I/O Mode Disable Function".

### 26.9.3 Standard Serial I/O Mode Disable Function

Use the standard serial I/O mode disable function in standard serial I/O mode. When the ID codes in the ID code stored addresses are set to "Protect" in ASCII code (see Table 26.20 "Reserved Word of ID Code"), the MCU does not communicate with the serial programmer. Therefore, the flash memory cannot be read, written or erased by the serial programmer. User boot mode can be selected even when the ID codes are set to "Protect".

When the ID codes are set to "Protect", the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled), and the ROMCP1 bit in the OFS1 address is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled by the serial programmer. Therefore, the flash memory cannot be read, written, or erased by the serial or parallel programmer.

### 26.9.4 Standard Serial I/O Mode 1

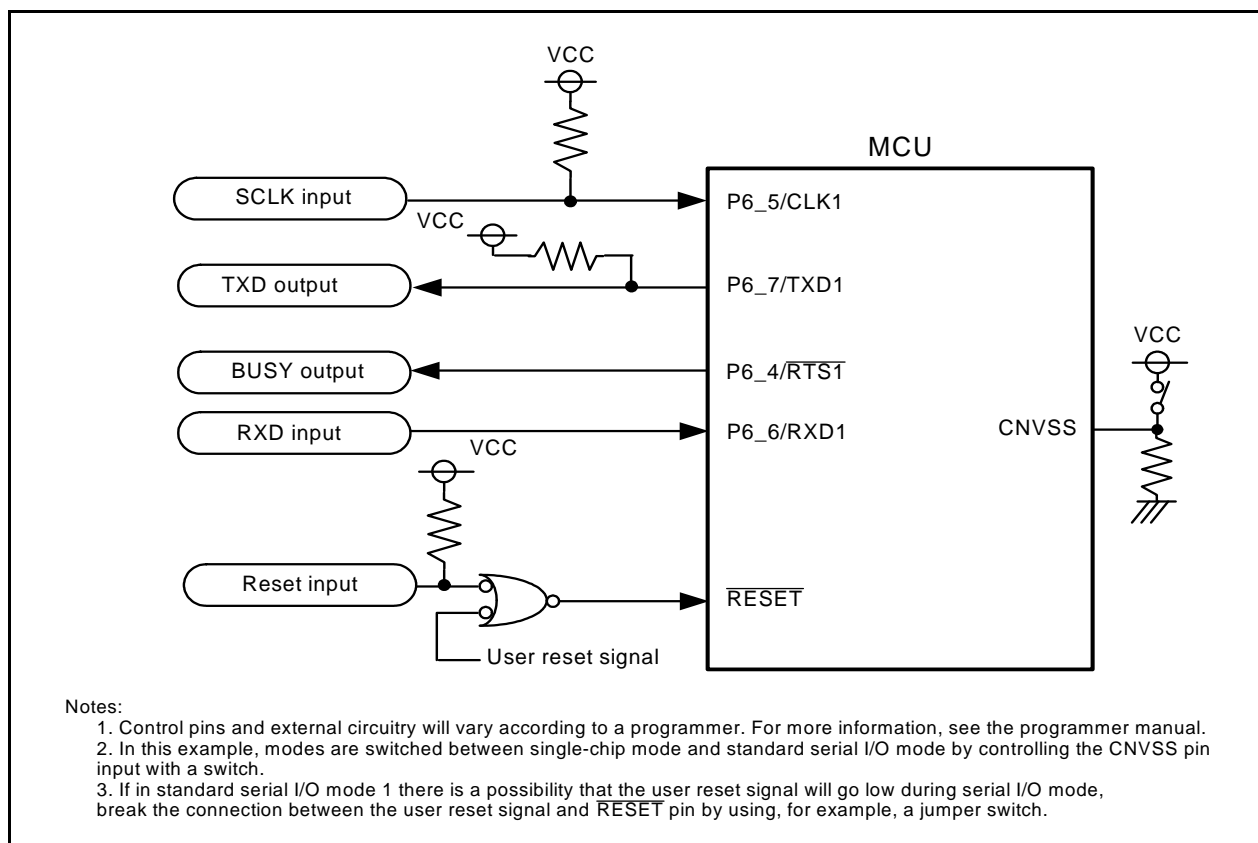
In standard serial I/O mode 1, a serial programmer is connected to the MCU using clock synchronous serial I/O.

**Table 26.22 Pin Functions (Flash Memory Standard Serial I/O Mode 1)**

Pin	Name	I/O	Description
VCC, VSS	Power input		Apply the flash memory program and erase voltage to the VCC pin. Apply 0 V to the VSS pin.
CNVSS	CNVSS	Input	Connect to the VCC pin.
RESET	Reset input	Input	Reset input pin.
XIN	Clock input	Input	Input a high-level signal to the XIN pin and open the XOUT pin when a main clock is not used.
XOUT	Clock output	Output	Connect a ceramic resonator or crystal between pins XIN and XOUT when the main clock is used. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
AVCC, AVSS	Analog power supply input		Connect the AVCC pin to VCC and the AVSS pin to VSS, respectively.
VREF	Reference voltage input	Input	Reference voltage input pin for A/D converter. When using standard serial I/O mode 1, and power supply to VREF is not supplied, connect with VSS.
P0_0 to P0_7	Input port P0	Input	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	Input	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	Input	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	Input	Input a high- or low-level signal or leave open.
P6_0 to P6_3	Input port P6	Input	Input a high- or low-level signal or leave open.
P6_4 / RTS1	BUSY output	Output	BUSY signal output pin
P6_5/CLK1	SCLK input	Input	Serial clock input pin
P6_6 / RXD1	RXD input	Input	Serial data input pin.
P6_7 / TXD1	TXD output	Output	Serial data output pin.
P7_0 to P7_7	Input port P7	Input	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	Input	Input a high- or low-level signal or leave open.
P9_0 to P9_3, P9_5 to P9_7	Input port P9	Input	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	Input	Input a high- or low-level signal or leave open.

**Table 26.23 Setting of Standard Serial I/O Mode 1**

Signal	Input Level
CNVSS	VCC
$\overline{\text{RESET}}$	VSS $\rightarrow$ VCC
SCLK	VCC

**Figure 26.26 Circuit Application in Standard Serial I/O Mode 1**

### 26.9.5 Standard Serial I/O Mode 2

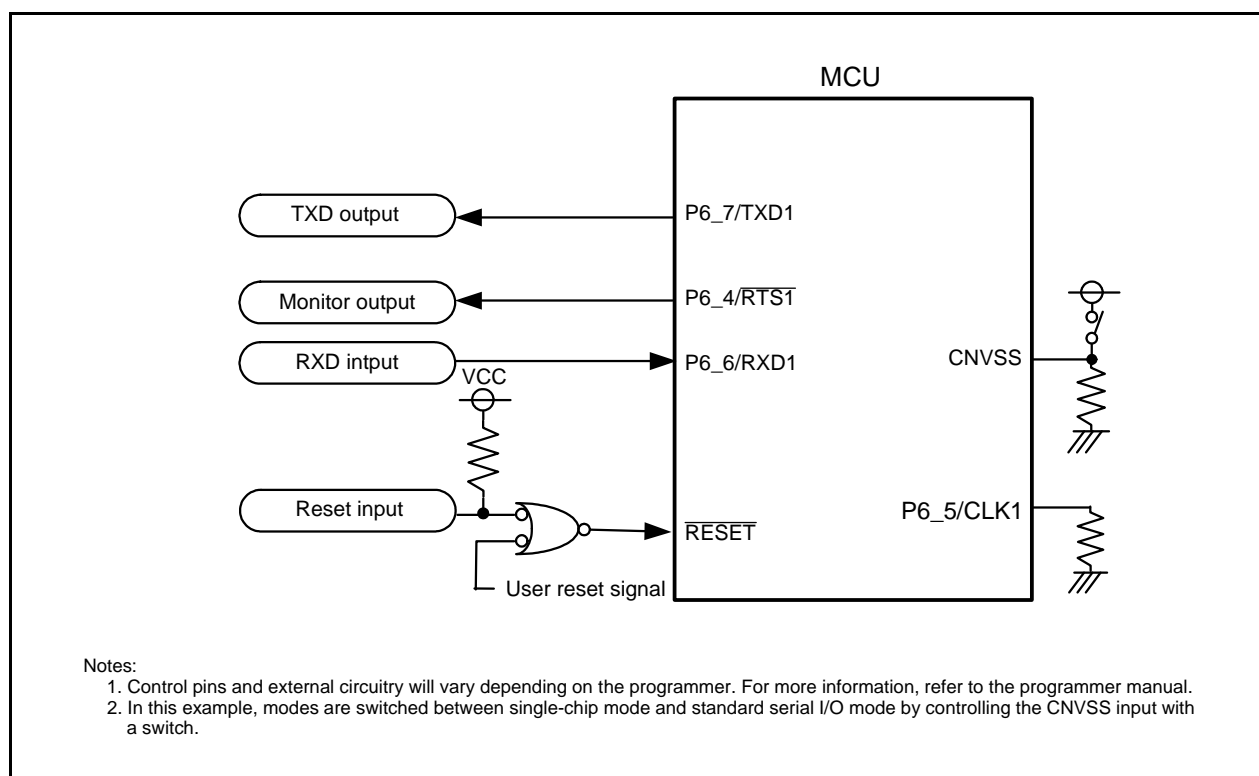
In standard serial I/O mode 2, a serial programmer is connected to the MCU by using 2-wire clock asynchronous serial I/O. The main clock is used.

**Table 26.24 Pin Functions (Flash Memory Standard Serial I/O Mode 2)**

Pin	Name	I/O	Description
VCC, VSS	Power input		Apply the flash memory program and erase voltage to the VCC pin. Apply 0 V to the VSS pin.
CNVSS	CNVSS	I	Connect to the VCC pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
XIN	Clock input	I	Connect a ceramic resonator or crystal between pins XIN and XOUT. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
XOUT	Clock output	O	
AVCC, AVSS	Analog power supply input		Connect the AVCC pin to VCC and the AVSS pin to VSS, respectively.
VREF	Reference voltage input	I	Reference voltage input pin for A/D converter. When using standard serial I/O mode 2, and power supply to VREF is not supplied, connect with VSS.
P0_0 to P0_7	Input port P0	I	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	I	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	I	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	I	Input a high- or low-level signal or leave open.
P6_0 to P6_3	Input port P6	I	Input a high- or low-level signal or leave open.
P6_4 / $\overline{\text{RTS1}}$	BUSY output	O	Monitor signal output pin for checking the boot program operation.
P6_5/CLK1	SCLK input	I	Input a low-level signal
P6_6 / RXD1	RXD input	I	Serial data input pin.
P6_7 / TXD1	TXD output	O	Serial data output pin.
P7_0 to P7_7	Input port P7	I	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	I	Input a high- or low-level signal or leave open.
P9_0 to P9_3, P9_5 to P9_7	Input port P9	I	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	I	Input a high- or low-level signal or leave open.

**Table 26.25 Setting of Standard Serial I/O Mode 2**

Signal	Input Level
CNVSS	VCC
$\overline{\text{RESET}}$	VSS $\rightarrow$ VCC
P6_5/CLK1	VSS

**Figure 26.27 Circuit Application in Standard Serial I/O Mode 2**

## 26.10 Parallel I/O Mode

In parallel I/O mode, program ROM 1, program ROM 2, and data flash can be rewritten using a parallel programmer supporting the M16C/5L Group, M16C/56 Group. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.

### 26.10.1 ROM Code Protect Function

The ROM code protect function disables the flash memory from being read or rewritten during parallel I/O mode. Refer to 26.4.1 "Optional Function Select Address 1 (OFS1)". The OFS1 address is located in block 0 of program ROM 1.

When the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled) and the ROMCP1 bit is set to 0, the ROM code protect function is enabled.

To cancel ROM code protect, erase block 0 including the OFS1 address using standard serial I/O mode or CPU rewrite mode.

## 26.11 Notes on Flash Memory

### 26.11.1 OFS1 Address, OFS2 Address, and ID Code Storage Address

The OFS1 address, OFS2 address, and ID code storage address are part of flash memory. When writing a program to flash memory, write an appropriate value to those addresses simultaneously.

In the OFS1 address, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected. The OFS1 address is 0FFFFFFh. This is the most significant address of block 0 in program ROM 1 and upper address of reset vector. Also, OFS2 address and the ID code storage address is in block 0 and upper address of the interrupt vector.

The ID code check function cannot be disabled. Even if the protect using the ID code check function is unnecessary, input the appropriate ID code when using a serial programmer or debugger. Without the appropriate ID code, the serial programmer or debugger cannot be used.

ex) Set FEh to the OFS1 address, and set FFh to the OFS2 address

When using an address control instruction and logical addition:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
```

RESET:

```
.lword start | 0FE00000h
```

When using an address control instruction:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
```

RESET:

```
.addr start
.byte 0FEh
```

(Program format varies depending on the compiler. Refer to the compiler manual.)

### 26.11.2 Reading Data Flash

When  $3.0\text{ V} < V_{CC} \leq 5.5\text{ V}$  and  $f(\text{BCLK}) \geq 20\text{ MHz}$ , one wait must be inserted to execute the program on the data flash and read the data. Set the PM17 in the PM1 register or FMR17 bit in the FMR1 register to insert one wait.

### 26.11.3 CPU Rewrite Mode

#### 26.11.3.1 Operating Speed

Select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

#### 26.11.3.2 CPU Rewrite Mode Select

Change FMR01 bit in the FMR0 register, FMR11 bit in the FMR1 register, and FMR60 bit in the FMR6 register while in the following state:

- The PM24 bit in the PM2 register is 0 ( $\overline{\text{NMI}}$  interrupt disabled).
- High is input to the  $\overline{\text{NMI}}$  pin.

Change the FMR60 bit while the FMR00 bit in the FMR0 register is 1 (ready).

#### 26.11.3.3 Prohibited Instructions

Do not use the following instructions in EW0 mode:

UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

#### 26.11.3.4 Interrupts (EW0 Mode and EW1 Mode)

- Do not use an address match interrupt during command execution because the address match interrupt vector is located in ROM.
- Do not use a non-maskable interrupt during block 0 erase because fixed vector is located in block 0.

#### 26.11.3.5 Rewrite (EW0 Mode)

If the power supply voltage drops while rewriting the block where the rewrite control program is stored, the rewrite control program is not correctly rewritten. This may prevent the flash memory from being rewritten. If this error occurs, use standard serial I/O mode or parallel I/O mode for rewriting.

#### 26.11.3.6 Rewrite (EW1 Mode)

Do not rewrite any blocks in which the rewrite control program is stored.

#### 26.11.3.7 DMA transfer

In EW0 mode, do not use flash memory as a source of the DMA transfer.

In EW1 mode, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is 0 (auto programming or auto erasing).

#### 26.11.3.8 Wait Mode

To enter wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction.

#### 26.11.3.9 Stop Mode

To enter stop mode, set the FMR01 bit to 0 (CPU rewrite mode disabled), and then disable DMA transfer before setting the CM10 bit in the CM 1 register to 1 (stop mode).



### 26.11.3.10 Software Command

Observe the notes below when using the following commands.

- Program
- Block erase
- Lock bit program
- Read lock bit status
- Block blank check

- (a) The FMR00 bit in the FMR0 register indicates the status while executing these commands. Do not execute other commands while the FMR00 bit is 0 (busy).
- (b) Use these commands in 40 MHz on-chip oscillator mode, high-speed mode, medium-speed mode, and PLL operating mode. Do not change clock modes while the FMR00 bit in the FMR0 register is 0 (busy).
- (c) After executing the program, block erase, or lock bit program command, perform a full status check per command (Do not execute multiple commands or same command more than once before performing a full status check).
- (d) Do not execute the program, block erase, lock bit program, or block blank check command when either or both bits FMR06 and FMR07 in the FMR0 register are 1 (error).
- (e) Do not use these commands in slow read mode (when the FMR22 bit is 1) or low current consumption read mode (when both bits FMR22 and FMR23 are 1).

### 26.11.3.11 Program and Erase Cycles and Execution Time

Execution time of the program, block erase, and lock bit program commands becomes longer as the number of programming and erasing increases.

### 26.11.3.12 Suspending the Auto-Erase and Auto-Program Operations

When the program, block erase, and lock bit program commands are suspended, the blocks for those commands must be erased. Execute the program and lock bit program commands again after erasing.

Those commands are suspended by the following reset or interrupts:

- Hardware, power-on, voltage monitor 0, voltage monitor 2, oscillator stop detect, watchdog timer, software resets.
- $\overline{\text{NMI}}$ , watchdog timer, oscillator stop/restart detect, and voltage monitor 2 interrupts.

## 26.11.4 User Boot

### 26.11.4.1 User Boot Mode Program

Note the following when using user boot mode:

- When using user boot mode, make sure to allocate the program to be executed to program ROM 2.
- The LVDAS bit in the OFS1 address and bits WDTRCS1 and WDTRCS0 in the OFS2 address are disabled in boot mode.
- When restarting the MCU in user boot mode after starting it in user boot mode, RAM becomes undefined.
- If addresses 13FF8h to 13FFBh are all 00h, the MCU does not enter standard serial I/O mode. Therefore, the programmer or on-chip debugger cannot be connected.
- As the reset sequence differs, the time necessary for starting the program is longer than in single-chip mode.
- Functions in user boot mode cannot be debugged by the on-chip debugging emulator or full spec emulator.
- While using user boot mode, do not change the input level of the pin used for user boot entry. However, if there is a possibility that the input level may change, perform the necessary processes in user boot mode, then restart the MCU in single-chip mode before the input level changes.
- To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

## 27. Electrical Characteristics

J-Version

### 27.1 Electrical Characteristics (J-Version, Common to 3 V and 5 V)

#### 27.1.1 Absolute Maximum Rating

Table 27.1 Absolute Maximum Ratings

Symbol	Characteristic		Condition	Rated Value	Unit
$V_{CC}$	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
$AV_{CC}$	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
$V_{REF}$	Analog reference voltage			-0.3 to $V_{CC} + 0.1$ <sup>(1)</sup>	V
$V_I$	Input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS		-0.3 to $V_{CC} + 0.3$	V
$V_O$	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XOUT		-0.3 to $V_{CC} + 0.3$	V
$P_d$	Power consumption		$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	300	mW
$T_{opr}$	Operating temperature range	While CPU operation		-40 to 85	°C
		While flash memory program and erase operation	Programming area	0 to 60	
			Data area	-40 to 85	
$T_{stg}$	Storage temperature range			-65 to 150	°C

Note:

1. Maximum value is 6.5 V.

## 27.1.2 Recommended Operating Conditions

**Table 27.2 Operating Conditions (1)**

$V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -40^{\circ}\text{C to }85^{\circ}\text{C}$  unless otherwise specified.

Symbol	Characteristic		Standard			Unit	
			Min.	Typ.	Max.		
$V_{CC}$	Supply voltage		3.0		5.5	V	
$AV_{CC}$	Analog supply voltage			$V_{CC}$		V	
$V_{SS}$	Ground voltage			0		V	
$AV_{SS}$	Analog ground voltage			0		V	
$V_{IH}$	High level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	Input level $0.50 V_{CC}$	$0.7 V_{CC}$	$V_{CC}$	V	
			Input level $0.70 V_{CC}$	$0.85 V_{CC}$	$V_{CC}$	V	
		XIN, $\overline{\text{RESET}}$ , CNVSS			$0.8 V_{CC}$	$V_{CC}$	
		SDAMM, SCLMM		When I <sup>2</sup> C-bus input level selected	$0.7 V_{CC}$	$V_{CC}$	V
			When SMBUS input level selected	2.1	$V_{CC}$	V	
$V_{IL}$	Low level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	Input level $0.50 V_{CC}$	0	$0.3 V_{CC}$	V	
			Input level $0.70 V_{CC}$	0	$0.45 V_{CC}$	V	
		XIN, $\overline{\text{RESET}}$ , CNVSS			0	$0.2 V_{CC}$	V
		SDAMM, SCLMM		When I <sup>2</sup> C-bus input level selected	0	$0.3 V_{CC}$	V
			When SMBUS input level selected	0	0.8	V	
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-80.0	mA	
$I_{OH(peak)}$	High level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-10.0	mA	
$I_{OH(avg)}$	High level average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-5.0	mA	
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			80.0	mA	
$I_{OL(peak)}$	Low level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			10.0	mA	
$I_{OL(avg)}$	Low level average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			5.0	mA	
$f_{(XIN)}$	Main clock input oscillation frequency (2)		0		20	MHz	
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz	
$f_{(PLL)}$	PLL clock oscillation frequency (2)		10		32	MHz	
$f_{(BCLK)}$	CPU operation frequency		0		32	MHz	
$t_{su(PLL)}$	Wait time to stabilize PLL frequency synthesizer				1	ms	

Notes:

- The mean output current is the mean value within 100 ms.
- Refer to Figure 27.1 "Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency" for the relationship between main clock oscillation frequency/PLL clock oscillation frequency and supply voltage.

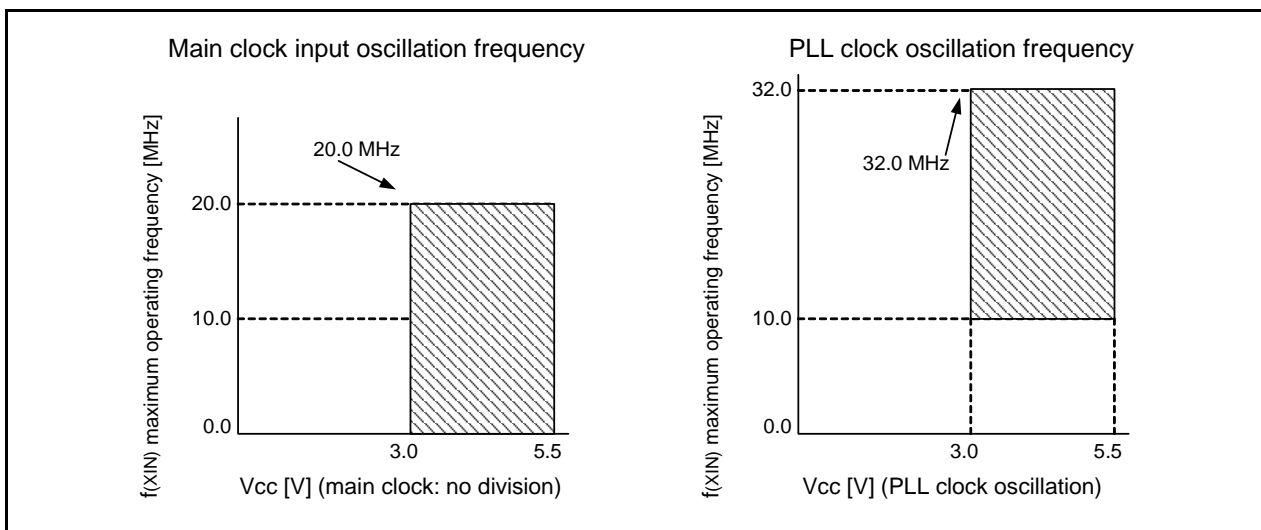


Figure 27.1 Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency

Table 27.3 Recommended Operating Conditions (2/2) (1)

$V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified.

The ripple voltage must not exceed  $V_{r(VCC)}$  and/or  $dV_{r(VCC)}/dt$ .

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	$V_{CC} = 5.0$ V		0.5	Vp-p
		$V_{CC} = 3.0$ V		0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage falling gradient	$V_{CC} = 5.0$ V		0.3	V/ms
		$V_{CC} = 3.0$ V		0.3	V/ms

Note:

1. The device is operationally guaranteed under these operating conditions.

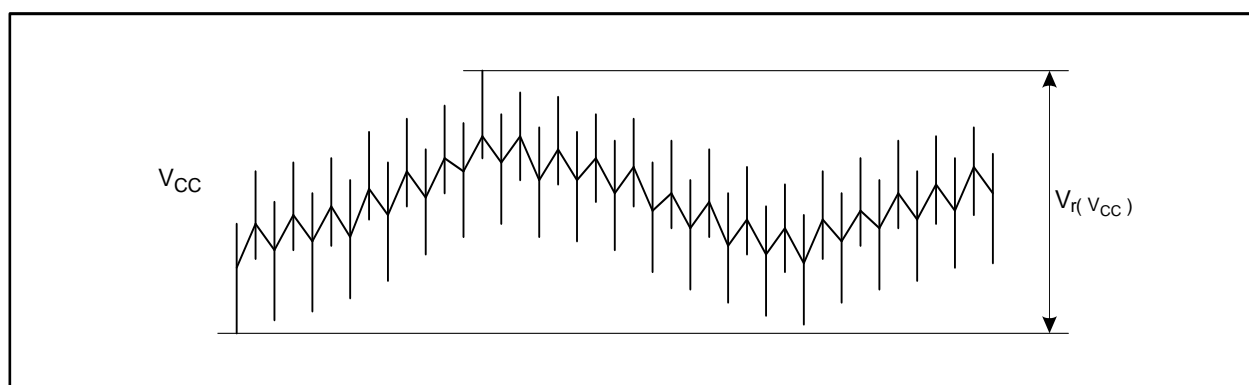


Figure 27.2 Ripple Waveform

J-Version

### 27.1.3 A/D Conversion Characteristics

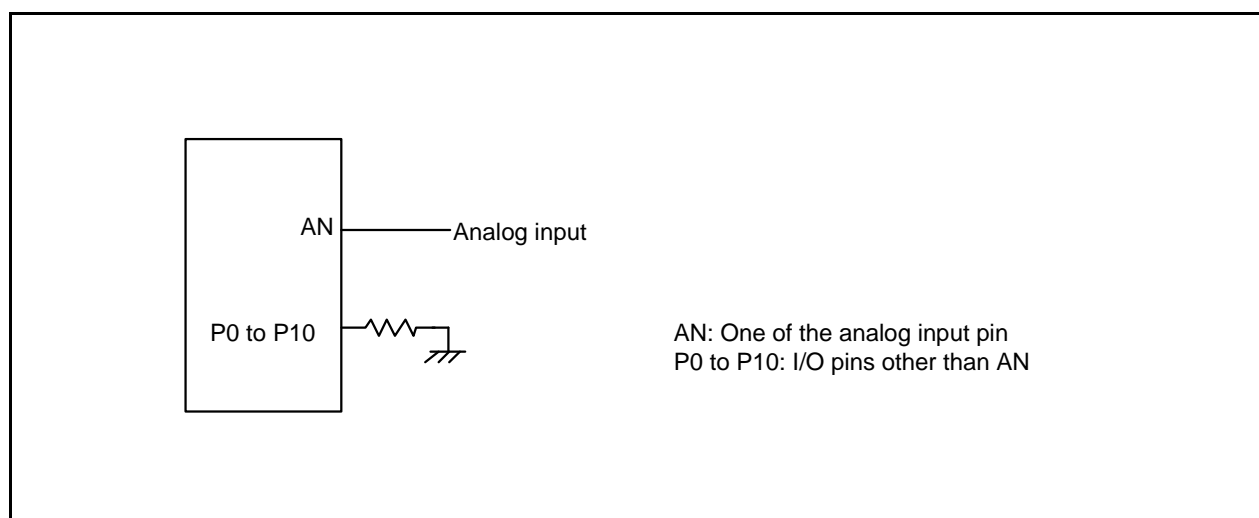
**Table 27.4 A/D Conversion Characteristics (1)**

$V_{CC} = AV_{CC} = V_{REF} = 3.0$  to  $5.5$  V,  $V_{SS} = AV_{SS} = 0$  V at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
$I_{NL}$	Integral non-linearity error	$V_{REF} = V_{CC} = 5.0$ V (2)			$\pm 3$	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			$\pm 5$	LSB
—	Absolute accuracy	$V_{REF} = V_{CC} = 5.0$ V (2)			$\pm 3$	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			$\pm 5$	LSB
$\phi_{AD}$	A/D operating clock frequency	$4.0$ V $\leq V_{CC} \leq 5.5$ V	2		25	MHz
		$3.2$ V $\leq V_{CC} \leq 4.0$ V	2		16	MHz
		$3.0$ V $\leq V_{CC} \leq 3.2$ V	2		10	MHz
—	Tolerance level impedance			3		k $\Omega$
$D_{NL}$	Differential non-linearity error	See note 2			$\pm 1$	LSB
—	Offset error	See note 2			$\pm 3$	LSB
—	Gain error	See note 2			$\pm 3$	LSB
$t_{CONV}$	10-bit conversion time	$V_{REF} = V_{CC} = 5$ V, $\phi_{AD} = 25$ MHz	1.60			$\mu\text{s}$
$t_{SAMP}$	Sampling time		0.6			$\mu\text{s}$
$V_{REF}$	Reference voltage		3.0		$V_{CC}$	V
$V_{IA}$	Analog input voltage (3)		0		$V_{REF}$	V

Notes:

1. Use when  $AV_{CC} = V_{CC}$
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to  $V_{SS}$ . See Figure 27.3 "A/D Accuracy Measure Circuit".
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.



**Figure 27.3 A/D Accuracy Measure Circuit**

### 27.1.4 Flash Memory Electrical Characteristics

**Table 27.5 CPU Clock When Operating Flash Memory ( $f_{(BCLK)}$ )**

$V_{CC} = 3.0$  to  $5.5$  V at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				16 (1)	MHz
$f_{(SLOW\_R)}$	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC	35	kHz
	Data flash read				20 (2)	MHz

Notes:

1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using the 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

## J-Version

**Table 27.6 Flash Memory (Program ROM 1, 2) Electrical Characteristics** $V_{CC} = 3.0$  to  $5.5$  V at  $T_{opr} = 0^{\circ}\text{C}$  to  $60^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$	1,000 (2)			times
-	2 words program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		150	4000	$\mu\text{s}$
-	Lock bit program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		70	3000	$\mu\text{s}$
-	Block erase time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f_{(BCLK)}}$	ms
-	Interval from erase start/restart until following suspend request		0			$\mu\text{s}$
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f_{(BCLK)}}$	$\mu\text{s}$
-	Program, erase voltage		3.0		5.5	V
-	Read voltage	$T_{opr} = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	3.0		5.5	V
-	Program, erase temperature		0		60	$^{\circ}\text{C}$
$t_{PS}$	Flash memory circuit stabilization wait time				50	$\mu\text{s}$
-	Data hold time (6)	Ambient temperature = $55^{\circ}\text{C}$	20			year

## Notes:

- Definition of program and erase cycles:  
The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are  $n$  ( $n = 1,000$ ), each block can be erased  $n$  times. For example, if a 64 KB block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
- Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.



## J-Version

**Table 27.7 Flash Memory (Data Flash) Electrical Characteristics** $V_{CC} = 3.0$  to  $5.5$  V at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$	10,000 (2)			times
-	2 words program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		300	4000	$\mu\text{s}$
-	Lock bit program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		140	3000	$\mu\text{s}$
-	Block erase time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f_{(BCLK)}}$	ms
-	Interval from erase start/restart until following suspend request		0			$\mu\text{s}$
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f_{(BCLK)}}$	$\mu\text{s}$
-	Program, erase voltage		3.0		5.5	V
-	Read voltage		3.0		5.5	V
-	Program, erase temperature		-40		85	$^{\circ}\text{C}$
$t_{PS}$	Flash memory circuit stabilization wait time				50	$\mu\text{s}$
-	Data hold time (6)	Ambient temperature = $55^{\circ}\text{C}$	20			year

- Definition of program and erase cycles  
The program and erase cycles refer to the number of per-block erasures.  
If the program and erase cycles are  $n$  ( $n = 10,000$ ), each block can be erased  $n$  times.  
For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
- Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

J-Version

### 27.1.5 Voltage Detector and Power Supply Circuit Electrical Characteristics

**Table 27.8 Voltage Detector 0 Electrical Characteristics**

The measurement condition is  $V_{CC} = 3.0$  to  $5.5$  V,  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{det0}$	Voltage detection level $V_{det0}$	When $V_{CC}$ is falling.	2.70	2.85	3.00	V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts <sup>(1)</sup>	$V_{CC} = 3.0$ to $5.0$ V			100	$\mu\text{s}$

Note:

- Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.

**Table 27.9 Voltage Detector 2 Electrical Characteristics**

The measurement condition is  $V_{CC} = 3.0$  to  $5.5$  V,  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{det2\_0}$	Voltage detection level $V_{det2\_0}$	When $V_{CC}$ is falling		3.21		V
$V_{det2\_1}$	Voltage detection level $V_{det2\_1}$			3.36		V
$V_{det2\_2}$	Voltage detection level $V_{det2\_2}$			3.51		V
$V_{det2\_3}$	Voltage detection level $V_{det2\_3}$			3.66		V
$V_{det2\_4}$	Voltage detection level $V_{det2\_4}$		3.51	3.81	4.11	V
$V_{det2\_5}$	Voltage detection level $V_{det2\_5}$			3.96		V
$V_{det2\_6}$	Voltage detection level $V_{det2\_6}$			4.10		V
$V_{det2\_7}$	Voltage detection level $V_{det2\_7}$			4.25		V
-	Hysteresis width at the rising of $V_{CC}$ in voltage detector 2			0.15		V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts <sup>(1)</sup>	$V_{CC} = 3.0$ to $5.0$ V			100	$\mu\text{s}$

Note:

- Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.

## J-Version

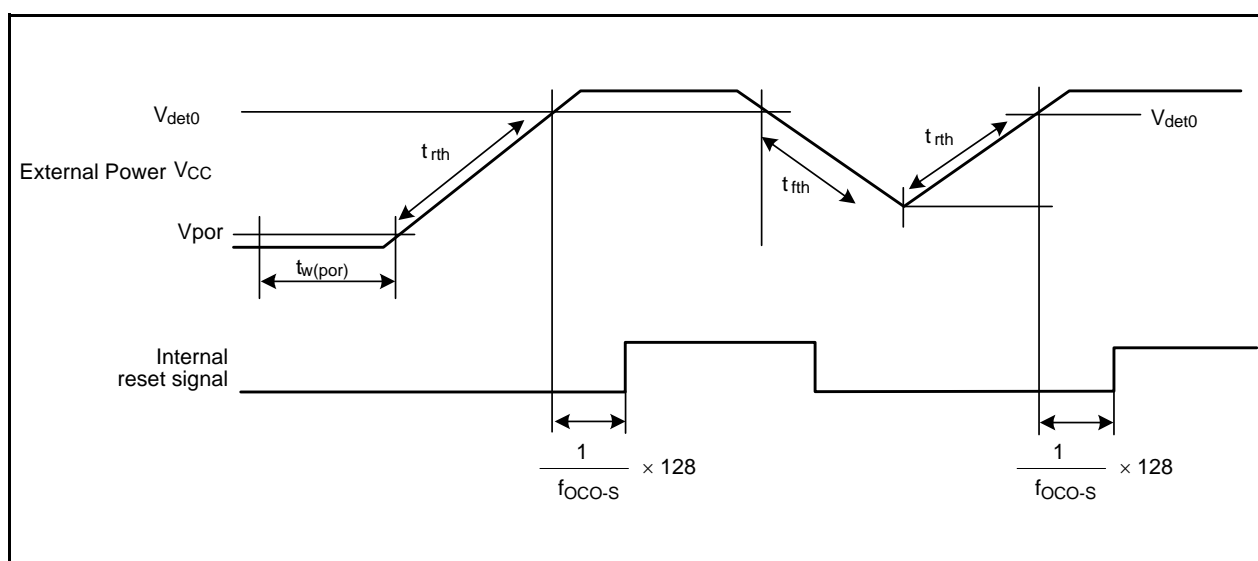
**Table 27.10 Power-On Reset Circuit**

The measurement condition is  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{rth}$	External power $V_{CC}$ rise gradient		2.0		50000	mV/ms
$t_{fth}$	External power $V_{CC}$ fall gradient				50000	mV/ms
$V_{por}$	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:

- To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

**Figure 27.4 Power-On Reset Circuit Electrical Characteristics****Table 27.11 Power Supply Circuit Timing Characteristics**

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	$V_{CC} = 3.0\text{ V to }5.5\text{ V}$			5	ms
$t_{d(R-S)}$	STOP release time				300	$\mu\text{s}$
$t_{d(W-S)}$	Low power mode wait mode release time				300	$\mu\text{s}$

Note:

- When  $V_{CC} = 5\text{ V}$ .

J-Version

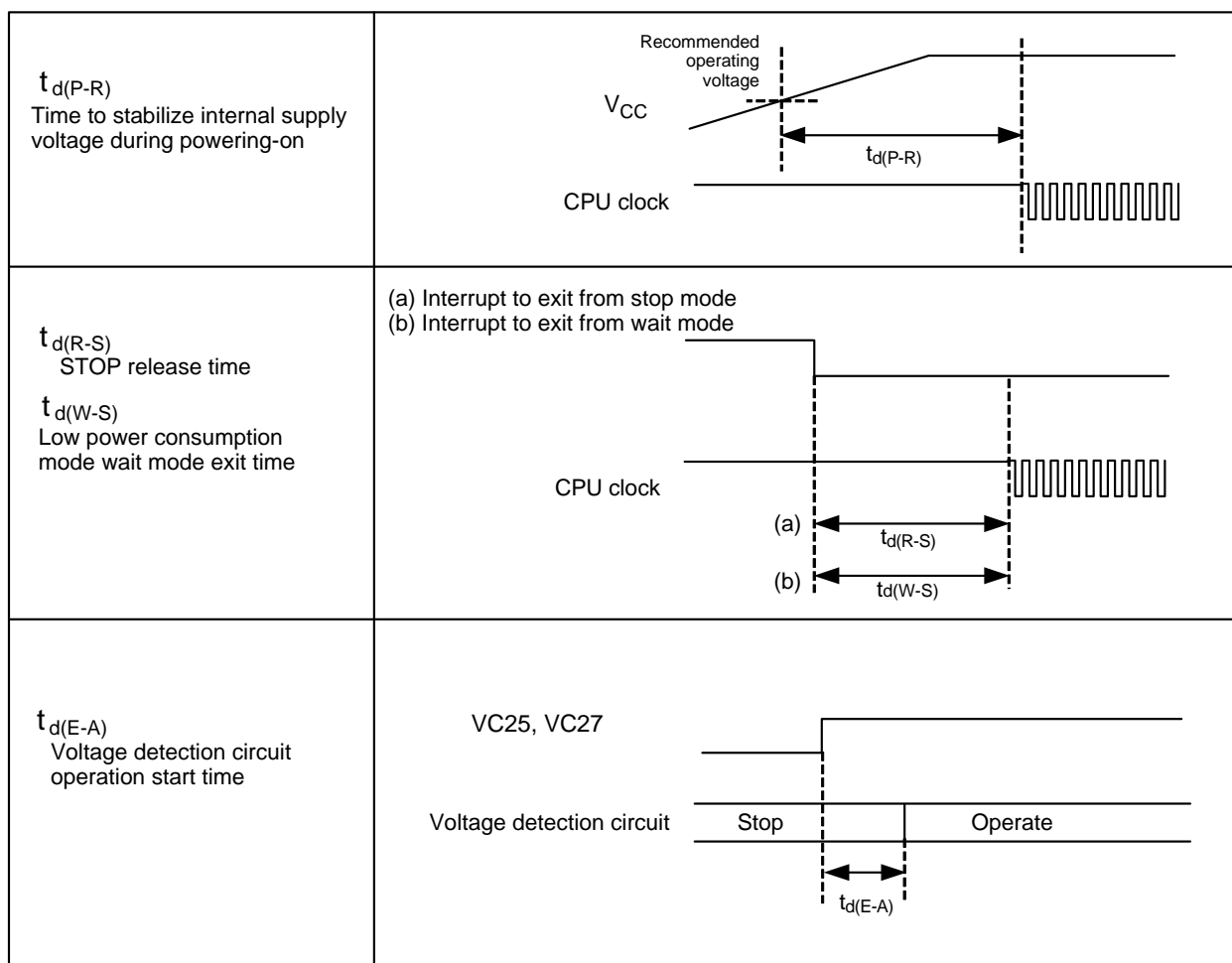


Figure 27.5 Power Supply Circuit Timing Diagram

### 27.1.6 Oscillator Electrical Characteristics

Table 27.12 On-Chip Oscillator Electrical Characteristics

 $V_{CC} = 3.0$  to  $5.5$  V,  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , unless otherwise specified

Symbol	Characteristic	Standard			Unit
		Min.	Typ.	Max.	
$f_{OCO-S}$	125 kHz on-chip oscillator oscillation frequency	100	125	150	kHz
$f_{OCO40M}$	40 MHz on-chip oscillator oscillation frequency	32	40	48	MHz
$f_{WDT}$	Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency	100	125	150	kHz

## 27.2 Electrical Characteristics (J-Version, $V_{CC} = 5\text{ V}$ )

### 27.2.1 Electrical Characteristics

J-Version,  $V_{CC} = 5\text{ V}$

**Table 27.13 Electrical Characteristics (1)**

$V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $f_{(BCLK)} = 32\text{ MHz}$  unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{OH}$	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OH} = -5\text{ mA}$	$V_{CC} - 2.0$		$V_{CC}$	V
$V_{OH}$	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OH} = -200\text{ }\mu\text{A}$	$V_{CC} - 0.3$		$V_{CC}$	V
$V_{OH}$	HIGH output voltage	XOUT	HIGH POWER	$I_{OH} = -1\text{ mA}$	$V_{CC} - 2.0$	$V_{CC}$	V
			LOW POWER	$I_{OH} = -0.5\text{ mA}$	$V_{CC} - 2.0$	$V_{CC}$	
	HIGH output voltage	XCOUT	HIGH POWER	With no load applied		2.5	V
			LOW POWER	With no load applied		1.6	
$V_{OL}$	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OL} = 5\text{ mA}$			2.0	V
$V_{OL}$	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OL} = 200\text{ }\mu\text{A}$			0.45	V
$V_{OL}$	LOW output voltage	XOUT	HIGH POWER	$I_{OL} = 1\text{ mA}$		2.0	V
			LOW POWER	$I_{OL} = 0.5\text{ mA}$		2.0	
	LOW output voltage	XCOUT	HIGH POWER	With no load applied		0	V
			LOW POWER	With no load applied		0	
$V_{T+} - V_{T-}$	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS3, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0		0.2		$0.4V_{CC}$	V
$V_{T+} - V_{T-}$	Hysteresis	RESET		0.2		2.5	V
$V_{T+} - V_{T-}$	Hysteresis	XIN		0.2		0.8	V
$I_{IH}$	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 5\text{ V}$			5.0	$\mu\text{A}$
$I_{IL}$	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 0\text{ V}$			-5.0	$\mu\text{A}$
$R_{PULLUP}$	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$V_I = 0\text{ V}$	30	50	170	$\text{k}\Omega$
$R_{FXIN}$	Feedback resistance	XIN			1.5		$\text{M}\Omega$
$R_{FXCIN}$	Feedback resistance	XCIN			15		$\text{M}\Omega$
$V_{RAM}$	RAM retention voltage		At stop mode	2.0			V

J-Version,  $V_{CC} = 5\text{ V}$ **Table 27.14 Electrical Characteristics (2)** $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified.

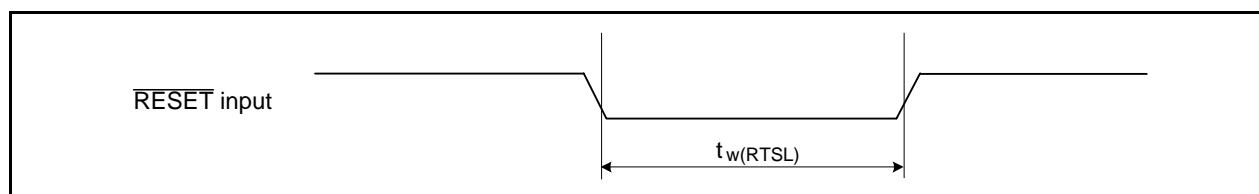
Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
$I_{CC}$	Power supply current ( $V_{CC} = 4.2\text{V}$ to $5.5\text{ V}$ ) In single-chip mode, the output pins are open and other pins are $V_{SS}$	High speed mode	$f_{(BCLK)} = 32\text{ MHz}$ , XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		28	42	mA
			$f_{(BCLK)} = 20\text{ MHz}$ , XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		20	30	mA
			$f_{(BCLK)} = 16\text{ MHz}$ , XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		16		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		20	30	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		5		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	$\mu\text{A}$
		Low power mode	$f_{(BCLK)} = 32\text{ kHz}$ On Flash memory (2) FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		$\mu\text{A}$
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$		20		$\mu\text{A}$
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 85^{\circ}\text{C}$		50		$\mu\text{A}$
		Stop mode	$T_{opr} = 25^{\circ}\text{C}$		3	15	$\mu\text{A}$
			$T_{opr} = 85^{\circ}\text{C}$		30		$\mu\text{A}$
During flash memory program	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 5.0\text{ V}$		20.0		mA		
During flash memory erase	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 5.0\text{ V}$		30.0		mA		
$I_{det2}$	Low voltage detection dissipation current		3		$\mu\text{A}$		
$I_{det0}$	Reset area detection dissipation current		6		$\mu\text{A}$		

Note:

1. This indicates the memory in which the program to be executed exists.

J-Version,  $V_{CC} = 5\text{ V}$ **27.2.2 Timing Requirements (Peripheral Functions and Others)** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.2.2.1 Reset Input ( $\overline{\text{RESET}}$  Input)****Table 27.15 Reset Input ( $\overline{\text{RESET}}$  Input)**

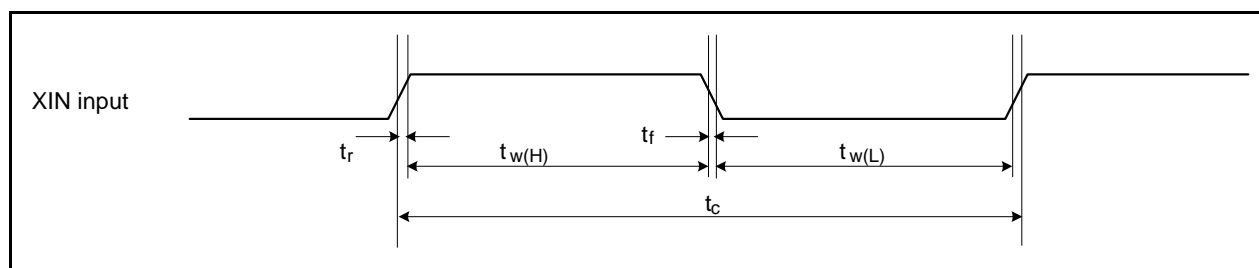
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(\text{RSTL})}$	$\overline{\text{RESET}}$ input low pulse width	10		$\mu\text{s}$

**Figure 27.6 Reset Input ( $\overline{\text{RESET}}$  Input)****27.2.2.2 External Clock Input****Table 27.16 External Clock Input (XIN Input) (1)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	50		ns
$t_{w(\text{H})}$	External clock input high pulse width	20		ns
$t_{w(\text{L})}$	External clock input low pulse width	20		ns
$t_r$	External clock rise time		9	ns
$t_f$	External clock fall time		9	ns

Note:

1. The condition is  $V_{CC} = 5.0\text{V}$ .

**Figure 27.7 External Clock Input (XIN Input)**

J-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.2.2.3 Timer A Input****Table 27.17 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

**Table 27.18 Timer A Input (Gating Input in Timer Mode)**

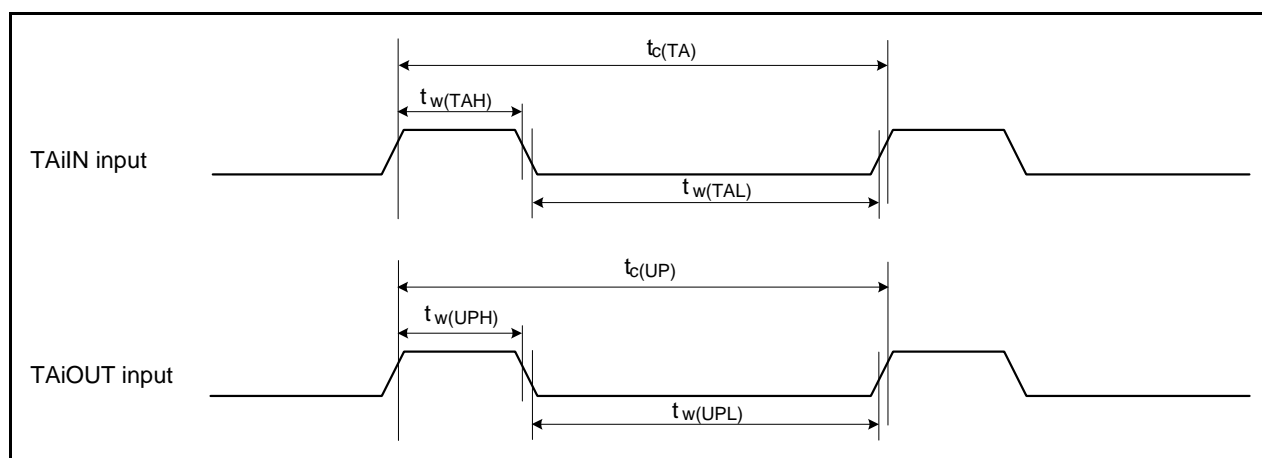
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

**Table 27.19 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

**Table 27.20 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)**

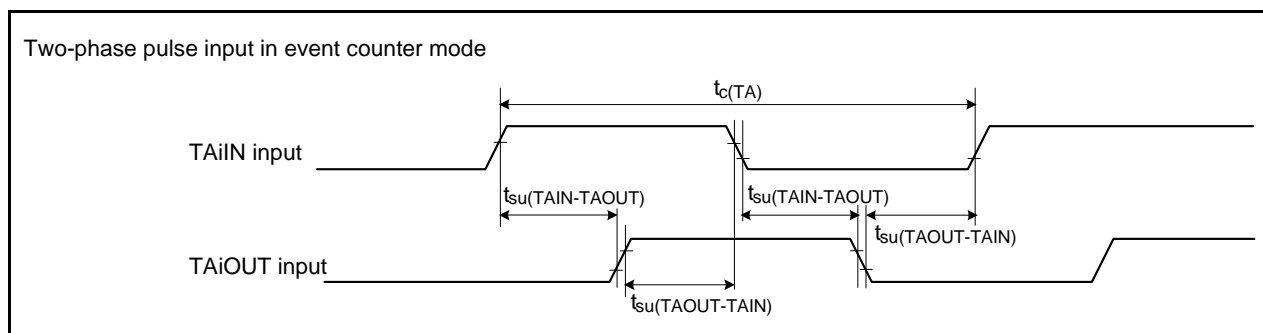
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

**Figure 27.8 Timer A Input**



J-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **Table 27.21 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

**Figure 27.9 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

J-Version,  $V_{CC} = 5\text{ V}$

**Timing Requirements**

( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified)

**27.2.2.4 Timer B Input**

**Table 27.22 Timer B Input (Counter Input in Event Counter Mode)**

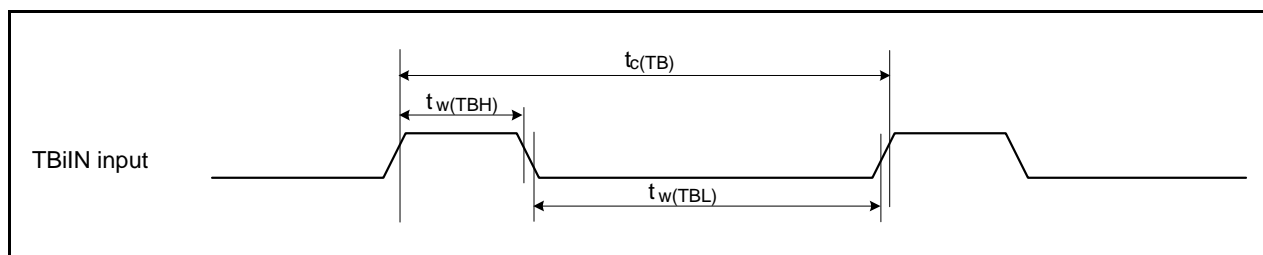
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	80		ns

**Table 27.23 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

**Table 27.24 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns



**Figure 27.10 Timer B Input**

J-Version,  $V_{CC} = 5\text{ V}$

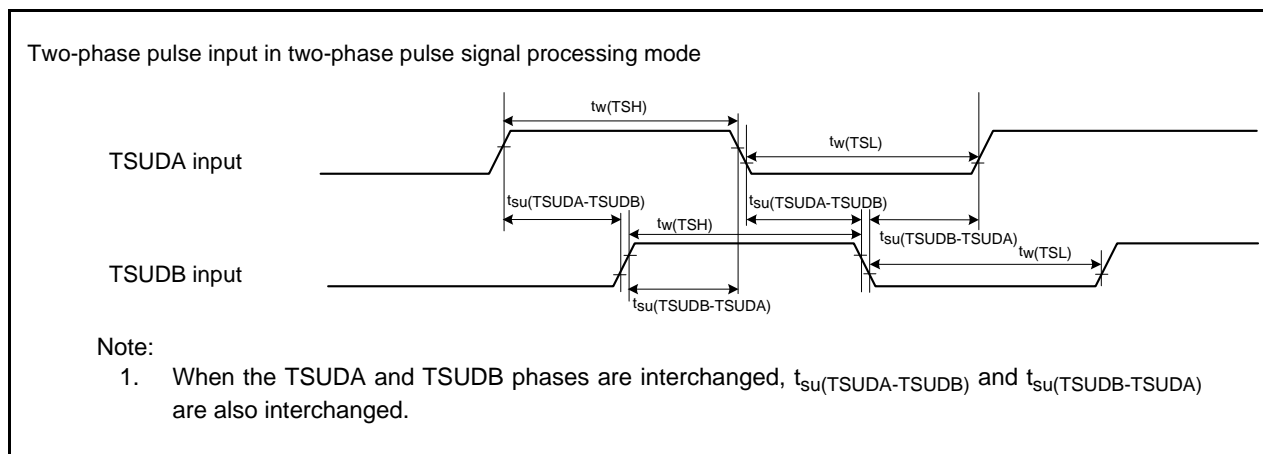
**Timing Requirements**

( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified)

**27.2.2.5 Timer S Input**

**Table 27.25 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

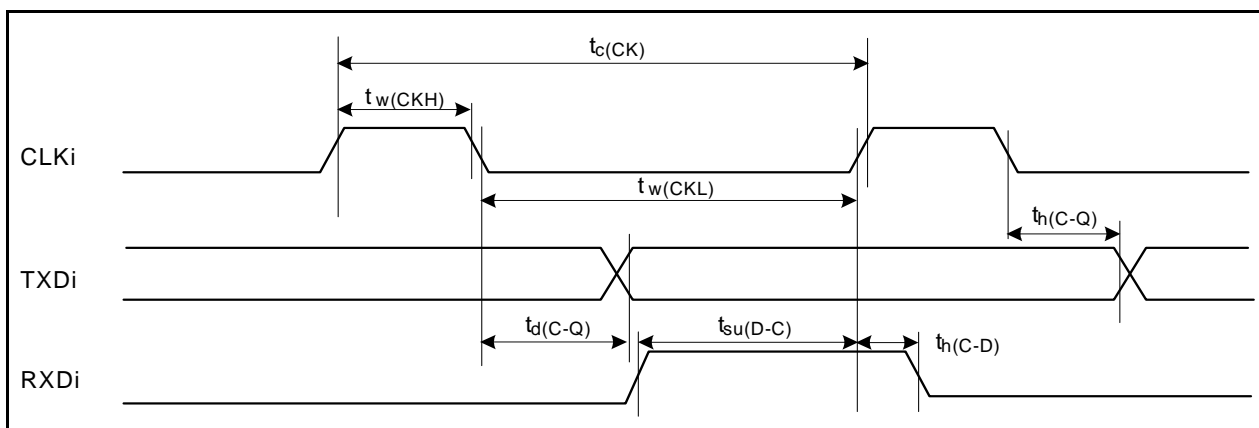
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_w(\text{TSH})$	TSUDA, TSUDB input high pulse width	2		$\mu\text{S}$
$t_w(\text{TSL})$	TSUDA, TSUDB input low pulse width	2		$\mu\text{S}$
$t_{su}(\text{TSUDA-TSUDB})$	TSUDB input setup time	1		$\mu\text{S}$
$t_{su}(\text{TSUDB-TSUDA})$	TSUDA input setup time	1		$\mu\text{S}$



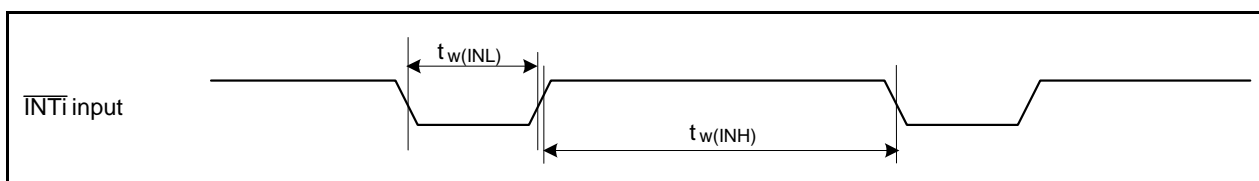
**Figure 27.11 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

J-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.2.2.6 Serial Interface****Table 27.26 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

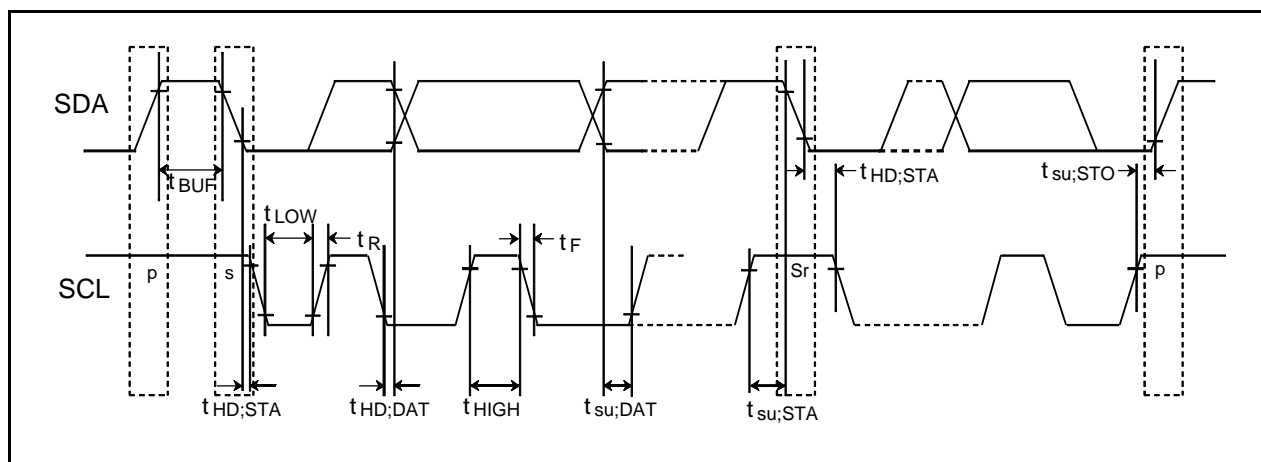
**Figure 27.12 Serial Interface****27.2.2.7 External Interrupt  $\overline{INTi}$  Input****Table 27.27 External Interrupt  $\overline{INTi}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

**Figure 27.13 External Interrupt  $\overline{INTi}$  Input**

J-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.2.2.8 Multi-master I<sup>2</sup>C-bus****Table 27.28 Multi-master I<sup>2</sup>C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
$t_{BUF}$	Bus free time	4.7		1.3		$\mu\text{s}$
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		$\mu\text{s}$
$t_{LOW}$	Hold time in SCL clock 0 status	4.7		1.3		$\mu\text{s}$
$t_R$	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	$\mu\text{s}$
$t_{HIGH}$	Hold time in SCL clock 1 status	4.0		0.6		$\mu\text{s}$
$t_F$	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		$\mu\text{s}$
$t_{su;STO}$	Stop condition setup time	4.0		0.6		$\mu\text{s}$

**Figure 27.14 Multi-master I<sup>2</sup>C-bus**

## 27.3 Electrical Characteristics (J-Version, $V_{CC} = 3\text{ V}$ )

### 27.3.1 Electrical Characteristics

J-Version,  $V_{CC} = 3\text{ V}$

**Table 27.29 Electrical Characteristics (1)**

$V_{CC} = 3.0\text{ to }3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -40^{\circ}\text{C to }85^{\circ}\text{C}$ ,  $f_{(BCLK)} = 32\text{ MHz}$  unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{OH}$	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OH} = -1\text{ mA}$	$V_{CC}-0.5$		$V_{CC}$	V
$V_{OH}$	HIGH output voltage	XOUT	HIGH POWER	$I_{OH} = -0.1\text{ mA}$	$V_{CC}-0.5$	$V_{CC}$	V
			LOW POWER	$I_{OH} = -50\text{ }\mu\text{A}$	$V_{CC}-0.5$	$V_{CC}$	V
	HIGH output voltage	XCOUT	HIGH POWER	With no load applied		2.5	V
			LOW POWER	With no load applied		1.6	V
$V_{OL}$	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OL} = 1\text{ mA}$			0.5	V
$V_{OL}$	LOW output voltage	XOUT	HIGH POWER	$I_{OL} = 0.1\text{ mA}$		0.5	V
			LOW POWER	$I_{OL} = 50\text{ }\mu\text{A}$		0.5	V
	LOW output voltage	XCOUT	HIGH POWER	With no load applied		0	V
			LOW POWER	With no load applied		0	V
$V_{T+}, V_{T-}$	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS3, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0				$0.4V_{CC}$	V
$V_{T+}, V_{T-}$	Hysteresis	RESET				1.8	V
$V_{T+}, V_{T-}$	Hysteresis	XIN				0.8	V
$I_{IH}$	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 3\text{ V}$			4.0	$\mu\text{A}$
$I_{IL}$	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 0\text{ V}$			-4.0	$\mu\text{A}$
$R_{PULLUP}$	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$V_I = 0\text{ V}$	50	100	500	k $\Omega$
$R_{FXIN}$	Feedback resistance	XIN			3.0		M $\Omega$
$R_{FXCIN}$	Feedback resistance	XCIN			25		M $\Omega$
$V_{RAM}$	RAM retention voltage		At stop mode	2.0			V

J-Version,  $V_{CC} = 3\text{ V}$ **Table 27.30 Electrical Characteristics (2)**Topr =  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified.

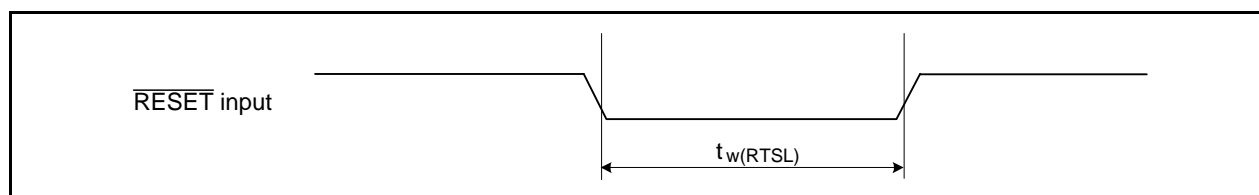
Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
$I_{CC}$	Power supply current ( $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ) In single-chip mode, the output pins are open and other pins are VSS	High speed mode	$f_{(BCLK)} = 32\text{ MHz}$ , XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		26	40	mA
			$f_{(BCLK)} = 20\text{ MHz}$ , XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		19	28	mA
			$f_{(BCLK)} = 16\text{ MHz}$ , XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		15		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		19	28	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		5		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	$\mu\text{A}$
		Low power mode	$f_{(BCLK)} = 32\text{ kHz}$ On Flash memory <sup>(1)</sup> FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		$\mu\text{A}$
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$		20		$\mu\text{A}$
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 85^{\circ}\text{C}$		50		$\mu\text{A}$
		Stop mode	$T_{opr} = 25^{\circ}\text{C}$		2	12	$\mu\text{A}$
$T_{opr} = 85^{\circ}\text{C}$			30		$\mu\text{A}$		
During flash memory program	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 3.0\text{ V}$		20.0		mA		
During flash memory erase	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 3.0\text{ V}$		30.0		mA		
$I_{det2}$	Low voltage detection dissipation current		3		$\mu\text{A}$		
$I_{det0}$	Reset area detection dissipation current		6		$\mu\text{A}$		

Note:

1. This indicates the memory in which the program to be executed exists.

J-Version,  $V_{CC} = 3\text{ V}$ **27.3.2 Timing Requirements (Peripheral Functions and Others)** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.3.2.1 Reset Input ( $\overline{\text{RESET}}$  Input)****Table 27.31 Reset Input ( $\overline{\text{RESET}}$  Input)**

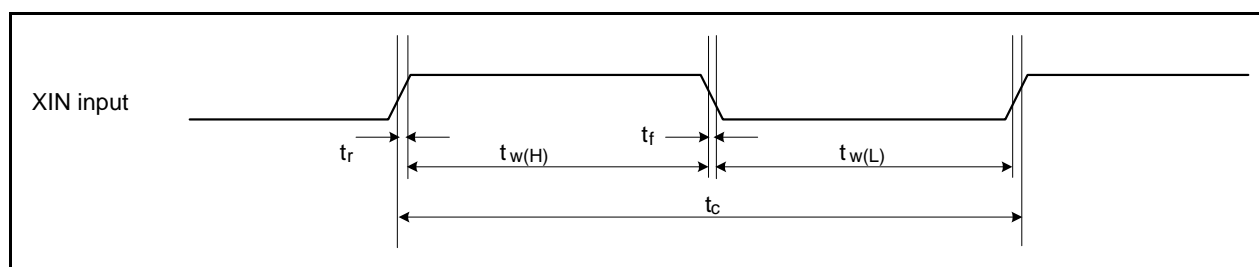
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(\text{RSTL})}$	RESET input low pulse width	10		$\mu\text{s}$

**Figure 27.15 Reset Input ( $\overline{\text{RESET}}$  Input)****27.3.2.2 External Clock Input****Table 27.32 External Clock Input (XIN input) (1)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	50		ns
$t_{w(\text{H})}$	External clock input high pulse width	20		ns
$t_{w(\text{L})}$	External clock input low pulse width	20		ns
$t_r$	External clock rise time		9	ns
$t_f$	External clock fall time		9	ns

Note:

1. The condition is  $V_{CC} = 3.0\text{V}$ .

**Figure 27.16 External Clock Input (XIN Input)**



J-Version,  $V_{CC} = 3\text{ V}$ **Timing Requirements** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.3.2.3 Timer A Input****Table 27.33 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

**Table 27.34 Timer A Input (Gating Input in Timer Mode)**

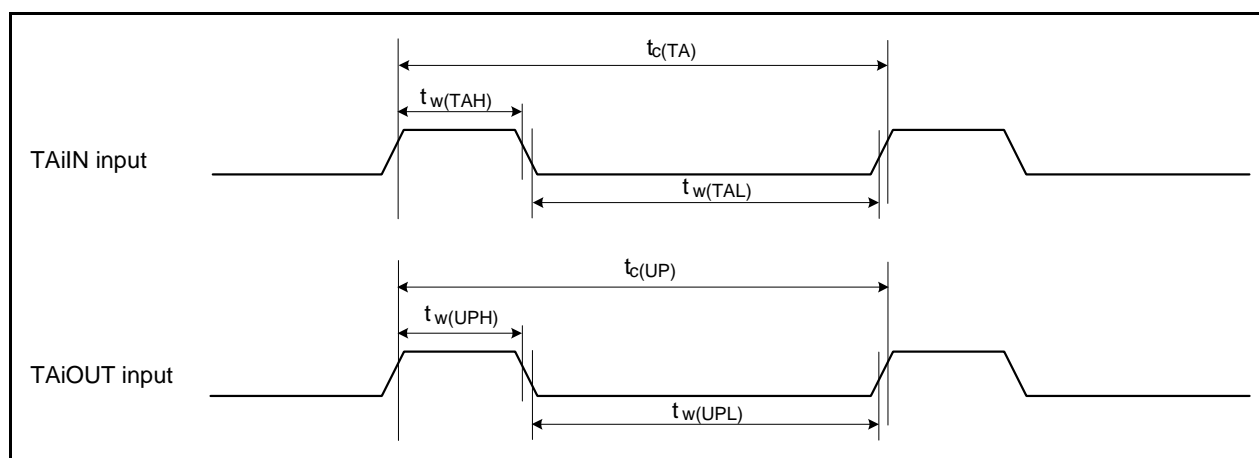
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

**Table 27.35 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

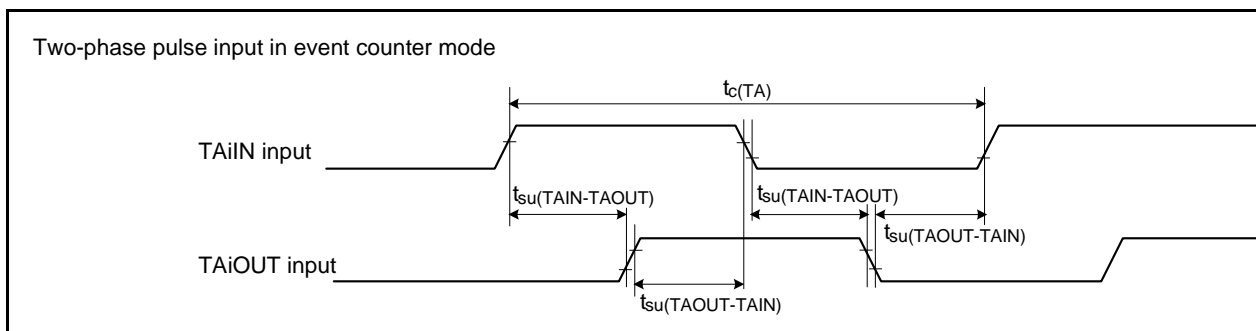
**Table 27.36 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

**Figure 27.17 Timer A Input**

J-Version,  $V_{CC} = 3\text{ V}$ **Timing Requirements** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **Table 27.37 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		$\mu\text{S}$
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

**Figure 27.18 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

J-Version,  $V_{CC} = 3\text{ V}$

**Timing Requirements**

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified)

**27.3.2.4 Timer B Input**

**Table 27.38 Timer B Input (Counter Input in Event Counter Mode)**

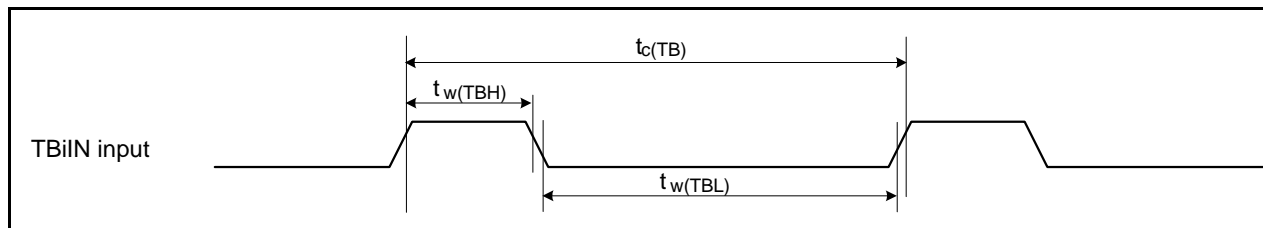
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	120		ns

**Table 27.39 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

**Table 27.40 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns



**Figure 27.19 Timer B Input**

J-Version,  $V_{CC} = 3\text{ V}$

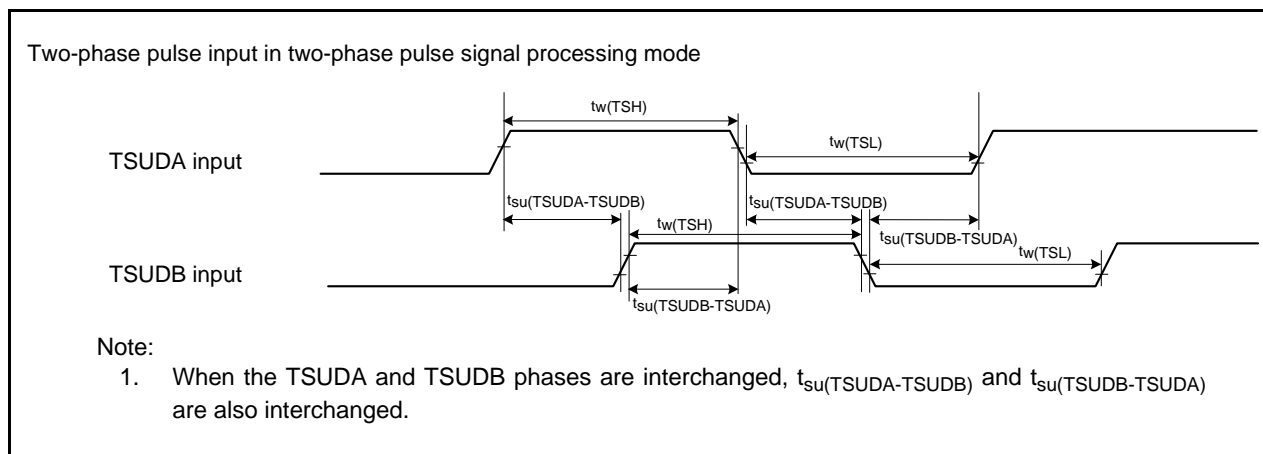
**Timing Requirements**

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified)

**27.3.2.5 Timer S Input**

**Table 27.41 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

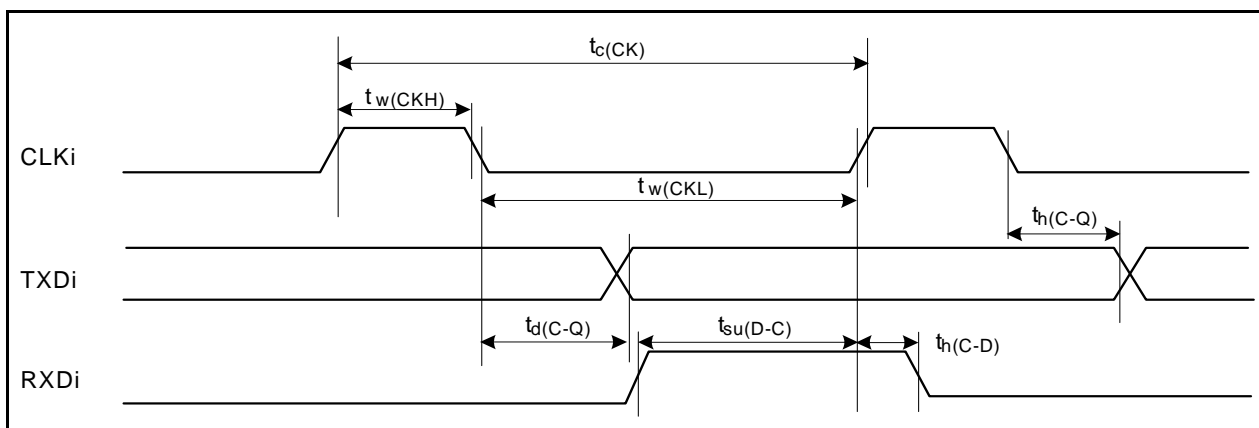
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_w(\text{TSH})$	TSUDA, TSUDB input high pulse width	2		$\mu\text{S}$
$t_w(\text{TSL})$	TSUDA, TSUDB input low pulse width	2		$\mu\text{S}$
$t_{su}(\text{TSUDA-TSUDB})$	TSUDB input setup time	1		$\mu\text{S}$
$t_{su}(\text{TSUDB-TSUDA})$	TSUDA input setup time	1		$\mu\text{S}$



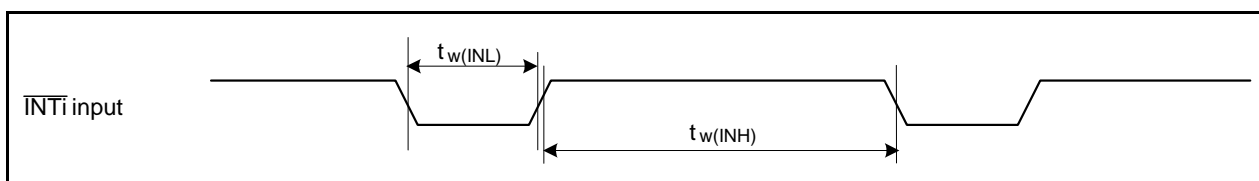
**Figure 27.20 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

J-Version,  $V_{CC} = 3\text{ V}$ **Timing Requirements** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 85^{\circ}\text{C unless otherwise specified})$ **27.3.2.6 Serial Interface****Table 27.42 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

**Figure 27.21 Serial Interface****27.3.2.7 External Interrupt  $\overline{INTi}$  Input****Table 27.43 External Interrupt  $\overline{INTi}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

**Figure 27.22 External Interrupt  $\overline{INTi}$  Input**

J-Version,  $V_{CC} = 3\text{ V}$

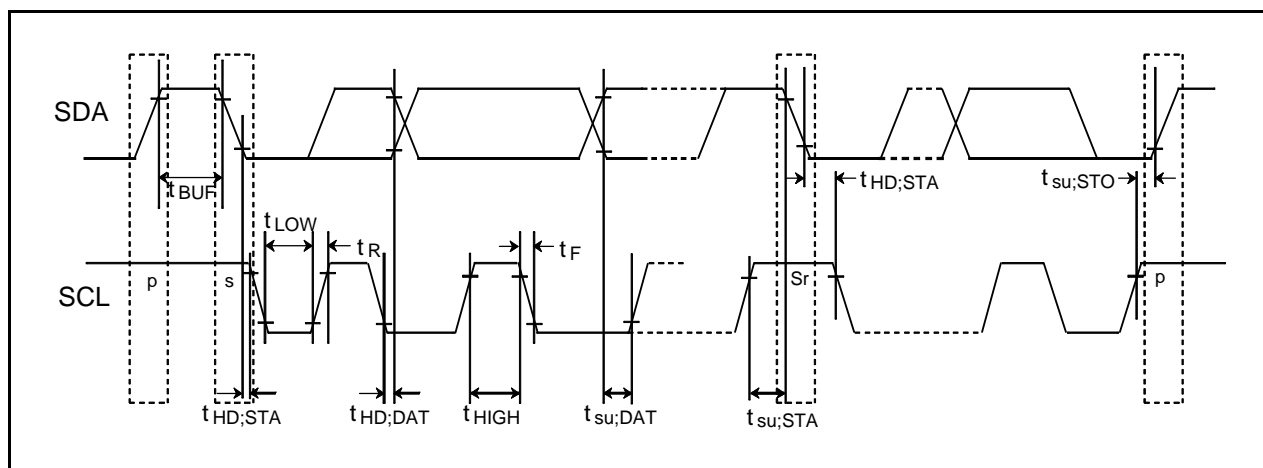
**Timing Requirements**

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise specified)

**27.3.2.8 Multi-master I<sup>2</sup>C-bus**

**Table 27.44 Multi-master I<sup>2</sup>C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
$t_{BUF}$	Bus free time	4.7		1.3		$\mu\text{s}$
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		$\mu\text{s}$
$t_{LOW}$	Hold time in SCL clock 0 status	4.7		1.3		$\mu\text{s}$
$t_R$	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	$\mu\text{s}$
$t_{HIGH}$	Hold time in SCL clock 1 status	4.0		0.6		$\mu\text{s}$
$t_F$	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		$\mu\text{s}$
$t_{su;STO}$	Stop condition setup time	4.0		0.6		$\mu\text{s}$



**Figure 27.23 Multi-master I<sup>2</sup>C-bus**

## K-Version

## 27.4 Electrical Characteristics (K-Version, Common to 3 V and 5 V)

## 27.4.1 Absolute Maximum Rating

Table 27.45 Absolute Maximum Ratings

Symbol	Characteristic		Condition	Rated Value	Unit
$V_{CC}$	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
$AV_{CC}$	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
$V_{REF}$	Analog reference voltage			-0.3 to $V_{CC} + 0.1$ <sup>(1)</sup>	V
$V_I$	Input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS		-0.3 to $V_{CC} + 0.3$	V
$V_O$	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XOUT		-0.3 to $V_{CC} + 0.3$	V
$P_d$	Power consumption		$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	300	mW
			$85^{\circ}\text{C} < T_{opr} \leq 125^{\circ}\text{C}$	250	mW
$T_{opr}$	Operating temperature range	While CPU operation		-40 to 125	°C
		While flash memory program and erase operation	Programming area	0 to 60	
			Data area	-40 to 125	
$T_{stg}$	Storage temperature range			-65 to 150	°C

Note:

1. Maximum value is 6.5 V.

K-Version

## 27.4.2 Recommended Operating Conditions

**Table 27.46 Operating Conditions (1)**
 $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $T_{opr} = -40^{\circ}\text{C to }125^{\circ}\text{C}$  unless otherwise specified.

Symbol	Characteristic		Standard			Unit	
			Min.	Typ.	Max.		
$V_{CC}$	Supply voltage		3.0		5.5	V	
$AV_{CC}$	Analog supply voltage			$V_{CC}$		V	
$V_{SS}$	Ground voltage			0		V	
$AV_{SS}$	Analog ground voltage			0		V	
$V_{IH}$	High level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	Input level 0.50 $V_{CC}$	0.7 $V_{CC}$	$V_{CC}$	V	
			Input level 0.70 $V_{CC}$	0.85 $V_{CC}$	$V_{CC}$	V	
		XIN, $\overline{\text{RESET}}$ , CNVSS		0.8 $V_{CC}$		$V_{CC}$	
		SDAMM, SCLMM	When I <sup>2</sup> C-bus input level selected	0.7 $V_{CC}$		$V_{CC}$	V
When SMBUS input level selected	2.1			$V_{CC}$	V		
$V_{IL}$	Low level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	Input level 0.50 $V_{CC}$	0	0.3 $V_{CC}$	V	
			Input level 0.70 $V_{CC}$	0	0.45 $V_{CC}$	V	
		XIN, $\overline{\text{RESET}}$ , CNVSS		0		0.2 $V_{CC}$	V
		SDAMM, SCLMM	When I <sup>2</sup> C-bus input level selected	0		0.3 $V_{CC}$	V
When SMBUS input level selected	0			0.8	V		
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-80.0	mA	
$I_{OH(peak)}$	High level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-10.0	mA	
$I_{OH(avg)}$	High level average output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-5.0	mA	
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			80.0	mA	
$I_{OL(peak)}$	Low level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			10.0	mA	
$I_{OL(avg)}$	Low level average output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			5.0	mA	
$f_{(XIN)}$	Main clock input oscillation frequency (2)		0		20	MHz	
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz	
$f_{(PLL)}$	PLL clock oscillation frequency (2)		10		32	MHz	
$f_{(BCLK)}$	CPU operation frequency		0		32	MHz	
$t_{su(PLL)}$	Wait time to stabilize PLL frequency synthesizer				1	ms	

Notes:

- The mean output current is the mean value within 100 ms.
- Refer to Figure 27.24 "Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency" for the relationship between main clock oscillation frequency/PLL clock oscillation frequency and supply voltage.



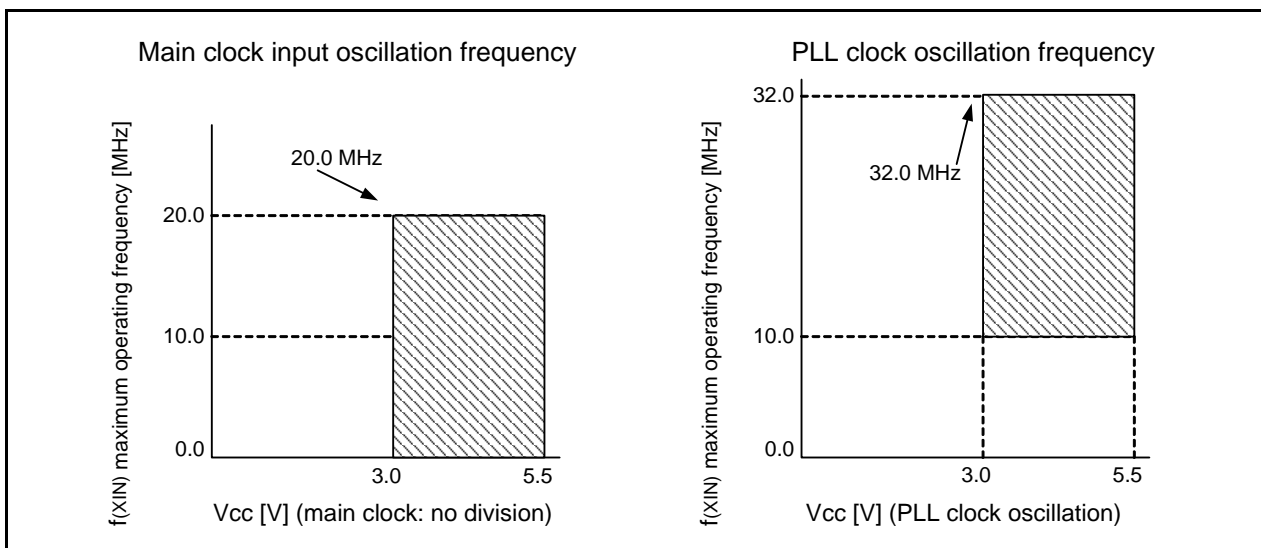


Figure 27.24 Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency

Table 27.47 Recommended Operating Conditions (2/2) (1)

$V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified.

The ripple voltage must not exceed  $V_{r(VCC)}$  and/or  $dV_{r(VCC)}/dt$ .

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	$V_{CC} = 5.0$ V		0.5	Vp-p
		$V_{CC} = 3.0$ V		0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage falling gradient	$V_{CC} = 5.0$ V		0.3	V/ms
		$V_{CC} = 3.0$ V		0.3	V/ms

Note:

- The device is operationally guaranteed under these operating conditions.

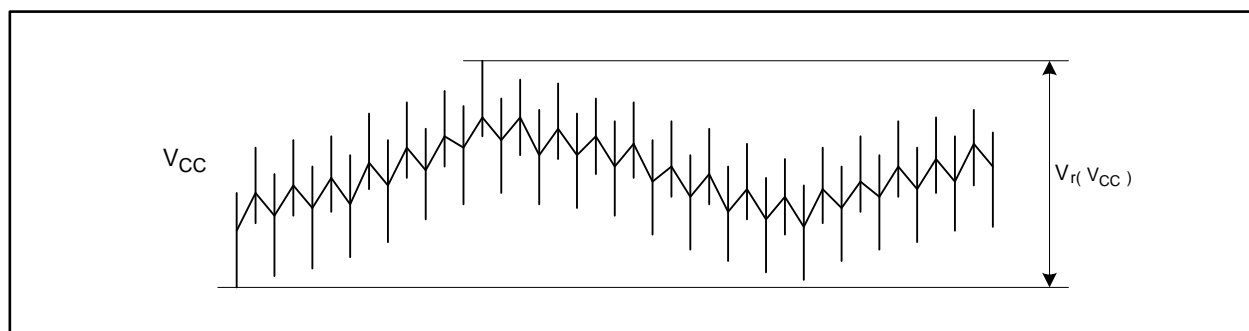


Figure 27.25 Ripple Waveform

K-Version

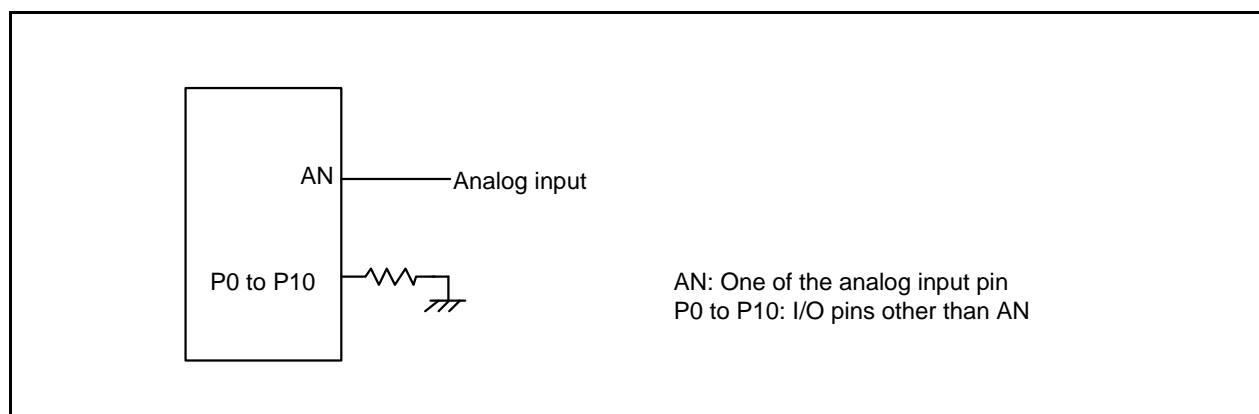
## 27.4.3 A/D Conversion Characteristics

**Table 27.48 A/D Conversion Characteristics (1)** $V_{CC} = AV_{CC} = V_{REF} = 3.0$  to  $5.5$  V,  $V_{SS} = AV_{SS} = 0$  V at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
$I_{NL}$	Integral non-linearity error	$V_{REF} = V_{CC} = 5.0$ V (2)			$\pm 3$	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			$\pm 5$	LSB
—	Absolute accuracy	$V_{REF} = V_{CC} = 5.0$ V (2)			$\pm 3$	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			$\pm 5$	LSB
$\phi_{AD}$	A/D operating clock frequency	$4.0$ V $\leq V_{CC} \leq 5.5$ V	2		25	MHz
		$3.2$ V $\leq V_{CC} \leq 4.0$ V	2		16	MHz
		$3.0$ V $\leq V_{CC} \leq 3.2$ V	2		10	MHz
—	Tolerance level impedance			3		$k\Omega$
$D_{NL}$	Differential non-linearity error	See note 2			$\pm 1$	LSB
—	Offset error (4)	See note 2			$\pm 3$	LSB
—	Gain error (4)	See note 2			$\pm 3$	LSB
$t_{CONV}$	10-bit conversion time	$V_{REF} = V_{CC} = 5$ V, $\phi_{AD} = 25$ MHz	1.60			$\mu\text{s}$
$t_{smp}$	Sampling time		0.6			$\mu\text{s}$
$V_{REF}$	Reference voltage		3.0		$V_{CC}$	V
$V_{IA}$	Analog input voltage (3)		0		$V_{REF}$	V

Notes:

1. Use when  $AV_{CC} = V_{CC}$
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to  $V_{SS}$ . See Figure 27.26 "A/D Accuracy Measure Circuit".
3. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.

**Figure 27.26 A/D Accuracy Measure Circuit**

K-Version

### 27.4.4 Flash Memory Electrical Characteristics

**Table 27.49 CPU Clock When Operating Flash Memory ( $f_{(BCLK)}$ )**

$V_{CC} = 3.0$  to  $5.5$  V at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				16 (1)	MHz
$f_{(SLOW\_R)}$	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC	35	kHz
-	Data flash read				20 (2)	MHz

Notes:

1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). No wait states are required if the 125 kHz on-chip oscillator clock or sub clock is used as the clock source of the CPU clock.

## K-Version

**Table 27.50 Flash Memory (Program ROM 1, 2) Electrical Characteristics** $V_{CC} = 3.0$  to  $5.5$  V at  $T_{opr} = 0^{\circ}\text{C}$  to  $60^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$	1,000 (2)			times
-	2 words program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		150	4000	$\mu\text{s}$
-	Lock bit program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		70	3000	$\mu\text{s}$
-	Block erase time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f_{(BCLK)}}$	ms
-	Interval from erase start/restart until following suspend request		0			$\mu\text{s}$
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f_{(BCLK)}}$	$\mu\text{s}$
-	Program, erase voltage		3.0		5.5	V
-	Read voltage	$T_{opr} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	3.0		5.5	V
-	Program, erase temperature		0		60	$^{\circ}\text{C}$
$t_{PS}$	Flash Memory Circuit Stabilization Wait Time				50	$\mu\text{s}$
-	Data hold time (6)	Ambient temperature = $55^{\circ}\text{C}$	20			year

## Notes:

- Definition of program and erase cycles:  
The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are  $n$  ( $n = 1,000$ ), each block can be erased  $n$  times. For example, if a 64 KB block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
- Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

## K-Version

**Table 27.51 Flash Memory (Data Flash) Electrical Characteristics** $V_{CC} = 3.0$  to  $5.5$  V at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program/erase cycles (1, 3, 4)	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$	10,000 (2)			times
-	2 words program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		300	4000	$\mu\text{s}$
-	Lock bit program time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		140	3000	$\mu\text{s}$
-	Block erase time	$V_{CC} = 3.3$ V, $T_{opr} = 25^{\circ}\text{C}$		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			$\mu\text{s}$
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	$\mu\text{s}$
-	Program, erase voltage		3.0		5.5	V
-	Read voltage		3.0		5.5	V
-	Program, erase temperature		-40		125	$^{\circ}\text{C}$
$t_{PS}$	Flash Memory Circuit Stabilization Wait Time				50	$\mu\text{s}$
-	Data hold time (6)	Ambient temperature = $55^{\circ}\text{C}$	20			year

## Notes:

- Definition of program and erase cycles  
The program and erase cycles refer to the number of per-block erasures.  
If the program and erase cycles are  $n$  ( $n = 10,000$ ), each block can be erased  $n$  times.  
For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
- Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
- The data hold time includes time that the power supply is off or the clock is not supplied.
- After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

K-Version

### 27.4.5 Voltage Detector and Power Supply Circuit Electrical Characteristics

**Table 27.52 Voltage Detector 0 Electrical Characteristics**

The measurement condition is  $V_{CC} = 3.0$  to  $5.5$  V,  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{det0}$	Voltage detection level $V_{det0}$	When $V_{CC}$ is falling.	2.70	2.85	3.00	V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)	$V_{CC} = 3.0$ to $5.0$ V			100	$\mu\text{s}$

Note:

1. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.

**Table 27.53 Voltage Detector 2 Electrical Characteristics**

The measurement condition is  $V_{CC} = 3.0$  to  $5.5$  V,  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$V_{det2\_0}$	Voltage detection level $V_{det2\_0}$	When $V_{CC}$ is falling		3.21		V
$V_{det2\_1}$	Voltage detection level $V_{det2\_1}$			3.36		V
$V_{det2\_2}$	Voltage detection level $V_{det2\_2}$			3.51		V
$V_{det2\_3}$	Voltage detection level $V_{det2\_3}$			3.66		V
$V_{det2\_4}$	Voltage detection level $V_{det2\_4}$		3.51	3.81	4.11	V
$V_{det2\_5}$	Voltage detection level $V_{det2\_5}$			3.96		V
$V_{det2\_6}$	Voltage detection level $V_{det2\_6}$			4.10		V
$V_{det2\_7}$	Voltage detection level $V_{det2\_7}$			4.25		V
-	Hysteresis width at the rising of $V_{CC}$ in voltage detector 2			0.15		V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)	$V_{CC} = 3.0$ to $5.0$ V			100	$\mu\text{s}$

Note:

1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.

## K-Version

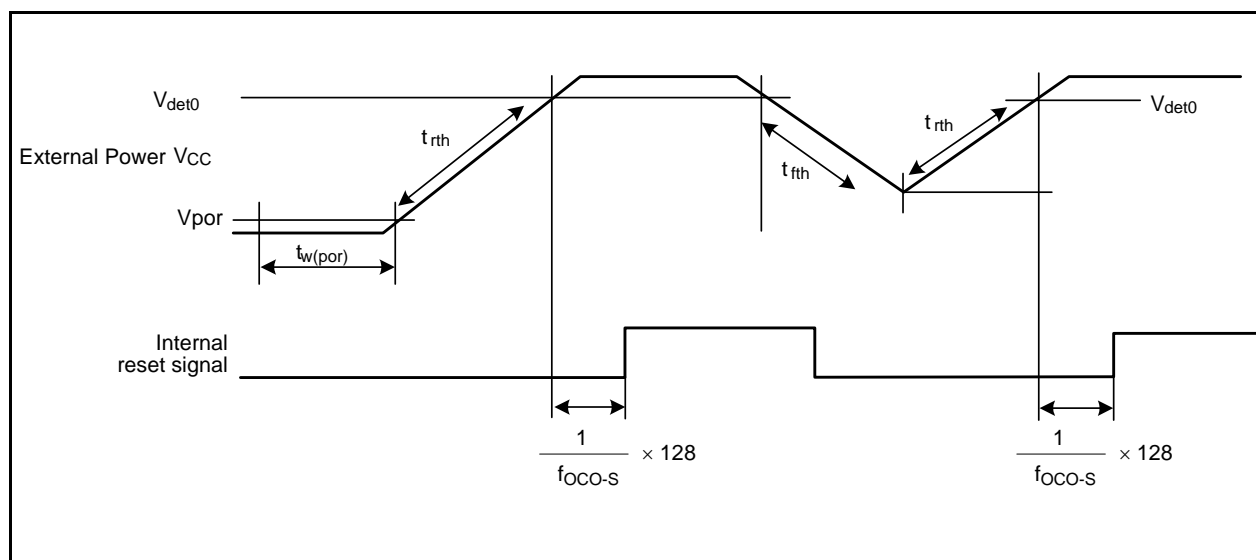
**Table 27.54 Power-On Reset Circuit**

The measurement condition is  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{rth}$	External power $V_{CC}$ rise gradient		2.0		50000	mV/ms
$t_{fth}$	External power $V_{CC}$ fall gradient				50000	mV/ms
$V_{por}$	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:

- To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

**Figure 27.27 Power-On Reset Circuit Electrical Characteristics****Table 27.55 Power Supply Circuit Timing Characteristics**

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	$V_{CC} = 3.0\text{ V to }5.5\text{ V}$			5	ms
$t_{d(R-S)}$	STOP release time				300	$\mu\text{s}$
$t_{d(W-S)}$	Low power mode wait mode release time				300	$\mu\text{s}$

Note:

- When  $V_{CC} = 5\text{ V}$ .

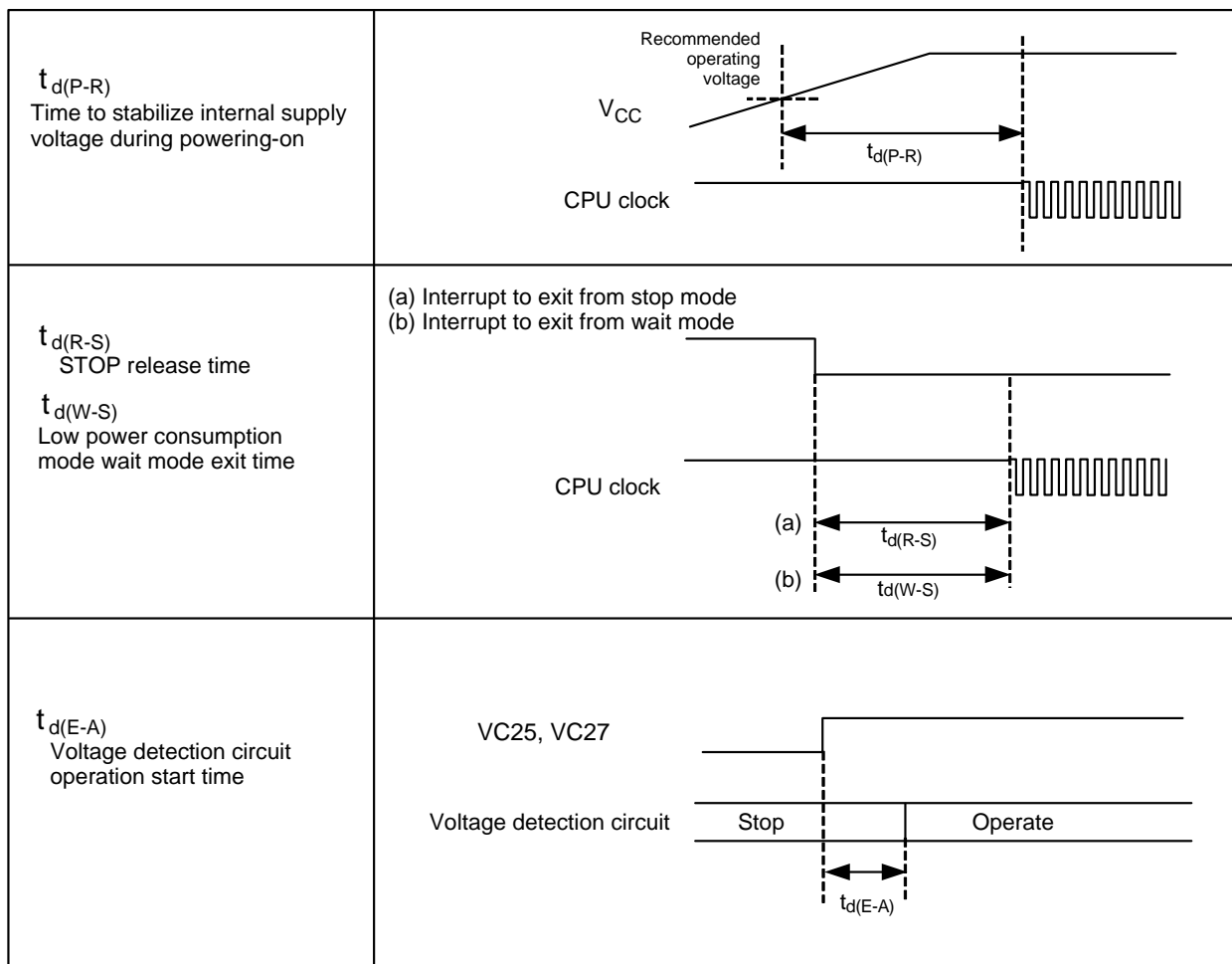


Figure 27.28 Power Supply Circuit Timing Diagram

### 27.4.6 Oscillator Electrical Characteristics

Table 27.56 On-Chip Oscillator Electrical Characteristics

$V_{CC} = 3.0$  to  $5.5$  V,  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , unless otherwise specified

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$f_{OCO-S}$	125 kHz on-chip oscillator oscillation frequency	100	125	150	kHz
$f_{OCO40M}$	40 kHz on-chip oscillator oscillation frequency	32	40	48	MHz
$f_{WDT}$	Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency	100	125	150	kHz



## 27.5 Electrical Characteristics (K-Version, $V_{CC} = 5\text{ V}$ )

### 27.5.1 Electrical Characteristics

K-Version,  $V_{CC} = 5\text{ V}$

**Table 27.57 Electrical Characteristics (1)**

$V_{CC} = 4.2\text{ to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -40^\circ\text{C to }125^\circ\text{C}$ ,  $f_{(BLK)} = 32\text{ MHz}$  unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{OH}$	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OH} = -5\text{ mA}$	$V_{CC} - 2.0$		$V_{CC}$	V
$V_{OH}$	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OH} = -200\text{ }\mu\text{A}$	$V_{CC} - 0.3$		$V_{CC}$	V
$V_{OH}$	HIGH output voltage	XOUT	HIGH POWER	$I_{OH} = -1\text{ mA}$	$V_{CC} - 2.0$	$V_{CC}$	V
			LOW POWER	$I_{OH} = -0.5\text{ mA}$	$V_{CC} - 2.0$	$V_{CC}$	V
	HIGH output voltage	XCOUT	HIGH POWER	With no load applied		2.5	V
			LOW POWER	With no load applied		1.6	V
$V_{OL}$	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OL} = 5\text{ mA}$			2.0	V
$V_{OL}$	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OL} = 200\text{ }\mu\text{A}$			0.45	V
$V_{OL}$	LOW output voltage	XOUT	HIGH POWER	$I_{OL} = 1\text{ mA}$		2.0	V
			LOW POWER	$I_{OL} = 0.5\text{ mA}$		2.0	V
	LOW output voltage	XCOUT	HIGH POWER	With no load applied		0	V
			LOW POWER	With no load applied		0	V
$V_{T+} - V_{T-}$	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS3, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, KI0 to KI3, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0		0.2		$0.4V_{CC}$	V
$V_{T+} - V_{T-}$	Hysteresis	RESET		0.2		2.5	V
$V_{T+} - V_{T-}$	Hysteresis	XIN		0.2		0.8	V
$I_{IH}$	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 5\text{ V}$			5.0	$\mu\text{A}$
$I_{IL}$	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS	$V_I = 0\text{ V}$			-5.0	$\mu\text{A}$
$R_{PULLUP}$	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$V_I = 0\text{ V}$	30	50	170	$\text{k}\Omega$
$R_{FXIN}$	Feedback resistance	XIN			1.5		$\text{M}\Omega$
$R_{FXCIN}$	Feedback resistance	XCIN			15		$\text{M}\Omega$
$V_{RAM}$	RAM retention voltage		At stop mode	2.0			V

K-Version,  $V_{CC} = 5\text{ V}$ **Table 27.58 Electrical Characteristics (2)** $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified.

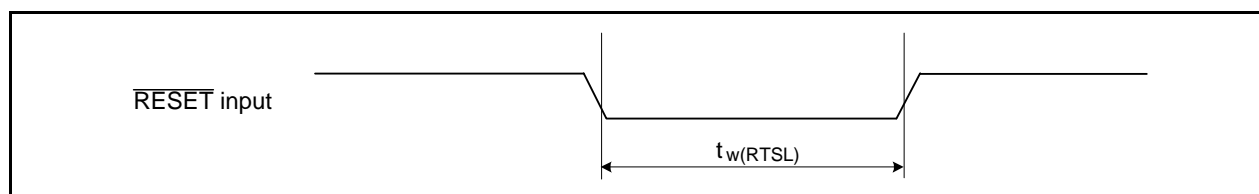
Symbol	Parameter	Measuring Condition	Standard			Unit	
			Min.	Typ.	Max.		
$I_{CC}$	Power supply current ( $V_{CC} = 4.2\text{ V}$ to $5.5\text{ V}$ ) In single-chip mode, the output pins are open and other pins are $V_{SS}$	High speed mode	$f_{(BCLK)} = 32\text{ MHz}$ , XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		28	42	mA
			$f_{(BCLK)} = 20\text{ MHz}$ , XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		20	30	mA
			$f_{(BCLK)} = 16\text{ MHz}$ , XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		16		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		20	30	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		5		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	$\mu\text{A}$
		Low power mode	$f_{(BCLK)} = 32\text{ kHz}$ On Flash memory <sup>(2)</sup> FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		$\mu\text{A}$
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$		20		$\mu\text{A}$
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 105^{\circ}\text{C}$		80		$\mu\text{A}$
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 125^{\circ}\text{C}$		120		$\mu\text{A}$
		Stop mode	$T_{opr} = 25^{\circ}\text{C}$		3	15	$\mu\text{A}$
			$T_{opr} = 105^{\circ}\text{C}$		60		$\mu\text{A}$
			$T_{opr} = 125^{\circ}\text{C}$		100		$\mu\text{A}$
During flash memory program	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 5.0\text{ V}$		20.0		mA		
During flash memory erase	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 5.0\text{ V}$		30.0		mA		
$I_{det2}$	Low voltage detection dissipation current		3		$\mu\text{A}$		
$I_{det0}$	Reset area detection dissipation current		6		$\mu\text{A}$		

Note:

1. This indicates the memory in which the program to be executed exists.

K-Version,  $V_{CC} = 5\text{ V}$ **27.5.2 Timing Requirements (Peripheral Functions and Others)** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **27.5.2.1 Reset Input ( $\overline{\text{RESET}}$  Input)****Table 27.59 Reset Input ( $\overline{\text{RESET}}$  Input)**

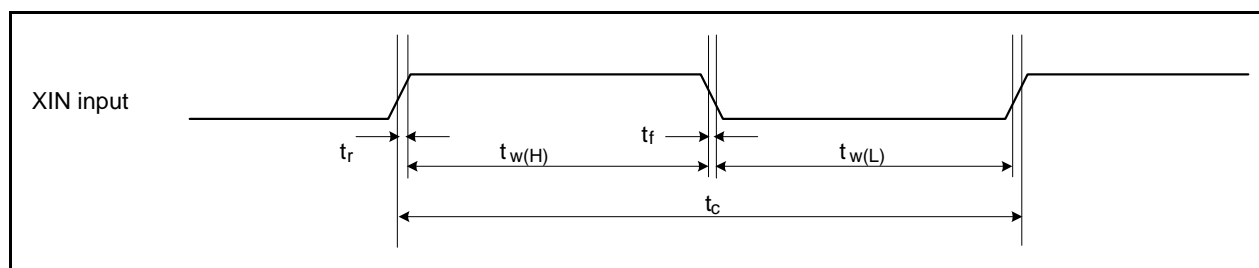
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(\text{RSTL})}$	$\overline{\text{RESET}}$ input low pulse width	10		$\mu\text{s}$

**Figure 27.29 Reset Input ( $\overline{\text{RESET}}$  Input)****27.5.2.2 External Clock Input****Table 27.60 External Clock Input (XIN input) (1)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	50		ns
$t_{w(\text{H})}$	External clock input high pulse width	20		ns
$t_{w(\text{L})}$	External clock input low pulse width	20		ns
$t_r$	External clock rise time		9	ns
$t_f$	External clock fall time		9	ns

Note:

1. The condition is  $V_{CC} = 5.0\text{V}$ .

**Figure 27.30 External Clock Input (XIN Input)**

K-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **27.5.2.3 Timer A Input****Table 27.61 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

**Table 27.62 Timer A Input (Gating Input in Timer Mode)**

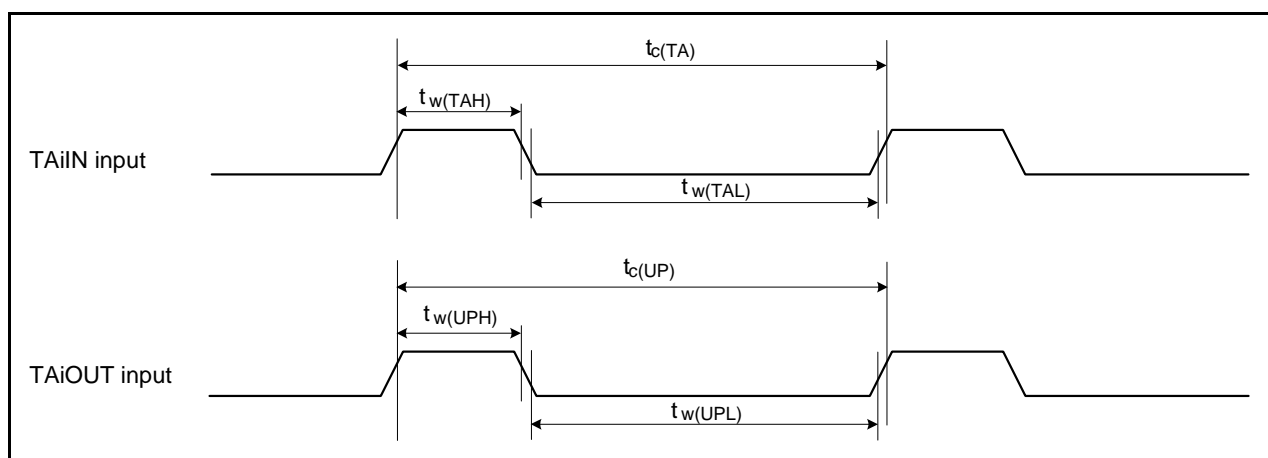
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

**Table 27.63 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

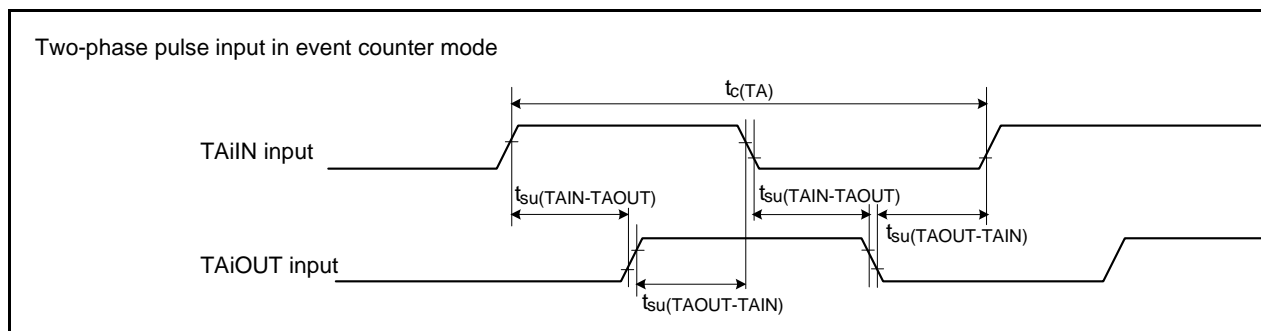
**Table 27.64 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

**Figure 27.31 Timer A Input**

K-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **Table 27.65 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

**Figure 27.32 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

K-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **27.5.2.4 Timer B Input****Table 27.66 Timer B Input (Counter Input in Event Counter Mode)**

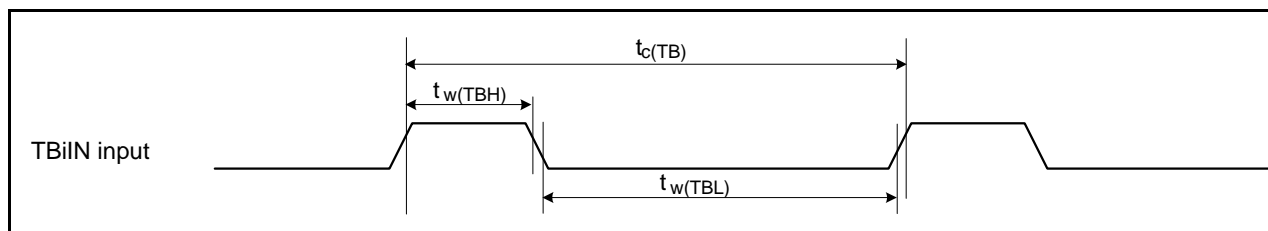
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	80		ns

**Table 27.67 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

**Table 27.68 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

**Figure 27.33 Timer B Input**

K-Version,  $V_{CC} = 5\text{ V}$

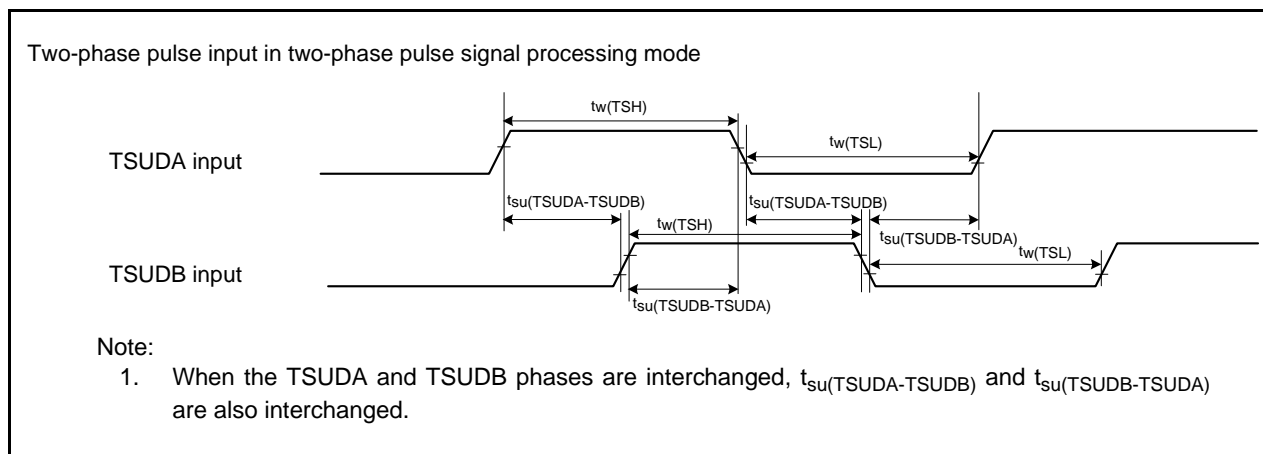
**Timing Requirements**

( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified)

**27.5.2.5 Timer S Input**

**Table 27.69 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

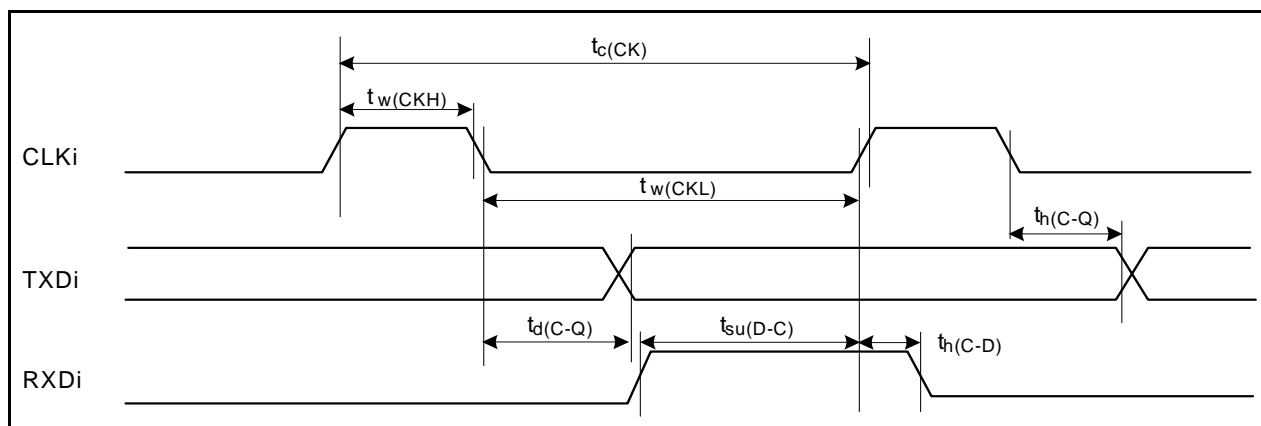
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_w(\text{TSH})$	TSUDA, TSUDB input high pulse width	2		$\mu\text{S}$
$t_w(\text{TSL})$	TSUDA, TSUDB input low pulse width	2		$\mu\text{S}$
$t_{su}(\text{TSUDA-TSUDB})$	TSUDB input setup time	1		$\mu\text{S}$
$t_{su}(\text{TSUDB-TSUDA})$	TSUDA input setup time	1		$\mu\text{S}$



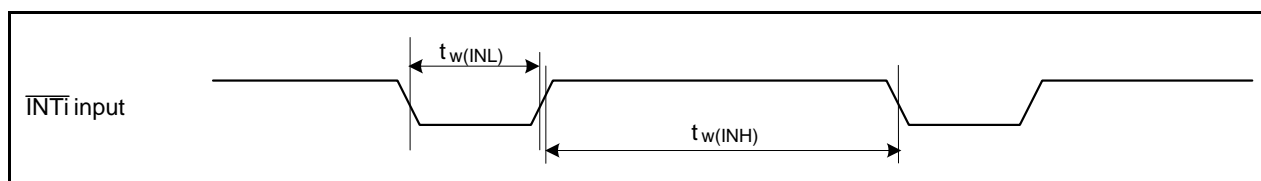
**Figure 27.34 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

K-Version,  $V_{CC} = 5\text{ V}$ **Timing Requirements** $(V_{CC} = 5\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **27.5.2.6 Serial Interface****Table 27.70 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

**Figure 27.35 Serial Interface****27.5.2.7 External Interrupt  $\overline{INTi}$  Input****Table 27.71 External Interrupt  $\overline{INTi}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

**Figure 27.36 External Interrupt  $\overline{INTi}$  Input**



K-Version,  $V_{CC} = 5\text{ V}$

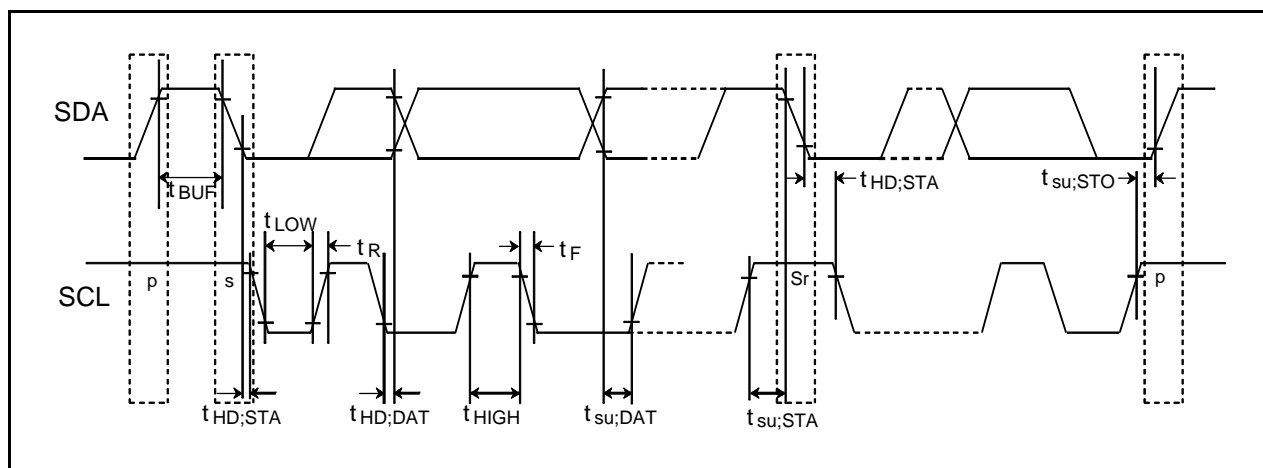
**Timing Requirements**

( $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified)

**27.5.2.8 Multi-master I<sup>2</sup>C-bus**

**Table 27.72 Multi-master I<sup>2</sup>C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
$t_{BUF}$	Bus free time	4.7		1.3		$\mu\text{s}$
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		$\mu\text{s}$
$t_{LOW}$	Hold time in SCL clock 0 status	4.7		1.3		$\mu\text{s}$
$t_R$	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	$\mu\text{s}$
$t_{HIGH}$	Hold time in SCL clock 1 status	4.0		0.6		$\mu\text{s}$
$t_F$	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		$\mu\text{s}$
$t_{su;STO}$	Stop condition setup time	4.0		0.6		$\mu\text{s}$



**Figure 27.37 Multi-master I<sup>2</sup>C-bus**

## 27.6 Electrical Characteristics (K-Version, $V_{CC} = 3\text{ V}$ )

### 27.6.1 Electrical Characteristics

K-Version,  $V_{CC} = 3\text{ V}$

**Table 27.73 Electrical Characteristics (1)**

$V_{CC} = 3.0$  to  $3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $f_{(BCLK)} = 32\text{ MHz}$  unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{OH}$	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OH} = -1\text{ mA}$	$V_{CC}-0.5$		$V_{CC}$	V
$V_{OH}$	HIGH output voltage	XOUT	HIGH POWER	$I_{OH} = -0.1\text{ mA}$	$V_{CC}-0.5$	$V_{CC}$	V
			LOW POWER	$I_{OH} = -50\text{ }\mu\text{A}$	$V_{CC}-0.5$	$V_{CC}$	V
	HIGH output voltage	XCOUT	HIGH POWER	With no load applied		2.5	V
			LOW POWER	With no load applied		1.6	V
$V_{OL}$	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$I_{OL} = 1\text{ mA}$			0.5	V
$V_{OL}$	LOW output voltage	XOUT	HIGH POWER	$I_{OL} = 0.1\text{ mA}$		0.5	V
			LOW POWER	$I_{OL} = 50\text{ }\mu\text{A}$		0.5	V
	LOW output voltage	XCOUT	HIGH POWER	With no load applied		0	V
			LOW POWER	With no load applied		0	V
$V_{T+}, V_{T-}$	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INTO to INT5, NMI, ADTRG, CTS0 to CTS3, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$ , RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0				$0.4V_{CC}$	V
$V_{T+}, V_{T-}$	Hysteresis	$\overline{RESET}$				1.8	V
$V_{T+}, V_{T-}$	Hysteresis	XIN				0.8	V
$I_{IH}$	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$ , CNVSS	$V_I = 3\text{ V}$			4.0	$\mu\text{A}$
$I_{IL}$	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$ , CNVSS	$V_I = 0\text{ V}$			-4.0	$\mu\text{A}$
$R_{PULLUP}$	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	$V_I = 0\text{ V}$	50	100	500	k $\Omega$
$R_{FXIN}$	Feedback resistance	XIN			3.0		M $\Omega$
$R_{FXCIN}$	Feedback resistance	XCIN			25		M $\Omega$
$V_{RAM}$	RAM retention voltage		At stop mode	2.0			V

K-Version,  $V_{CC} = 3\text{ V}$

**Table 27.74 Electrical Characteristics (2)**

$T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit	
			Min.	Typ.	Max.		
$I_{CC}$	Power supply current ( $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ) In single-chip mode, the output pins are open and other pins are $V_{SS}$	High speed mode	$f_{(BCLK)} = 32\text{ MHz}$ , XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operating		26	40	mA
			$f_{(BCLK)} = 20\text{ MHz}$ , XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operating		19	28	mA
			$f_{(BCLK)} = 16\text{ MHz}$ , XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operating		15		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating No division		19	28	mA
			Main clock stopped 40 MHz on-chip oscillator operating 125 kHz on-chip oscillator operating Divide-by-8		5		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	$\mu\text{A}$
		Low power mode	$f_{(BCLK)} = 32\text{ kHz}$ On ROM FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		$\mu\text{A}$
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 25^{\circ}\text{C}$		20		$\mu\text{A}$
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 105^{\circ}\text{C}$		80		$\mu\text{A}$
			Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator operating Peripheral clock operating $T_{opr} = 125^{\circ}\text{C}$		120		$\mu\text{A}$
		Stop mode	$T_{opr} = 25^{\circ}\text{C}$		2	12	$\mu\text{A}$
			$T_{opr} = 105^{\circ}\text{C}$		60		$\mu\text{A}$
			$T_{opr} = 125^{\circ}\text{C}$		100		$\mu\text{A}$
		During flash memory program	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 3.0\text{ V}$		20.0		mA
During flash memory erase	$f_{(BCLK)} = 10\text{ MHz}$ , PM17 = 1 (one wait) $V_{CC} = 3.0\text{ V}$		30.0		mA		
$I_{det2}$	Low voltage detection dissipation current		3		$\mu\text{A}$		
$I_{det0}$	Reset area detection dissipation current		6		$\mu\text{A}$		

K-Version,  $V_{CC} = 3\text{ V}$

### 27.6.2 Timing Requirements (Peripheral Functions and Others)

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified)

#### 27.6.2.1 Reset Input ( $\overline{\text{RESET}}$ Input)

Table 27.75 Reset Input ( $\overline{\text{RESET}}$  Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(\text{RSTL})}$	RESET input low pulse width	10		$\mu\text{s}$

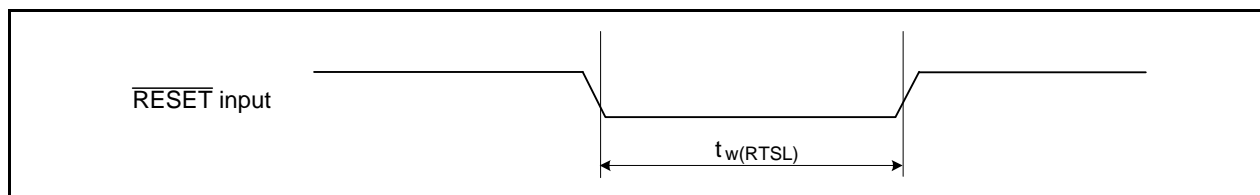


Figure 27.38 Reset Input ( $\overline{\text{RESET}}$  Input)

#### 27.6.2.2 External Clock Input

Table 27.76 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c$	External clock input cycle time	50		ns
$t_{w(\text{H})}$	External clock input high pulse width	20		ns
$t_{w(\text{L})}$	External clock input low pulse width	20		ns
$t_r$	External clock rise time		9	ns
$t_f$	External clock fall time		9	ns

Note:

1. The condition is  $V_{CC} = 3.0\text{V}$ .

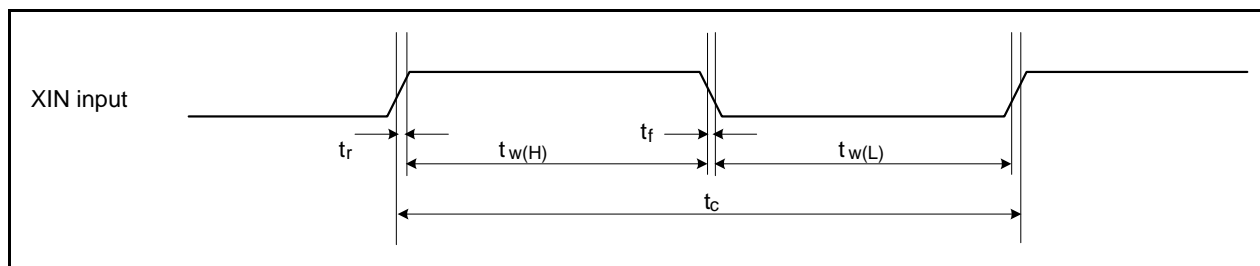


Figure 27.39 External Clock Input (XIN Input)

K-Version,  $V_{CC} = 3\text{ V}$ **Timing Requirements** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **27.6.2.3 Timer A Input****Table 27.77 Timer A Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

**Table 27.78 Timer A Input (Gating Input in Timer Mode)**

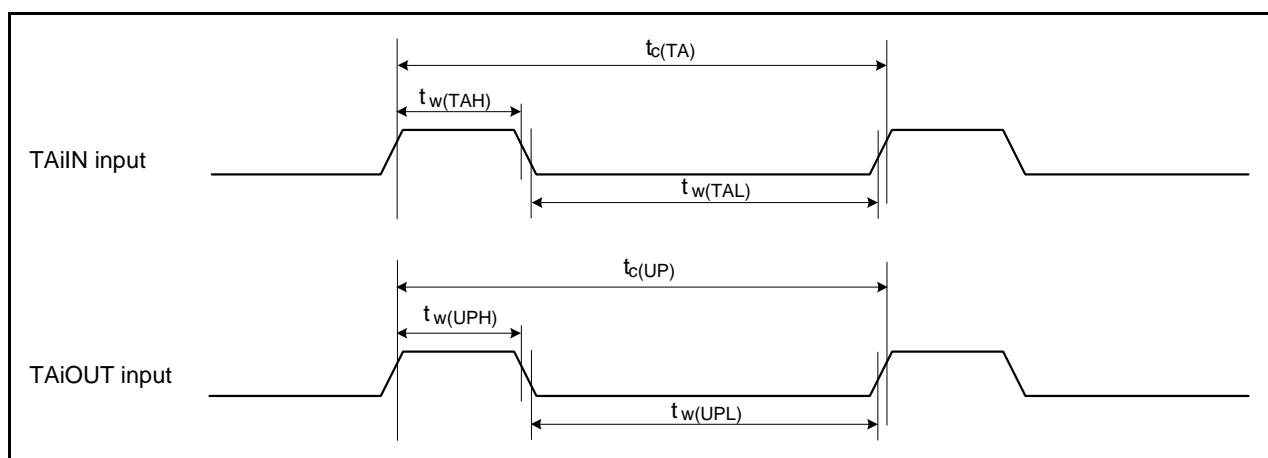
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

**Table 27.79 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

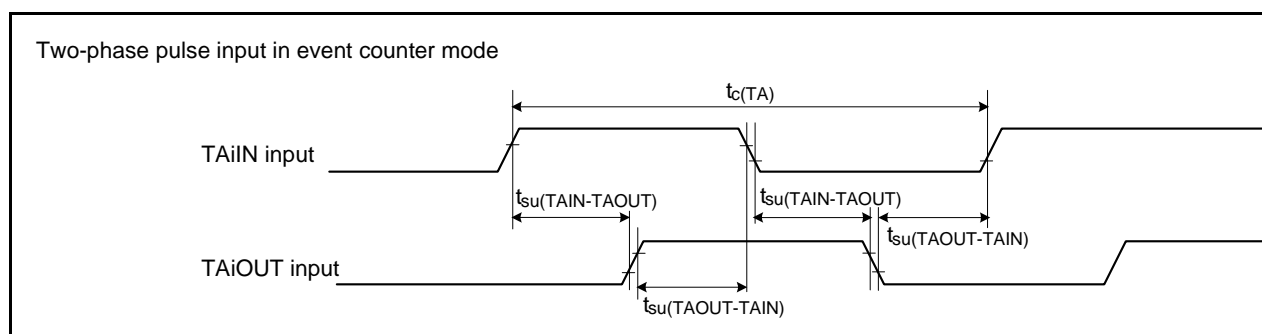
**Table 27.80 Timer A Input (External Trigger Input in PWM Mode, Programmable Output Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

**Figure 27.40 Timer A Input**

K-Version,  $V_{CC} = 3\text{ V}$ **Timing Requirements** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **Table 27.81 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		$\mu\text{S}$
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

**Figure 27.41 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)**

K-Version,  $V_{CC} = 3\text{ V}$

**Timing Requirements**

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified)

**27.6.2.4 Timer B Input**

**Table 27.82 Timer B Input (Counter Input in Event Counter Mode)**

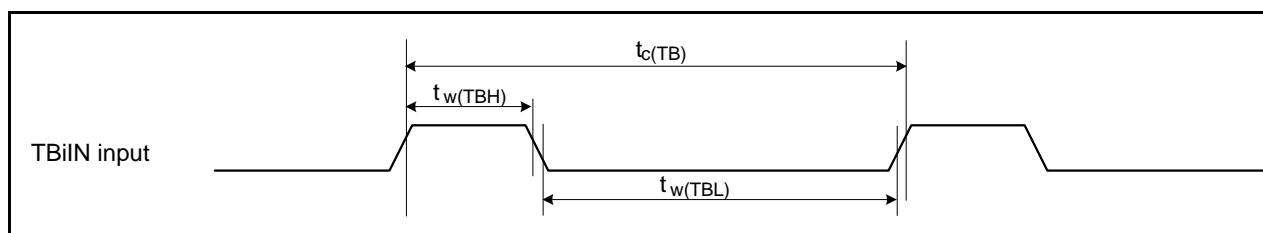
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	120		ns

**Table 27.83 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

**Table 27.84 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns



**Figure 27.42 Timer B Input**

K-Version,  $V_{CC} = 3\text{ V}$

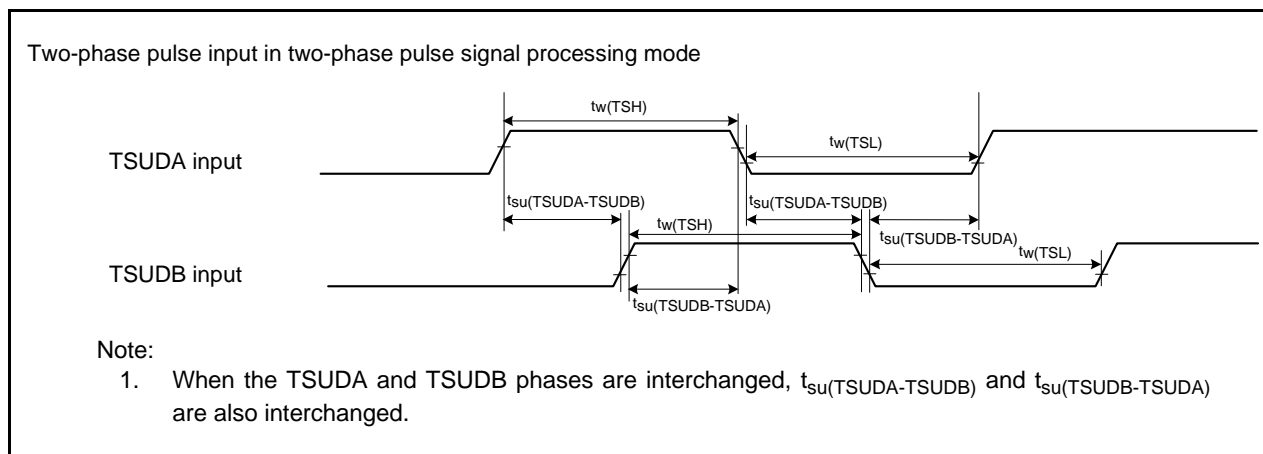
**Timing Requirements**

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified)

**27.6.2.5 Timer S Input**

**Table 27.85 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_w(\text{TSH})$	TSUDA, TSUDB input high pulse width	2		$\mu\text{S}$
$t_w(\text{TSL})$	TSUDA, TSUDB input low pulse width	2		$\mu\text{S}$
$t_{su}(\text{TSUDA-TSUDB})$	TSUDB input setup time	1		$\mu\text{S}$
$t_{su}(\text{TSUDB-TSUDA})$	TSUDA input setup time	1		$\mu\text{S}$

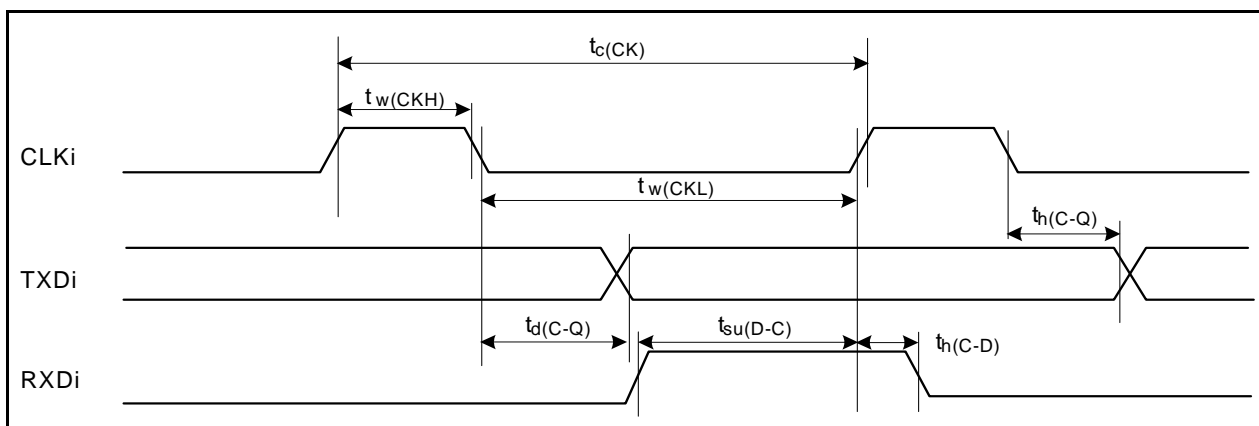


**Figure 27.43 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)**

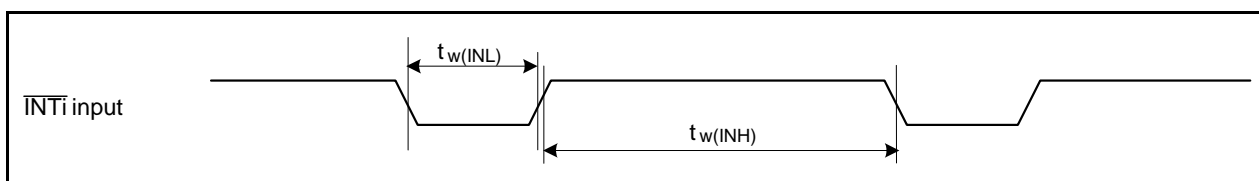


K-Version,  $V_{CC} = 3\text{ V}$ **Timing Requirements** $(V_{CC} = 3\text{ V}, V_{SS} = 0\text{ V}, \text{ at } T_{opr} = -40^{\circ}\text{C to } 125^{\circ}\text{C unless otherwise specified})$ **27.6.2.6 Serial Interface****Table 27.86 Serial Interface**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

**Figure 27.44 Serial Interface****27.6.2.7 External Interrupt  $\overline{INTi}$  Input****Table 27.87 External Interrupt  $\overline{INTi}$  Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

**Figure 27.45 External Interrupt  $\overline{INTi}$  Input**

K-Version,  $V_{CC} = 3\text{ V}$

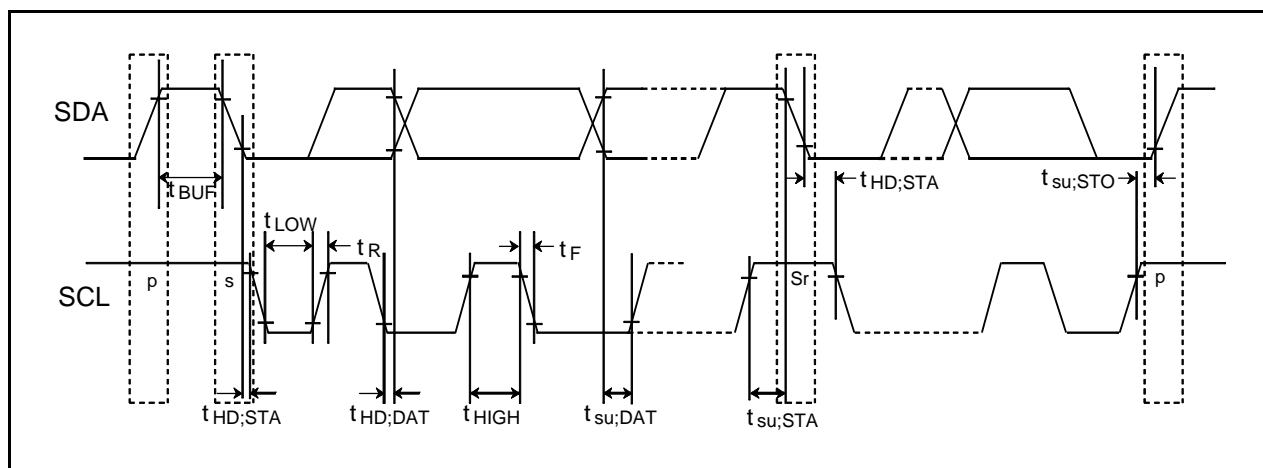
**Timing Requirements**

( $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , at  $T_{opr} = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise specified)

**27.6.2.8 Multi-master I<sup>2</sup>C-bus**

**Table 27.88 Multi-master I<sup>2</sup>C-bus**

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
$t_{BUF}$	Bus free time	4.7		1.3		$\mu\text{s}$
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		$\mu\text{s}$
$t_{LOW}$	Hold time in SCL clock 0 status	4.7		1.3		$\mu\text{s}$
$t_R$	SCL, SDA signals' rising time		1000	$20 + 0.1 C_b$	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	$\mu\text{s}$
$t_{HIGH}$	Hold time in SCL clock 1 status	4.0		0.6		$\mu\text{s}$
$t_F$	SCL, SDA signals' falling time		300	$20 + 0.1 C_b$	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		$\mu\text{s}$
$t_{su;STO}$	Stop condition setup time	4.0		0.6		$\mu\text{s}$



**Figure 27.46 Multi-master I<sup>2</sup>C-bus**

## 28. Usage Notes

### 28.1 Notes on Noise

Connect a bypass capacitor (approximately 0.1  $\mu\text{F}$ ) across pins VCC and VSS using the shortest and thickest possible wiring. Figure 28.1 shows the Bypass Capacitor Connection.

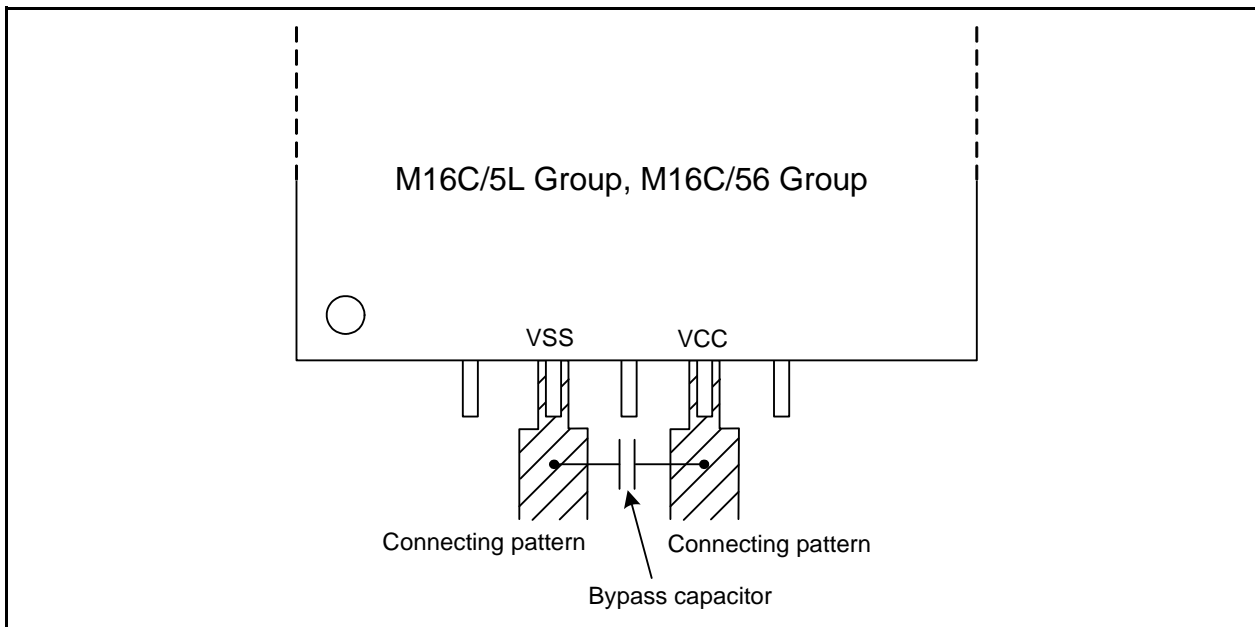


Figure 28.1 Bypass Capacitor Connection

## 28.2 Notes on SFRs

### 28.2.1 Register Settings

Table 28.1 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM. Read-modify-write instructions can be used when writing to the no register bits.

**Table 28.1 Registers with Write-Only Bits**

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0299h	UART4 Bit Rate Register	U4BRG
029Bh to 029Ah	UART4 Transmit Buffer Register	U4TB
02A9h	UART3 Bit Rate Register	U3BRG
02ABh to 02AAh	UART3 Transmit Buffer Register	U3TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR

**Table 28.2 Read-Modify-Write Instructions**

Function	Mnemonic
Transfer	<i>MOVDir</i>
Bit processing	BCLR, <i>BMCnd</i> , BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

### 28.3 Notes on Protection

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0 (write disabled). Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure there are no interrupts or DMA transfers between the instruction that sets the PRC2 bit to 1 and the next instruction.

## 28.4 Notes on Resets

### 28.4.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC) (Voltage range: 0 to 2)	0.05			V/ms

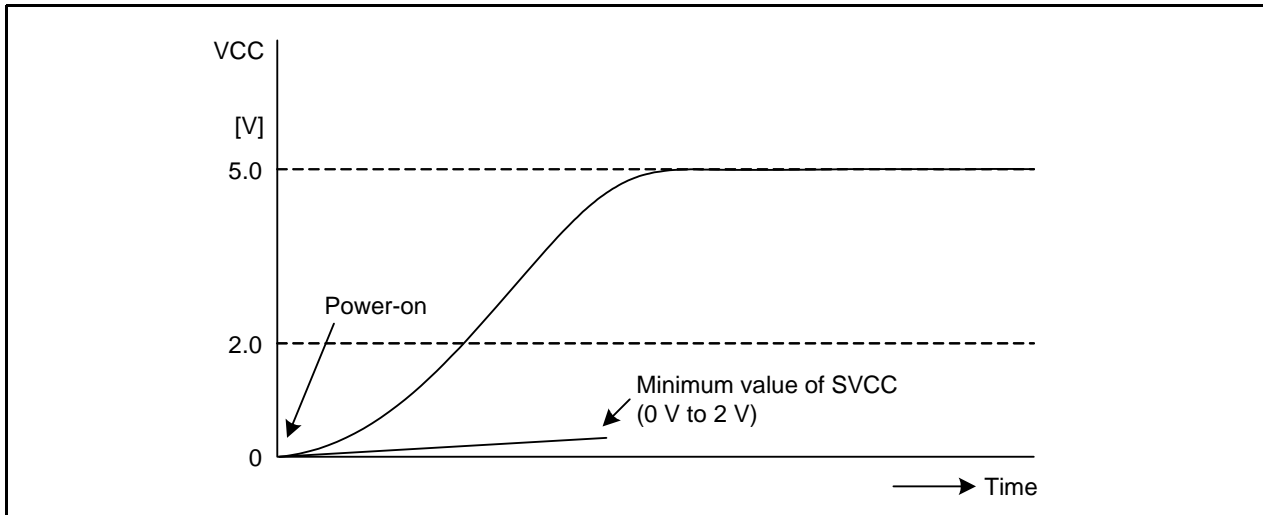


Figure 28.2 SVCC Timing

### 28.4.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use the power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable these bits by a program.

### 28.4.3 OSDR Bit (Oscillation Stop Detect Reset Detect Flag)

When an oscillator stop detect reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit in the RSTFR register is not affected by a hardware reset, but becomes 0 (not detected) from a voltage monitor 0 reset.

### 28.4.4 Hardware Reset When $VCC < V_{det0}$

If a hardware reset is executed when the LVDAS bit in the OFS1 address is 0 (voltage monitor 0 reset enabled after hardware reset) and  $VCC < V_{det0}$ , the MCU executes the program at the address indicated by the reset vector when changing the signal applied to the  $\overline{RESET}$  pin from low to high. A voltage monitor 0 reset is not generated.

## 28.5 Notes on Clock Generator

### 28.5.1 Oscillator Using a Crystal or a Ceramic Resonator

To connect a crystal/ceramic resonator follow the instructions below:

- The oscillation characteristics are tied closely to the user's board design. Perform a careful evaluation of the board before connecting an oscillator.
- Oscillator structure depends on a crystal/ceramic resonator. The M16C/5L Group, M16C/56 Group MCUs contain a feedback resistor, but an additional external feedback resistor may be required. Contact the manufacturer of crystal/ceramic resonator regarding circuit constants, as they are dependent on the a crystal/ceramic resonator or stray capacitance of the mounted circuit.
- Check output from the CLKOUT pin to confirm that the clock generated by the oscillator is properly transmitted to the MCU.

The procedure for outputting a clock from the CLKOUT pin is listed below. Set the clock output from the CLKOUT pin to 25 MHz or lower.

Outputting the main clock

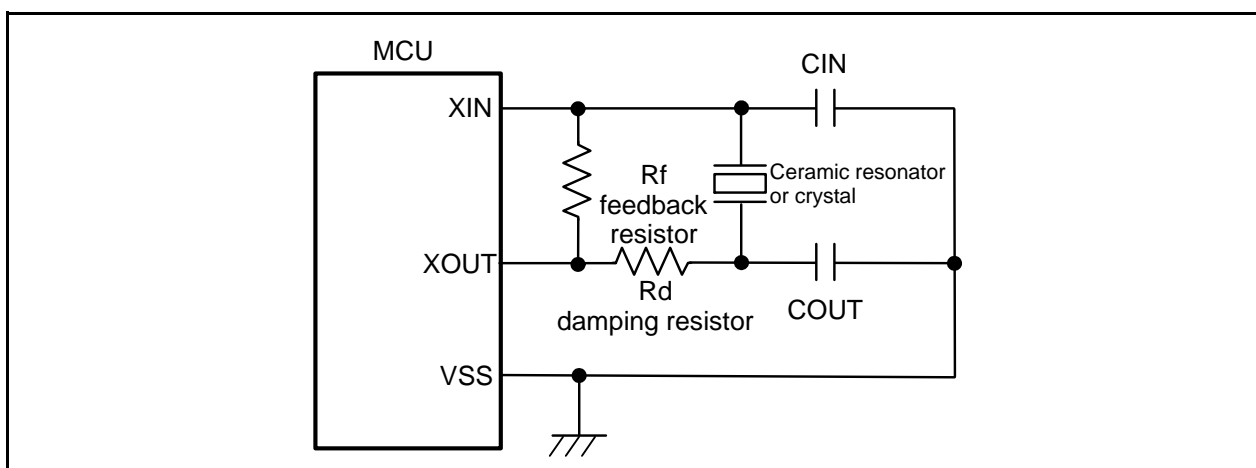
- (1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
- (2) Set the CM11 bit in the CM1 register, the CM07 bit in the CM0 register, and the CM21 bit in the CM2 register all to 0 (main clock selected).
- (3) Select the clock output from the CLKOUT pin (see the table below).
- (4) Set the PRC0 bit in the PRCR register to 0 (write disabled).

**Table 28.3 Output from CLKOUT Pin When Selecting Main Clock**

Bit Setting		Output from the CLKOUT Pin
PCLKR register	CM0 register	
PCLK5 bit	Bits CM01 to CM00	
1	00b	Clock with the same frequency as the main clock
0	10b	Main clock divided by 8
0	11b	Main clock divided by 32

Outputting the sub clock

- (1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
- (2) Set the CM07 bit in the CM0 register to 1 (sub clock selected).
- (3) Set the PCLK5 bit in the PCLKR register to 0, and bits CM01 to CM00 in the CM0 register to 01b (fC output from CLKOUT pin).
- (4) Set the PRC0 bit in the PRCR register to 0 (write disabled).



**Figure 28.3 Oscillator Example**



## 28.5.2 Noise Countermeasure

### 28.5.2.1 Clock I/O Pin Wiring

- Connect the shortest possible wiring to the clock I/O pin.
- Connect (a) the capacitor's ground lead connected to the crystal/ceramic resonator, and (b) the MCU's VSS pin, with the shortest possible wiring (maximum 20 mm).

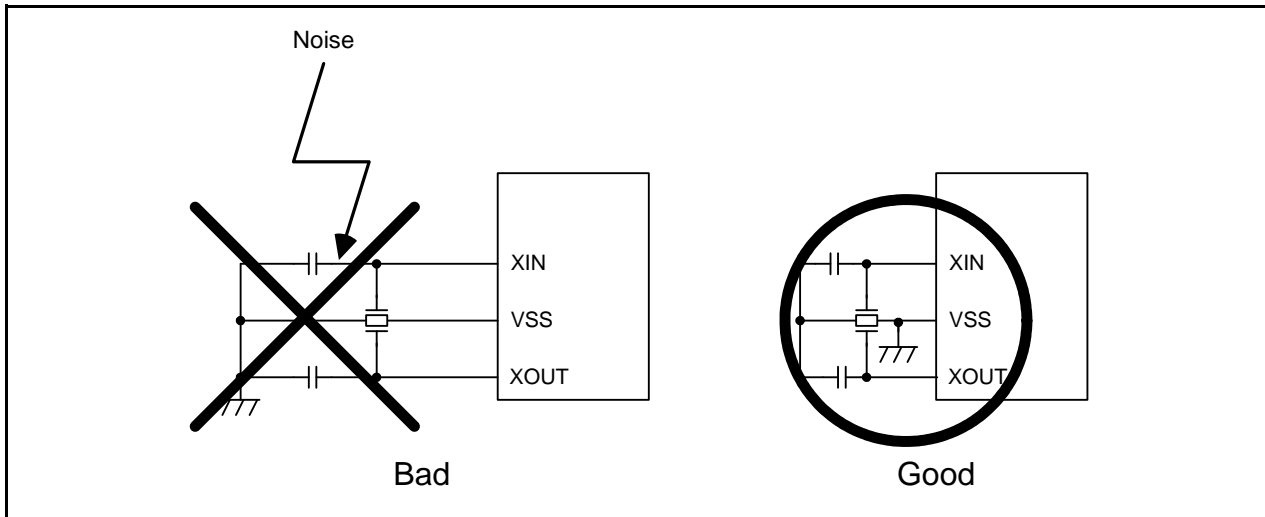


Figure 28.4 Clock I/O Pin Wiring

Reason:

When noise enters the clock I/O pin, the clock waveform becomes unstable, which causes an error in operation or a program runaway. Also, if a potential difference attributed to the noise occurs between the VSS level of the MCU and the VSS level of the crystal/ceramic resonator, an accurate clock is not input to the MCU.

### 28.5.2.2 Large Current Signal Line

For large currents that exceed the MCU's current range, wire the signal lines as far away from the MCU as possible (especially the crystal/ceramic resonator).

Reason:

In the system using the MCU, there are signal lines for controlling motors, LEDs, and thermal heads. When a large current flows through these signal lines, noise is generated due to mutual inductance.

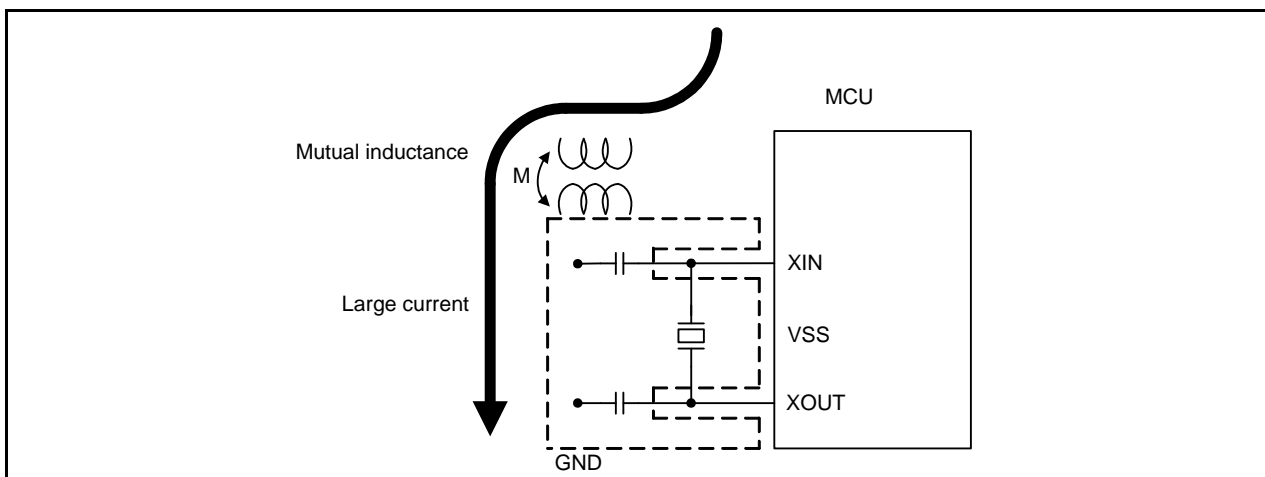


Figure 28.5 Large Current Signal Line Wiring

### 28.5.2.3 Signal Line Whose Level Changes at a High-Speed

For a signal line whose level changes at a high-speed, wire it as far away from the crystal/ceramic resonator and its wiring pattern as possible. Do not wire it across or extend it parallel to a clock-related signal line or other signal lines which are sensitive to noise.

Reason:

A signal whose level changes at a high-speed (such as the signal from the TAIOUT pin) affects other signal lines due to the level change at rising or falling edges. Specifically, when the signal line crosses the clock-related signal line, the clock waveform becomes unstable, which causes an error in operation or a program runaway.

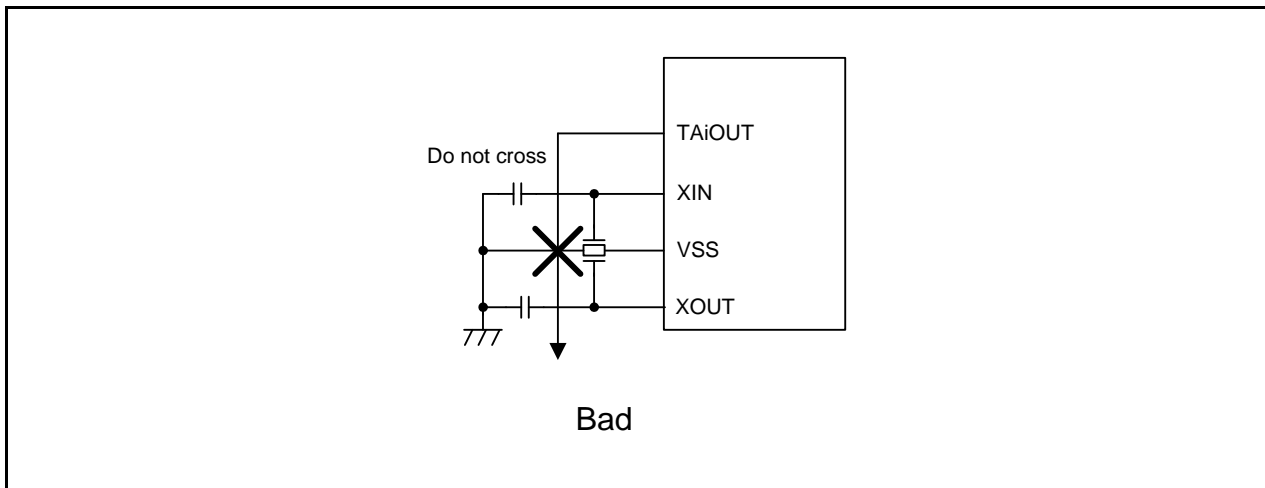


Figure 28.6 Wiring of Signal Line Whose Level Changes at High-Speed

### 28.5.3 CPU Clock

(Technical update number: TN-M16C-109-0309)

When an external clock is input from the XIN pin and the main clock is used as the CPU clock, do not stop the external clock.

### 28.5.4 Oscillator Stop/Restart Detect Function

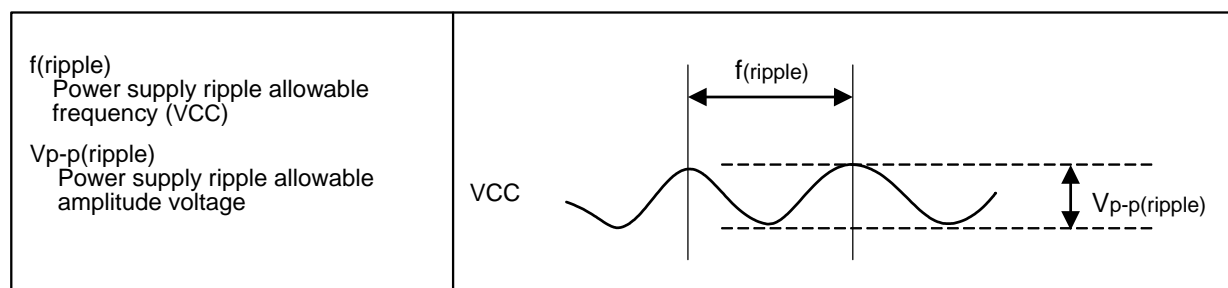
- In the following cases, set the CM20 bit to 0 (oscillator stop/restart detect function disabled), and then change the setting of each bit.
  - When the CM05 bit is set to 1 (main clock stopped)
  - When the CM10 bit is set to 1 (stop mode)
- To enter wait mode while using the oscillator stop/restart detect function, set the CM02 bit to 0 (peripheral function clock f1 not turned off during wait mode).
- This function cannot be used if the main clock frequency is 2 MHz or lower. In that case, set the CM20 bit to 0 (oscillator stop/restart detect function disabled).
- While the CM27 bit is 1 (oscillation stop/restart detect interrupt), when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). (Do not set the FRA00 bit to 0 while FRA01 bit is 1, and vice versa.)

### 28.5.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage within the acceptable range of power supply ripple.

**Table 28.4** Acceptable Range of Power Supply Ripple

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
f(ripple)	Power supply ripple allowable frequency (VCC)			10	kHz
VP-P(ripple)	Power supply ripple allowable amplitude voltage	(VCC = 5 V)		0.5	V
		(VCC = 3 V)		0.3	V
VCC( ΔV / ΔT )	Power supply ripple rising/falling gradient	(VCC = 5 V)		0.3	V/ms
		(VCC = 3 V)		0.3	V/ms



**Figure 28.7** Voltage Fluctuation Timing

## 28.6 Notes on Power Control

### 28.6.1 CPU Clock

When switching the CPU clock source, wait until oscillation of the switched clock source is stable. After exiting stop mode, wait until oscillation stabilizes before changing the division.

### 28.6.2 Wait Mode

- Insert four or more NOP instructions following the WAIT instruction. When entering wait mode, because the instruction queue prefetches instructions that follow the WAIT instruction, prefetched instructions are sometimes executed prior to the interrupt routine used to exit wait mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the WAIT instruction, interrupt requests are not accepted before the WAIT instruction is executed.

The following is an example program for entering wait mode:

```

Program Example: FSET    I        ;
                  WAIT      ; Enter wait mode
                  NOP        ; Insert at least four NOP instructions
                  NOP
                  NOP
                  NOP

```

- Do not enter wait mode from PLL operating mode. To enter wait mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter wait mode from low current consumption read mode. To enter wait mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter wait mode from CPU rewrite mode. To enter wait mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Set the PLC07 bit in the PLC0 register to 0 (PLL off). When the PLC07 bit is 1 (PLL on), current consumption cannot be reduced even in wait mode.

### 28.6.3 Stop Mode

- When exiting stop mode by a hardware reset, drive the  $\overline{\text{RESET}}$  pin low for 20 fOCO-S cycles or more.
- Set the MR0 bit in the TAiMR register ( $i = 0$  to 4) to 0 (pulse not output) when using timer A to exit stop mode.
- When entering stop mode, insert a JMP.B instruction immediately after executing an instruction that sets the CM10 bit in the CM1 register to 1 (stop mode), and then insert at least four NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to 1. Thus, some of the instructions may be executed before the MCU enters stop mode or before the interrupt routine for returning from stop mode. As shown below, when the instruction to set the I flag to 1 is allocated just before the instruction to set the CM10 bit to 1, interrupt requests are not accepted before entering stop mode.

The following is an example program for entering stop mode:

```

Program Example:  FSET   I
                  BSET   0, CM1 ; Enter stop mode
                  JMP.B  L2      ; Insert a JMP.B instruction
L2:
                  NOP                ; At least four NOP instructions
                  NOP
                  NOP
                  NOP

```

- The CLKOUT pin outputs a high-level signal in stop mode. Thus, if stop mode is entered right after output on the CLKOUT pin changes state from high to low, the low-level duration of the output signal to the CLKOUT pin becomes shorter.



- Do not enter stop mode from PLL operating mode. To enter stop mode from PLL operating mode, first enter medium-speed mode, then set the PLC07 bit to 0 (PLL off).
- Do not enter stop mode from low current consumption read mode. To enter stop mode from low current consumption read mode, set the FMR23 bit in the FMR2 register to 0 (low current consumption read mode disabled).
- Do not enter stop mode from CPU rewrite mode. To enter stop mode from CPU rewrite mode, first set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled), then disable the DMA transfer.
- Do not enter stop mode when the oscillator stop/restart detect function is enabled. To enter stop mode, set the CM20 bit in the CM2 register to 0 (oscillator stop/restart detect function disabled).
- Do not enter stop mode when the FMR01 bit is 1 (CPU rewrite mode enabled), and do not enter stop mode when the flash memory is stopped (bits FMR01 and FMSTP are 1).

#### 28.6.4 Low Current Consumption Read Mode

- Enter low current consumption read mode through slow read mode (see Figure 9.4 “Setting and Canceling Low Current Consumption Read Mode” for details).
- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.
- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR23 bit in the FMR2 register to 1 (low current consumption read mode enable).

#### 28.6.5 Slow Read Mode

- When the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled), do not set the FMR22 bit in the FMR2 register to 1 (slow read mode enabled).

## 28.7 Notes on Programmable I/O Ports

### Note

The 64-pin package has no P0\_4 to P0\_7, P1\_0 to P1\_4, P3\_4 to P3\_7, P9\_5 to P9\_7.

### 28.7.1 Pin Assignment Control

Bits PACR2 to PACR0 in the PACR register are 000b after reset. Set 010b (64-pin package) or 011b (80-pin package) to select the pin package, depending on the product.

After setting bits PACR2 to PACR0, set the programmable I/O ports and I/O pins for peripherals.

### 28.7.2 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance:

P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/ $\overline{CTS2}$ / $\overline{RTS2}$ /TA1IN/ $\overline{V}$ /TXD1, P7\_4/TA2OUT/W,  
P7\_5/TA2IN/ $\overline{W}$ , P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/ $\overline{U}$ /TSUDB

### 28.7.3 Input Voltage Threshold

The input threshold voltage differs in the programmable I/O port and peripherals. When the programmable I/O port and peripheral is sharing the same pin, and the pin input level is lower than  $V_{IH}$  and higher than  $V_{IL}$  (input voltage is neither high or low), the input signal voltage level may be determined differently between the programmable I/O port and peripheral because the input voltage thresholds for those two are not necessarily the same.

## 28.8 Notes on Interrupts

### 28.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from address 00000h during the interrupt sequence. At this time, the IR bit of the accepted interrupt is cleared to 0 (interrupt not requested).

If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts becomes 0. This may cause problems such as interrupts being canceled or an unexpected interrupt request being generated.

### 28.8.2 SP Setting

Set a value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is set to 0000h after reset. Therefore, if an interrupt is accepted before setting a value in the SP (USP, ISP), the program may go out of control.

Set a value in the ISP at the beginning of the program. For the first instruction after reset only, all interrupts are disabled.

### 28.8.3 $\overline{\text{NMI}}$ Interrupt

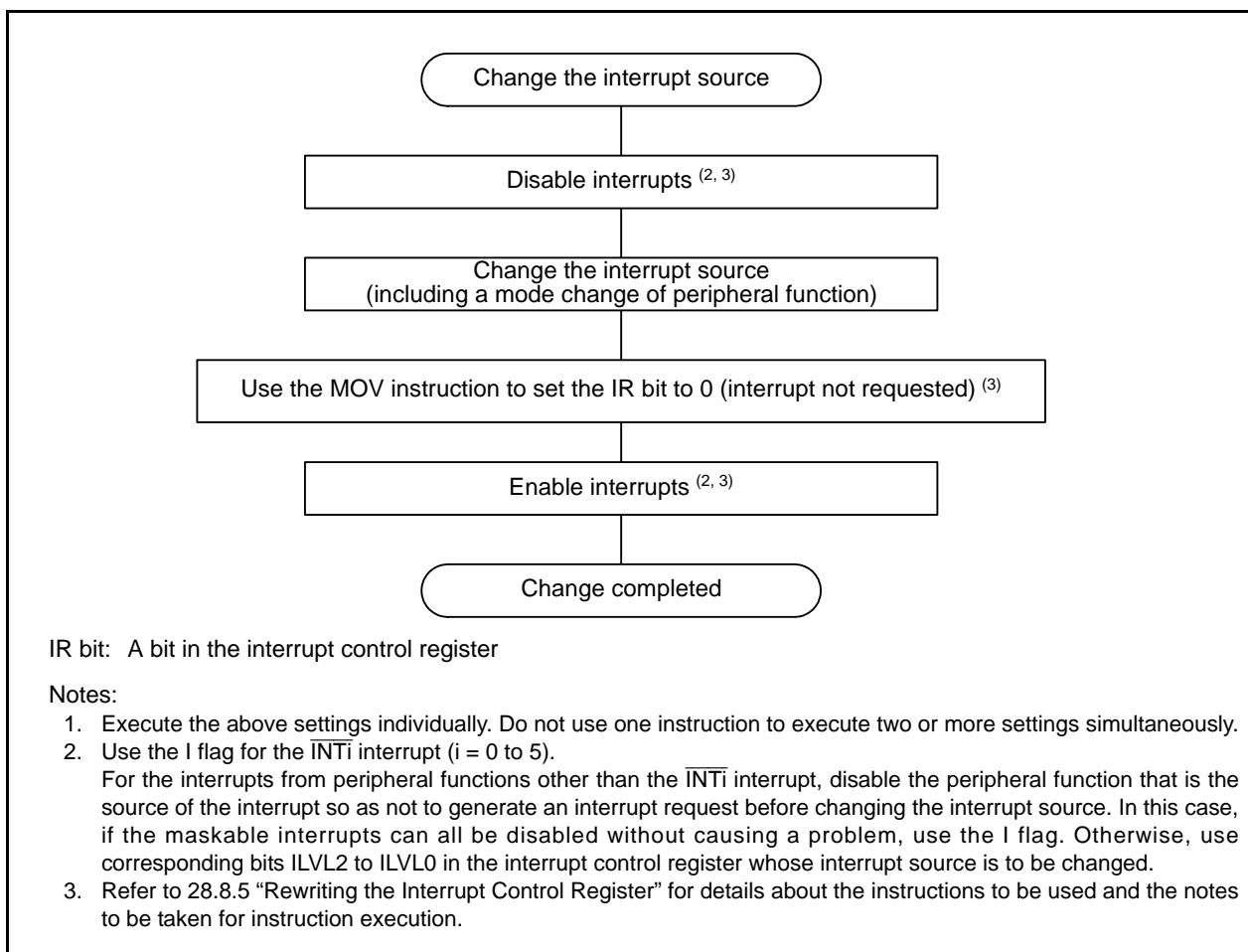
- When not using the  $\overline{\text{NMI}}$  interrupt, set the PM24 bit in the PM2 register to 0 ( $\overline{\text{NMI}}$  interrupt disabled).
- The  $\overline{\text{NMI}}$  interrupt is disabled after reset. The  $\overline{\text{NMI}}$  interrupt is enabled by setting the PM24 bit in the PM2 register to 1. Set the PM24 bit to 1 when a high-level signal is applied to the  $\overline{\text{NMI}}$  pin. When the PM24 bit is set to 1 while a low-level signal is applied, an  $\overline{\text{NMI}}$  interrupt is generated. Once the  $\overline{\text{NMI}}$  interrupt is enabled, it cannot be disabled until the MCU is reset.
- The MCU cannot enter stop mode while the PM24 bit is 1 ( $\overline{\text{NMI}}$  interrupt enabled) and input on the  $\overline{\text{NMI}}$  pin is low. When input on the  $\overline{\text{NMI}}$  pin is low, the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while the PM24 bit is 1 ( $\overline{\text{NMI}}$  interrupt enabled) and a low signal is input to the  $\overline{\text{NMI}}$  pin. When the  $\overline{\text{NMI}}$  pin is driven low, the CPU clock remains active even though the CPU stops, and therefore, the current consumption of the chip does not drop. In this case, the normal condition is restored by the next interrupt generation.
- Set the low- and high-level durations of the input signal to the  $\overline{\text{NMI}}$  pin to 2 CPU clock cycles + 300 ns or more.

### 28.8.4 Changing an Interrupt Source

When the interrupt source is changed, the IR bit in the interrupt control register may become 1 (interrupt requested). To use an interrupt, change the interrupt source, and then set the IR bit to 0 (interrupt not requested).

In this section, the changing of an interrupt source refers to all elements used in changing the interrupt source, polarity, and timing assigned to each software interrupt number. Therefore, if a mode change of any peripheral function involves changing the source, polarity or timing of an interrupt, be sure to clear the IR bit for that interrupt to 0 (interrupt not requested) after making such changes. Refer to the descriptions of the individual peripheral functions for details of the interrupts.

Figure 28.8 shows the Procedure for Changing the Interrupt Generate Source.



**Figure 28.8 Procedure for Changing the Interrupt Generate Source**



### 28.8.5 Rewriting the Interrupt Control Register

To modify the interrupt control register, follow either of the procedures below:

- Modify in places where no interrupt requests corresponding to the interrupt control register may occur.
- If an interrupt request can be generated, disable that interrupt and then rewrite the interrupt control register.

When using the I flag to disable an interrupt, set the I flag as shown in the sample program code below. (Refer to 28.8.6 “Instruction to Rewrite the Interrupt Control Register” for rewriting the interrupt control registers using the sample program code.)

Examples 1 through 3 show how to prevent the I flag from becoming 1 (interrupt enabled) before the contents of the interrupt control register is rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to pause the program until the interrupt control register is modified

```
INT_SWITCH1:
  FCLR      I                ; Disable interrupts.
  AND.B     #00H, 0055H      ; Set the TA0IC register to 00h.
  NOP
  NOP
  FSET      I                ; Enable interrupts.
```

Example 2: Using a dummy read to delay the FSET instruction

```
INT_SWITCH2:
  FCLR      I                ; Disable interrupts.
  AND.B     #00H, 0055H      ; Set the TA0IC register to 00h.
  MOV.W     MEM, R0          ; Dummy read.
  FSET      I                ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC     FLG
  FCLR      I                ; Disable interrupts.
  AND.B     #00H, 0055H      ; Set the TA0IC register to 00h.
  POPC      FLG              ; Enable interrupts.
```

### 28.8.6 Instruction to Rewrite the Interrupt Control Register

- Do not use the BTSTC and BTSTS instructions to rewrite the interrupt control registers.
- Use the AND, OR, BCLR, BSET, or MOV instruction to rewrite interrupt control registers. When an interrupt request is generated for the register being rewritten while executing an AND, OR, BCLR, or BSET instruction, the IR bit becomes 1 (interrupt requested) and remains 1.

### 28.8.7 $\overline{\text{INT}}$ Interrupt

- Either a low level of at least  $t_w(\text{INL})$  width or a high level of at least  $t_w(\text{INH})$  width is necessary for the signal input to pins  $\overline{\text{INT0}}$  through  $\overline{\text{INT5}}$ , regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT5IC or bits IFSR7 to IFSR0 in the IFSR register are changed, the IR bit may inadvertently become 1 (interrupt requested). Be sure to set the IR bit to 0 (interrupt not requested) after changing any of these register bits.

## 28.9 Notes on the Watchdog Timer

After the watchdog timer interrupt is generated, use the WDTR register to refresh the watchdog timer counter.

## 28.10 Notes on DMAC

### 28.10.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

(Technical update number: TN-M16C-92-0306)

When both of the following conditions are met, follow steps (1) and (2) below.

#### Conditions

- Write 1 (DMAi is in active state) to the DMAE bit when it is 1.
- A DMA request may be generated simultaneously when writing to the DMAE bit.

#### Steps

- (1) Set bits DMAE and DMAS in the DMiCON register to 1 simultaneously. <sup>(1)</sup>
- (2) Make sure the DMAi circuit is in an initialized state <sup>(2)</sup> by a program.  
If DMAi is not in an initialized state, repeat these two steps.

#### Notes:

1. The DMAS bit does not change even if set to 1. However, it becomes 0 when set to 0 (DMA not requested). Therefore, when writing to the DMiCON register to set the DMAE bit to 1, set the value to be written to the DMAS bit to 1 to retain its state immediately before writing. Similarly, when writing to the DMAE bit with a read-modify-write instruction, set the DMAS bit to 1 to retain the DMA request that was generated while executing the instruction.
2. Read the TCRi register to verify whether DMAi is in an initialized state.  
If the read value is equal to the value that was written to the TCRi register before the DMA transfer started, DMAi is in an initialized state. When a DMA request is generated after writing to the DMAE bit, the read value is a value written to the TCRi register minus 1. If the read value is a value in the middle of a transfer, DMAi is not in an initialized state.

### 28.10.2 Changing the DMA Request Source

When the DMS bit or any of bits from DSEL4 to DSEL0 in the DMiSL register is changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Set the DMAS bit to 0 (DMA not requested) after changing the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register.

## 28.11 Notes on Timer A

### 28.11.1 Common Notes on Multiple Modes

#### 28.11.1.1 Register Setting

The timer stops after reset. Set the mode, count source, counter value, etc., using registers TAI<sub>MR</sub>, TAI<sub>i</sub>, TAI<sub>1</sub>, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, and TA0TGH in the ONSF register before setting the TAI<sub>S</sub> bit in the TABSR register to 1 (count started) (i = 0 to 4).

Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Always make sure registers TAI<sub>MR</sub>, UDF, TRGSR, PWMFS, TACS0 to TACS2, TAPOFS, TCKDIVC0, PCLKR, and bits TAZIE, TA0TGL, TA0TGH in the ONSF register are modified while the TAI<sub>S</sub> bit is 0 (count stopped), regardless of whether after reset or not.

#### 28.11.1.2 Event or Trigger

When bits TAI<sub>TGH</sub> to TAI<sub>TGL</sub> in the registers ONSF or TRGSR are 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

For some modes of the timers selected using bits TAI<sub>TGH</sub> to TAI<sub>TGL</sub>, an interrupt request is generated by a source other than overflow or underflow.

For example, when using pulse-period measurement mode or pulse-width measurement mode in timer B2, an interrupt request is generated at an active edge of the measurement pulse. For details, refer to the "Interrupt request generation timing" in each mode's specification table.

#### 28.11.1.3 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/CTS2/RTS2/TA1IN/V/TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/W, P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/U/TSUDB

## 28.11.2 Timer A (Timer Mode)

### 28.11.2.1 Reading the Timer

The counter value can be read from the TAI register at any time while counting. However, if the counter is read at the same time as it is reloaded, the read value is FFFFh. Also, if the counter is read before it starts counting, or after a value is set in the TAI register while not counting, the set value is read.

## 28.11.3 Timer A (Event Counter Mode)

### 28.11.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TAI register. However, while reloading, FFFFh can be read in underflow, and 0000h in overflow. When the counter is read before it starts counting and after a value is set in the TAI register while not counting, the set value is read.

## 28.11.4 Timer A (One-Shot Timer Mode)

### 28.11.4.1 Stop While Counting

When setting the TAI<sub>S</sub> bit to 0 (count stopped), the following occurs:

- The counter stops counting and reload register values are reloaded.
- The TAI<sub>OUT</sub> pin outputs a low-level signal when the POFS<sub>i</sub> bit in the TAPOFS register is 0, and outputs a high-level signal when it is 1.
- After one cycle of the CPU clock, the IR bit in the TAI<sub>IC</sub> register becomes 1 (interrupt requested).

### 28.11.4.2 Delay between the Trigger Input and Timer Output

As the one-shot timer output is synchronized with an internally generated count source, when an external trigger is selected, a maximum 1.5 cycle delay of the count source occurs between the trigger input to the TAI<sub>IN</sub> pin and timer output.

### 28.11.4.3 Changing Operating Modes

The IR bit becomes 1 when the timer operating mode is set by any of the following:

- Selecting one-shot timer mode after reset
- Changing the operating mode from timer mode to one-shot timer mode
- Changing the operating mode from event counter mode to one-shot timer mode

To use the timer A<sub>i</sub> interrupt (IR bit), set the IR bit to 0 after the changes listed above are made.

### 28.11.4.4 Retrigger

When a trigger occurs while counting, the counter reloads the reload register to continue counting after generating a retrigger and decrementing once. To generate a trigger while counting, generate a retrigger after at least one cycle of the timer count source has elapsed following the previous trigger. When an external trigger is generated, do not generate a retrigger for 300 ns before the count value becomes 0000h. The one-shot timer may stop counting.

## 28.11.5 Timer A (Pulse Width Modulation Mode)

### 28.11.5.1 Changing Operating Modes

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

### 28.11.5.2 Stop While Counting

When setting the TAI<sub>S</sub> bit to 0 (count stopped) during PWM pulse output, the following occur:

When the POFS<sub>i</sub> bit in the TAPOFS register is 0:

- Counting stops
- When the TAI<sub>OUT</sub> pin is high, the output level goes low and the IR bit becomes 1.
- When the TAI<sub>OUT</sub> pin is low, both the output level and the IR bit remain unchanged.

When the POFS<sub>i</sub> bit in the TAPOFS register is 1:

- Counting stops.
- When the TAI<sub>OUT</sub> pin output is low, the output level goes high and the IR bit is set to 1.
- When the TAI<sub>OUT</sub> pin output is high, both the output level and the IR bit remain unchanged.

## 28.11.6 Timer A (Programmable Output Mode)

### 28.11.6.1 Changing the Operating Mode

The IR bit becomes 1 when setting a timer operating mode with any of the following:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

### 28.11.6.2 Stop While Counting

When setting the TAI<sub>S</sub> bit to 0 (count stopped) during pulse output, the following occur:

When the POFS<sub>i</sub> bit in the TAPOFS register is 0:

- Counting stops.
- When the TAI<sub>OUT</sub> pin is high, the output level goes low.
- When the TAI<sub>OUT</sub> pin is low, the output level remains unchanged.
- The IR bit remains unchanged.

When the POFS<sub>i</sub> bit in the TAPOFS register is 1:

- Counting stops
- When the TAI<sub>OUT</sub> pin output is low, the output level goes high.
- When the TAI<sub>OUT</sub> pin output is high, the output level remains unchanged.
- The IR bit remains unchanged.



## 28.12 Notes on Timer B

### 28.12.1 Common Notes on Multiple Modes

#### 28.12.1.1 Register Setting

The timer is stopped after reset. Set the mode, count source, etc., using registers TBiMR, TBCS0 to TBCS1, TBi, PCLKR and PPWFS1 before setting the TBiS bit in the TABSR register to 1 (count started) (i = 0 to 2).

Rewrite registers TBiMR, TBCS0 to TBCS1, PCLKR, and PPWFS1 while the TBiS bit is 0 (count stopped), regardless of whether after reset or not.

### 28.12.2 Timer B (Timer Mode)

#### 28.12.2.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

### 28.12.3 Timer B (Event Counter Mode)

#### 28.12.3.1 Reading the Timer

While counting, the counter value can be read at any time by reading the TBi register. However, FFFFh is read while reloading. When the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

#### 28.12.3.2 Event

When the TCK1 bit in the TBiMR register is 1, an event occurs when an interrupt request of the selected timer is generated. An event or trigger occurs while an interrupt is disabled because an interrupt request signal is generated regardless of the I flag, IPL, or interrupt control registers.

When the timer selected by the TCK1 bit uses pulse-period measurement mode or pulse-width measurement mode, an interrupt request is generated at an active edge of the measurement pulse.

## 28.12.4 Timer B (Pulse Period/Pulse Width Measurement Modes)

### 28.12.4.1 MR3 Bit in the TBiMR Register

To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is 1 (count started), be sure to set the same value as previously set to bits TMOD0, TMOD1, MR0, MR1, TCK0, and TCK1, and set bit 4 to 0.

### 28.12.4.2 Interrupts

The IR bit in the TBiIC register becomes 1 (interrupt requested) when an active edge of a measurement pulse is input, or timer Bi overflows ( $i = 0$  to  $2$ ). The source of an interrupt request can be determined by setting the MR3 bit in the TBiMR register within the interrupt routine.

Use the IR bit in the TBiIC register to detect overflows only. Use the MR3 bit only to determine the interrupt source.

### 28.12.4.3 Event or Trigger

When timer Bi in pulse-period measurement mode or pulse-width measurement mode is used as an event or trigger for timer A or timer B other than timer Bi, an event or trigger occurs at both the overflow and active edge of the measurement pulse.

### 28.12.4.4 Operations between Count Start and the First Measurement

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, a timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If the count is started in this state, the MR3 bit may become 1 and a timer Bi interrupt request may be generated after the count starts before an active edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stopped), the same value is written to the counter.

### 28.12.4.5 Pulse Period Measurement Mode

When an active edge and overflow are generated simultaneously, input is not recognized at the active edge because an interrupt request is generated only once. Use this mode so an overflow is not generated, or use pulse width measurement mode.

### 28.12.4.6 Pulse Width Measurement Mode

In pulse width measurement, pulse widths are measured successively. Check whether the measurement result is a high-level width or a low-level width in the user program.

When an interrupt request is generated, read the TBiIN pin level in the interrupt routine, and check whether it is the edge of an input pulse or overflow. The TBiIN pin level can be read from bits in the register of ports sharing a pin.

## 28.13 Notes on Three-Phase Motor Control Timer Function

### 28.13.1 Timer A and Timer B

Refer to 15.5 “Notes on Timer A” and 16.5 “Notes on Timer B”.

### 28.13.2 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/ $\overline{CTS2}$ /RTS2/TA1IN/V/TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/ $\overline{W}$ , P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/ $\overline{U}$ /TSUDB

## 28.14 Notes on Timer S

### 28.14.1 Register Access

The explanation for some bits and registers states, “the value written to this register or this bit is reflected to the internal circuit when the clock is synchronized with the base timer count source (fBT1)”. When writing these bits or registers, the written value is not reflected to the internal circuits immediately. After writing the value, prewrite operations are performed for up to one fBT1 cycle. When reading these bits or registers immediately after writing the value, the value before writing may be read.

### 28.14.2 Changing the G1IR Register

Set the G1IR<sub>j</sub> bit in the G1IR register ( $j = 0$  to  $7$ ) to  $0$  by a program since it does not become  $0$  automatically with an interrupt request reception.

However, the G1IR<sub>j</sub> bit cannot be set to  $0$  for one fBT1 cycle after this bit becomes  $1$ . Wait for one or more fBT1 cycles after the G1IR<sub>j</sub> bit becomes  $1$ , then set this bit to  $0$ .

To write  $0$  to the G1IR<sub>j</sub> bit, use the AND and BCLR instructions to avoid deleting requests for other channels.

Figure 28.9 shows “IC/OC Interrupt 0 Operation Example”. As shown in the operation example, disable interrupt requests for all channels once at the last part of an interrupt process, then enable them again.

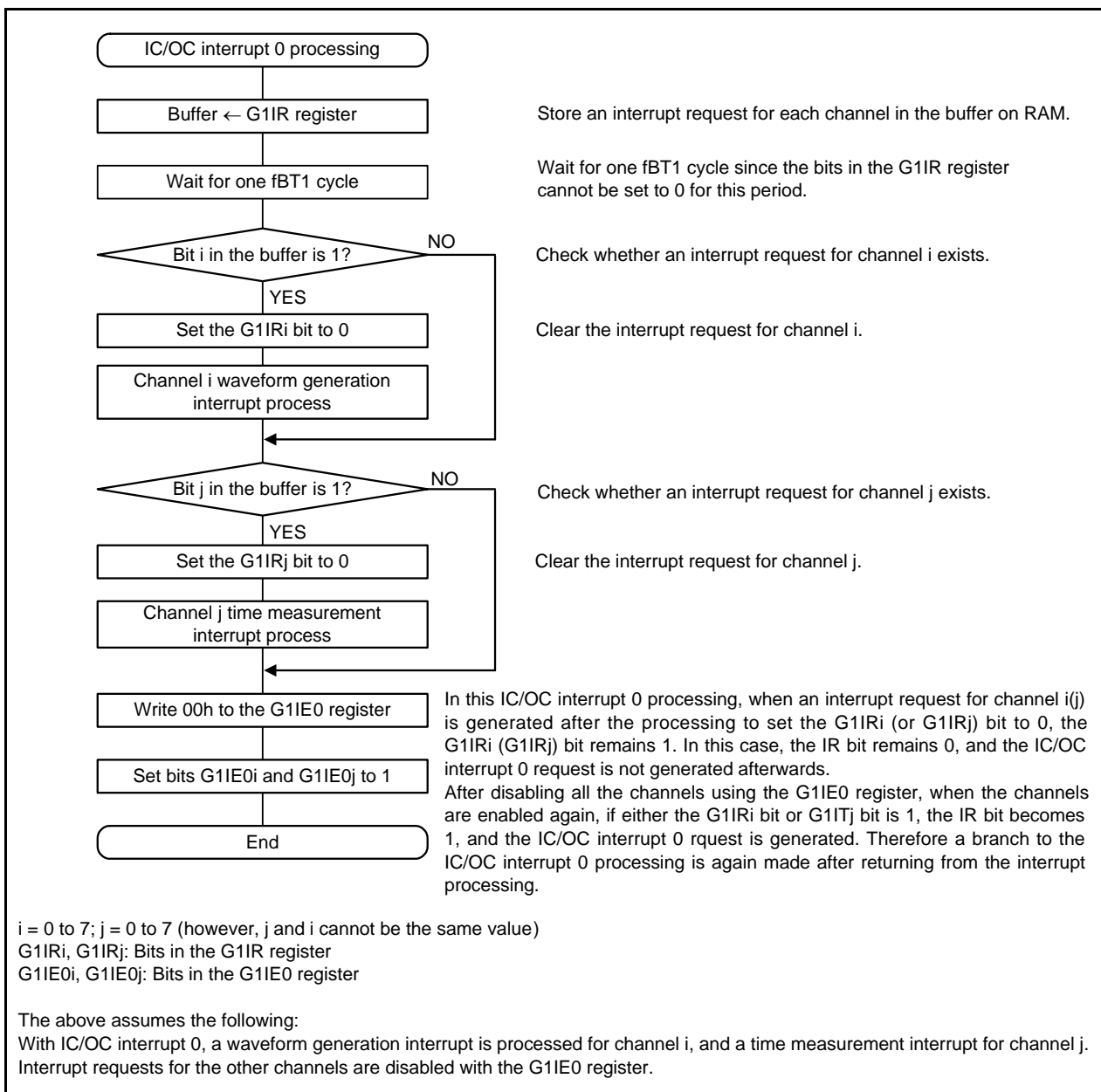


Figure 28.9 IC/OC Interrupt 0 Operation Example

### 28.14.3 Changing Registers ICOCiIC (i = 0, 1)

While the G1IE<sub>j</sub> bit in the G1IE<sub>i</sub> register is 1 (IC/OC interrupt 1 request enabled), use the AND, OR, BCLR, or BSET instruction to change bits ILVL2 to ILVL0 in the ICOCiIC register at the point where a channel j interrupt request may be generated (j = 0 to 7). The IR bit becomes 1 (interrupt requested) if a channel j interrupt is generated while executing these instructions.

If the MOV instruction is used to perform the above, when a channel j interrupt request is generated while executing the MOV instruction, the IR bit does not become 1, and the interrupt request is ignored. The G1IR<sub>j</sub> bit in the G1IR register becomes 1 (interrupt requested) at this timing. If the G1IR<sub>j</sub> remains 1, subsequent IC/OC interrupt i requests are not generated.

When timer S is initialized, change registers ICOCiIC after registers ICOCiIC and G1IR are both set to 00h.

### 28.14.4 Output Waveform During the Base Timer Reset with the BTS bit

When the BTS bit in the G1BCR1 register is set to 0 (base timer reset), the waveform output pin level remains as it is at that point. This output level is held until the base timer value matches the G1PO<sub>j</sub> register value after the BTS bit is set to 1 (base timer starts counting).

### 28.14.5 OUTC1\_0 Pin Output During the Base Timer Reset with the G1PO0 register

While the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset when the base timer matches the G1PO0 register), when the base timer matches the G1PO0 register, the base timer is reset after two fBT1 cycles. During the two fBT1 cycles from when the base timer value matches the G1PO0 register value to the base timer being reset, the OUTC1\_0 pin is driven high. Thus set the EOC0 bit in the G1OER register to 1 (output disabled).

### 28.14.6 Interrupt Request When Selecting Time Measurement Function

When the FSC<sub>j</sub> bit (j = 0 to 7) in the G1FS register is set to 1, and the IFE<sub>j</sub> bit in the G1FE register is also set to 1, the G1IR<sub>j</sub> bit in the G1IR register, or the IR bits in registers ICOCiIC (i = 0, 1) or ICOCHjIC (j = 0 to 3) may become 1 (interrupt requested) after a maximum of two fBT1 cycles.

When using IC/OC interrupt i or IC/OC channel j interrupt, set bits FSC<sub>j</sub> and IFE<sub>j</sub> to 1, then perform the following:

- (1) Wait for two or more fBT1 cycles.
- (2) Set the IR bit in the ICOCiIC register and/or the ICOCHjIC register to 0.
- (3) Wait for three or more fBT1 cycles after the time measurement function is selected. Set the G1IR register to 00h after setting the IR bit in the ICOCiIC register to 0.

## 28.15 Notes on Task Monitor Timer

### 28.15.1 Register Settings

After reset, the task monitor timer counter is stopped. After setting the counter value and count source by setting registers TMOS register and TMOSCS, set the TMOS0S bit in the TMOSSR register to 1 (start counting).

Change the TMOSCS register value when the TMOS0S bit is 0 (stop counting).

### 28.15.2 Reading the Timer

While the task monitor timer is counting, the counter value can be read at any given time by reading the TMOS register. However, when reading the counter at its reload timing, the value is read as FFFFh. When the task monitor timer stops counting and after setting the value to the TMOS register, the setting value can be read until the counter starts counting.

## 28.16 Notes on Real-Time Clock

### 28.16.1 Starting and Stopping the Count

The real-time clock uses the TSTART bit for instructing the count to start or stop, and the TCSTF bit which indicates count started or stopped. Bits TSTART and TCSTF are in the RTCCR1 register.

The real-time clock starts counting and the TCSTF bit becomes 1 (count started) when the TSTART bit is set to 1 (count started). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock <sup>(1)</sup> other than the TCSTF bit.

Similarly, when setting the TSTART bit to 0 (count stopped), the real-time clock stops counting and the TCSTF bit becomes 0 (count stopped). It takes up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock other than the TCSTF bit.

Note:

1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

### 28.16.2 Register Settings (Time Data, etc.)

Write to the following registers/bits when the real-time clock is stopped:

- Registers RTCSEC, RTCMIN, RTCHR, RTCWK, and RTCCR2
- Bits H12H24 and RTCPM in the RTCCR1 register
- Bits RCS0 to RCS4 in the RTCCSR register

The real-time clock is stopped when bits TSTART and TCSTF in the RTCCR1 register are 0 (real-time clock stopped).

Set the RTCCR2 register after setting the registers and bits mentioned above (immediately before the real-time clock count starts).

Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare Mode 1), and Figure 20.5 shows Time and Day Change Procedure (Compare Mode 2 or Compare Mode 3).

### 28.16.3 Register Settings (Compare Data)

Write to the following registers when the BSY bit in the RTCSEC register is 0 (not while data is updated).

- Registers RTCCSEC, RTCCMIN, and RTCCHR



### 28.16.4 Time Reading Procedure in Real-Time Clock Mode

In real-time clock mode, read time data bits <sup>(1)</sup> when the BSY bit in the RTCSEC register is 0 (not while data is updated).

When reading multiple registers, if data is rewritten between reading registers, an errant time will be read. To prevent this, use one of the following steps when reading:

- Using an interrupt

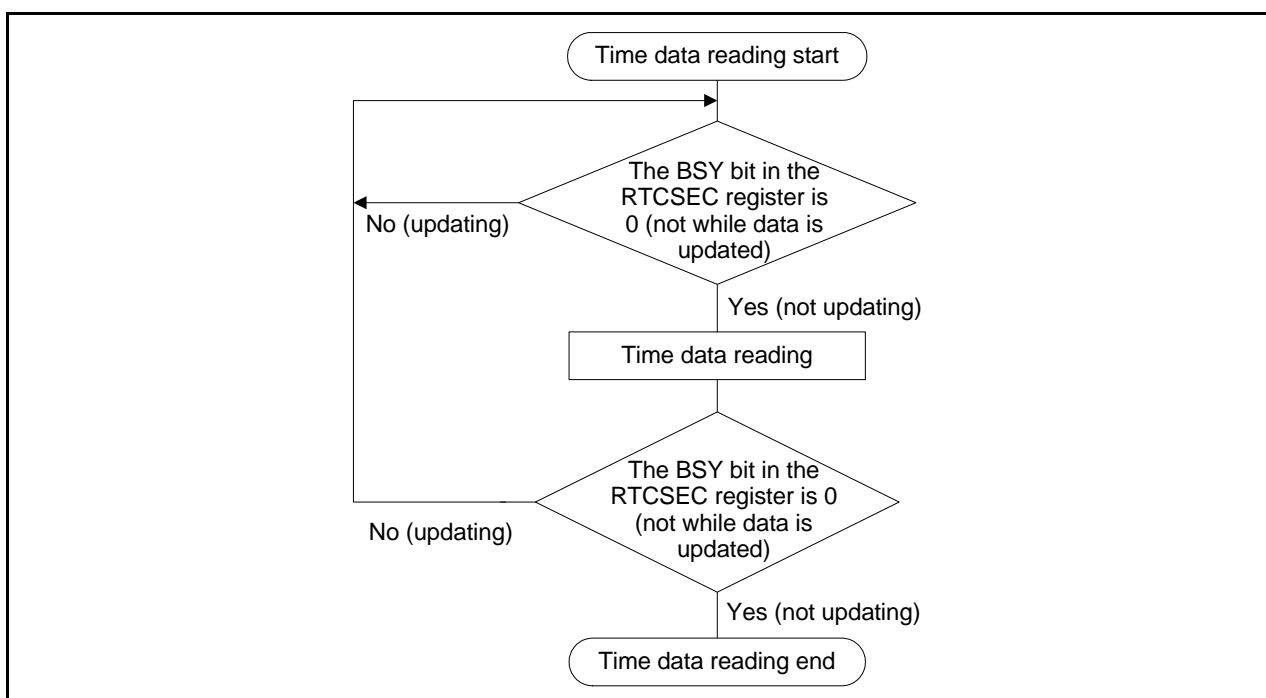
In the real-time clock periodic interrupt routine, read the values necessary from the appropriate time data bits.

- Monitoring by a program 1

Monitor the IR bit in the RTCTIC register by a program and read necessary values of time data bits after the IR bit becomes 1 (periodic interrupt requested).

- Monitoring by a program 2

Read the time data according to Figure 28.10 “Time Data Reading”.



**Figure 28.10 Time Data Reading**

Also, when reading multiple registers, read them as continuously as possible.

Note:

1. Time data bits are as follows:  
 Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register  
 Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register  
 Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register  
 Bits WK2 to WK0 in the RTCWK register  
 The RTCPM bit in the RTCCR1 register

## 28.17 Notes on Serial Interface UARTi (i = 0 to 4)

### Note

Pins CLK4, RXD4, and TXD4 do not exist in the 64-pin package. Do not access the UART4 associated registers.

### 28.17.1 Common Notes on Multiple Modes

#### 28.17.1.1 Influence of $\overline{SD}$

When a low-level signal is applied to the  $\overline{SD}$  pin while the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on  $\overline{SD}$  pin enabled), the following pins become high-impedance: P7\_2/CLK2/TA1OUT/V/RXD1, P7\_3/ $\overline{CTS2}$ / $\overline{RTS2}$ /TA1IN/ $\overline{V}$ /TXD1, P7\_4/TA2OUT/W, P7\_5/TA2IN/ $\overline{W}$ , P8\_0/TA4OUT/U/TSUDA, P8\_1/TA4IN/ $\overline{U}$ /TSUDB

#### 28.17.1.2 Register Setting

Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART4. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART4 again.

### 28.17.2 Clock Synchronous Serial I/O Mode

#### 28.17.2.1 Transmission/Reception

When the  $\overline{RTS}$  function is used with an external clock, the  $\overline{RTSi}$  pin (i = 0 to 3) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The  $\overline{RTSi}$  pin outputs a high-level signal when a receive operation starts. Therefore, transmit timing and receive timing can be synchronized by connecting the  $\overline{RTSi}$  pin to the  $\overline{CTSi}$  pin on the transmitting side. The  $\overline{RTS}$  function is disabled when an internal clock is selected.

#### 28.17.2.2 Transmission

If the transmission is started while an external clock is selected and the TXEPT bit in the UiC0 register (i = 0 to 4) is 1 (no data present in transmit register), meet the last requirement at either of the following timings:

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start transmission (in no particular order):

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When the  $\overline{CTS}$  function is selected, input on the  $\overline{CTSi}$  pin is low.

### 28.17.2.3 Reception

In clock synchronous serial I/O mode, a shift clock is generated by activating a transmitter. Set the UAR*T**i*-associated registers for a transmit operation even if the MCU is used for a receive operations only. Dummy data is output from the TXD*i* pin (*i* = 0 to 4) while receiving.

When an internal clock is selected, a shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), set dummy data in the UiTB register, and input an external clock to the CLK*i* pin to generate a shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is 1 (data present in the UiRB register) and the next receive data is received in the UAR*T**i* receive register. Then, the OER bit in the UiRB register becomes 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs again, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register for each receive operation.

If the reception is started while an external clock is selected and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement at either of the timings below.

External clock level:

- The CKPOL bit in the UiC0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge) and the external clock is high.
- The CKPOL bit is 1 (transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge) and the external clock is low.

Requirements to start reception (in no particular order):

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

## 28.17.3 Special Mode 1 (I<sup>2</sup>C Mode)

### 28.17.3.1 Generating Start and Stop Conditions

(Technical update number: TN-16C-130A/EA)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than a half cycle of the transmit/receive clock. Then set each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

### 28.17.3.2 IR Bit

Set the following bits first, and then set the IR bit in each UART2 interrupt control register to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, the CKPH bit in the U2SMR3 register

### 28.17.3.3 Setup and Hold Times When Generating a Start/Stop Condition

When generating a start condition, the hold time ( $t_{HD:STA}$ ) is a half cycle of the SCL clock. When generating a stop condition, the setup time ( $t_{SU:STO}$ ) is a half cycle of the SCL clock.

When the SDA digital delay function is enabled, take delay time into consideration (see 21.3.3.7 "SDA Digital Delay").

The following shows a calculation example of hold and setup times when generating a start/stop condition.

Calculation example when setting 100 kbps

- U2BRG count source:  $f_1 = 20$  MHz
- U2BRG register setting value:  $n = 100 - 1$
- SDA digital delay setting value: DL2 to DL0 are 101b (5 or 6 cycles of U2BRG count source)

$$f_{SCL} \text{ (theoretical value)} = f_1 / (2(n+1)) = 20 \text{ MHz} / (2 \times (99 + 1)) = 100 \text{ kbps}$$

$$t_{DL} = \text{delay cycle count} / f_1 = 6 / 20 \text{ MHz} = 0.3 \mu\text{s}$$

$$t_{HD:STA} \text{ (theoretical value)} = 1 / (2f_{SCL} \text{ (theoretical value)}) = 1 / (2 \times 100 \text{ kbps}) = 5 \mu\text{s}$$

$$t_{SU:STO} \text{ (theoretical value)} = 1 / (2f_{SCL} \text{ (theoretical value)}) = 1 / (2 \times 100 \text{ kbps}) = 5 \mu\text{s}$$

$$t_{HD:STA} \text{ (actual value)} = t_{HD:STA} \text{ (theoretical value)} - t_{DL} = 5 \mu\text{s} - 0.3 \mu\text{s} = 4.7 \mu\text{s}$$

$$t_{SU:STO} \text{ (actual value)} = t_{SU:STO} \text{ (theoretical value)} + t_{DL} = 5 \mu\text{s} + 0.3 \mu\text{s} = 5.3 \mu\text{s}$$

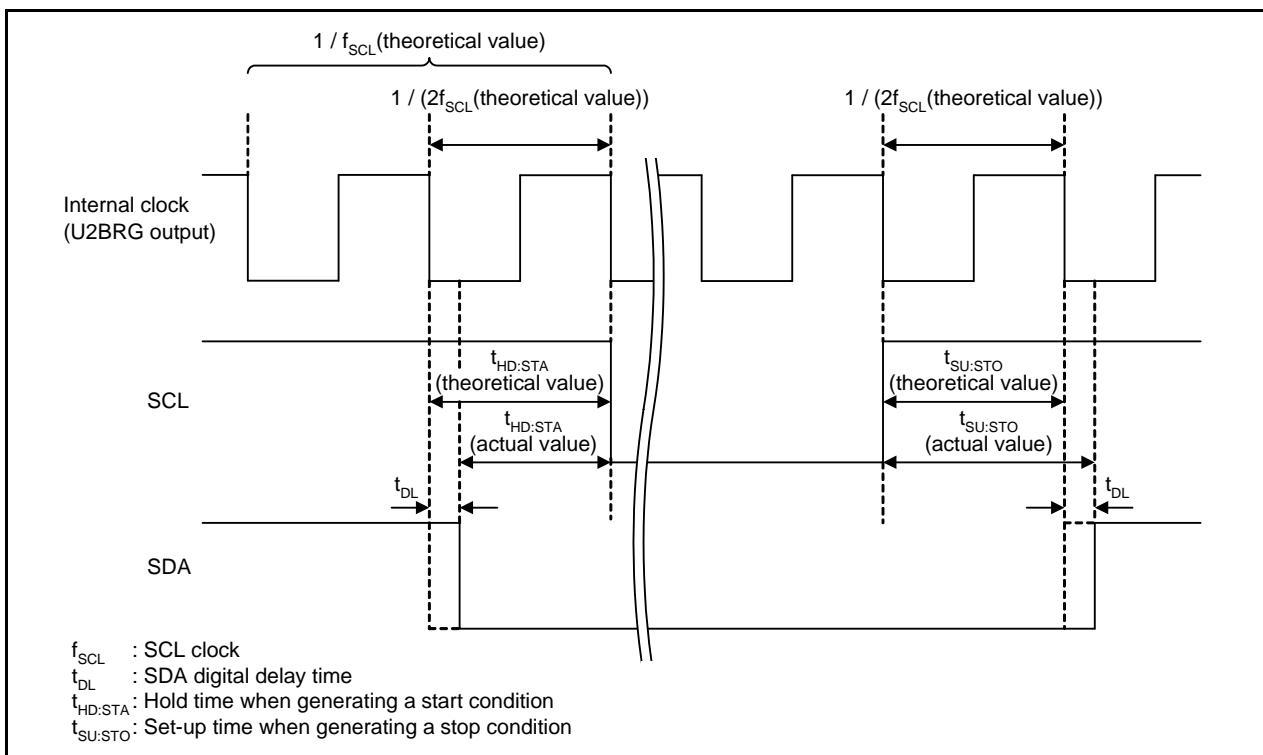


Figure 28.11 Setup and Hold Times When Generating Start and Stop Conditions

### 28.17.3.4 Restrictions on the Bit Rate When Using the U2BRG Count Source

In I<sup>2</sup>C mode, set the U2BRG register to a value of 03h or greater.

A maximum of three U2BRG count source cycles are necessary until the internal circuit acknowledges the SCL clock level. The connectable I<sup>2</sup>C-bus bit rate is one-third or less than the U2BRG count source speed. If a value between 00h to 02h is set to the U2BRG register, bit slippage may occur.

### 28.17.3.5 Restart Condition in Slave Mode

When a restart condition is detected in slave mode, the successive processes may not be executed correctly. In slave mode, do not use a restart condition.

### 28.17.3.6 Requirements to Start Transmission/Reception in Slave Mode

When transmission/reception is started in slave mode and the TXEPT bit in the UiC0 register is 1 (no data present in transmit register), meet the last requirement when the external clock is high.

Requirements to start transmission (in no particular order):

- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

Requirements to start reception (in no particular order):

- The RE bit in the U2C1 register is 1 (reception enabled).
- The TE bit in the U2C1 register is 1 (transmission enabled).
- The TI bit in the U2C1 register is 0 (data present in the UiTB register).

### 28.17.4 Special Mode 4 (SIM Mode)

(Technical update number: TN-M16C-101-0309)

After reset is deasserted, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed, error signal output), then setting the TE bit to 1 (transmission enabled) and the transmission data to the U2TB register. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

## 28.18 Notes on Multi-master I<sup>2</sup>C-bus Interface

### 28.18.1 Limitation on CPU Clock

When the CM07 bit in the CM0 register is 1 (CPU clock is a sub clock), do not access the registers listed in Table 22.4 "Registers". Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock) to access these registers.

### 28.18.2 Register Access

Refer to the notes below when accessing the I<sup>2</sup>C interface control registers. The period from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of an ACK clock is considered to be the transmission/reception period. When the ACKCLK bit is 0 (no ACK clock), the transmission/reception period is from the rising edge of the first clock of the slave address or 1-byte data transmission/reception to the falling edge of the eighth clock.

#### 28.18.2.1 S00 Register

Do not write to the S00 register during transmission/reception.

#### 28.18.2.2 S1D0 Register

Do not change bits other than the IHR bit in the S1D0 register during transmission/reception.

#### 28.18.2.3 S20 Register

Do not change bits other than the ACKBIT bit in the S20 register during transmission/reception.

#### 28.18.2.4 S3D0 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use the MOV instruction to write to this register.
- Rewrite bits ICK1 and ICK0 when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).

#### 28.18.2.5 S4D0 Register

Rewrite bits ICK4 to ICK2 when the ES0 bit in the S1D0 register is 0 (I<sup>2</sup>C interface disabled).

#### 28.18.2.6 S10 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use the MOV instruction to write to this register.
  - Do not write to the S10 register when bits MST and TRX change their values.
- Refer to operation examples in 22.3 "Operations" for bits MST and TRX change.

## 28.19 Notes on CAN Module

Note

Do not use CAN function in the M16C/56 Group.

## 28.20 Notes on A/D Converter

### Note

The 64-pin package has no AN0\_4 to AN0\_7 (P0\_4 to P0\_7), AN2\_0 to AN2\_3 (P1\_0 to P1\_3), AN2\_5 to AN2\_7 (P9\_5 to P9\_7).

### 28.20.1 Analog Input Pin

Do not use any pin from AN4 to AN7 as analog input pin if any pin from  $\overline{KI0}$  to  $\overline{KI3}$  is used as a key input interrupt.

### 28.20.2 Pin Configuration

To prevent operation errors due to noise or latchup, and to reduce conversion errors, place capacitors between the AVSS pin and the AVCC pin, the VREF pin, and analog inputs (AN<sub>i</sub> (i = 0 to 7), AN0<sub>i</sub>, AN2<sub>i</sub>, and AN3<sub>0</sub> to AN3<sub>2</sub>). Also, place a capacitor between the VCC pin and VSS pin.

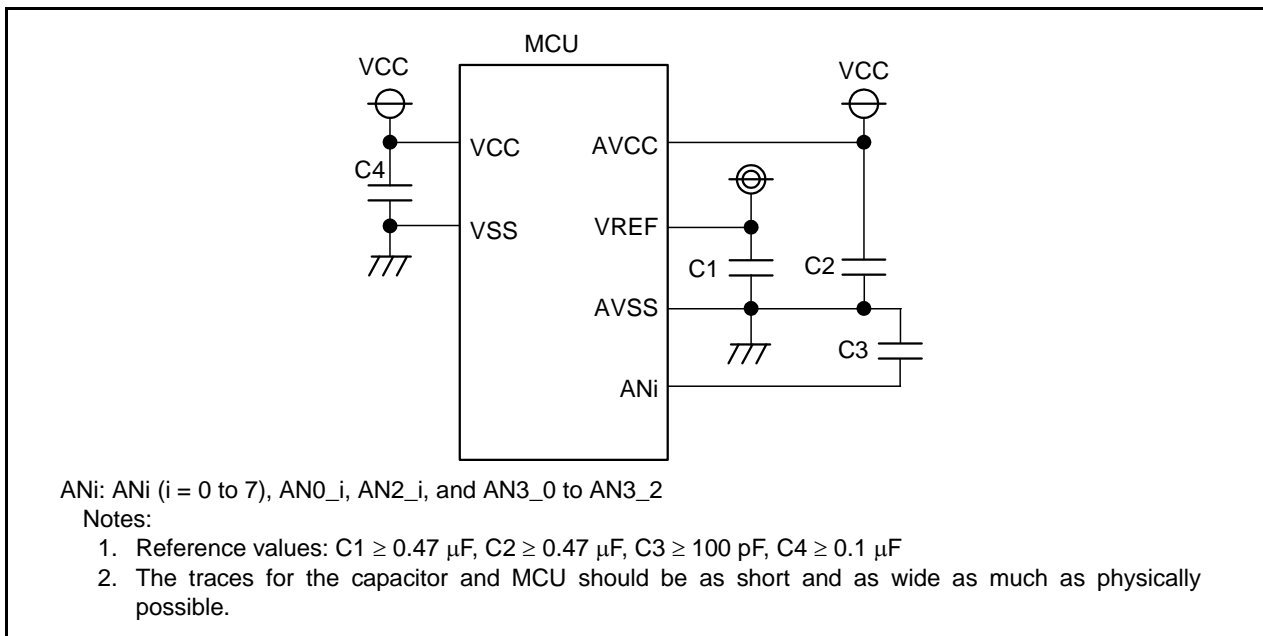


Figure 28.12 Example of Pin Configuration

### 28.20.3 Register Access

Set registers associated with A/D converter after setting the CKS3 bit in the ADCON2 register. However the other bits in the ADCON2 register and the CKS3 bit can be set at the same time. After changing the CKS3 bit, set the others in the same way.

Write registers ADCON0 (excluding the ADST bit), ADCON1, and ADCON2 when A/D conversion stops (before a trigger is generated).

After A/D conversion stops, set the ADSTBY bit in the ADCON1 register from 1 to 0.



### 28.20.4 A/D Conversion Start

When rewriting the ADSTBY bit in the ADCON1 register from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for one  $\phi_{AD}$  cycle or more before starting A/D conversion.

### 28.20.5 A/D Operation Mode Change

When the A/D operation mode has been changed, reselect analog input pins by using bits CH2 to CH0 in the ADCON0 register or bits SCAN1 to SCAN0 in the ADCON1 register.

### 28.20.6 State When Forcibly Terminated

If A/D conversion in progress is halted by setting the ADST bit in the ADCON0 register to 0 (A/D conversion stopped), the conversion result is undefined. In addition, the unconverted AD<sub>i</sub> register ( $i = 0$  to 7) may also become undefined. Do not use any value in AD<sub>i</sub> registers when setting the ADST bit to 0 by a program during A/D conversion.

### 28.20.7 A/D Open-Circuit Detection Assist Function

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation of the system.

When A/D conversion starts after changing the AINRST register, follow these steps:

- (1) Change bits AINRST1 to AINRST0 in the AINRST register.
- (2) Wait for one cycle of  $\phi_{AD}$ .
- (3) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started).

### 28.20.8 Detecting Completion of A/D Conversion

In one-shot mode and single sweep mode, use the IR bit in the ADIC register to detect completion of A/D conversion. When not using an interrupt, set the IR bit to 0 by a program after detection.

When 1 is written to the ADST bit in the ADCON0 register, the ADST bit becomes 1 (A/D conversion start) after start processing time elapses (see Table 24.6 “Cycles of A/D Conversion Item”). Therefore when reading the ADST bit immediately after writing 1, 0 (A/D conversion stop) may be read.

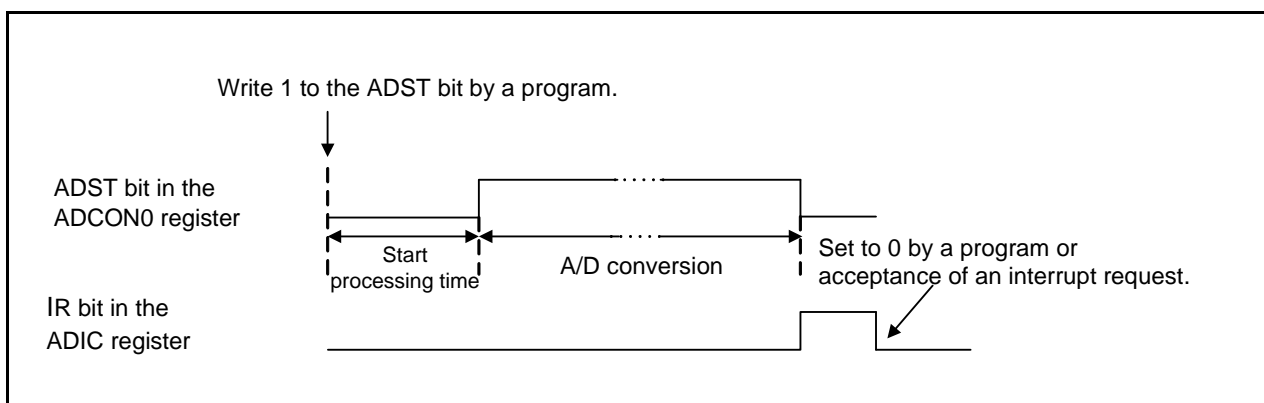


Figure 28.13 ADST Bit Operation

### 28.20.9 $\phi_{AD}$

Divide  $f_{AD}$  so  $\phi_{AD}$  conforms to the standard frequency.

In particular, consider the maximum and minimum values of  $f_{OCO40M}$  when the CKS3 bit in the ADCON2 register is 1 ( $f_{OCO40M}$  is  $f_{AD}$ ).

## 28.21 Notes on Flash Memory

### Note

Pins P0\_4 to P0\_7, P1\_0 to P1\_4, P3\_4 to P3\_7, P9\_5 to P9\_7 cannot be used in the 64-pin package. For the 64-pin package, do not use these pins for the entry of user boot function.

### 28.21.1 OFS1 Address, OFS2 Address, and ID Code Storage Address

The OFS1 address, OFS2 address, and ID code storage address are part of flash memory. When writing a program to flash memory, write an appropriate value to those addresses simultaneously.

In the OFS1 address, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected. The OFS1 address is 0FFFFFFh. This is the most significant address of block 0 in program ROM 1 and upper address of reset vector. Also, OFS2 address and the ID code storage address is in block 0 and upper address of the interrupt vector.

The ID code check function cannot be disabled. Even if the protect using the ID code check function is unnecessary, input the appropriate ID code when using a serial programmer or debugger. Without the appropriate ID code, the serial programmer or debugger cannot be used.

ex) Set FEh to the OFS1 address, and set FFh to the OFS2 address

When using an address control instruction and logical addition:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
```

RESET:

```
.lword start | 0FE00000h
```

When using an address control instruction:

```
.org 0FFDBH
.byte 0FFh
.org 0FFFFCh
```

RESET:

```
.addr start
.byte 0FEh
```

(Program format varies depending on the compiler. Refer to the compiler manual.)

### 28.21.2 Reading Data Flash

When  $3.0\text{ V} < V_{CC} \leq 5.5\text{ V}$  and  $f(\text{BCLK}) \geq 20\text{ MHz}$ , one wait must be inserted to execute the program on the data flash and read the data. Set the PM17 in the PM1 register or FMR17 bit in the FMR1 register to insert one wait.

### 28.21.3 CPU Rewrite Mode

#### 28.21.3.1 Operating Speed

Select a CPU clock frequency of 16 MHz or less by setting the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

#### 28.21.3.2 CPU Rewrite Mode Select

Change FMR01 bit in the FMR0 register, FMR11 bit in the FMR1 register, and FMR60 bit in the FMR6 register while in the following state:

- The PM24 bit in the PM2 register is 0 ( $\overline{\text{NMI}}$  interrupt disabled).
- High is input to the  $\overline{\text{NMI}}$  pin.

Change the FMR60 bit while the FMR00 bit in the FMR0 register is 1 (ready).

#### 28.21.3.3 Prohibited Instructions

Do not use the following instructions in EW0 mode:

UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

#### 28.21.3.4 Interrupts (EW0 Mode and EW1 Mode)

- Do not use an address match interrupt during command execution because the address match interrupt vector is located in ROM.
- Do not use a non-maskable interrupt during block 0 erase because fixed vector is located in block 0.

#### 28.21.3.5 Rewrite (EW0 Mode)

If the power supply voltage drops while rewriting the block where the rewrite control program is stored, the rewrite control program is not correctly rewritten. This may prevent the flash memory from being rewritten. If this error occurs, use standard serial I/O mode or parallel I/O mode for rewriting.

#### 28.21.3.6 Rewrite (EW1 Mode)

Do not rewrite any blocks in which the rewrite control program is stored.

#### 28.21.3.7 DMA transfer

In EW0 mode, do not use flash memory as a source of the DMA transfer.

In EW1 mode, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is 0 (auto programming or auto erasing).

#### 28.21.3.8 Wait Mode

To enter wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction.

#### 28.21.3.9 Stop Mode

To enter stop mode, set the FMR01 bit to 0 (CPU rewrite mode disabled), and then disable DMA transfer before setting the CM10 bit in the CM 1 register to 1 (stop mode).

### 28.21.3.10 Software Command

Observe the notes below when using the following commands.

- Program
- Block erase
- Lock bit program
- Read lock bit status
- Block blank check

- (a) The FMR00 bit in the FMR0 register indicates the status while executing these commands. Do not execute other commands while the FMR00 bit is 0 (busy).
- (b) Use these commands in 40 MHz on-chip oscillator mode, high-speed mode, medium-speed mode, and PLL operating mode. Do not change clock modes while the FMR00 bit in the FMR0 register is 0 (busy).
- (c) After executing the program, block erase, or lock bit program command, perform a full status check per command (Do not execute multiple commands or same command more than once before performing a full status check).
- (d) Do not execute the program, block erase, lock bit program, or block blank check command when either or both bits FMR06 and FMR07 in the FMR0 register are 1 (error).
- (e) Do not use these commands in slow read mode (when the FMR22 bit is 1) or low current consumption read mode (when both bits FMR22 and FMR23 are 1).

### 28.21.3.11 Program and Erase Cycles and Execution Time

Execution time of the program, block erase, and lock bit program commands becomes longer as the number of programming and erasing increases.

### 28.21.3.12 Suspending the Auto-Erase and Auto-Program Operations

When the program, block erase, and lock bit program commands are suspended, the blocks for those commands must be erased. Execute the program and lock bit program commands again after erasing.

Those commands are suspended by the following reset or interrupts:

- Hardware, power-on, voltage monitor 0, voltage monitor 2, oscillator stop detect, watchdog timer, software resets.
- $\overline{\text{NMI}}$ , watchdog timer, oscillator stop/restart detect, and voltage monitor 2 interrupts.

## 28.21.4 User Boot

### 28.21.4.1 User Boot Mode Program

Note the following when using user boot mode:

- When using user boot mode, make sure to allocate the program to be executed to program ROM 2.
- The LVDAS bit in the OFS1 address and bits WDTRCS1 and WDTRCS0 in the OFS2 address are disabled in boot mode.
- When restarting the MCU in user boot mode after starting it in user boot mode, RAM becomes undefined.
- If addresses 13FF8h to 13FFBh are all 00h, the MCU does not enter standard serial I/O mode. Therefore, the programmer or on-chip debugger cannot be connected.
- As the reset sequence differs, the time necessary for starting the program is longer than in single-chip mode.
- Functions in user boot mode cannot be debugged by the on-chip debugging emulator or full spec emulator.
- While using user boot mode, do not change the input level of the pin used for user boot entry. However, if there is a possibility that the input level may change, perform the necessary processes in user boot mode, then restart the MCU in single-chip mode before the input level changes.
- To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

## REGISTER INDEX

<b>A</b>		CM2 .....	97
AD0 to AD7 .....	620	CPSRF .....	234, 283
ADCON0 .....	622	CRCD .....	644
ADCON1 .....	624	CRCIN .....	644
ADCON2 .....	621	CRCMR .....	644
ADIC .....	171	CRCSAR .....	643
AIER .....	176	CSPR .....	203
AIER2 .....	176	<b>D</b>	
AINRST .....	619	DAR0 to DAR3 .....	215
<b>B</b>		DM0CON .....	217
BCNIC .....	171	DM0IC to DM3IC .....	171
BTIC .....	171	DM0SL .....	218
<b>C</b>		DM1CON .....	217
C0AFSR .....	584	DM1SL .....	218
C0BCR .....	555	DM2CON .....	217
C0CLKR .....	554	DM2SL .....	218
C0CSSR .....	583	DM3CON .....	217
C0CTLR .....	550	DM3SL .....	218
C0ECSR .....	592	DTT .....	314
C0EIC .....	171	<b>F</b>	
C0EIER .....	585	FMR0 .....	119, 651
C0EIFR .....	587	FMR1 .....	142, 654
C0FIDCR0, C0FIDCR1 .....	558	FMR2 .....	120, 655
C0FRIC .....	171	FMR3 .....	656
C0FTIC .....	171	FMR6 .....	657
COMB0 to COMB31 .....	562	FRA0 .....	102
COMCTL0 to COMCTL31 .....	566	FRA2 .....	103
COMIER .....	565	<b>G</b>	
COMKIVLR .....	560	G1BCR0 .....	357
COMKR0 to COMKR7 .....	557	G1BCR1 .....	358
COMSMR .....	580	G1BT .....	356
COMSSR .....	581	G1BTRR .....	361
CORECR .....	590	G1DV .....	361
CORFCR .....	570	G1FE .....	359
CORFPCR .....	573	G1FS .....	360
CORIC .....	171	G1IE0 .....	366
COSTR .....	577	G1IE1 .....	367
COTCR .....	595	G1IOR0 .....	363
COTECR .....	591	G1IOR1 .....	364
COTFCR .....	574	G1IR .....	365
COTFPCR .....	576	G1OER .....	362
COTIC .....	171	G1PO0 to G1PO7 .....	351
COTSR .....	594	G1POCR0 to G1POCR7 .....	352
COWIC .....	171	G1TM0 to G1TM7 .....	350
CM0 .....	93	G1TMCR0 to G1TMCR7 .....	354
CM1 .....	95	G1TPR6, G1TPR7 .....	359

I	
ICOC0IC .....	171
ICOC1IC .....	171
ICOCH0IC .....	171
ICOCH1IC .....	171
ICOCH2IC .....	171
ICOCH3IC .....	171
ICTB2 .....	315
IDB0, IDB1 .....	314
IFSR .....	175
IFSR2A .....	174
IFSR3A .....	173
IICIC .....	171
INT0IC to INT2IC .....	172
INT3IC .....	172
INT4IC .....	172
INT5IC .....	172
INVC0 .....	310
INVC1 .....	312

K	
KUPIC .....	171

N	
NDDR .....	153, 178

O	
OFS1 .....	64, 205, 659
OFS2 .....	206, 660
ONSF .....	242

P	
P0 to P3, P6 to P10 .....	160
P17DDR .....	153, 178
PACR .....	159, 449
PCLKR .....	99, 234, 283, 436
PCR .....	156
PD0 to PD3, PD6 to PD10 .....	161
PDRF .....	317
PFCR .....	318
PLC0 .....	100
PM0 .....	62
PM1 .....	140
PM2 .....	101, 170
PPWFS1 .....	285
PRCR .....	57
PRG2C .....	141
PUR0 .....	154
PUR1 .....	154

PUR2 .....	155
PWMFS .....	237

R	
RMAD0 to RMAD3 .....	177
RSTFR .....	63
RTCCHR .....	418
RTCCIC .....	171
RTCCMIN .....	417
RTCCR1 .....	411
RTCCR2 .....	413
RTCCSEC .....	416
RTCCSR .....	415
RTCHR .....	409
RTCMIN .....	408
RTCSEC .....	407
RTCTIC .....	171
RTCWK .....	410

S	
S00 .....	503
S0D0 to S0D2 .....	504
S0RIC to S3RIC .....	171
S0TIC to S2TIC .....	171
S10 .....	516
S11 .....	521
S1D0 .....	505
S20 .....	507
S2D0 .....	509
S3D0 .....	510
S3TIC .....	171
S4D0 .....	514
S4RIC .....	171
S4TIC .....	171
SAR0 to SAR3 .....	215
SCLDAIC .....	171

T	
TA0 to TA4 .....	240
TA0IC to TA4IC .....	171
TA0MR to TA4MR .....	245
TA1, TA2, TA4 .....	309
TA11, TA21, TA41 .....	241, 309
TABSR .....	241, 287
TACS0 to TACS2 .....	236
TAOW .....	239
TAPOFS .....	238
TB0 to TB2 .....	284
TB01 .....	285
TB0IC to TB2IC .....	171

TB0MR .....	288
TB11 .....	285
TB1MR .....	288
TB2 .....	309
TB21 .....	285
TB2MR .....	288
TB2SC .....	316
TBCS0, TBCS1 .....	286
TCKDIVC0 .....	235, 287
TCR0 to TCR3 .....	216
TMOS .....	399
TMOSCS .....	400
TMOSIC .....	171
TMOSPR .....	400
TMOSSR .....	399
TPRC .....	318
TRGSR .....	243

## U

U0BRG to U4BRG .....	438
U0C0 to U4C0 .....	439
U0C1 to U4C1 .....	441
U0MR to U4MR .....	437
U0RB to U4RB .....	442
U0TB to U4TB .....	438
U2SMR .....	448
U2SMR2 .....	447
U2SMR3 .....	446
U2SMR4 .....	444
UCLKSEL0 .....	436
UDF .....	244

## V

VCR1 .....	75
VCR2 .....	76
VD2LS .....	78
VLT0 .....	157
VLT1 .....	158
VLT2 .....	158
VW0C .....	79
VW2C .....	80, 202
VWCE .....	77

## W

WDC .....	204
WDTR .....	203
WDTS .....	204



1. Items revised or added in this version

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	Overall	Specified Renesas Electronics sales office as a contact.
		Overall	Modified register names are as follows: <ul style="list-style-type: none"> <li>• 0075h "CAN0 Receive Completion Interrupt Control Register" to "CAN0 Reception Complete Interrupt Control Register"</li> <li>• 0076h "CAN0 Transmit Completion Interrupt Control Register" to "CAN0 Transmission Complete Interrupt Control Register"</li> <li>• 0071h "CAN0 Wakeup Interrupt Control Register" to "CAN0 Wake-up Interrupt Control Register"</li> <li>• 037Ch "Count Source Protect Mode Register" to "Count Source Protection Mode Register"</li> </ul>
		Overall	Changed terminologies are as follows: <ul style="list-style-type: none"> <li>• "voltage detector 2" to "voltage monitor 2"</li> <li>• "oscillation stop detection reset" to "oscillator stop detect reset"</li> <li>• "detection circuit" to "detector"</li> <li>• "Oscillation stop and re-oscillation detect" to "Oscillator stop/restart detect"</li> <li>• "oscillation/oscillator circuit" to "oscillator"</li> <li>• "oscillator" to "a crystal/ceramic resonator"</li> <li>• "oscillator manufacturer" to "manufacturer of crystal/ceramic resonator"</li> <li>• "on-chip oscillator oscillation circuit" to "on-chip oscillator"</li> </ul>
		<b>Overview</b>	
		3, 5	Table 1.2, Table 1.4 Specifications (2/2) (80-pin, 64-pin): Added the Current Consumption row.
		6	Table 1.5 Product List of M16C/5L Group and Table 1.6 Product List of M16C/56 Group: Changed the product statuses.
		8, 9	Figure 1.3, Figure 1.4 Block Diagram (80-pin, 64-pin): <ul style="list-style-type: none"> <li>• Deleted "8-bit" from the description for the UART/clock synchronous serial interface.</li> <li>• Deleted "(8-bit x 1 channel)" from the description for the Real-time clock.</li> <li>• Added "(1 channel)" to the description for the Multi-master I<sup>2</sup>C-bus.</li> <li>• Moved "dedicated 125 kHz on-chip oscillator for the watchdog timer" to description for the watchdog timer.</li> </ul>
		10, 13	Figure 1.5, Figure 1.6 Pin Assignments (80-pin, 64-pin): Added TSUDA and TSUDB to pins P8_0 and P8_1, respectively.
		11, 14	Table 1.7, Table 1.9 Pin Names (1/2) (80-pin, 64-pin): Added TSUDA and TSUDB to pins P8_0 and P8_1, respectively.
		16	Table 1.11 Pin Functions (64-Pin and 80-Pin Packages) (1/2): <ul style="list-style-type: none"> <li>• Deleted "pin" or "pins" from "input pin/pins" and "output pin/pins".</li> <li>• Changed "low active input" to "input".</li> <li>• Added "Pins" to "AVCC and AVSS" in the Description column of the Analog power supply row.</li> <li>• Deleted "Low active input pin." from the Reset input row.</li> <li>• Changed the description in the Description column of the CNVSS row.</li> <li>• Added footnote reference number (1) in the Sub clock input and output rows in the Description column.</li> <li>• Deleted "INT2 is used to input Z-phase of timer A" in the Description column of the <math>\overline{\text{INT}}</math> interrupt input row.</li> <li>• Added UART0 to UART3 in the Signal Name column of the Serial interface row.</li> <li>• Added UART2 to the Signal Name column of the I<sup>2</sup>C mode row.</li> </ul>
17	Table 1.12 Pin Functions (64-Pin and 80-Pin Packages) (2/2): <ul style="list-style-type: none"> <li>• Changed "low active input" to "input".</li> <li>• Added "TSUDA, TSUDB" to the Pin Name in the Timer S row.</li> <li>• Changed "Input pin" to "Receive data input" and "Output pin" to "Transmit data output" in the Description column of the CAN Module row.</li> <li>• In the Description column of the I/O port row, changed the explanation of the direction register, and changed "4 input ports" to "4 bits".</li> </ul>		
18	Table 1.13 Pin Functions (80-Pin Package Only): <ul style="list-style-type: none"> <li>• Added UART4 to the Signal Name column of the Serial interface row.</li> <li>• In the Description column of the I/O port row, changed the explanation of the direction register, and changed "4 input ports" to "4 bits".</li> </ul>		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	<b>Memory</b>	
		23	Figure 3.1 Memory Map: <ul style="list-style-type: none"> <li>• Added note 2.</li> <li>• Added footnote reference numbers (1) and (2).</li> </ul>
		<b>Special Function Registers (SFRs)</b>	
		55	4.2.1 Register Settings: Added the description regarding read-modify-write instructions.
		56	Table 4.33 Read-Modify-Write Instructions: Added.
		<b>Resets</b>	
		60	Table 6.1 Types of Resets: Added the "Registers and Bits Not to Reset" column.
		60	Figure 6.1 Reset Circuit Block Diagram: Deleted SFR names from the figure, and the SFR details are described in Table 6.2 Classification of SFRs Which are Reset.
		61	Table 6.2 Classification of SFRs Which are Reset: Added.
		62	Table 6.4 Registers: <ul style="list-style-type: none"> <li>• Changed the reset value of the RSTFR register from "XX0X 001Xb".</li> <li>• Added note 1.</li> </ul>
		63	6.2.2 Reset Source Determine Register (RSTFR): HWR bit explanation: Changed "the reset" to "the hardware reset" in the last sentence. OSDR bit explanation: Added "Conditions to become 0" to the explanation.
		64	6.3.1 Optional Function Select Address 1 (OFS1): Added "This bit is enabled in single-chip mode, while disabled in boot mode." to the LVDAS bit explanation.
		66	Table 6.7 Pin Status When $\overline{\text{RESET}}$ Pin Level is Low: Changed note 1.
		67	Figure 6.3 Reset Sequence: Changed the oscillation period of XIN.
		68	6.4.2 Hardware Reset: Changed "20 fOCO-S cycles" to "tw(RSTL)" in When the power supply is stable, (2). Changed "20 fOCO-S cycles" to "1/fOCO-S x 20 cycles" in When the power is turned on, (4).
		69	6.4.3 Power-On Reset Function: Changed "at 0.8 VCC or more" to "in the range of VIH" in the first paragraph.
		69	Figure 6.5 Example of Power-On Reset Operation: Changed "External power VCC" to "VCC".
		70	6.4.6 Oscillator Stop Detect Reset: Added "after oscillator stop detect reset" to the sentence starting with "The OSDR bit...".
		70	6.4.7 Watchdog Timer Reset: Added "after watchdog timer reset" to the sentence starting with "The WDR bit...".
		71	6.4.8 Software Reset: Added "after software reset" to the sentence starting with "The SWR bit...".
		72	Figure 6.6 SVCC Timing: Revised.
		<b>Voltage Detector</b>	
		88	Figure 7.6 Voltage Monitor 2 Interrupt/Reset Operation Example: Added "or above" to note 1.
		<b>Clock Generator</b>	
		Chap. 8.	Changed the bit name from "XCIN-XCOUT drive level select bit" to "XCIN-XCOUT drive capacity select bit".
		Chap. 8.	Deleted descriptions regarding 0004h Processor Mode Register 0.
		90	Table 8.1 Clock Generator Specifications: <ul style="list-style-type: none"> <li>• Changed the description for the Clock frequency row.</li> <li>• Rewrote note 1.</li> </ul>
		91	Figure 8.1 System Clock Generator: <ul style="list-style-type: none"> <li>• Deleted buffers in the peripheral clock, and added the main clock.</li> <li>• Changed the description of the circuit after the main clock in the Oscillator Stop/Restart Detector.</li> <li>• Changed a part of the configuration in the PLL frequency synthesizer.</li> </ul>
		93	8.2.1 System Clock Control Register 0 (CM0): <ul style="list-style-type: none"> <li>• Deleted I/O port names from the Function column in the register diagram.</li> <li>• Rewrote bit explanations.</li> <li>• Added description for 40 MHz on-chip oscillator mode to the CM05 bit explanation.</li> </ul>

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description			
		Page	Summary		
1.10	Sep. 01, 2011	95	8.2.2 System Clock Control Register 1 (CM1): <ul style="list-style-type: none"> <li>• CM10 bit explanation: Rewrote the condition for the bit to remain unchanged as a bulleted list, and added the last two conditions to the list.</li> <li>• CM13 bit explanation: Changed the description for connection between XIN and XOUT.</li> <li>• CM14 and CM15 explanation: Rewritten.</li> </ul>		
		101	8.2.6 Processor Mode Register 2 (PM2): <ul style="list-style-type: none"> <li>• Corrected "CM20 register" typo to "CM2 register" in the PM21 bit explanation.</li> <li>• Changed the name of the PM21 bit from "System clock protect bit" to "System clock protection bit".</li> <li>• Changed the name of the PM25 bit from "Peripheral clock fC enable bit" to "Peripheral clock fC provide bit".</li> </ul>		
		102	8.2.7 40 MHz On-Chip Oscillator Control Register 0 (FRA0): Changed the name of the FRA01 bit from "40-MHz on-chip oscillator select bit" to "On-chip oscillator select bit".		
		104	8.3.1 Main Clock: <ul style="list-style-type: none"> <li>• Changed "oscillator" to "ceramic resonator or crystal".</li> <li>• Changed the description in the parenthesis in To start the main clock oscillation, (3).</li> </ul>		
		104	Figure 8.2 Main Clock Connection Example: Rewrote note 1.		
		105	8.3.2 PLL Clock: Changed the explanation of how to generate the PLL clock from the main clock.		
		105	Figure 8.3 Relation between Main Clock and PLL Clock: Changed note 2.		
		106	8.3.4 fOCO-F: Changed the description for the clock division of 40 MHz.		
		106	8.3.5 125 kHz On-Chip Oscillator Clock (fOCO-S): Added the description for when the CSPRO bit in the CSPR register is 1 to the first paragraph.		
		107	Figure 8.4 Sub Clock Connection Example: Changed the title.		
		108	8.4.1 CPU Clock and BCLK: <ul style="list-style-type: none"> <li>• Added "fOCO-F" to the third paragraph.</li> <li>• Deleted the description for the clock division when fOCO-F is selected as the clock source for the CPU clock.</li> <li>• Changed the description for when the CM06 bit becomes 1.</li> </ul>		
		108	8.4.2 Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC, Main Clock): <ul style="list-style-type: none"> <li>• Changed "fOCO-F divided by 2, 4, or 8" to "fOCO-F divided by 1 (no division)".</li> <li>• Deleted the A/D converter from the functions which can use fOCO-F.</li> <li>• Added the description about the PM25 bit to the explanation of fC.</li> <li>• Added descriptions regarding the main clock.</li> </ul>		
		109	Figure 8.5 Peripheral Function Clocks: Revised		
		111	Table 8.6 Oscillator Stop/Restart Detect Function Specifications: Changed descriptions in the Item column.		
		111	8.7.1 Operation When CM27 Bit is 0 (Oscillator Stop Detect Reset): Added "voltage monitor 0 reset" to the description for status cancellation.		
		113	8.7.3 Using the Oscillator Stop/Restart Detect Function: Moved the explanations to 8.8 Interrupt except the one for after detected oscillation stop.		
		113	8.8 Interrupt: Added.		
		117	8.9.5 PLL Frequency Synthesizer: Changed "to meet the power supply ripple standard" to "within the acceptable range of power supply ripple".		
		117	Figure 8.11 Voltage Fluctuation Timing: Changed the range of $f_{(ripple)}$ .		
				<b>Power Control</b>	
		Chap. 9.	Changed terminologies are as follows: <ul style="list-style-type: none"> <li>• "fOCO-S" to "125 kHz on-chip oscillator" (distinguished between signal name and circuit name)</li> <li>• "fOCO-F" to "40 MHz on-chip oscillator" (distinguished between signal name and circuit name)</li> </ul>		
		119	9.2.1 Flash Memory Control Register 0 (FMR0): Changed the bit explanations for FMR01 and FMSTP.		
120	9.2.2 Flash Memory Control Register 2 (FMR2): FMR23 bit explanation: Rewrote and added usage restrictions.				

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	122	9.3.1.3 40 MHz On-Chip Oscillator Mode: Changed the description for the clock division of fOCO-F in the first paragraph.
		123	9.3.1.6 Low-Speed Mode: Changed the division of fOCO-F for when bits CM21 and FRA01 are both 1.
		123	9.3.1.7 Low Power Mode: Deleted the explanation about the CM06 bit.
		124	Table 9.2 Clocks in Normal Operating Mode: <ul style="list-style-type: none"> <li>• Changed "fOCO-F divided by 2, 4, or 8" to "fOCO-F divided by 1".</li> <li>• Changed "and/or" to "and" for the explanation of bit settings in note 1.</li> <li>• Combined notes 2 to 6 into note 2.</li> </ul>
		124, 125	Table 9.3 Clock-Related Bit Setting and Modes, Table 9.4 Selecting Clock Division Related Bits, Table 9.5 Example Settings for 40 MHz On-Chip Oscillator Mode Division Related Bits: Added a legend below each table.
		126	9.3.2 Clock Mode Transition Procedure: <ul style="list-style-type: none"> <li>• (1) in b: Changed "Select the reference clock division" to "Select the division of reference frequency counter".</li> <li>• e: Added "low-speed mode".</li> <li>• i: Corrected "40 kHz on-chip oscillator" typo to "40 MHz on-chip oscillator".</li> </ul>
		129	9.3.3 Wait Mode: Changed the explanation about the operation of peripheral functions.
		129	9.3.3.2 Entering Wait Mode: Added a procedure for entering wait mode.
		130	9.3.3.4 Exiting Wait Mode: Deleted the explanations below the table except the explanation about exiting wait mode using an interrupt.
		130	Table 9.7 Resets and Interrupts to Exit Wait Mode and Conditions for Use: <ul style="list-style-type: none"> <li>• Changed the conditions for use in the Serial interface row.</li> <li>• Changed the conditions for use in the CM02 = 1 column of the A/D converter row.</li> <li>• Changed the conditions for use in the Voltage monitor 2 row.</li> <li>• Changed "Usable when fOCO-S is supplied" to "Usable" in the Voltage monitor 0 reset row.</li> <li>• Changed the conditions for use in the Voltage monitor 2 reset row.</li> </ul>
		131	9.3.4.1 Entering Stop Mode: <ul style="list-style-type: none"> <li>• Deleted "However, when the PM21 bit in the PM2 register is 1 (disables a clock change) or when the CSPRO bit in the CSPR register is 1 (watchdog timer count source protect mode enabled), writing the CM10 bit has no effect and the MCU does not enter stop mode." from the first paragraph.</li> <li>• Moved some of explanations under Table 9.9 here and added a procedure for entering stop mode.</li> </ul>
		132	Table 9.10 CPU Clock After Exiting Stop Mode: <ul style="list-style-type: none"> <li>• Changed the description for the fOCO-F clock division.</li> <li>• Deleted note 1.</li> </ul>
		133	9.4 "Power Control in Flash Memory": Added title.
		133	Figure 9.2 Stop and Restart of the Flash Memory: <ul style="list-style-type: none"> <li>• Deleted the description of "Program A".</li> <li>• Changed the ranges of the Stop Procedure and Restart Procedure.</li> <li>• Added "or 40 MHz on-chip oscillator to start oscillator" in the first process box in the restart procedure.</li> <li>• Deleted note 4.</li> </ul>
		134	9.4.2.1 Slow Read Mode: <ul style="list-style-type: none"> <li>• Changed "f(BCLK) must be f(SLOW_R)" to "f(BCLK) is less than or equal to f(SLOW_R)" in the first line.</li> <li>• Added an explanation for when no wait operation is required.</li> </ul>
		134, 135	Figure 9.3 Setting and Canceling Slow Read Mode, Figure 9.4 Setting and Canceling Low Current Consumption Read Mode: Deleted the last process to restore the CPU clock from the canceling procedure.
135	9.4.2.2 Low Current Consumption Read Mode: Deleted "To enter low current consumption read mode, set or the sub clock or fOCO-S divided by 8 or 16 as the CPU clock." from the first paragraph.		
136	9.5.2 A/D Converter: Deleted the explanation for when A/D conversion is performed.		
137	9.6.1 CPU Clock: Added line 2.		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	137	9.6.2 Wait Mode: <ul style="list-style-type: none"> <li>• Added lines 4 and 5 to the first bullet.</li> <li>• Deleted second bullet in the previous version and added the second to fifth bullets.</li> </ul>
		137	9.6.3 Stop Mode: <ul style="list-style-type: none"> <li>• Added the last sentence to the third bullet.</li> <li>• Deleted fifth bullet in the previous version and added fourth to ninth bullets.</li> </ul>
		138	9.6.4 Low Current Consumption Read Mode: Added the third bullet.
		138	9.6.5 Slow Read Mode: Added.
		<b>Processor Mode</b>	
		143	10.4 Bus Hold: Added.
		<b>Programmable I/O Ports</b>	
		161	11.3.12 Port Pi Direction Register (PDi) (i = 0 to 3, 6 to 10): Port P9 Direction Register: Corrected typo in all bit symbols from "P9_" to "PD9_".
		166	11.6.2 Influence of $\overline{SD}$ : <ul style="list-style-type: none"> <li>• Changed the title from "Effect of <math>\overline{SD}</math> Pin".</li> <li>• Changed the explanation.</li> </ul>
		<b>Interrupt</b>	
		170	12.2.1 Processor Mode Register 2 (PM2): Changed the bit name and the function of the PM25 bit.
		171, 172	12.2.2 Interrupt Control Register 1 and 12.2.3 Interrupt Control Register 2: Moved symbol and address information to the tables below the register diagram.
		174	12.2.5 Interrupt Source Select Register 2 (IFSR2A): Changed the Function column of the IFSR24 bit.
		181	12.5.1.3 Watchdog Timer Interrupt: Changed "initialize the watchdog timer" to "refresh the watchdog timer".
		182	12.6.1 Fixed Vector Tables: Changed "used by the ID code check function" to "used for the ID code check function and OFS1 address".
		184	Table 12.7 Relocatable Vector Tables (2/2): Changed note 5.
		186	Figure 12.3 Time Required for Executing Interrupt Sequence: Changed "accept instructions" to "prefetch" in note 1.
		192	12.10 Key Input Interrupt: Rewritten.
		<b>Watchdog Timer</b>	
		199	Table 13.1 Watchdog Timer Specifications: <ul style="list-style-type: none"> <li>• Changed "Watchdog timer counter reset value conditions" to "Watchdog timer counter refresh timing" in the Item column.</li> <li>• Changed the description for Prescaler divide ratio in the Selectable functions row.</li> </ul>
		202	13.2.1 Voltage Monitor 2 Control Register (VW2C): <ul style="list-style-type: none"> <li>• Changed the VW2C3 bit name from "WDT detection flag" to "Watchdog timer detection flag".</li> <li>• Changed the VW2C6 bit name from "Voltage monitor 2 circuit mode select bit" to "Voltage monitor 2 mode select bit".</li> <li>• Deleted "voltage monitor 1 reset" from the register explanation.</li> <li>• VW2C3 bit explanation: Deleted the first bullet from the description for Conditions to become 0.</li> </ul>
		203	13.2.2 Count Source Protection Mode Register (CSPR): <ul style="list-style-type: none"> <li>• Changed bits b6 to b0 from "Reserved bits" to "No register bits".</li> <li>• Changed "125-kHz on-chip oscillator" to "Dedicated 125 kHz on-chip oscillator" in the first bullet of the CSPRO bit explanation.</li> </ul>
		206	13.3.2 Optional Function Select Address 2 (OFS2): Changed the bit name of WDTUFS1 and WDTUFS0 from "Watchdog timer reset value setting bit" to "Watchdog timer initial setting bit".
		207	13.4.1 Refresh Operation Period: Rewritten.
		<b>DMAC</b>	
		212	Table 14.1 DMAC Specifications: <ul style="list-style-type: none"> <li>• Corrected "DMAiCON" typo to "DMiCON" in the Specifications column of DMA transfer start.</li> <li>• Changed "SARi or DARi pointer" to "SARi or DARi register" in the Specifications column of the Reload timing for forward address pointer and DMAi transfer counter row.</li> </ul>

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description			
		Page	Summary		
1.10	Sep. 01, 2011	213	Figure 14.1 DMAC Block Diagram: Unified data buses for low/high-order bits with a single data bus.		
		221	Table 14.7 Timing at Which the DMAS Bit Value Changes: Changed "selected by setting bits DSEL4 to DSEL0" to "selected by setting bits DSEL4 to DSEL0 and DMS" in the Timing at which the bit becomes 1 column of the External source row.		
		222	14.3.3 Transfer Cycles: Added "and the source and destination addresses are both odd addresses" to the second line from the bottom.		
		227	Figure 14.5 DMA Transfer Initiated by External Sources: Changed "DMAS bit in DMA0" and "DMAS bit in DMA1" to "DMAS bit in the DM0CON register" and "DMAS bit in the DM1CON register", respectively.		
		<b>Timer A</b>			
		230	Figure 15.1 Timer A and B Count Sources: Deleted the divide-by-2 circuit on fOCO-F.		
		231	Figure 15.2 Timer A Configuration: Corrected "TAiGH to TAiGL" typo to "TAiTGH to TAiTGL".		
		232	Table 15.3 I/O Ports: Changed "the port direction bits corresponding to the pins to 0" to "the port direction bits sharing pins to 0" in note 1.		
		242	15.2.11 One-Shot Start Flag (ONSF): Changed the last sentence of the TA0TGH-TA0TGL bit explanation.		
		243	15.2.12 Trigger Select Register (TRGSR): Changed the last sentence of the bit explanation about bits TA1TGH-TA1TGL, TA2TGH-TA2TGL, TA3TGH-TA3TGL, and TA4TGH-TA4TGL.		
		247	15.3.1.3 Count Source: Changed "fOCO-F divided by 2, 4, or 8" to "fOCO-F divided by 1 (no division)".		
		249,253, 257,262, 266	Table 15.7, Table 15.9, Table 15.11, Table 15.13, and Table 15.15 Registers and Settings: <ul style="list-style-type: none"> <li>• Added TAOW.</li> <li>• Changed "TAiTGH and TAiTGL" to "TA0TGH to TA0TGL" in the Bit column of ONSF.</li> </ul>		
		252	Table 15.8 Event Counter Mode Specifications (When Not Using Two-Phase Pulse Signal Processing): <ul style="list-style-type: none"> <li>• Deleted "by a program" from the first bullet in the Specification column of the Count source row.</li> <li>• Added "When selecting reload type:" to the Specification column of the Number of counts row.</li> </ul>		
		256	Table 15.10 Event Counter Mode Specifications (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4): <ul style="list-style-type: none"> <li>• Added "When selecting reload type:" to the Specification column of the Number of counts row.</li> </ul>		
		260	Figure 15.9 Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase: <ul style="list-style-type: none"> <li>• Added "(Z-phase)".</li> <li>• Changed the description of input pulse for ZP input.</li> </ul>		
		261	15.3.5 One-Shot Timer Mode: Changed "the timer counter decrements" to "the timer starts" in the explanation.		
		261	Table 15.12 One-Shot Timer Mode Specifications: Changed the descriptions in the Write to timer row.		
		265	Table 15.14 PWM Mode Specifications: Changed the Specification in the Count start condition row.		
		271	Table 15.17 Registers and Settings in Programmable Output Mode: Changed "TAiTGH and TAiTGL" to "TA0TGH to TA0TGL" in the Bit column of ONSF.		
		275	15.5 Notes on Timer A: Rewritten by common items, and each mode.		
		<b>Timer B</b>			
		279	Figure 16.1 Timer A and B Count Sources: Deleted the divide-by-2 circuit on fOCO-F.		
		284	16.2.3 Timer Bi Register (TBi) (i = 0 to 2): Deleted the description about "TBSR" from the Pulse Period Measurement Mode, Pulse Width Measurement Mode bit explanation.		
		290	16.3.1.3 Count Source: Changed "fOCO-F divided by 2, 4, or 8" to "fOCO-F divided by 1 (no division)".		
		294	16.3.3 Event Counter Mode: <ul style="list-style-type: none"> <li>• Changed "TBj overflow or underflow" to "timer Bj" in the Function column of the TCK1 bit in the register diagram and the explanation of bits MR1 and MR0 explanation.</li> <li>• Added the TCK1 bit explanation.</li> </ul>		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	296	Table 16.9 Specifications of Pulse Period/Pulse Width Measurement Modes: <ul style="list-style-type: none"> <li>• Moved previous note 3 to the description for TBiS above notes.</li> <li>• Added note 3.</li> </ul>
		297	Table 16.10 Registers and Settings in Pulse Period/Pulse Width Measurement Modes: Modified "TBCS0 to TBCS3" to "TBCS0 to TBCS1" in the Register column.
		302	16.5 Notes on Timer B: Rewritten by common items, and each mode.
		<b>Three-Phase Motor Control Timer</b>	
		Chap. 17	Changed "Three-Phase Motor Control Timer" to "Three-Phase Motor Control Timer Function".
		305	Table 17.1 Three-Phase Motor Control Timer Function Specifications: Changed "Three-phase waveform output pins" to "Three-phase PWM waveform output pins" in the Item column.
		325	Table 17.8 Three-Phase Mode 0 Specifications: Modified the description in the parenthesis in the Timer B2 interrupt row.
		337	Table 17.15 Sawtooth Wave Modulation Mode Specifications: Modified the description in the parenthesis in the Timer B2 interrupt row.
		343	17.5.2 Influence of $\overline{SD}$ : Changed the title from "Forced Cutoff Input" and changed the explanation.
		<b>Timer S</b>	
		Chap. 18.	Changed the configuration, and added detailed explanations.
		Chap. 18.	Changed terminologies in this chapter are as follows: <ul style="list-style-type: none"> <li>• "digital debounce function" to "digital debounce filter"</li> <li>• Remove the term "mode" from increment, increment/decrement, and two-phase pulse signal processing.</li> <li>• "channel interrupt" to "IC/OC channel interrupt"</li> <li>• "base timer interrupt" to "IC/OC base timer interrupt"</li> <li>• Appropriate explanations/names are provided for base timer reset depending on its condition.</li> <li>• "fBT1 clock cycles" to "fBT1 cycles"</li> </ul>
		Chap. 18.	Specified the internal circuit as the place to reflect a value written to the GT bit when the clock is synchronized with the base timer count source (fBT1).
		Chap. 18.	Added pin names for two-phase clock input. Accordingly, changed "P8_0" and "P8_1" to "TSUDA" and "TSUDB", respectively.
		Chap. 18.	Added legends where i, j, or k is used to indicate its value.
		Chap. 18.	Changed "single-waveform" to "single-phase waveform".
		345, 346	Figure 18.1 IC/OC Block Diagram (1/2) and Figure 18.2 IC/OC Block Diagram (2/2): Added details.
		347	Table 18.2 I/O Pins: <ul style="list-style-type: none"> <li>• Added pins TSUDA, TSUDB, and <math>\overline{INT1}</math>.</li> <li>• Added note 1 and note 2.</li> </ul>
		351	18.2.2 Waveform Generation Register j (G1POj) (j = 0 to 7): <ul style="list-style-type: none"> <li>• Specified the internal buffer as the place to reflect the value written to the G1POj register.</li> <li>• Added details.</li> </ul>
		352	18.2.3 Waveform Generation Control Register j (G1POCRj) (j = 0 to 7): <ul style="list-style-type: none"> <li>• Changed the explanation of bits MOD1 and MOD0.</li> <li>• Changed "internal counter" to "buffer" in the sentence starting with "When writing a value to the G1POj register..." in the RLD explanation.</li> </ul>
		354	18.2.4 Time Measurement Control Register j (G1TMCRj) (j = 0 to 7): <ul style="list-style-type: none"> <li>• Added some descriptions to the Function columns of bits DFS1 and DFS0, and the GOC bit.</li> <li>• Changed the register explanation.</li> <li>• Added explanations to bits DFS1 and DFS0, and the GSC bit.</li> </ul>
		356	18.2.5 Base Timer Register (G1BT): <ul style="list-style-type: none"> <li>• Changed the Function column in the register diagram.</li> <li>• Changed the explanation since the write operation to this register is disabled.</li> <li>• Added "the state is released" to the explanation for when the BTS bit is set to 1.</li> </ul>
		357	18.2.6 Base Timer Control Register 0 (G1BCR0): <ul style="list-style-type: none"> <li>• Rewrote the first and second paragraphs in the explanation for bits BCK1 and BCK0.</li> <li>• Added the IT bit explanation.</li> </ul>
358	18.2.7 Base Timer Control Register 1 (G1BCR1); Changed the following in the RST1 bit explanation: <ul style="list-style-type: none"> <li>• Added "while the RST1 bit is 1" to the first sentence in the second paragraph.</li> <li>• Changed the reference target.</li> <li>• Deleted the explanation regarding the G1POj register and moved it to 18.2.2.</li> </ul>		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	359	18.2.8 Time Measurement Prescaler Register j (G1TPRj) (j = 6 and 7): Added the Set Value column.
		362	18.2.13 Waveform Output Master Enable Register (G1OER): Changed "set the EOCj bit to 0" to "set the EOCj bit to 1" in line 4 of the register explanation.
		365	18.2.16 Interrupt Request Register (G1IR): Changed the register explanation.
		368	Table 18.5 Base Timer Specifications: <ul style="list-style-type: none"> <li>• Added a condition regarding the BTS bit to the Base timer reset conditions.</li> <li>• Deleted "while the base timer is counting" from "Base timer reset value while the base timer is counting".</li> <li>• Deleted the Write to base timer row.</li> <li>• Deleted the Selectable functions row and moved the contents to 18.3.1.2 and 18.3.1.3.</li> </ul>
		369	Figure 18.3 Base Timer Block Diagram: <ul style="list-style-type: none"> <li>• Added registers G1DV and G1BT.</li> <li>• Added detailed description of two-phase pulse clock.</li> </ul>
		369	Table 18.6 Base Timer Associated Register Settings: Added details.
		370, 371, 372	18.3.1.1 Increment, 18.3.1.2 Increment/Decrement and 18.3.1.3 Two-Phase Pulse Signal Processing: <ul style="list-style-type: none"> <li>• Added titles and explanations.</li> <li>• Changed descriptions of interrupt requests in figures for each operation.</li> </ul>
		373	Figure 18.7 Two-Phase Pulse Signal Processing (When Using the Base Timer Reset): <ul style="list-style-type: none"> <li>• Deleted the values to indicate timings, and moved the information to the Electrical Characteristics chapter.</li> <li>• Added a condition for the G1DV register.</li> </ul>
		374	18.3.1.4 Base Timer Reset While the Base Timer is Counting: Modified the register name from "G1BCR0" to "G1PO0" in the parenthesis of the second bullet.
		374	Figure 18.8 Base Timer Reset with the G1BTRR Register: <ul style="list-style-type: none"> <li>• Deleted the description of the base timer overflow request.</li> <li>• Added a condition.</li> </ul>
		374	Figure 18.9 Base Timer Reset with the G1PO0 Register: <ul style="list-style-type: none"> <li>• Corrected "G1IR0 register" typo to "G1IR0 bit in the G1IR register".</li> <li>• Changed "base timer interrupt" and "channel 0 interrupt" to "IC/OC base timer interrupt request" and "IC/OC channel 0 interrupt request", respectively.</li> <li>• Added a condition.</li> </ul>
		375	Figure 18.10 Base Timer Reset with INT1 Pin Input: <ul style="list-style-type: none"> <li>• Deleted the description of P8_3.</li> <li>• Changed note 2.</li> <li>• Added a condition.</li> </ul>
		376, 380	18.3.2 Time Measurement Function and 18.3.3 Waveform Generation Function: <ul style="list-style-type: none"> <li>• Moved under 18.3 Operations.</li> <li>• Changed line 1.</li> </ul>
		376	Table 18.10 Time Measurement Function Specifications: <ul style="list-style-type: none"> <li>• Changed the Interrupt request to the Interrupt request occurrence timing in the Item column.</li> <li>• Changed the Specification column of the Interrupt request occurrence timing row.</li> <li>• The explanations for the Gate function and Digital debounce filter in the Selectable functions are simplified.</li> </ul>
		377	Table 18.11 Time Measurement Function Associated Registers: <ul style="list-style-type: none"> <li>• Changed.</li> <li>• Added settings when the gate function is used.</li> </ul>
		377	Figure 18.11 Time Measurement Function (1/2): <ul style="list-style-type: none"> <li>• Modified "at falling edge" to "at rising edge" in the first bullet.</li> <li>• Deleted the description for when the base timer and the G1PO0 register match.</li> </ul>
		378	Figure 18.12 Time Measurement Function (2/2): <ul style="list-style-type: none"> <li>• Added "However, values in the G1TMj register change." to note 1 in (2).</li> <li>• Modified timings.</li> </ul>
		379	Figure 18.13 Prescaler and Gate Functions: Modified the timing of the G1IR bit.
		380	18.3.2.1 Gate Function (Channel 6 and 7): Added
		381	Table 18.12 Single-Phase Waveform Output Mode Specifications: <ul style="list-style-type: none"> <li>• Changed the range of values for m and n.</li> <li>• Changed the Interrupt request to the Interrupt request occurrence timing in the Item column.</li> <li>• Added "or I/O port" to the Specification of the OUTC1_j pin.</li> <li>• Simplified the explanation for the Compare match output in the Selectable functions</li> </ul>
382	Table 18.13 Registers and Settings in Single-Phase Waveform Output Mode: Added.		



REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description			
		Page	Summary		
1.10	Sep. 01, 2011	383	Figure 18.14 Single-Phase Waveform Output Mode Operation (1/2): Changed "fBT" to "fBT1" in (1).		
		384	Figure 18.15 Single-Phase Waveform Output Mode Operation (2/2): <ul style="list-style-type: none"> <li>• Added "when bits IOj1 and IOj0 are 10b" to the description "Output high by compare match".</li> <li>• Added a condition regarding the EOCj bit in the G1OER register.</li> </ul>		
		385	18.3.3.2 Inverted Waveform Output Mode: Rewrote the explanation for when the inverted waveform output mode is set.		
		385	Table 18.14 Inverted Waveform Output Mode Specifications: <ul style="list-style-type: none"> <li>• Changed the range of values for m and n.</li> <li>• Changed the Interrupt request to the Interrupt request occurrence timing in the Item column.</li> <li>• Added "or I/O port" to the Specification of the OUTC1_j pin.</li> </ul>		
		386	Table 18.15 Registers and Settings in Inverted Waveform Output Mode: Added.		
		388	Figure 18.17 Inverted Waveform Output Mode Operation (2/2): <ul style="list-style-type: none"> <li>• Added "when bits IOj1 and IOj0 are 10b" to the description "Output high by compare match".</li> </ul>		
		389	18.3.3.3 Set/Reset Waveform Output Mode (SR Waveform Output Mode): <ul style="list-style-type: none"> <li>• Changed "G1POCRi register (i = 0 to 7)" to "G1POCRj register (j = 0, 2, 4, 6)" in line 1.</li> <li>• Added "and G1POCRk" to line 4.</li> </ul>		
		389	Table 18.16 SR Waveform Output Mode Specifications: <ul style="list-style-type: none"> <li>• Changed the range of values for m, n and p.</li> <li>• Changed the Interrupt request to the Interrupt request occurrence timing in the Item column.</li> <li>• Added "or I/O port" to the Specification of the OUTC1_j pin.</li> <li>• Rewrote the description of the Output disabled in the Specifications column of the Selectable functions row.</li> </ul>		
		390	Table 18.17 Registers and Settings in SR Waveform Output Mode: Added.		
		392	18.3.4 "I/O Port Select Function": Rewrote the contents of "18.6.1 INPC1_7 Alternate Input Pin" and "18.6.2 P1_7/INPC1_7 Digital Debounce Function", and moved here.		
		392	Table 18.18 Pin Settings for Time Measurement and Waveform Generation: Simplified.		
		393	18.4 Interrupts: Changed.		
		395	18.5.1 Register Access: Added.		
		395	18.5.2 Changing the G1IR Register: Changed the title from "G1IR Register", and changed the explanation.		
		396	Figure 18.20 IC/OC Interrupt 0 Operation Example: Changed from "IC/OC Interrupt 0 and 1 Operation".		
		397	18.5.3 Changing Registers ICOCiC (i = 0, 1): Changed from "Registers ICOCiC and ICOCHjC".		
		397	18.5.4 Output Waveform During the Base Timer Reset with the BTS bit and 18.5.5 OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register: Changed from "Waveform Generation Function".		
		397	18.5.6 Interrupt Request When Selecting Time Measurement Function: Added.		
		<b>Real-Time Clock</b>			
		Chap. 20.		Changed "compare x mode" to "compare mode x".	
		404	Table 20.1 Real-Time Clock Specifications: Changed "timer stops" to "count stopped" in the Specification column of the Write to timer row.		
		<b>Serial Interface UARTi</b>			
		Chap. 21.		Changed the configuration. The orders of tables or sections possibly changed, accordingly.	
		Chap. 21.		21.3.3.6 SDA Output Control to 21.3.3.10 Initialization of Transmission/Reception: Revised.	
		Chap. 21.		21.8.2 Clock Asynchronous Serial I/O Mode (UART Mode): Deleted.	
		Chap. 21.		Changed terminologies in this chapter are as follows: <ul style="list-style-type: none"> <li>• "transfer clock" to "transmit/receive clock"</li> <li>• "transfer data length" to "character length"</li> <li>• "transfer data format" to "bit order"</li> </ul>	
		431	21.1 Introduction: Changed the layout of the introduction, including tables.		
		433	Figure 21.2 UARTi Transmit/Receive Unit Block Diagram: <ul style="list-style-type: none"> <li>• Unified data buses for low/high-order bits with a single data bus.</li> <li>• Deleted CKDIR from the explanation about bits.</li> </ul>		
		437	21.2.3 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 to 4): Added an explanation to bits SMD2 to SMD0 for when the bits are set to 000b.		
		438	21.2.4 UARTi Bit Rate Register (UiBRG) (i = 0 to 4): Changed the Setting Range.		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	438	21.2.5 UARTi Transmit Buffer Register (UiTB) (i = 0 to 4): Added "or I <sup>2</sup> C mode" after "When character length is 9 bits long...".
		439	21.2.6 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 4): <ul style="list-style-type: none"> <li>• Deleted the CRS bit explanation.</li> <li>• Changed the first and second paragraphs in the NCH bit explanation.</li> </ul>
		444	21.2.9 UART2 Special Mode Register 4 (U2SMR4): <ul style="list-style-type: none"> <li>• Changed the Function column of bits STSPSEL, ACKC, SCLHI, and SWC9.</li> <li>• Changed the bit names of bits SCLHI and SWC9.</li> <li>• Added an explanation regarding I<sup>2</sup>C master mode to the existing bit explanations of STAREQ, RSTAREQ, and STPREQ.</li> <li>• Added bit explanations for the other bits.</li> </ul>
		447	21.2.11 UART2 Special Mode Register 2 (U2SMR2): <ul style="list-style-type: none"> <li>• Changed the bit names of bits SWC, ALS, and STAC.</li> <li>• Changed the functions of bits other than b7.</li> </ul>
		450	21.3 Operations: Inserted the title.
		450	Table 21.5 Clock Synchronous Serial I/O Mode Specifications: Changed note 1 and note 2.
		459	Table 21.6 Pin Functions in Clock Synchronous Serial I/O Mode: <ul style="list-style-type: none"> <li>• Added the I/O column.</li> <li>• Changed "the port direction bit corresponding to xxx pin" to "the port direction bit sharing pin" in the Method of Selection column.</li> <li>• Added the Input, Input port row to the RXDi pin.</li> </ul>
		452	Table 21.7 Registers Used and Settings in Clock Synchronous Serial I/O Mode: <ul style="list-style-type: none"> <li>• Added UCLKSEL0 and PCLKR rows to the Register column.</li> <li>• Added b8 to UiTB.</li> <li>• Added b8, b11, and b13 to b15 to UiRB.</li> <li>• Added b4 to b6 to UiMR.</li> <li>• Deleted note 1.</li> </ul>
		455	21.3.1.3 Continuous Receive Mode: <ul style="list-style-type: none"> <li>• Added an explanation for when using an external clock.</li> <li>• Added Figure 21.6 Operation Example in Continuous Receive Mode.</li> </ul>
		457, 466	21.3.1.5 CTS/RTS Function, 21.3.2.5 CTS/RTS Function: Deleted the CRD and CRS bit explanation and added a reference to a table that includes similar information.
		457	21.3.1.6 Processing When Terminating Communication or When an Error Occurs: Moved the contents of "21.2.1 Transmit/Receive Register Initialization" here and rewrote the explanation.
		458	Table 21.8 UART Mode Specifications: Deleted note 2.
		459	Table 21.9 I/O Pin Functions in UART Mode: <ul style="list-style-type: none"> <li>• Added the I/O column.</li> <li>• Changed "the port direction bit corresponding to xxx pin" to "the port direction bit sharing pin" in the Method of Selection column.</li> <li>• Modified "RTS input" to "RTS output".</li> </ul>
		460	Table 21.10 Registers Used and Settings in UART Mode: <ul style="list-style-type: none"> <li>• Added the UCLDSEL0 and PCLKR rows.</li> <li>• Added b11 to UiRB.</li> <li>• Changed the order of notes, and changed note 4.</li> </ul>
		462	Figure 21.9 Receive Timing in UART Mode: Changed "UiBRG count source" to "Clock divided by UiBRG".
		466	21.3.2.6 Processing When Terminating Communication or When an Error Occurs: Moved the contents of "21.3.2 Transmit/Receive Circuit Initialization" here and rewrote the explanation.
		467	Table 21.12 I <sup>2</sup> C Mode Specifications: <ul style="list-style-type: none"> <li>• Changed the setting value of U2BRG register n from "00h to FFh" in the Transfer clock row.</li> <li>• Changed note 1 and note 2.</li> </ul>
468	Figure 21.14 Internal Clock Configuration: Added.		
468	Table 21.13 I/O Pin Functions in I <sup>2</sup> C Mode: Added note 1, and the previous note 1 became note 2.		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description			
		Page	Summary		
1.10	Sep. 01, 2011	469	Table 21.14 Registers Used and Settings in I <sup>2</sup> C Mode (1/2): <ul style="list-style-type: none"> <li>• Added UCLKSEL0 and PCLKR to the Register column.</li> <li>• Added "When receiving, set FFh." to b0 to b7 of U2TB in the Function column.</li> <li>• Added b8 to U2TB.</li> <li>• Added b13 to b15 to U2RB.</li> <li>• Added b4 to b6 to U2MR.</li> <li>• Deleted note 1.</li> </ul>		
		470	Table 21.15 Registers Used and Settings in I <sup>2</sup> C Mode (2/2): <ul style="list-style-type: none"> <li>• Changed the function of the SWC bit and CKPH bit.</li> <li>• Deleted the IFSR2A register.</li> </ul>		
		471	Table 21.16 I <sup>2</sup> C Mode Functions: <ul style="list-style-type: none"> <li>• Added an explanation above the table.</li> <li>• Rewrote all of the content.</li> </ul>		
		472	Figure 21.15 Transfer to U2RB Register and Interrupt Timing: Deleted "(1) IICM2 = 0 (ACK and NACK interrupts), CKPH = 0 (no clock delay)" and "(3) IICM2 = 1 (UART transmit/receive interrupt), CKPH = 0".		
		473	21.3.3.1 Detecting Start and Stop Conditions: Added the last paragraph.		
		473	Figure 21.16 Detecting Start and Stop Conditions: Revised.		
		474	Figure 21.17 STSPSEL Bit Functions: Revised.		
		475	Figure 21.18 Register Setting Procedures for Condition Generation: Added.		
		476	21.3.3.3 Arbitration: Rewritten.		
		476	21.3.3.4 SCL Control and Clock Synchronization: Added, including Figure 21.19 and Figure 21.20.		
		478	21.3.3.5 SCL Clock Frequency: Added, including Figure 21.21.		
		482	Table 21.18 Special Mode 2 Specifications: Changed "While transmission" to "For transmit interrupt", and "While receiving" to "For receive interrupt".		
		484	Table 21.20 Registers Used and Settings in Special Mode 2 <ul style="list-style-type: none"> <li>• Added UCLKSEL0 and PCLKR to the Register column.</li> <li>• Added b8 to U2TB.</li> <li>• Added b8, b11, and b13 to b15 to U2RB.</li> <li>• Added b4 to b6 to U2MR.</li> <li>• Deleted note 1.</li> </ul>		
		486	Table 21.21 Registers Used and Settings in IE Mode: Deleted the IFSR2A register.		
		488	Table 21.22 SIM Mode Specifications: Changed note 2.		
		490	Figure 21.30 Transmit/Receive Timing in SIM Mode: Added the timing when the IR bit in the S2TIC register becomes 1.		
		493-494	21.4 Interrupts, 21.4.1 Interrupt Related Registers and 21.4.2 Reception Interrupt: Added.		
		495	21.5.1 Common Notes on Multiple Modes: Added.		
		495, 496	21.5.2.2 Transmission and 21.5.2.3 Reception: Changed the style of the explanations about the external clock level into bulleted lists.		
		497-498	21.5.3.3 Setup and Hold Times When Generating a Start/Stop Condition to 21.5.3.6 Requirements to Start Transmission/Reception in Slave Mode: Added.		
		498	21.5.4 Special Mode 4 (SIM Mode): Changed the conditions to generate a transmit interrupt request.		
		<b>Multi-Master I<sup>2</sup>C-bus Interface</b>			
		Chap. 22.	Changed terminology "High-speed clock mode" to "Fast-mode".		
		505	22.2.3 I2C0 Control Register 0 (S1D0): Changed "P2_0/SDAMM pin and P2_1/SCLMM pin" to "SCLMM pin and SDAMM pin" in the TISS bit explanation.		
		516	22.2.8 I2C0 Status Register 0 (S10): Changed explanations for the following bits. <ul style="list-style-type: none"> <li>• LRB bit: Rewritten.</li> <li>• AL bit: Changed "master-slave mode" to "master receive mode" in the third and fourth bullets of the Conditions to become 1.</li> <li>• PIN bit: Deleted the description about the MSLAD bit from the second last bullet in the Conditions become 0.</li> <li>• PIN bit: Rewrote the conditions for the SCLMM pin not to output a low signal.</li> </ul>		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	523	22.3.1.2 Bit Rate and Duty Cycle: Added more details to the explanation of the relation between low/high period and bit rate.
		524	22.3.1.3 Receiving a Slave Address in Wait Mode and Stop Mode: Rewritten.
		535	Figure 22.15 Operation When Transmitted/Received a Slave Address or Data: Changed the description of bits TRX, ADR0, and AAS in parenthesis for when a slave address is received.
		536	Figure 22.16 Timeout Detection Timing: <ul style="list-style-type: none"> <li>• Deleted the bit descriptions in the SDAMM timing.</li> <li>• Deleted "Timeout detection enabled" in the SCLMM timing.</li> </ul>
		537	22.3.10 Data Transmit/Receive Examples: Changed the explanation in the last paragraph.
		541	22.3.10.5 Slave Transmission: Added an explanation for when arbitration lost is detected.
		545	22.5.2.4 S3D0 Register and 22.5.2.6 S10 Register: Added "Use the MOV instruction to write to this register." to the first bullet.
		<b>CAN Module</b>	
		550	23.1.1 CAN0 Control Register (C0CTLR): Changed note 2 and note 3.
		<b>A/D Converter</b>	
		Chap. 24.	Changed terminologies in this chapter are as follows: <ul style="list-style-type: none"> <li>• "precharge" to "charge"</li> <li>• "between execution processing time" to "inter-execution processing time"</li> </ul>
		Chap. 24.	24.7.2 $\phi$ AD Frequency: Deleted.
		617	Figure 24.1 A/D Converter Block Diagram: <ul style="list-style-type: none"> <li>• Unified upper data bus and lower data bus with a single data bus.</li> <li>• Changed "Initializing cycle 2 cycles of <math>\phi</math>AD" to "2 cycles of <math>\phi</math>AD".</li> </ul>
		620	24.2.2 A/D Register i (ADi) (i = 0 to 7): Added "Read the ADi register in 16-bit units." to the register explanation.
		621	24.2.3 A/D Control Register 2 (ADCON2): Changed "Frequency select bit" to "Frequency select bit 2" in the Bit Name column of the CKS2 bit.
		622	24.2.4 A/D Control Register 0 (ADCON0): <ul style="list-style-type: none"> <li>• Changed the Function column of bits CH2 to CH0.</li> <li>• Changed "ADCON2" to "ADCON0" in the register explanation.</li> </ul>
		624	24.2.5 A/D Control Register 1 (ADCON1), Changes made to the register diagram are as follows: <ul style="list-style-type: none"> <li>• Changed the reset value from "XX00 X000b".</li> <li>• Changed the Function column of SCAN1 and SCAN0.</li> <li>• Changed bits b7 to b6 from "No register bits" to "Reserved bit".</li> </ul>
		625	24.3.1 A/D Conversion Cycle: Changed the sentence that describes selecting multiple pins.
		627	24.3.2.2 External Trigger: <ul style="list-style-type: none"> <li>• Changed the explanation in the first paragraph.</li> <li>• Added "with <math>\overline{\text{ADTRG}}</math>" to the first bullet.</li> <li>• Added Figure 24.5 A/D Conversion Start Timing When External Trigger Input.</li> </ul>
		629	Figure 24.6 A/D Open-Circuit Detection Example on AVCC (Preconversion Charge), Figure 24.7 A/D Open-Circuit Detection Example on AVSS (Preconversion discharge): Added the switch right to the Analog input ANi.
		631, 633, 635, 637	Tables 24.8, 24.10, 24.12 and 24.14 for Registers and Settings: Replaced the register diagrams with tables.
		631, 633, 635, 637	Figures 24.8 to 24.11 for Operation Example in each mode: Changed the description regarding single A/D conversion.
		640	24.7.1 Analog Input Pin: Changed the description.
		640	24.7.2 Pin Configuration: Rewritten.
		640	24.7.3 Register Access: Changed "exclude bit 6" to "excluding the ADST bit" in line 4.
		641	24.7.9 $\phi$ AD: Added
		<b>Flash Memory</b>	
		Chap.26.	26.10.1 Functions to Prevent Flash Memory from Being Rewritten: Deleted.
		649	Table 26.2 Flash Memory Rewrite Modes Overview: Added "CPU operating mode" and "On-board rewrite" rows.
		652	26.3.1 Flash Memory Control Register 0 (FMR0): Added the description for the FMR22 bit to the FMSTP bit explanation.

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	661	26.7 User Boot Mode: Added.
		661	26.7.1 User Boot Function <ul style="list-style-type: none"> <li>• Changed “with the input of the selected port” to “with the input level of the selected port” in the first paragraph below Table 26.6.</li> <li>• Deleted “The content of the OFS1 address is valid.” from the third paragraph below Table 26.6.</li> </ul>
		663	Table 26.9 Addresses of Selectable Ports for Entry: Divided the Address column into columns “13FF9h” and “13FF8h”.
		663	Table 26.10 Example Settings of User Boot Code Area: Added.
		664	Figure 26.4 Program Starting Address in User Boot Mode: Added.
		665	Table 26.11 EW0 Mode and EW1 Mode: <ul style="list-style-type: none"> <li>• Changed the State during auto write and auto erase row.</li> <li>• Corrected “FRA0” typo to “FMR0” in the EW0 Mode column of the Flash memory status detection row.</li> <li>• Changed note 1.</li> </ul>
		666	26.8.1 EW0 Mode: <ul style="list-style-type: none"> <li>• Deleted “the flash memory is reset. The flash memory restarts after a certain period of time” from the third bullet below Figure 26.5.</li> <li>• Changed the last paragraph.</li> </ul>
		667	Table 26.12 Modes after Executing Commands (in EW0 Mode): Added.
		668-670	Figure 26.6 Program Flowchart in EW0 Mode (Suspend Function Enabled), Figure 26.7 Block Erase Flowchart in EW0 Mode (Suspend Function Enabled), Figure 26.8 Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled): <ul style="list-style-type: none"> <li>• Added “I flag ← 0”.</li> <li>• Moved “I flag ← 1”.</li> <li>• Deleted “Wait td(SR-SUS)”.</li> <li>• Changed “FMR33 = 1 ?” / “FMR32 = 1 ?” to “FMR00 = 1 ?” and its arrow direction.</li> </ul>
		672	26.8.2 EW1 Mode: <ul style="list-style-type: none"> <li>• Deleted “the flash memory is reset. The flash memory restarts after a certain period of time” from the third bullet below 26.10.</li> <li>• Changed the explanation regarding watchdog timer.</li> </ul>
		673	Table 26.13 Modes after Executing Commands (in EW1 Mode): Added.
		674-676	Figure 26.11 Program Flowchart in EW1 Mode (Suspend Function Enabled), Figure 26.12 Block Erase Flowchart in EW1 Mode (Suspend Function Enabled), Figure 26.13 Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled): <ul style="list-style-type: none"> <li>• Added “I flag ← 0”.</li> <li>• Moved “I flag ← 1”.</li> <li>• Changed “the highest-order block address” to “BA address”. (Figure 26.13 only)</li> </ul>
		681	Table 26.16 Software Commands: Added note 1.
		683, 684	26.8.6.4 Program Command, 26.8.6.5 Block Erase Command: Deleted the description regarding the read status register mode in EW0 mode.
		686	Figure 26.22 Read Lock Bit Status Command: Changed “FMR16 = 0?” (decision) to “Read the FMR16 bit” (process).
		687	Figure 26.23 Block Blank Check Command: Changed “FMR07 = 0?” (decision) to “Read the FMR07 bit” (process).
		687	26.8.6.8 Block Blank Check Command: Changed the explanation below Figure 26.23.
		689	Table 26.19 Errors and FMR0 Register States: Changed note 1.
		690	26.8.7.2 Handling Procedure for Errors: <ul style="list-style-type: none"> <li>• Changed (4) and the explanation below (4) in the Erase error.</li> <li>• Moved a part of the explanation of (2) to after (3) in the Program error.</li> </ul>
		693	26.9.2 Forced Erase Function: Added “the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled)” to the first paragraph.
693	26.9.3 Standard Serial I/O Mode Disable Function: Added “the ROMCR bit in the OFS1 address is 1 (ROMCP1 bit enabled)” to the second paragraph.		
694, 696	Table 26.22, Table 26.24 Pin Functions (Flash Memory Standard Serial I/O Mode 1, 2): Added the description to the Description column of the VREF row.		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description			
		Page	Summary		
1.10	Sep. 01, 2011	697	Figure 26.27 Circuit Application in Standard Serial I/O Mode 2: Moved P6_5/CLK1 to a lower position.		
		697	26.10 Parallel I/O Mode: Changed the title number from "29.9.6." to "26.10".		
		697	26.10.1 ROM Code Protect Function: Added the description for the ROMCR bit.		
		698	26.11.1 OFS1 Address, OFS2 Address, and ID Code Storage Address: Added.		
		699	26.11.3.2 CPU Rewrite Mode Select: Added the description for the FMR60 bit after the bullets.		
		699	26.11.3.7 DMA transfer: Added the description for EW0 mode.		
		700	26.11.3.10 Software Command: <ul style="list-style-type: none"> <li>• Changed (b) and (c).</li> <li>• Added the description for slow read mode to (e).</li> </ul>		
		700	26.11.3.12 Suspending the Auto-Erase and Auto-Program Operations: Added the details on reset to the first bullet.		
		701	26.11.4.1 User Boot Mode Program: Unified the contents of "Location of User Boot Mode Program" and "Entering User Boot Mode After Standard Serial I/O Mode" here, and changed the explanations.		
		<b>Electrical Characteristics</b>			
		Chap. 27.	Specified symbols for the following pins according to the change in Timer S. <ul style="list-style-type: none"> <li>• P8_0, P8_0 (A-phase) to TSUDA</li> <li>• P8_1, P8_1 (B-phase) to TSUDB</li> </ul>		
		<b>J version, Common to 3 V and 5 V</b>			
		702	Table 27.1 Absolute Maximum Ratings: Deleted VREF from the $V_I$ .		
		703	Table 27.2 Operating Conditions (1): <ul style="list-style-type: none"> <li>• Changed the maximum value of <math>I_{OH(sum)}</math> from "80".</li> <li>• Changed the maximum value of <math>I_{OL(sum)}</math> from "-80."</li> </ul>		
		709	Table 27.9 Voltage Detector 2 Electrical Characteristics: Added Vdet2_0 to Vdet2_3, and Vdet2_5 to Vdet2_7.		
		711	Table 27.12 On-Chip Oscillator Electrical Characteristics: Added the Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency.		
		<b>J-Version, <math>V_{CC} = 5 V</math></b>			
		712	Table 27.13 Electrical Characteristics (1): Changed the maximum value of $V_T+-V_T-$ , which includes TA0IN and others in Hysteresis, from "2.5".		
		720	Figure 27.14 Multi-master I <sup>2</sup> C-bus: Changed $t_{HD};DTA$ to $t_{HD};DAT$ and $t_{su};DTA$ to $t_{su};DAT$ .		
		<b>J-Version, <math>V_{CC} = 3 V</math></b>			
		721	Table 27.29 Electrical Characteristics (1): Changed the maximum value of $V_T+-V_T-$ , which includes TA0IN and others in Hysteresis, from "1.8".		
		729	Figure 27.23 Multi-master I <sup>2</sup> C-bus: Changed $t_{HD};DTA$ to $t_{HD};DAT$ and $t_{su};DTA$ to $t_{su};DAT$ .		
		<b>K-Version, Common to 3 V and 5 V</b>			
		730	Table 27.45 Absolute Maximum Ratings: <ul style="list-style-type: none"> <li>• Deleted VREF from the <math>V_I</math>.</li> <li>• Changed the value of Power consumption for <math>85^{\circ}C &lt; T_{opr} \leq 125^{\circ}C</math> from "200".</li> </ul>		
		731	Table 27.46 Operating Conditions (1): <ul style="list-style-type: none"> <li>• Changed the maximum value of <math>I_{OH(sum)}</math> from "80".</li> <li>• Changed the maximum value of <math>I_{OL(sum)}</math> from "-80".</li> </ul>		
		737	Table 27.53 Voltage Detector 2 Electrical Characteristics: Added Vdet2_0 to Vdet2_3, and Vdet2_5 to Vdet2_7.		
		739	Table 27.56 On-Chip Oscillator Electrical Characteristics: Added the Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency.		
		<b>K-Version, <math>V_{CC} = 5 V</math></b>			
		740	Table 27.57 Electrical Characteristics (1): Changed the maximum value of $V_T+-V_T-$ , which includes TA0IN and others in Hysteresis, from "2.5".		

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	748	Figure 27.37 Multi-master I <sup>2</sup> C-bus: Changed t <sub>HD</sub> ;DTA to t <sub>HD</sub> ;DAT and t <sub>SU</sub> ;DTA to t <sub>SU</sub> ;DAT.
		<b>K-Version, V<sub>CC</sub> = 3 V</b>	
		749	Table 27.73 Electrical Characteristics (1): Changed the maximum value of V <sub>T+</sub> -V <sub>T-</sub> , which includes TA0IN and others in Hysteresis, from "1.8".
		750	Table 27.74 Electrical Characteristics (2): • Changed the typical value of 125 kHz on-chip oscillator mode from "160". • Changed the typical value of low power mode from "450".
		757	Figure 27.46 Multi-master I <sup>2</sup> C-bus: Changed t <sub>HD</sub> ;DTA to t <sub>HD</sub> ;DAT and t <sub>SU</sub> ;DTA to t <sub>SU</sub> ;DAT.
		<b>Usage Notes</b>	
		Chap. 28.	28.1 OFS1 Address and ID Code Storage: Deleted since same description is in the Flash chapter.
		Chap. 28.	28.21.2 φAD Frequency: Deleted.
		Chap. 28.	28.22.1 Functions to Prevent Flash Memory from Being Rewritten: Deleted.
		760	Table 28.2 Read-Modify-Write Instructions: Added.
		762	Figure 28.2 SVCC Timing: Revised.
		766	28.5.5 PLL Frequency Synthesizer: Changed "...to meet the power supply ripple standard" to "...within the acceptable range of power supply ripple".
		767	28.6.1 CPU Clock: Added line 2.
		767	28.6.2 Wait Mode: • Added lines 4 and 5 to the first bullet. • Deleted second bullet in the previous version and added the second to fifth bullets.
		767	28.6.3 Stop Mode: • Added the last sentence to the third bullet. • Deleted fifth bullet in the previous version and added fourth to ninth bullets.
		768	28.6.4 Low Current Consumption Read Mode: Added the third bullet.
		768	28.6.5 Slow Read Mode: Added.
		769	28.7.2 Influence of $\overline{SD}$ : • Changed the title from "Effect of $\overline{SD}$ Pin". • Changed the explanation.
		776	28.11 Notes on Timer A: Rewritten by common items, and each mode.
		780	28.12 Notes on Timer B: Rewritten by common items, and each mode.
		782	28.13.2 Influence of $\overline{SD}$ : Changed the title from "Forced Cutoff Input" and changed the explanation.
		783	28.14.1 Register Access: Added.
		783	28.14.2 Changing the G1IR Register: Changed the title from "G1IR Register", and changed the explanation.
		784	Figure 28.9 IC/OC Interrupt 0 Operation Example: Changed from "IC/OC Interrupt 0 and 1 Operation".
		785	28.14.3 Changing Registers ICOCiIC (i = 0, 1): Changed from "Changing Registers ICOCiIC and ICOCHjIC".
		785	28.14.4 Output Waveform During the Base Timer Reset with the BTS bit and 28.14.5 OUTC1_0 Pin Output During the Base Timer Reset with the G1PO0 register: Changed from "Waveform Generation Function".
		785	28.14.6 Interrupt Request When Selecting Time Measurement Function: Added.
		789	28.17.1 Common Notes on Multiple Modes: Added.
		789, 790	28.17.2.2 Transmission and 28.17.2.3 Reception: Changed the style of the explanations about the external clock level into bulleted lists.
		791-792	28.17.3.3 Setup and Hold Times When Generating a Start/Stop Condition to 28.17.3.6 Requirements to Start Transmission/Reception in Slave Mode: Added.
		792	28.17.4 Special Mode 4 (SIM Mode): Changed the conditions to generate a transmit interrupt request.

REVISION HISTORY	M16C/5L, M16C/56 Group User's Manual: Hardware
------------------	--

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 01, 2011	793	28.18.2.4 S3D0 Register and 28.18.2.6 S10 Register: Added "Use the MOV instruction to write to this register." to the first bullet.
		795	28.20.1 Analog Input Pin: Changed the description.
		795	28.20.2 Pin Configuration: Rewritten.
		795	28.20.3 Register Access: Changed "exclude bit 6" to "excluding the ADST bit" in line 4.
		796	28.20.9 $\phi$ AD: Added
		797	28.21.1 OFS1 Address, OFS2 Address, and ID Code Storage Address: Added.
		798	28.21.3.2 CPU Rewrite Mode Select: Added the description for the FMR60 bit after the bullets.
		798	28.21.3.7 DMA transfer: Added the description for EW0 mode.
		799	28.21.3.10 Software Command: <ul style="list-style-type: none"> <li>• Changed (b) and (c).</li> <li>• Added the description for slow read mode to (e).</li> </ul>
		799	28.21.3.12 Suspending the Auto-Erase and Auto-Program Operations: Added reset details to the first bullet.
		800	28.21.4.1 User Boot Mode Program: <ul style="list-style-type: none"> <li>• Unified "Location of User Boot Mode Program" and "Entering User Boot Mode After Standard Serial I/O Mode" and changed explanations.</li> </ul>

Refer to 2. "Items revised or added in previous versions" for the items revised or added in previous versions.



## 2. Items revised or added in previous versions

REVISION HISTORY		M16C/5L Group, M16C/56 Group Hardware Manual	
Rev.	Date	Page	Revision History
0.61	Jul. 31, 2009	—	Initial release
0.70	Oct. 09, 2009		<p><b>The manual in general</b></p> <p>— Description for M16C/56 Group added</p> <p>— 03A2h “Open-Circuit Detection Assist Function Register” reset value modified</p> <p>— 0075h register name “CAN0 Successful Receive Interrupt Control Register” changed to “CAN0 Receive Completion Interrupt Control Register”</p> <p>— 0076h register name “CAN0 Successful Transmit Interrupt Control Register” changed to “CAN0 Transmit Completion Interrupt Control Register”</p> <p><b>SFR Quick Reference</b></p> <p>B-3 0140h to 0147h “Register 0 to 3” modified</p> <p>B-4 0152h “A/D1 Trigger Control Register” modified</p> <p>B-4 0154h, 0156h, and 0157h “A/D1 Control Register 2, 0, and 1” modified</p> <p><b>Overview</b></p> <p>4 Table 1.3 “Specifications (64-pin Package) (1/2)” partially modified</p> <p>10, 13 Figure 1.5 “Pin Assignment for 80-Pin Package (Top View)” and Figure 1.6 “Pin Assignment for 64-Pin Package (Top View)” partially modified</p> <p>10 1.5 “Pin Assignments” partially modified</p> <p><b>Special Function Registers (SFRs)</b></p> <p>23 Table 4.1 SFR List (1) reset value for VCR1 modified</p> <p>35 Table 4.13 SFR List (13) reset value for FMR0 modified</p> <p>38 Table 4.16 SFR List (16) reset values for S1D0 and S4D0 modified</p> <p>45-57 Table 4.23 SFR List (23) to Table 4.35 SFR List (35) reset values modified</p> <p>60 Table 4.38 SFR List (38) reset values for C0BCR, C0MSMR, C0TSR, and C0AFSR modified</p> <p><b>Resets</b></p> <p>72 Figure 6.3 “Reset Sequence” partially modified</p> <p><b>Voltage Detector</b></p> <p>79 Table 7.2 “Register List” reset value for VCR1 modified</p> <p>79 Table 7.2 “Register List” notes 4 and 5 added</p> <p>80 7.2.1 “Voltage Detection 2 Circuit Flag Register (VCR1)” reset value modified</p> <p>85 7.2.6 “Voltage Monitor 2 Circuit Control Register (VW2C)” description “(excluding the VW2C3 bit)” added</p> <p>90 Table 7.5 “Steps to Set Voltage Monitor 0 Reset Related Bits” partially modified</p> <p>90 Figure 7.4 “Voltage Monitor 0 Reset Operation Example” description “Oscillation stop detection interrupt signal” modified to “Oscillation stop/restart detection interrupt signal”</p> <p>92 Table 7.6 “Steps to Set Voltage Monitor 2 Interrupt/Reset Related Bits” Step 4 added</p> <p><b>Clock Generator</b></p> <p>104 “CM14 (125 kHz On-Chip Oscillator Stop Bit) (b4)” partially modified</p> <p>106 “CM22 (Oscillation stop/restart detect flag) (b2)” partially modified</p> <p>114 8.3.3 “fOCO40M” description “td(OCOF)” changed to “tsu (fOCO40M)”</p> <p>115 8.3.5 “125-kHz On-Chip Oscillator Clock (fOCO-S)” partially modified; “tosc(OCOF)” changed to “tsu (fOCO-S)”</p> <p>116 8.3.6 “Sub Clock (fC)” partially modified</p> <p>116 Figure 8.4 “Sub Clock Circuit Connection” modified</p> <p>117 8.4.2 “Peripheral Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC)” some description added</p> <p>121 8.7.2 “When the CM27 Bit is 1 (Oscillation Stop/Re-oscillation Detect Interrupt)” partially deleted</p> <p>121 Table 8.7 “After Main Clock Oscillation Stop/Re-Oscillation Detection When the CM27 Bit is 1” description for bits CM14, CM21, CM22, and CM23 added</p> <p>122 8.7.3 “Using the Oscillation Stop/Re-Oscillation Detect Function” partially modified</p> <p><b>Power Control</b></p> <p>131 9.3 “Clocks” and 9.3.1 “Normal Operating Mode” partially modified</p> <p>131-132 9.3.1.1 “High-Speed Mode and Medium-Speed Mode” to 9.3.1.7 “Low Power Mode” modified</p> <p>133 Table 9.2 “Clocks in Normal Operating Mode” note 4 modified</p> <p>141 9.3.3.4 “Exiting Wait Mode” partially modified</p>

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
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Rev.	Date	Page	Revision History		
0.70	Oct. 09, 2009	141	Table 9.7 "Resets and Interrupts to Exit Wait Mode and Usage Conditions" partially modified		
		144	Table 9.9 "Resets and Interrupts to Exit Stop Mode and Usage Conditions" partially modified		
		146	Figure 9.2 "Setting Procedures to Stop and Restart the Flash Memory" partially modified		
		150	9.7.2 "Wait Mode" partially modified		
		<b>Processor Mode</b>			
		153	Table 10.2 "Register List" partially modified		
		155	Processor Mode Register 2 (PM2) deleted		
		155	10.2.3 "Flash Memory Control Register 1 (FMR1)" note deleted		
		155	"FMR17 (Data Flash Wait Bit) (b7)" modified		
		156	Table 10.3 "Software Wait Related Bits and Bus Cycles" partially modified		
		<b>Programmable I/O Ports</b>			
		169-170	11.3.7 "Input Threshold Select Register 0 (VLT0)" to 11.3.9 "Input Threshold Select Register 2 (VLT2)" register name "Input Thershold Control Register" changed to "Input Thershold Select Register"		
		171	11.3.10 "Pin Assignment Control Register (PACR)" note deleted		
		172	11.3.11 "Port Pi Registers (Pi) (i = 0 to 10)" partially modified		
		<b>Interrupts</b>			
		184	Table 12.5 "Register List (3)" 02F0h, 02F1h, and 02F2h deleted		
		185	"PM24 (NMI Interrupt Enable Bit) (b4)" partially modified		
		193	Port Control Register (PCR) deleted		
		193	12.2.11 "P1_7 Digital Debounce Register (P17DDR)" added		
		197	Table 12.6 "Fixed Vector Tables" partially modified		
		198-199	Table 12.7 "Relocatable Vector Tables (1/2)" and Table 12.8 "Relocatable Vector Tables (2/2)" "INT instruction interrupt" moved		
		209	12.9 "NMI Interrupt" partially modified		
		210	12.10 "Key Input Interrupt" and Figure 12.10 "Key Input Interrupt" partially modified		
		213	12.13.3 "NMI Interrupt" some description added		
		215	12.13.5 "Rewriting the Interrupt Control Register" partially modified		
		215	12.13.6 "Instruction to Rewrite the Interrupt Control Register" added		
		<b>Watchdog Timer</b>			
		220	13.2.1 "Voltage Monitor 2 Circuit Control Register (VW2C)" description "(excluding the VW2C3 bit)" added		
		222	13.2.1 "Voltage Monitor 2 Circuit Control Register (VW2C)" partially modified		
		<b>DMAC</b>			
		243	Table 14.8 "DMAC Transfer Cycles" description for DMBIT added		
		<b>Timer A</b>			
		267	15.3.1.3 "Count Source" partially modified		
		269	Table 15.7 "Registers and the Setting in Timer Mode (1)" bit for TAI1 and TAI modified		
		273	Table 15.9 "Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal) (1)" bit for TAI1 and TAI modified		
		275	Figure 15.6 "Operation Example in Event Counter Mode" set value of the TAI register added		
		277	Table 15.11 "Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal) (1)" bit for TAI1 and TAI modified		
		280	15.3.4.3 "Counter Initialization by Two-Phase Pulse Signal Processing" modified		
		282	Table 15.13 "Registers and the Settings in One-Shot Timer Mode (1)" bit for TAI1 and TAI modified		
		286	Table 15.15 "Registers and Settings in Pulse Width Modulation Mode (1)" bit for TAI1 and TAI modified		
		291	Table 15.17 "Registers and Settings in Programmable Output Mode (1)" bit for TAI1 and TAI; register TAOW added		
		<b>Timer B</b>			
		306	16.2.5 "Pulse Period/Pulse Width Measurement Mode Function Select Register 1 (PPWFS1)" partially modified		

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
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Rev.	Date	Page	Revision History	
0.70	Oct. 09, 2009	307	16.2.5 "Pulse Period/Pulse Width Measurement Mode Function Select Register 1 (PPWFS1)" partially modified	
		312	16.3.1.3 "Count Source" partially modified	
		316	Table 16.8 "Registers and the Setting in Event Counter Mode (1)" bit for TBi1 and TBi modified	
		320	Table 16.10 "Registers and the Setting in Pulse Period/Pulse Width Measurement Modes (1)" bit for TBi1 and TBi modified	
		<b>Three-Phase Motor Control Timer</b>		
		368	17.5.2 "Forced Cutoff Input" partially modified	
		<b>Timer S</b>		
		394	Figure 18.4 "Increment/Decrement Mode" description for conditions added	
		414	Figure 18.17 "IC/OC Interrupt and DMA Request Generation" partially modified	
		<b>Task Monitor Timer</b>		
		421	19.2.3 "Task Monitor Timer Count Source Select Register (TMOSCS)" partially modified	
		<b>Real-Time Clock</b>		
		428-436	"timer stops" changed to "count stops"	
		428	20.2.1 "Real-Time Clock Second Data Register (RTCSEC)" partially modified	
		429	20.2.2 "Real-Time Clock Minute Data Register (RTCMIN)" partially modified	
		430	20.2.3 "Real-Time Clock Hour Data Register (RTCHR)" partially modified	
		431	20.2.4 "Real-Time Clock Day Data Register (RTCWK)" partially modified	
		432	20.2.5 "Real-Time Clock Control Register 1 (RTCCR1)" "2 cycles" changed to "three cycles"	
		436	20.2.7 "Real-Time Clock Count Source Select Register (RTCCSR)" partially modified	
		444	Figure 20.6 "Difference between Compare Modes" partially modified	
		446	Figure 20.8 "Compare 1 Mode Operating Example" partially modified	
		447	Figure 20.9 "Compare 2 Mode Operating Example" partially modified	
		450	20.5.1 "Starting and Stopping Count" partially modified	
		451	20.5.4 "Time Reading Procedure of Real-Time Clock Mode" partially modified	
		451	Figure 20.11 "Time Data Reading" added	
		<b>Serial Interface UARTi (i = 0 to 4)</b>		
		453	Figure 21.1 "UARTi Block Diagram" partially modified	
		454	Figure 21.2 "UARTi Transmit / Receive Unit" partially modified	
		455	Figure 21.3 "Registers U0TB to U4TB and U0RB to U4RB" partially modified	
		457	Figure 21.5 "Registers U0C0 to U4C0" partially modified	
		460	Figure 21.8 "Registers U2SMR2 and U2SMR3" partially modified	
		453	Figure 21.1 "UARTi Block Diagram" partially modified	
		464	Table 21.2 "Registers and Settings in Clock Synchronous Serial I/O Mode" note 3 added	
		467	21.1.1 "Transmit/Receive Register Initialization" title changed; description partially modified	
		467	Figure 21.13 "Transfer Clock Polarity" partially modified	
		471	Table 21.5 "Registers and Settings in UART Mode" note 4 added	
		474	21.2.1 "Bit Rate" partially modified	
		475	21.2.2 "Transmit/Receive Circuit Initialization" title changed; description partially modified	
		476	Figure 21.19 "Serial Data Logic Switching" partially modified	
		477	Figure 21.20 "TXD and RXD I/O Polarity Reverse" partially modified	
		480	Table 21.9 "Registers to Be Used and Settings in I <sup>2</sup> C Mode (1)" note 2 added	
		481	Table 21.10 "Registers Used and Settings in I <sup>2</sup> C Mode (2)" note 1 added	
		483	Figure 21.22 "Transfer to U2RB Register and Interrupt Timing" partially modified	
		488	Table 21.13 "Special Mode 2 Specifications" description for "Slave mode" deleted	
		489	Figure 21.25 "Serial Bus Communication Control Example in Special Mode 2" partially modified	
		489	Table 21.14 "Registers and Settings in Special Mode 2" note 2 added	
		492	Table 21.15 "Registers and Settings in IE Mode" note added	
		495	Table 21.17 "Registers and Settings in SIM Mode" note 2 added	
		499	21.7 "Notes on Serial Interface UARTi (i = 0 to 4)" partially modified	
		500	21.7.3 "Special Mode (I <sup>2</sup> C Mode)" modified: 21.7.3.1 "Generating Start and Stop Conditions" and 21.7.3.2 "IR Bit" added	

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
------------------	--

Rev.	Date	Page	Revision History		
0.70	Oct. 09, 2009	<b>Multi-Master I<sup>2</sup>C-bus Interface</b>			
		504	Table 22.4 "Register List" reset values for S1D0 and S4D0 modified		
		507	22.2.3 "I2C0 Control Register 0 (S1D0)" reset value modified		
		514	22.2.6 "I2C0 Control Register 1 (S3D0)" partially modified		
		519	22.2.7 "I2C0 Control Register 2 (S4D0)" partially modified		
		532	22.2.7 "I2C0 Control Register 2 (S4D0)" partially modified		
		<b>A/D Converter</b>		628	CKS0 (Frequency Select Bit 0) (b7) partially modified
		<b>Flash Memory</b>		663	26.3.2 "Flash Memory Control Register 1 (FMR1)" note deleted
				663	"FMR11 (Write to FMR6 register enable bit) (b1)" "low" changed to "high"
				666	"FMR60 (EW1 mode select bit) (b0)" "low" changed to "high"
				667	26.4 "Optional Function Select Area" partially modified
				678	26.8.4.4 "Program Command" partially modified
				679	26.8.4.5 "Block Erase Command" partially modified
				680	26.8.4.6 "Lock Bit Program Command" partially modified
				703	26.10.3.2 "CPU Rewrite Mode Select" "low" changed to "high"
		<b>Electrical Characteristics</b>		712, 735	Table 27.7 "Low Voltage Detection Circuit Electrical Characteristics" and Table 27.45 "Voltage Detection Circuit Electrical Characteristics" partially modified
				716	Table 27.17 "Timer A Input (External Trigger Input in Pulse Width Modulation Mode, Programmable Output Mode)" title changed
				717, 725	Table for "A/D Trigger Input" deleted
				724	Table 27.31 "Timer A Input (External Trigger Input in Pulse Width Modulation Mode, Programmable Output Mode)" title changed
				727, 742	Figure 27.8 "Timing Diagram (1)" and Figure 27.15 "Timing Diagram (1)" partially modified
				739	Table 27.55 "Timer A Input (External Trigger Input in Pulse Width Modulation Mode, Programmable Output Mode)" title changed
				740, 748	Table for "A/D Trigger Input" deleted
				747	Table 27.69 "Timer A Input (External Trigger Input in Pulse Width Modulation Mode, Programmable Output Mode)" title changed
		<b>Usage Notes</b>		761	28.7.2 "Wait Mode" partially modified
				764	28.9.3 "NMI Interrupt" partially modified
				766	28.9.5 "Rewriting the Interrupt Control Register" partially modified
				766	28.9.6 "Instruction to Rewrite the Interrupt Control Register" added
				783	28.17.1 "Starting and Stopping Count" partially modified
				784	28.17.4 "Time Reading Procedure of Real-Time Clock Mode" partially modified
				785	28.18 "Notes on Serial Interface UARTi (i= 0 to 4)" partially modified
				786	28.18.3 "Special Mode (I <sup>2</sup> C Mode)" modified: 28.18.3.1 "Generating Start and Stop Conditions" and 28.18.3.2 "IR Bit" added
				787	28.19.1 "Limitation on CPU Clock" partially modified
				791	28.22.3.2 "CPU Rewrite Mode Select" "low" changed to "high"
1.00	Jan. 31, 2010	<b>The manual in general</b>			
		—	0019h the register name changed to "Voltage Detector 2 Flag Register"		
		—	001Ah the register name changed to "Voltage Detector Operation Enable Register"		
		—	0028h the register name changed to "Voltage Detector 2 Level Select Register"		
		—	002Ah the register name changed to "Voltage Monitor 0 Control Register"		
		—	002Ch the register name changed to "Voltage Monitor 2 Control Register"		
		—	0366h "Port Control Register" the reset value changed		
		<b>Overview</b>		3, 5	Table 1.2 "Specifications (80-pin Package) (2/2)" and Table 1.4 "Specifications (64-pin Package) (2/2)" note 1 added
				6	1.3 "Product List" Table 1.5 and Table 1.6 the status of products updated; Typos in the part numbers of the M16C/56 Group corrected
				8, 9	Figure 1.3 "M16C/5L Group, M16C/56 Group 80-Pin Block Diagram" and Figure 1.4 "M16C/5L Group, M16C/56 Group 64-Pin Block Diagram" "Voltage detector", "Power-on reset", and "On-chip debugger" added

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
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Rev.	Date	Page	Revision History
1.00	Jan. 31, 2010	15	Table 1.10 "Pin Names, 64-Pin Package (2/2)" TB2IN moved from 63 pin to 64 pin
		16	Table 1.11 "Pin Functions (64-Pin and 80-Pin Packages)" "Three-phase motor control timer output" modified to "Three-phase motor control timer"; Note 1 added
		<b>Special Function Registers (SFRs)</b>	
		24	Table 4.2 SFR List (2) "the VW2C3 bit" in note 2 modified to "bits VW2C2 and VW2C3"
		57	Table 4.35 "Registers with Write-Only Bits" the order of registers changed; "CAN0 Receive FIFO Pointer Control Register" and "CAN0 Transmit FIFO pointer Control Register" added
		<b>Resets</b>	
		61	Figure 6.1 "Reset Circuit Block Diagram" illustration for the VD2LS register added
		<b>Voltage Detector</b>	
		74	Table 7.2 "Register List" notes 4 and 6 added; "the VW2C3 bit" in note 7 modified to "Bits VW2C2 and VW2C3"
		77	7.2.3 "Voltage Monitor Function Select Register (VWCE)" typo corrected from "PCR3" to "PRC3"
		78	7.2.4 "Voltage Detector 2 Level Select Register (VD2LS)" RW for b7 to b4 modified to RW; Function for VD2LS0 to VD2LS3 modified; typo corrected from "PCR3" to "PRC3"
		80	7.2.6 "Voltage Monitor 2 Control Register (VW2C)" "The VW2C3 bit" in the 4th line modified to "Bits VW2C2 and VW2C3"
		82	7.3 "Optional Function Select Area" description for "programmed products" added
		82	7.3.1 "Option Function Select Address 1 (OFS1)" three lines below the register diagram deleted
		82	"LVDAS (Voltage Detector 0 Start Bit) (b6)" added
		83	7.4.1 "Digital Filter" "next sampling timing" modified to "third sampling timing" in the sixth line
		<b>Clock Generator</b>	
		90	8.1 "Introduction" description for the fifth bullet deleted
		91, 92	Table 8.1 "Clock Generator Specifications" and Figure 8.1 "System Clock Generator" description for "Dedicated 125-kHz on-chip oscillator for watchdog timer" deleted (moved to 13. "Watchdog Timer")
		95	"CM01-CM00 (Clock Output Function Select Bit) (b1-b0)" "the CM01 and CM00 bit settings enabled" in the second line modified to "selected by the CM01 and CM00 bit"
		96	"CM06 (Main Clock Division Select Bit) (b6)" description of the second bullet deleted
		98	"CM15 (XIN-XOUT Drive Level Select Bit) (b5)" description modified
		101	8.2.5 "Peripheral Clock Select Register (PCLKR)" Bit Name for PCLK0 corrected
		103	8.2.7 "Processor Mode Register 2 (PM2)" description of "Once the PM21 bit is set to 1, it cannot be set to 0 by a program (writing a 0 has no effect)." added
		109	8.3.5 "125-kHz On-Chip Oscillator Clock (fOCO-S)" typo in the description for "To stop fOCO-S oscillation" corrected from "CM14 bit becomes 1 (125 kHz on-chip oscillator oscillates)" to "CM14 bit becomes 0 (125 kHz on-chip oscillator oscillates)"
		<b>Power Control</b>	
		122	"FMR01 (CPU Rewrite Mode Select Bit) (b1)" "FMSTP (Flash Memory Stop Bit) (b3)" "located in an area other than the flash memory" modified to "in the RAM"
		124	"FMR23 (Low-Current Consumption Read Mode Enable Bit) (b3)" the second paragraph modified
		133	Table 9.7 "Resets and Interrupts to Exit Wait Mode and Usage Conditions" usage conditions for "Multi-master I <sup>2</sup> C bus" and "Voltage monitor 0 reset" modified
		138	9.4 "Stopping Flash Memory" "an area other than the flash memory" modified to "the RAM"
		<b>Processor Mode</b>	
		148	10.3 "Software Wait" note 1 deleted (moved to 27.1.4 and 27.4.4 "Flash Memory Electrical Characteristics")
		<b>Programmable I/O Ports</b>	
		150	11.2 "I/O Ports and Pins" diagrams for I/O ports revised; Table 11.3 "I/O Ports (Basic)" to Table 11.8 "I/O Ports (XC)" added
		162-163	11.3.7 to 11.3.9 "Input Threshold Select Register 0/1/2" description for the input level added
		169	11.4.2 "Priority Level of Peripheral Function I/O" added
		<b>Interrupts</b>	
		179, 180	"IR (Interrupt Request Bit) (b3)" description modified to "Do not write 1 when the IR bit is 0"
		183	12.2.6 "Interrupt Source Select Register (IFSR)" function for IFSR6 and IFSR7 modified
		206	12.13.2 "SP Setting" the second paragraph added

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
------------------	--

Rev.	Date	Page	Revision History		
1.00	Jan. 31, 2010	<b>Watchdog Timer</b>			
		210	Table 13.1 "Watchdog Timer Specification" "Dedicated 125-kHz on-chip oscillator for watchdog timer" added to fWDT		
		211	Figure 13.1 "Watchdog Timer Block Diagram" "Dedicated 125-kHz on-chip oscillator for watchdog timer" added; Typos corrected from "WDTc" to "WDC"		
		217	"WDTUFS1 to WDTUFS0 (Watchdog Timer Initial Set Bit) (b0-b1)" typo corrected from "CSPRO" to "CSPRO"		
		220	13.4.3 "Count Source Protect Mode Enabled" description added below Table 13.4		
		<b>DMAC</b>			
		231	Table 14.4 "DMA Request Sources for DMA1" "Both edges of INT1" moved to 00111b		
		232	Table 14.5 "DMA Request Sources for DMA2" "Both edges of INT2" moved to 00110b		
		233	14.3.2 "DMA Request" "interrupts" in the 12th line modified to "the interrupt control registers"		
		<b>Timer A</b>			
		243	Figure 15.2 "Timer A Configuration" "programmable output mode" deleted from Timer A0 and Timer A3		
		255	"TA0TGH and TA0TGL (Timer A0 Event/Trigger Select Bit) (b7-b6)" typo corrected from "TA0GH to TA0GL" to "TA0TGH to TA0TGL"		
		266	Table 15.9 "Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal) (1)" and Table 15.11 "Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal) (1)" setting for PCLKR, TCKDIVC0, TACS0 to TACS2, and ONSF (TAiTGH to TAiTGL) modified to "-" (setting unnecessary)"		
		<b>Timer B</b>			
		309	Table 16.8 "Registers and the Setting in Event Counter Mode (1)" setting for PCLKR, TCKDIVC0, and TBCS0 to TBCS1 modified to "-" (setting unnecessary)"		
		312	Table 16.9 "Specifications of Pulse Period/Pulse Width Measurement Modes" specification for "Write to timer" the second bullet deleted		
		<b>Timer S</b>			
		—	"phase-delayed waveform" modified to "inverted waveform"		
		—	Description of INT5 and IDU deleted		
		362	Table 18.1 "IC/OC Specifications" Specifications for Channel interrupts modified		
		368	"MOD1 and MOD0 (Operating Mode Select Bit) (b1-b0)" the second line modified		
		371	18.2.5 "Base Timer Register (G1BT)" description added to function		
		384	Table 18.5 "Base Timer Specifications" "while the base timer is counting" added to "Base timer reset value"; "and the BTS bit is 0" added to function for "Read from base timer" and "Write to base timer"		
		399	Table 18.14 "Inverted Waveform Output Mode Specifications" "single-waveform" "single-phase waveform" in specifications for "Selectable functions" modified to "inverted waveform"		
		402	Table 18.15 "SR Waveform Output Mode Specifications" "(n>m)" added to specifications for output waveform; "single-phase waveform" in specifications for selectable function modified to "SR waveform"; Note 1 deleted		
		<b>Serial Interface UARTi (i = 0 to 4)</b>			
		448-462	21.1 "Registers" description for registers revised; Table 21.1 "Registers (1/2)" added; Register diagrams revised		
		449	21.1.1 "Peripheral Clock Select Register (PCLKR)" added		
		479	Table 21.11 "I/O Pin Functions in I <sup>2</sup> C Mode" added		
		482	Table 21.14 "I <sup>2</sup> C Mode Functions" description for "Store received data" moved to "Read received data"		
		488	Table 21.16 "Special Mode 2 Specifications" note 1 deleted		
		489	Table 21.17 "I/O Pin Functions in Special Mode 2" added		
		491	21.5.1 "Clock Phase Setting Function" the sixth and seventh lines deleted		
		491	Diagrams for "Transmit and Receive Timing (CKPH = 0) in Slave Mode (External Clock)" and "Transmit and Receive Timing (CKPH = 1) in Slave Mode (External Clock)" deleted		
		499	21.8.1.3 "Reception" typo corrected from "the RE bit" to "the RI bit" in the third paragraph		
		<b>Multi-Master I<sup>2</sup>C-bus Interface</b>			
		501	Table 22.1 "Multi-Master I <sup>2</sup> C Interface Specifications" description for "Timeout detection" in selectable functions modified		
		502	Table 22.2 "Detections by I <sup>2</sup> C Interface" function for slave address match modified		
		507	"BC2 to BC0 (Bit counter) (b2 to b0)" description modified		
		515	"WIT (Data Receive Interrupt Enable Bit) (b1)" "slave address transmission/reception" in the 12th line modified to "slave address reception"		

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
------------------	--

Rev.	Date	Page	Revision History		
1.00	Jan. 31, 2010	522	Table 22.9 "Functions by Write Access to the S10 Register" "Selects communication mode" divided into four modes		
		524	"PIN (I2C-bus Interface Interrupt Request Bit) (b4)" description added to the third bullet in "Conditions to become 0"		
		528	Table 22.11 "CCR4 to CCR0 Bit Settings and Bit Rates (fVILC = 4 MHz)" "167" in high-speed clock mode and "16.7" in standard clock mode modified to "166" and "16.6" respectively		
		530	22.3.2 "Generation of Start Condition" description added to (2); "after the falling edge of the BB bit" in the 14th line modified to "after the BB bit changes from 1 to 0"		
		534	Figure 22.10 "Start Condition Overlap Protect Operation" the illustration for bits MST and TRX modified		
		534	22.3.5 "Start Condition Overlap Protect" "and the S00 register" added to the second line below Figure 22.10		
		536	22.3.6 "Arbitration Lost" description for (a) modified; The last paragraph added		
		542	22.3.9 "Timeout Detection" description for the last bullet deleted		
		544	22.3.10.2 "Master Transmission" "Check whether ACK presents" deleted from (B)		
		545	22.3.10.3 "Master Reception" "Check whether ACK presents" deleted from (B)		
		546	22.3.10.4 "Slave Reception" (2) deleted from (A); "1 (no ACK presents)" modified to "0 (ACK presents)" in (B); (2) added to (C)		
		544	22.3.10.5 "Slave Transmission" "Check whether ACK presents" deleted from (B)		
		549	Table 22.15 "I <sup>2</sup> C-bus Interrupt" "Completion of transmitting slave address" deleted from interrupt source		
		<b>A/D Converter</b>			
		622	Table 24.1 "A/D Converter Specifications" specification for "Integral nonlinearity error" modified		
		625	24.2 "Registers" description for the PCR register deleted		
		630	24.3.1 "A/D Conversion Cycle" "Divide fAD so φAD conforms the standard frequency." added; the second paragraph deleted		
		<b>CRC Calculator</b>			
		652	25.1 "Introduction" the last sentence deleted		
		652	Figure 25.1 "CRC Calculator Block Diagram" modified		
		653	25.2 "Registers" the order of register diagrams changed		
		<b>Flash Memory</b>			
		661	"FMR00 (RY/BY status flag) (b0)" two conditions added to "Conditions to become 0"		
		662	"FMR02 (Lock bit disable select bit) (b2)" the last sentence added		
		667	"FMR60 (EW1 mode select bit) (b0)" the last sentence added		
		673	26.8 "CPU Rewrite Mode" the third paragraph for the suspend function added		
		673	Table 26.10 "EW0 Mode and EW1 Mode" "Mode after program or erase" modified to "Mode after program/erase, or during program/erase suspend"; "and bits FMR32 and FMR33 in the FMR3 register" added to the both modes for flash memory status detection		
		676	Figure 26.4 "Suspend Request" "suspend is requested" modified to "request a suspend"		
		683	Figure 26.12 "Block Blank Check Command" "command sequence error" detection added		
		683	26.8.4.8 "Block Blank Check Command" two paragraphs added below Figure 26.12		
		685	Table 26.16 "Errors and FMR0 Register States" "block blank check, or read lock bit status" added to error occurrence conditions for command sequence error		
		686	26.8.5.2 "Handling Procedure for Errors" the seventh line in "Erase error" added		
		688-690	Figure 26.15 "Program Flowchart in EW0 Mode (Suspend Function Enabled)" to Figure 26.17 "Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)" "Wait td(SR-SUS)" added		
		699	Table 26.18 "Forced Erase Function" "No ID match" added to function for "0 (ROM code protect enabled)"		
		702	26.9.5 "Standard Serial I/O Mode 2" "The main clock is used" added		
		702	Table 26.21 "Pin Functions (Flash Memory Standard Serial I/O Mode 2)" "when the main clock is used" deleted from description for XIN and XOUT		
		705	26.10.3.10 "Software Command" (e) added		
		<b>Electrical Characteristics</b>			
		706-761	This chapter revised		
		<b>J version, Common to 3 V and 5 V</b>			
		706	Table 27.1 "Absolute Maximum Ratings" "Analog reference voltage" added; Note 1 added		
707	Table 27.2 "Operating Conditions (1)" "High peak output current" and "Low peak output current" added				

REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
------------------	--

Rev.	Date	Page	Revision History		
1.00	Jan. 31, 2010	708	Table 27.3 "Recommended Operating Conditions (2/2) (1)" added; Figure 27.2 "Ripple Waveform" added		
		709	Table 27.4 "A/D Conversion Characteristics (1)" "A/D operating clock frequency" added; Note 3 added		
		710	Table 27.5 "CPU Clock When Operating Flash Memory ( $f_{BCLK}$ )" "(wait state)" in note 2 modified to "one wait"		
		711	Table 27.6 "Flash Memory (Program ROM 1, 2) Electrical Characteristics" conditions for read voltage added		
		713	Table for "Low Voltage Detection Circuit Electrical Characteristics" replaced by Table 27.8 "Voltage Detector 0 Electrical Characteristics" and Table 27.9 "Voltage Detector 2 Electrical Characteristics"		
		714	Figure 27.4 "Power-On Reset Circuit Electrical Characteristics" $t_{fth}$ modified		
		714	Table 27.11 "Power Supply Circuit Timing Characteristics" moved to below Figure 27.4; " $t_{d(E-A)}$ " deleted (moved to Table 27.8 and Table 27.9); Maximum value for $t_{d(W-S)}$ changed		
		715	Figure 27.5 "Power Supply Circuit Timing Diagram" "VC26" modified to "VC25"		
		715	Table 27.12 "On-chip Oscillator Oscillation Circuit Electrical Characteristics" conditions added below the table title; Minimum value and maximum value for $f_{OCO40M}$ changed		
		<b>J-Version, VCC = 5 V</b>			
		716	Table 27.13 "Electrical Characteristics (1)" Parameter for $V_{T+}$ - $V_{T-}$ modified: "SCL, SDA", and "TA2OUT" modified to "SCL2, SDA2", and "TA0OUT" respectively; "ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0" added		
		717	Table 27.14 "Electrical Characteristics (2)" "During flash memory program" and "During flash memory erase" added		
		718	27.2.2.1 "Reset Input (RESET Input)" added		
		718-723	Figure 27.7 "External Clock Input (XIN Input)" to Figure 27.13 "External Interrupt INTi Input" added (replaced Timing Diagram (1) and (2))		
		722	27.2.2.5 "Timer S Input" added		
		724	Figure 27.14 "Multi-master I <sup>2</sup> C-bus" the title changed		
		<b>J-Version, VCC = 3 V</b>			
		725	Table 27.29 "Electrical Characteristics (1)", Parameter for $V_{T+}$ - $V_{T-}$ modified: "SCL, SDA", and "TA2OUT" modified to "SCL2, SDA2", and "TA0OUT" respectively; "ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0" added		
		726	Table 27.30 "Electrical Characteristics (2)" "During flash memory program" and "During flash memory erase" added		
		727	27.3.2.1 "Reset Input (RESET Input)" added		
		727-732	Figure 27.16 "External Clock Input (XIN Input)" to Figure 27.22 "External Interrupt INTi Input" added (replaced Timing Diagram (1) and (2))		
		731	27.3.2.5 "Timer S Input" added		
		733	Figure 27.23 "Multi-master I <sup>2</sup> C-bus" the title changed		
		<b>K-Version, Common to 3 V and 5 V</b>			
		734	Table 27.45 "Absolute Maximum Ratings" "Analog reference voltage" added; Note 1 added		
		735	Table 27.46 "Operating Conditions (1)" "High peak output current" and "Low peak output current" added		
		736	Table 27.47 "Recommended Operating Conditions (2/2) (1)" added; Figure 27.25 "Ripple Waveform" added		
		737	Table 27.48 "A/D Conversion Characteristics (1)" "A/D operating clock frequency" added; Note 3 added		
		739	Table 27.50 "Flash Memory (Program ROM 1, 2) Electrical Characteristics" conditions for read voltage added		
		741	Table for "Low Voltage Detection Circuit Electrical Characteristics" replaced by Table 27.52 "Voltage Detector 0 Electrical Characteristics" and Table 27.53 "Voltage Detector 2 Electrical Characteristics"		
		742	Figure 27.27 "Power-On Reset Circuit Electrical Characteristics" $t_{fth}$ modified		
		742	Table 27.55 "Power Supply Circuit Timing Characteristics" moved to below Figure 27.25; " $t_{d(E-A)}$ " deleted; Maximum value for $t_{d(W-S)}$ changed		
		743	Figure 27.28 "Power Supply Circuit Timing Diagram" "VC26" modified to "VC25"		
		743	Table 27.56 "On-chip Oscillator Oscillation Circuit Electrical Characteristics" conditions added below the table title; Minimum value and maximum value for $f_{OCO40M}$ changed		



REVISION HISTORY	M16C/5L Group, M16C/56 Group Hardware Manual
------------------	--

Rev.	Date	Page	Revision History
1.00	Jan. 31, 2010	<b>K-Version, VCC = 5 V</b>	
		744	Table 27.57 "Electrical Characteristics (1)" Parameter for $V_{T+}$ , $V_{T-}$ modified: "SCL, SDA", and "TA2OUT" modified to "SCL2, SDA2", and "TA0OUT" respectively; "ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0" added
		745	Table 27.58 "Electrical Characteristics (2)" "During flash memory program" and "During flash memory erase" added
		746	27.5.2.1 "Reset Input (RESET Input)" added
		746-751	Figure 27.30 "External Clock Input (XIN Input)" to Figure 27.36 "External Interrupt INTi Input" added (replaced Timing Diagram (1) and (2))
		750	27.5.2.5 "Timer S Input" added
		752	Figure 27.37 "Multi-master I <sup>2</sup> C-bus" the title changed
		<b>K-Version, VCC = 3 V</b>	
		753	Table 27.73 "Electrical Characteristics (1)" Parameter for $V_{T+}$ , $V_{T-}$ modified: "SCL, SDA", and "TA2OUT" modified to "SCL2, SDA2", and "TA0OUT" respectively; "ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0" added
		754	Table 27.74 "Electrical Characteristics (2)" "During flash memory program" and "During flash memory erase" added
		755	27.6.2.1 "Reset Input (RESET Input)" added
		755-760	Figure 27.39 "External Clock Input (XIN Input)" to Figure 27.45 "External Interrupt INTi Input" added (replaced Timing Diagram (1) and (2))
		759	27.6.2.5 "Timer S Input" added
		761	Figure 27.46 "Multi-master I <sup>2</sup> C-bus" the title changed
		<b>Usage Notes</b>	
		762	28.1 "OFS1 Address, OFS2 Address, and ID Code Storage Address" "OFS2 address" added to the title and the ninth line; "set FFh to the OFS2 address", "org 0FFDBH", and "byte 0FFh" added to description for example
		764	Table 28.1 "Registers with Write-Only Bits" the order of registers changed; "CAN0 Receive FIFO Pointer Control Register" and "CAN0 Transmit FIFO pointer Control Register" added
		774	28.9.2 "SP Setting" the second paragraph added
		795	28.18.1.1 "Transmission/Reception" "(i = 0 to 3)" added to the second line
		795	28.18.1.3 "Reception" typo corrected from "the RE bit" to "the RI bit" in the third paragraph
		796	28.18.2.1 "Transmission/Reception" "(i = 0 to 3)" added to the second line
		797	28.19.2.6 "S10 Register" the third line modified
		802	28.22.3.10 "Software Command" the third line modified

Refer to 1. "Items revised or added in this version" for the items revised or added in this version.

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