



IDT™ 89EBPES64H16 / 89EBPES48H12 / 89EBPES48T12 Evaluation Board Manual

(Eval Board: 18-624-000)

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Description of the EB64H16 Eval Board

Notes

Foreword

This evaluation board manual includes hardware and software information on the 89HPES64H16, 89HPES48H12, and 89HPES48T12 peripheral chips. All three devices are members of IDT's PRECISE™ family of PCI Express® switching solutions.

The 89HPES64H16 (PES64H16) is a 64-lane, 16-port switch and the 89HPES48H12 (PES48H12) is a 48-lane, 12-port switch. Both devices are system interconnect switches that perform PCI Express packet switching with a feature set optimized for high-performance applications where multiple peer-to-peer traffic flows are simultaneously transmitted.

The 89HPES48T12 (PES48T12) is a 48-lane, 12-port peripheral chip that performs PCI Express Packet switching with a feature set optimized for high-performance applications such as servers, storage, and communications/networking.

The same evaluation board is used for all three of these devices and, consequently, the information in this manual applies equally, with some exceptions, to all three devices. Throughout the manual, numerous references are made to the 89BPES64H16 Evaluation Board (also referred to as EB64H16). These references to the EB64H16 should be interpreted as also applying to both an EB48H12 board and an EB48T12 board, except where noted.

Introduction

The EB64H16 evaluation board provides an evaluation platform for the PES64H16 switch. The EB64H16 has two x4 ports which can be merged to provide one x8 upstream port on a standard x16 PCI Express connector. This port is used to connect an adaptor card with a cable to another adaptor card in the root complex or host system. Alternatively, the upstream port can be defined as a x4 port allowing for fifteen downstream ports.

The downstream slots will conform to the x8 and x4 connector pin assignments but will be populated with x16 connectors. The unused lane bits on the x16 connectors will be unconnected. The core and IO power for the PES64H16 is derived from the 12V power supply connector from a 12VEPS type power supply with a 24-pin connector and a 8-pin connector with 12V. The downstream slot power is controlled through hot-plug controllers with power provided from the 12VEPS power supply connector with 12V. A personality module is used to optionally merge two x4 ports into one x8 downstream port connector. The PES64H16 Evaluation board block diagram is shown in Figure 1.1 and the PES48H12 / PES48T12 block diagram is shown in Figure 1.2.

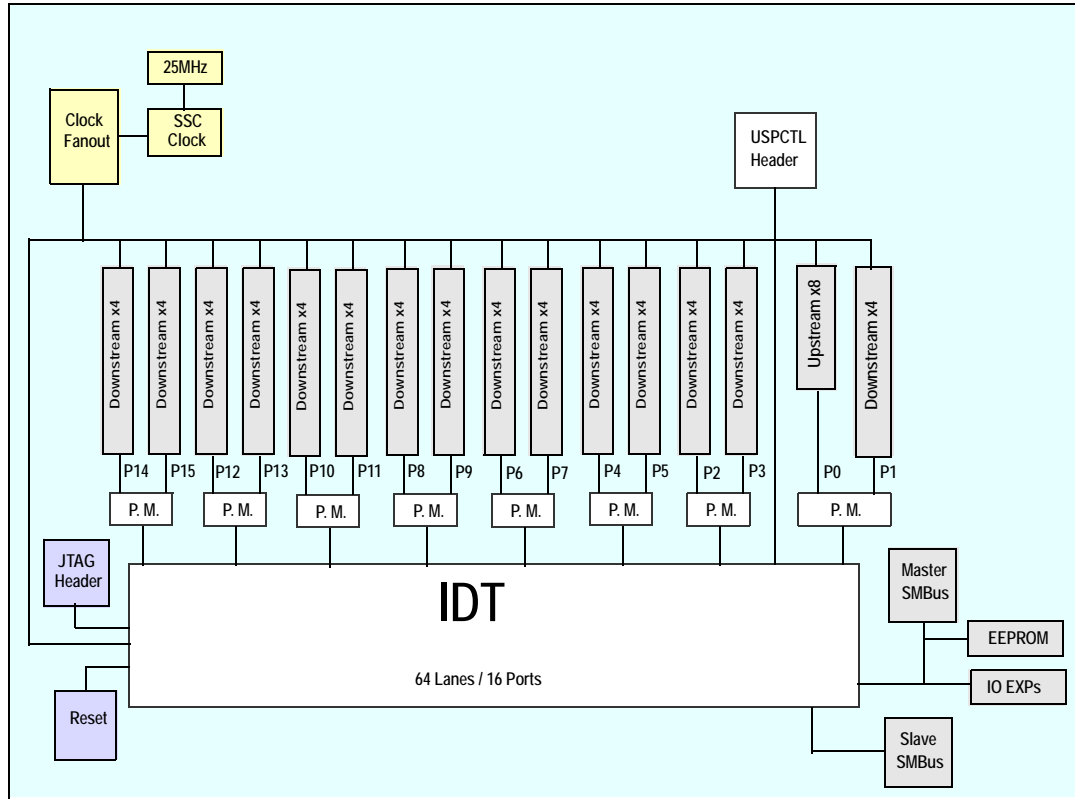


Figure 1.1 Functional Block Diagram of the EB64H16 Eval Board

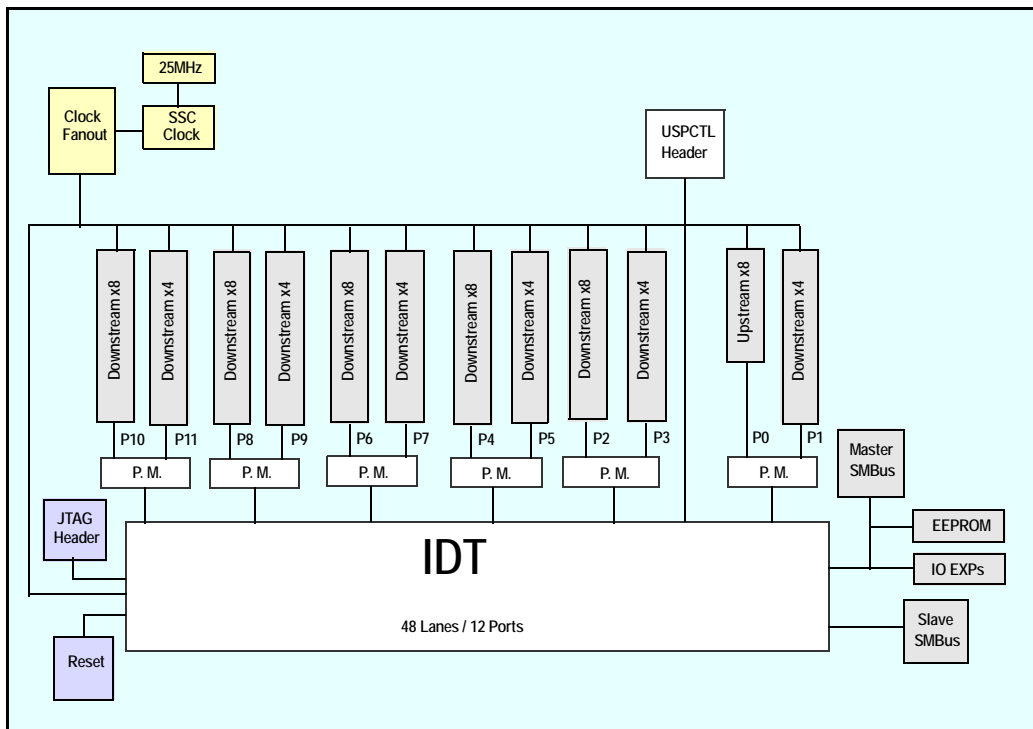


Figure 1.2 Functional Block Diagram of the EB48H12 and EB48T12 Eval Boards

Notes

Board Features
Feature List

- ◆ The EB64H16 has one x8 PCI Express upstream port to the root complex provided by a PCI Express adaptor board to a cable that connects to another adaptor board in the root complex or host system.
- ◆ The EB64H16 provides fifteen downstream connectors with x4 ports, while the EB48H12 and EN48T12 provide 11 downstream connectors. Two x4 downstream slots can be configured as one x8 port through the personality modules.
- ◆ All fifteen downstream slots for the PES64H16 and all eleven downstream slots for the PES48H12 and PES48T12 have hot-plug support through power isolation controlled by a hot-plug controller and IO expanders on the Master SMBUS. The Master SMBUS is controlled by the PES64H16 through configuration registers.
- ◆ The EB64H16 has a 12V to 2.5V DC-DC converter that uses the 12V power from an external 12VEPS power supply connector with 12V. The 2.5V provides power to the DC-DC converters for the PES64H16 core power.
- ◆ JTAG connector to the PES64H16 JTAG pins.
- ◆ Serial EEPROM on the PES64H16 master SMBUS interface.
- ◆ Provides an SMBUS connector on the PES64H16 slave SMBUS interface.
- ◆ Has a fundamental cold and warm reset mechanism and a reset push button switch.
- ◆ Provides a clock reference to the fifteen (or eleven) downstream ports from the upstream clock reference or from an on-board clock generator. The clock generator has spread spectrum clocking option and SMA connectors are provided to monitor the clock.
- ◆ Has LED displays to indicate power is applied, reset condition, port status, and downstream slot power.
- ◆ Has card present detect pins implemented on upstream and downstream slots.
- ◆ Has ATTN push button switches and LED displays for each downstream slot.
- ◆ Has a +12V fan connector for the integrated heatsink for the socket and soldered device.

Performance Summary

- ◆ Provides up to 16 ports with 64 PCIe lanes (PES64H16) or up to 12 ports with 48 PCIe lanes (PES48H12/PES48T12)
- ◆ Integrated SerDes support 2.5 Gbps operation
- ◆ Delivers up to 32 GBps (256 Gbps) of aggregate bandwidth
- ◆ Sub 280ns latency through the switch
- ◆ Supports two virtual channels
- ◆ Compliant with PCI Express Base Specification Rev1.1 with Rev 2.0 features
- ◆ Flexible Architecture with Numerous Configuration Options
- ◆ Eight x8 PCIe ports
- ◆ Each port can be independently bifurcated into two x4 PCIe ports
- ◆ Supports automatic per port link width negotiation(e.g., x8/x4/x2/x1 for a x8 port)
- ◆ Automatic lane reversal detection
- ◆ Independent per port crosslink support
- ◆ Supports lock transactions, allowing use of PCI Express with legacy software
- ◆ Ability to load device configuration from serial EEPROM
- ◆ Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems
- ◆ Supports external signal for power management event notification

Notes

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES64H16 within host systems running popular operating systems.

- ◆ Installation programs
 - Operating Systems Supported: Windows2000, WindowsXP, Linux
- ◆ GUI based application for Windows and Linux
 - Allows users to view and modify registers in the PES64H16
 - Binary file generator for programming the serial EEPROMs attached to the SMBUS

Other

An external power supply may be required under some conditions.

An SMBUS cable may be required for certain evaluation exercises.

SMA connectors are provided on the EB64H16 board for specific test points.

Revision History

January 16, 2007: Published production release board revision 0.9.



Installation of the EB64H16 Eval Board

Notes

EB64H16 Installation

This chapter discusses the steps required to configure and install the EB64H16 evaluation board. All available DIP switches and jumper configurations are explained in detail. The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Connect a PCI Express adapter card in an upstream port with a cable to another PCI Express adaptor card in the root complex or host system, as shown in Figure 2.1.
4. Turn the power switch on the eval board (located at S3) to ON.
5. Apply power to the host system.

The EB64H16 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

PCI Express Adapter Card

The PCI Express adapter card contains eight PCI Express lanes (see Figure 2.1). The lower four lanes are routed to an Infiniband connector J2 and the upper four lanes to J3. The differential REFCLKp and REFCLKn pins are routed to J5 and J6, respectively. The JTAG interface and PERST# pins are routed to J4 although only PERST# pin is actually used. Two PCI Express Adapter cards are required to connect the EB64H16 evaluation board to the host PC and remember to match the connector connection between two cards.

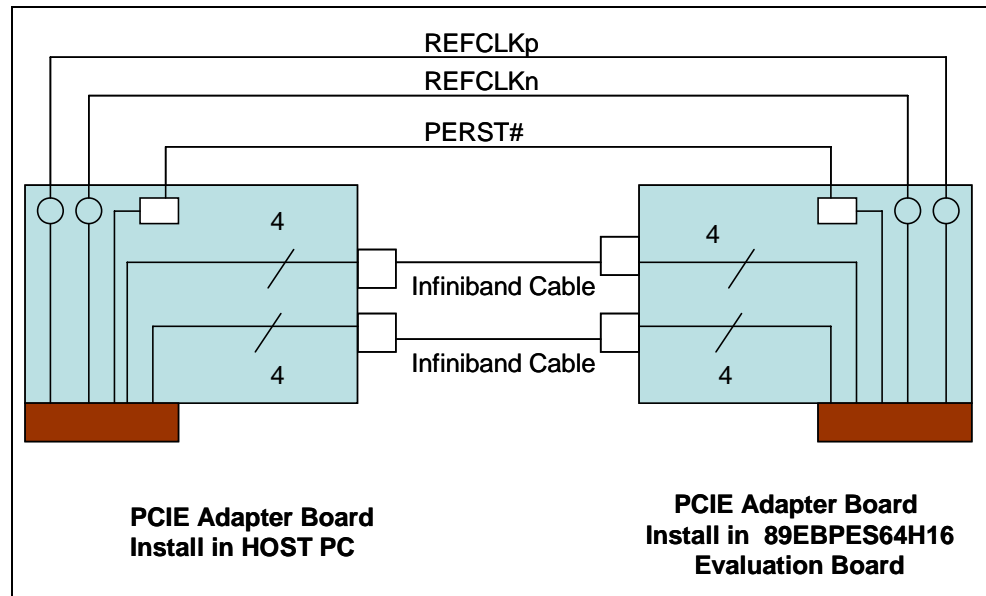


Figure 2.1 PCIe Adapter

Notes

Hardware Description

The PES64H16 is a 64-lane, 16-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 15 downstream ports or peer-to-peer switching between downstream ports.

The EB64H16 has 15 PCI Express downstream ports, accessible through fifteen x16 connectors. Seven specific ports are capable of negotiating a x1, x2, x4, or x8 link width and all fifteen ports are capable of negotiating a x1, x2, x4 link width. All endpoint cards connected to the PES64H16 must support at least one of these link widths. A personality module can be used to provide a single x8 downstream port by merging two specific x4 ports (see section PCI Express Personality Module on page 2-23).

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot. (If your host system does not offer a x8 slot, please contact ssdhelp@idt.com for alternative solutions.)
- x1, x2, x4, or x8 PCI Express Endpoint Cards.

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot is required to take full advantage of the PES64H16's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors, but only two are electronically connected for a x8 link width (J15 and J16). The remaining slots are electronically connected for a x4 link width configuration. Care must be taken to avoid using the EB64H16 in the x4 slot (J17). Figure 2.2 shows the proper connectors.

Notes

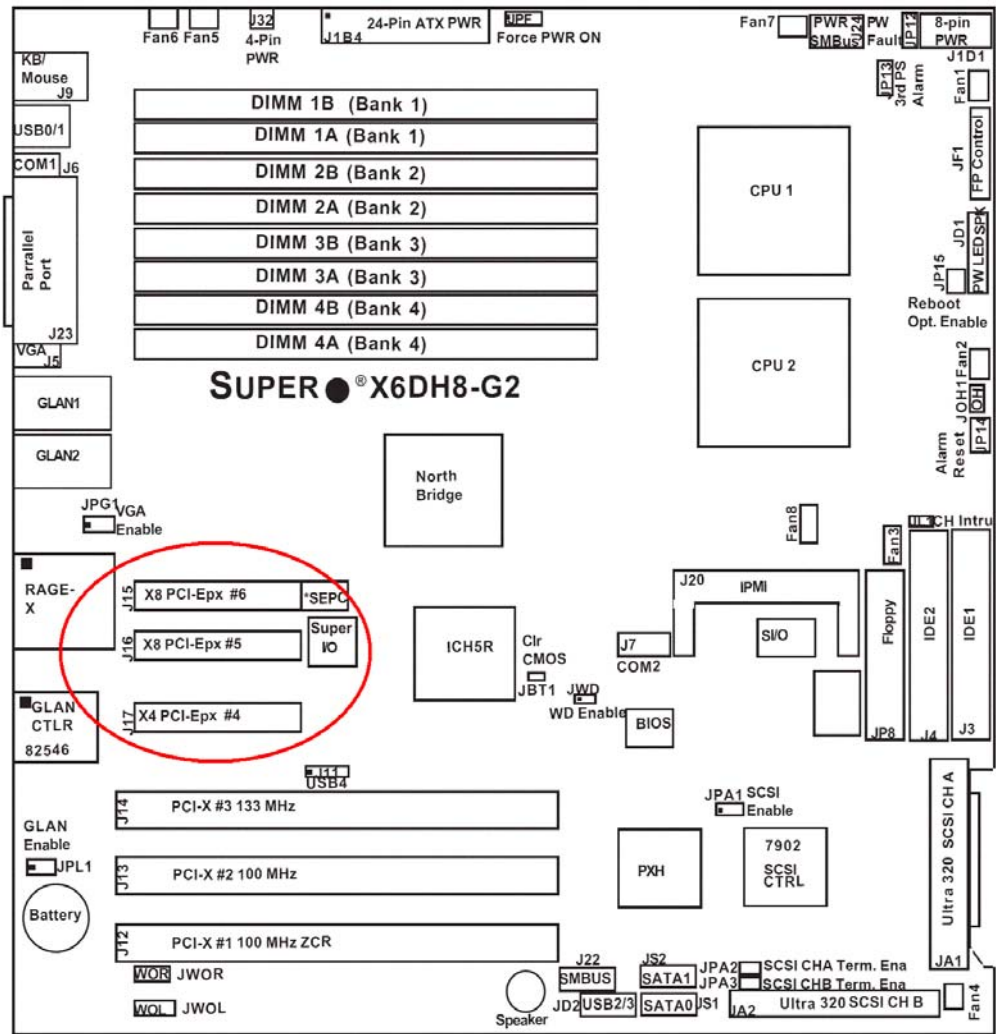


Figure 2.2 SuperMicro X6DH8-G2 Motherboard

Reference Clocks

The PES64H16 requires four differential reference clocks. The EB64H16 derives these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Install	Clock Source
R36, R37	Onboard Reference Clock – Use onboard clock generator
R35, R148	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS59FG104 clock generator device (U14) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB64H16 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S2[4:2]			
S2[4]	S2[3]	S2[2]	Clock Frequency
ON	ON	ON	100 MHz (Default)
ON	ON	OFF	125 MHz
ON	ON	ON	<Reserved>
OFF	OFF	OFF	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[1]	
S2[1]	Spread
OFF	No Spread (Default)
ON	Spread Enable

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock must be used instead.

The output of the two onboard clock generator is accessible through four SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J1, J3, J15, J8	
J1, J15	Positive Reference Clock
J3, J8	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Figure 2.3 illustrates the clock distribution block diagram for the EB64H16 evaluation board.

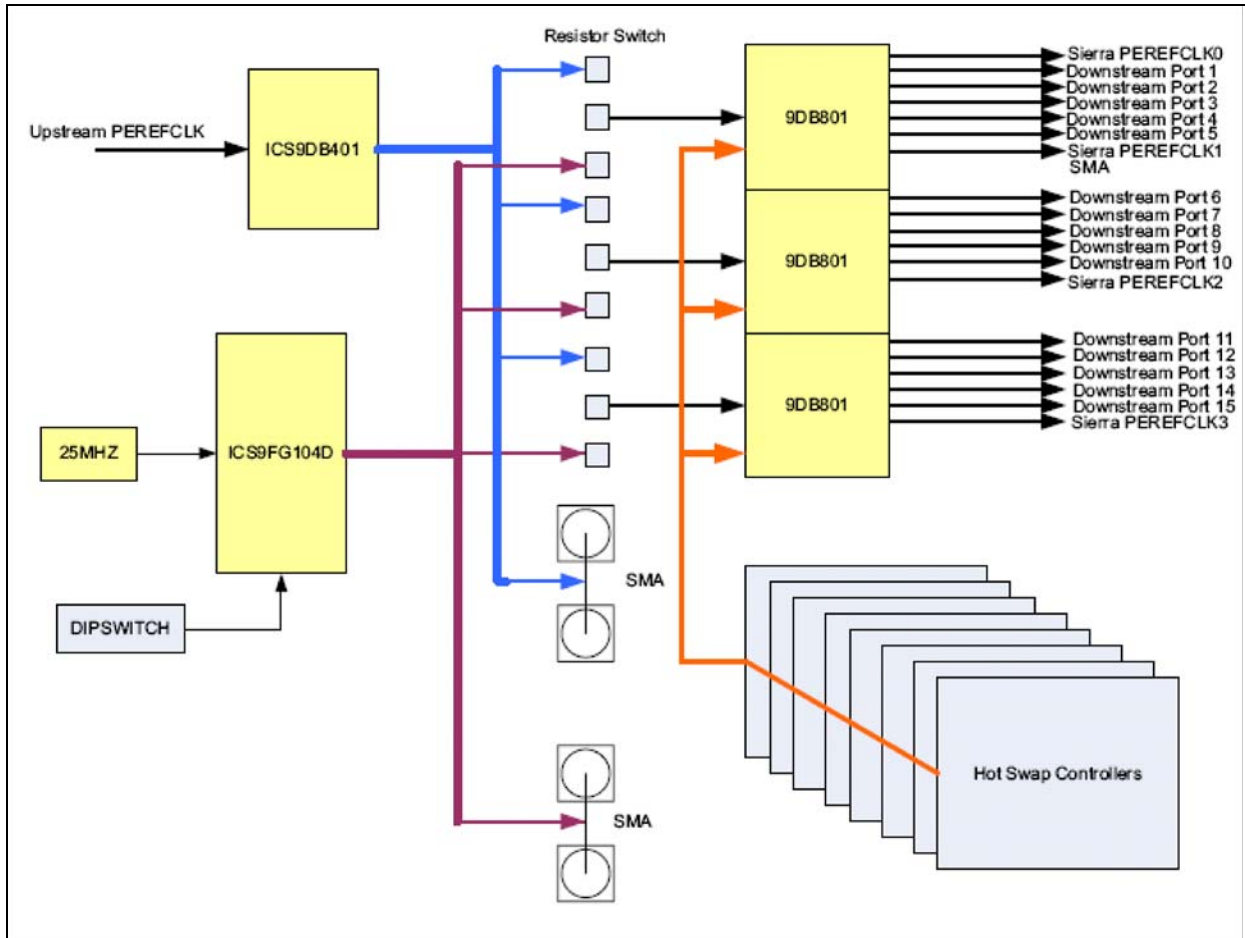


Figure 2.3 Clock Distribution Block Diagram

Power Sources

Power for the PES64H16 and all downstream ports is generated from the 12V from an external power connector. See Figure 2.4. A 12V to 2.5V DC-DC converter is used to provide power to four LDO linear regulators to generate V_{DDCORE} , V_{DDPEe} , V_{DDAPE} , and V_{TTPE} voltages. The 2.5V from the DC-DC converter is used to power the clock buffers. 3.3V is supplied from the power connector for V_{DDIO} .

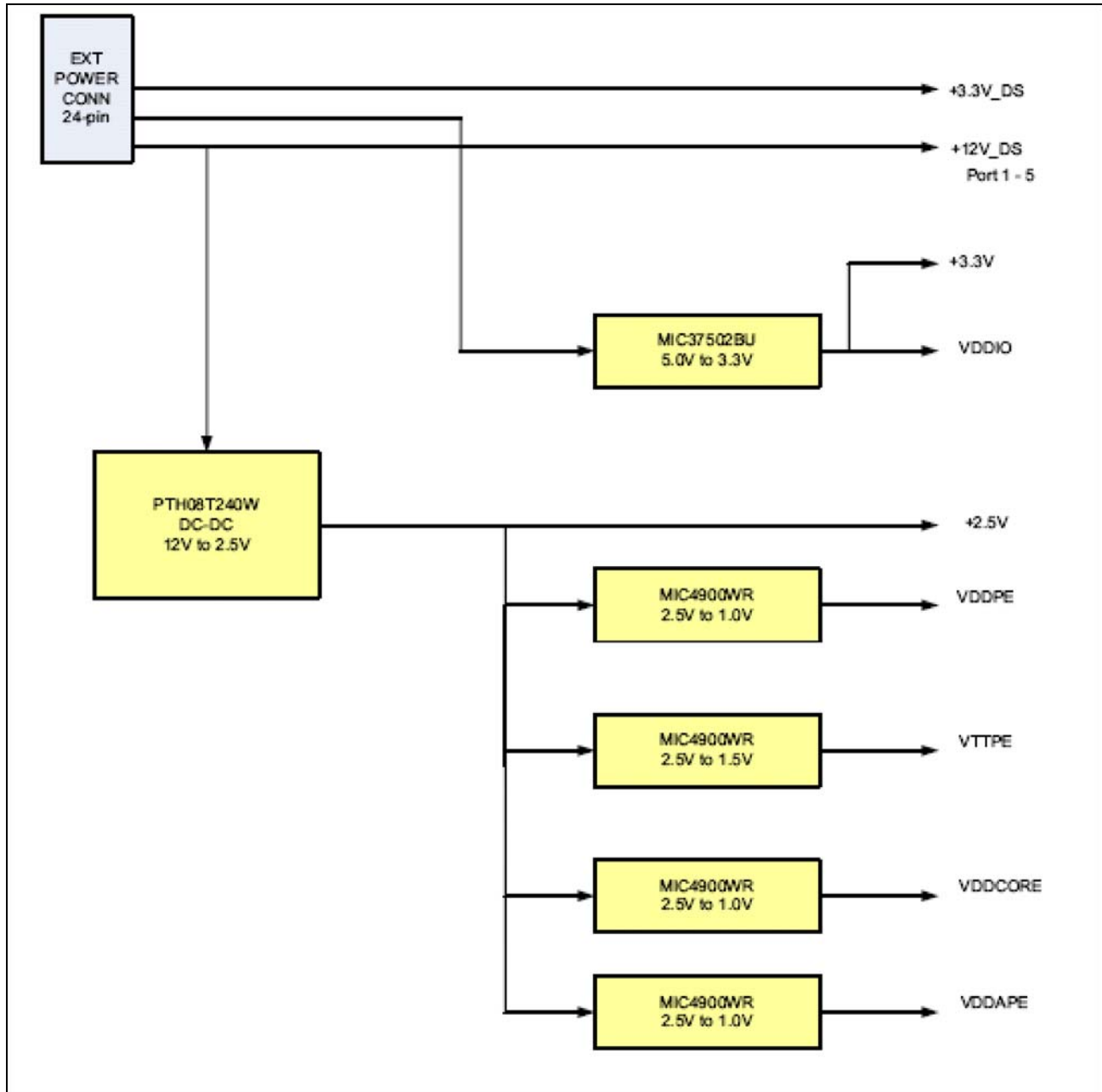


Figure 2.4 Power Distribution Block Diagram

Notes

The external power supply connectors are a 24-pin (J6) and an 8-pin (J5) molex connector as described in Table 2.5 and Table 2.6. The +12V3 is used to power PES64H16 and downstream ports 1 through 5. The +12V1 is used to power downstream ports 6 through 10. The +12V2 is used to power downstream ports 11 through 15.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.5 EPS12V 24_pin Power Connector - J6

Pin	Signal	Pin	Signal
1	GND	5	+12V1
2	GND	6	+12V1
3	GND	7	+12V2
4	GND	8	+12V2

Table 2.6 EPS12V 8-Pin Connector - J5

The power on switch located at S3 can be used to control the supply power from the external power supply connector. Add a shunt to W19 to enable power on switch.

Power Supply Minimum Load Connectors

To provide the minimum load requirement for each rail of the EPS12V supply, a 2-pin fan connector is provided for connecting to an external power resistor for each rail.

Connector	Supply	Load Resistor Value
W157	3.3V	5.0 ohm
W158	5V	5.0 ohm
W100	12V1	25.0 ohm
W156	12V2	25.0 ohm
W159	12V3	25.0 ohm

Table 2.7 Minimum Load Connectors

Notes

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (VTT) to the PES64H16.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES64H16.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U28) provides a 1.0V PCI Express analog power voltage (VDDAPE) to the PES64H16.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES64H16.

3.3V I/O Power Module

A separate DC-DC converter (U17) provides the 3.3V I/O voltage (VDDIO) to the PES64H16.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements.

Required Jumpers

To deliver power to the PES64H16 switch, the following jumpers must be shunted: W151, W152, WW153, W154, W155. These jumpers were implemented so that the power consumption of the PES64H16 can be measured.

Heatsink Requirement

The PES64H16 with a maximum power dissipation of 13W will require a heatsink. The EB64H16 evaluation board utilizes Molex heatsink with integrated fan.

Reset

The PES64H16 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES64H16, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES64H16 User Manual. The EB64H16 evaluation board provides seamless support for Hot Reset.

Notes

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB64H16 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES64H16.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
 - Pressing a push-button switch (S1) located on EB64H16 board
 - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB64H16. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W1.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES64H16 while power is on.

Downstream Reset

The PES64H16 provides a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.8.

Port #	Jumper	Selection
1	W102	[1-2] Software controlled reset through GPIO6 [2-3] Fundamental reset PERST# (default)
2	W107	[1-2] Software controlled reset through GPIO7 [2-3] Fundamental reset PERST# (default)
3	W108	[1-2] Software controlled reset through GPIO8 [2-3] Fundamental reset PERST# (default)
4	W113	[1-2] Software controlled reset through GPIO9 [2-3] Fundamental reset PERST# (default)
5	W114	[1-2] Software controlled reset through GPIO10 [2-3] Fundamental reset PERST# (default)
6	W119	[1-2] Software controlled reset through GPIO11 [2-3] Fundamental reset PERST# (default)
7	W120	[1-2] Software controlled reset through GPIO12 [2-3] Fundamental reset PERST# (default)
8	W125	[1-2] Software controlled reset through GPIO13 [2-3] Fundamental reset PERST# (default)
9	W126	[1-2] Software controlled reset through GPIO14 [2-3] Fundamental reset PERST# (default)
10	W131	[1-2] Software controlled reset through GPIO15 [2-3] Fundamental reset PERST# (default)
11	W132	[1-2] Software controlled reset through GPIO16 [2-3] Fundamental reset PERST# (default)
12	W137	[1-2] Software controlled reset through GPIO17 [2-3] Fundamental reset PERST# (default)

Table 2.8 Downstream Reset Selection (Part 1 of 2)

Notes

Port #	Jumper	Selection
13	W138	[1-2] Software controlled reset through GPIO18 [2-3] Fundamental reset PERST# (default)
14	W143	[1-2] Software controlled reset through GPIO19 [2-3] Fundamental reset PERST# (default)
15	W144	[1-2] Software controlled reset through GPIO20 [2-3] Fundamental reset PERST# (default)

Table 2.8 Downstream Reset Selection (Part 2 of 2)

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.9 is sampled by the PES64H16 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5 and S6 as defined in Table 2.10.

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0
P01MERGEN	Port 0 and 1 Merge: When this pin is asserted (i.e. low), port 1 is merged with port 0 to form a single x8 port. Default: 0x0
P23MERGEN	Port 2 and 3 Merge: When this pin is asserted (i.e. low), port 2 is merged with port 3 to form a single x8 port. Default: 0x1
P45MERGEN	Port 4 and 5 Merge: When this pin is asserted (i.e. low), port 4 is merged with port 5 to form a single x8 port. Default: 0x1
P67MERGEN	Port 6 and 7 Merge: When this pin is asserted (i.e. low), port 6 is merged with port 7 to form a single x8 port. Default: 0x1
P89MERGEN	Port 8 and 9 Merge: When this pin is asserted (i.e. low), port 8 is merged with port 9 to form a single x8 port. Default: 0x1
P1011MERGEN	Port 10 and 11 Merge: When this pin is asserted (i.e. low), port 10 is merged with port 11 to form a single x8 port. Default: 0x1
P1213MERGEN	Port 12 and 13 Merge: When this pin is asserted (i.e. low), port 12 is merged with port 13 to form a single x8 port. Default: 0x1
P1415MERGEN	Port 14 and 15 Merge: When this pin is asserted (i.e. low), port 14 is merged with port 15 to form a single x8 port. Default: 0x1
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES64H16 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0

Table 2.9 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
SWMODE[3:0]	Switch Mode. These configuration pins determine the PES64H16 switch operating mode. Default: 0x0 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x7 - Reserved 0x8 - Normal switch mode with upstream port failover (port 0 selected as the upstream port) 0x9 - Normal switch mode with upstream port failover (port 2 selected as the upstream port) 0xA - Normal switch mode with Serial EEPROM and upstream port failover (port 0 selected as the upstream port) 0xB - Normal switch mode with Serial EEPROM and upstream port failover (port 2 selected as the upstream port) 0xC through 0xF - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[4:1]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.9 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S19[1]	CCLKDS	OFF
S19[2]	CCLKUS	OFF
S19[3]	MSMBSMODE	ON
S20[1]	P01MERGEN	ON
S20[2]	P23MERGEN	OFF
S20[3]	P45MERGEN	OFF
S20[4]	P67MERGEN	OFF
S20[5]	P89MERGEN	OFF
S20[6]	P1011MERGEN	OFF
S20[7]	P1213MERGEN	OFF
S20[8]	P11415MERGEN	OFF
S19[8]	RSTHALT	ON
S21[1]	SWMODE[0]	ON
S21[2]	SWMODE[1]	ON
S21[3]	SWMODE[2]	ON
S21[4]	SWMODE[3]	ON
S21[5]	REFCLKM	ON
S21[6]	MSMBADDR[0]	ON
S21[7]	MSMBADDR[1]	ON
S21[8]	MSMBADDR[2]	ON

Table 2.10 Boot Configuration Vector Switches S19, S20 & S21 (ON=0, OFF=1)

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I²C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES64H16 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the EB64H16 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.11.

Slave SMBus Interface Connector J34	
Pin	Signal
1	N/C
2	SSMBCLK
3	GND
4	SSMBDATA

Table 2.11 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES64H16 slave interface is **0b1110111** by default and is configurable using jumpers W146, W147, W148, and W149 as described in Tables 2.12 and 2.13.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.12 SMBus Slave Interface Address Configuration

Notes

SMBUS Slave Interface Address Setting				
W146 SSMBADDR[5]	W147 SSMBADDR[3]	W148 SSMBADDR[2]	W149 SSMBADDR[1]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.13 PES64H16 SMBus Slave Interface Address Setting

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are 10 16-bit I/O Expanders (Maxim PAX731) and a serial EEPROM (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through I/O Expander 10 are fixed through the stuffing resistor as 0x0, 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9 and 0xA, respectively.

The bus address for the selected EEPROM device is **0b1000** by default and is configurable using W145 and the switch S21 as described in Table 2.14.

W145	S21[8]	S21[7]	S21[6]	Bus Address
OFF	OFF	OFF	OFF	0b0101 1111
OFF	OFF	OFF	ON	0b0101 1110
OFF	OFF	ON	OFF	0b0101 1101

Table 2.14 EEPROM SMBus Address Setting (Part 1 of 2)

Notes

W145	S21[8]	S21[7]	S21[6]	Bus Address
OFF	OFF	ON	ON	0b0101 1100
OFF	ON	OFF	OFF	0b0101 1011
OFF	ON	OFF	ON	0b0101 1010
OFF	ON	ON	OFF	0b0101 1001
OFF	ON	ON	ON	0b0101 1000
ON	ON	ON	ON	0b0101 0000 (Default)

Table 2.14 EEPROM SMBus Address Setting (Part 2 of 2)

JTAG Header

The PES64H16 provides a JTAG connector J33 for access to the PES64H16 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.15 for the JTAG Connector J33 pin out.

JTAG Connector J33					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.15 JTAG Connector Pin Out

Attention Buttons

The PES64H16 features fifteen attention buttons, shown in Table 2.16. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S5	Port 1 Attention Button
S4	Port 2 Attention Button
S10	Port 3 Attention Button
S11	Port 4 Attention Button
S6	Port 5 Attention Button
S7	Port 6 Attention Button
S8	Port 7 Attention Button
S9	Port 8 Attention Button
S12	Port 9 Attention Button
S13	Port 10 Attention Button
S14	Port 11 Attention Button

Table 2.16 Attention Buttons (Part 1 of 2)

Notes

Button	Description
S15	Port 12 Attention Button
S16	Port 13 Attention Button
S17	Port 14 Attention Button
S18	Port 15 Attention Button

Table 2.16 Attention Buttons (Part 2 of 2)

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W2-W4, W7, W10-W16, W48-W51	Header	Shunted	Bypass hot-plug controller - Enable REFCLK to downstream ports (Default)
W150	Header	Shunted	Disable EEPROM Write protect feature (Default)
W19	Header	Open	Enable Power On Switch (S3) (Default)
W91	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 1 (Default)
W57	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 2 (Default)
W58	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 3 (Default)
W70	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 4 (Default)
W71	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 5 (Default)
W75	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 6 (Default)
W76	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 7 (Default)
W79	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 8 (Default)
W80	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 9 (Default)
W83	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 10 (Default)
W84	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 11 (Default)
W87	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 12 (Default)

Table 2.17 Miscellaneous Jumpers, Headers (Part 1 of 4)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W88	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 13 (Default)
W91	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 14 (Default)
W92	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 15 (Default)
W97	Header	Shunted	2-3: Port 1, 3.3Vaux source from External Power (Default) 1-2: Port 1, 3.3Vaux source from hot-plug controller
W69	Header	2-3 Shunted	2-3: Port 2, 3.3Vaux source from External Power (Default) 1-2: Port 2, 3.3Vaux source from hot-plug controller
W70	Header	2-3 Shunted	2-3: Port 3, 3.3Vaux source from External Power (Default) 1-2: Port 3, 3.3Vaux source from hot-plug controller
W73	Header	2-3 Shunted	2-3: Port 4, 3.3Vaux source from External Power (Default) 1-2: Port 4, 3.3Vaux source from hot-plug controller
W74	Header	2-3 Shunted	2-3: Port 5, 3.3Vaux source from External Power (Default) 1-2: Port 5, 3.3Vaux source from hot-plug controller
W77	Header	2-3 Shunted	2-3: Port 6, 3.3Vaux source from External Power (Default) 1-2: Port 6, 3.3Vaux source from hot-plug controller
W78	Header	2-3 Shunted	2-3: Port 7, 3.3Vaux source from External Power (Default) 1-2: Port 7, 3.3Vaux source from hot-plug controller
W81	Header	2-3 Shunted	2-3: Port 8, 3.3Vaux source from External Power (Default) 1-2: Port 8, 3.3Vaux source from hot-plug controller
W82	Header	2-3 Shunted	2-3: Port 9, 3.3Vaux source from External Power (Default) 1-2: Port 9, 3.3Vaux source from hot-plug controller
W85	Header	2-3 Shunted	2-3: Port 10, 3.3Vaux source from External Power (Default) 1-2: Port 10, 3.3Vaux source from hot-plug controller
W86	Header	2-3 Shunted	2-3: Port 11, 3.3Vaux source from External Power (Default) 1-2: Port 11, 3.3Vaux source from hot-plug controller
W89	Header	2-3 Shunted	2-3: Port 12, 3.3Vaux source from External Power (Default) 1-2: Port 12, 3.3Vaux source from hot-plug controller
W90	Header	2-3 Shunted	2-3: Port 13, 3.3Vaux source from External Power (Default) 1-2: Port 13, 3.3Vaux source from hot-plug controller
W93	Header	2-3 Shunted	2-3: Port 14, 3.3Vaux source from External Power (Default) 1-2: Port 14, 3.3Vaux source from hot-plug controller
W94	Header	2-3 Shunted	2-3: Port 15, 3.3Vaux source from External Power (Default) 1-2: Port 15, 3.3Vaux source from hot-plug controller
W99	Header	2-3 Shunted	2-3: Port 1, +12V source base on W91 (Default) 1-2: Port 1, +12V source from hot-plug controller
W103	Header	2-3 Shunted	2-3: Port 2, +12V source base on W57 (Default) 1-2: Port 2, +12V source from hot-plug controller
W104	Header	2-3 Shunted	2-3: Port 3, +12V source base on W58 (Default) 1-2: Port 3, +12V source from hot-plug controller

Table 2.17 Miscellaneous Jumpers, Headers (Part 2 of 4)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W109	Header	2-3 Shunted	2-3: Port 4, +12V source base on W71 (Default) 1-2: Port 4, +12V source from hot-plug controller
W110	Header	2-3 Shunted	2-3: Port 5, +12V source base on W72 (Default) 1-2: Port 5, +12V source from hot-plug controller
W115	Header	2-3 Shunted	2-3: Port 6, +12V source base on W75 (Default) 1-2: Port 6, +12V source from hot-plug controller
W116	Header	2-3 Shunted	2-3: Port 7, +12V source base on W76 (Default) 1-2: Port 7, +12V source from hot-plug controller
W121	Header	2-3 Shunted	2-3: Port 8, +12V source base on W79 (Default) 1-2: Port 8, +12V source from hot-plug controller
W122	Header	2-3 Shunted	2-3: Port 9, +12V source base on W80 (Default) 1-2: Port 9, +12V source from hot-plug controller
W127	Header	2-3 Shunted	2-3: Port 10, +12V source base on W83 (Default) 1-2: Port 10, +12V source from hot-plug controller
W128	Header	2-3 Shunted	2-3: Port 11, +12V source base on W84 (Default) 1-2: Port 11, +12V source from hot-plug controller
W133	Header	2-3 Shunted	2-3: Port 12, +12V source base on W87 (Default) 1-2: Port 12, +12V source from hot-plug controller
W34	Header	2-3 Shunted	2-3: Port 13, +12V source base on W88 (Default) 1-2: Port 13, +12V source from hot-plug controller
W139	Header	2-3 Shunted	2-3: Port 14, +12V source base on W91 (Default) 1-2: Port 14, +12V source from hot-plug controller
W140	Header	2-3 Shunted	2-3: Port 15, +12V source base on W92 (Default) 1-2: Port 15, +12V source from hot-plug controller
W101	Header	2-3 Shunted	2-3: Port 1, +3.3V source base on W95 (Default) 1-2: Port 1, +3.3V source from hot-plug controller
W105	Header	2-3 Shunted	2-3: Port 2, +3.3V source base on W57 (Default) 1-2: Port 2, +3.3V source from hot-plug controller
W106	Header	2-3 Shunted	2-3: Port 3, +3.3V source base on W58 (Default) 1-2: Port 3, +3.3V source from hot-plug controller
W111	Header	2-3 Shunted	2-3: Port 4, +3.3V source base on W71 (Default) 1-2: Port 4, +3.3V source from hot-plug controller
W112	Header	2-3 Shunted	2-3: Port 5, +3.3V source base on W72 (Default) 1-2: Port 5, +3.3V source from hot-plug controller
W117	Header	2-3 Shunted	2-3: Port 6, +3.3V source base on W75 (Default) 1-2: Port 6, +3.3V source from hot-plug controller
W118	Header	2-3 Shunted	2-3: Port 7, +3.3V source base on W76 (Default) 1-2: Port 7, +3.3V source from hot-plug controller
W123	Header	2-3 Shunted	2-3: Port 8, +3.3V source base on W79 (Default) 1-2: Port 8, +3.3V source from hot-plug controller
W124	Header	2-3 Shunted	2-3: Port 9, +3.3V source base on W80 (Default) 1-2: Port 9, +3.3V source from hot-plug controller

Table 2.17 Miscellaneous Jumpers, Headers (Part 3 of 4)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W129	Header	2-3 Shunted	2-3: Port 10, +3.3V source base on W83 (Default) 1-2: Port 10, +3.3V source from hot-plug controller
W130	Header	2-3 Shunted	2-3: Port 11, +3.3V source base on W84 (Default) 1-2: Port 11, +3.3V source from hot-plug controller
W135	Header	2-3 Shunted	2-3: Port 12, +3.3V source base on W87 (Default) 1-2: Port 12, +3.3V source from hot-plug controller
W136	Header	2-3 Shunted	2-3: Port 13, +3.3V source base on W88 (Default) 1-2: Port 13, +3.3V source from hot-plug controller
W141	Header	2-3 Shunted	2-3: Port 14, +3.3V source base on W91 (Default) 1-2: Port 14, +3.3V source from hot-plug controller
W142	Header	2-3 Shunted	2-3: Port 15, +3.3V source base on W92 (Default) 1-2: Port 15, +3.3V source from hot-plug controller

Table 2.17 Miscellaneous Jumpers, Headers (Part 4 of 4)

LEDs

There are several LED indicators on the EB64H16 which convey status feedback. A description of each is provided in Table 2.18.

Location	Color	Definition
DS87	Green	Port1: Power-is-good indicator
DS74	Green	Port2: Power-is-good indicator
DS73	Green	Port3: Power-is-good indicator
DS76	Green	Port4: Power-is-good indicator
DS75	Green	Port5: Power-is-good indicator
DS78	Green	Port6: Power-is-good indicator
DS77	Green	Port7: Power-is-good indicator
DS80	Green	Port8: Power-is-good indicator
DS79	Green	Port9: Power-is-good indicator
DS82	Green	Port10: Power-is-good indicator
DS81	Green	Port11: Power-is-good indicator
DS84	Green	Port12: Power-is-good indicator
DS83	Green	Port13: Power-is-good indicator
DS86	Green	Port14: Power-is-good indicator
DS85	Green	Port15: Power-is-good indicator
DS9	Yellow	Port1: Attention Indicator
DS4	Yellow	Port2: Attention Indicator
DS5	Yellow	Port3: Attention Indicator

Table 2.18 LED Indicators (Part 1 of 3)

Notes

Location	Color	Definition
DS6	Yellow	Port4: Attention Indicator
DS7	Yellow	Port5: Attention Indicator
DS8	Yellow	Port6: Attention Indicator
DS11	Yellow	Port7: Attention Indicator
DS12	Yellow	Port8: Attention Indicator
DS13	Yellow	Port9: Attention Indicator
DS14	Yellow	Port10: Attention Indicator
DS15	Yellow	Port11: Attention Indicator
DS16	Yellow	Port12: Attention Indicator
DS17	Yellow	Port13: Attention Indicator
DS18	Yellow	Port14: Attention Indicator
DS19	Yellow	Port15: Attention Indicator
DS10	Green	Port1: Power Indicator
DS20	Green	Port2: Power Indicator
DS21	Green	Port3: Power Indicator
DS22	Green	Port4: Power Indicator
DS23	Green	Port5: Power Indicator
DS24	Green	Port6: Power Indicator
DS25	Green	Port7: Power Indicator
DS26	Green	Port8: Power Indicator
DS27	Green	Port9: Power Indicator
DS28	Green	Port10: Power Indicator
DS29	Green	Port11: Power Indicator
DS30	Green	Port12: Power Indicator
DS31	Green	Port13: Power Indicator
DS32	Green	Port14: Power Indicator
DS33	Green	Port15: Power Indicator
DS3	Green	Port0: Active Status Output
DS50	Green	Port1: Active Status Output
DS51	Green	Port2: Active Status Output
DS52	Green	Port3: Active Status Output
DS53	Green	Port4: Active Status Output
DS54	Green	Port5: Active Status Output
DS55	Green	Port6: Active Status Output
DS56	Green	Port7: Active Status Output
DS57	Green	Port8: Active Status Output
DS58	Green	Port9: Active Status Output

Table 2.18 LED Indicators (Part 2 of 3)

Notes

Location	Color	Definition
DS59	Green	Port10: Active Status Output
DS60	Green	Port11: Active Status Output
DS61	Green	Port12: Active Status Output
DS62	Green	Port13: Active Status Output
DS63	Green	Port14: Active Status Output
DS64	Green	Port15: Active Status Output
DS42	Green	Port0: Link Up Status Output
DS43	Green	Port1: Link Up Status Output
DS44	Green	Port2: Link Up Status Output
DS45	Green	Port3: Link Up Status Output
DS46	Green	Port4: Link Up Status Output
DS34	Green	Port5: Link Up Status Output
DS35	Green	Port6: Link Up Status Output
DS36	Green	Port7: Link Up Status Output
DS37	Green	Port8: Link Up Status Output
DS38	Green	Port9: Link Up Status Output
DS39	Green	Port10: Link Up Status Output
DS40	Green	Port11: Link Up Status Output
DS41	Green	Port12: Link Up Status Output
DS47	Green	Port13: Link Up Status Output
DS48	Green	Port14: Link Up Status Output
DS49	Green	Port15: Link Up Status Output
DS65	Red	Hot Plug Controller1: Power Fault Indicator
DS66	Red	Hot Plug Controller2: Power Fault Indicator
DS67	Red	Hot Plug Controller3: Power Fault Indicator
DS68	Red	Hot Plug Controller4: Power Fault Indicator
DS69	Red	Hot Plug Controller5: Power Fault Indicator
DS70	Red	Hot Plug Controller6: Power Fault Indicator
DS71	Red	Hot Plug Controller7: Power Fault Indicator
DS72	Red	Hot Plug Controller8: Power Fault Indicator
DS2	Green	Board Power Indicator (3.3V)
DS1	Red	Board Reset Indicator

Table 2.18 LED Indicators (Part 3 of 3)

Notes

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved

Table 2.19 PCI Express x16 Connector Pinout (Part 1 of 3)

Notes

Pin	Side A		Side B	
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground
50	PETp8	Transmitter differential	RSVD	Reserved
51	PETn8	pair, Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential
53	GND	Ground	PERn8	pair, Lane 8
54	PETp9	Transmitter differential	GND	Ground
55	PETn9	pair, Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential
57	GND	Ground	PERn9	pair, Lane 9
58	PETp10	Transmitter differential	GND	Ground
59	PETn10	pair, Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential
61	GND	Ground	PERn10	pair, Lane 10
62	PETp11	Transmitter differential	GND	Ground
63	PETn11	pair, Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential
65	GND	Ground	PERn11	pair, Lane 11
66	PETp12	Transmitter differential	GND	Ground
67	PETn12	pair, Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential
69	GND	Ground	PERn12	pair, Lane 12
70	PETp13	Transmitter differential	GND	Ground

Table 2.19 PCI Express x16 Connector Pinout (Part 2 of 3)

Notes

Pin	Side A		Side B	
71	PETn13	pair, Lane 13	GND	Ground
72	GND	Ground	PERp13	Receiver differential
73	GND	Ground	PERn13	pair, Lane 13
74	PETp14	Transmitter differential	GND	Ground
75	PETn14	pair, Lane 14	GND	Ground
76	GND	Ground	PERp14	Receiver differential
77	GND	Ground	PERn14	pair, Lane 14
78	PETp15	Transmitter differential	GND	Ground
79	PETn15	pair, Lane 15	GND	Ground
80	GND	Ground	PERp15	Receiver differential
81	PRSNT2#	Hot-Plug presence detect	PERn15	pair, Lane 15
82	RSVD	Reserved	GND	Ground

Table 2.19 PCI Express x16 Connector Pinout (Part 3 of 3)

Note: These x16 PCI Express connectors comply with the PCIe specification. However, the downstream ports on the EB64H16 are electronically connected in either a x8 configuration (ports 2, 4, 6, 8, 10, 12, and 14) or a x4 configuration (ports 1 through 15).

PCI Express Personality Module

The PES64H16 supports port merging in a static manner during a fundamental reset. A PCI Express personality module is used in the EB64H16 to merge two consecutive x4 even and odd ports into a single x8 port, e.g., ports 0 and 1, ports 2 and 3, etc., finishing with ports 14 and 15. When side 1 of the personality module is inserted into the personality module connector (see Table 2.20 below for connector locations), four PCI Express lanes are routed to each port. When side 2 of the personality module is inserted into the personality module connector, eight PCI Express lanes are routed to the even port and the odd port is disconnected. Note that all eight connectors must have a personality module inserted, whether all side 1, all side 2, or a combination. If all eight personality module cards have side 1 plugged in, all 16 ports are in use. If all cards have side 2 plugged in, only 8 ports are in use.

Merged Ports	Personality Module Location
0/1	J7
2/3	J9
4/5	J10
6/7	J11
8/9	J12
10/11	J13
12/13	J14
14/15	J15

Table 2.20 PES64H16 Personality Module Locations

EB64H16 Evaluation Board Block Diagram

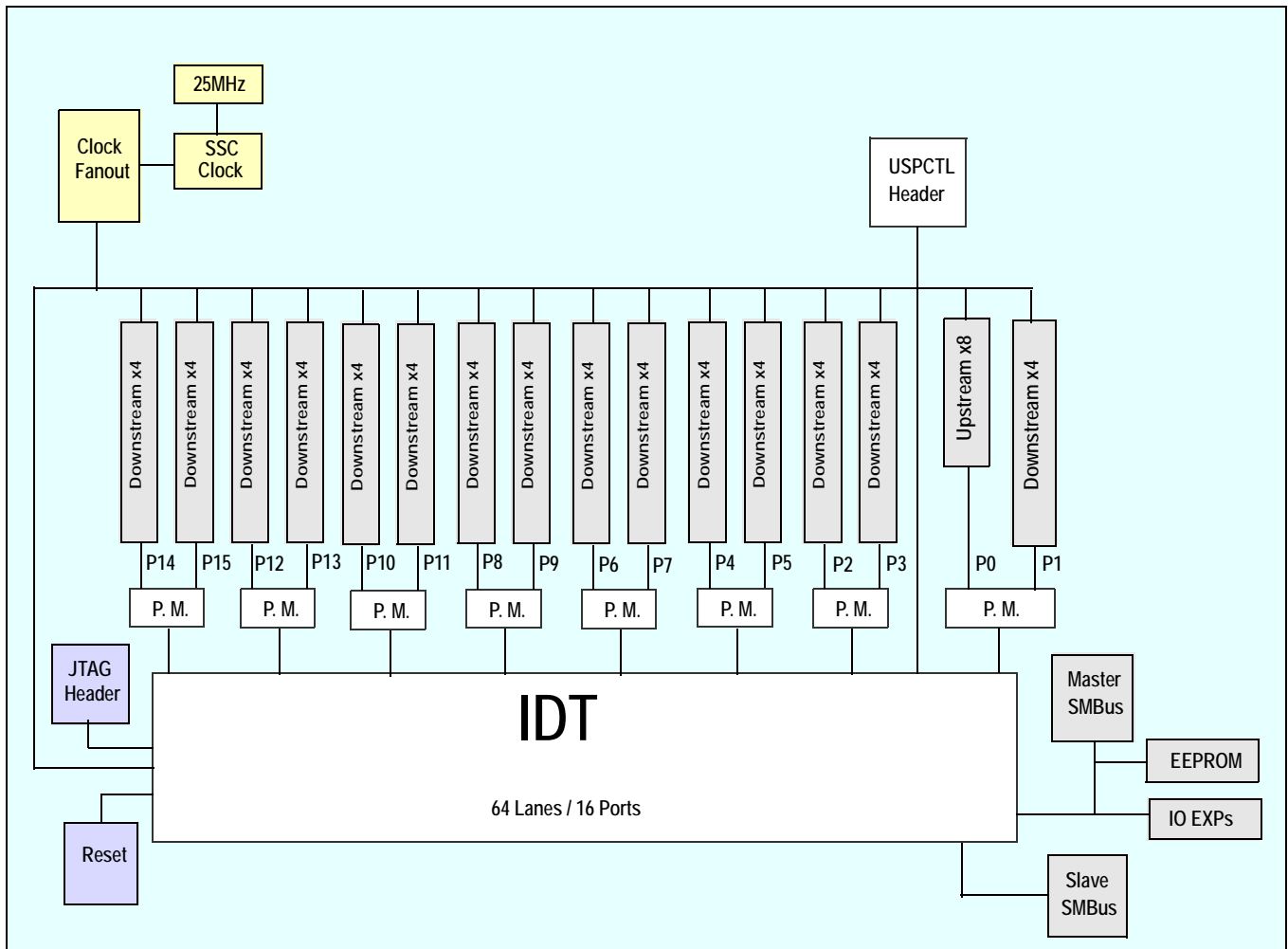


Figure 2.5 EB64H16 Eval Board Block Diagram

EB48H12 / EB48T12 Evaluation Board Block Diagram

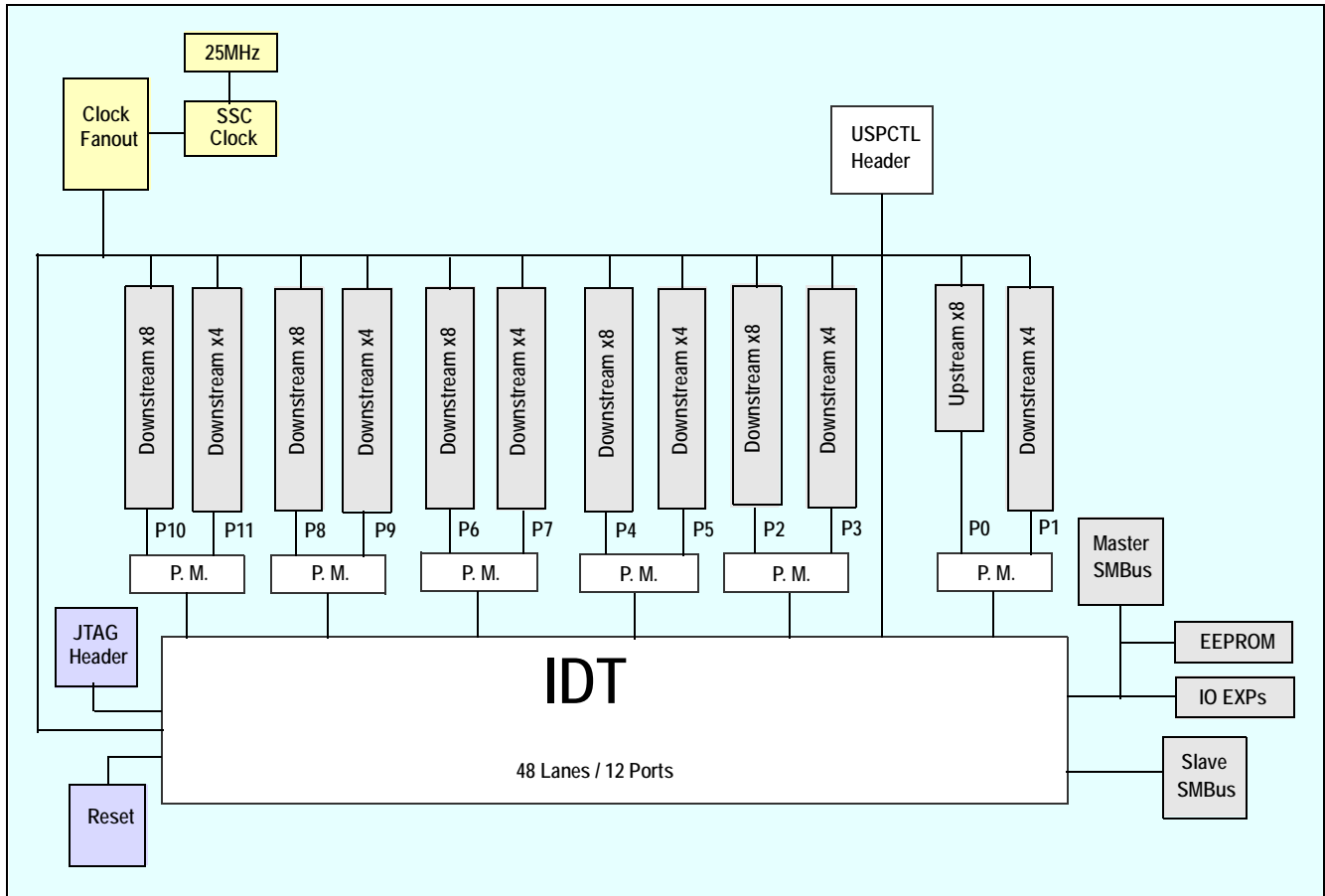


Figure 2.6 EB48H12 / EB48T12 Eval Board Block Diagram



Software for the EB64H16 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB64H16 evaluation board using the device management software. Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES64H16 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES64H16.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES64H16, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES64H16 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes

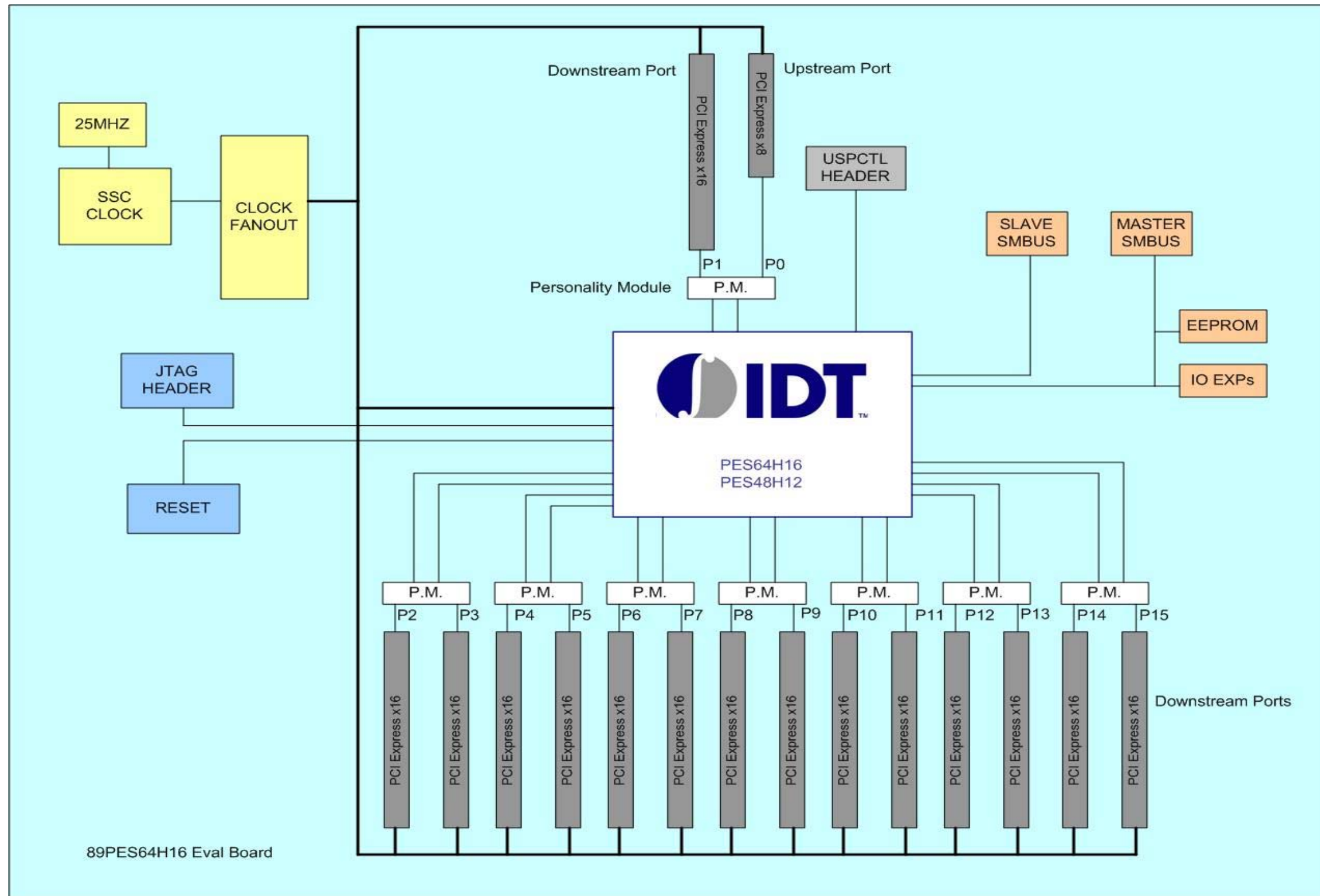


Schematics

Notes

Schematics

BLOCK DIAGRAM



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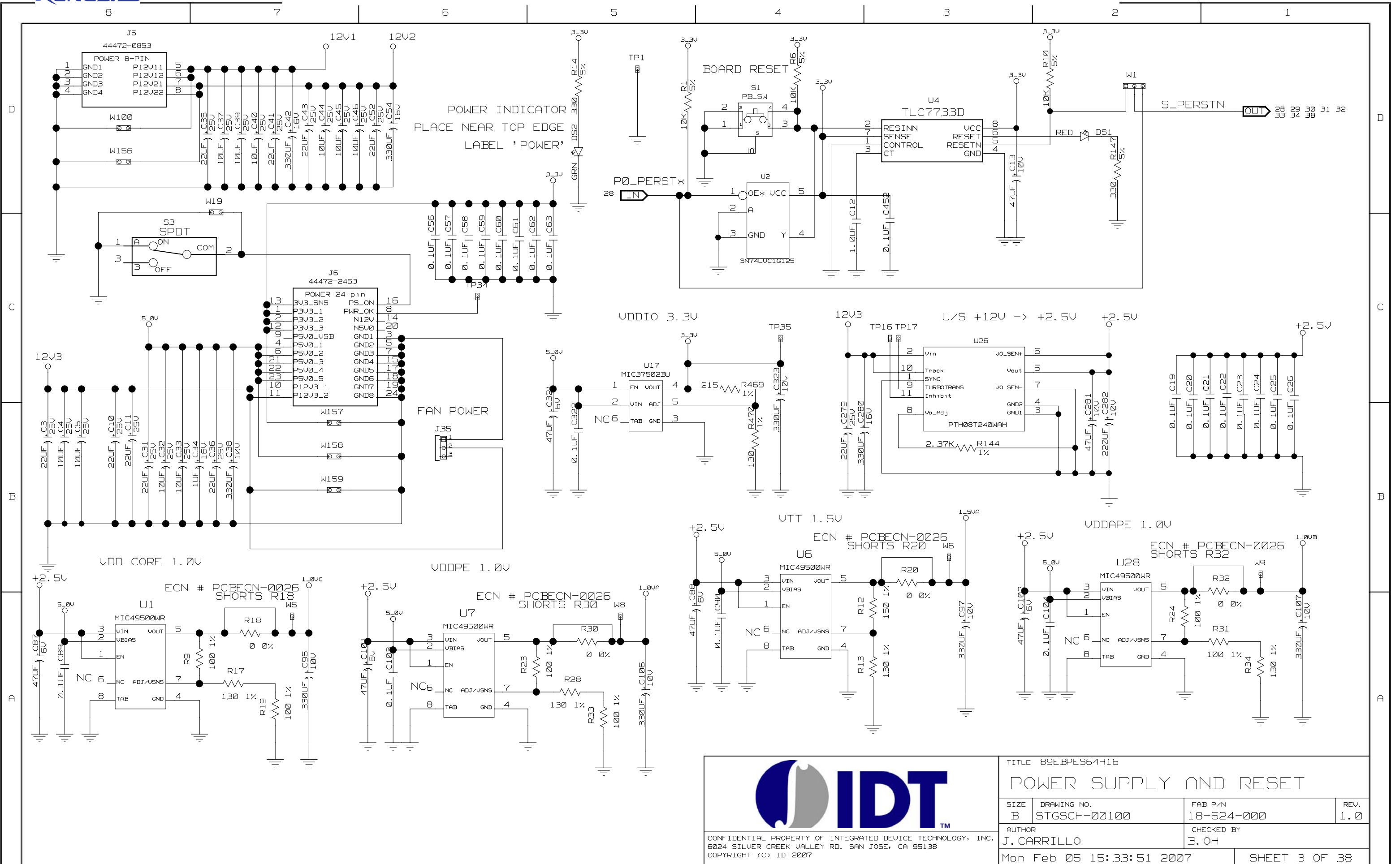
BLOCK DIAGRAM

SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
-----------	-----------------------------	-----------------------	-------------

AUTHOR J. CARRILLO	CHECKED BY B. OH
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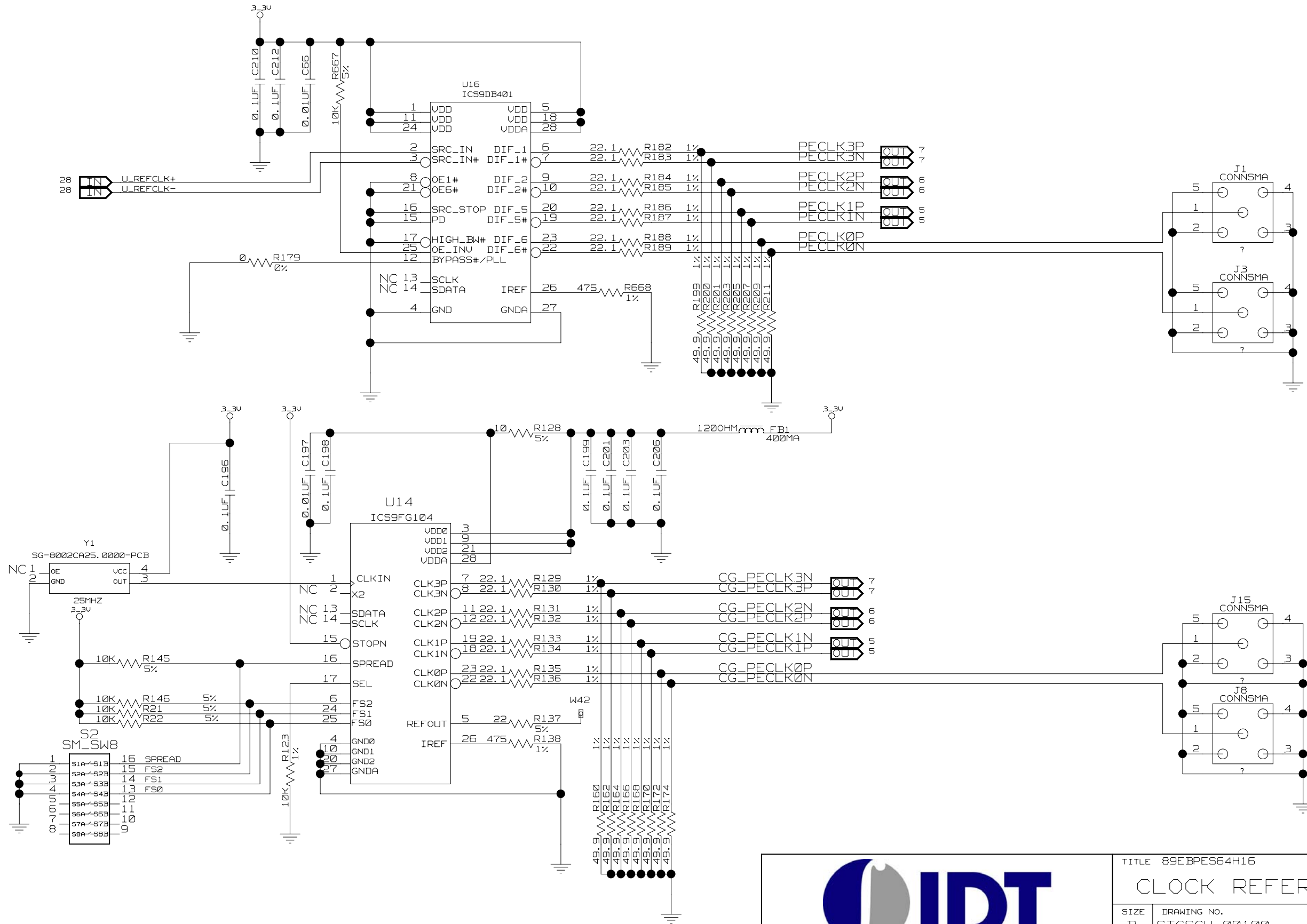
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POWER SUPPLY AND RESET			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0
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J. CARRILLO		B. OH	
Mon Feb 05 15:33:51 2007			SHEET 3 OF 38

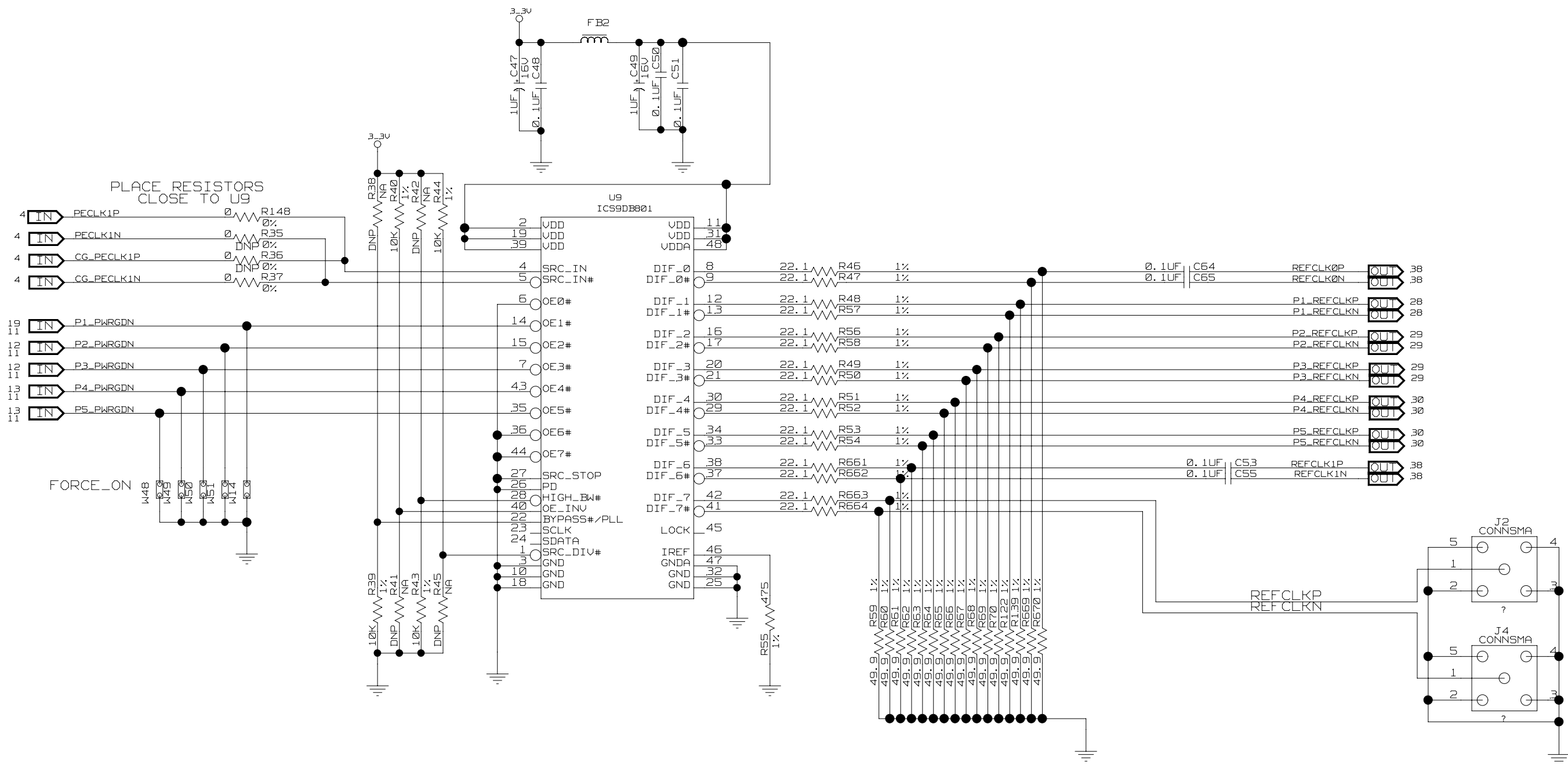


		TITLE 89EBPES64H16		
		CLOCK REFERENCE		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00100	18-624-000	1.0	
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8 7 6 5 4 3 2 1



		TITLE 89EBPES64H16		
		CLOCK DISTRIBUTION P1-5		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0	
AUTHOR J. CARRILLO		CHECKED BY B. OH		
Mon Feb 05 15:33:53 2007			SHEET 5 OF 38	

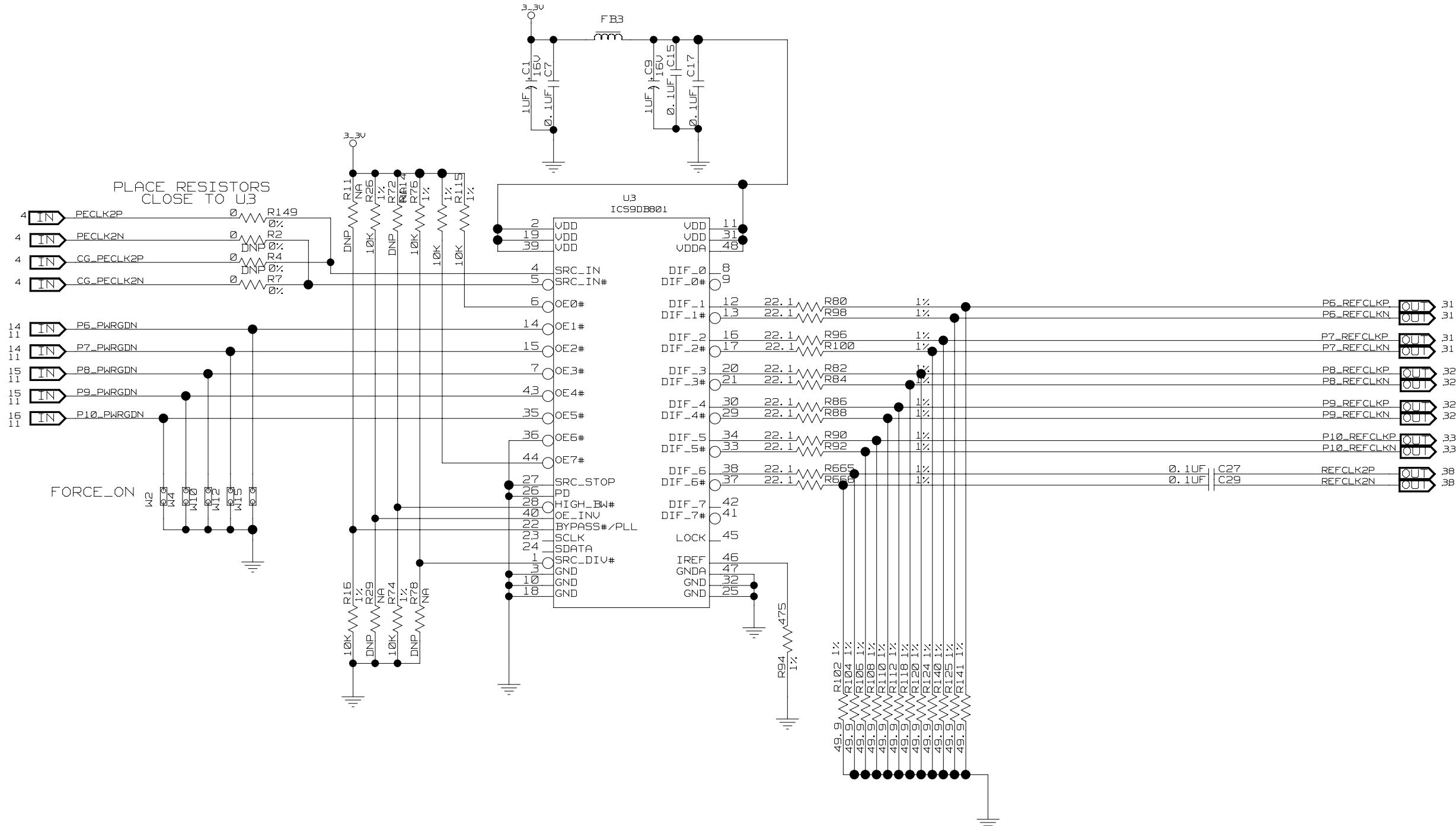
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6 5 4 3 2 1



8 7 6 5 4 3 2 1

D
C
B
A



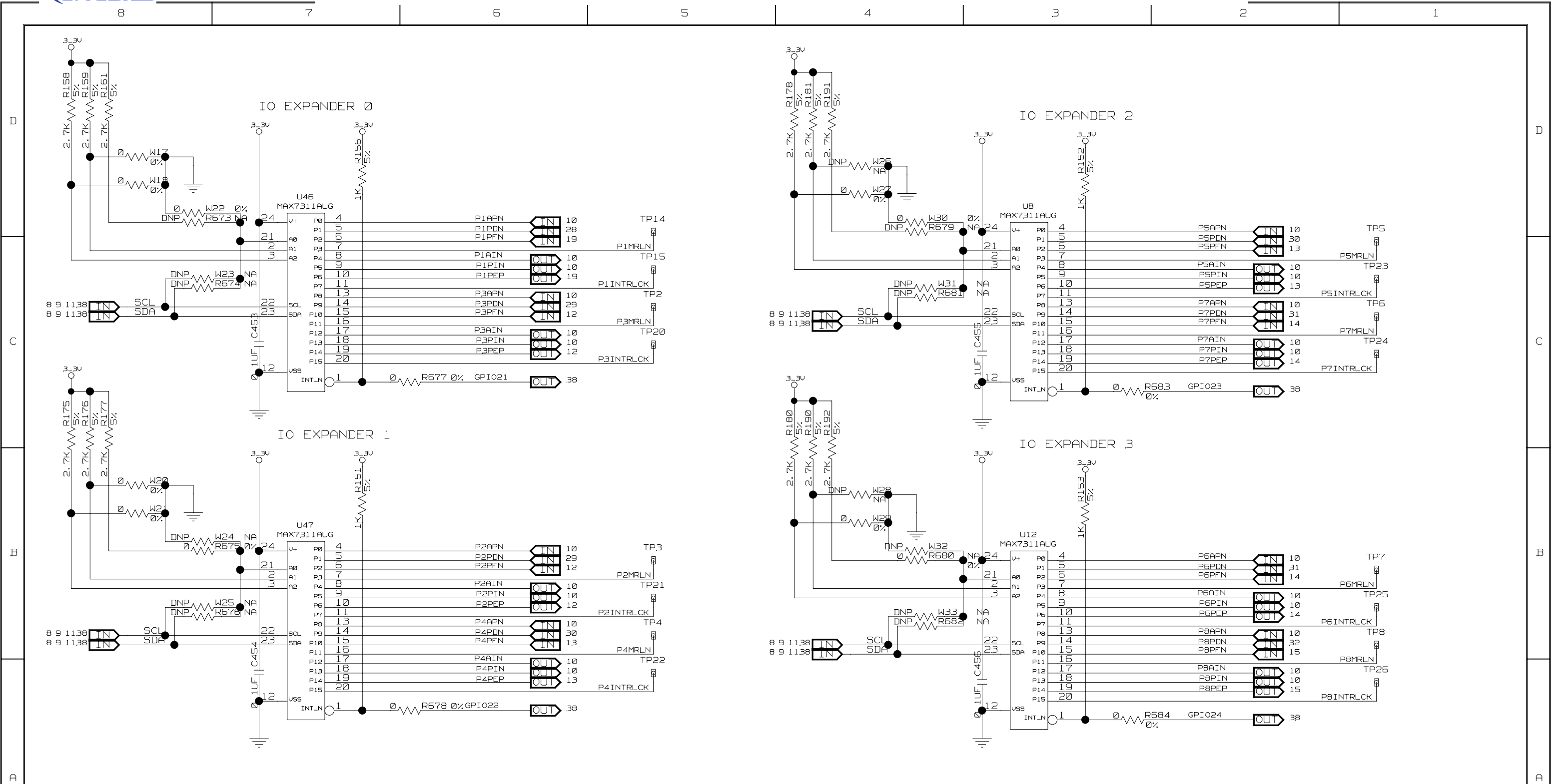
PLACE RESISTORS CLOSE TO U3

FORCE_ON

		TITLE 89EBPES64H16		
		CLOCK DISTRIBUTION P6-10		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0	
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Mon Feb 05 15:33:53 2007			SHEET 6 OF 38	

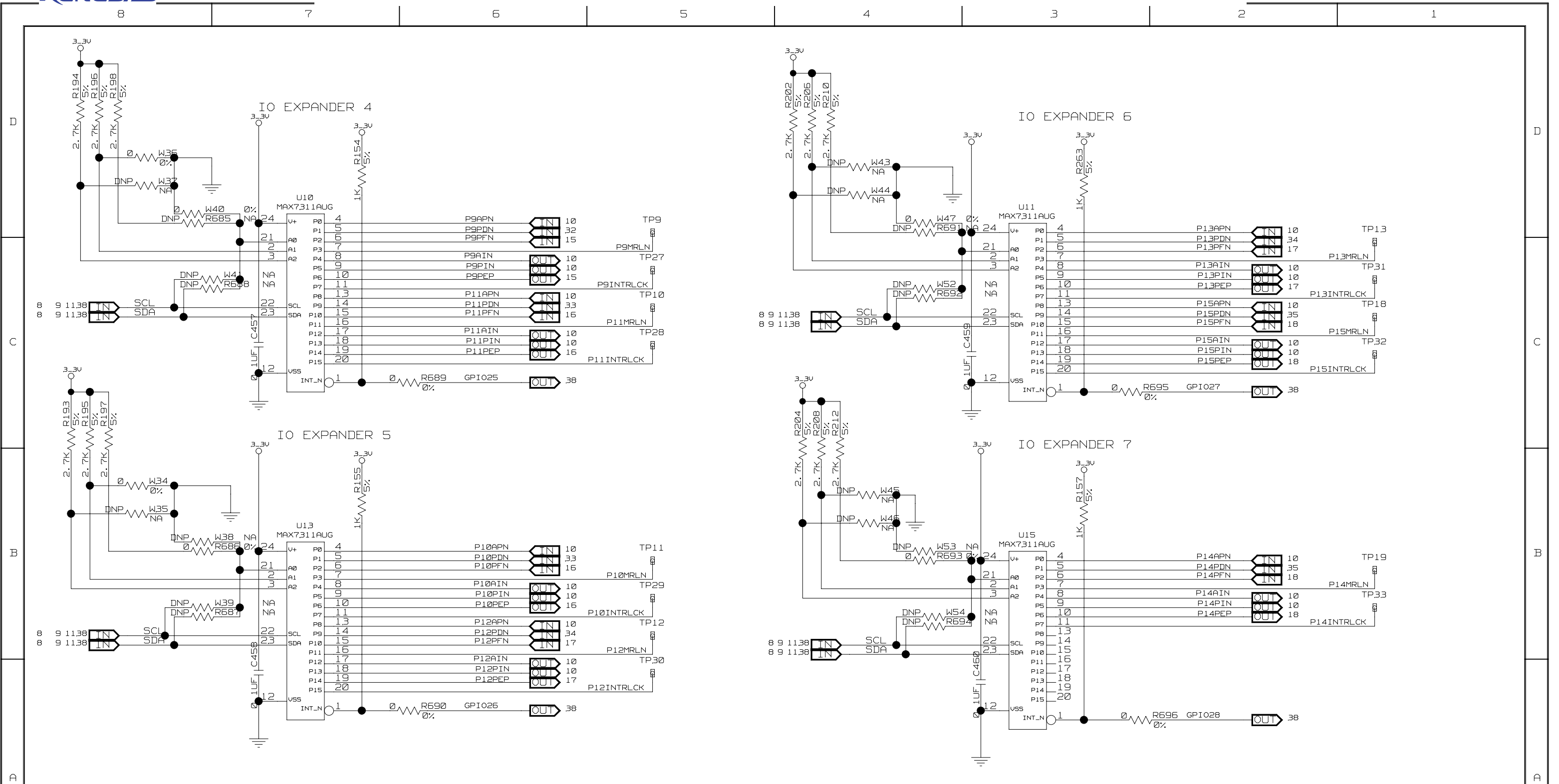
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6 5 4 3 2 1



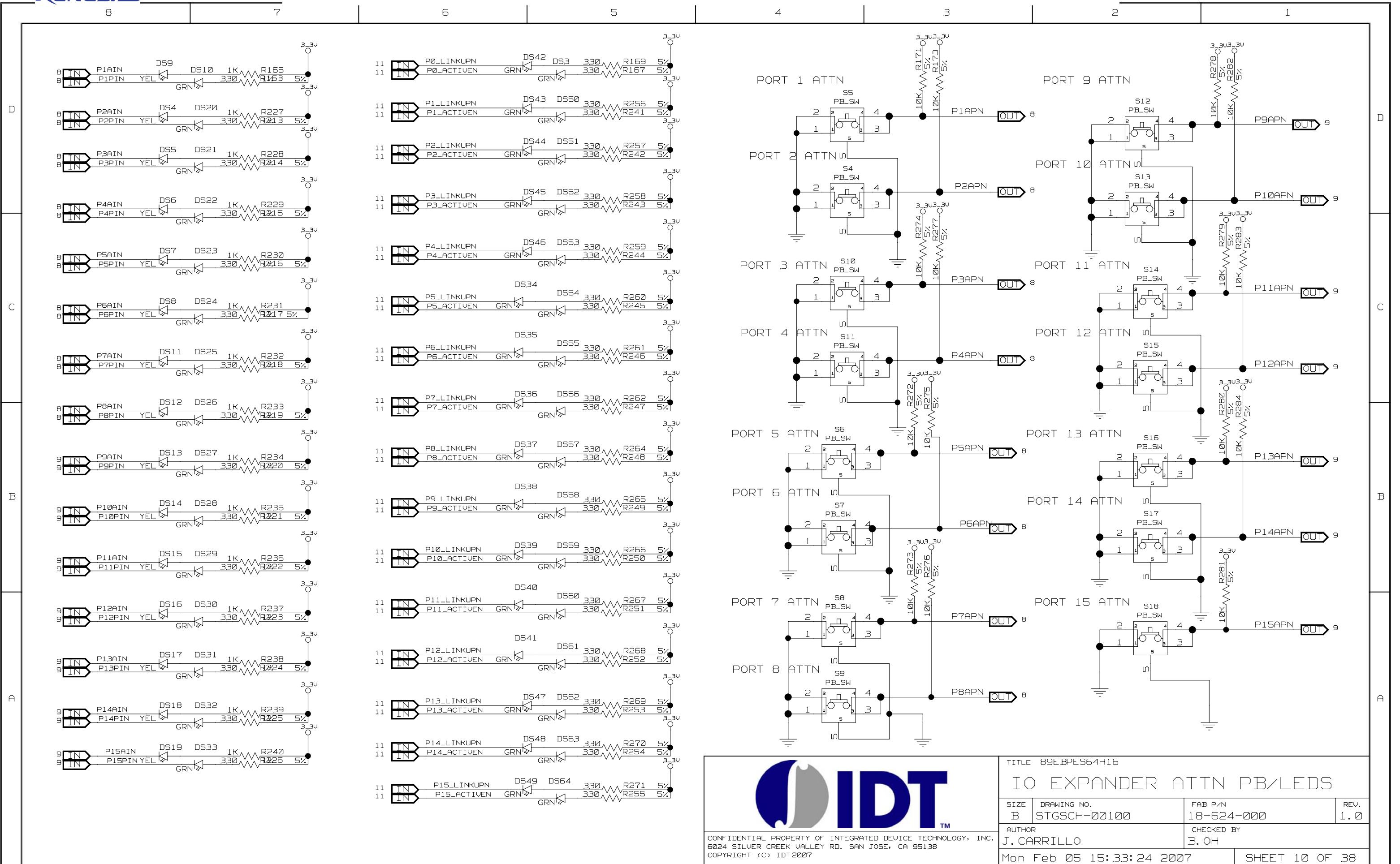
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TITLE 89EBPES64H16			
IO EXPANDER P1 - P8			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0
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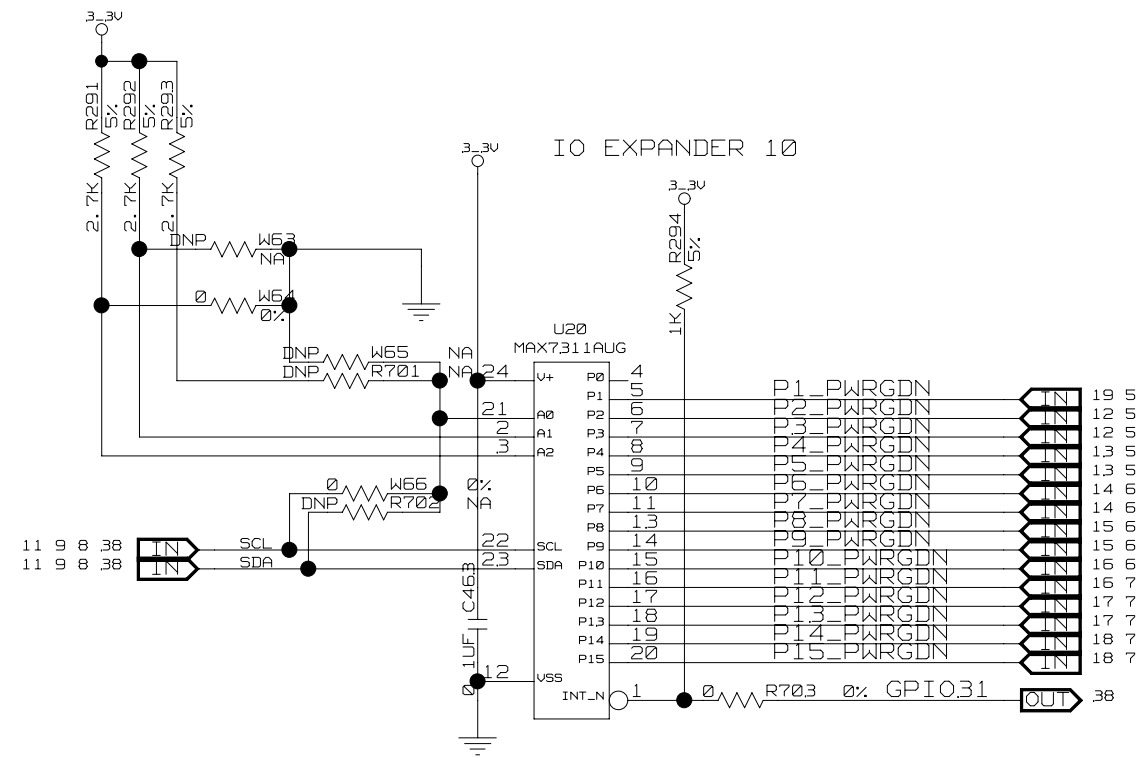
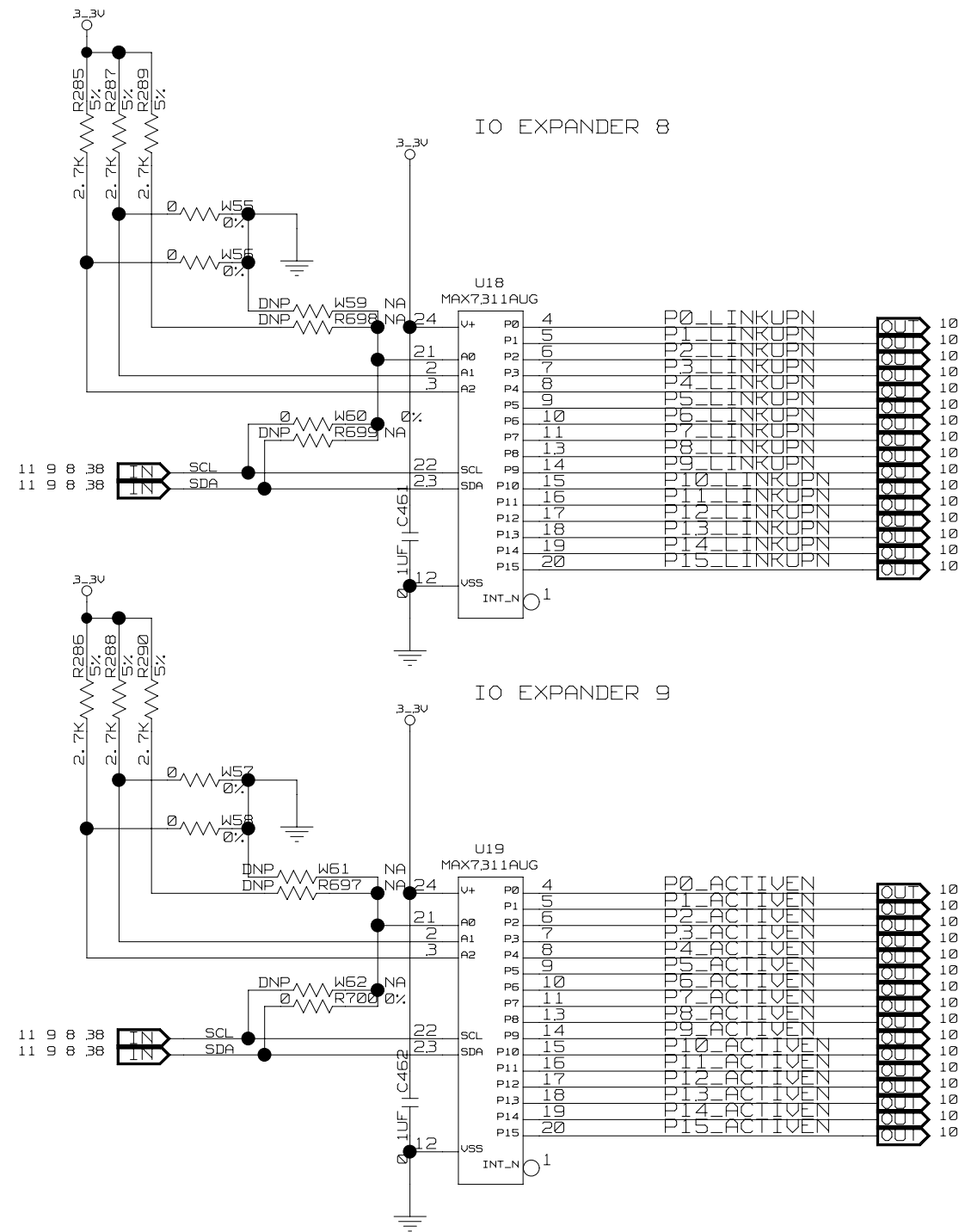
		TITLE 89EBPES64H16		
		IO EXPANDER P9 - P15		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00100	18-624-000	1.0	
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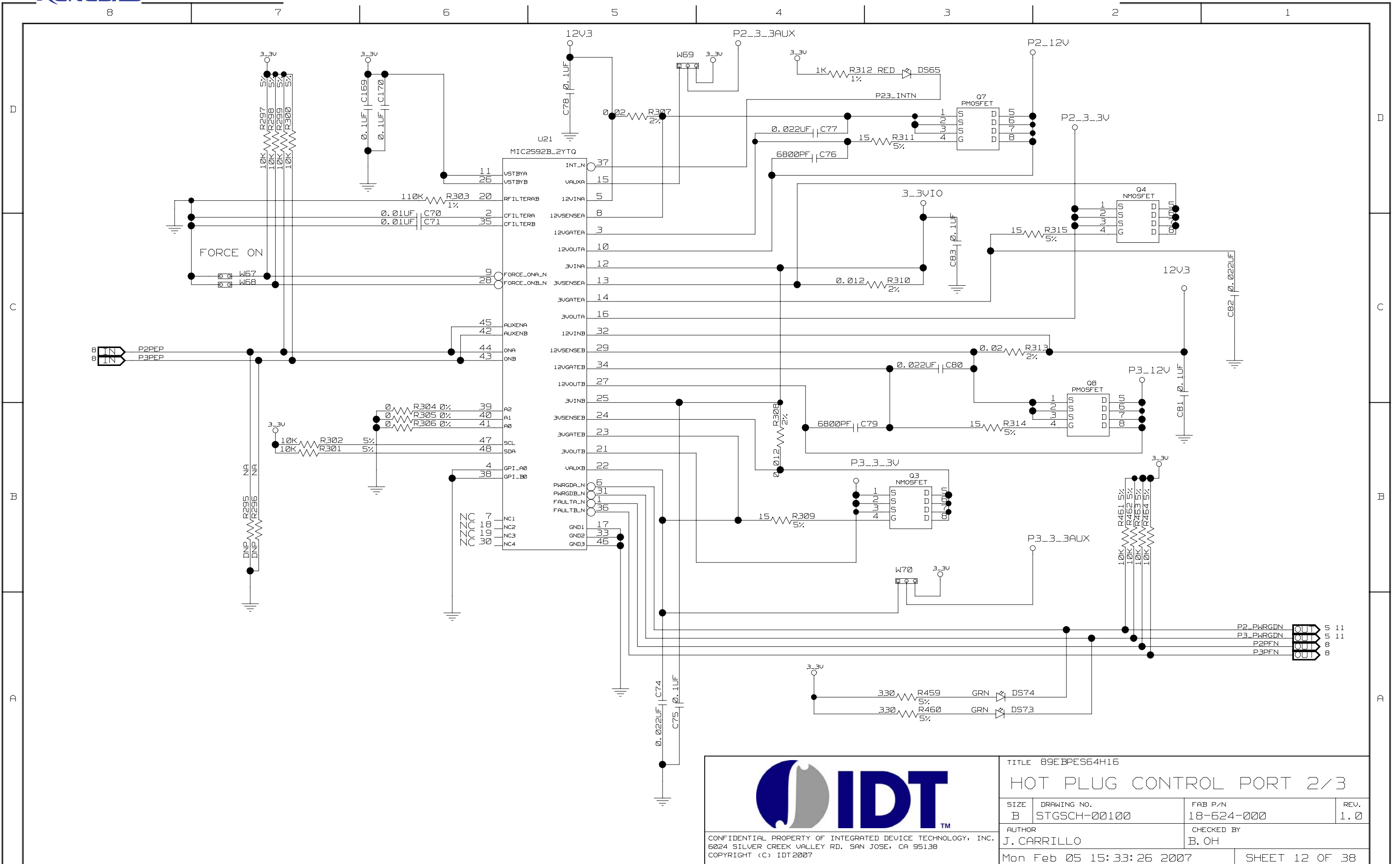
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IO EXPANDER ATTN PB/LEDS			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
Mon Feb 05 15:33:24 2007			SHEET 10 OF 38



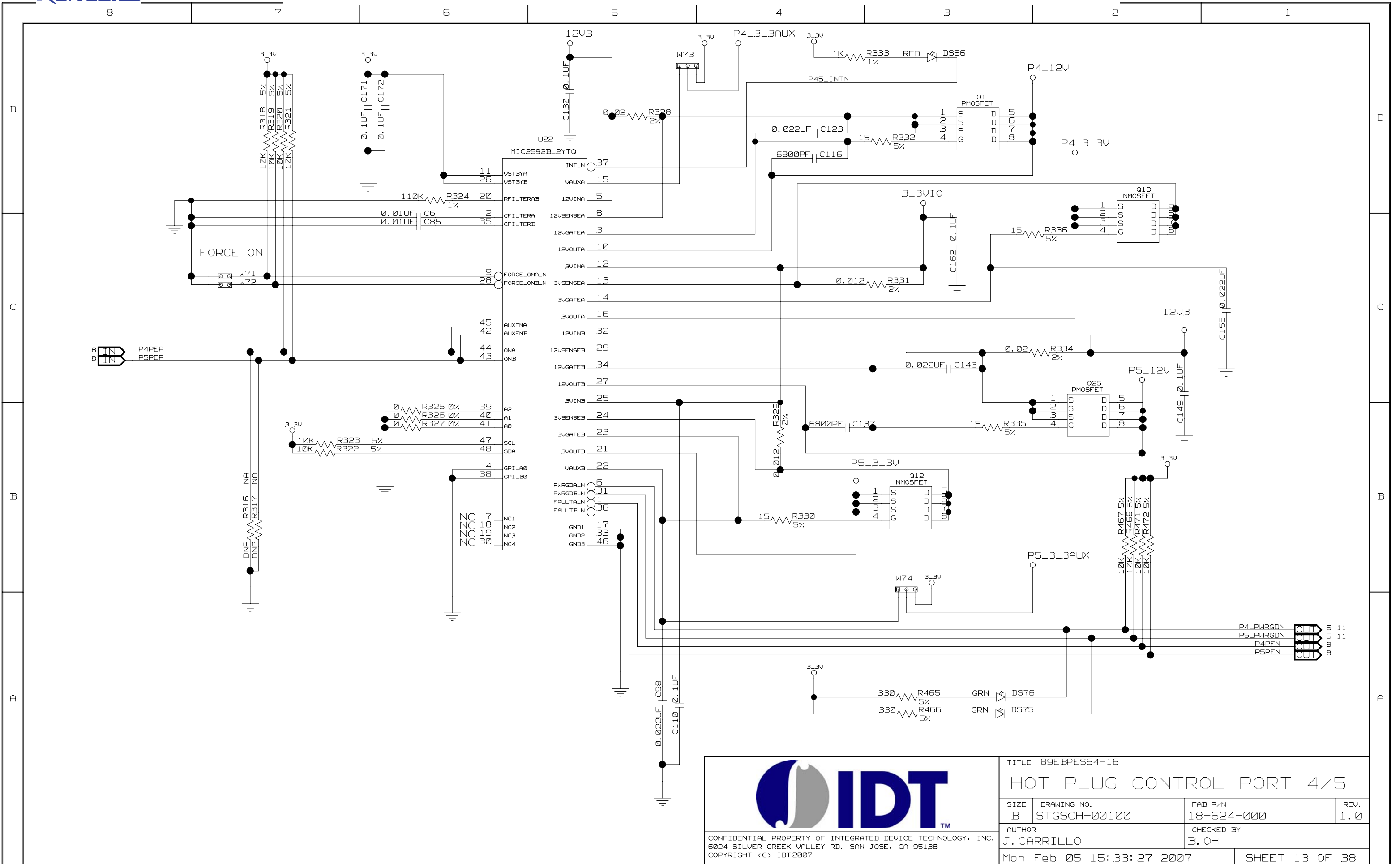
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IO EXPANDER LINK STATUS			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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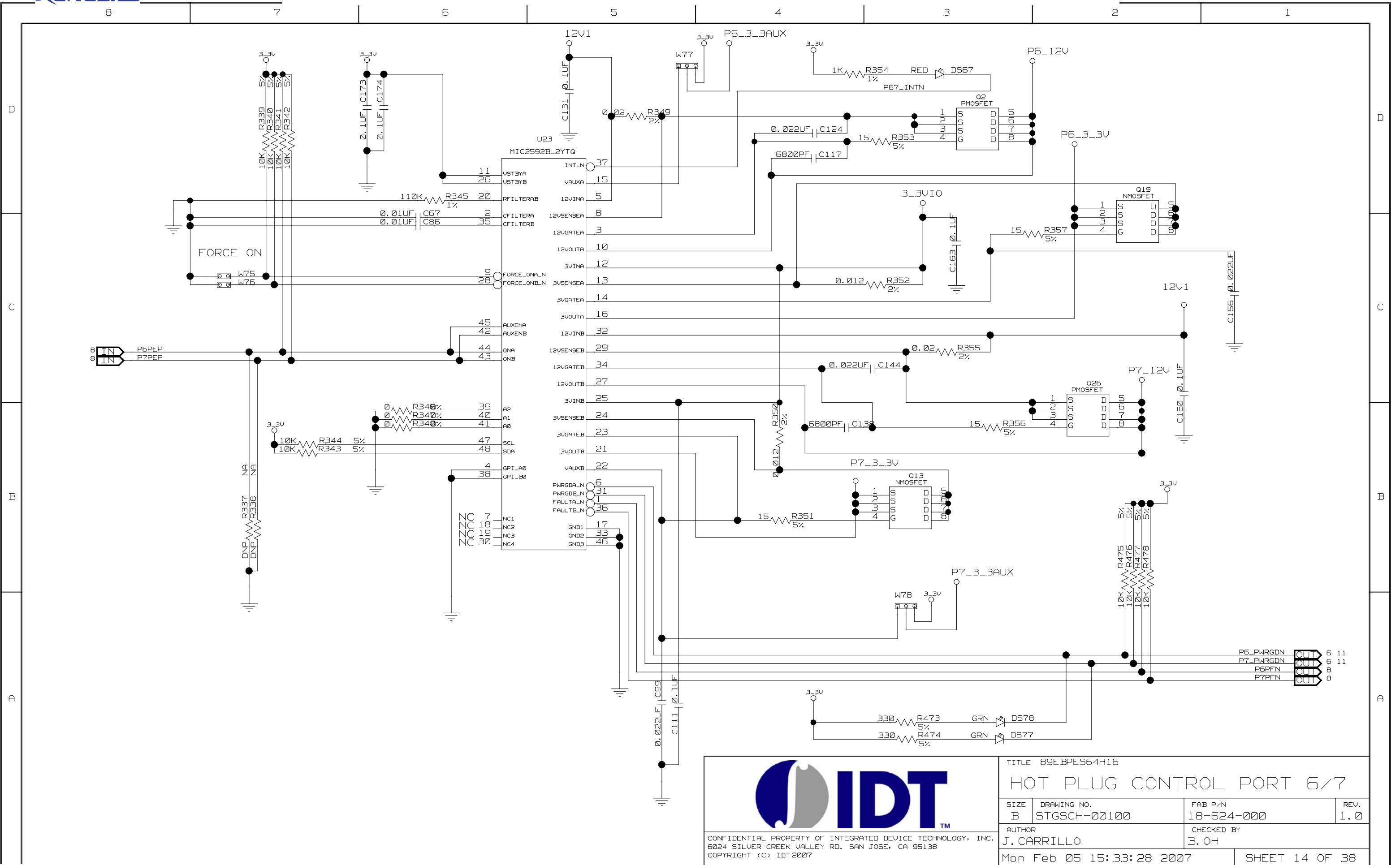
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HOT PLUG CONTROL PORT 2/3			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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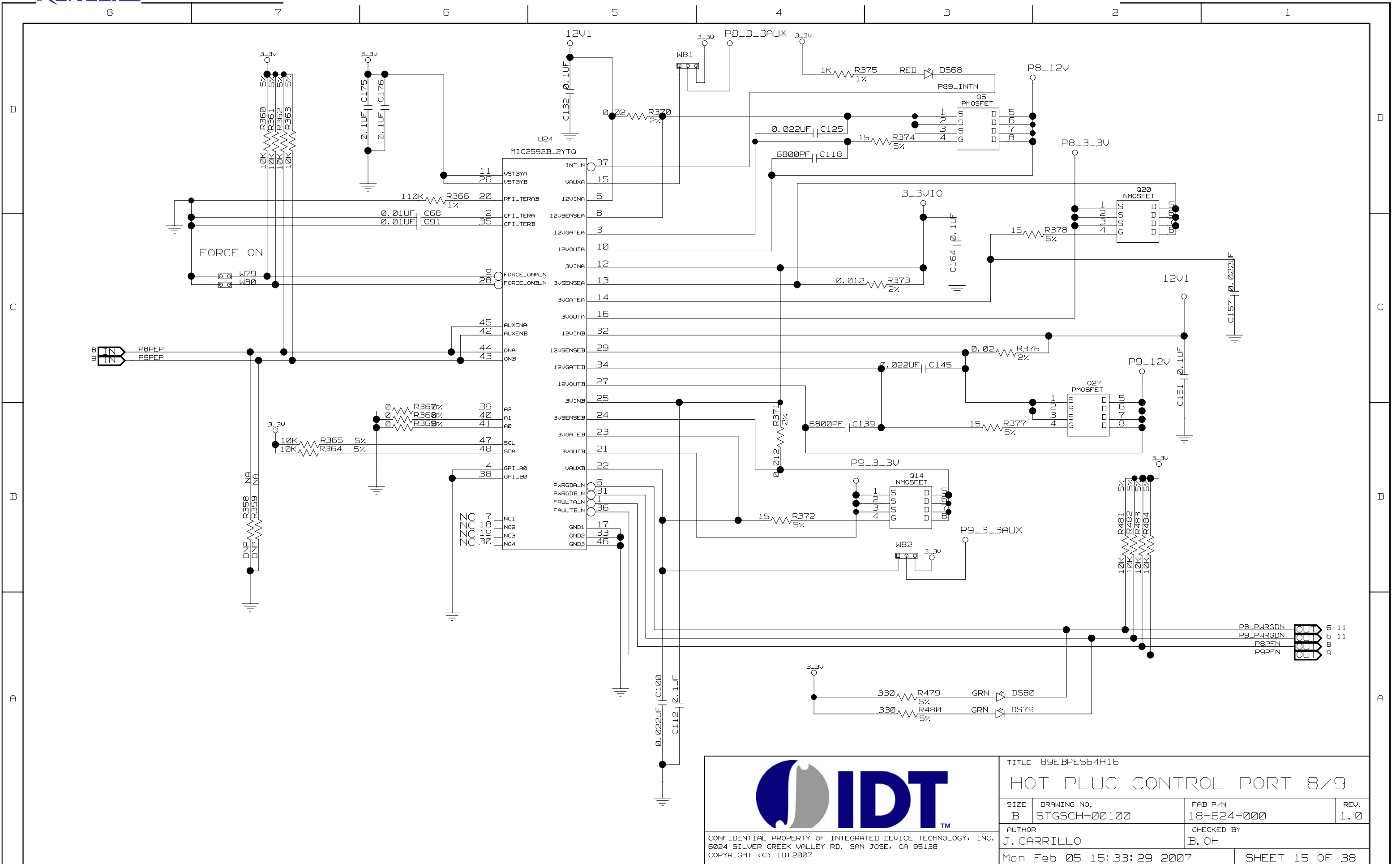
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TITLE 89EBPES64H16			
HOT PLUG CONTROL PORT 4/5			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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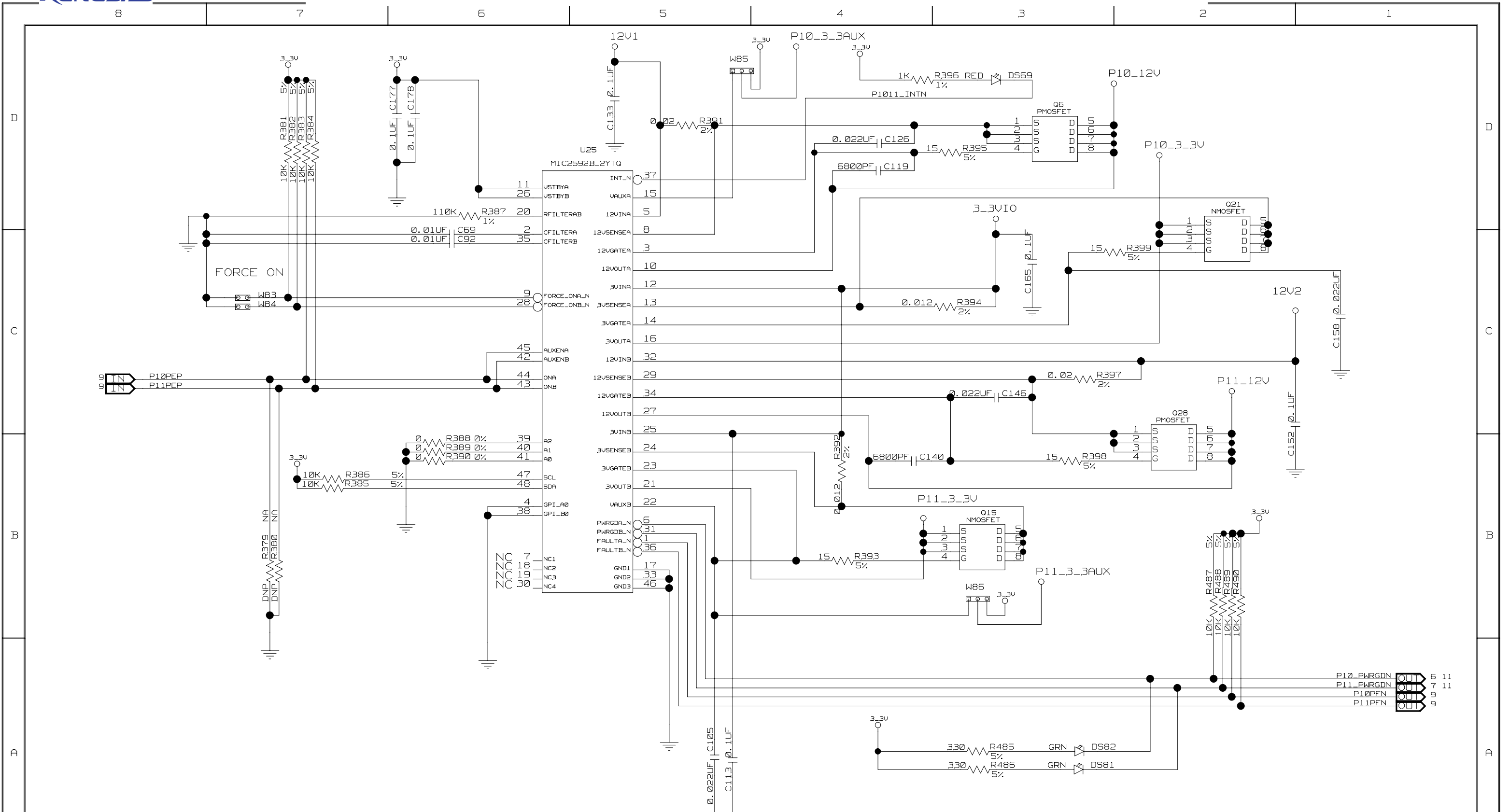


		TITLE 89EBPES64H16		
		HOT PLUG CONTROL PORT 6/7		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00100	18-624-000	1.0	
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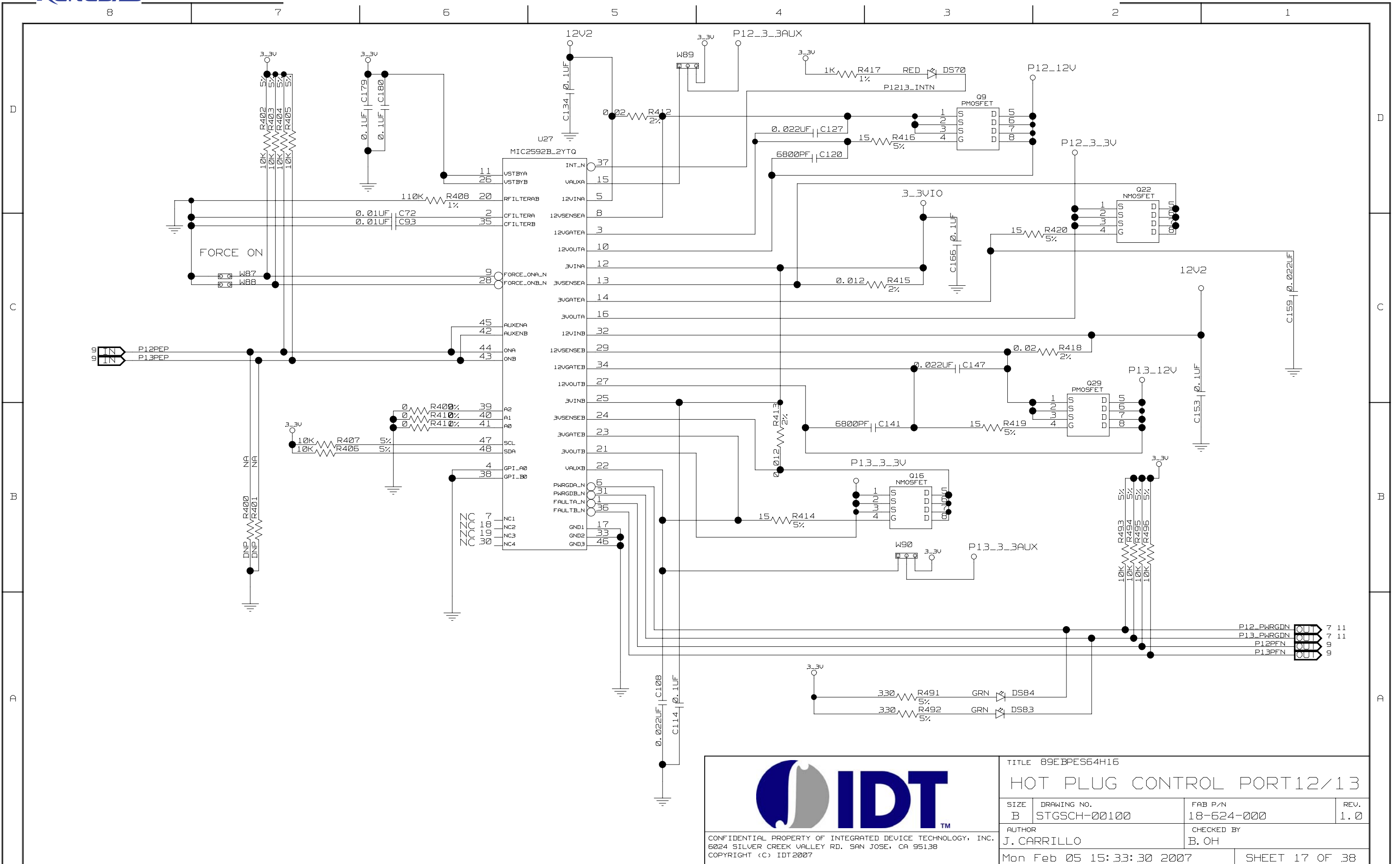


		TITLE 89EBPES64H16	
		HOT PLUG CONTROL PORT 8/9	
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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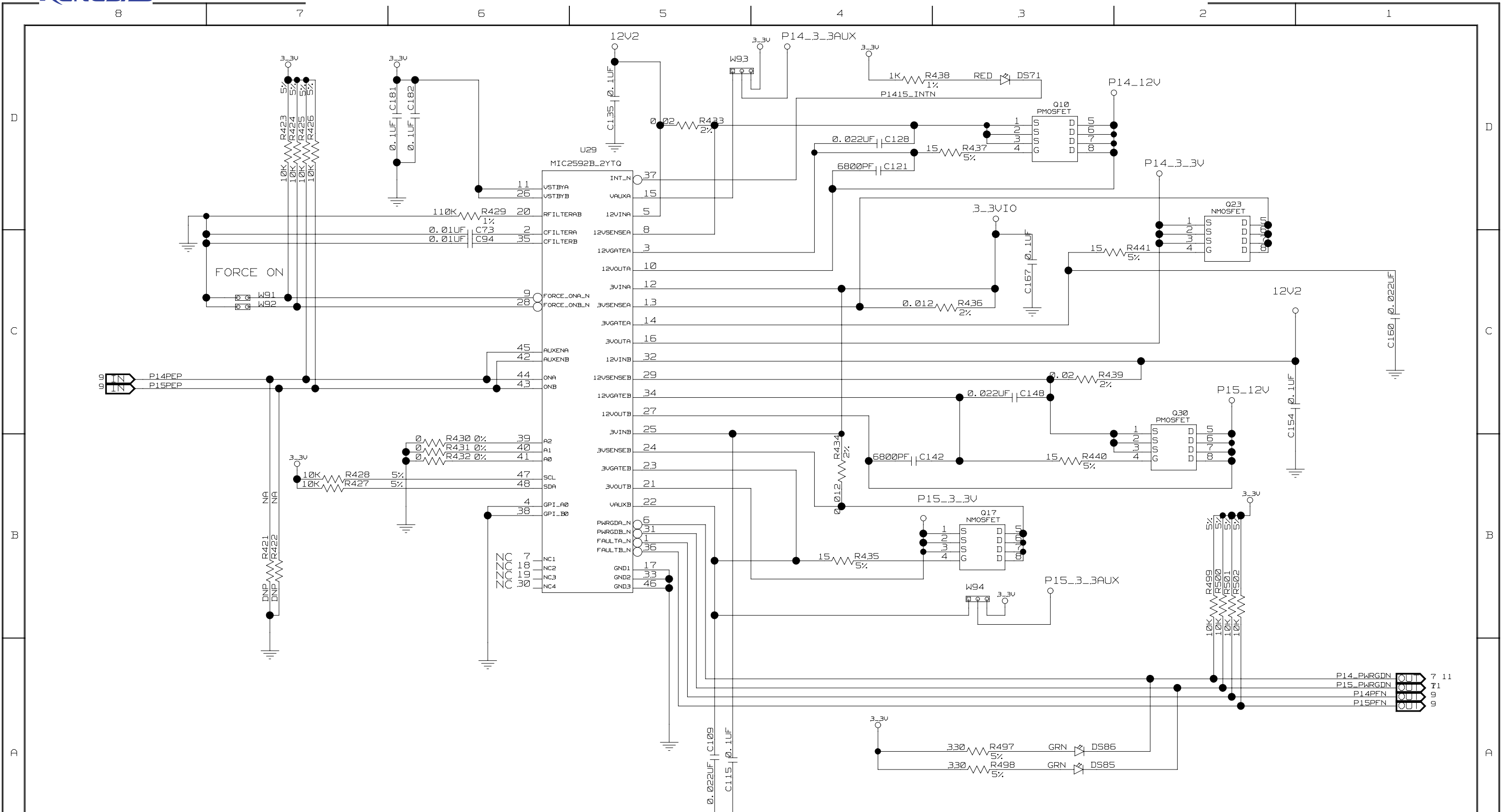
		TITLE 89EBPES64H16		
		HOT PLUG CONTROL PORT10/11		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00100	18-624-000	1.0	
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		TITLE 89EBPES64H16		
		HOT PLUG CONTROL PORT12/13		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0	
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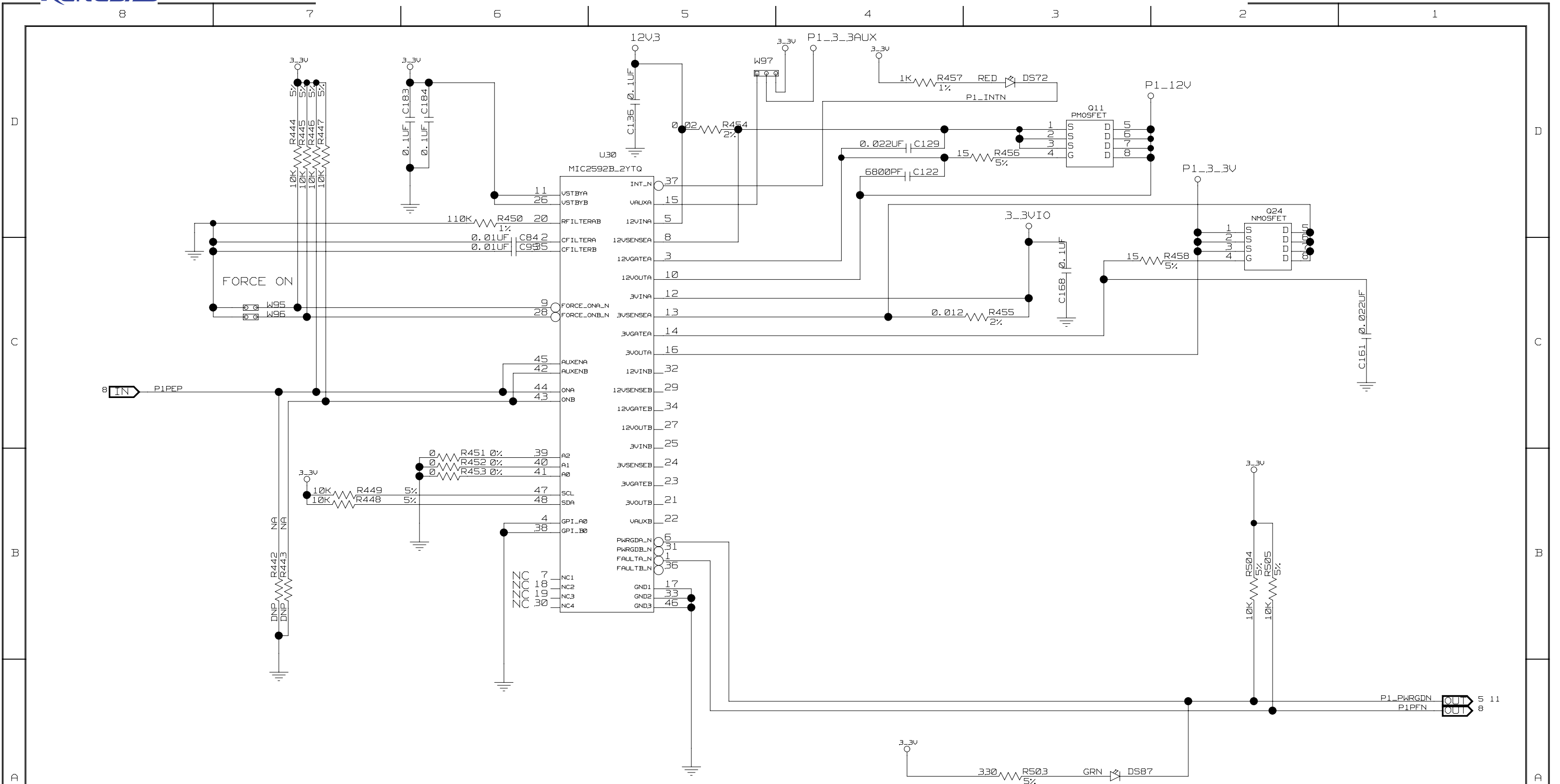




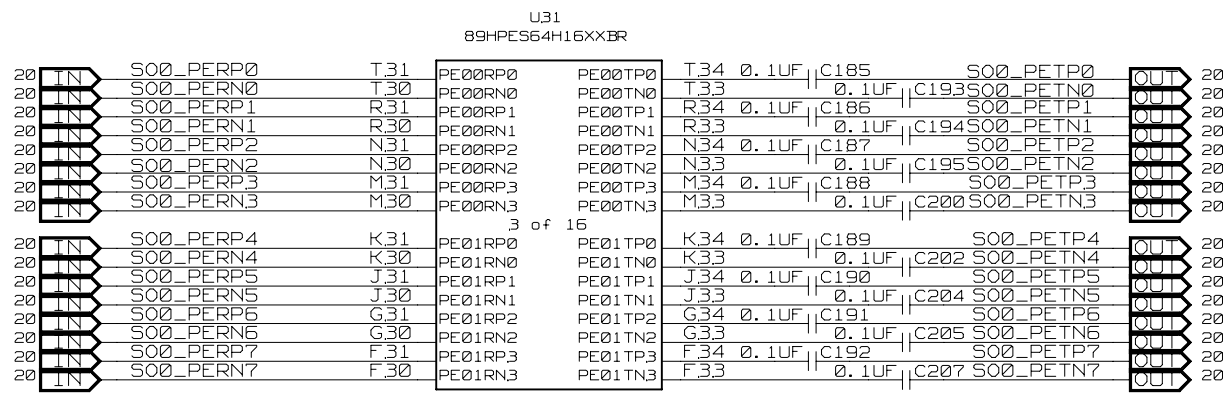
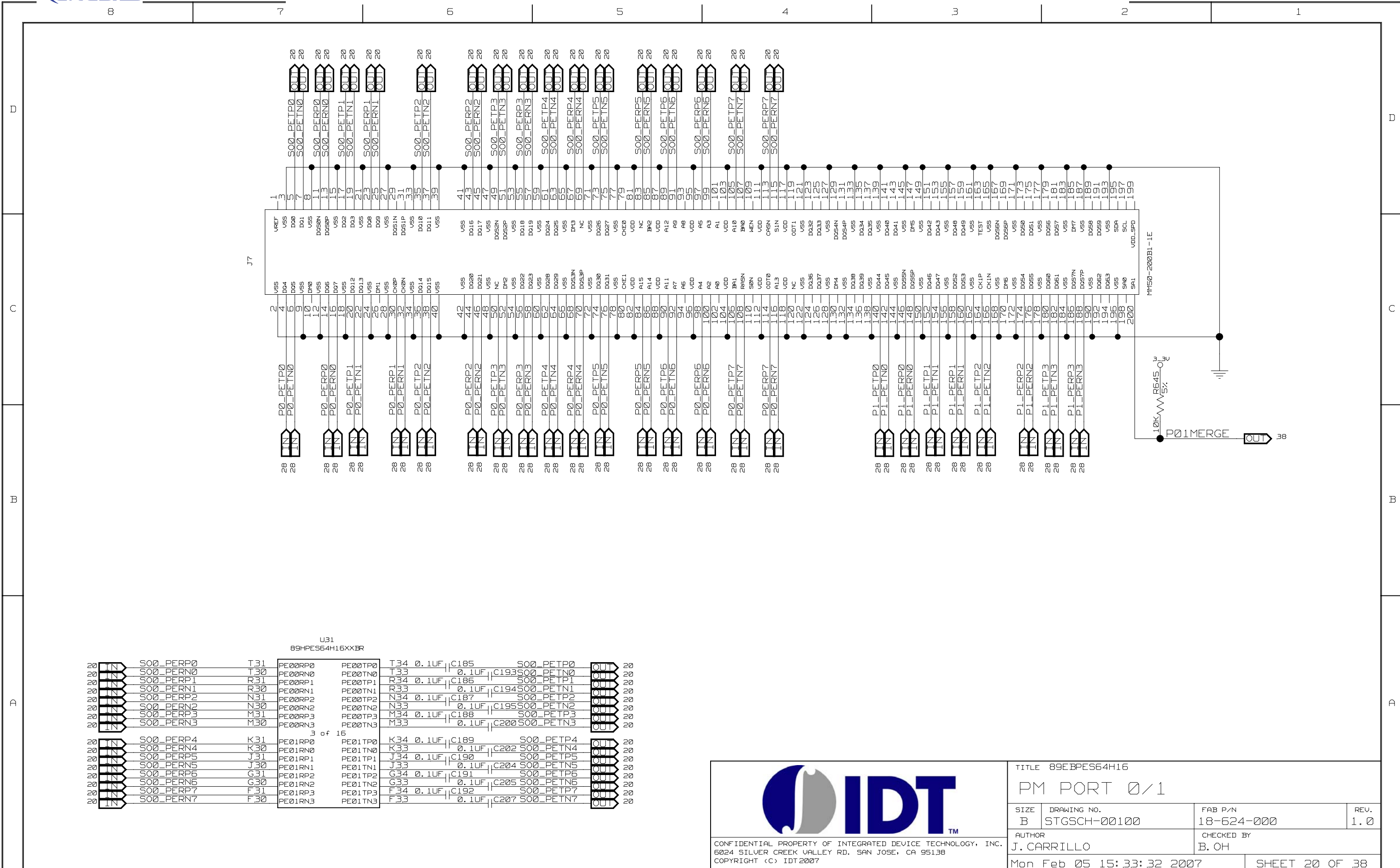
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HOT PLUG CONTROL PORT14/15

SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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Mon Feb 05 15:33:31 2007			SHEET 18 OF 38

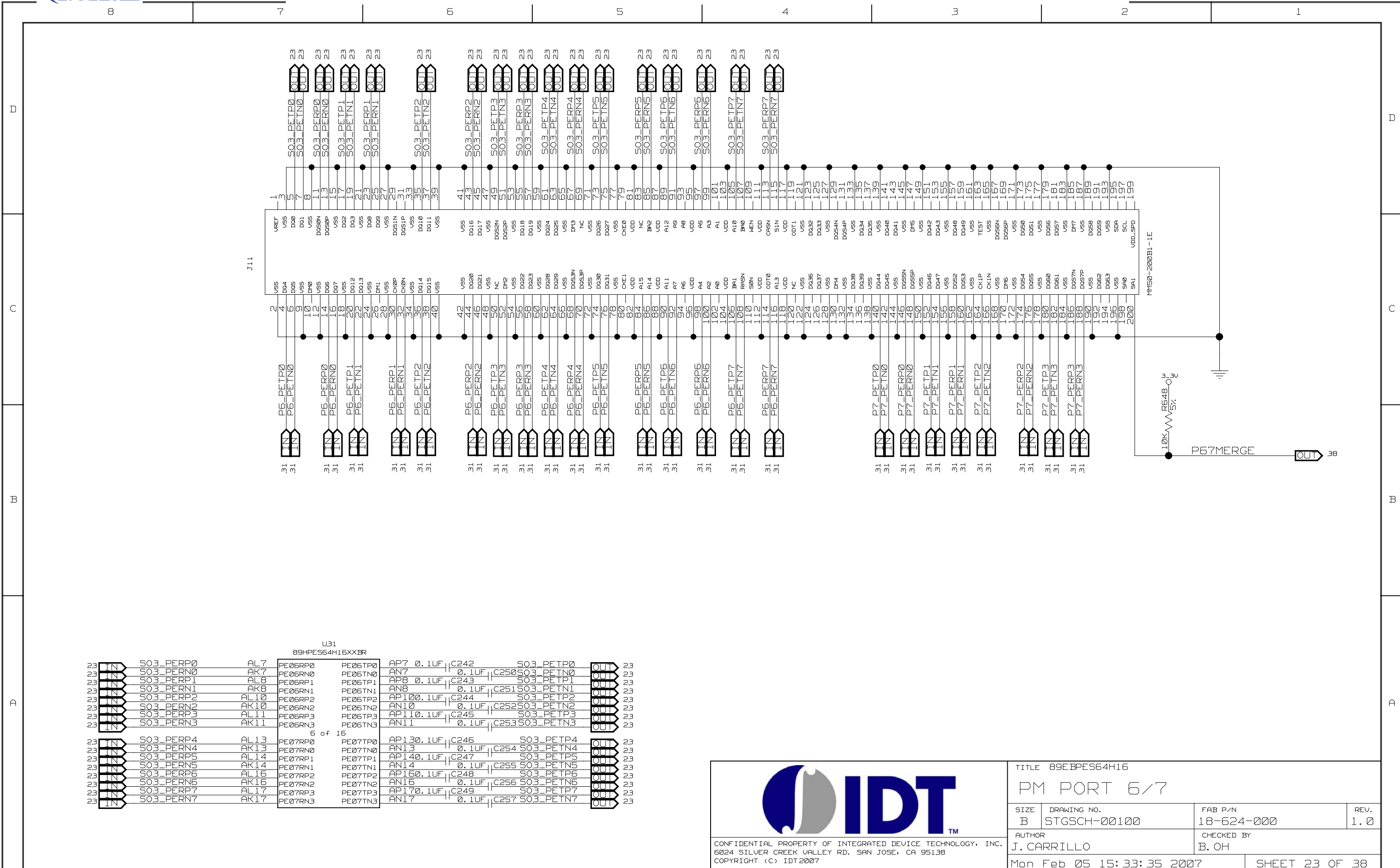


		TITLE 89EBPES64H16	
		HOT PLUG CONTROL PORT 1	
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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TITLE 89EBPES64H16			
PM PORT 0/1			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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Mon Feb 05 15:33:32 2007			SHEET 20 OF 38

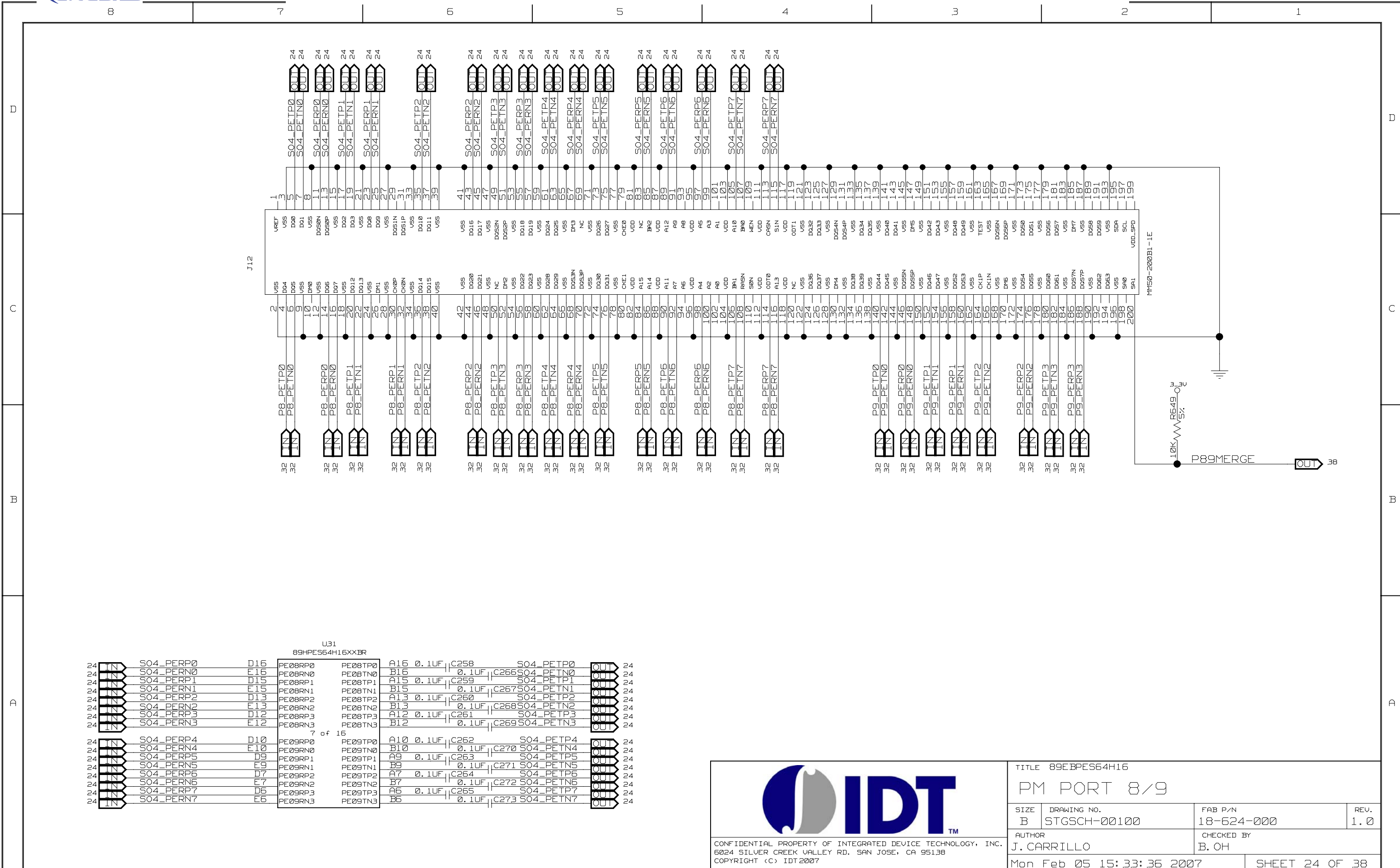


U31
89HPE64H16XXBR

23	S03_PERP0	AL7	PE06RP0	PE06TP0	AP7 0.1UF C242	S03_PETP0	23
23	S03_PERN0	AK7	PE06RN0	PE06TN0	AN7 0.1UF C250	S03_PETN0	23
23	S03_PERP1	AL8	PE06RP1	PE06TP1	AP8 0.1UF C243	S03_PETP1	23
23	S03_PERN1	AK8	PE06RN1	PE06TN1	AN8 0.1UF C251	S03_PETN1	23
23	S03_PERP2	AL10	PE06RP2	PE06TP2	AP10 0.1UF C244	S03_PETP2	23
23	S03_PERN2	AK10	PE06RN2	PE06TN2	AN10 0.1UF C252	S03_PETN2	23
23	S03_PERP3	AL11	PE06RP3	PE06TP3	AP11 0.1UF C245	S03_PETP3	23
23	S03_PERN3	AK11	PE06RN3	PE06TN3	AN11 0.1UF C253	S03_PETN3	23
6 of 16							
23	S03_PERP4	AL13	PE07RP0	PE07TP0	AP13 0.1UF C246	S03_PETP4	23
23	S03_PERN4	AK13	PE07RN0	PE07TN0	AN13 0.1UF C254	S03_PETN4	23
23	S03_PERP5	AL14	PE07RP1	PE07TP1	AP14 0.1UF C247	S03_PETP5	23
23	S03_PERN5	AK14	PE07RN1	PE07TN1	AN14 0.1UF C255	S03_PETN5	23
23	S03_PERP6	AL15	PE07RP2	PE07TP2	AP15 0.1UF C248	S03_PETP6	23
23	S03_PERN6	AK15	PE07RN2	PE07TN2	AN15 0.1UF C256	S03_PETN6	23
23	S03_PERP7	AL17	PE07RP3	PE07TP3	AP17 0.1UF C249	S03_PETP7	23
23	S03_PERN7	AK17	PE07RN3	PE07TN3	AN17 0.1UF C257	S03_PETN7	23

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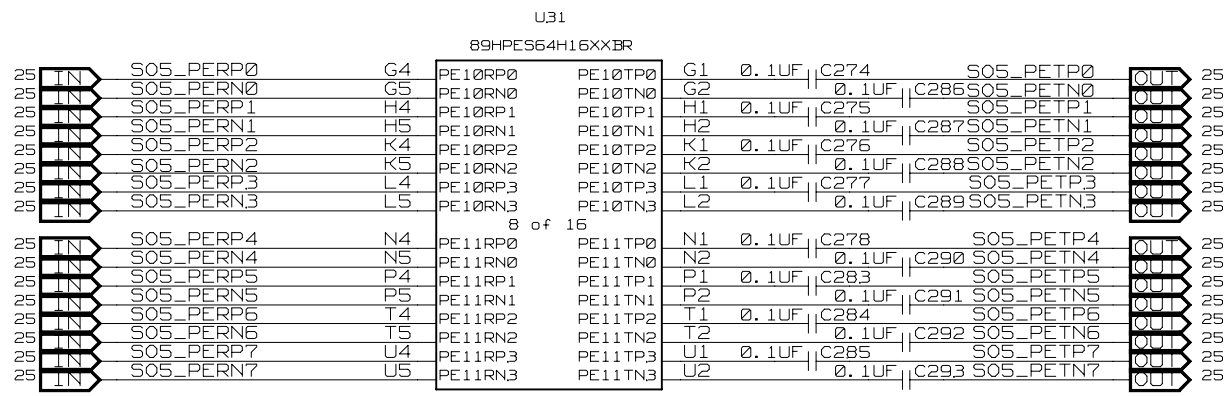
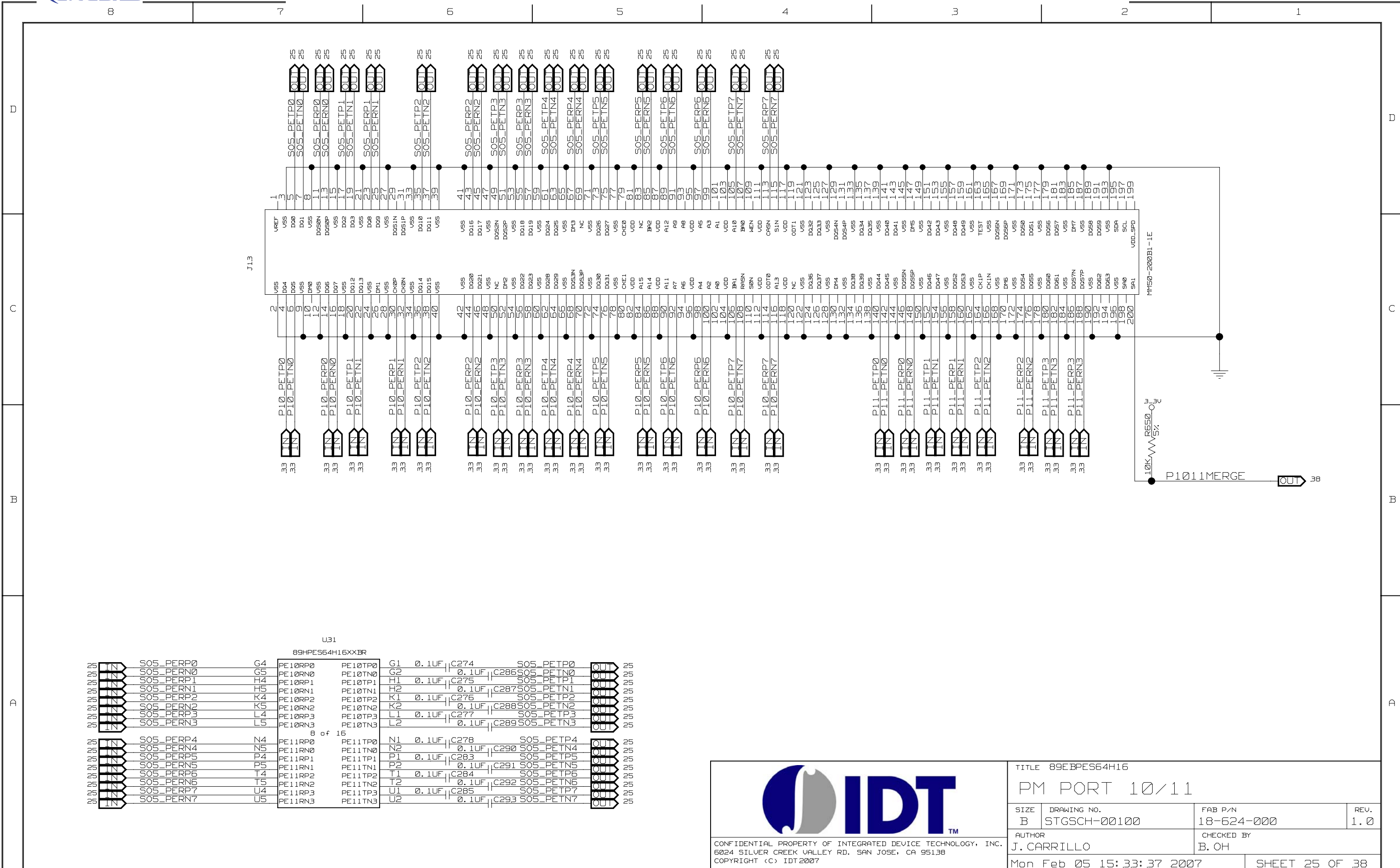
TITLE 89EBPES64H16			
PM PORT 6/7			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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U31		89HPE64H16XXBR	
24	SO4_PERP0	D16	PE08RP0
24	SO4_PERN0	E16	PE08RN0
24	SO4_PERP1	D15	PE08RP1
24	SO4_PERN1	E15	PE08RN1
24	SO4_PERP2	D13	PE08RP2
24	SO4_PERN2	E13	PE08RN2
24	SO4_PERP3	D12	PE08RP3
24	SO4_PERN3	E12	PE08RN3
7 of 16			
24	SO4_PERP4	D10	PE09RP0
24	SO4_PERN4	E10	PE09RN0
24	SO4_PERP5	D9	PE09RP1
24	SO4_PERN5	E9	PE09RN1
24	SO4_PERP6	D7	PE09RP2
24	SO4_PERN6	E7	PE09RN2
24	SO4_PERP7	D6	PE09RP3
24	SO4_PERN7	E6	PE09RN3

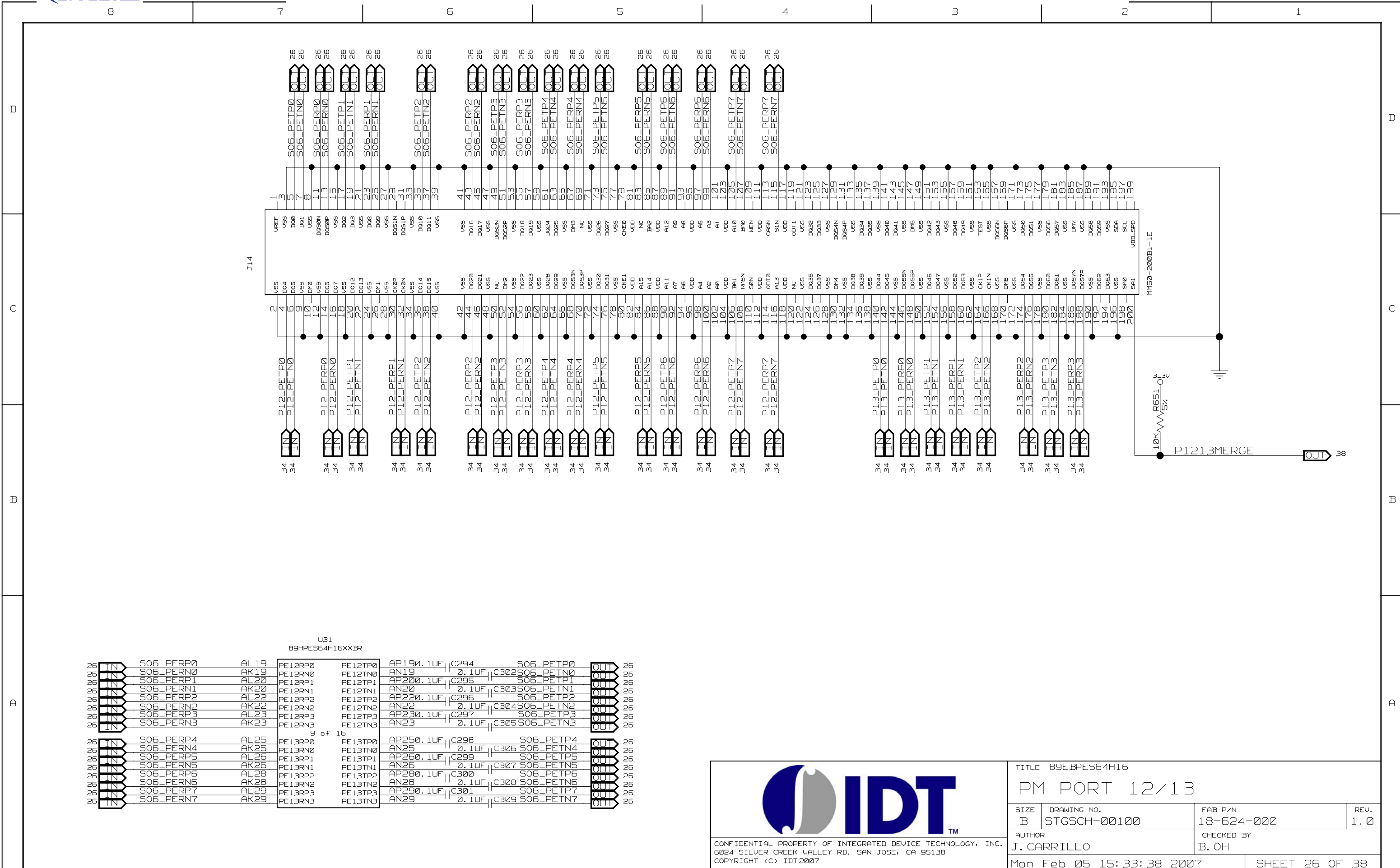
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PM PORT 8/9			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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PM PORT 10/11			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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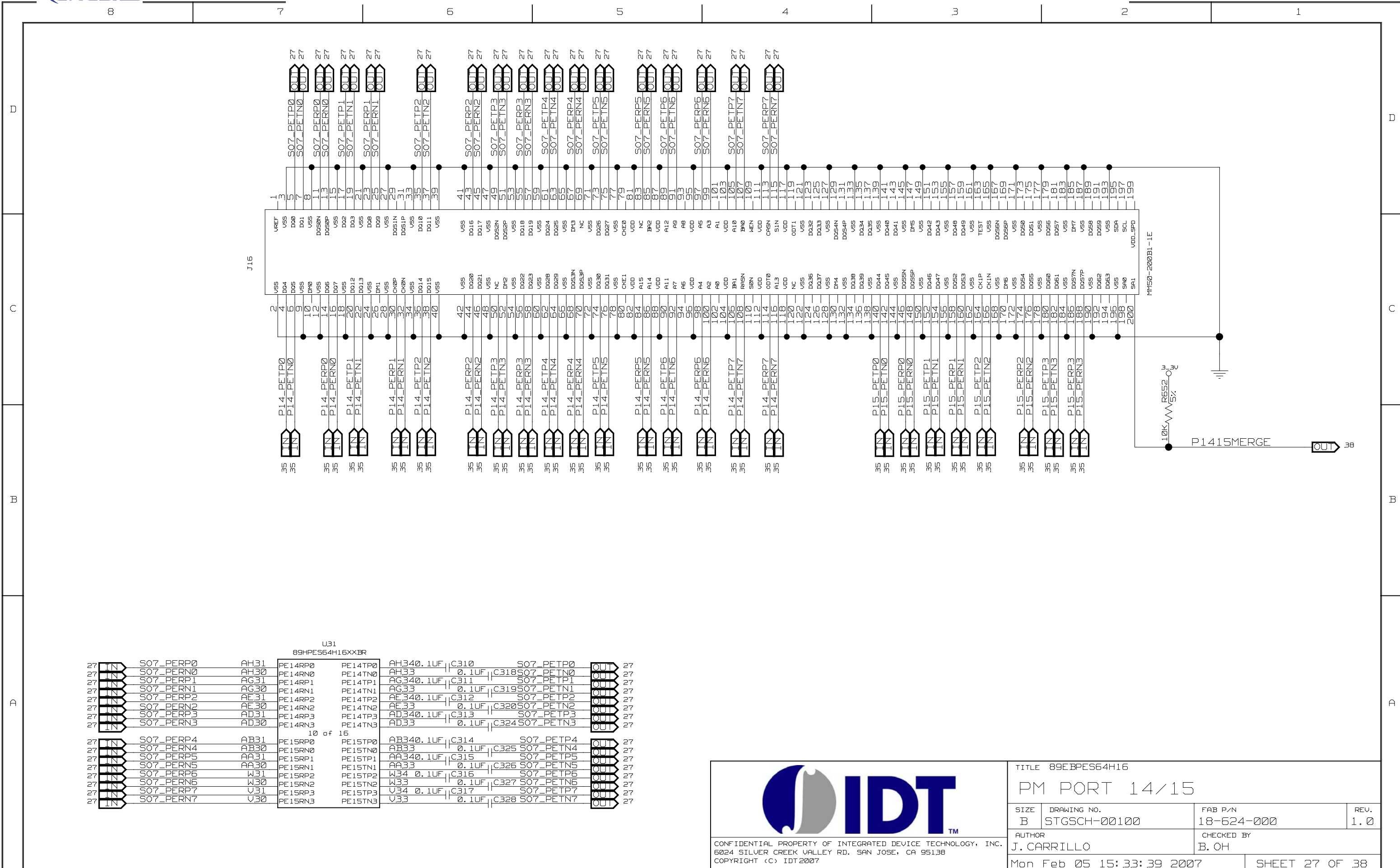


U31
89HPES64H16XXBR

26	S06_PERP0	AL19	PE12RP0	PE12TP0	AP190.1UF	C294	S06_PETP0	26
26	S06_PERN0	AK19	PE12RN0	PE12TN0	AN19	0.1UF	S06_PETN0	26
26	S06_PERP1	AL20	PE12RP1	PE12TP1	AP200.1UF	C295	S06_PETP1	26
26	S06_PERN1	AK20	PE12RN1	PE12TN1	AN20	0.1UF	S06_PETN1	26
26	S06_PERP2	AL22	PE12RP2	PE12TP2	AP220.1UF	C296	S06_PETP2	26
26	S06_PERN2	AK22	PE12RN2	PE12TN2	AN22	0.1UF	S06_PETN2	26
26	S06_PERP3	AL23	PE12RP3	PE12TP3	AP230.1UF	C297	S06_PETP3	26
26	S06_PERN3	AK23	PE12RN3	PE12TN3	AN23	0.1UF	S06_PETN3	26
9 of 16								
26	S06_PERP4	AL25	PE13RP0	PE13TP0	AP250.1UF	C298	S06_PETP4	26
26	S06_PERN4	AK25	PE13RN0	PE13TN0	AN25	0.1UF	S06_PETN4	26
26	S06_PERP5	AL26	PE13RP1	PE13TP1	AP260.1UF	C299	S06_PETP5	26
26	S06_PERN5	AK26	PE13RN1	PE13TN1	AN26	0.1UF	S06_PETN5	26
26	S06_PERP6	AL28	PE13RP2	PE13TP2	AP280.1UF	C300	S06_PETP6	26
26	S06_PERN6	AK28	PE13RN2	PE13TN2	AN28	0.1UF	S06_PETN6	26
26	S06_PERP7	AL29	PE13RP3	PE13TP3	AP290.1UF	C301	S06_PETP7	26
26	S06_PERN7	AK29	PE13RN3	PE13TN3	AN29	0.1UF	S06_PETN7	26

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PM PORT 12/13			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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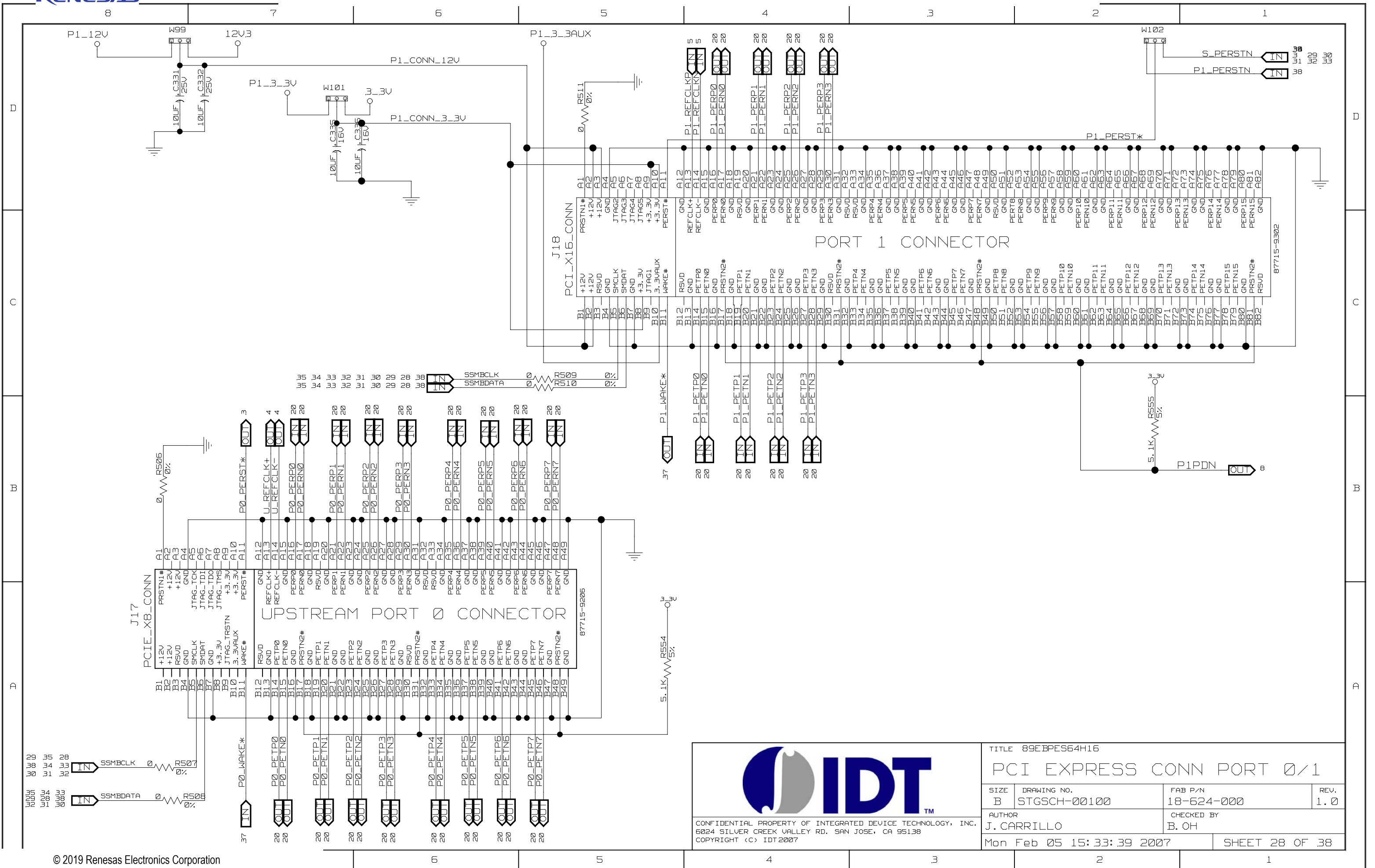


U31
89HPE64H16XXBR

27	S07_PERP0	AH31	PE14RP0	PE14TP0	AH340.1UF	C310	S07_PETP0	27
27	S07_PERN0	AH30	PE14RN0	PE14TN0	AH33	0.1UF	C318	S07_PETN0
27	S07_PERP1	AG31	PE14RP1	PE14TP1	AG340.1UF	C311	S07_PETP1	27
27	S07_PERN1	AG30	PE14RN1	PE14TN1	AG33	0.1UF	C319	S07_PETN1
27	S07_PERP2	AE31	PE14RP2	PE14TP2	AE340.1UF	C312	S07_PETP2	27
27	S07_PERN2	AE30	PE14RN2	PE14TN2	AE33	0.1UF	C320	S07_PETN2
27	S07_PERP3	AD31	PE14RP3	PE14TP3	AD340.1UF	C313	S07_PETP3	27
27	S07_PERN3	AD30	PE14RN3	PE14TN3	AD33	0.1UF	C324	S07_PETN3
10 of 16								
27	S07_PERP4	AB31	PE15RP0	PE15TP0	AB340.1UF	C314	S07_PETP4	27
27	S07_PERN4	AB30	PE15RN0	PE15TN0	AB33	0.1UF	C325	S07_PETN4
27	S07_PERP5	AA31	PE15RP1	PE15TP1	AA340.1UF	C315	S07_PETP5	27
27	S07_PERN5	AA30	PE15RN1	PE15TN1	AA33	0.1UF	C326	S07_PETN5
27	S07_PERP6	W31	PE15RP2	PE15TP2	W34 0.1UF	C316	S07_PETP6	27
27	S07_PERN6	W30	PE15RN2	PE15TN2	W33	0.1UF	C327	S07_PETN6
27	S07_PERP7	V31	PE15RP3	PE15TP3	V34 0.1UF	C317	S07_PETP7	27
27	S07_PERN7	V30	PE15RN3	PE15TN3	V33	0.1UF	C328	S07_PETN7

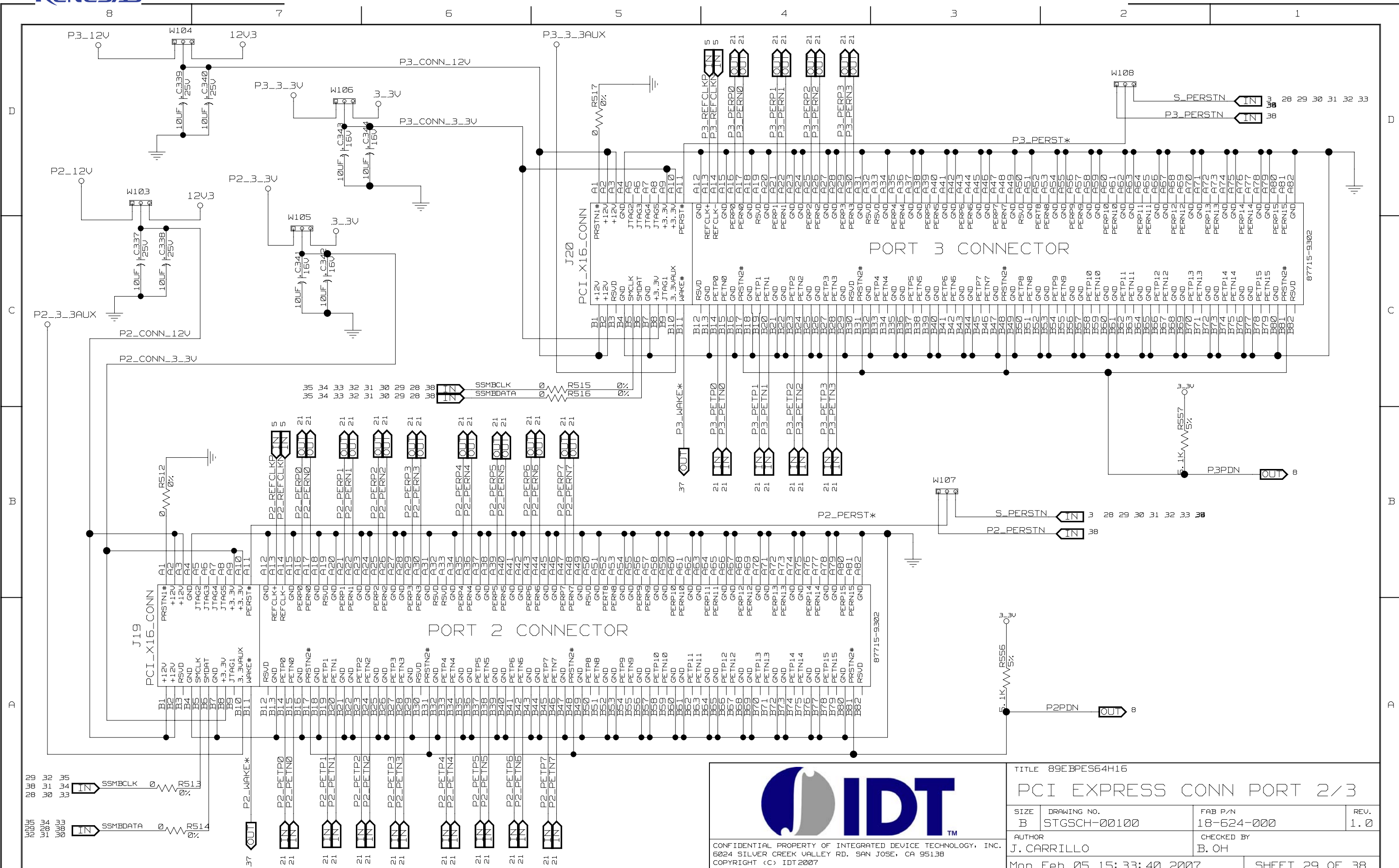
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PM PORT 14/15			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
AUTHOR J. CARRILLO		CHECKED BY B. OH	
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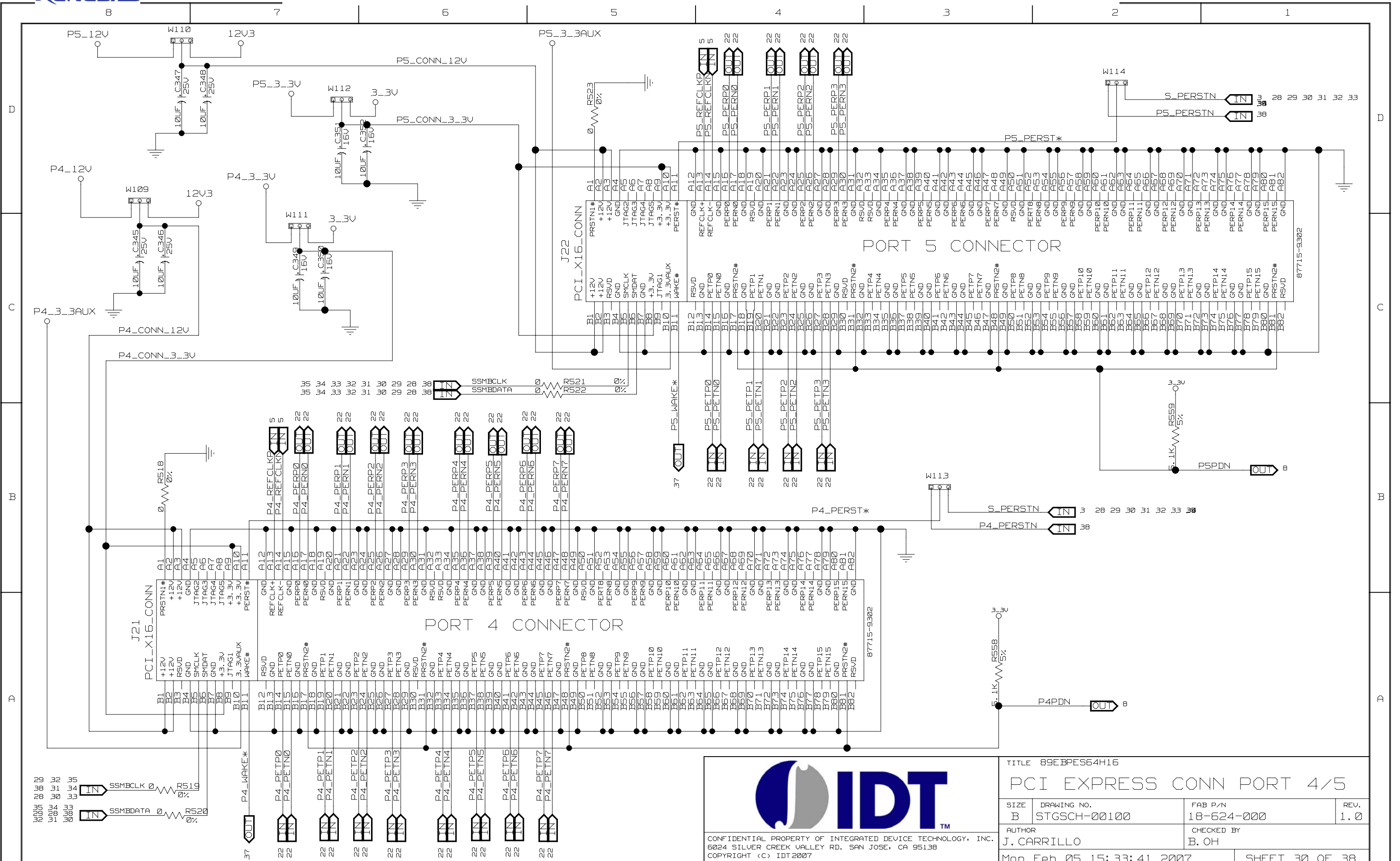
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PCI EXPRESS CONN PORT 0/1		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
AUTHOR J. CARRILLO		REV. 1.0
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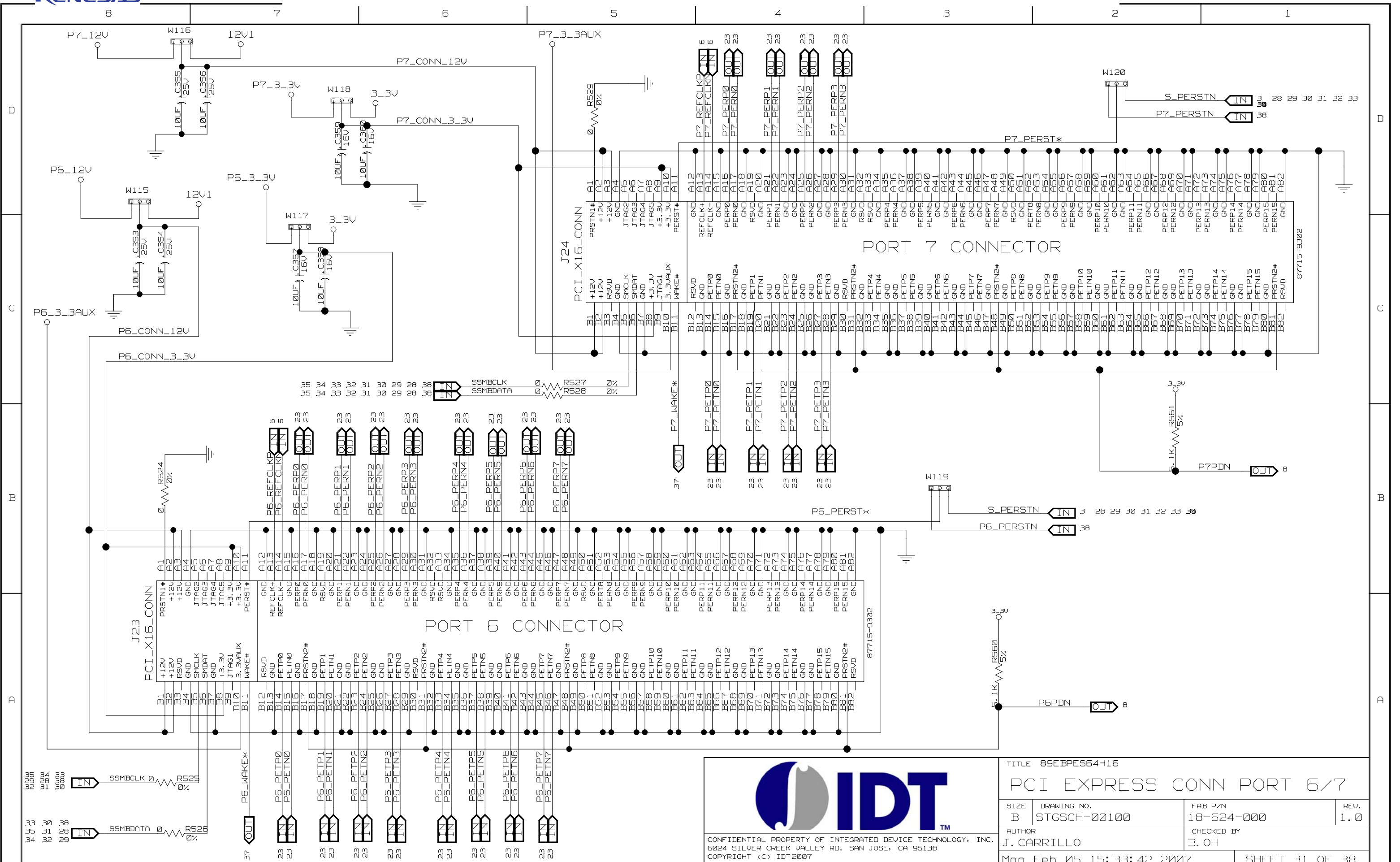
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PCI EXPRESS CONN PORT 2/3		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
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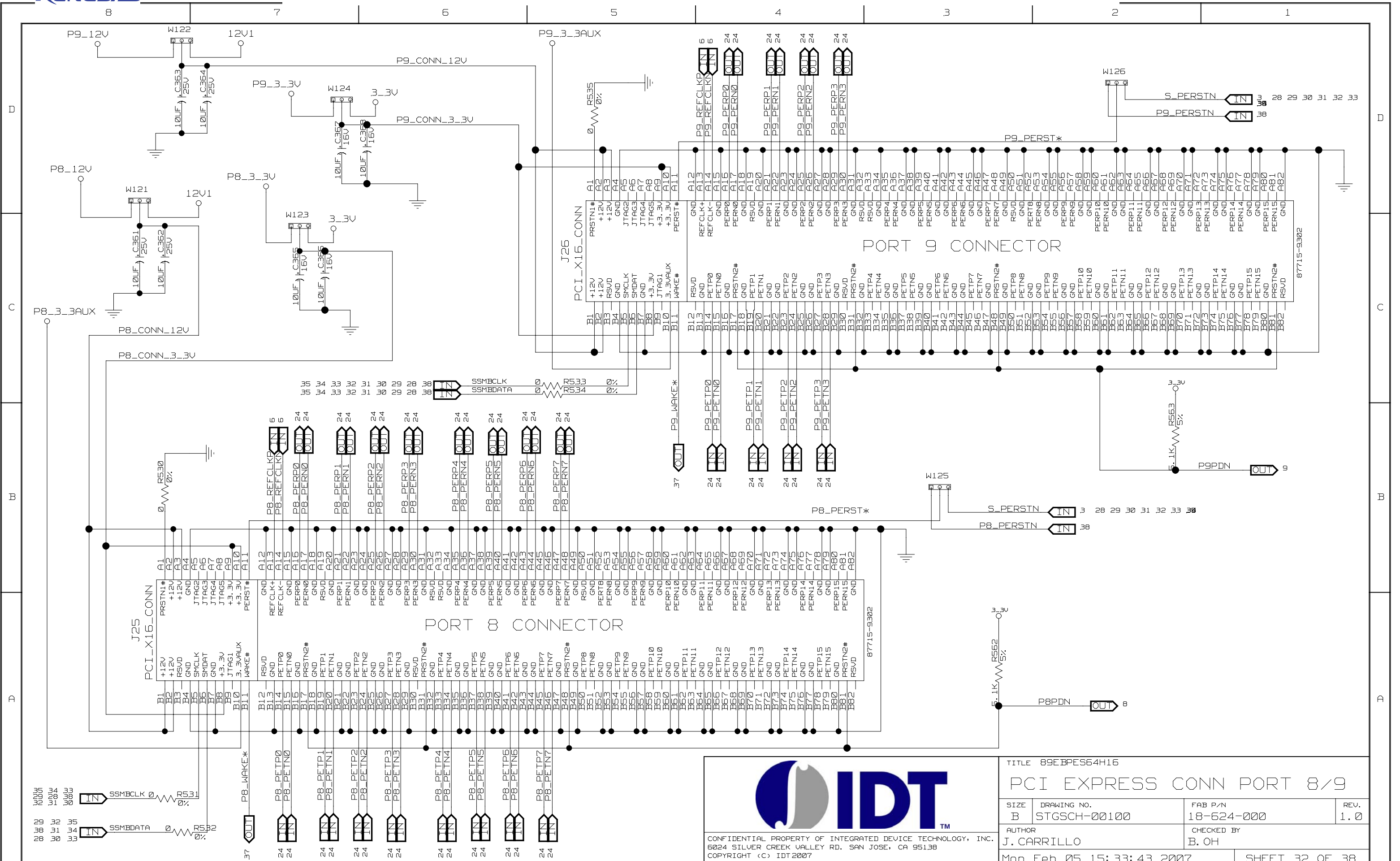
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PCI EXPRESS CONN PORT 4/5		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
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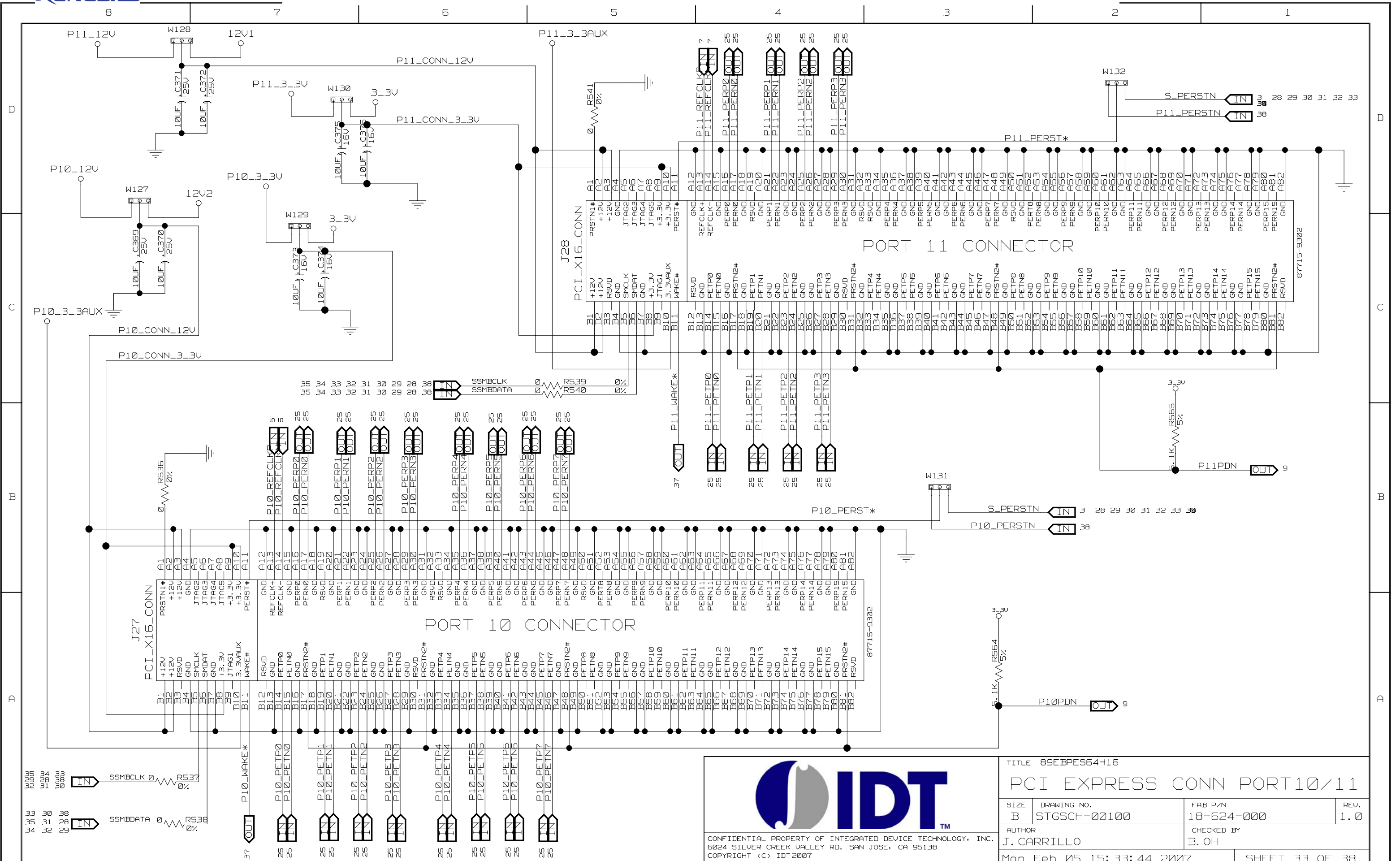
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PCI EXPRESS CONN PORT 6/7		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
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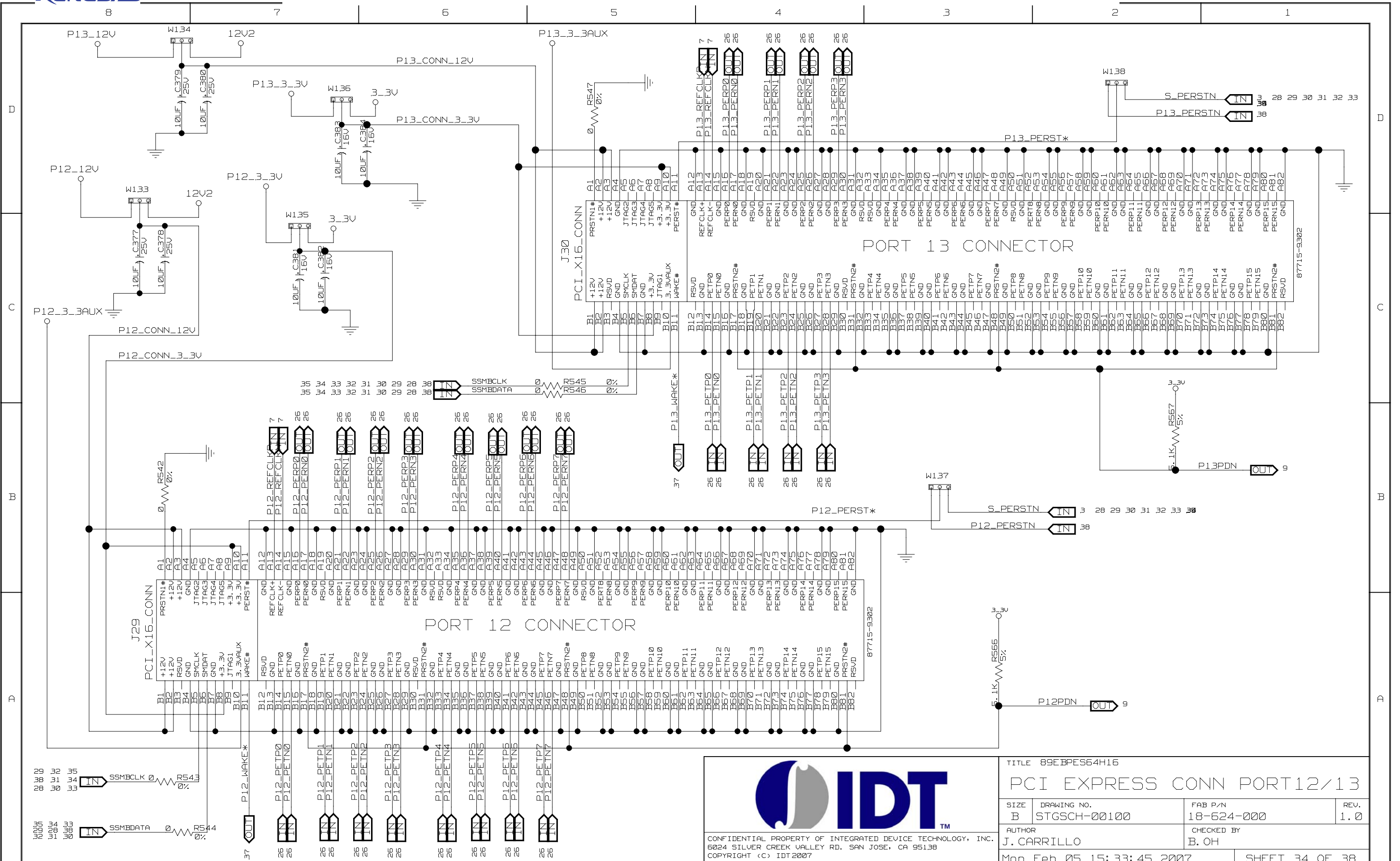
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PCI EXPRESS CONN PORT 8/9		
SIZE	DRAWING NO.	FAB P/N
B	STGSCH-00100	18-624-000
AUTHOR		REV.
J. CARRILLO		1.0
CHECKED BY		
B. OH		
Mon Feb 05 15:33:43 2007		SHEET 32 OF 38



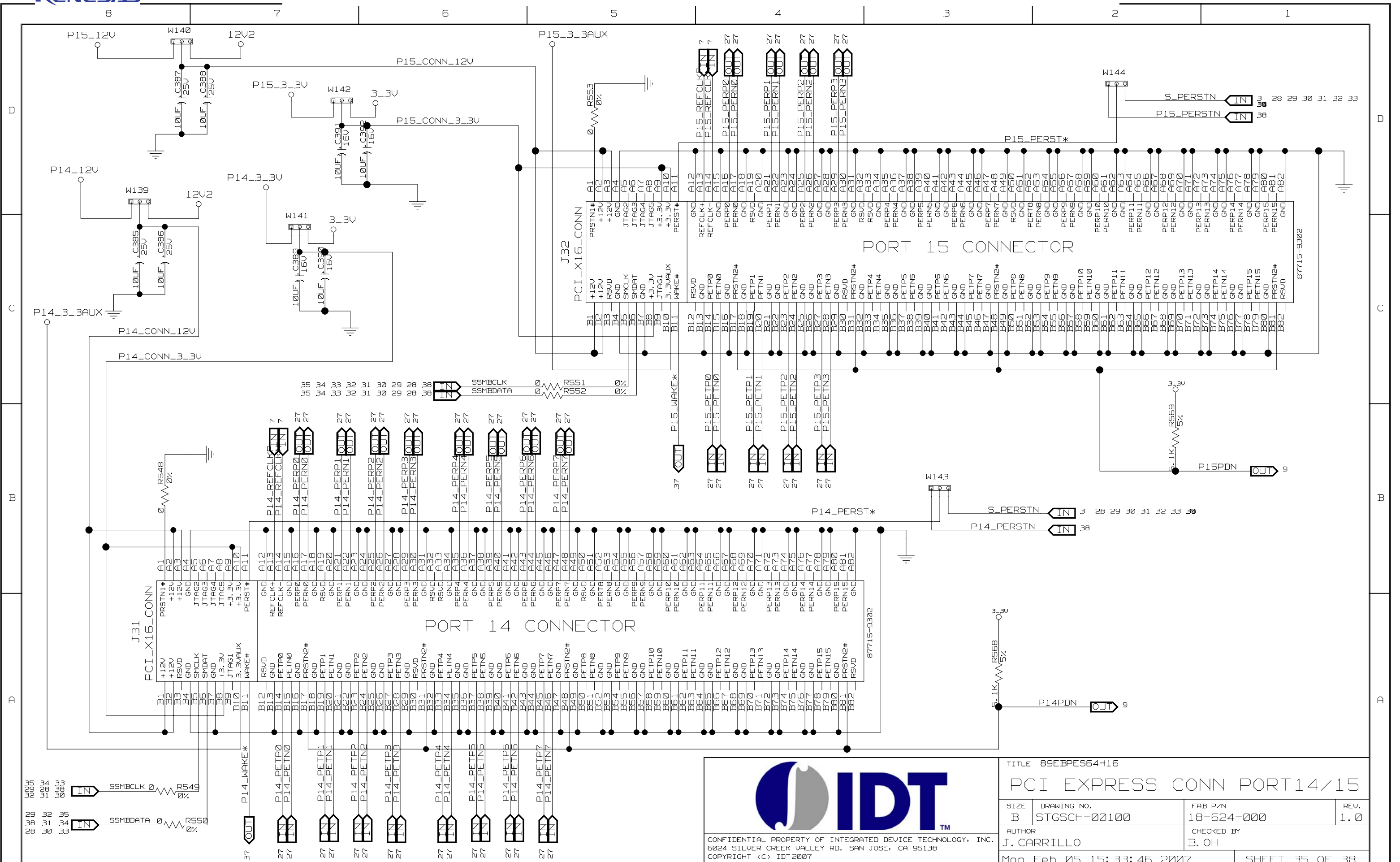
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PCI EXPRESS CONN PORT10/11		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
AUTHOR J. CARRILLO		REV. 1.0
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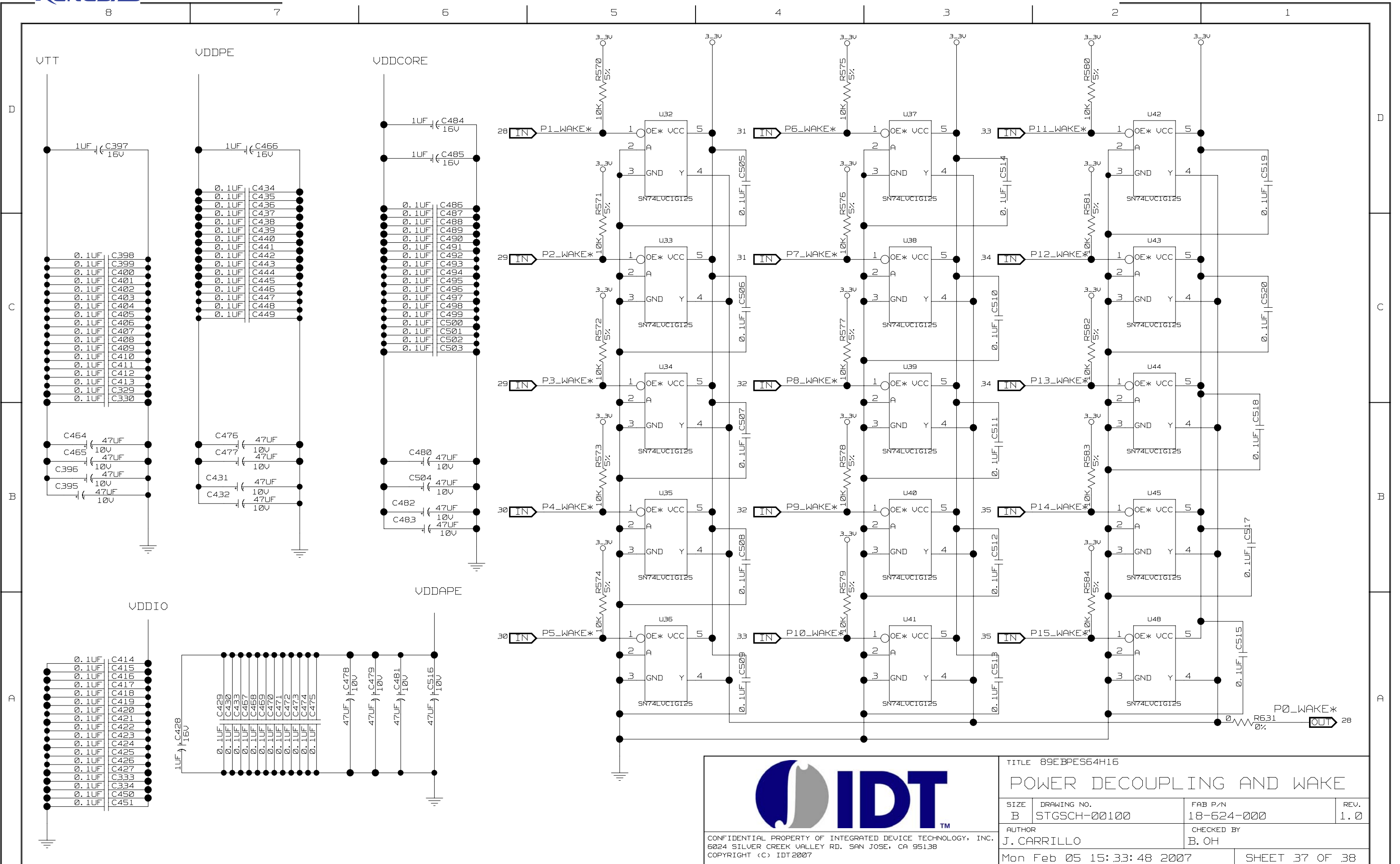
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PCI EXPRESS CONN PORT12/13		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
AUTHOR J. CARRILLO		REV. 1.0
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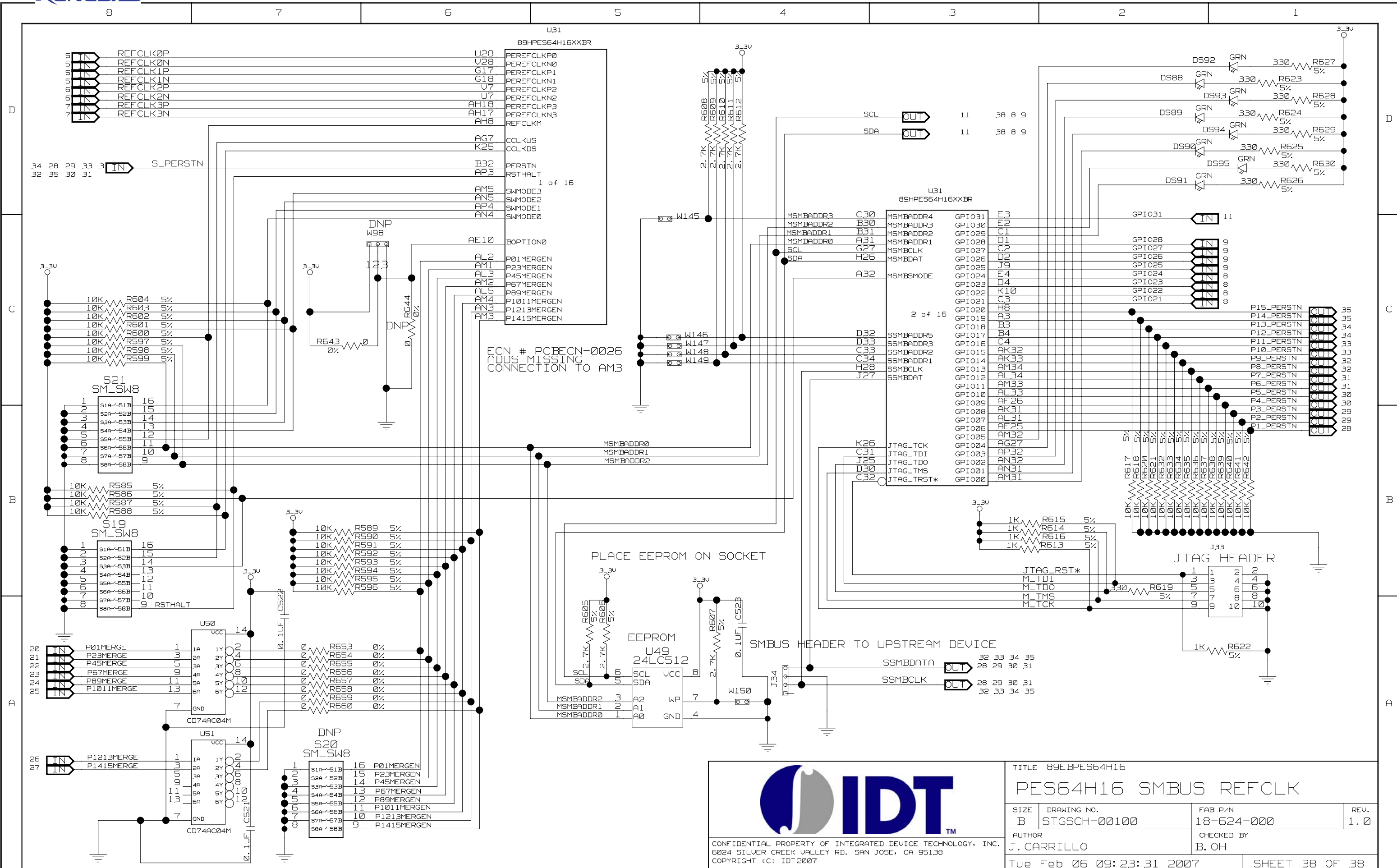
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PCI EXPRESS CONN PORT14/15		
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000
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TITLE 89EBPES64H16			
POWER DECOUPLING AND WAKE			
SIZE B	DRAWING NO. STGSCH-00100	FAB P/N 18-624-000	REV. 1.0
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TITLE 89BPES64H16			
PES64H16 SMBUS REFCLK			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00100	18-624-000	1.0
AUTHOR		CHECKED BY	
J. CARRILLO		B. OH	
Tue Feb 06 09:23:31 2007			SHEET 38 OF 38

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