

EVALUATION BOARD USER'S GUIDE

INTRODUCTION

The 82V3911 evaluation board kit, including an evaluation board and evaluation software, provides a platform to evaluate 82V3911.

The evaluation board kit contains the following components:

- 82V3911 evaluation board ver 1.00 with all necessary components
- 82V3911 evaluation GUI software ver 1.00
- 82V3911 evaluation board user's guide ver 1.0

FEATURES

- Professional evaluation software to configure and monitor the device
- Current configuration data can be saved as a file for later use

PC REQUIREMENTS

The 82V3911 evaluation software runs on Microsoft Windows. The system requirements are as follows:

- Pentium 166 MMX or higher (recommended)
- Minimum 500M bytes free hard disk space
- Minimum 64M bytes memory
- Display with the resolution of 1024x768, small font (recommended)
- Operating System: Microsoft Windows 2000/XP/NT (English version recommended) or newer OS version
- Microsoft Windows compatible 2-button or 3-button mouse

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1 HARDWARE CONFIGURATION

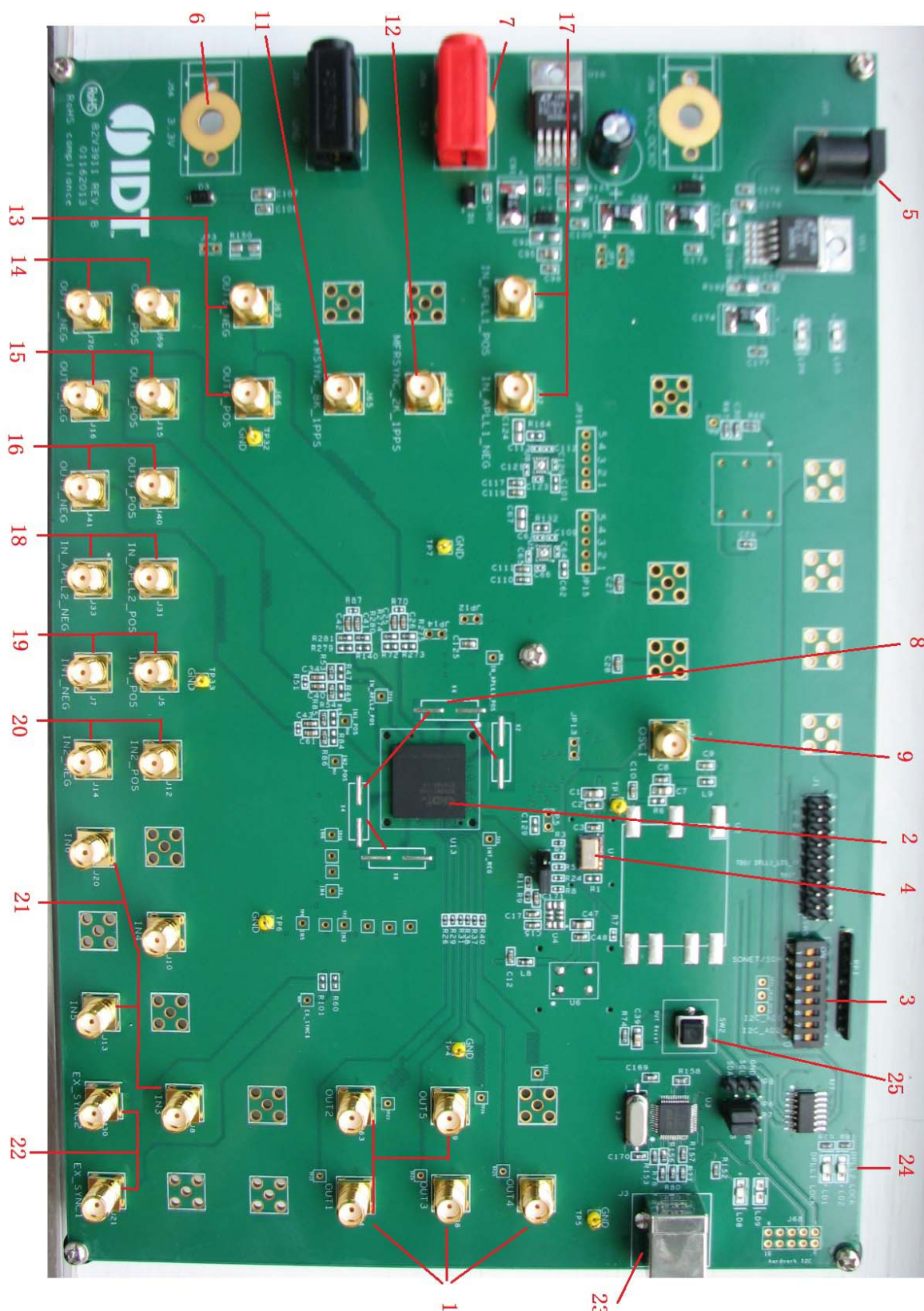


Figure-1 82V3911 Evaluation Board Illustration

1.1 ANNOTATION FOR FIGURE-1

- [1] Output clock 1 - 5
 [2] 82V3911 chip
 [3] Switch SW5: The function of this switch is described in [Table-1](#).

Table-1 Switch SW5 Function Description

Switch	Function Description	
SW5-2	SDH/SONET selection	Off: SDH
		On: SONET
SW5-3	not used	
SW5-4-6	not used	
SW5-7	I2C_AD1	Off: "0"
		On: "1"
SW5-8	I2C_AD2 I2C_AD1 and I2C_AD2 pins are the address bus of the microprocessor interface.	Off: "0"
		On: "1"

- [4] Crystal oscillator Master Clock
 [5] +5 V DC power supply
 [6] +3.3 V power supply for test purpose
 [7] +5 V power supply for test purpose
 [8] Crystal oscillator for APLL1 and APLL2
 [9] OSCI: master clock input
 [11] 8 kHz or 1pps frame synchronization output
 [12] 2 kHz multi-frame or 1pps frame synchronization output
 [13] Output clock 6 (differential)
 [14] Output clock 7 (differential)
 [15] Output clock 8 (differential)
 [16] Output clock 9 (differential)
 [17] Input clock to APLL1 (differential)
 [18] Input clock to APLL2 (differential)
 [19] Input clock 1 (differential)
 [20] Input clock 2 (differential)
 [21] Input clock 3-6
 [22] External frame sync 1 and 2 input
 [23] USB communication port
 [24] DPLL1 and DPLL2 DPLL lock indicator
 [25] Reset button: Press to reset all devices on the board

2 SOFTWARE CONFIGURATION

2.1 INSTALLATION

Double click on the "82V3911 VER1.00_SETUP.exe" file and follow the screen prompts, you will finish the evaluation software installation. After the installation, the evaluation software can be launched by choosing **Start>Programs>IDT WAN PLL>IDT WAN PLL 82V3911**.

2.2 GENERAL INTRODUCTION

2.2.1 OVERVIEW

The 82V3911 evaluation software provides a friendly interface for users to configure and control the 82V3911. As shown in [Figure-2](#), the main window includes:

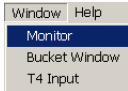



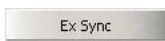
- ◆ Menu bar
- ◆ Shortcut icon
- ◆ Main work area (the area with blue background)
 - Input ports configuration area
 - Monitor
 - DPLL2 path configuration area
 - DPLL1 path configuration area
 - Output ports configuration area
 - General configuration area
 - DPLL1/ DPLL2 path selection and DPLL status indication area
 - APLL1/2 configuration

◆ Status bar

To operate this evaluation software, we assume that you have a basic familiarity with the 82V3911. If you have difficulties in understanding this users' manual, please refer to the 82V3911 datasheet.

2.2.2 CONVENTIONS USED

Users can operate this evaluation software by clicking on the menu bar, the shortcut icons, the function blocks or the buttons. For easy explanation, we have adopted a few simple conventions to describe these tools. See the following table for details.

Name	Image (Example)	Convention Used
menu bar		"Window > Monitor"
shortcut icon		shortcut icon 
function block		"Monitor"
button		"Ex Sync"

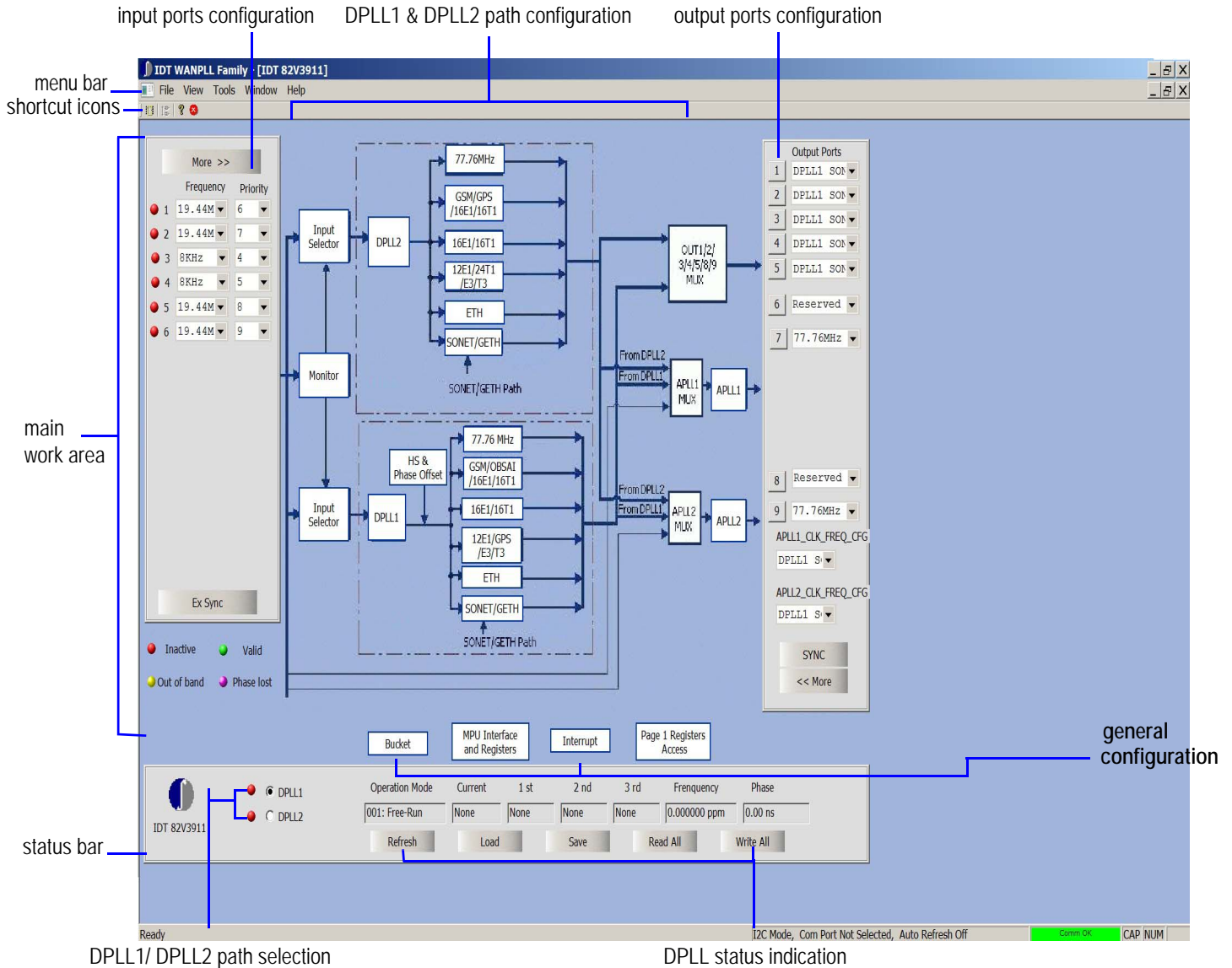


Figure-2 Graphic User Interface (GUI)

2.2.3 DPLL1/ DPLL2 PATH SELECTION

Since some registers are related to the input ports, the DPLL1 and the DPLL2 are shared paths, and users must select a path (DPLL1 or DPLL2) before configuring these registers. See [Figure-3](#) for details.

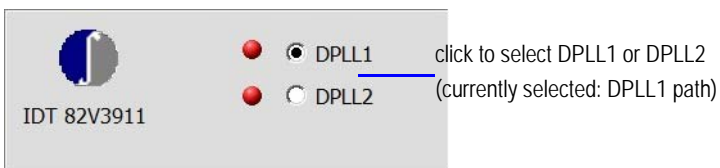


Figure-3 DPLL1/ DPLL2 Path Selection

2.2.4 READ/WRITE THE CONFIGURATION DATA

Generally, once a configuration is made, the configuration data will be directly written to device. But in the Register Set I dialog box, after configuring the registers, you need to click the "Write" or "Write All" button to write the configuration data to device.

In the main work area or in the dialog boxes, you can click on the "Refresh" button to read the register value from the device.

2.2.5 LOAD/SAVE THE CONFIGURATION DATA

To load or save the configuration data, please open the Register Set I dialog box by selecting "Windows > Register Set I" or clicking on "MCU Interface and Registers". Or you can click on the Load or Save button in the Main window. Refer to [2.9.1 Registers Configuration](#) for details.

2.2.6 TIPS FOR THE PARAMETERS AND BUTTONS

The evaluation software provides tips for the parameters, shortcut icons and buttons to help users make configurations. For example, when the mouse focus is on a parameter, a tip will appear displaying the related register's name, address and bits. See [Figure-4](#).

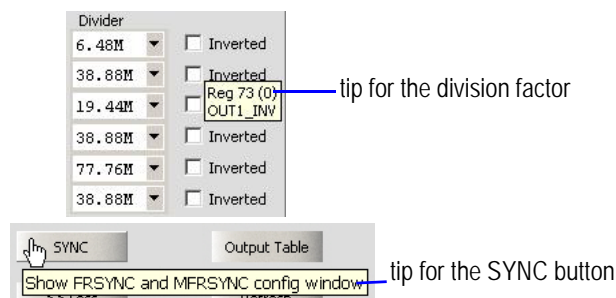
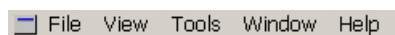


Figure-4 Tips for Parameters and Buttons

2.2.7 MENU BAR

The menu bar contains five menus as shown in the following:



◆ File Menu

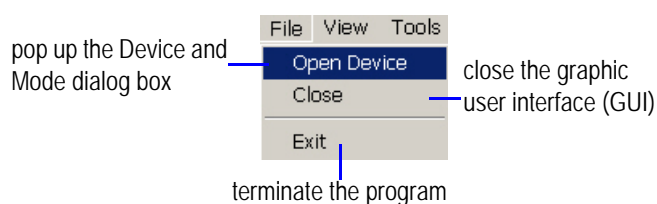


Figure-5 File Menu

◆ View Menu

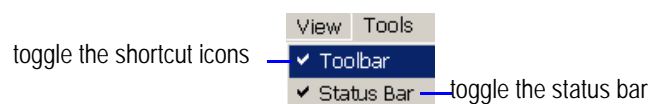


Figure-6 View Menu

◆ Tools Menu

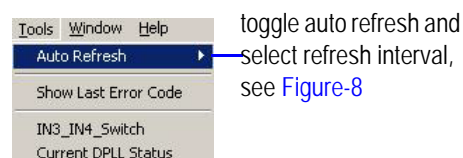


Figure-7 Tools Menu

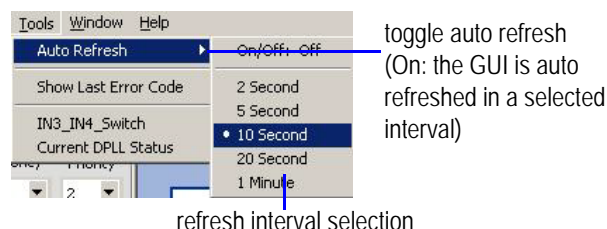


Figure-8 Auto Refresh Configuration

◆ Window Menu

The Window menu contains 13 sub-menus as shown in [Figure-9](#). All these sub-menus except "Register Set II" and "Hide All Popup" have the same functions as their respective buttons/function blocks in the main window. Refer to the corresponding sections for details.

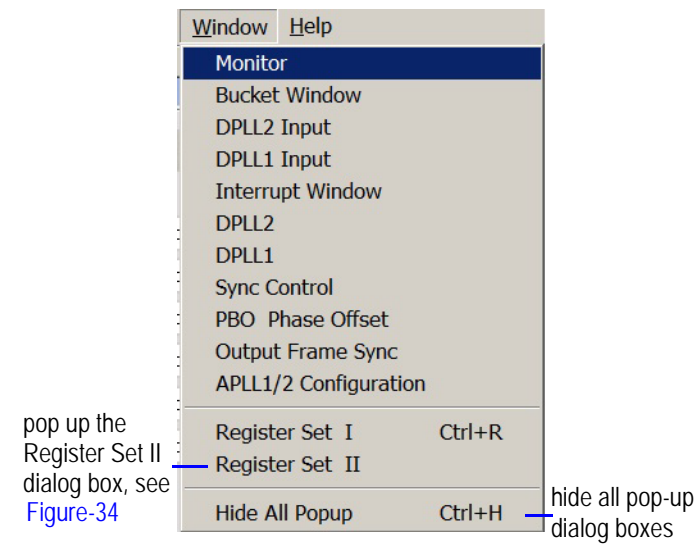


Figure-9 Window Menu

◆ Help Menu

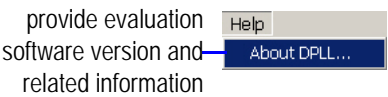


Figure-10 Help Menu

2.2.8 SHORTCUT ICONS

The functions of the shortcut icons are described in the following table:

Shortcut Icon	Function
	the same as menu "File > Open Device"
	the same as menu "Help > About DPLL..."
	the same as menu "File > Exit"

2.2.9 STATUS BAR

The status bar shows the currently selected microprocessor interface and communication port. See [Figure-11](#) for details.

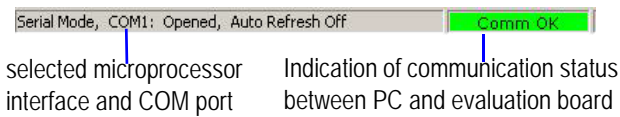



Figure-11 Status Bar

2.3 INITIALIZATION

After the program is launched, the Device Port Selection dialog box pops out as shown in [Figure-12](#). Users can select a COM port in this dialog box.

Click on "Detect", and the status of the COM ports will be detected and displayed in the lower part of this dialog. The evaluation software will automatically select the port which successfully communicates with the 82V3911 evaluation board.

Click on "OK", and the evaluation board will be initialized and the main window will appear as shown in [Figure-2](#).

After initialization, users can re-open this dialog box by selecting "File > Open Device" or clicking on the shortcut icon .

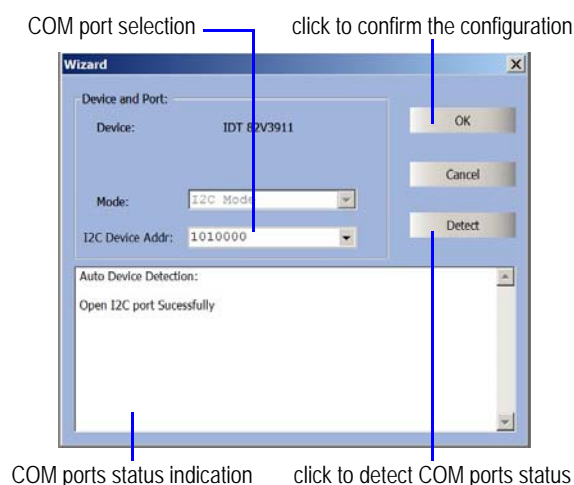


Figure-12 Device Port Selection

2.4 INPUT PORTS STATUS AND CONFIGURATION

The input ports status and configuration interface is as shown in [Figure-13](#). Users can select frequency and priority for each of the 14 input ports in the corresponding pull-down list. The status of the input ports are indicated by color LEDs.

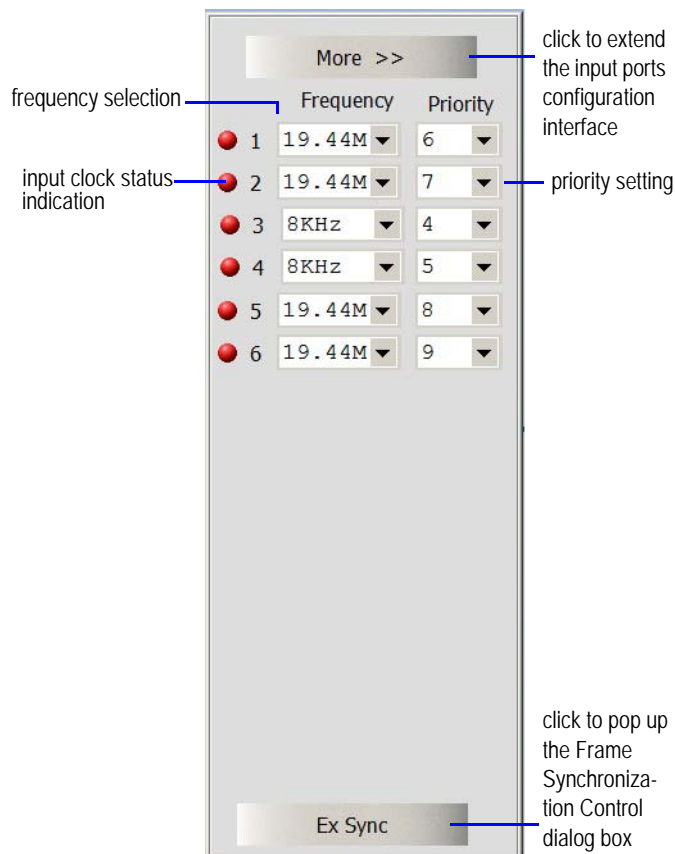


Figure-13 Input Configuration (Shrunk)

Click on "More >>", and the input configuration interface will be extended to display all input-related status and configuration. See [Figure-14](#) for details.

The screenshot shows the 'Input Configuration (Extended)' dialog box. It features a table of input ports (1-6) with columns for Frequency, Priority, DivN, 8K, Bucket I.D., Remote Valid, Input Valid, (soft) out of band, (hard) out of band, No Active, and Phase Lost. Below the table are controls for 'Ex Sync', 'Revertive mode', 'Rising Edge', 'Input 1/2', 'Pre DivN CH/Value', 'IN 3', '32767', '+ 1', 'Buckets', 'Refresh', and '<< Less'. Annotations point to various elements: 'leaky bucket configuration selection' points to the 'Bucket I.D.' column; 'lock 8k divider (checked: used)' points to the '8K' column; 'DivN divider (checked: used)' points to the 'DivN' column; 'priority setting' points to the 'Priority' column; 'clock frequency selection' points to the 'Frequency' column; 'input clock status indication' points to the 'Input Valid' column; 'allow/dis-allow lock to the input clock (checked: allow)' points to the 'Remote Valid' column; 'input clock quality indication (checked: valid)' points to the '(soft) out of band' column; 'hard frequency alarm indication (checked: has alarm)' points to the '(hard) out of band' column; 'no activity indication (checked: no activity)' points to the 'No Active' column; 'phase loss indication (checked: phase loss)' points to the 'Phase Lost' column; 'register address and bits' points to the rightmost column containing register addresses like 'R45(3:0)'; 'click to pop up the Frame Synchronizing Control dialog box' points to the 'Ex Sync' button; 'revertive mode enable' points to the 'Revertive mode' checkbox; 'master clock active edge selection' points to the 'Rising Edge' dropdown; 'IN1/IN2 electrical level selection' points to the 'Input 1/2' dropdown; 'HF divider enable' points to the 'HF divider enable' checkbox; 'DivN divider selection' points to the 'Pre DivN CH/Value' dropdown; 'division factor' points to the 'IN 3' dropdown; 'click to pop up the Bucket Configuration dialog box' points to the 'Buckets' button; 'click to read all the related registers and refresh the display' points to the 'Refresh' button; and 'click to shrink this input configuration interface' points to the '<< Less' button.

leaky bucket configuration selection

lock 8k divider (checked: used)

DivN divider (checked: used)

priority setting

clock frequency selection

input clock status indication

allow/dis-allow lock to the input clock (checked: allow)

input clock quality indication (checked: valid)

hard frequency alarm indication (checked: has alarm)

no activity indication (checked: no activity)

phase loss indication (checked: phase loss)

register address and bits

click to pop up the Frame Synchronizing Control dialog box

revertive mode enable

master clock active edge selection

IN1/IN2 electrical level selection

HF divider enable

DivN divider selection

division factor

click to pop up the Bucket Configuration dialog box

click to read all the related registers and refresh the display

click to shrink this input configuration interface

	Frequency	Priority	DivN	8K	Bucket I.D.	Remote Valid	Input Valid	(soft) out of band	(hard) out of band	No Active	Phase Lost	
1	19.44M	6	<input type="checkbox"/>	<input type="checkbox"/>	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	R45(3:0)
2	19.44M	7	<input type="checkbox"/>	<input type="checkbox"/>	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	R45(7:4)
3	8KHz	4	<input type="checkbox"/>	<input type="checkbox"/>	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	R44(3:0)
4	8KHz	5	<input type="checkbox"/>	<input type="checkbox"/>	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	R44(7:4)
5	19.44M	8	<input type="checkbox"/>	<input type="checkbox"/>	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	R46(3:0)
6	19.44M	9	<input type="checkbox"/>	<input type="checkbox"/>	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	R46(7:4)

Figure-14 Input Configuration (Extended)

2.4.1 LEAKY BUCKET CONFIGURATION

Click on "Buckets" or select "Window > Bucket Window". The buckets dialog box pops up as shown in Figure-15. Users can set the four leaky bucket configurations in this dialog box.

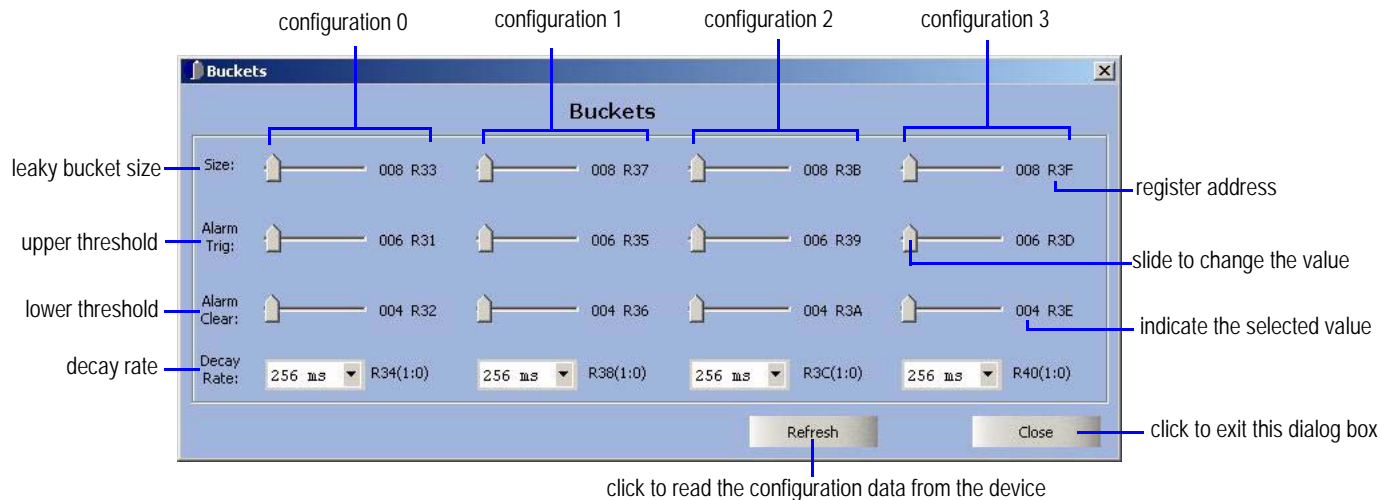


Figure-15 Buckets Dialog Box

2.4.2 FRAME SYNCHRONIZATION CONTROL

Click on "Ex Sync". The Frame synchronization Control dialog box pops up as shown in Figure-16. In this dialog box, users can configure the registers related to the external frame synchronization signal.

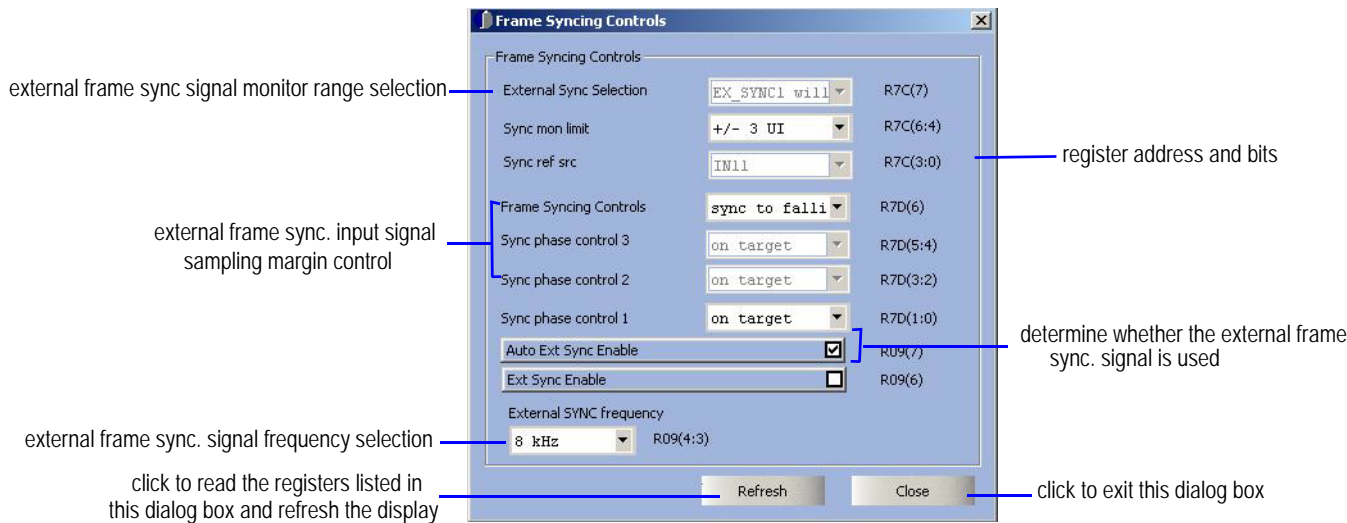


Figure-16 Frame Synchronization Control Dialog Box

2.5 MONITOR CONFIGURATION

Click on "Monitor" or select "Window > Monitor". The Monitors dialog box pops up as shown in Figure-17. In this dialog box, users can configure the input clock quality monitor.

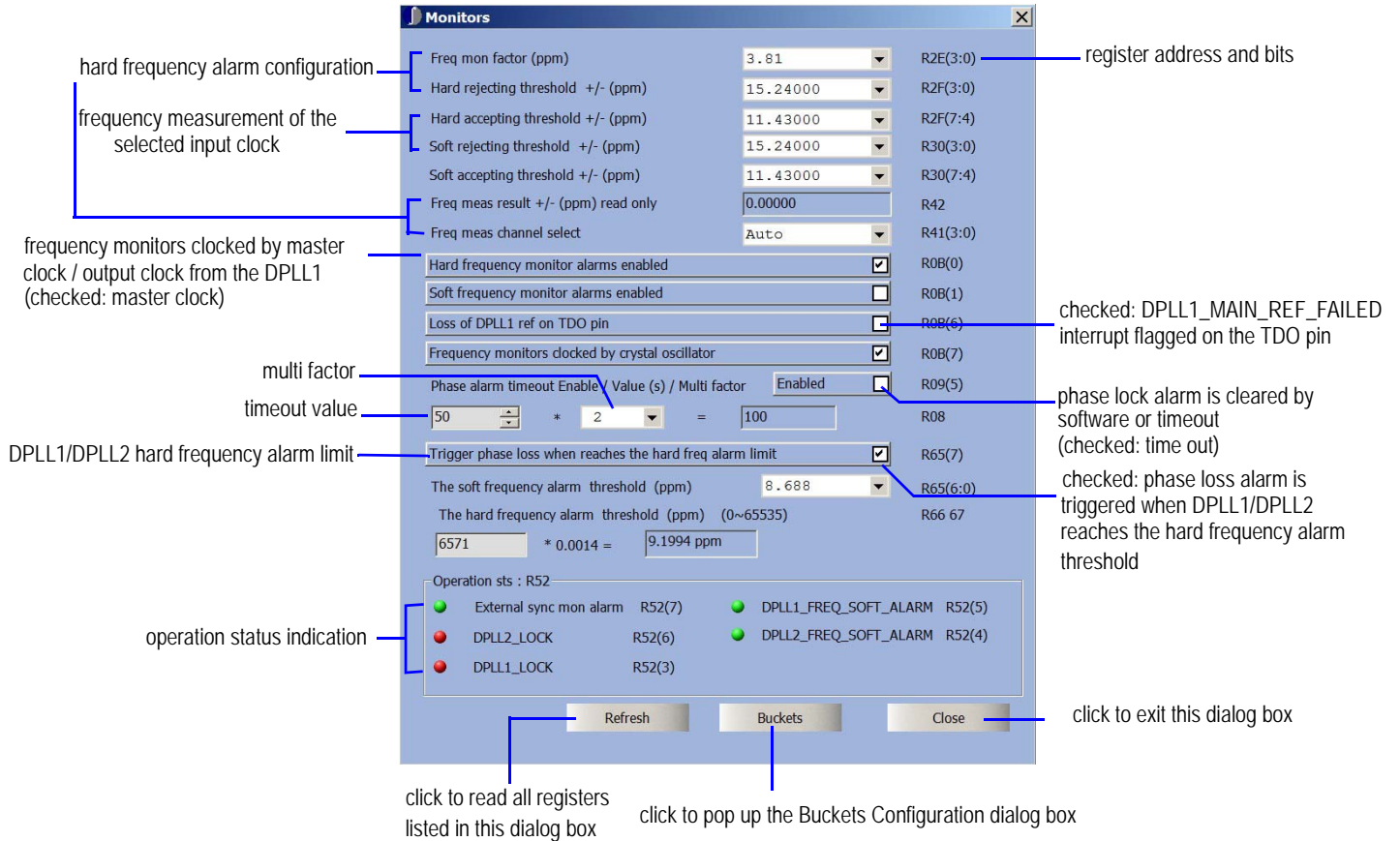


Figure-17 Monitors Dialog Box

2.6 DPLL2 PATH CONFIGURATION

2.6.1 DPLL2 INPUT SELECTOR

Click on "DPLL2 Input Selector" or select "*Window > DPLL2 Input*". The following dialog box pops out, allowing users to select an input to the DPLL2.

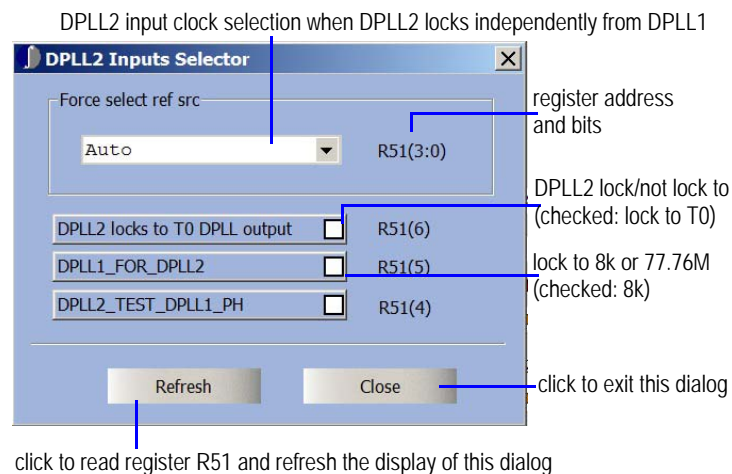


Figure-18 DPLL2 Input Selector Dialog Box

2.6.2 DPLL2 DPLL

Click on "DPLL2 PFD & LP" or select "*Window > DPLL2*". The DPLL2 dialog box pops out as shown in Figure-19. This dialog box allows users to configure the DPLL2.

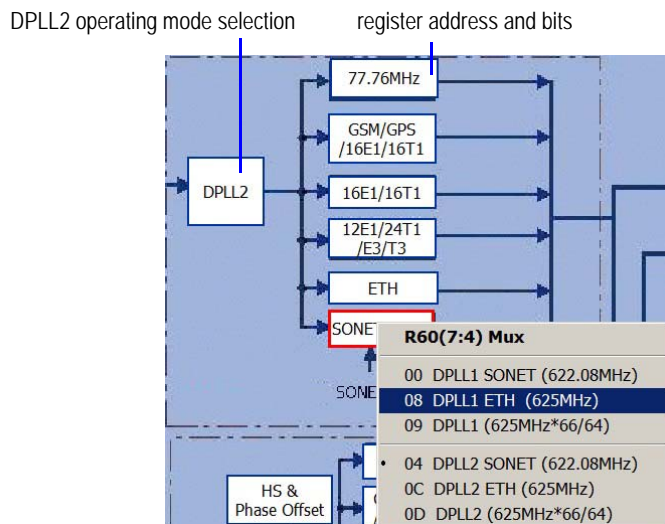


Figure-19 DPLL2 Dialog Box

Note: Before opening this dialog box, users must select the DPLL2 path (see 2.2.3 DPLL1/ DPLL2 Path Selection), otherwise the DPLL2 coarse/fine phase detector can not be configured.

2.6.3 DPLL2 DCO OUTPUT CLOCK FREQUENCY SELECTION

Click on "GSM/GPS/16E1/16T1", "16E1/16T1" and "12E1/24T1/E3/T3" in the DPLL2 path to select the DCO output clock frequency. See [Figure-20](#) for details.

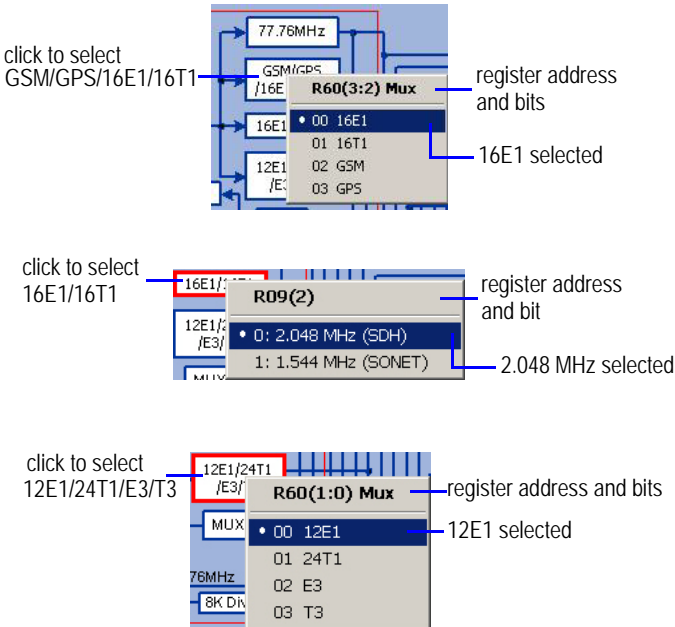


Figure-20 DPLL2 DCO Output Frequency Selection

2.6.4 DPLL2 SONET/GETH CONFIGURATION

Click on "SONET/GETH" to select an input source for the DPLL2 SONET/GETH. See [Figure-21](#).

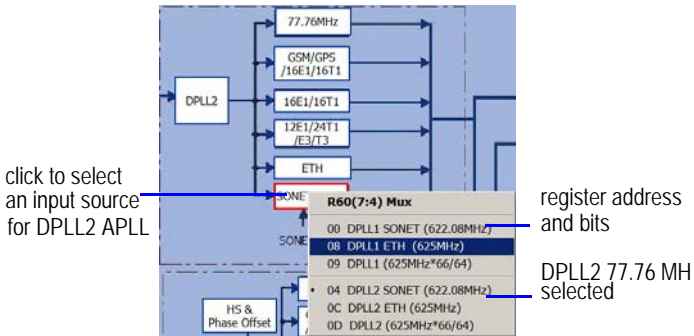


Figure-21 DPLL2 SONET/GETH Input Source Selection

2.7 DPLL1 PATH CONFIGURATION

2.7.1 DPLL1 INPUT SELECTOR

Click on "DPLL1 Input Selector" or select "Window > DPLL1 Input". The following dialog box pops out, allowing users to select an input for the DPLL1.

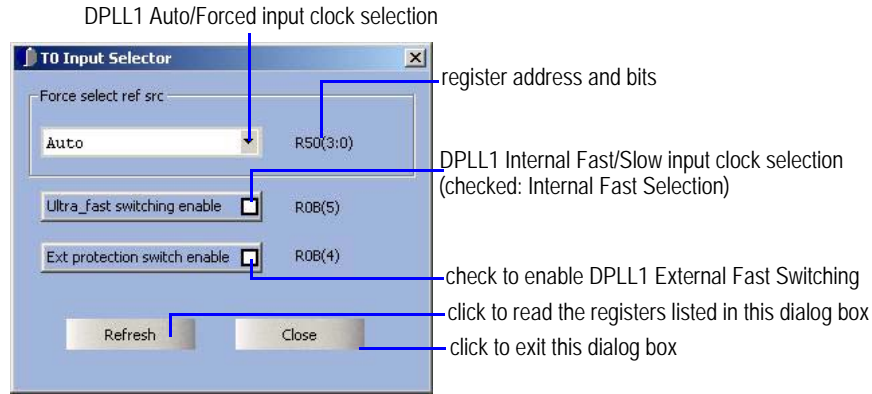


Figure-22 DPLL1 Input Selector Dialog Box

2.7.2 DPLL1

Click on "DPLL1 PFD & LP" or select "Window > DPLL1". The DPLL1 dialog box pops out as shown in Figure-23. This dialog box allows users to configure the DPLL1.

Note: Before opening this dialog box, users must select the DPLL1 path (see 2.2.3 DPLL1/ DPLL2 Path Selection), otherwise the DPLL1 coarse/fine phase detector can not be configured.

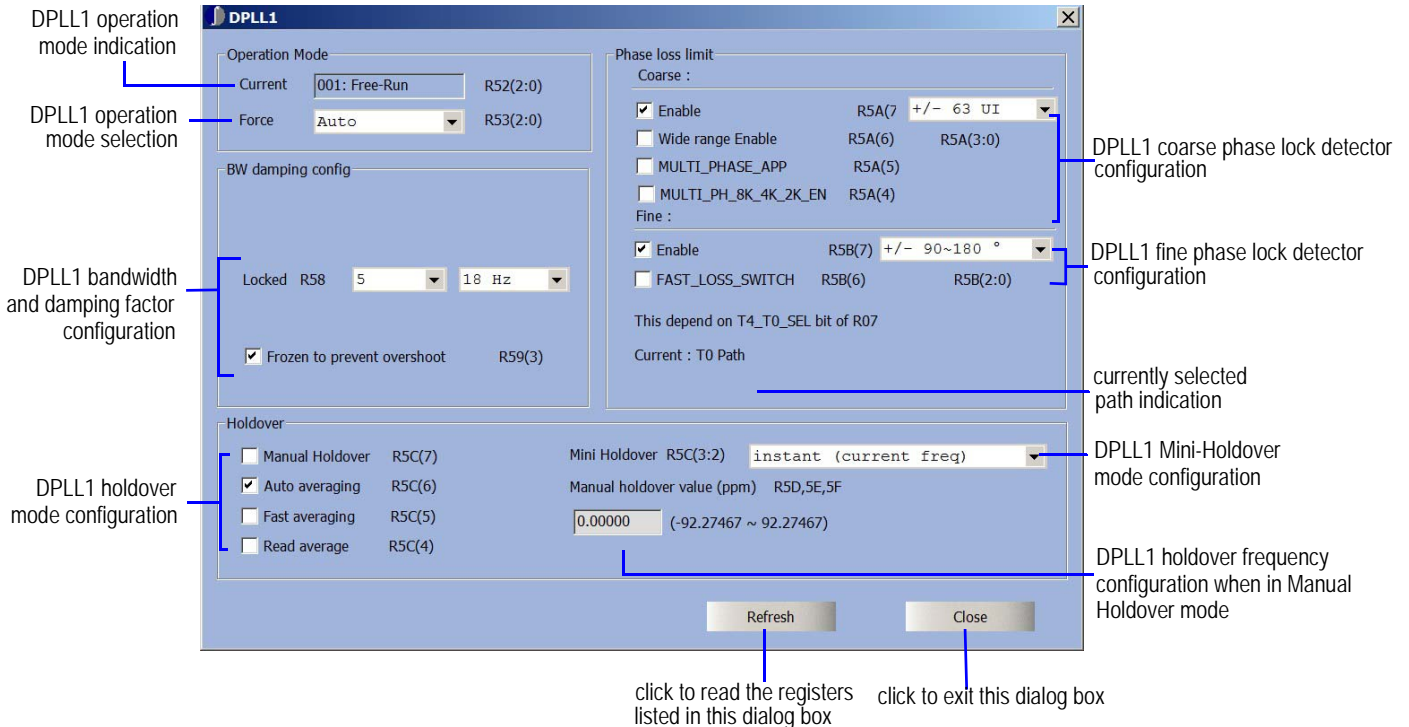


Figure-23 DPLL1 Dialog Box

2.7.3 HS AND PHASE OFFSET CONFIGURATION

Click on "HS & Offset" or select "Window > HS Phase Offset". The HS and Phase Offset dialog box pops out as shown in Figure-24. This dialog box allows users to configure HS & phase offset.

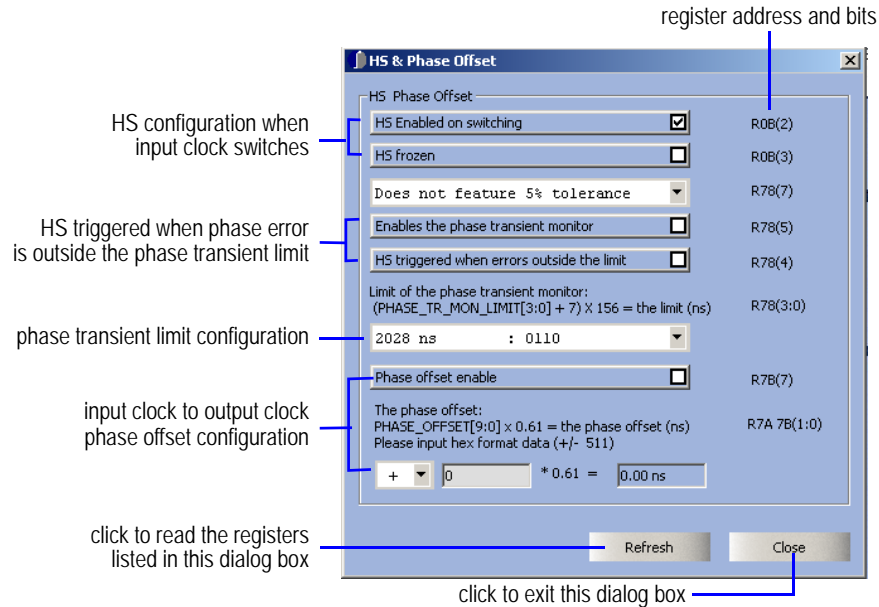


Figure-24 HS and Phase Offset Dialog Box

2.7.4 DPLL1 DCO OUTPUT CLOCK FREQUENCY SELECTION

Click on "GSM/OBSAI/16E1/16T1", "16E1/16T1" and "12E1/24T1/E3/T3" in the DPLL1 path to select the DCO output clock frequency. See Figure-25 for details.

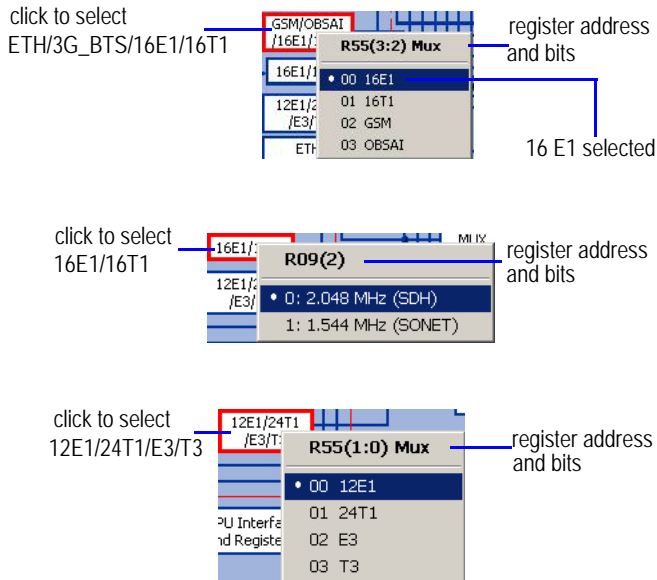


Figure-25 DPLL1 DCO Output Frequency Selection

2.7.5 DPLL1 SONET/GETH CONFIGURATION

Click on "DPLL1 SONET/GETH" to select an input source for the DPLL1 APPL. See Figure-26.

Click on "DPLL1 SONET/GETH" to select a bandwidth for the DPLL1 APPL. See Figure-27.

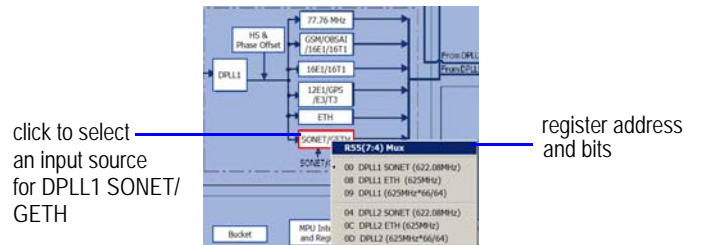


Figure-26 DPLL1 SONET/GETH Input Source Selection

2.8 OUTPUT PORTS CONFIGURATION

The default output ports configuration interface is as shown in Figure-27. Click on "<< More", and this interface extends to show all output-related configuration information. See Figure-28 for details.

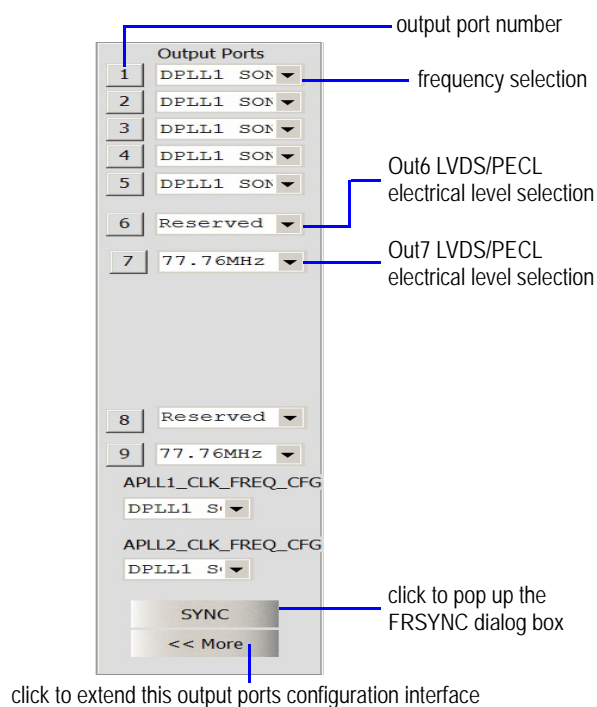


Figure-27 Output Ports Configuration (Shrunked)

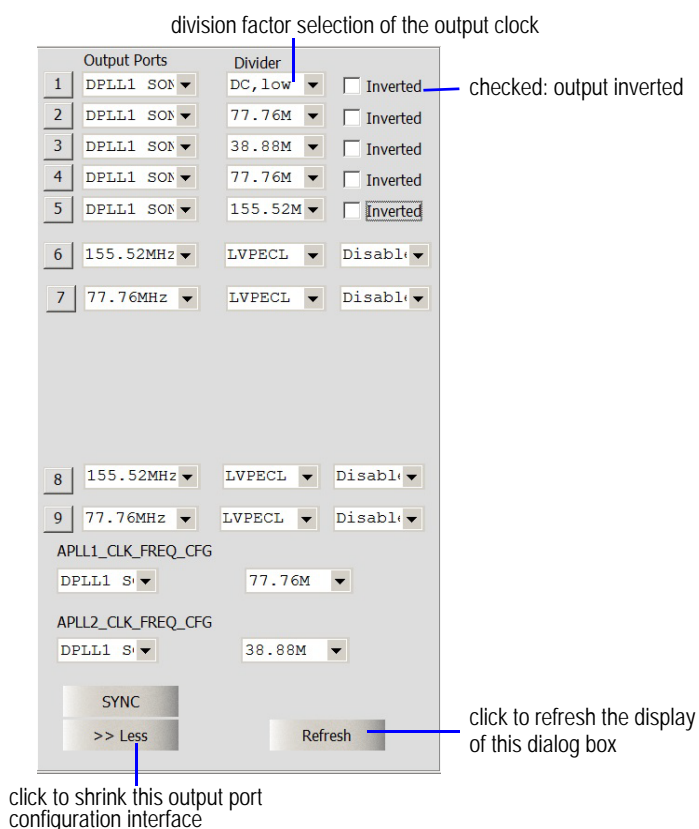


Figure-28 Output Ports Configuration (Extended)

2.8.1 ETHERNET CLOCK CONFIGURATION FOR OUTPUT PORTS

Following is an example using Ethernet clocks from the DPLL1 SONET/GETH (625 MHz) path to configure the output 6. The steps below are performed from the main GUI (refer to Figure-2).

1. Click on "DPLL1 SONET/GEHT" to select "08 DPLL1 ETH (625 MHz)".

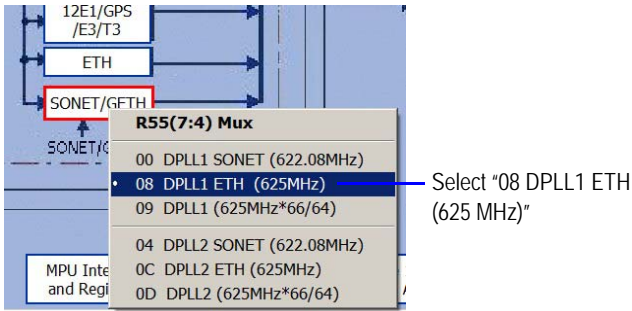


Figure-29 Selecting a DPLL1 Input Source

2. Click on "APLL1" or "APLL2" to configure the APLL interface, and setting "19525" to PDSEL and "3124" to M

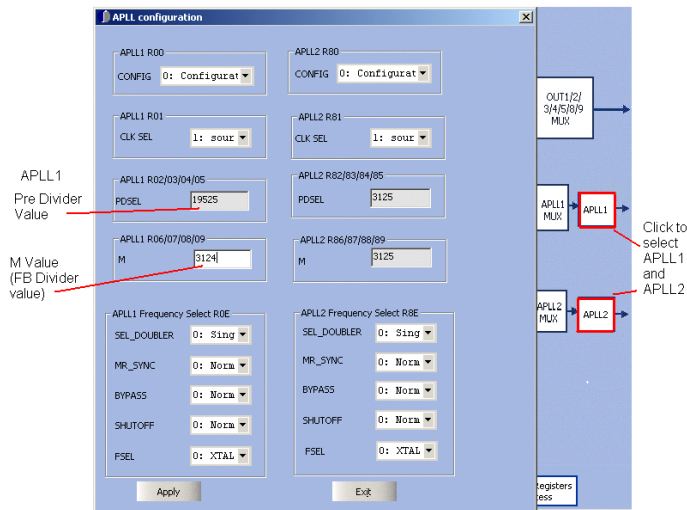


Figure-30 APLL Configuration Interface

3. Click on "<< More" in the output ports configuration interface to show all output-related configuration information. Click on output 6 in the output ports configuration interface to select "25MHz/ 125MHz/ 156.25MHz/ 312.5MHz/ 625MHz". The "Enable Output" and "156.25MHz" clock on DPLL1 SONET/GETH Path should be selected.

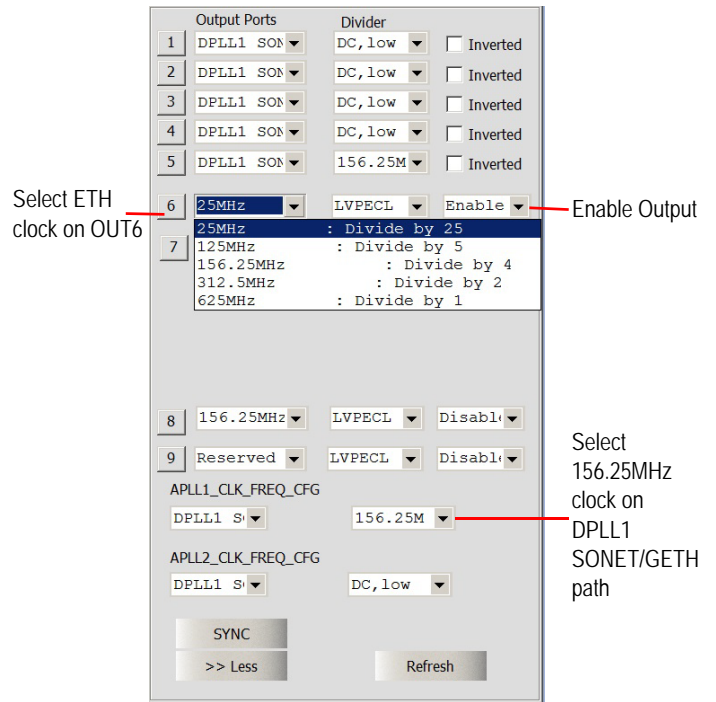


Figure-31 DPLL1 APLL1 ETH Clock Selection for Output 6

2.8.2 FRAME AND MULTI-FRAME CONFIGURATION

Click on "SYNC" or select "Window > Output Frame Sync". The Frame and Multi-Frame configuration dialog box pops up as shown in Figure-32.

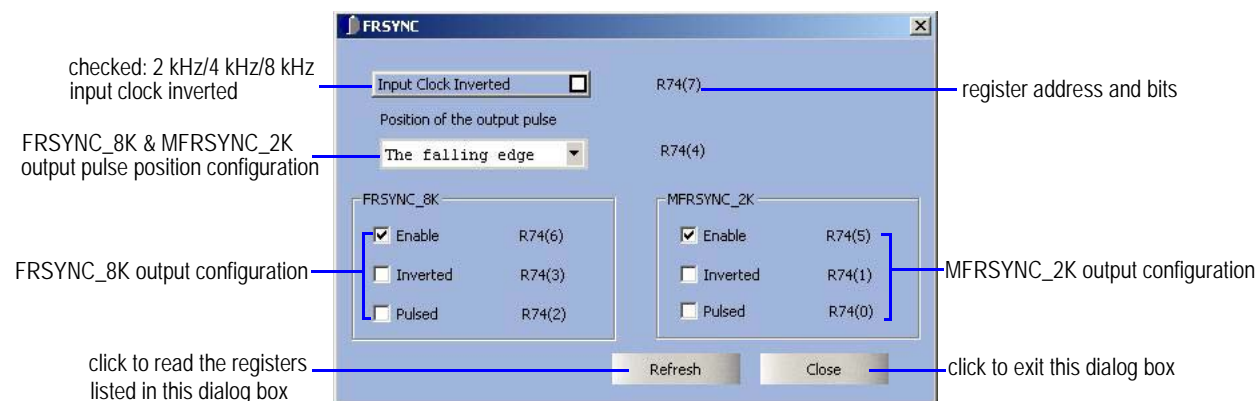


Figure-32 Frame/Multi-Frame Configuration Dialog Box

2.9 OTHER CONFIGURATION

2.9.1 REGISTERS CONFIGURATION

◆ Register Set I Dialog Box

Click on "MPU Interface and Registers" or select "Window > Register Set I". The Register Set dialog box pops up as shown in Figure-33. Users can configure all registers or check the status of all registers in this dialog box. Users can save the register configuration data as a file (*.rgf) for later use, or load the configuration data from a file.

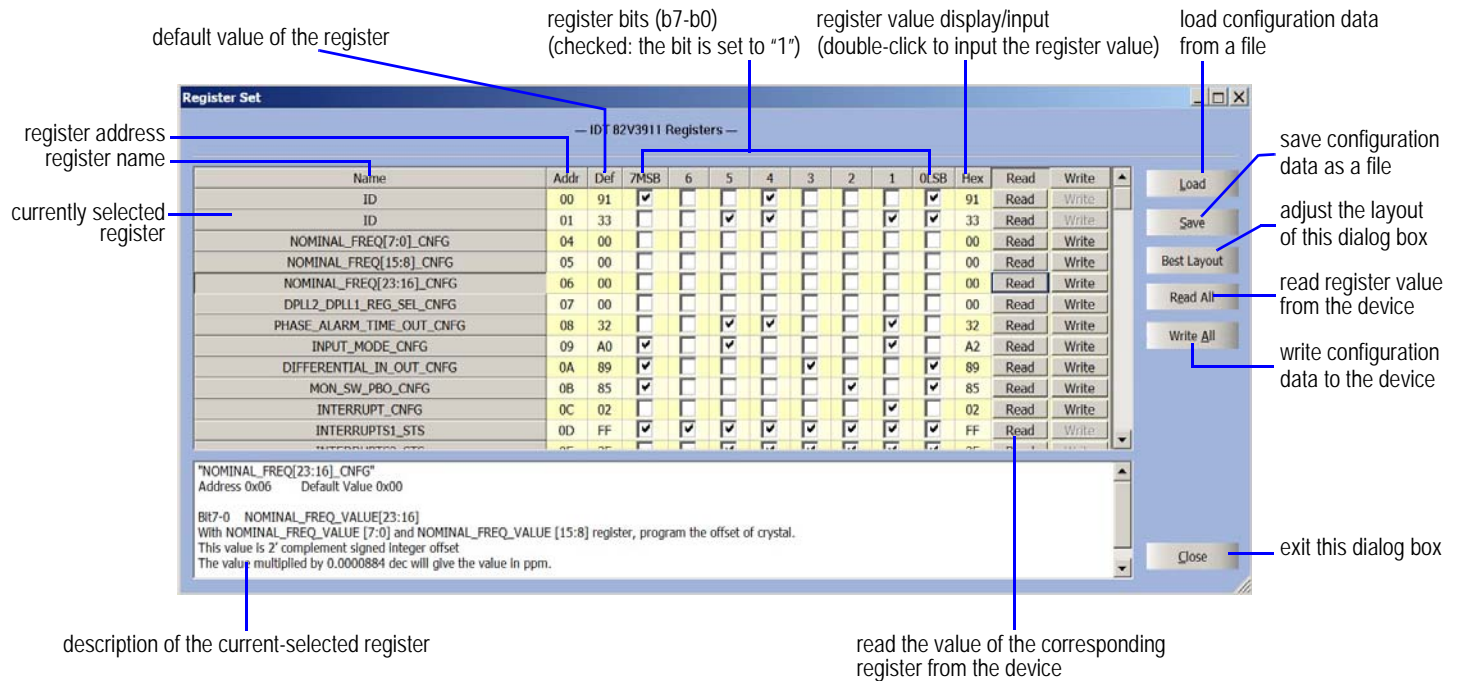


Figure-33 Register Set I Dialog Box

◆ Register Set II Dialog Box

Select "Window > Register Set II". The Register Set II dialog pops up as shown in Figure-34. This dialog box provides a convenient way to access a group of registers that have related functions.

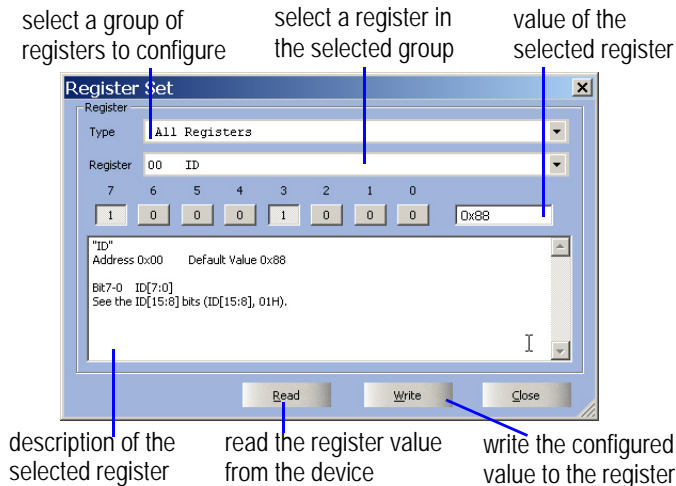


Figure-34 Register Set II Dialog Box

2.9.2 INTERRUPTS CONFIGURATION

Click on "Interrupt" or select "Window > Interrupt Window". The Interrupt dialog box pops up as shown in Figure-35.

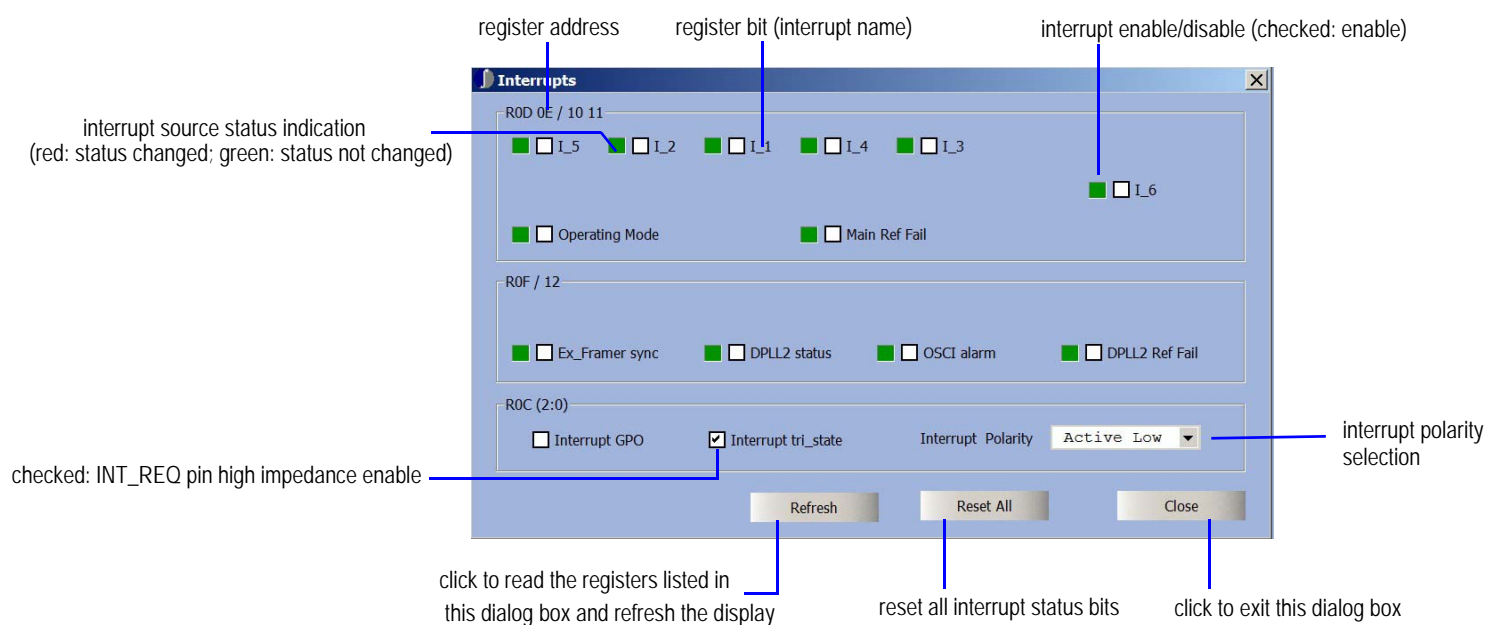


Figure-35 Interrupt Dialog Box

2.10 DPLL STATUS INDICATION

The DPLL status indication area is as shown in Figure-36. Users can choose to show DPLL1 or DPLL2 status. Here shows the situation that DPLL1 is selected.

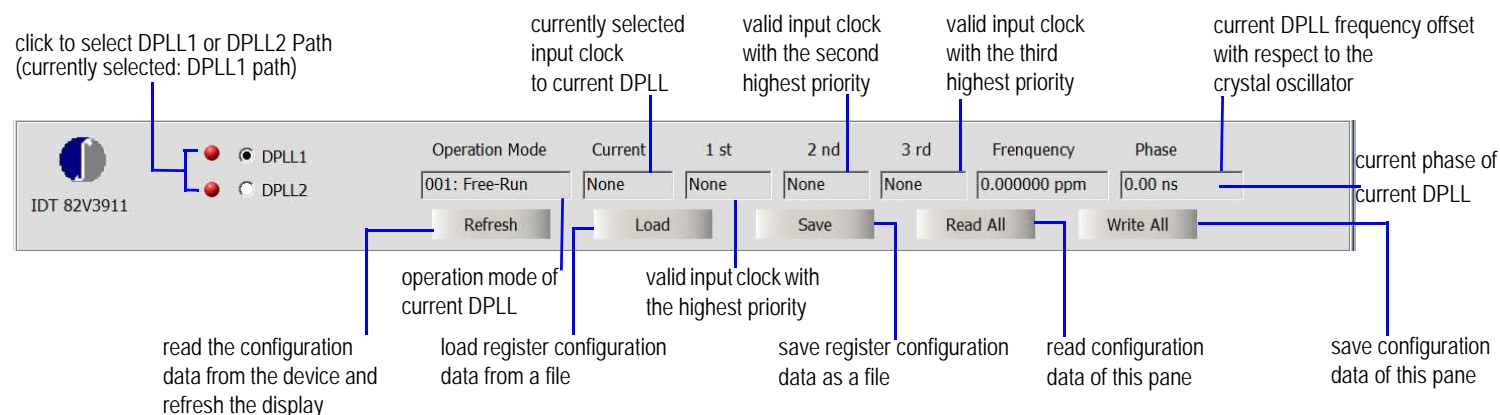


Figure-36 DPLL1/DPLL2 Path Selection and DPLL Status Indication

2.10.1 CURRENT DPLL STATUS

Select "Tools>Current DPLL Status" from the menu bar. The pop-up dialog box provides a convenient way to read CURRENT_DPLL_PHASE[15:0] and CURRENT_DPLL_FREQ[23:0] data.

Right click on either the Current Phase or the Current Frequency graphic area in Figure-37, a list of context menu items pops out, as shown in Figure-38. Select the "Setup" item, the Graphic Properties dialog box then pops out as shown in Figure-39.

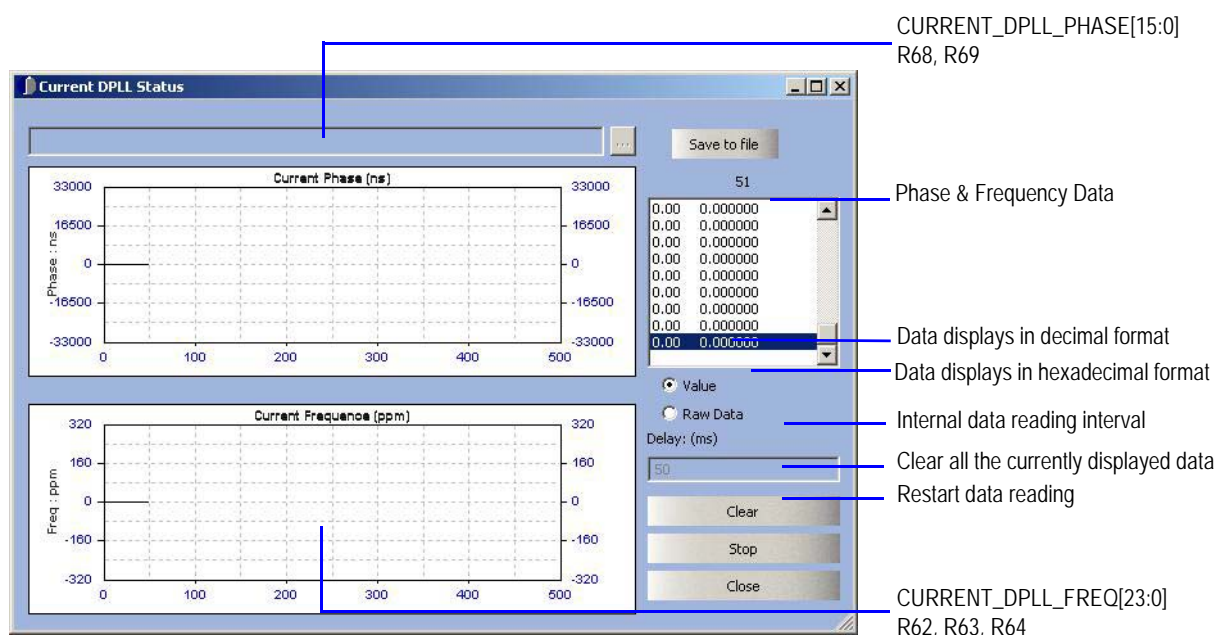


Figure-37 Current DPLL Status

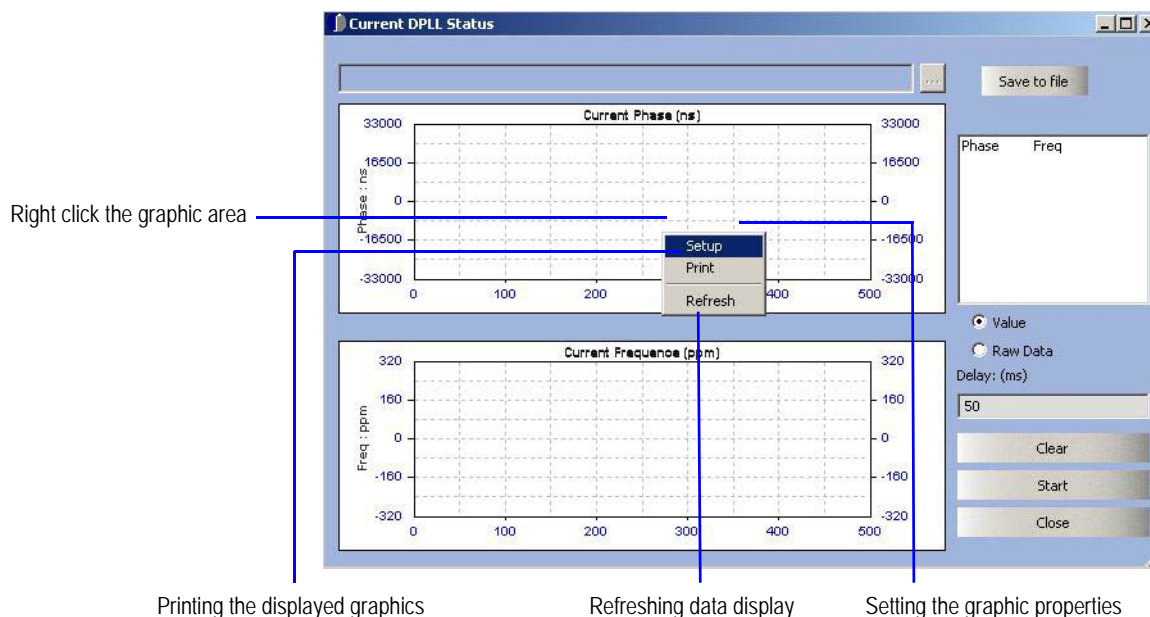


Figure-38 Context Menu Items

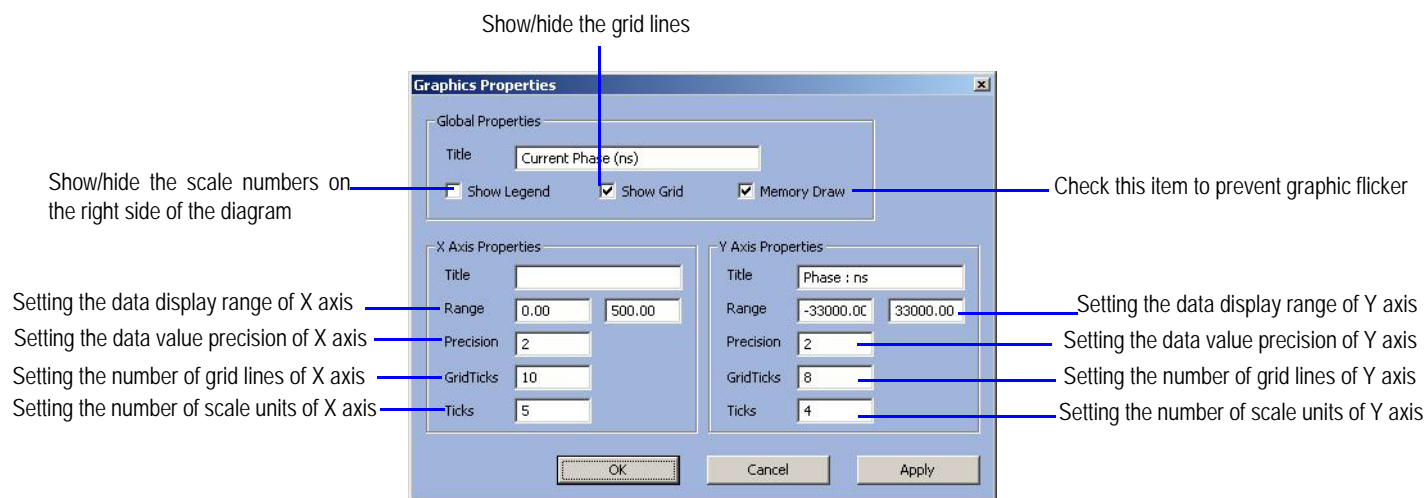


Figure-39 Graphic Properties Dialog Box

2.11 PAGE 1 REGISTERS CONFIGURATION

Click the button of Page 1 Registers Access in the main window, the user can configure the registers in the page 1. See [Figure-40](#) for details.

Click on the button, then select the DFS enable

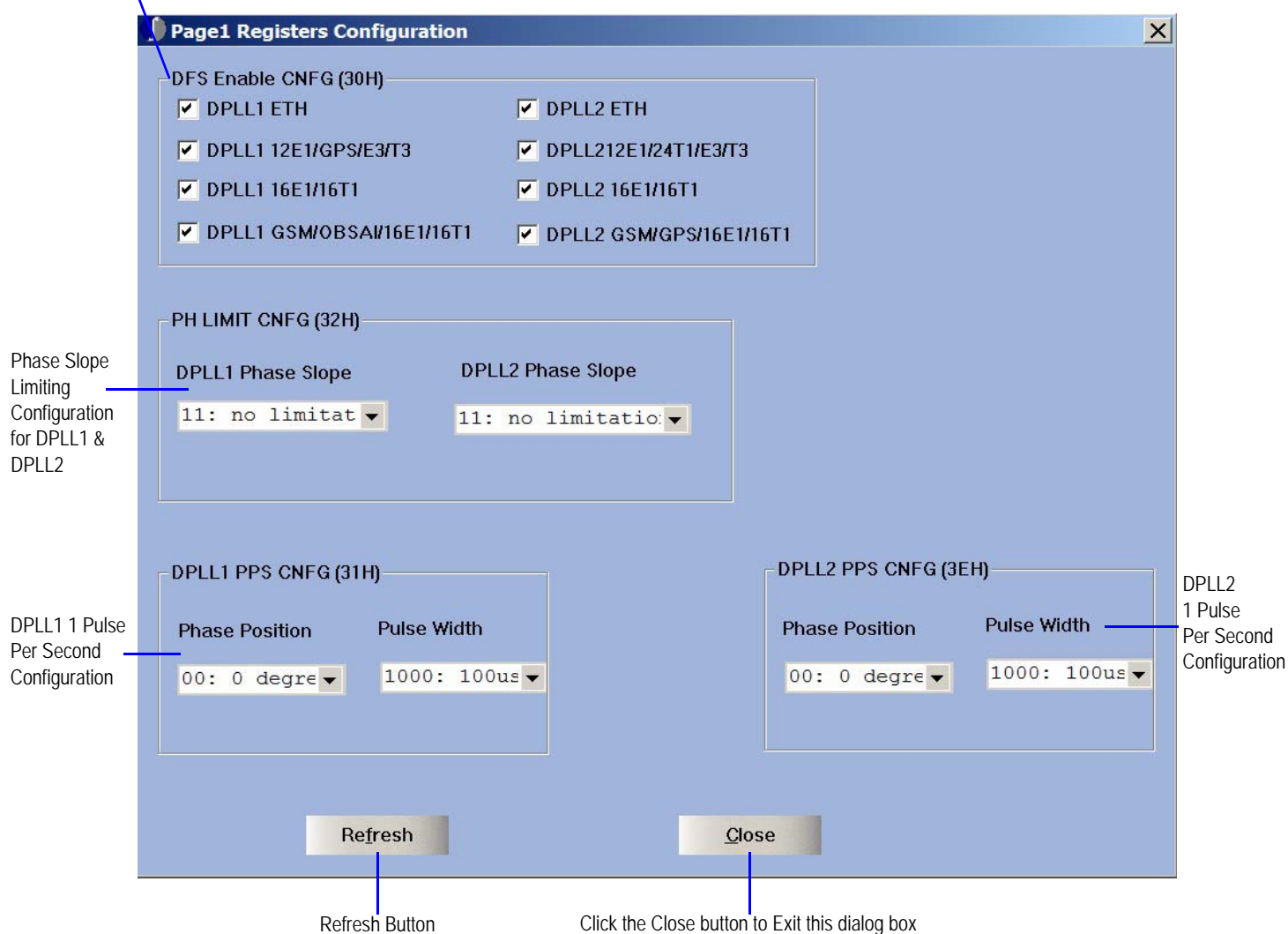
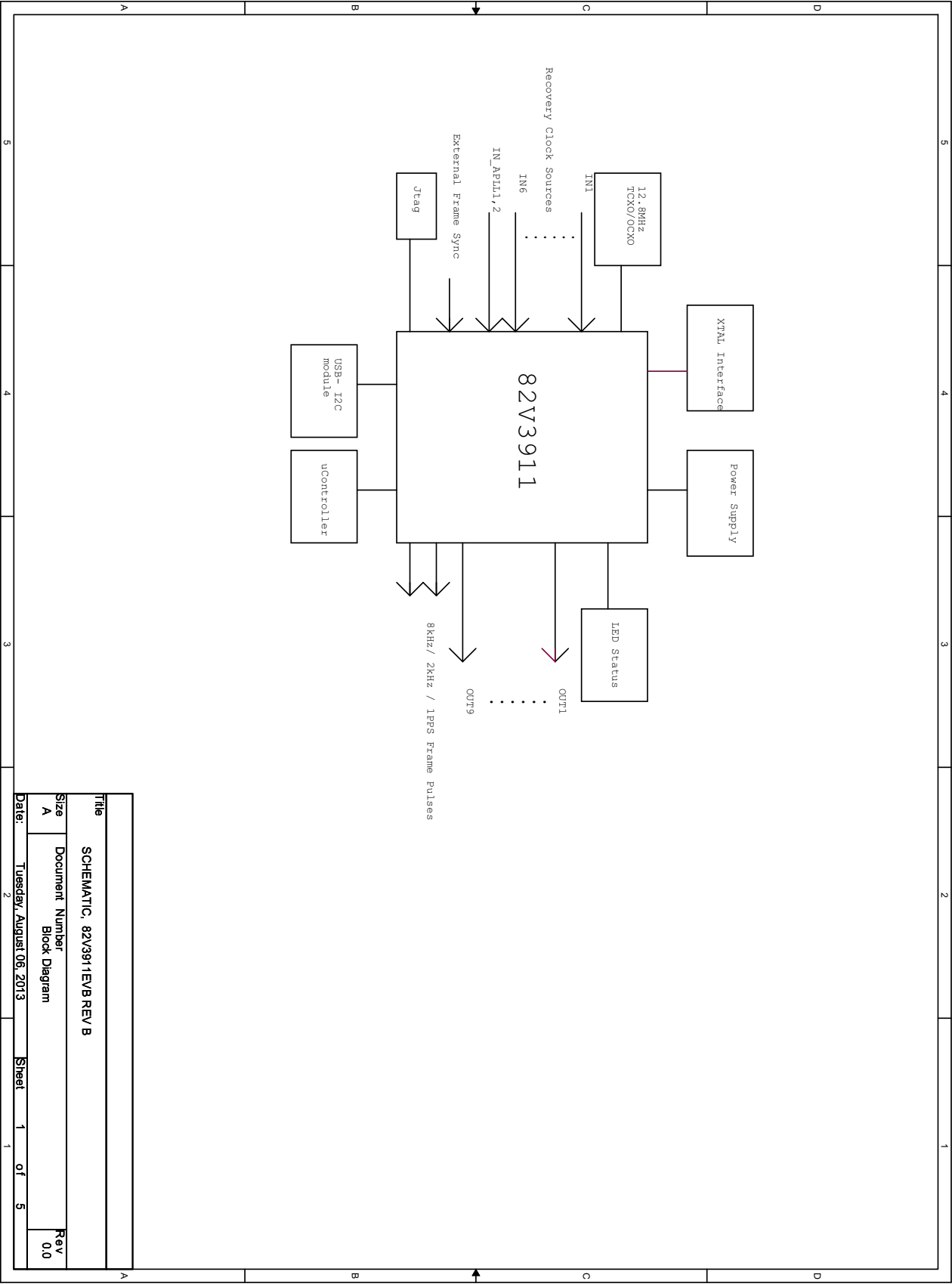
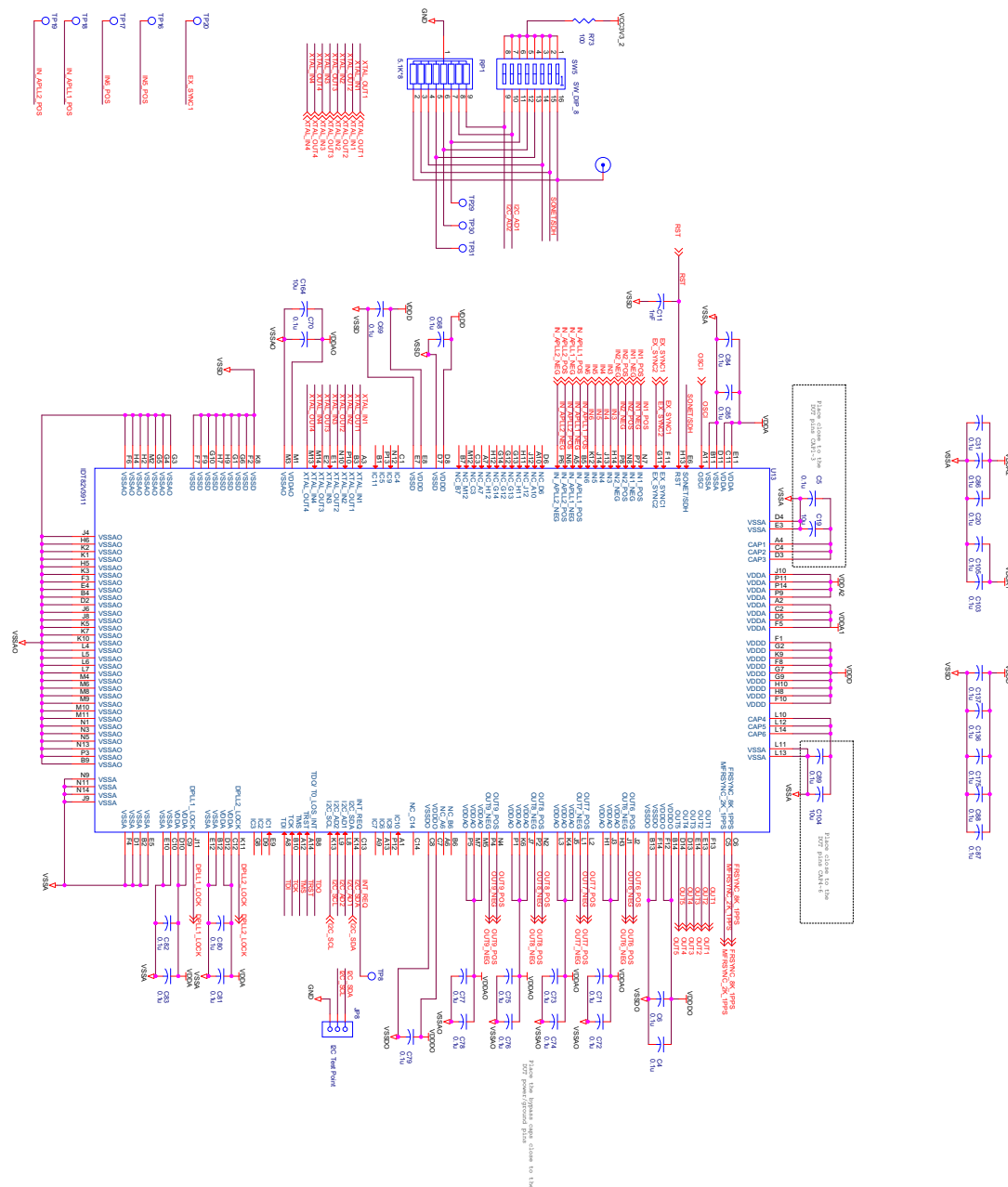


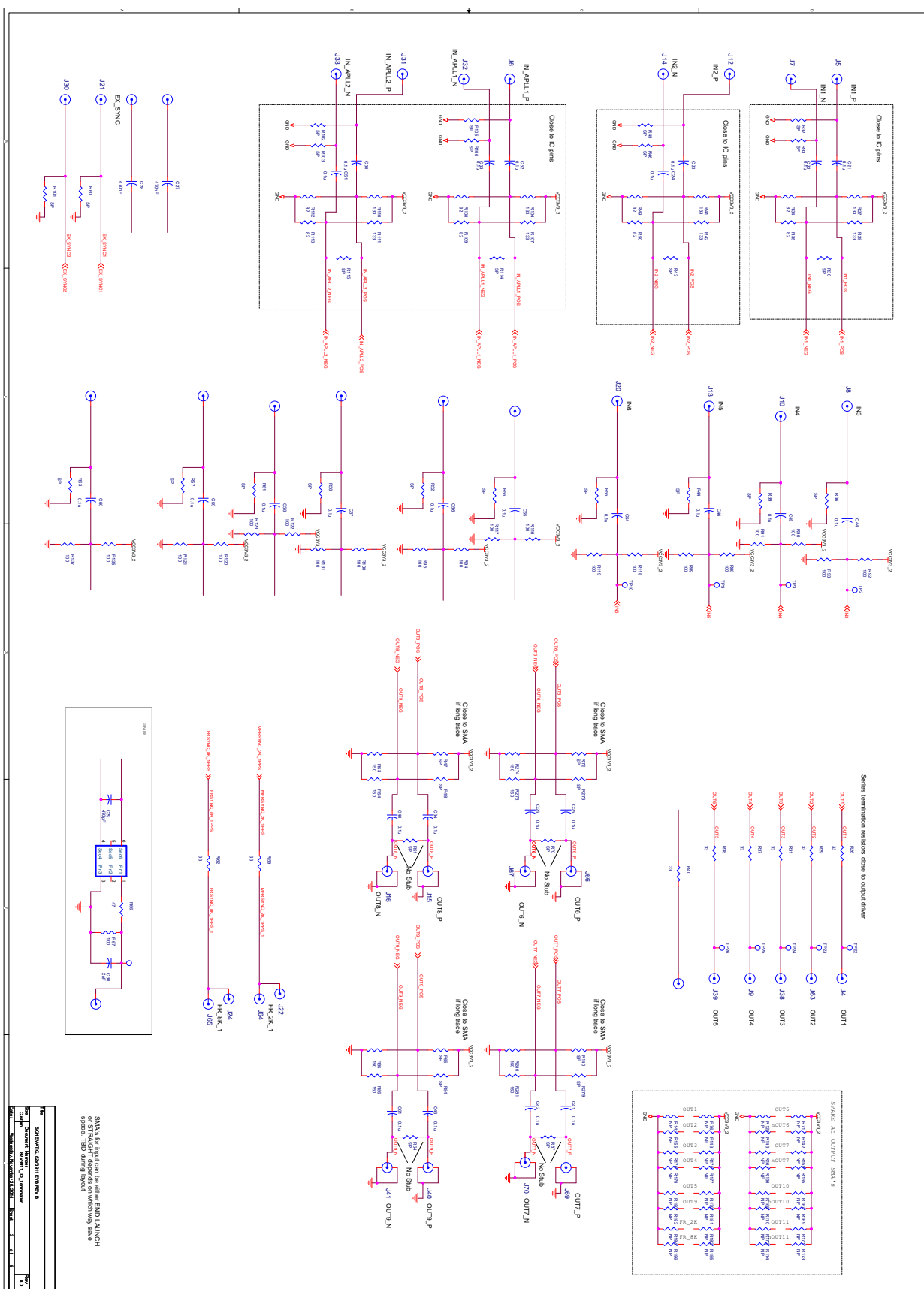
Figure-40 Page 1 Register Configuration

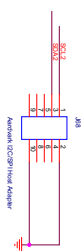
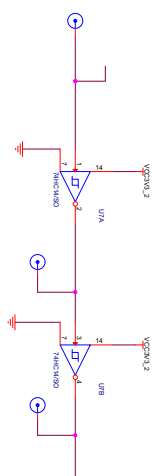
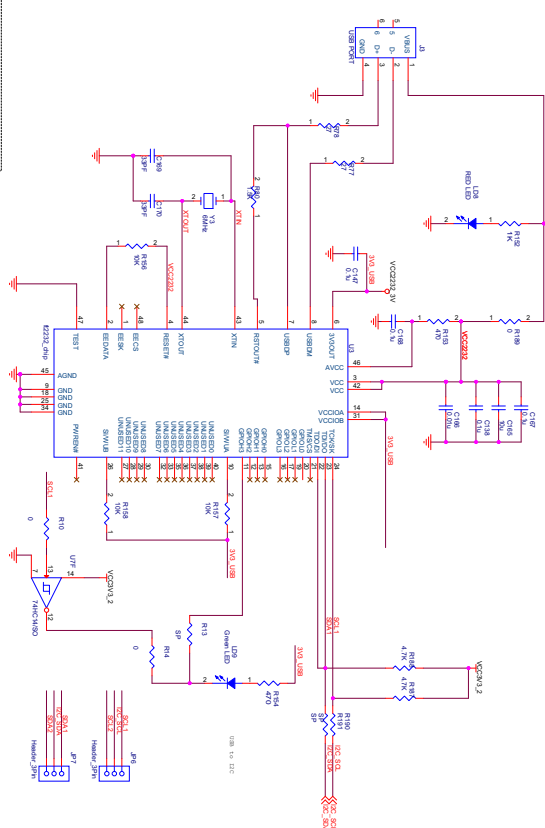
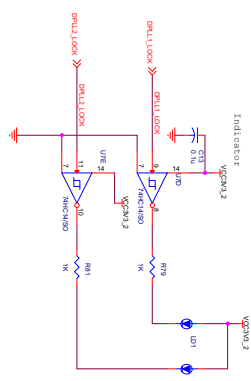
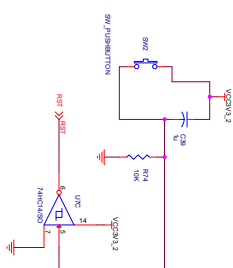
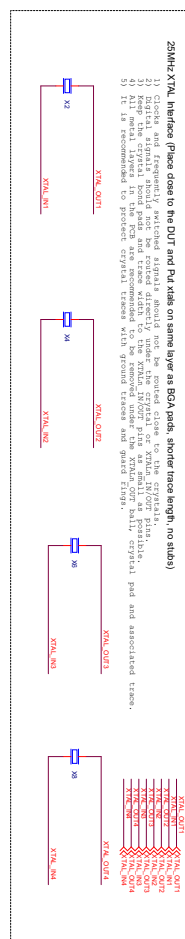
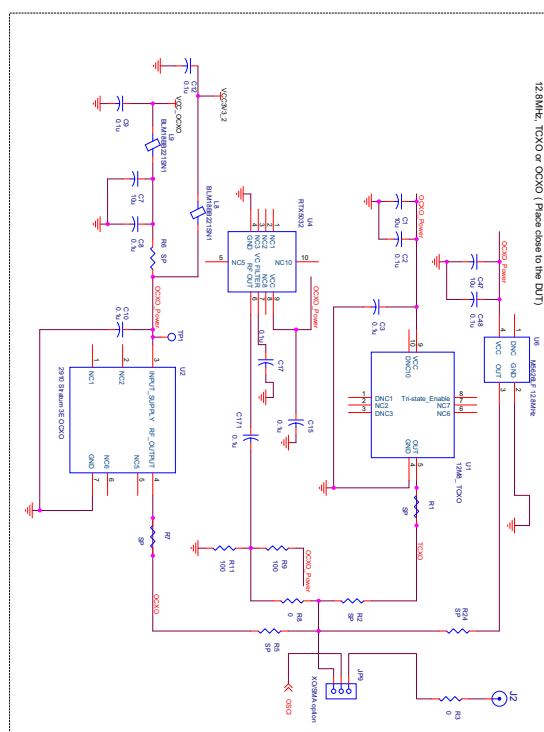
3 APPENDIX: SCHEMATIC FILE



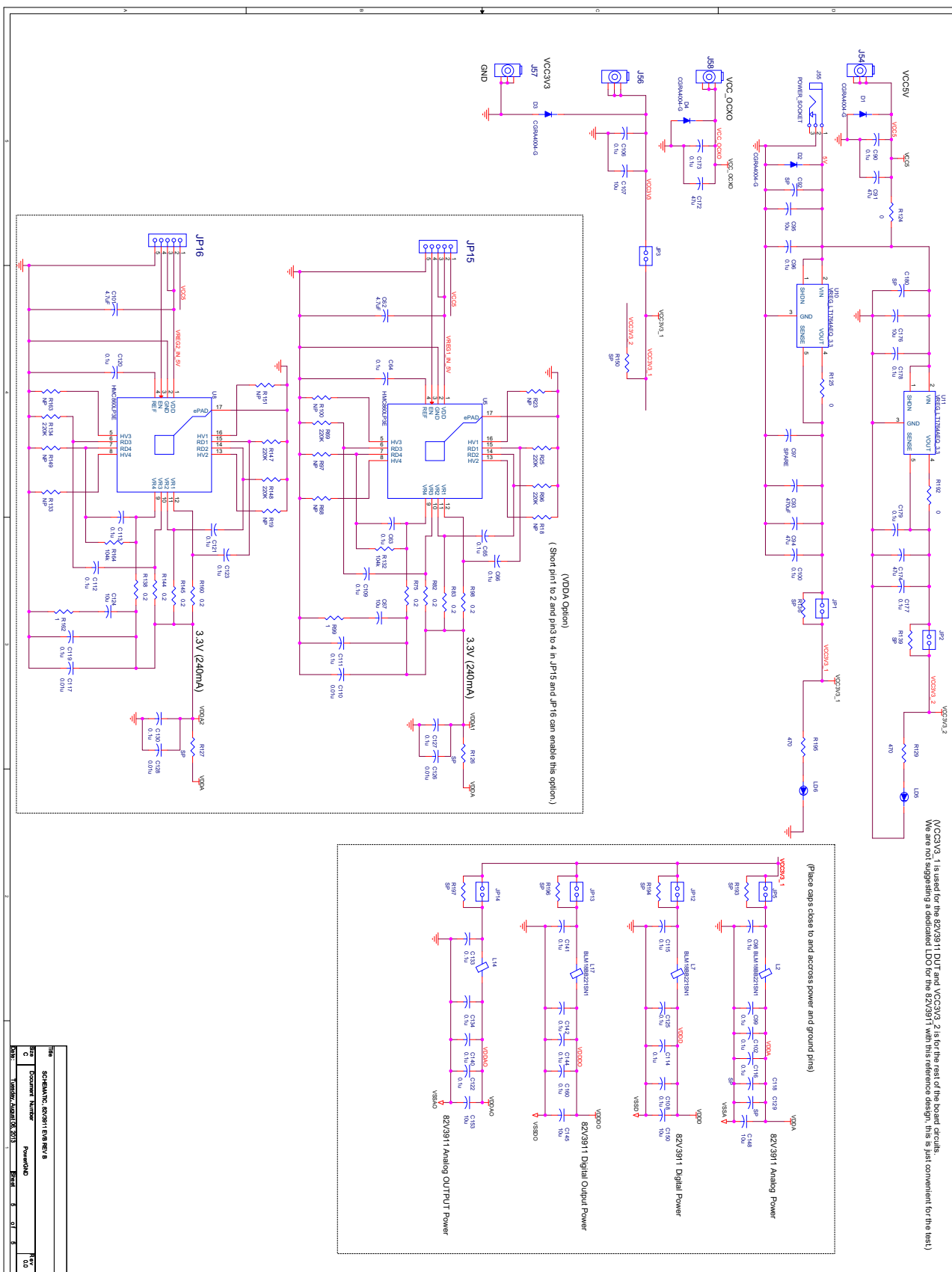


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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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