RENESAS VersaClock® 5 - 5P49V5935/33 Evaluation Boards

Introduction

The evaluation board is designed to help the customer evaluate the 5P49V5935/33, the latest addition to the family of programmable devices in IDT's Timing portfolio. When the board is connected to a PC running IDT Timing Commander™ Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Board Overview

Use the following diagram to identify: power supply jacks, USB connector, input and output frequency SMA connectors.

Figure 1. Board Overview
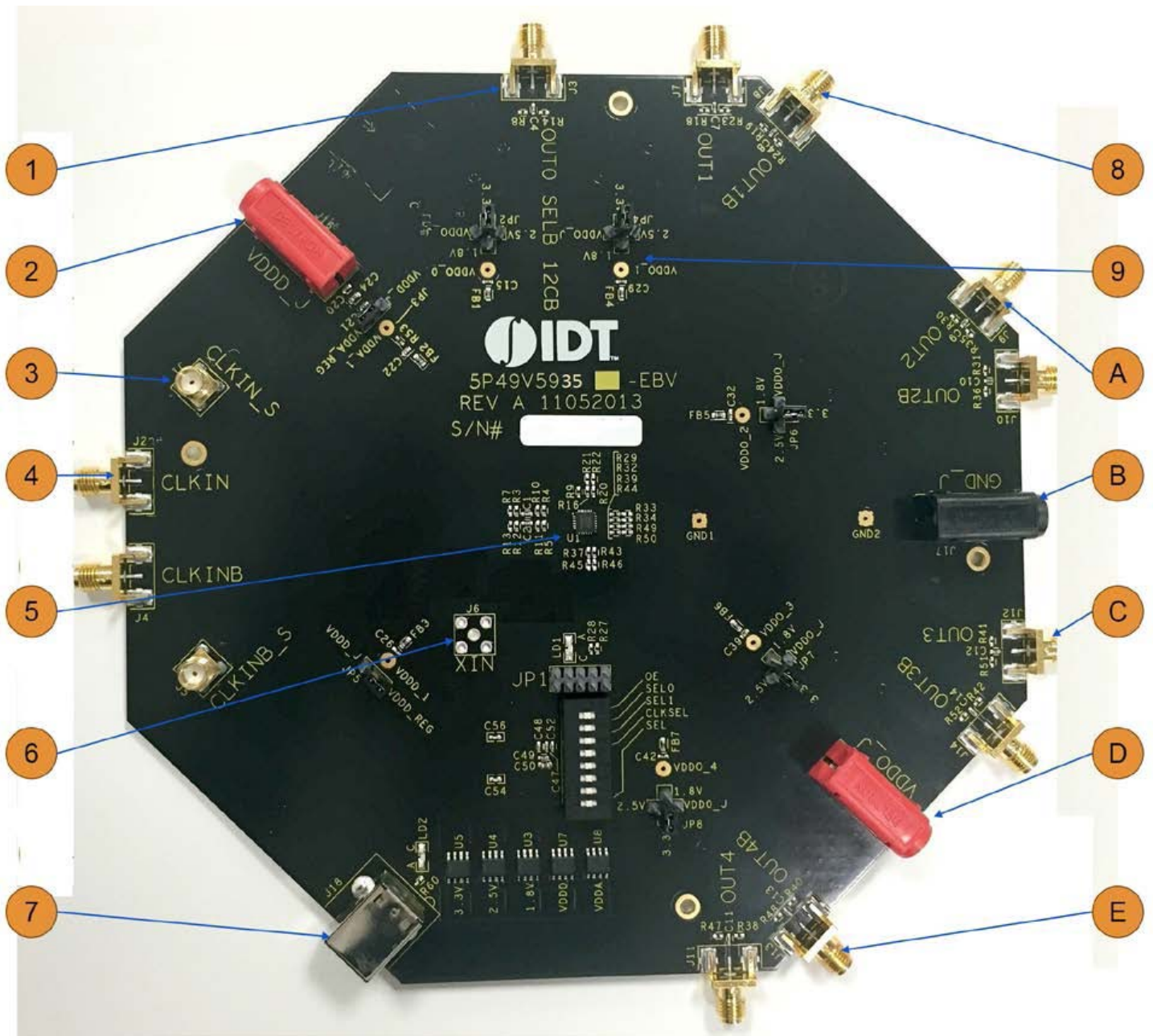
(1) OUT0 - This is a buffered output of the input reference clock, singled ended.

(2) Power supply jack, J16 – Connect to 3.3V, 2.5V or 1.8V for the core voltage of the device.

(3) CLKIN_S/CLKINB_S – SMA pair used to monitor the differential input CLKIN/CLKINB.

(4) Differential Input clock connector – A differential clock can be connected as a source for the device.

(5) 5P49V5935/33 – the device to be evaluated.

(6) XIN Connector – This SMA connector is for single-ended clock input. Please note the full swing of this input is 1.2V maximum.

(7) USB connector – Used this connector to connect with your PC to run IDT Timing Commander Software.

(8) OUT1 /OUT1B – Output 1. It can be a differential pair or two individual single-ended outputs. By default, it's an LVPECL differential output.

(9) Output voltage selector – 4-way header to select an output voltage. The center pin is the output voltage. Use the jumper to select from 1.8V, 2.5V or 3.3V. VDDO_J is the voltage from J15 (see E).

(A) OUT2/OUT2B – Output 2. It can be a differential pair or two individual single-ended outputs. By default, it's an LVPECL differential output.

(B) Ground Jack – J17. If J15 and/or J16 is used for power supply, this jack is the power return.

(C) OUT3/OUT3B – Output 3. It can be a differential pair or two individual single-ended outputs. By default, it's an LVPECL differential output. (OUT3/OUT3B is not populated on 5P49V5933 EVB.)

(D) Output Voltage Jack – J15. Connect to a voltage of 1.8V, 2.5V or 3.3V for output voltages.

(E) OUT4/OUT4B – Output 4. It can be a differential pair or two individual single-ended outputs. By default, it's an LVPECL differential output. (OUT4/OUT4B is not populated on 5P49V5933 EVB.)
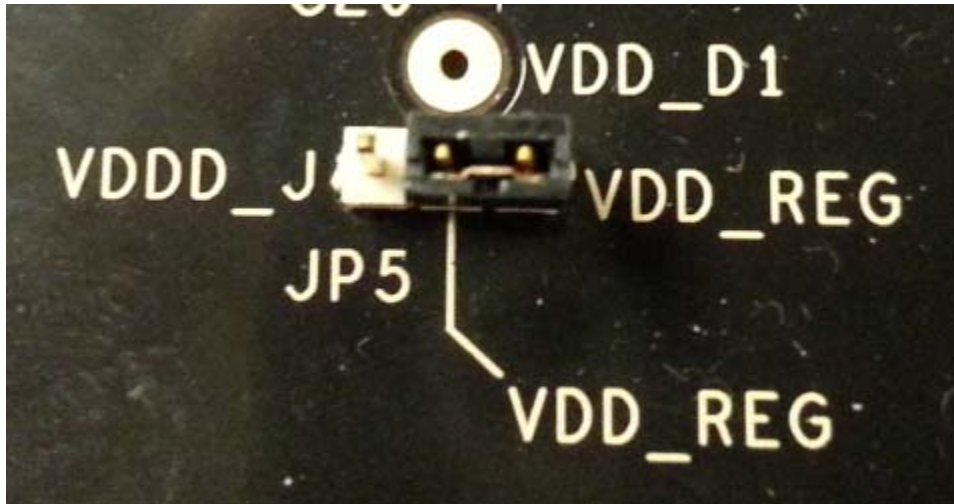
Board Power Supply

• Core Voltages

The core voltage includes a digital voltage VDDD and an analog voltage VDDA. Both core voltages can be powered by an external bench power supply or by USB.

Bench Power Supply – To supply VDDD with a bench power supply, connect power to J16. To supply VDDA with a bench power supply, connect power to J15. In the same time, place the jumpers in JP3 and JP5 to connect VDDA_J and VDDD_J, respectively.

USB Power Supply – When the board is connected to a PC through a USB cable, on-board voltage regulators will generate a 3.3V for the device. In this case, place the jumpers in JP3 and JP5 to connect VDDA_REG and VDDD_REG, respectively. See JP5 jumper position for VDDD_REG in the following figure. USB power source is recommended because it's readily available right from your laptop.

Figure 2. Jumping to the VDDD_J side will select external bench power supply; Jumping to the VDD_REG side will select power source from on-board regulators powered by USB


• **Output Clock Voltages**

Like VDDA and VDDD having two sources, each output voltage VDDO0~4 is also provided with two sources to choose from: bench power supply or powered from USB. The selection is made by a 4-way header as shown in Figure 3 below. Jumping to VDDO_J will select external power supply (JP15 and JP16 are connected to external power supply); Jumping to 1.8V, 2.5V or 3.3V will select each respective voltage from on-board voltage regulators powered by USB port.

Please note: each output voltage can be individually selected. Use the label on the evaluation board: VDDO_0 for OUT0, VDDO_1 for OUT1, VDDO_2 for OUT2, VDDO_3 for OUT3, and VDDO_4 for OUT4 (5P49V5933 has only two outputs – OUT1/OUT1B and OUT2/OUT2B whereas, 5P49V5935 has 4 outputs – OUT1/OUT1B, OUT2/OUT2B, OUT3/OUT3B and OUT4/OUT4B).

Figure 3. Use the jumper to select a voltage for OUT3: 1.8V/2.5V/3.3V is from on-board voltage regulators powered by USB; VDDO_J is from external power supply connecting to JP15 and JP16
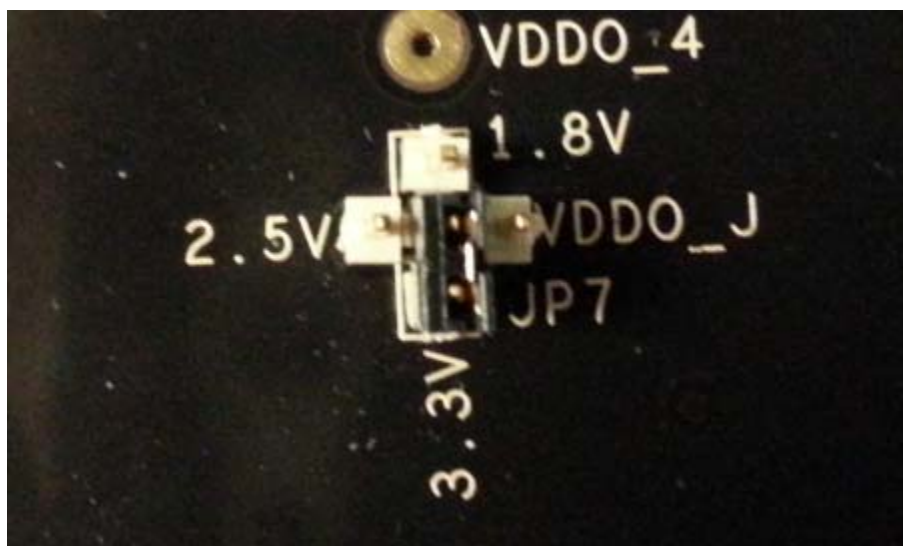
Connecting the Board

The board is connected to a PC through a USB connector for configuring and programming the device, as shown in Figure 4 below. The USB interface will also provide +5V power supply to the board, from which on-board voltage regulators generate various voltages for the core as well as for each output.

The board can also be powered by a bench power supply by connecting two banana jacks J15, J16 for output and core voltages, respectively. Please see board power supply section for details.

Figure 4. Connecting the Board with USB Port for Communications with Timing Commander Software
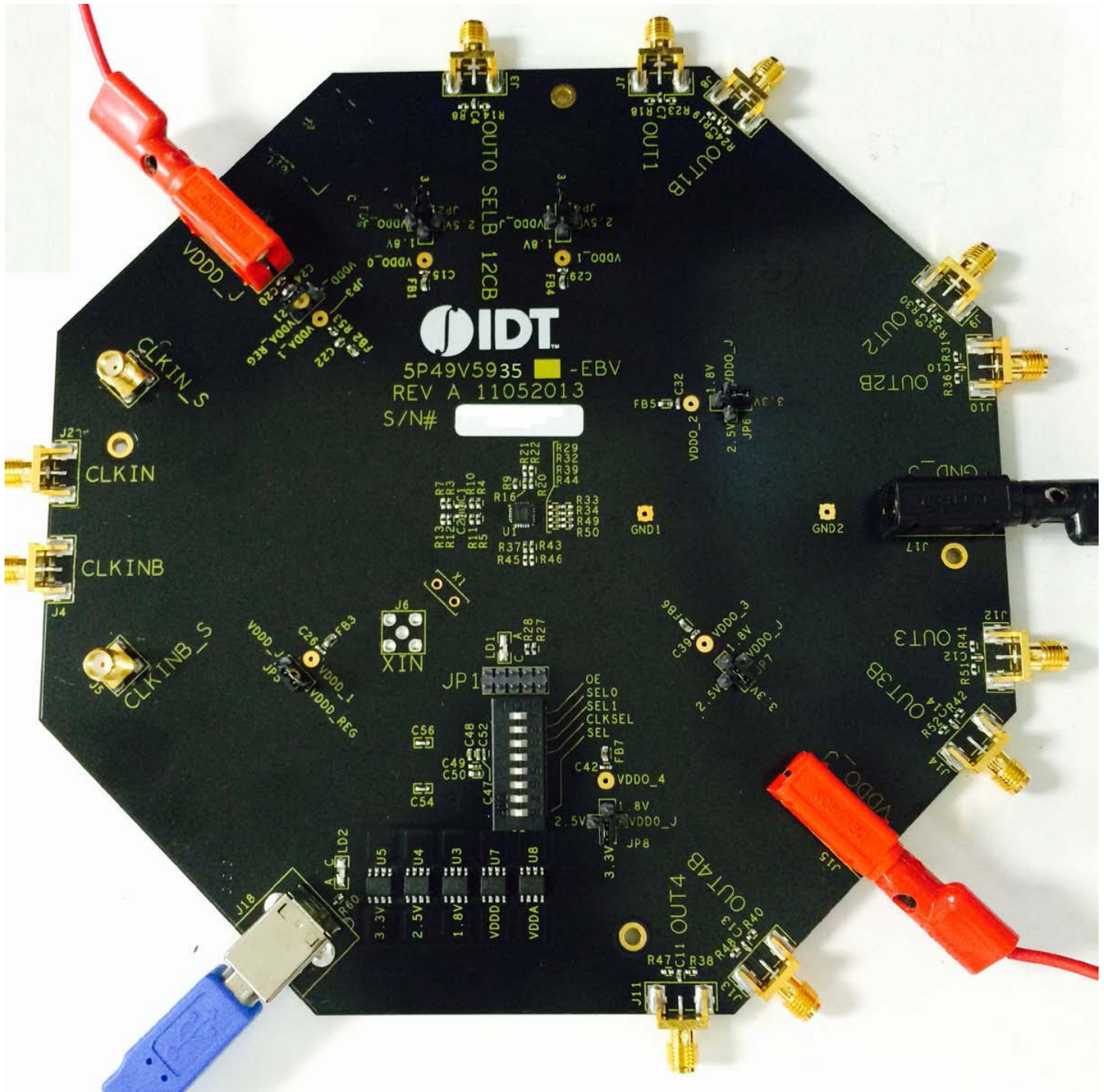
Configuration and Setup

The 5P49V5935/33 EVB do not need an on board crystal since it is integrated inside the device. An external clock can still be supplied to CLKIN/CLKINB connectors. The device will have two default outputs: OUT0 = 25MHz, OUT1 =100MHz when powered up.

Use the following steps to setup the board using I^2C and start the configuration of the board.

1. Set SEL pin (pin 8) of dip switch (U2) to "0" to select I2C mode.

2. Connect J18 to a USB port of the PC using the supplied I2C cable.

3. Power up the board.

4. Launch Timing Commander Software (refer to VersaClock5 Timing Commander User Guide - Getting Started Step 1~7). Following the Getting Started steps in the Timing Commander software, an I^2C connection is established between the GUI software and chip.

5. First load the personality file 1.30 and select 5P49V5933 or 5P49V5935 part number, then load the setting file into the GUI and start configuring the IC.

6. All intended outputs should be available for measurement.

Board Schematics

Evaluation board schematics are shown on the following pages.

Figure 5. VersaClock 5 Evaluation Board Schematics – Page 1
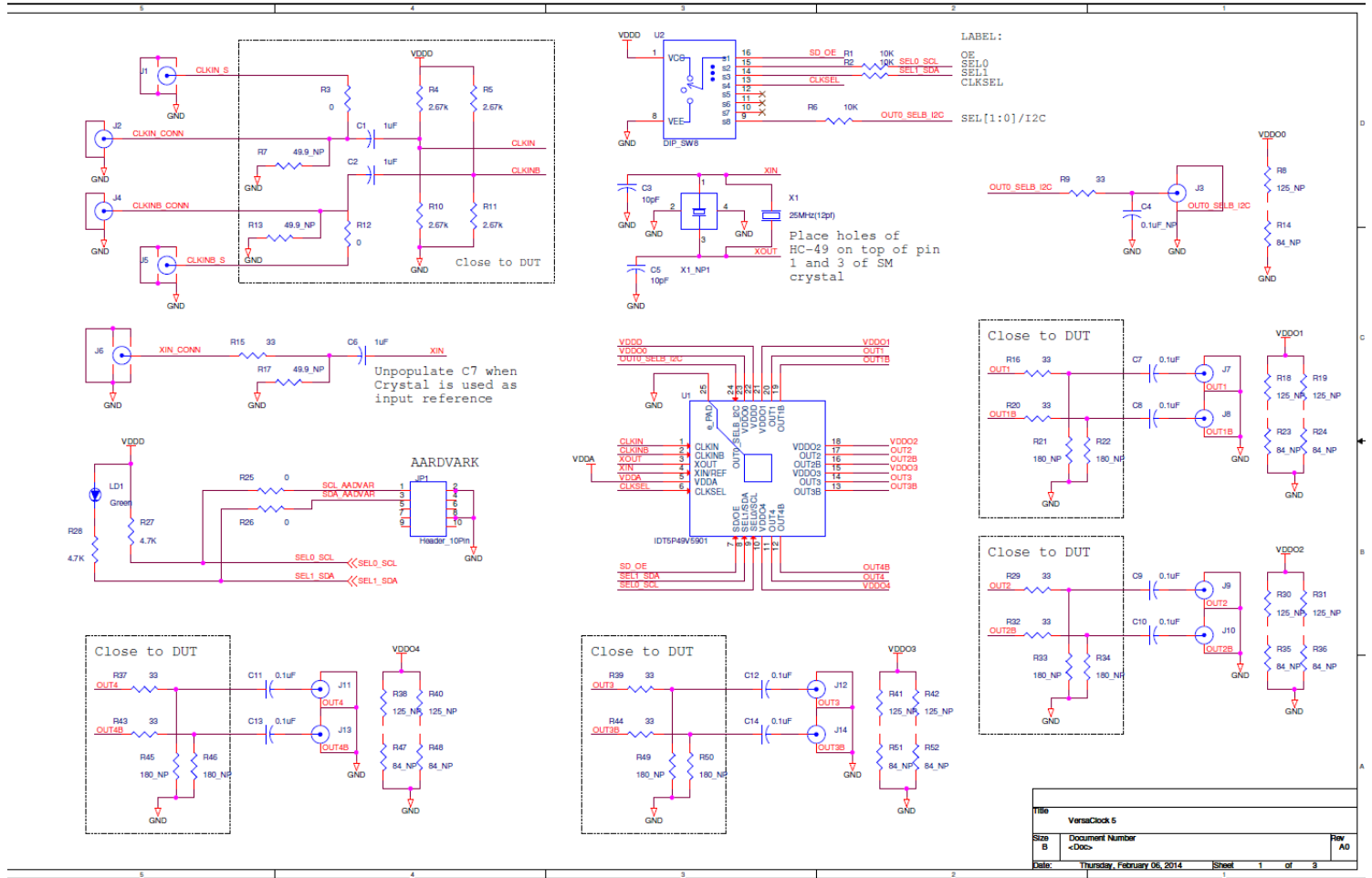
Figure 6. VersaClock 5 Evaluation Board Schematics – Page 2
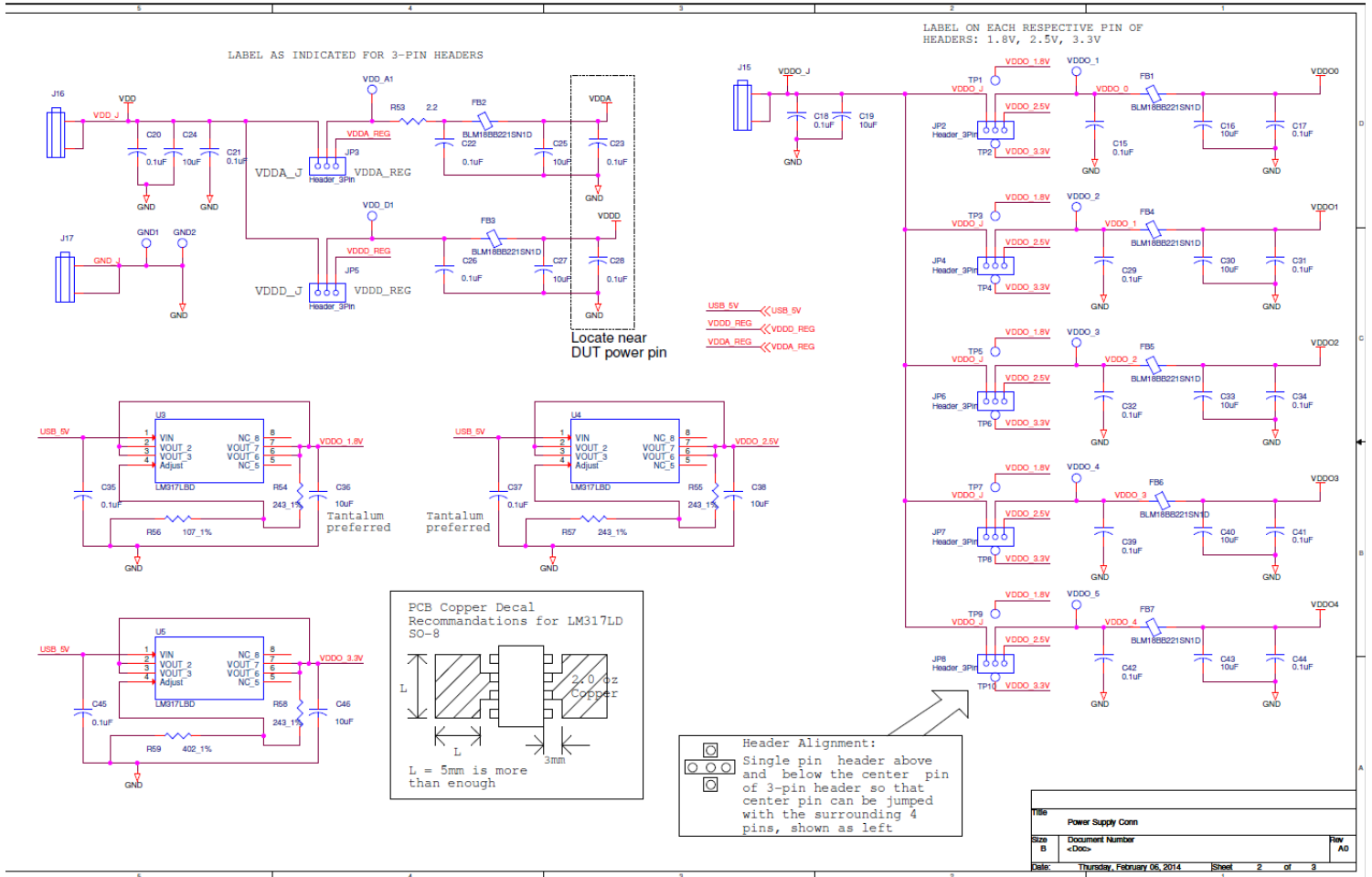
Figure 7. Evaluation Board Schematics – Page 3
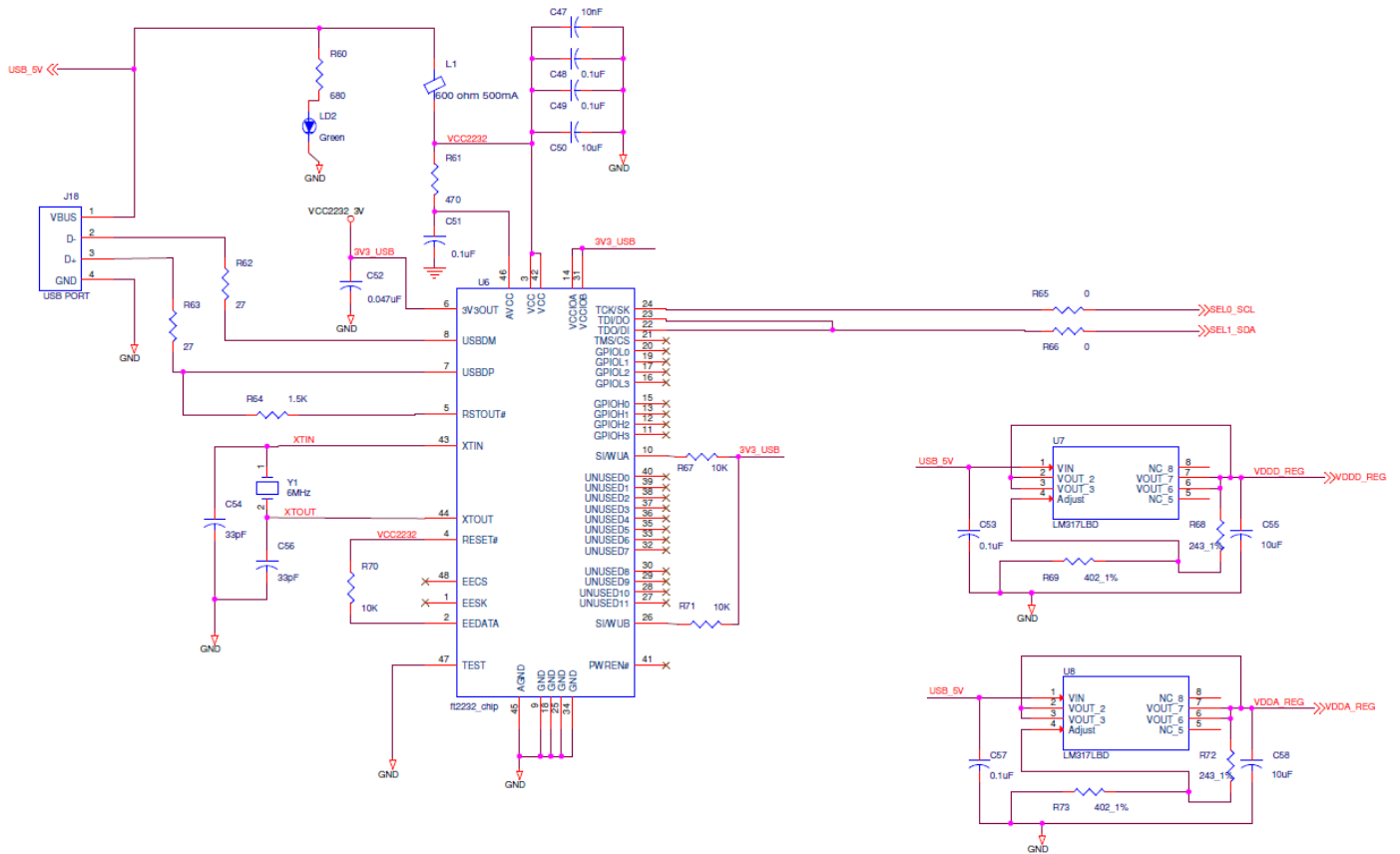
Signal Termination Options

Termination options for OUTPUT1 – 4 in the evaluation board are displayed in Figure 8. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not-populating) some resistors. DC or AC coupling of these outputs are also supported.

Tables1 – 2, below, tabulates component installations to support LVPECL, HCSL, LVCMOS and LVDS signal types for OUTPUT1 – 4, respectively. Please note that by doing so, the output signals will be measured and terminated by an oscilloscope with a 50Ω internal termination.

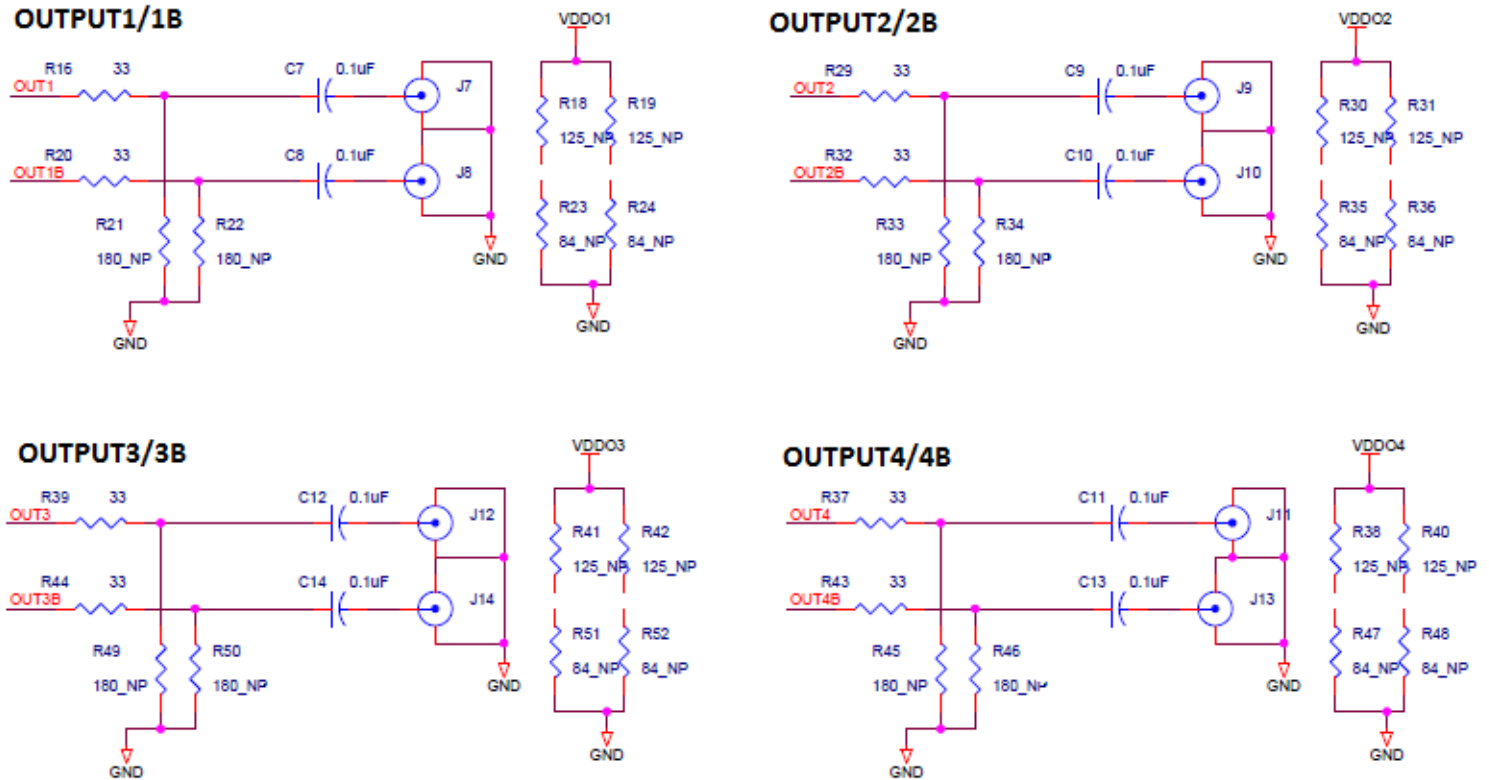## Figure 8. Output Termination Options

Table 1. 5P49V5933 EVB Output Termination

Output Number	Signal Type	Series Resistors	180-ohm pull-down	Series Capacitor	Resistor Network
OUTPUT1	LVPECL	R16=R20=0 Ω	R21, R22 installed	C7=C8=0.1 µF	R18, R19, R23, R24 not installed
OUTPUT2	LVDS	R29=R32=0 Ω	R33, R34 not installed	C9=C10=0.1 µF	R30, R31, R35, R36 not installed

Table 2. 5P49V5935 EVB Output Termination

Output Number	Signal Type	Series Resistors	180-ohm pull-down	Series Capacitor	Resistor Network
OUTPUT1	HCSL	R16=R20=33 Ω	R21, R22 not installed	C7=C8=0 µF	R18, R19, R23, R24 not installed
OUTPUT2	LVDS	R29=R32=0 Ω	R33, R34 not installed	C9=C10=0.1 µF	R30, R31, R35, R36 not installed
OUTPUT3	LVPECL	R39=R44=0 Ω	R49, R50 installed	C12=C14=0.1 µF	R41, R42, R51, R52 not installed
OUTPUT4	LVCMOS	R37=R43=33 Ω	R45, R46 not installed	C11=C13=0.1 µF	R38, R40, R47, R48 not installed

Orderable Part Numbers

The following evaluation board part numbers are available for order.

Table 3. Orderable Part Numbers

Part Number	Description
EVKVC5-5935ALL	Evaluation board for 5P49V5935. Output termination configurations are described in Table 2.
EVKVC5-5933ALL	Evaluation board for 5P49V5933. Output termination configurations are described in Table 1.

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