

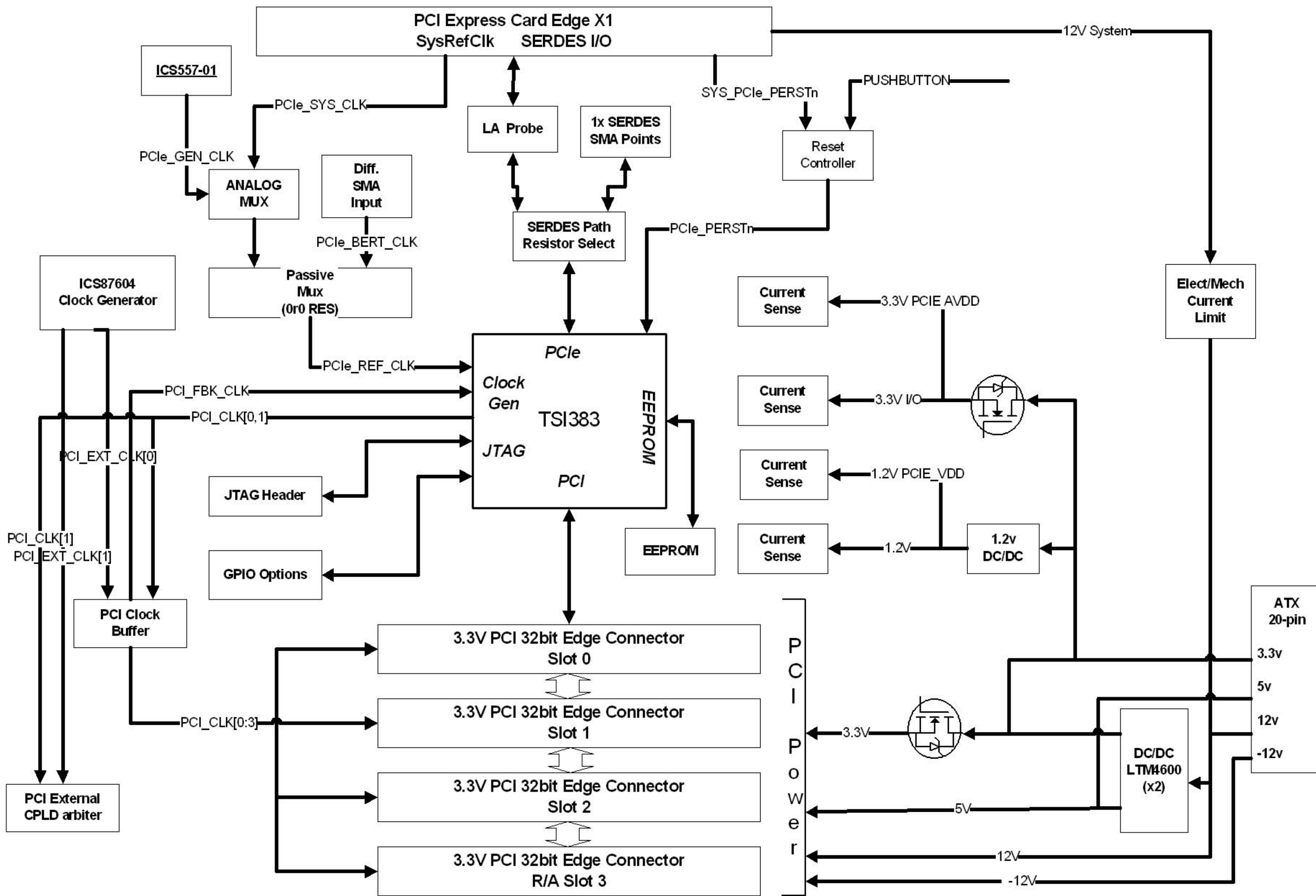
# Tsi383 (QFP) Evaluation Board Schematics

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# BLOCK DIAGRAM



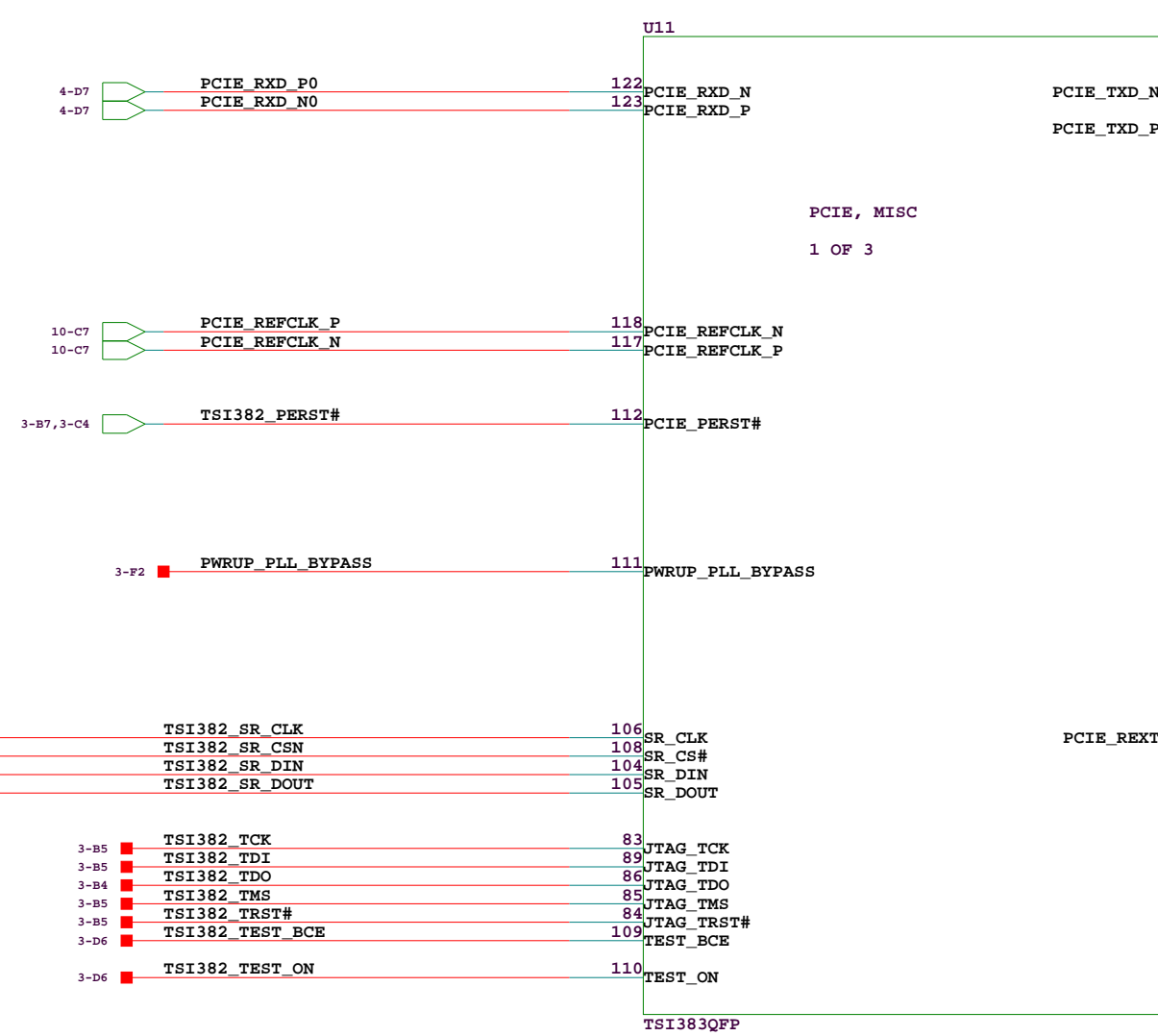
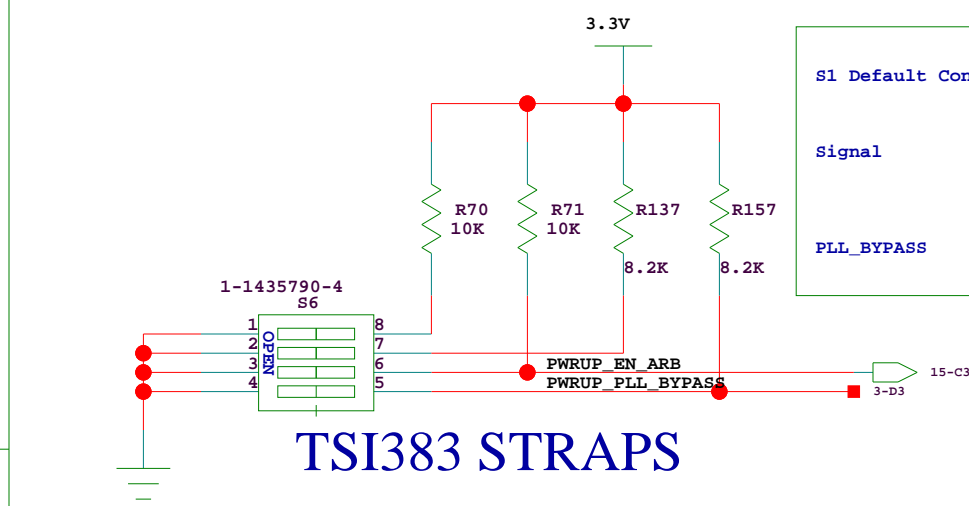
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SIZE <b>C</b>	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
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# TSI383 PCIE/MISC INTERFACE

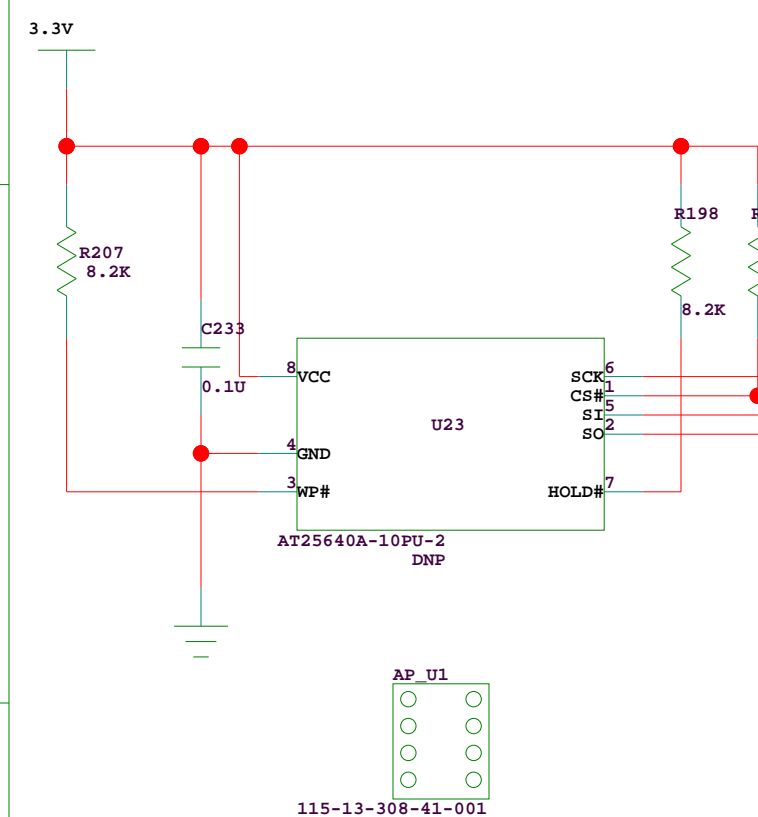
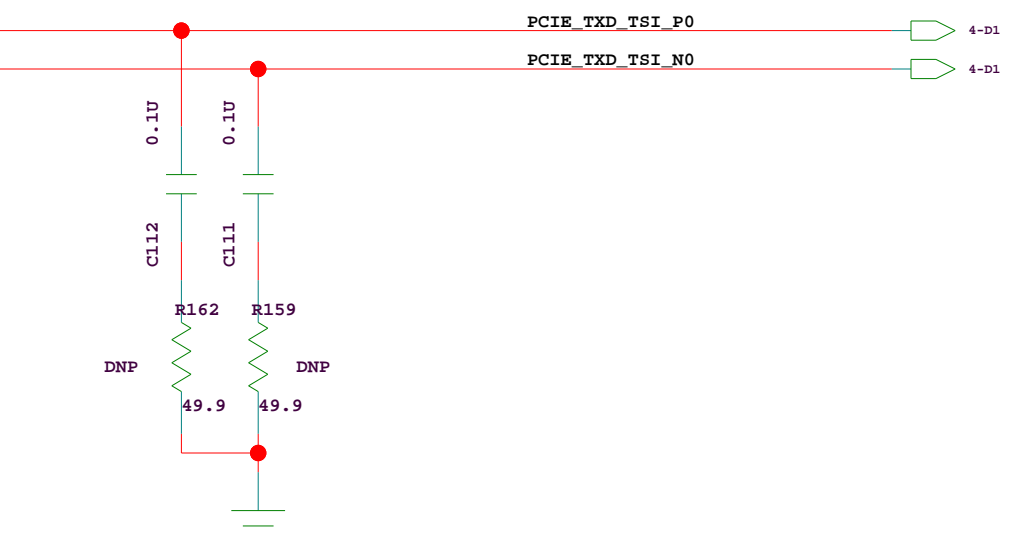
## TSI383 STRAPS

S1 Default Configuration

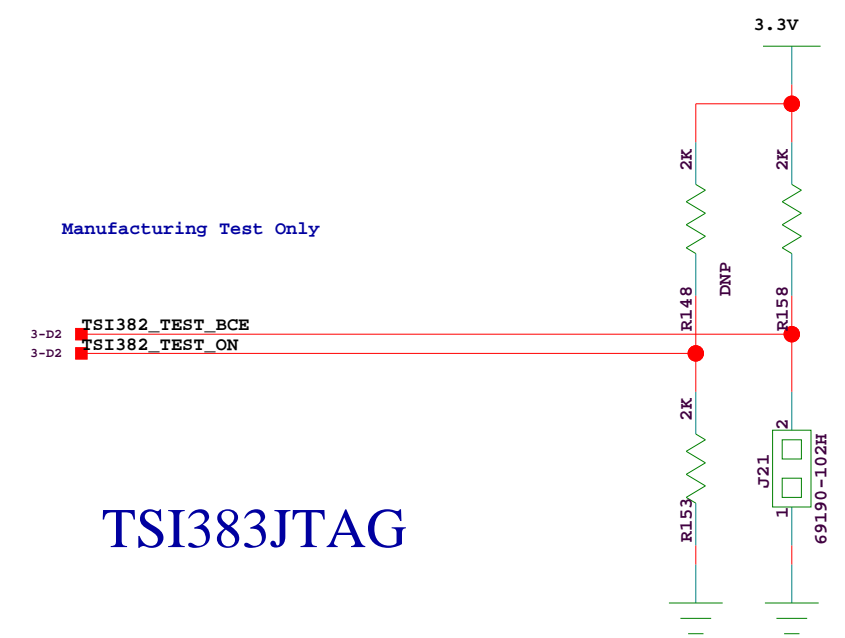
Signal	(1=High,0=Low)
PLL_BYPASS	0



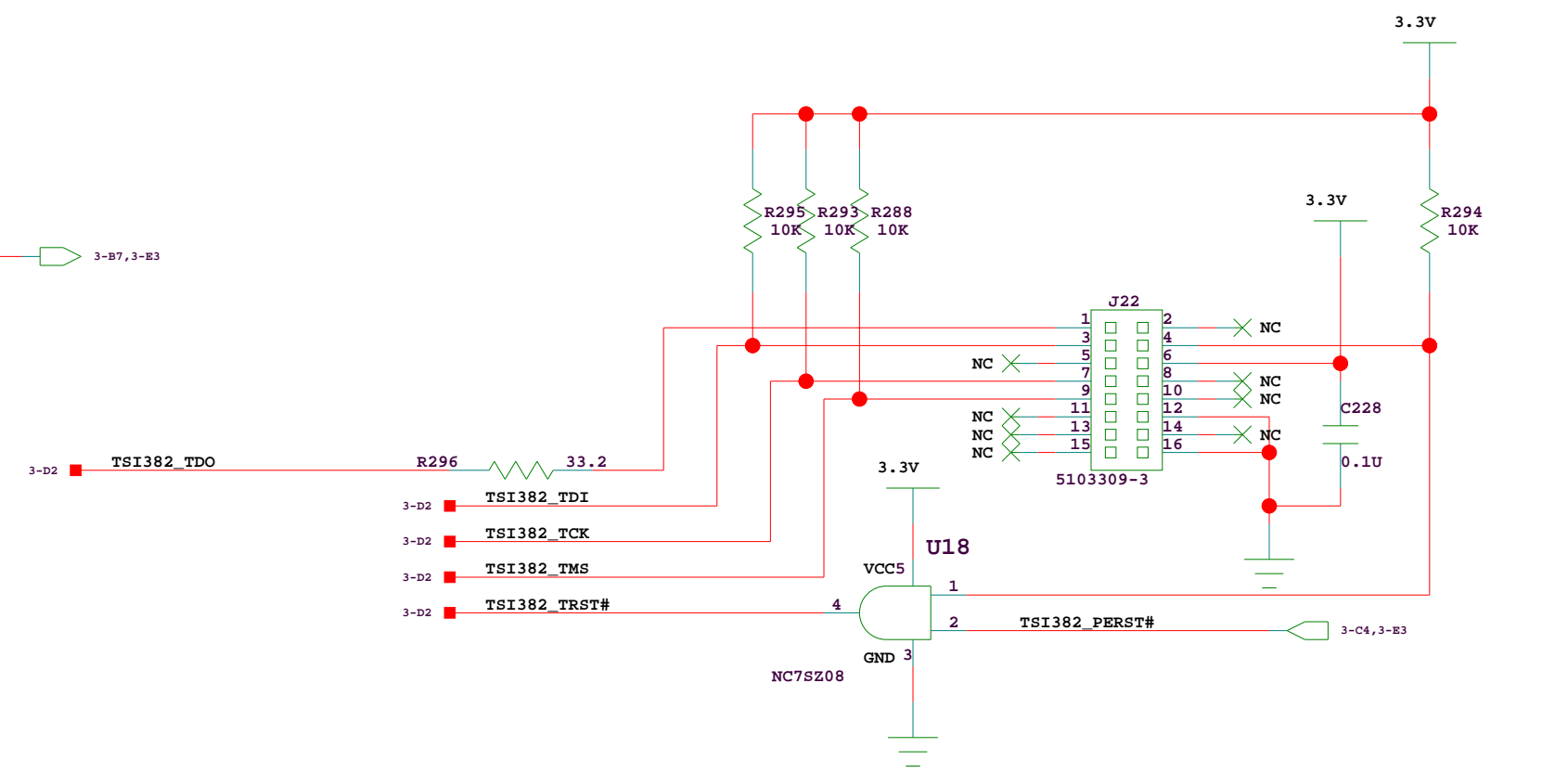
## TX Compliance Testing



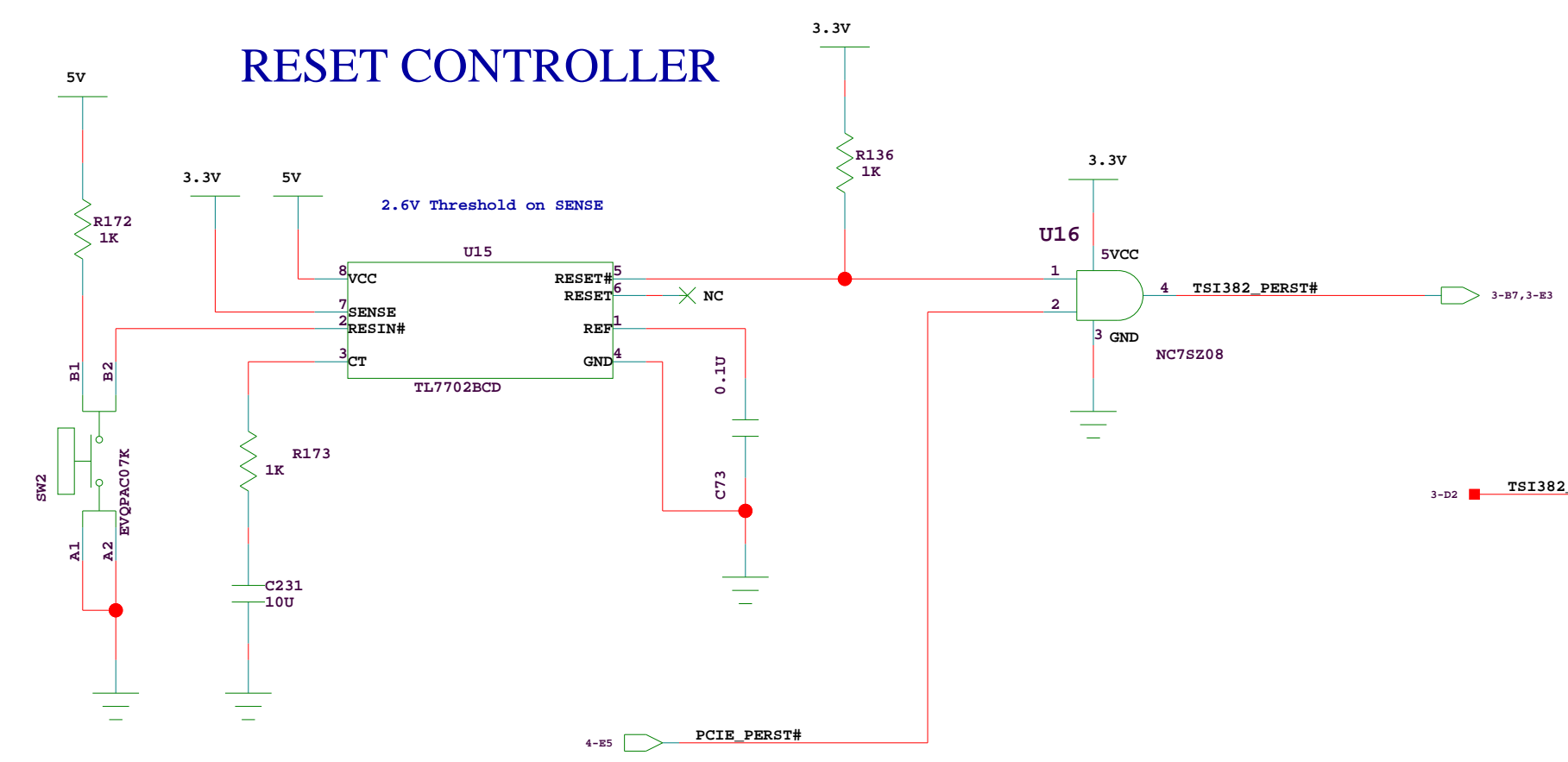
## Manufacturing Test Only



## TSI383JTAG

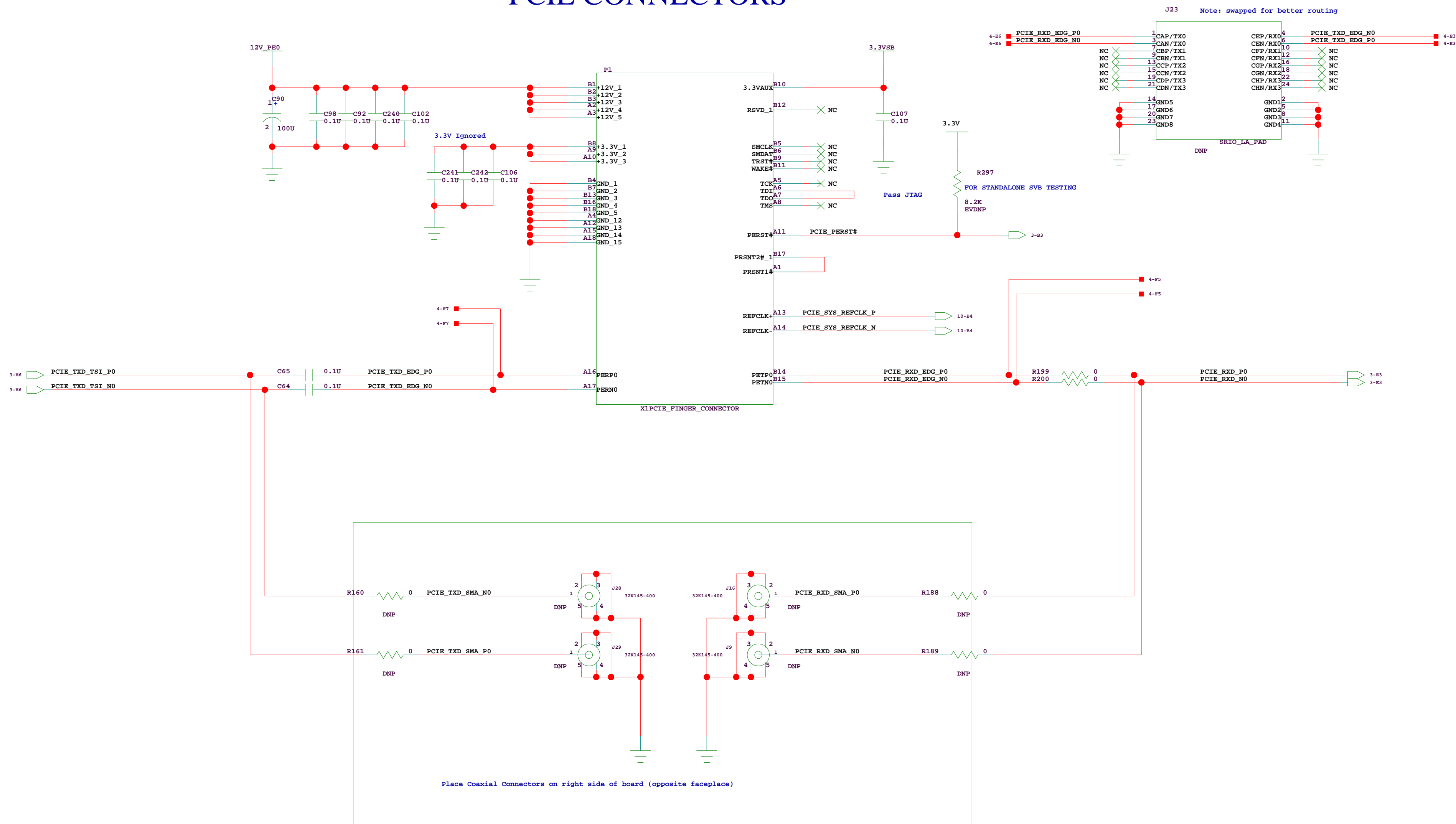


## RESET CONTROLLER



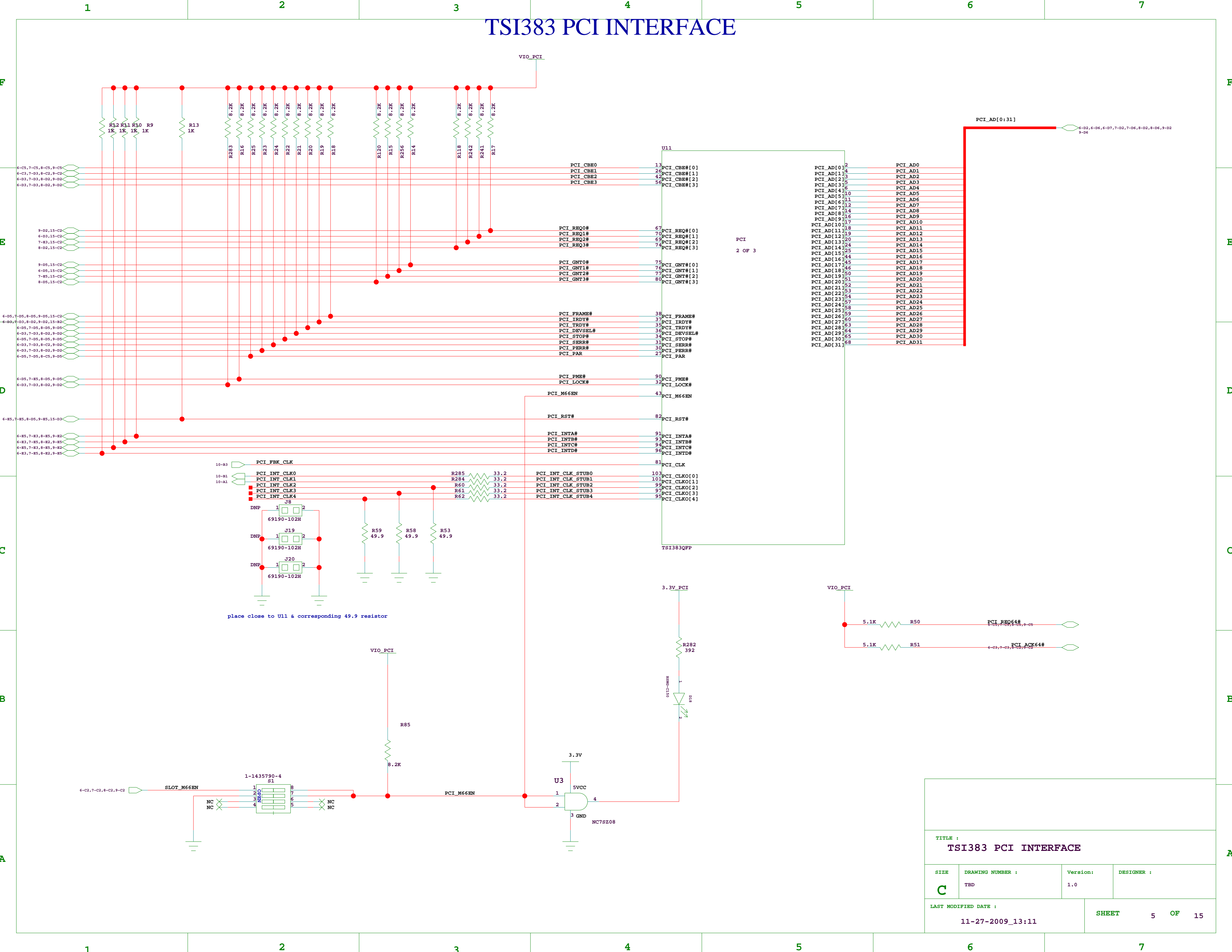
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LAST MODIFIED DATE : 11-27-2009_13:11		SHEET 3 OF 15	

# PCIE CONNECTORS



TITLE :			
PCIE CONNECTORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
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# TSI383 PCI INTERFACE

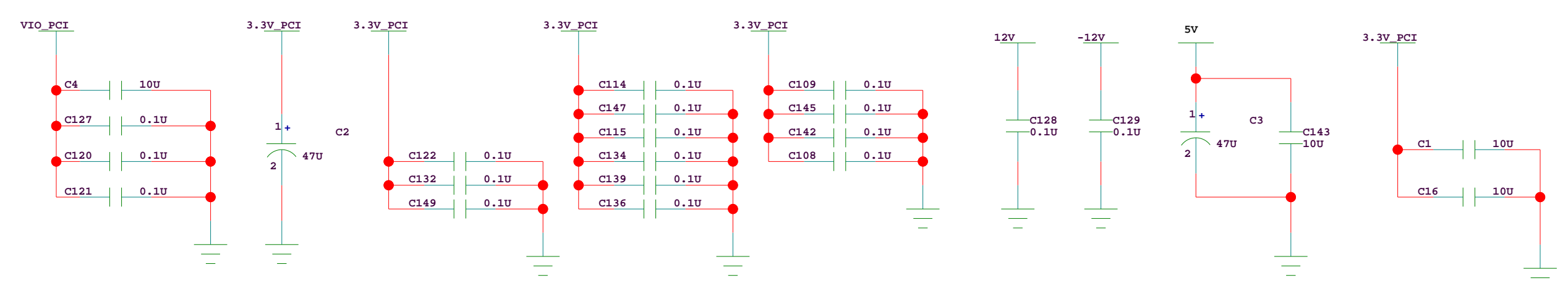


<b>TITLE :</b> TSI383 PCI INTERFACE			
<b>SIZE</b> C	<b>DRAWING NUMBER :</b> TBD	<b>Version:</b> 1.0	<b>DESIGNER :</b>
<b>LAST MODIFIED DATE :</b> 11-27-2009_13:11		<b>SHEET</b> 5 <b>OF</b> 15	

# PCI SLOT 0 (R/A)

IDSEL AD16

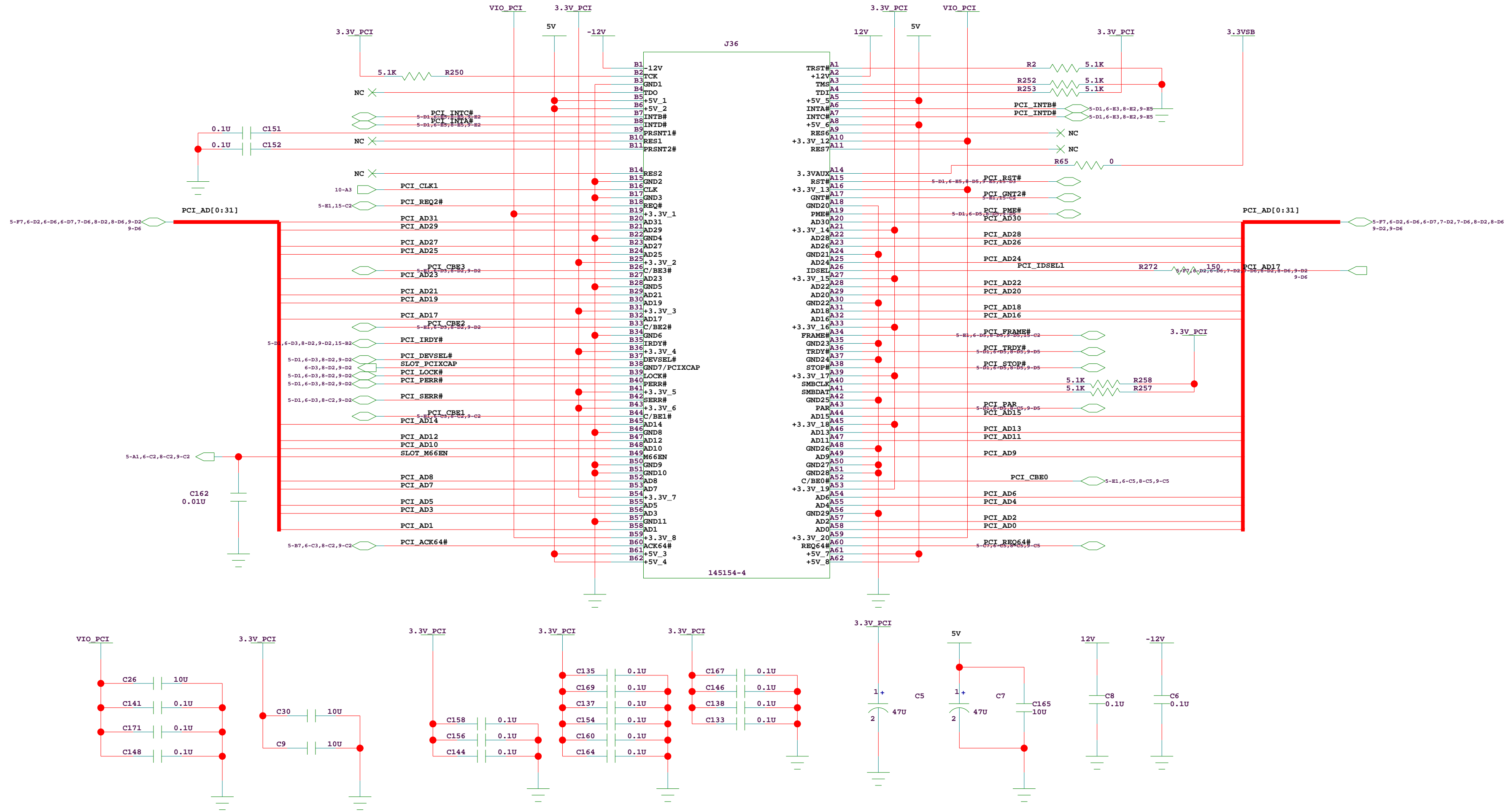
- Required Interrupt Routing
- SLOT : BRIDGE
- INTA -> INTA
- INTB -> INTB
- INTC -> INTC
- INTD -> INTD
- PCI Clock PCI\_CLK0
- PCI Arbitration PCI\_GNT#1/PCI\_REQ#1



TITLE :			
PCI SLOT 0			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
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# PCI SLOT 1 (Vertical)

**IDSEL AD17**  
 - Required Interrupt Routing  
 SLOT : BRIDGE  
 INTA -> INTB  
 INTB -> INTC  
 INTC -> INTD  
 INTD -> INTA  
  
 - PCI Clock PCI\_CLK1  
  
 - PCI Arbitration PCI\_GNT2#/PCI\_REQ#2

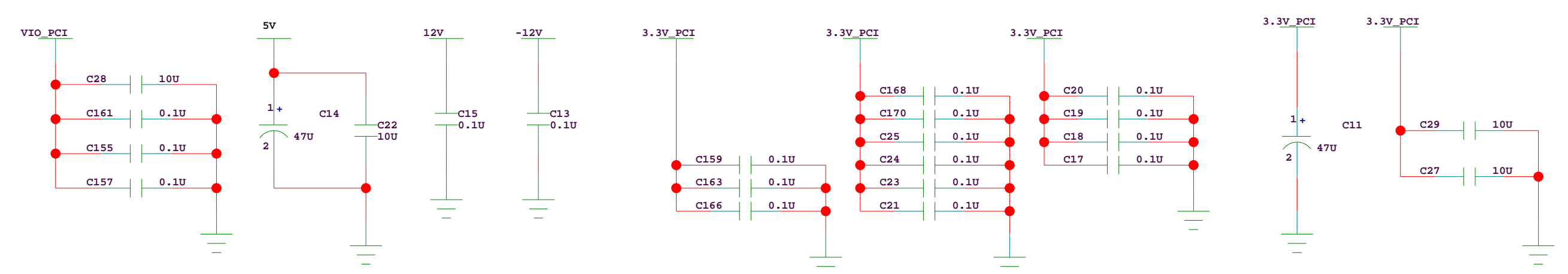
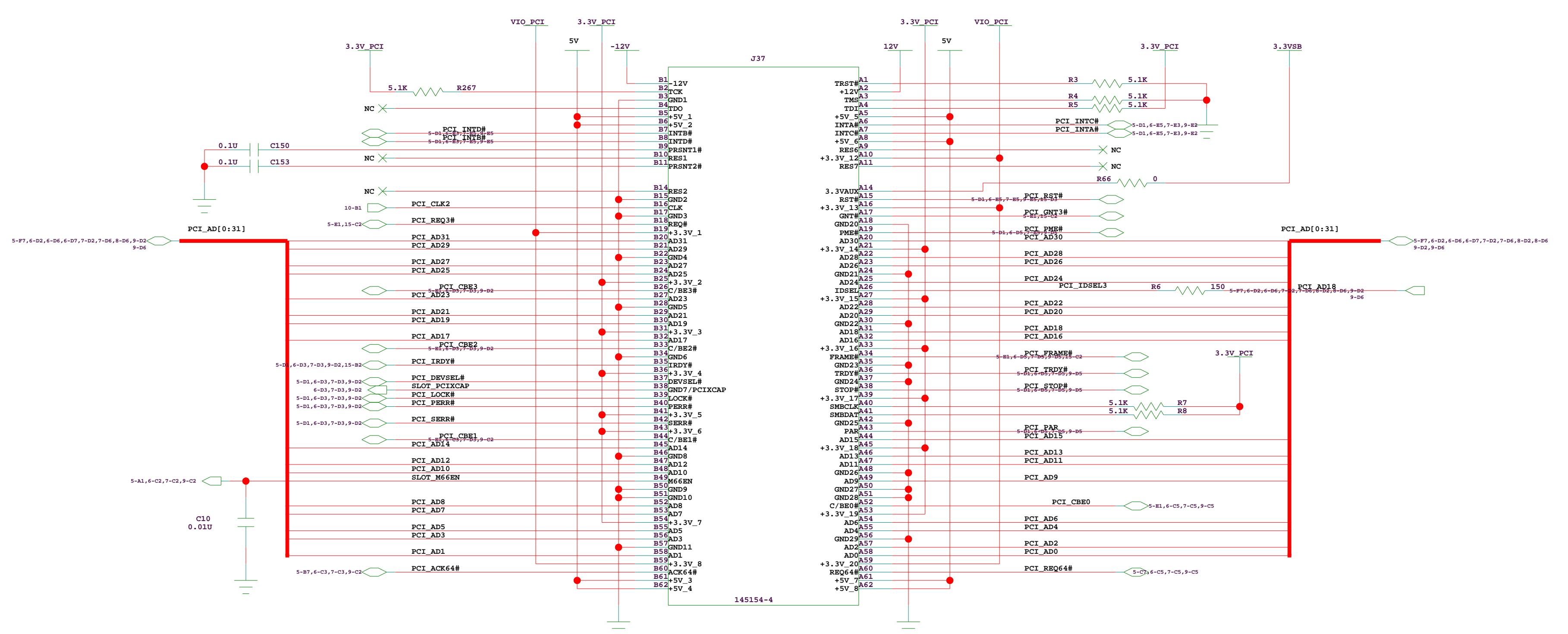


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PCI SLOT 1			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# PCI SLOT 3 (Vertical)

IDSEL AD18

- Required Interrupt Routing
- SLOT : BRIDGE
- INTA -> INTC
- INTB -> INTD
- INTC -> INTA
- INTD -> INTB
- PCI Clock PCI\_CLK2
- PCI Arbitration PCI\_GNT#3/PCI\_REQ#3



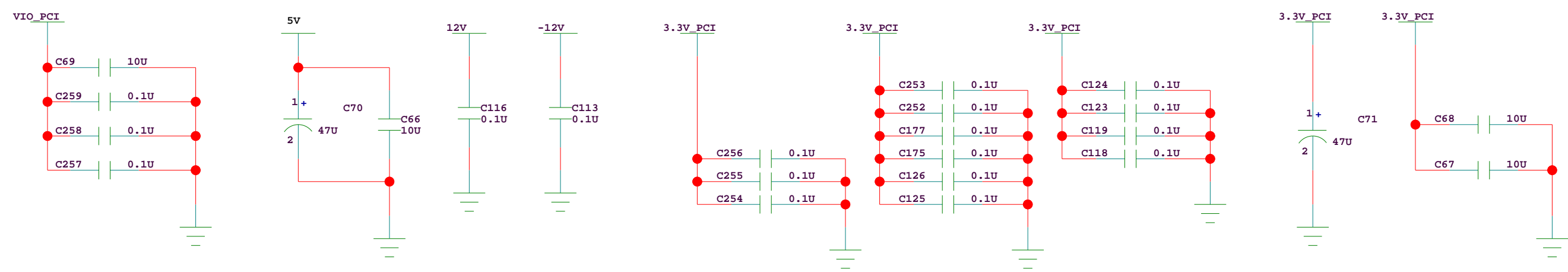
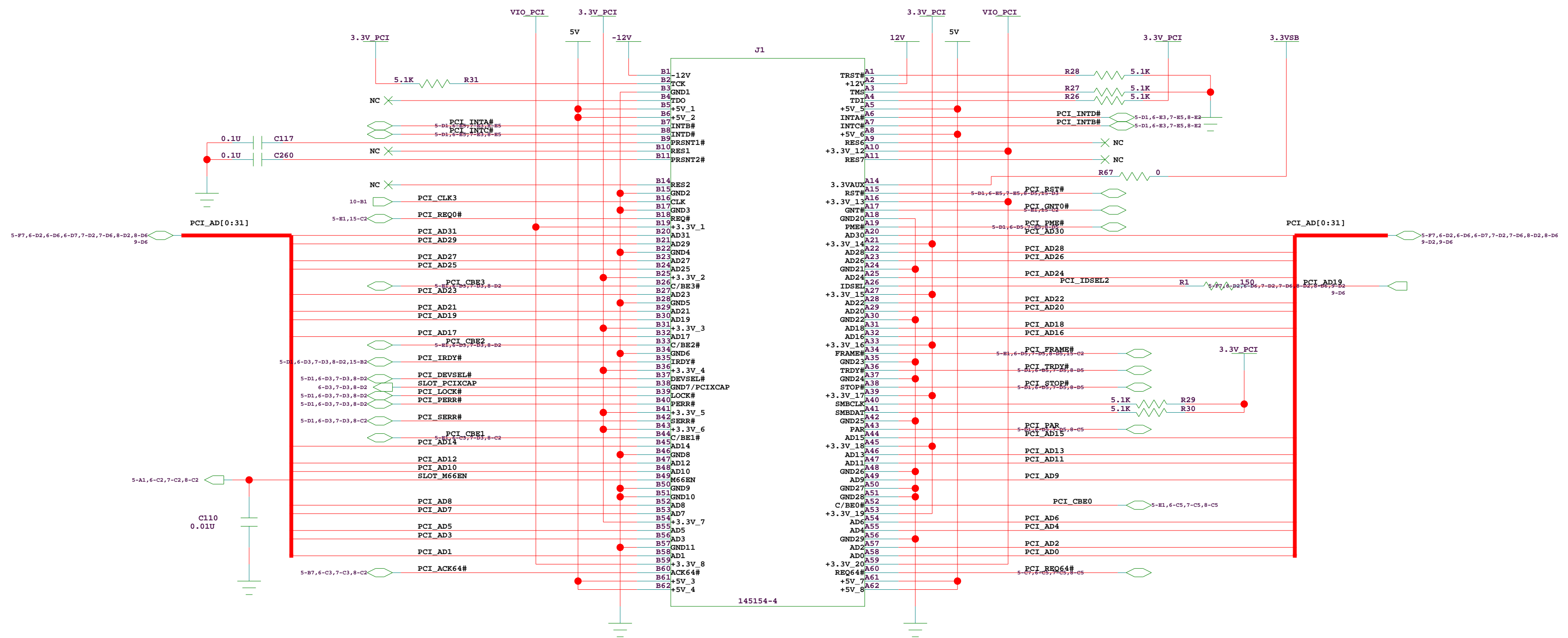
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<b>PCI SLOT 3</b>			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# PCI SLOT 2 (Vertical)

IDSEL AD19

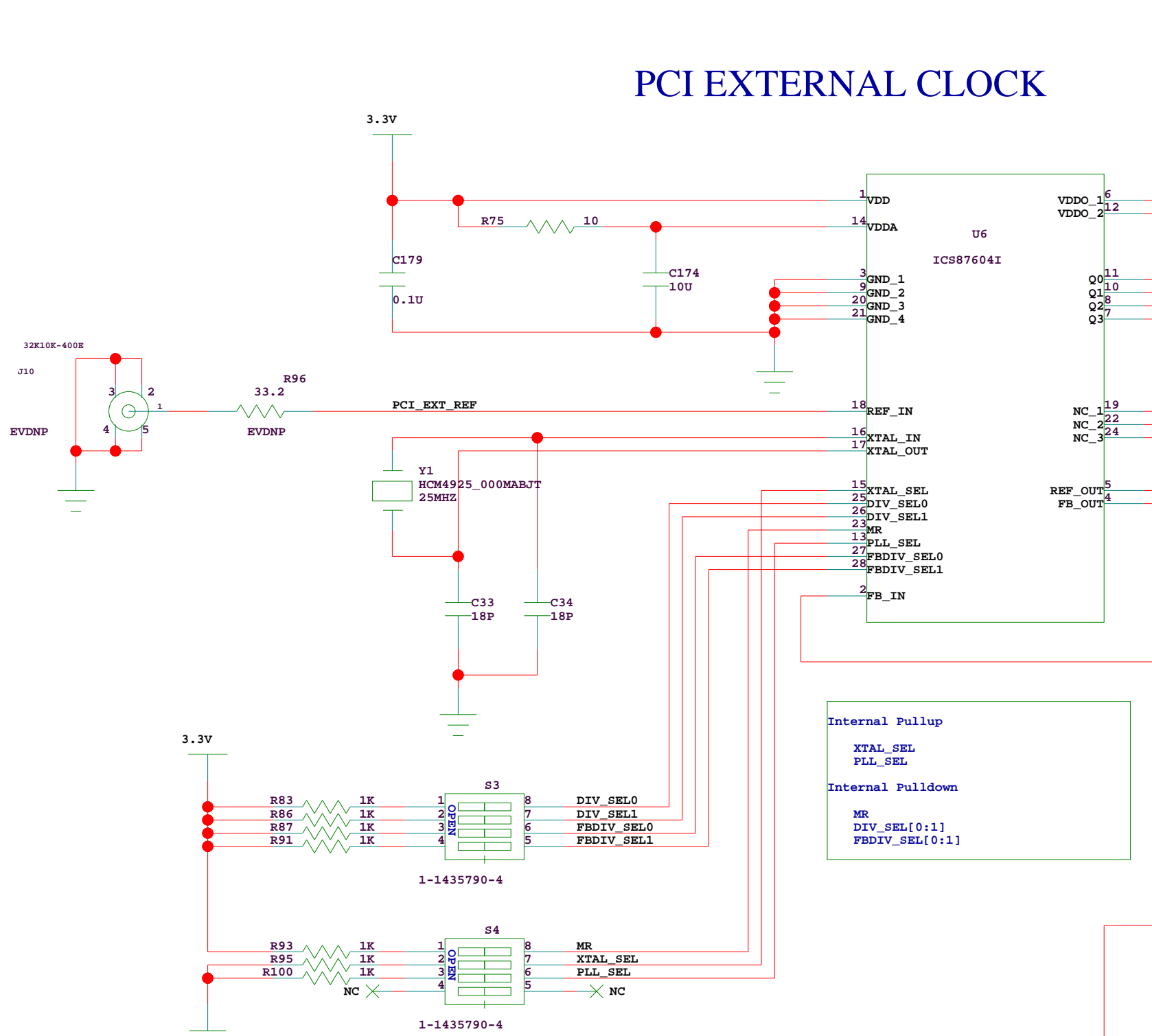
- Required Interrupt Routing
- SLOT : BRIDGE
- INTA -> INTD
- INTB -> INTA
- INTC -> INTB
- INTD -> INTC
- PCI Clock PCI\_CLK3
- PCI Arbitration PCI\_GNT#0/PCI\_REQ#0



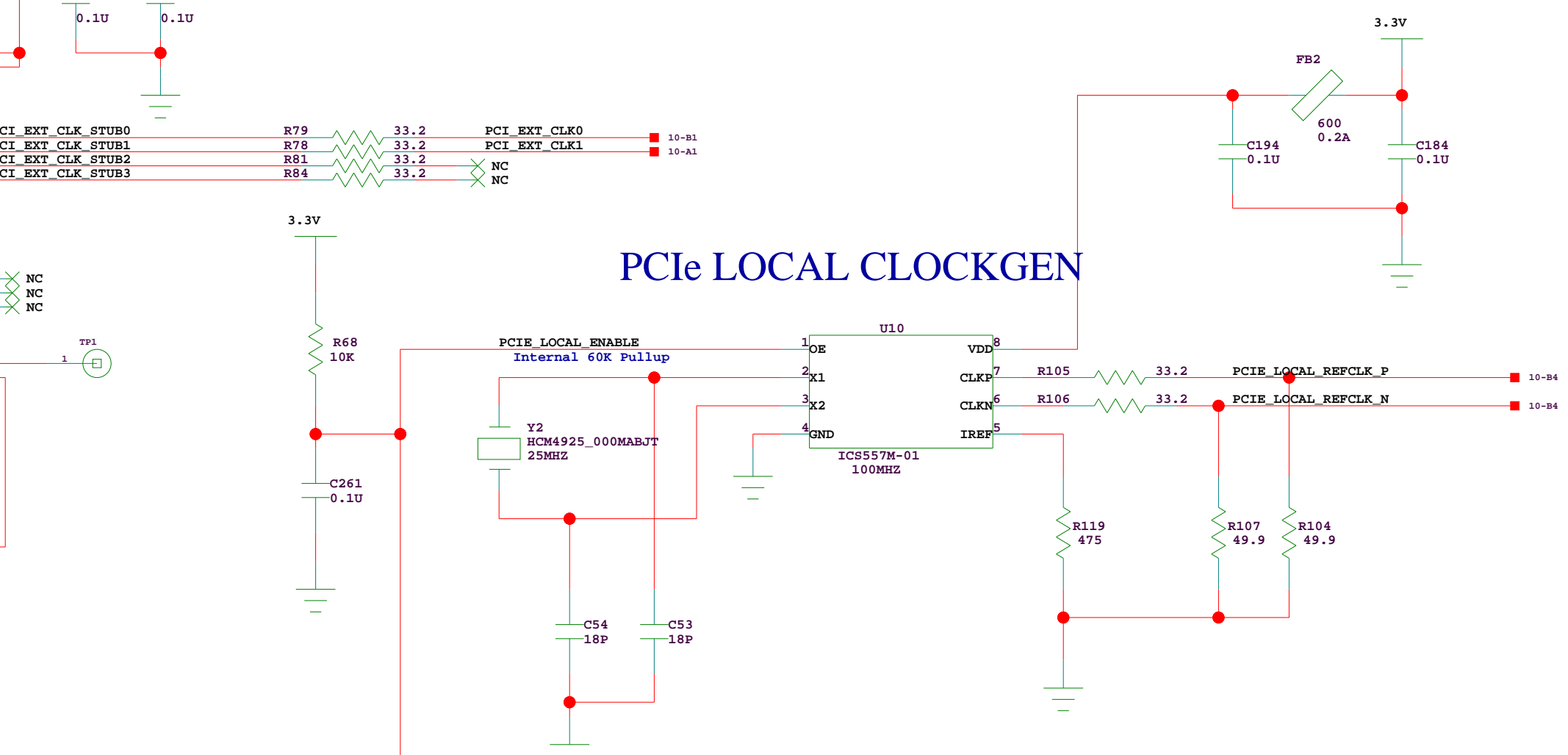
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PCI SLOT 2			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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# CLOCK DISTRIBUTION

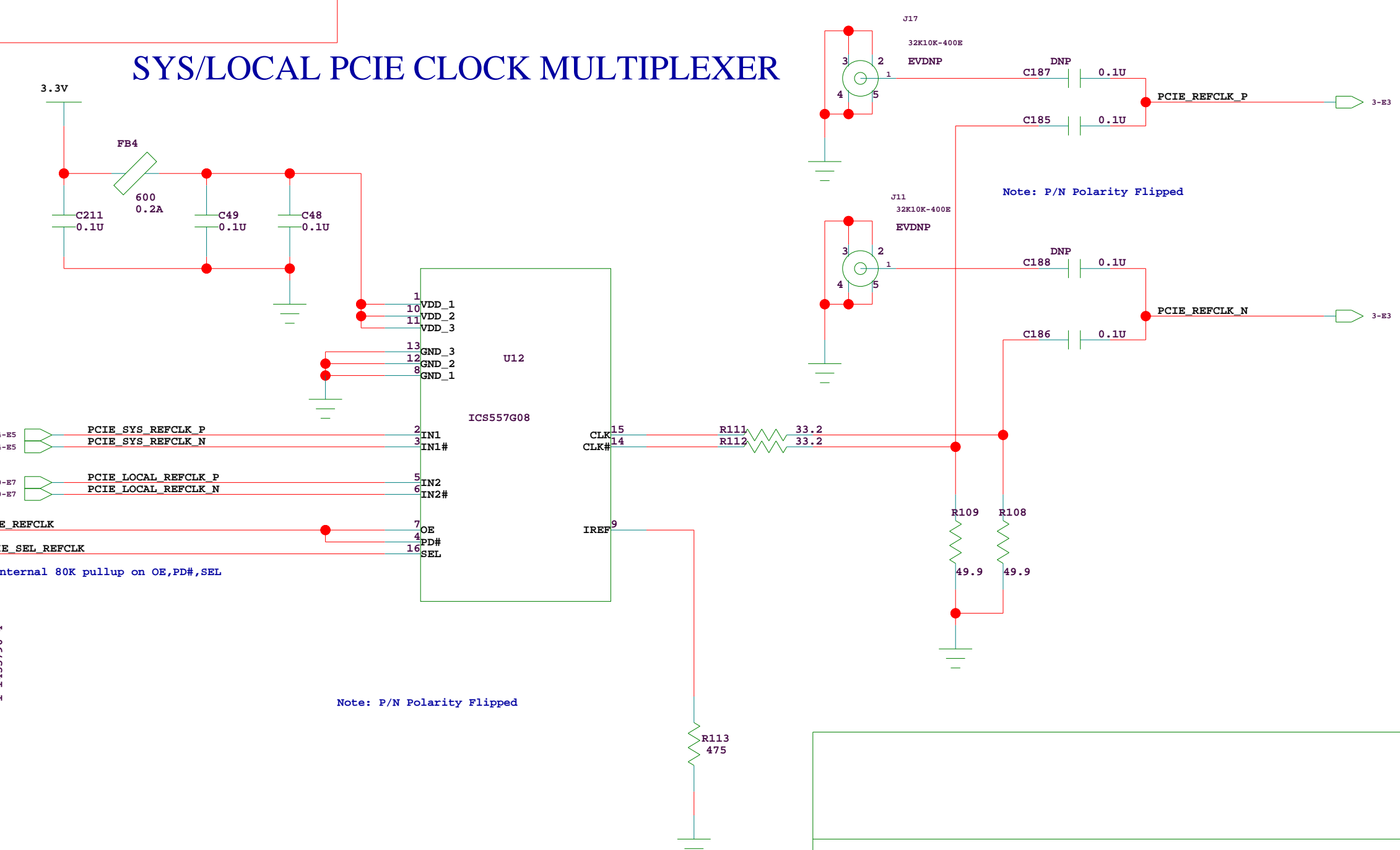
## PCI EXTERNAL CLOCK



## PCIe LOCAL CLOCKGEN

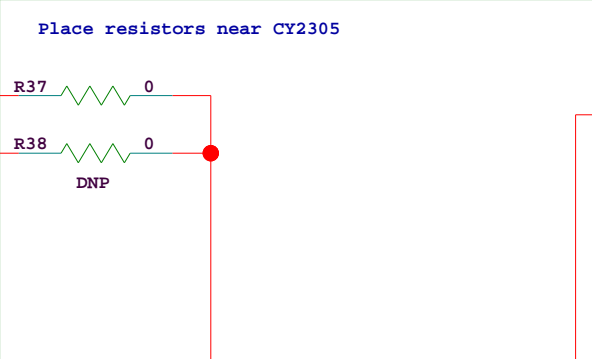


## SYS/LOCAL PCIe CLOCK MULTIPLEXER



Frequency Select (ICS87604I)

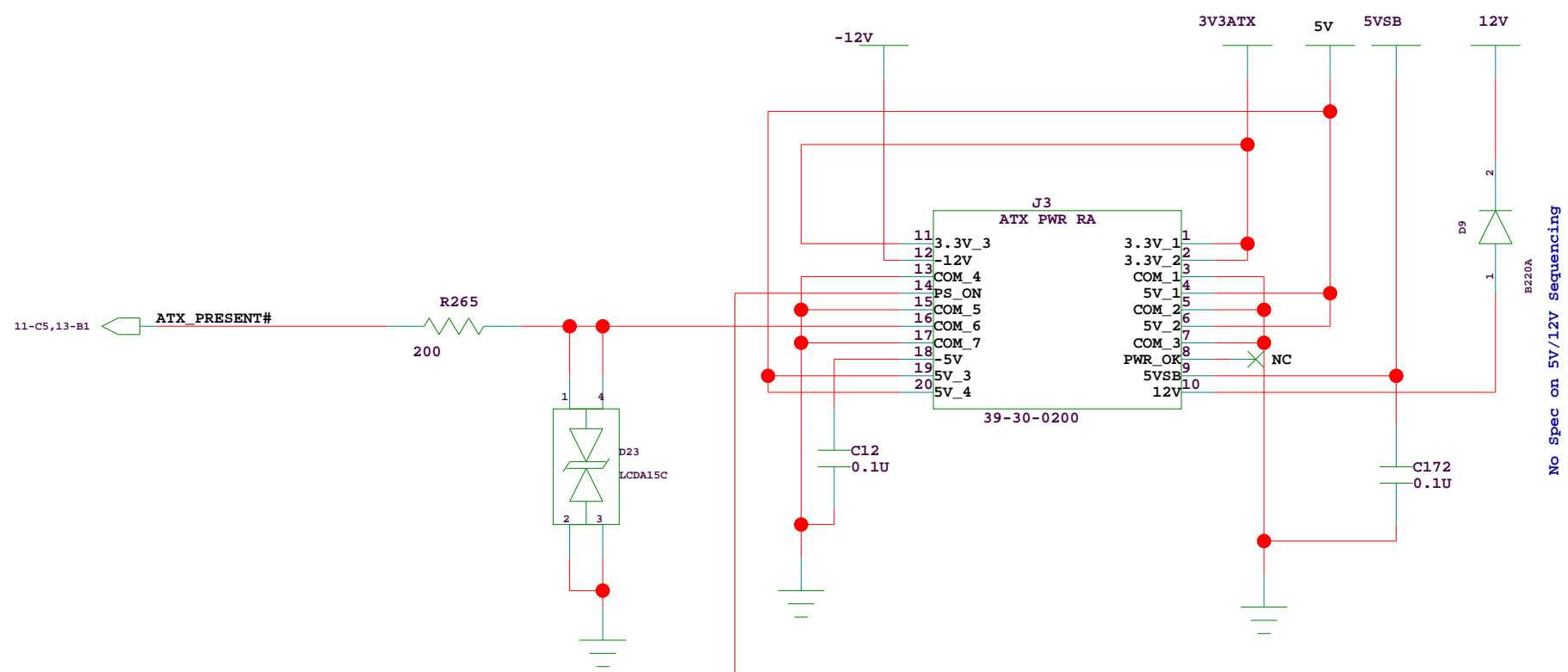
FBDIV_SEL[0:1]	DIV_SEL[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz



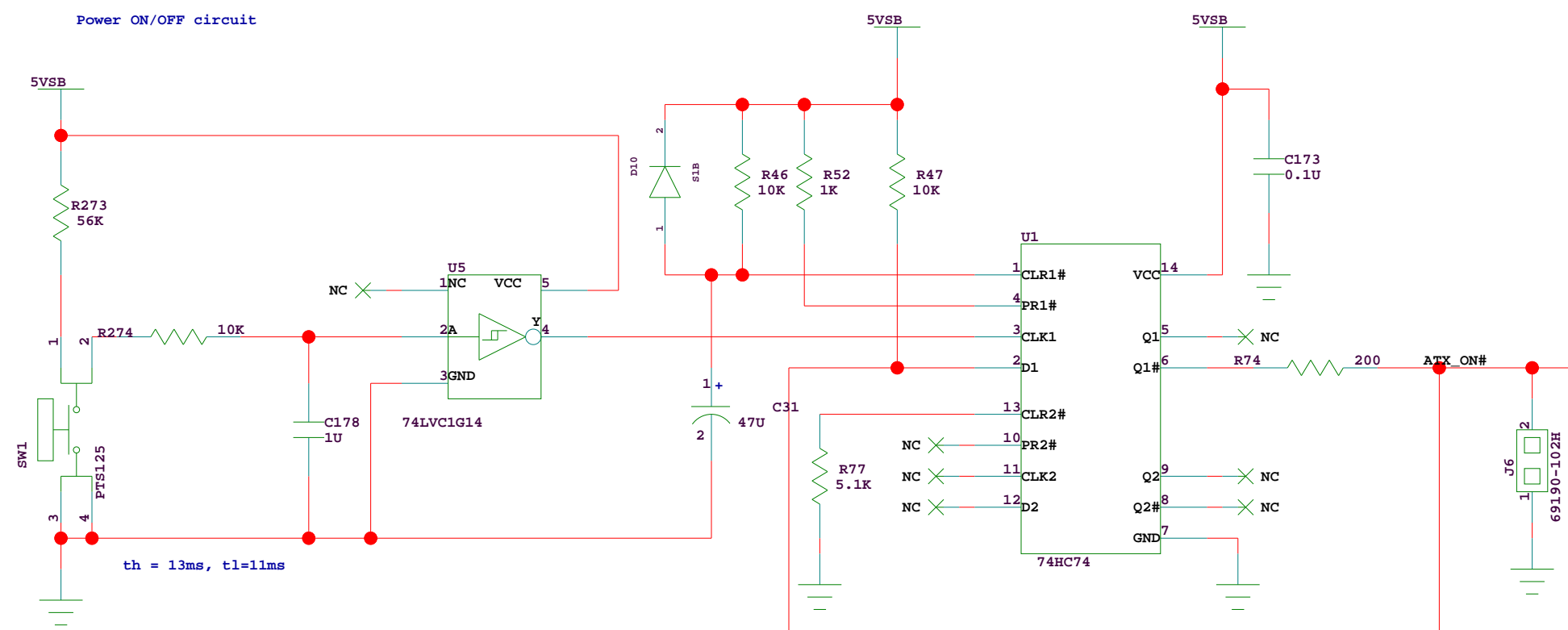
TITLE :			
CLOCK DISTRIBUTION			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C		1.0	
LAST MODIFIED DATE :			SHEET
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# POWER SOURCES

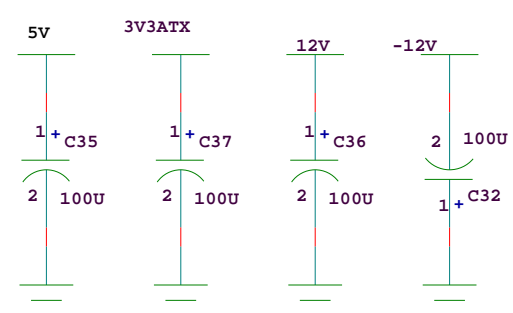
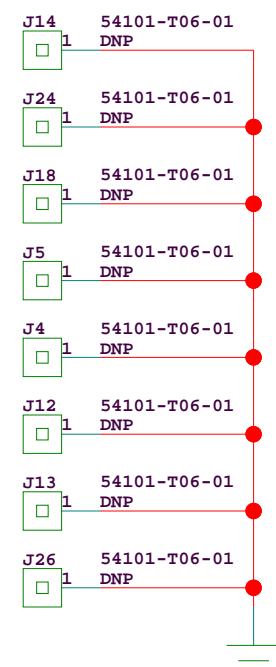
## ATX



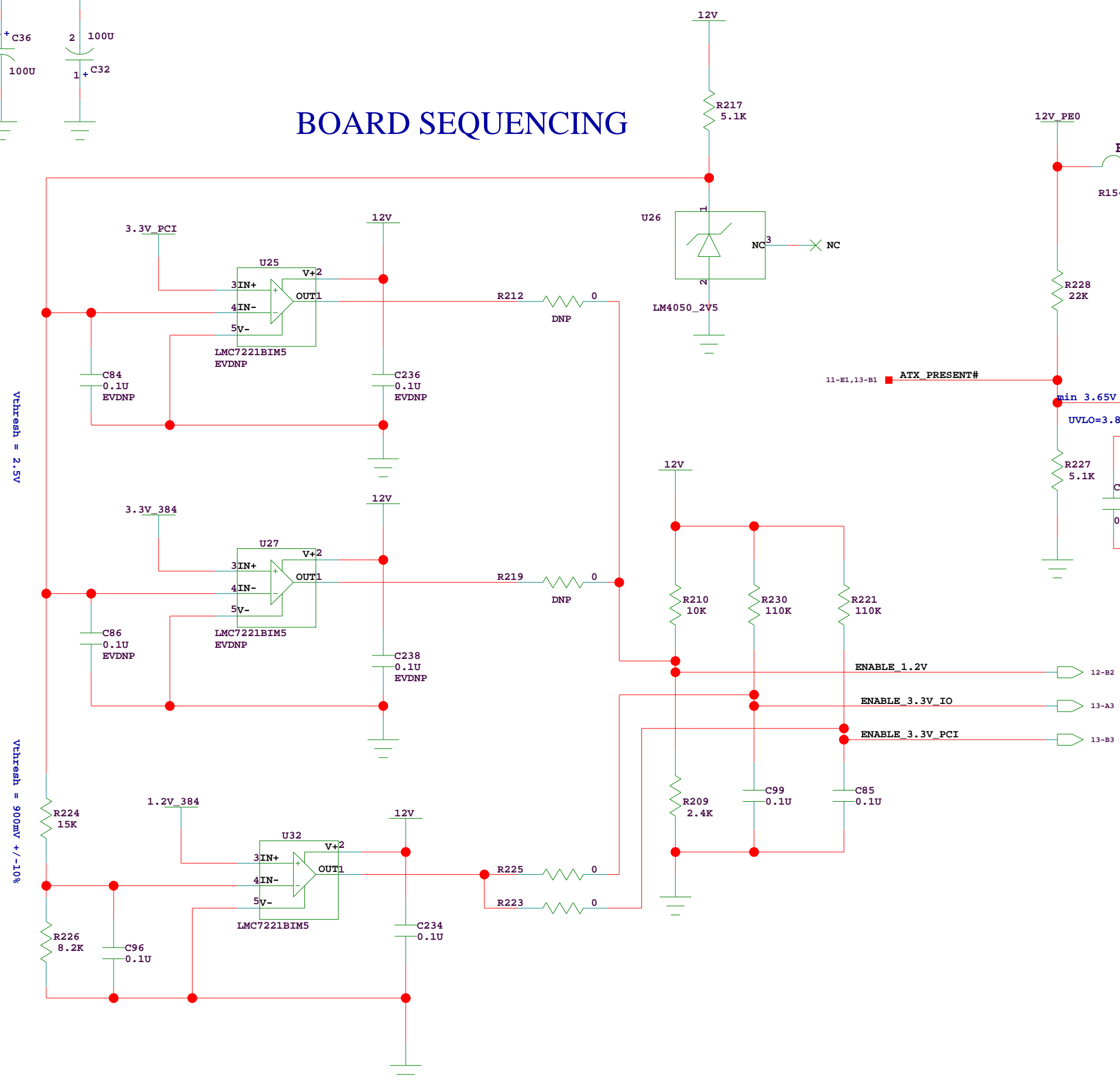
## ATX SUPPLY TOGGLE



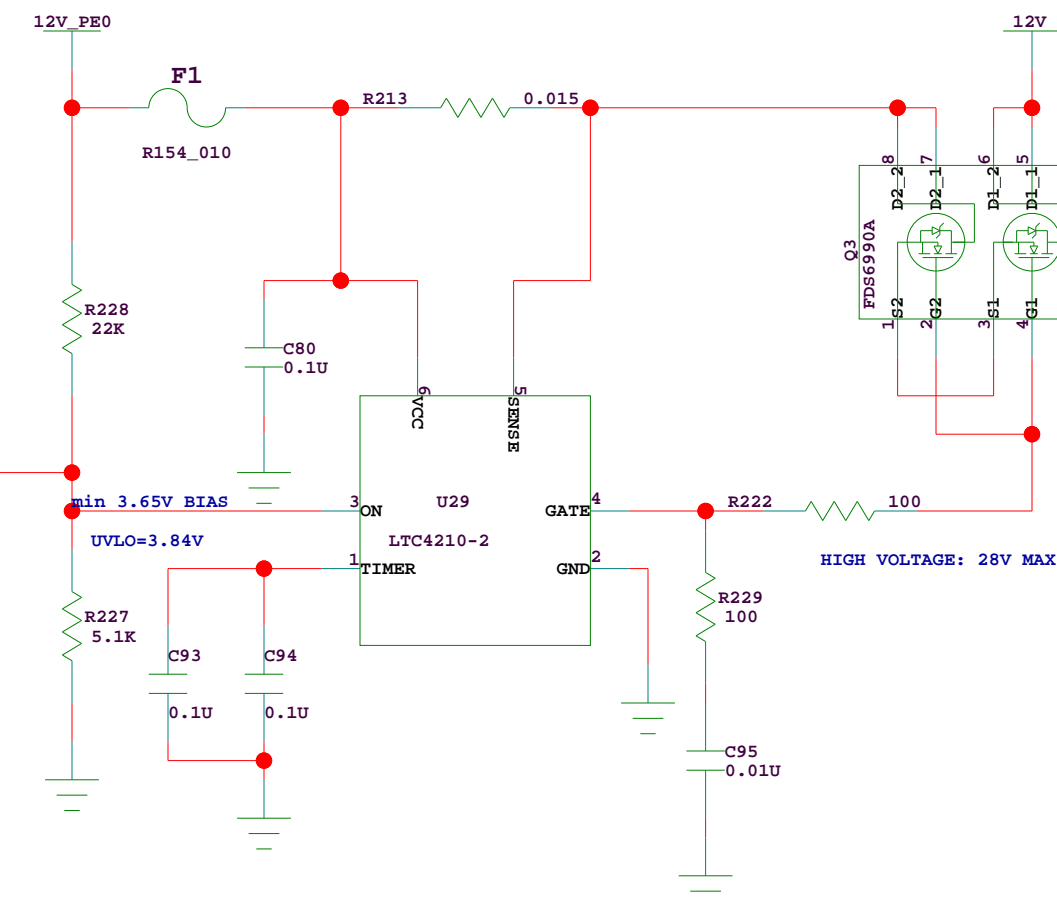
## GND TESTPOINTS



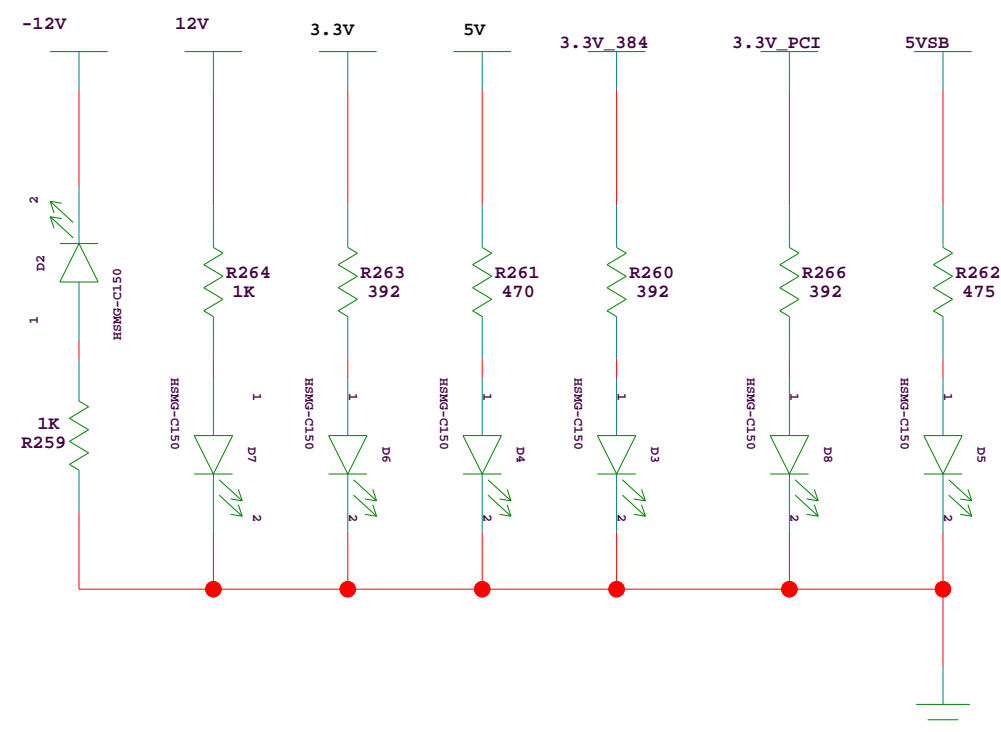
## BOARD SEQUENCING



## SYS SUPPLY SWITCH

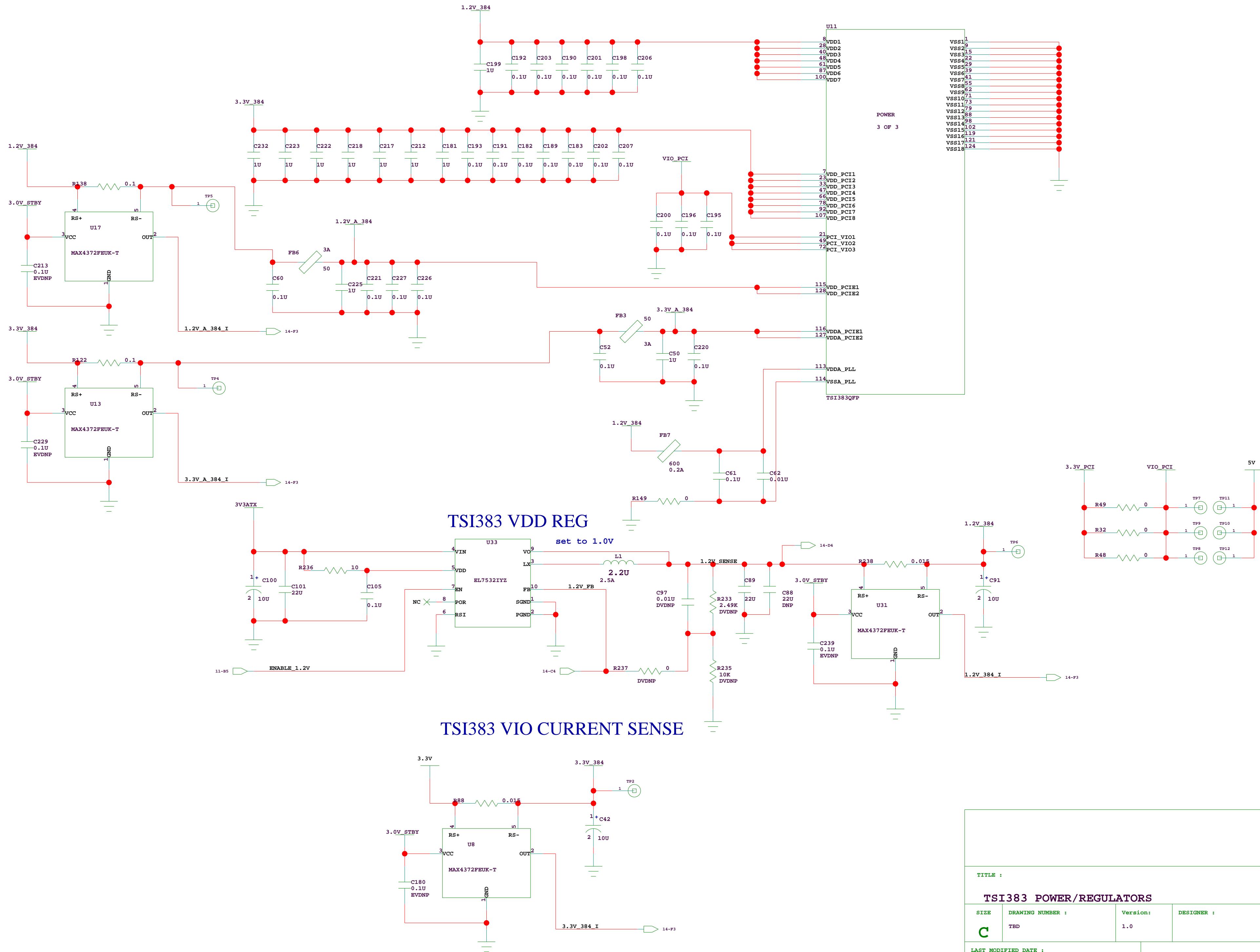


## POWER STATUS



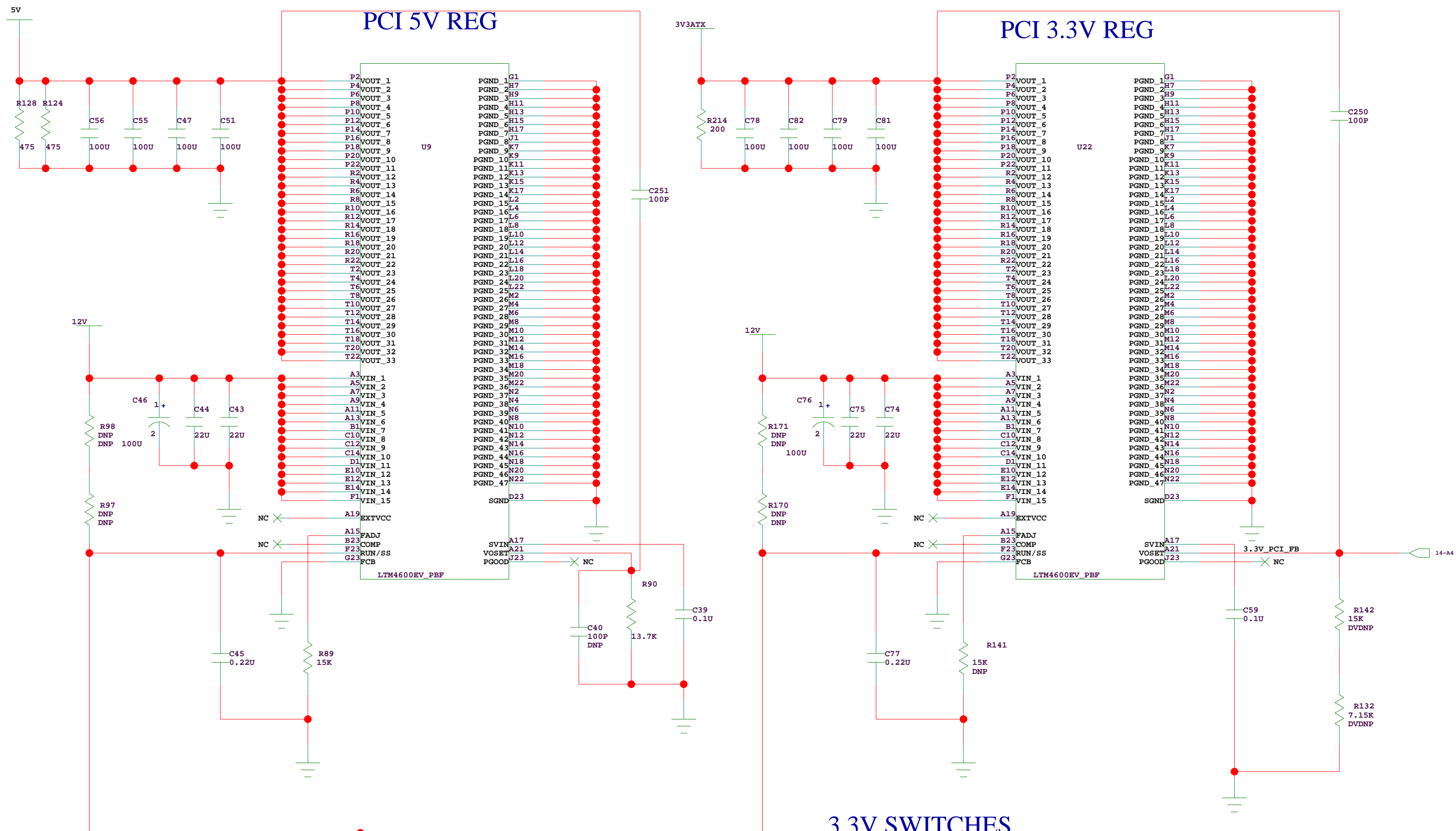
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LAST MODIFIED DATE : <b>11-27-2009_13:11</b>		SHEET <b>11</b> OF <b>15</b>	

# TSI383 POWER/REGULATORS

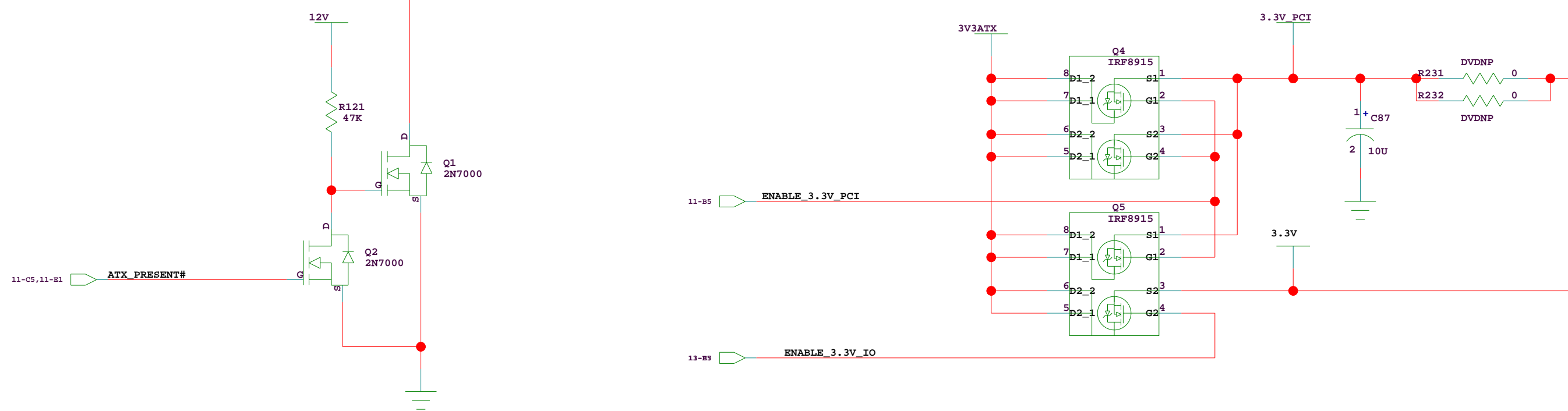


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# PCI POWER REGULATORS



## 3.3V SWITCHES



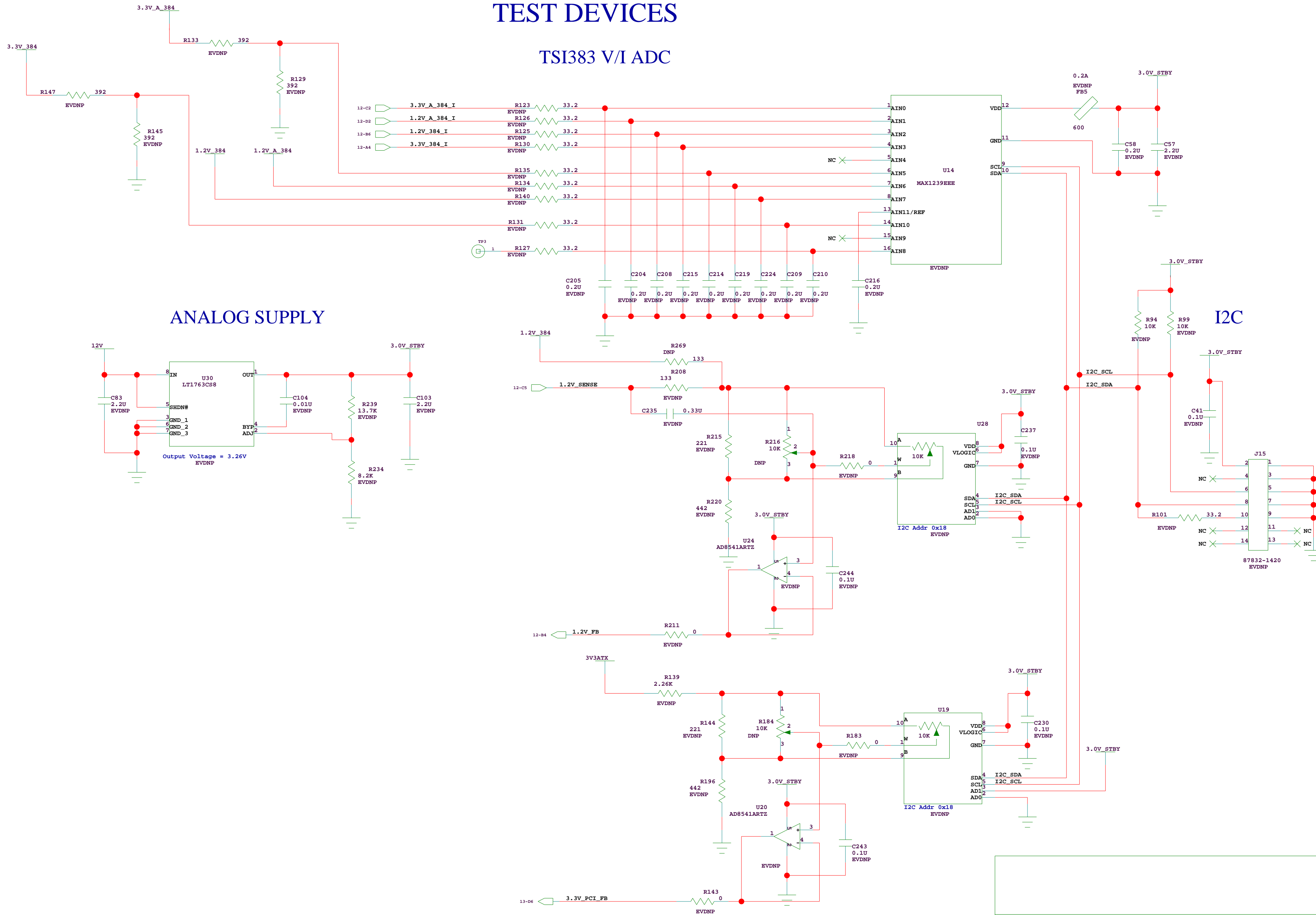
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# TEST DEVICES

## TSI383 V/I ADC

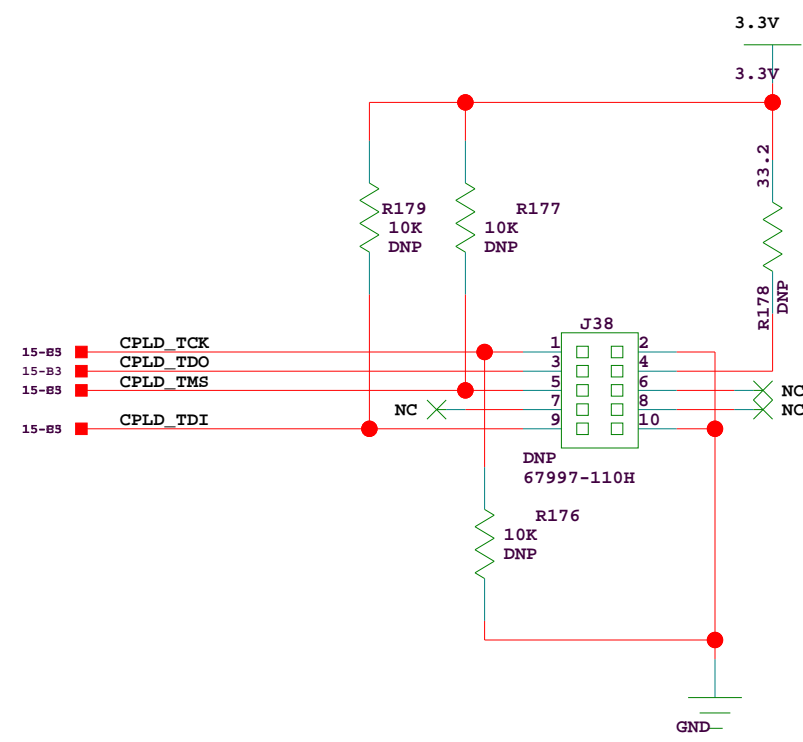
### ANALOG SUPPLY

### I2C

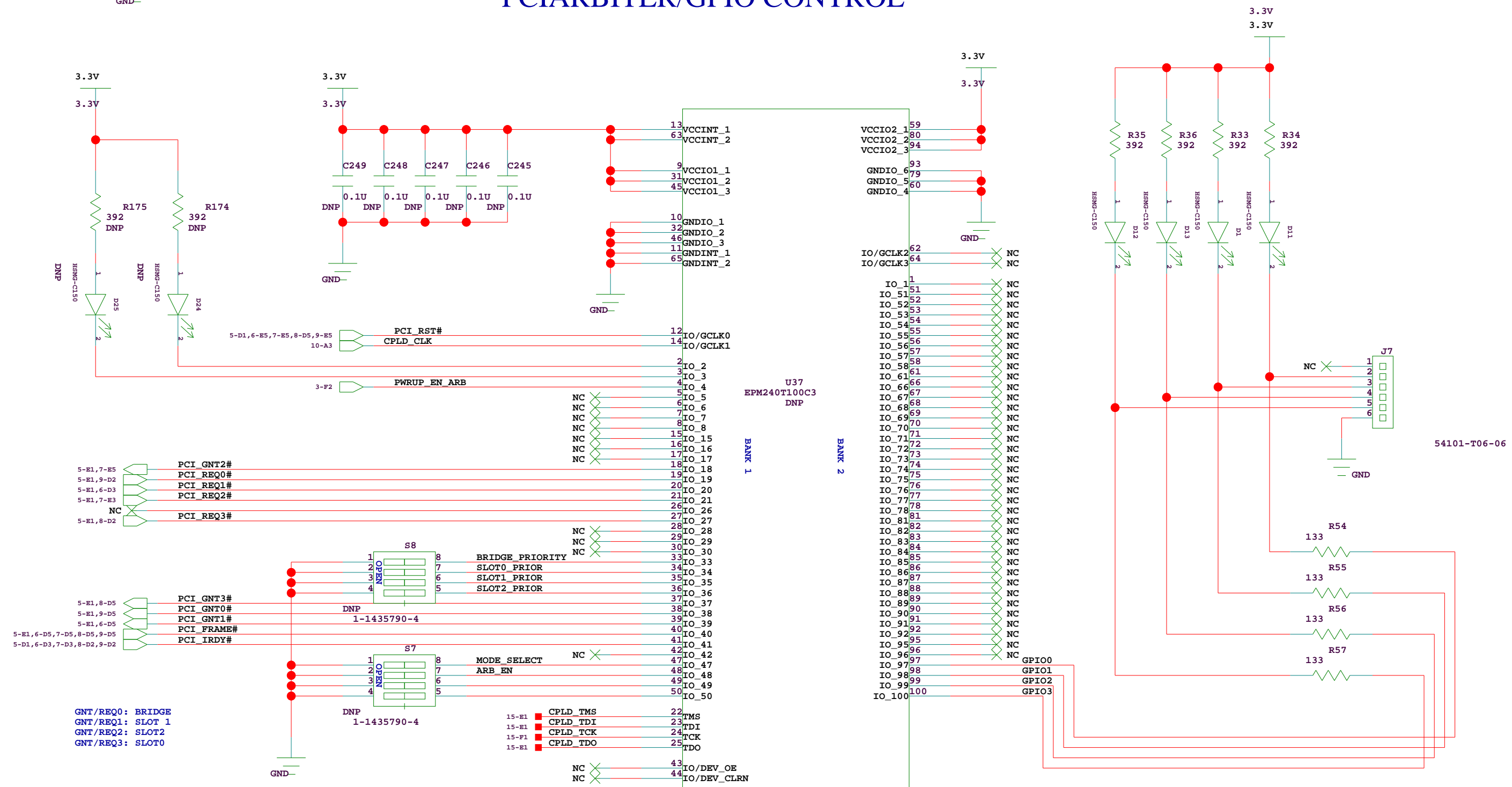


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# TEST DEVICES CONT'D



## PCIARBITER/GPIO CONTROL



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TEST DEVICES CONT'D			
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