PCIe2 to S-RIO2 Bridging and Switching Evaluation Platform User Manual

Formal Status

April 20, 2015

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- Revision History

Revision History

April 20, 2015

Updated the Ordering Information table.

June 12, 2012

Added a new chapter, Recommended Cables.

March 29, 2012

Updated ordering information for the evaluation platform.

July 11, 2011

First release of the *PCIe2 to S-RIO2 Evaluation Platform Manual*.

Overview

This document discusses the architecture, specifications, and functional characteristics of the PCIe2 to S-RIO2 Evaluation Platform. The evaluation platform's main purpose is to help customers evaluate the Tsi721 and CPS-1432 devices, and to allow early development of software. It is also intended to provide a design reference for board designers who are implementing the Tsi721 or CPS-1432 devices in their design.

Ordering Information

Part Number	Components	Description
TSI721-16GEBI	Evaluation Board	• PCIe2 to S-RIO2 Evaluation Platform with Tsi721 and CPS-1432 • *PCIe2 to S-RIO2 Evaluation Platform Quick Start Guide*
	RapidFET JTAG - Standard[a] Debug Tool with a 30-day trial of the "Enhanced" functionality	• RapidFET USB to JTAG/I2C Module • RapidFET JTAG USB Key • USB Cable, 1 m • *RapidFET JTAG Quick Start Installation Guide*

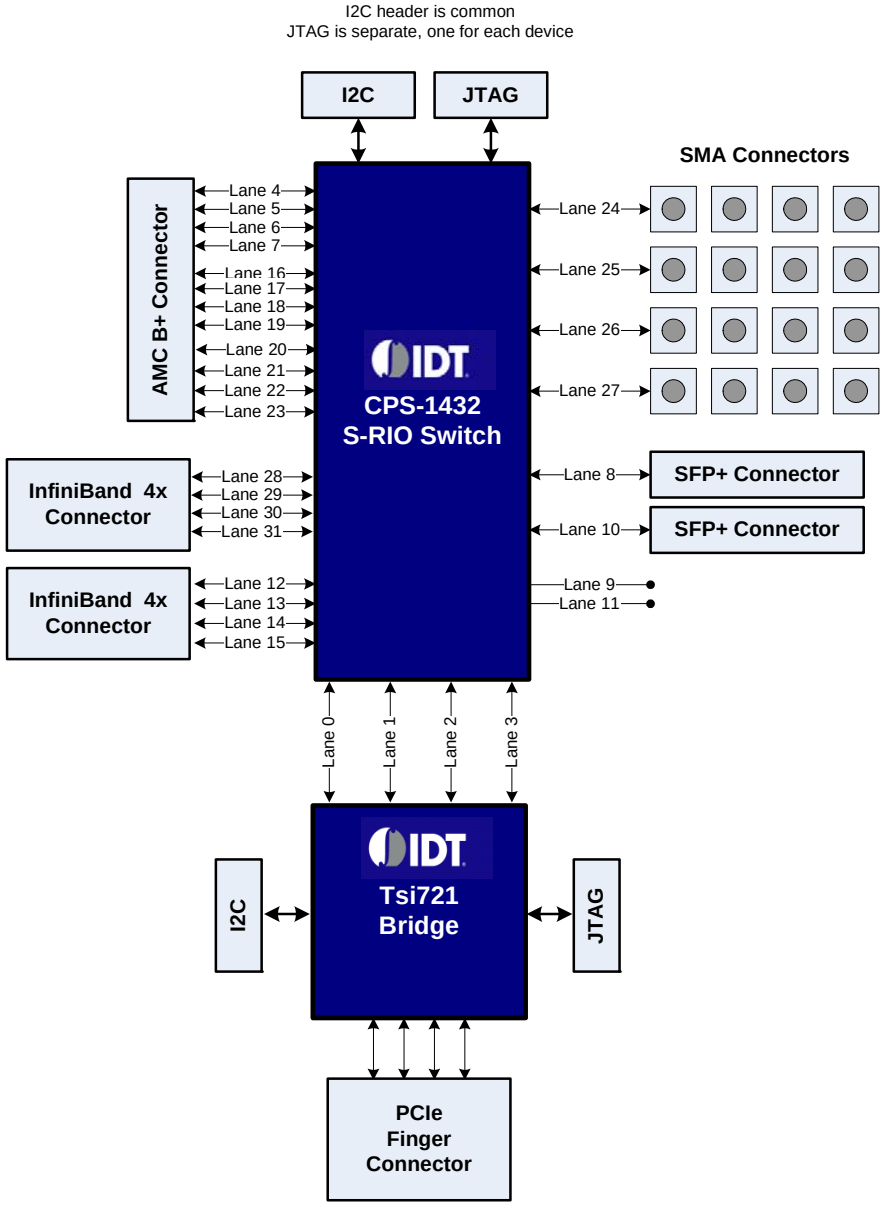
a. For more information about the RapidFET JTAG - Standard and Enhanced debug tools, go to the Fabric Embedded Tools website at www.fetcorp.com.

1. Overview

1.1 Introduction

The PCIe2 to S-RIO2 Evaluation Platform is a flexible platform for testing the Tsi721 PCIe to S-RIO bridge and the CPS-1432 S-RIO Gen2 switch. It can be used as a PCIe plug-in card or as a stand-alone bench top platform powered by an ATX power supply. It is composed of several standard connectors and debug features. Figure 1 shows a block diagram of the PCIe2 to S-RIO2 Evaluation Platform.

Figure 1: PCIe2 to S-RIO2 Evaluation Platform Block Diagram



1.2 Key Features

- PCI Express to S-RIO Bridge
  - PCIe Gen2 endpoint
  - S-RIO Gen2 bridging
- S-RIO Switching Fabric
  - Device: IDT CPS-1432 S-RIO Gen2 switch
  - Link speed: 6.25, 5, 3.125, 2.5, 1.25 Gbaud
  - Protocol: S-RIO Gen1 (v1.3) or S-RIO Gen2 (v2.1)
- Industry-standard system interconnect connectors
  - 1 AMC B+ connectors: 4x S-RIO link, Ports 4–7 and 8–11 and 20-17 (No support on IPMC and JTAG)
  - 2 SFP+ connectors: 1x S-RIO link
  - 2 InfiniBand/CX4 connectors: 4x S-RIO link
  - SMA arrays (4x S-RIO link)
- Flexible clocking options
  - On-board reference clock for S-RIO switch
  - On-board reference clock for PCIe bridge
  - Option for on-board PCIe reference clock or PC-based reference clock
  - Reference clock out: SMA, differential LVDS
  - Reference clock in: SMA, LVTTL, 25 MHz
- JTAG and I2C
  - JTAG header: 0.1" 10-pin header, one for each device
  - I2C header: 0.1” 10-pin header, for both PCIe bridge and S-RIO switch
  - One I2C EEPROM per device
  - USB connector: on-board JTAG/I2C to USB converter (FTDI FT2232HL)
- Power distribution
  - External power supply: ATX power supply with on-board, push-button ON/OFF control
  - Power from Host PC
  - Automatic power source selection. No jumpers required.

1.3 Using the Evaluation Platform in a Host PC

The PCIe2 to S-RIO2 Evaluation Platform is intended to be used in a host PC. It plugs into a x4 PCIe connector (or larger: x8, x16). In this configuration, the PCIe clock source and board power are derived from the host PC. For more information about configuring the platform, see Default Configuration for Host PC.

1.4 Using the Evaluation Platform on a “Bench Top”

The platform can be used outside of a host PC. In this configuration, board power comes from the 20-pin ATX supply. If the PCIe interface is not used, the PCIe reference clock must be sourced from the on-board oscillator. Use S9.4 to select on-board clocking.

If PCIe reset (PERST) is not connected to the platform, the reset pull-up jumper (J27) should be inserted in order to prevent the reset signal from floating. For more information about configuring the platform for bench top operation, see Stand-Alone Configuration.

1.5 Power Supply Options

When the platform is plugged in a PC, power comes from the PCIe connector (see Figure 2). If the host PC is unable to supply enough power to the platform, there are two options available:

- Plug in a spare hard-drive ATX power connector in J1 (see Figure 3)
- Plug in a separate ATX power connector in J25 (see Figure 4)

When an external supply is connected, either in J1 or J25, the PC's 12V rail is cut off from the platform such that there is no contention between the PC supply and the external supplies.

Figure 2: Board Power for PC Motherboard

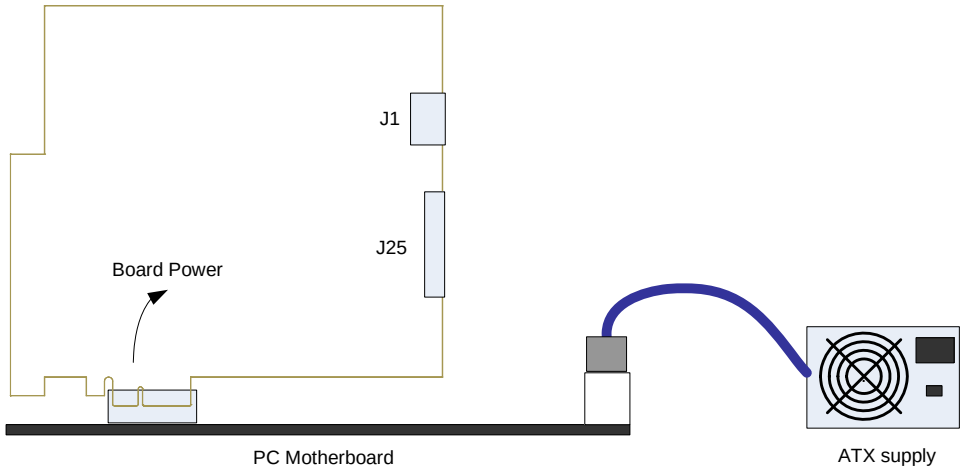


Figure 3: Board Power for 4-Pin ATX Connector

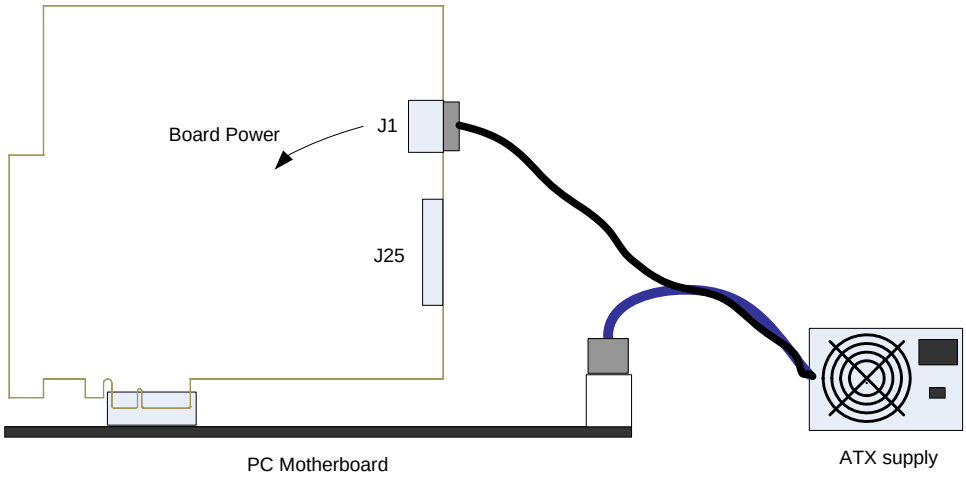
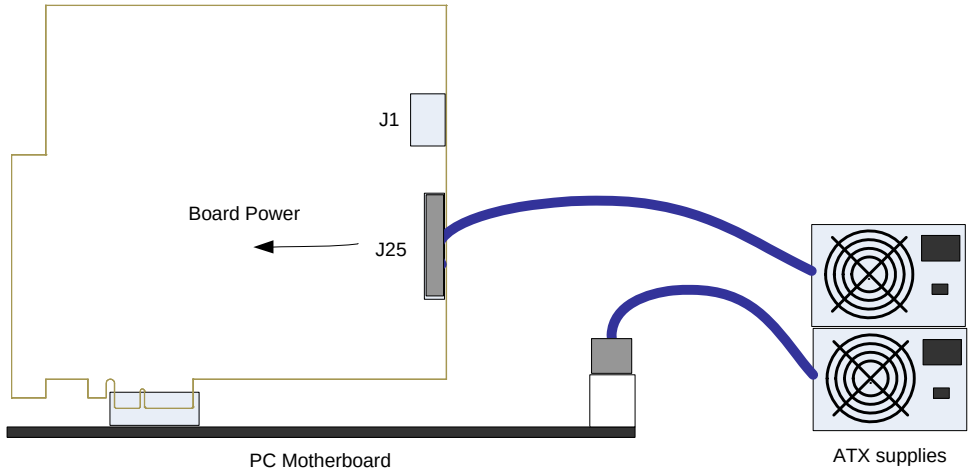


Figure 4: Board Power from Separate ATX Power Supply

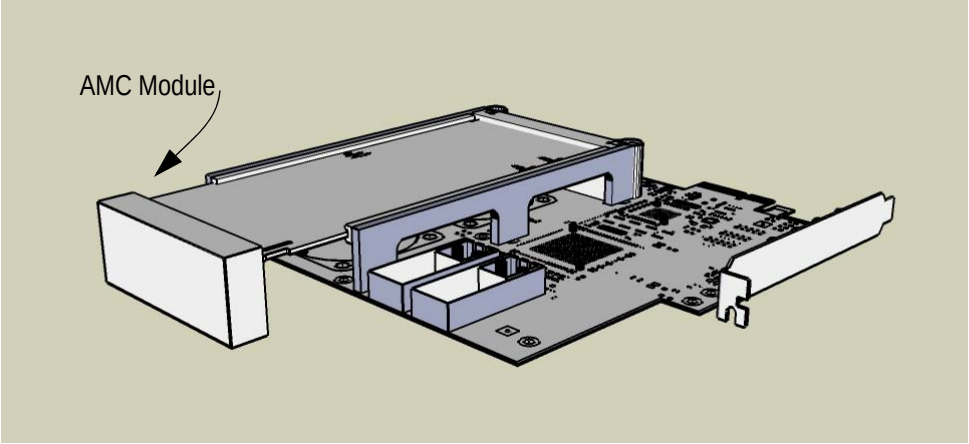


When outside a PC, the 20-pin ATX supply or the 4-pin ATX supply (or both) must be used. When the 20-pin ATX supply connector is used, the ATX power supply module can be powered on/off with the on-board push button. If only the 4-pin ATX connector is used, the ON/OFF push button is not activated. The ATX power supply module must be powered up by different methods.

1.6 Inserting AMC Modules

AMC modules *must be* inserted top side-down as shown in Figure 5. Connecting the module top side-up might damage the module. Note that only mid-size modules can be used.

Figure 5: AMC Module Insertion Orientation



2. Design Description

This chapter describes the design characteristics of the PCIe2 to S-RIO2 Evaluation Platform. It discusses how the platform's components are connected together and how they interact.

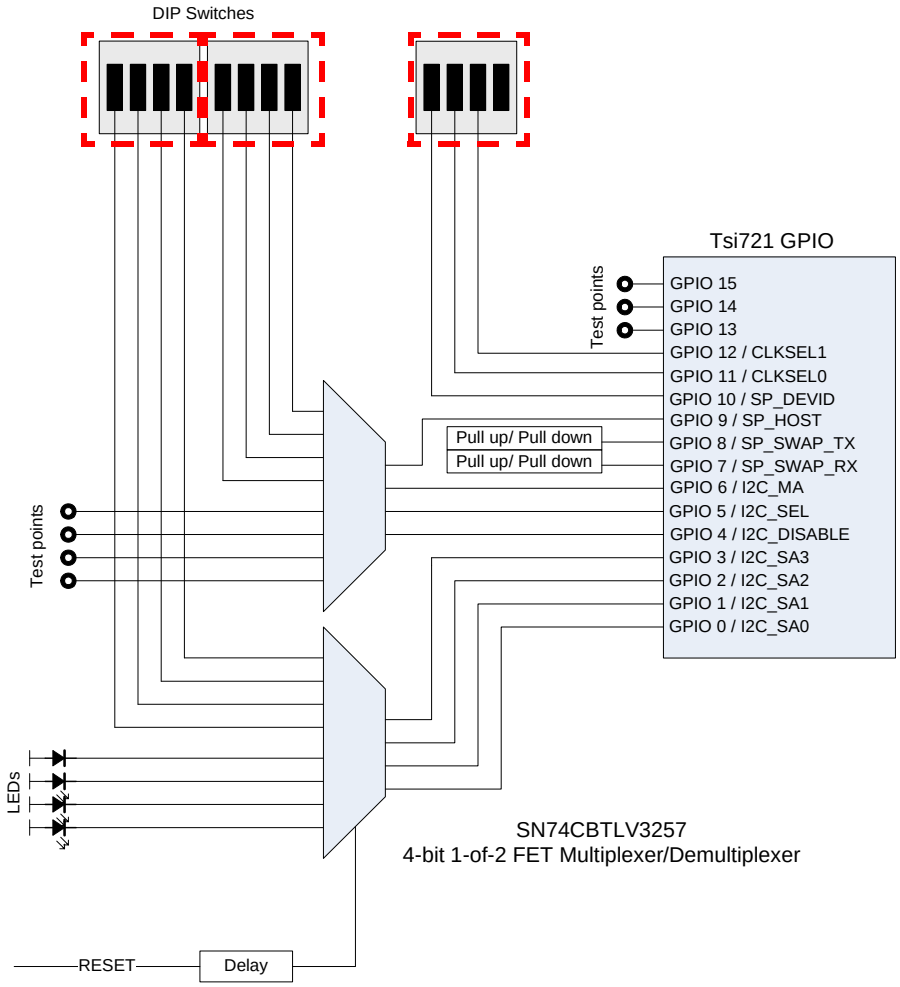
2.1 Tsi721 Power-Up Options

2.1.1 GPIOs

All of the Tsi721's power-up pins are multiplexed with GPIOs. During normal operation GPIO[2:0] provide device status. In order to properly set the power-up options and use GPIOs, FET multiplexers/demultiplexers are used. GPIO[12:0] levels are set with DIP switches with the exception of GPIO[8:7] (SP_SWAP_TX and SP_SWAP_TX) which are set with pull-up/pull-down resistors. After RESET is de-asserted, the FET MUX/DEMUX connects GPIO[3:0] to LEDs and GPIO[7:4] to test points.

The reset delay is made by an analog delay timer. The delay is longer than 4000 REFLCK cycles (256 us).

Figure 6: Tsi721 Power-Up Options[1]



2.1.2 CLKMOD

CLKMOD is set with a switch on the platform.

2.1.3 SR_BOOT

SR_BOOT is set with a switch on the platform.

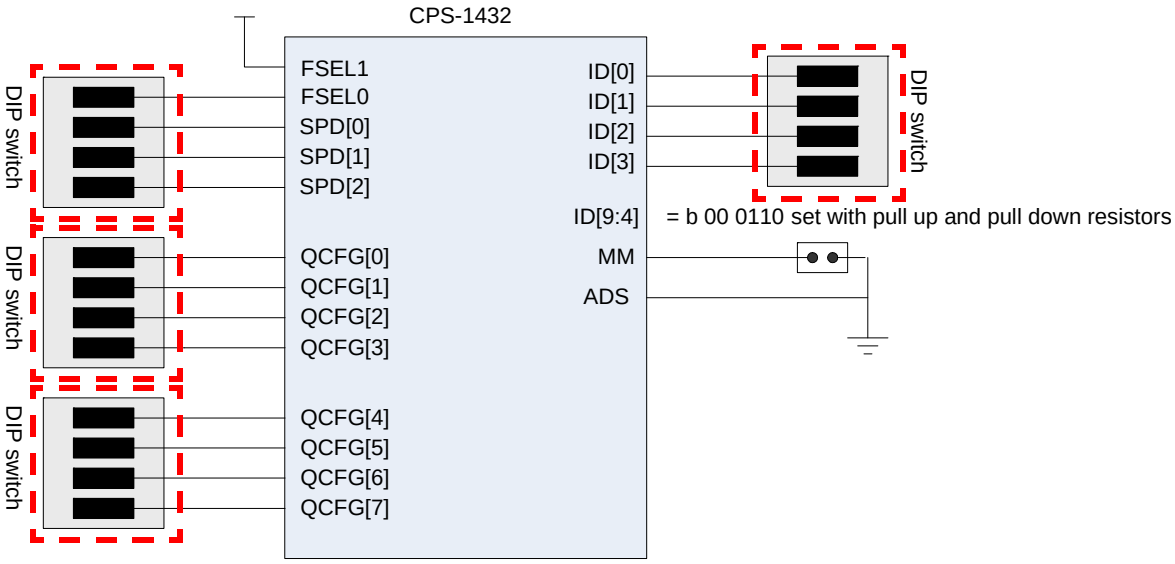
2.1.4 STRAP_RATE[2:0]

STRAP_RATE[2:0] are set with a switch on the platform. Unfortunately the bit code setting for the CPS-1432 and Tsi721 are different; therefore, two DIP switches are used.

2.2 CPS-1432 Power-Up Options

The following figure summarizes the CPS-1432's power-up options.

Figure 7: CPS-1432 Power-Up Options[1]



2.2.1 FSEL[1:0]

2.2.1.1 FSEL[0]

FSEL[0] selects the core frequency of the switch. It is connected to a DIP switch (see Table 11 and 12).

2.2.1.2 FSEL[1]

FSEL[1] is set to 1 with a resistor option to ground. FSEL[1] = 1 is the setting for a 156.25-MHz reference clock input (see Table 11 and 12).

1. The dashed boxes around the DIP switches indicate PDF links to switch setting definitions.

2.2.2 SPD[2:0]

SPD[2:0] are set with DIP switches as follows (see Table 11):

- 000 = 1.25 Gbaud
- 001 = 2.5 Gbaud
- 010 = 3.125 Gbaud
- 011 = 5.0 Gbaud
- 100 = 6.25 Gbaud
- All others = Reserved

2.2.3 MM

MM (active low) is connected to a suitcase jumper. When the jumper is installed, the switch is an I2C master on power up.

2.2.4 ADS, ID[9:0]

ADS is set to GND (7-bit I2C addressing) with a resistor option to VDD3.

ID[9:0] is set to b00 0110 xxxx with resistor options to set any bits to VDD3 or ground. The 4 LSBs are set with switches.

2.2.5 QCFG[7:0]

QCFG is set with DIP switches. Table 1 indicates the port width based on the QCFG setting.

2.2.6 MCAST

The MCAST input is tied to a header. The header can be used to connect to an external pulse generator.

2.3 CPS-1432 Port Assignments

The switch lanes to connector assignment is detailed in Table 1. The CPS-1432 and Tsi721 are connected together using four lanes.

Table 1: Lane Assignment (CPS-1432)

CPS-1432 Lane	Connection	Assignment
0	Tsi721	Lane 0
1		Lane 1
2		Lane 2
3		Lane 3
4	AMC	AMC Port 20
5		AMC Port 19
6		AMC Port 18
7		AMC Port 17

Table 1: Lane Assignment (CPS-1432) ***(Continued)***

CPS-1432 Lane	Connection	Assignment
8	SFP+	J44
9		Not connected
10		J45
11		Not connected
12	Infiniband CX4 (J4)	Lane 0
13		Lane 1
14		Lane 2
15		Lane 3
16	AMC	AMC Port 8
17		AMC Port 9
18		AMC Port 10
19		AMC Port 11
20	AMC	AMC Port 4
21		AMC Port 5
22		AMC Port 6
23		AMC Port 7
24	SMA	J19/J20 and J11/J12
25		J17/J18 and J9/J10
26		J15/J16 and J7/J8
27		J5/J6 and J13/J14
28	Infiniband CX4 (J3)	Lane 0
29		Lane 1
30		Lane 2
31		Lane 3

2.4 Clocking

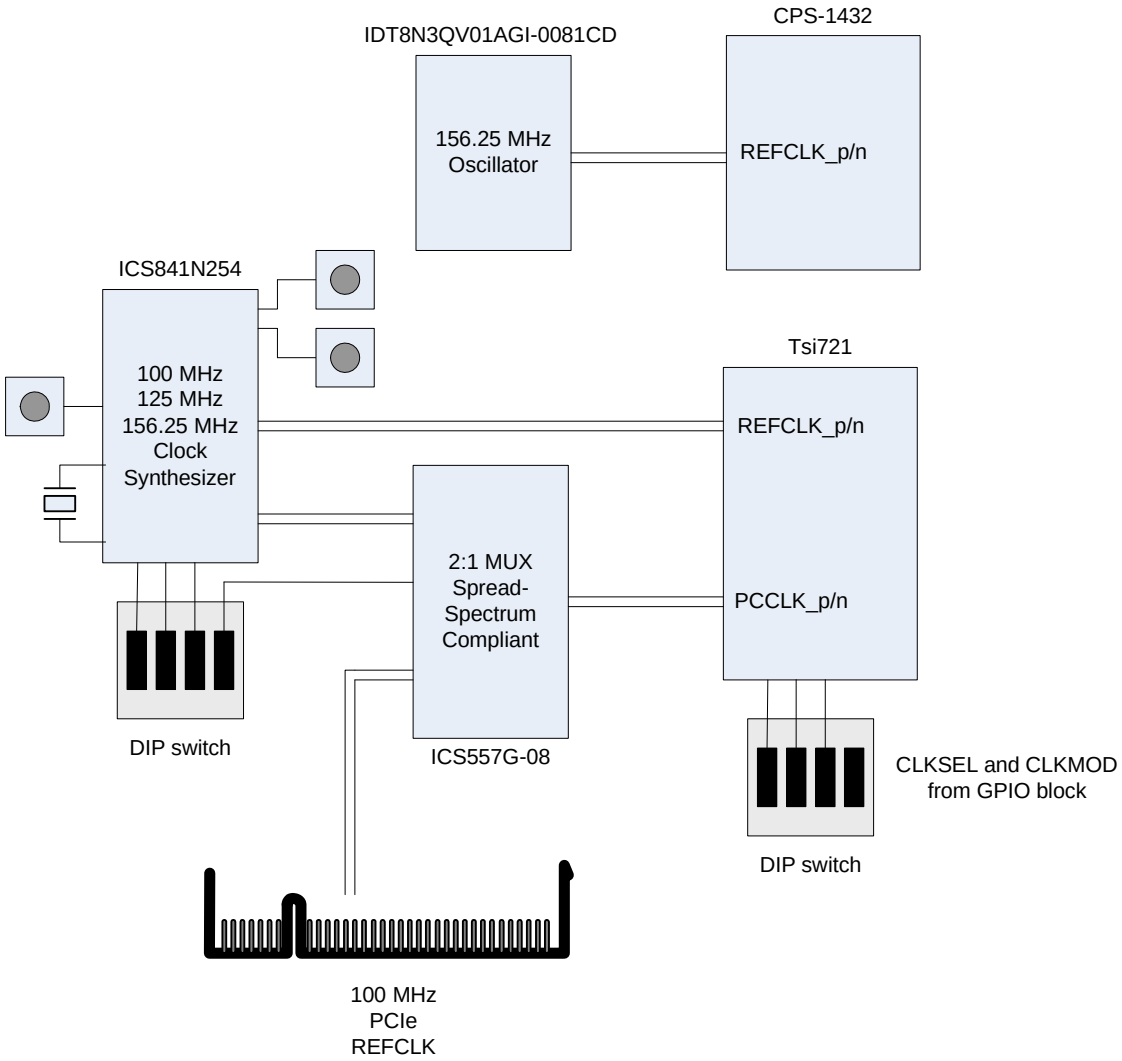
The FemtoClock synthesizer (ICS841N254i) is designed for S-RIO 1.3 and 2.1 applications. The synthesizer has phase jitter characteristic of 0.5 ps RMS specified for the 1–20 MHz frequency range, in compliance with S-RIO Gen2 switch reference clock requirement.

The synthesizer's source clock can be supplied from the on-board 25-MHz crystal, or from an external 25-MHz LVTTL reference clock. The synthesizer generates 156.25,125, or 100 MHz reference clock outputs. There are four clock outputs, two of which are HCSL and two LVDS: the HCSL output is used to drive Tsi721's PCCLK and REFCLK reference clock inputs through DC coupling. The LVDS reference clock output is available on SMA connectors.

The Tsi721 PCCLK can also be sourced from the host PC. A multiplexer is used to select between the on-board clock source or external clock source.

The CPS-1432 is clocked separately with an IDT VCXO (IDT8N3QV01) set at 156.25 MHz. The IDT8N3QV01 uses fourth-generation FemtoClock® NG technology.

Figure 8: Clock Generation and Distribution



2.5 Reset

Board-level reset is activated in two different ways: power-up and manual reset. These options are discussed below.

2.5.1 Power-Up Reset

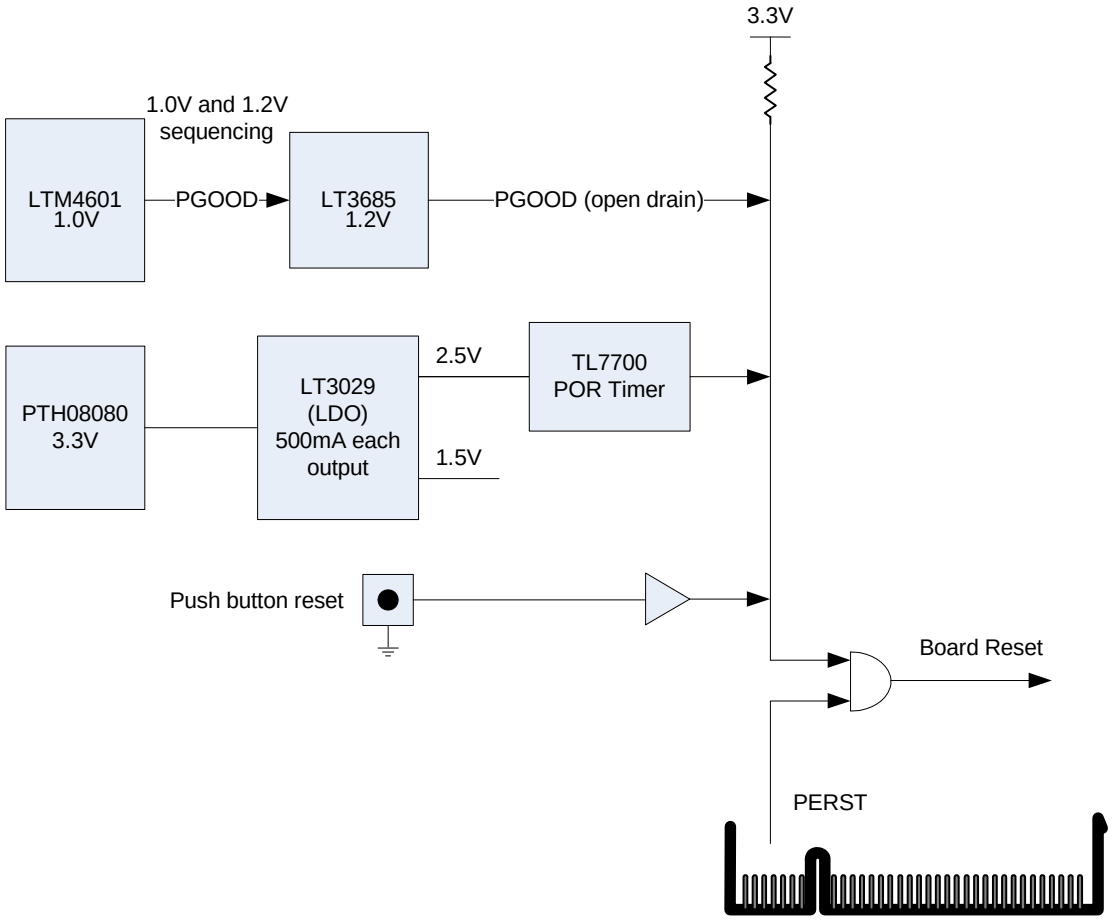
On power-up, the CPS-1432 and Tsi721 are held in reset by voltage supervisors/reset timers.

On-board voltage regulators provide Power Good status which are used for power sequencing and Reset control. There is one open-drain voltage supervisor "wired OR" together with the voltage regulator's Power Good status. The voltage supervisor controls the reset time. The combined power-up time of the 3.3V regulator followed by the 2.5V, then followed by release, is set to be longer than the 1.0V and 1.2V branches.

2.5.2 Manual Reset

A manual reset push-button is also OR-wired with the voltage supervisors (see Figure 9). The push button is debounced and buffered. A reset status LED is also provided for visual indication of the platform's reset status.

Figure 9: Board Reset Circuit



2.6 Power

The PCIe2 to S-RIO2 Evaluation Platform can be powered by an ATX power supply or a host PC.

The platform is design to operate stand-alone or use the host PC power. When operating stand-alone, the 20-pin ATX connector is used. When plugged into a PC, all options are available. Power can be obtained from the PCIe finger connector. If an ATX 20-pin connector is inserted or a 4-pin peripheral connector is inserted, a transistor will isolate the finger connector's power from the ATX power. This allows the use of an external supply even when connected in a PC.

When an ATX power supply is used as the power source, it is turned On/Off by an on-board push button. The push button toggles a flip-flop that drives the ON/OFF control of the ATX power supply. A jumper is provided to force the ATX supply ON. When the jumper is installed, the ATX supply is turned on regardless of the state of the flip-flop.

2.6.1 Voltage Regulators

The on-board voltage regulators are sized to supply the current requirement as listed in Table 2.

Table 2: PCIe2 to S-RIO2 Evaluation Platform Power Budget (Using Worst-Case Current Draw)

	3.3V	2.5V	1.5V	1.2V	1.0V
CPS-1432	0.027A	-	-	1.52	6.62A
Tsi721	0.1A	0.15A	0.35A	-	~ 1.5A
2 x SFP pwr	0.6A	-	-	-	-
Clock buffers	0.3A	-	-	-	-
Others (LEDs, etc)	0.2A	-	-	-	-
Total	1.23A	0.15A	0.35A	1.52A	8.12A

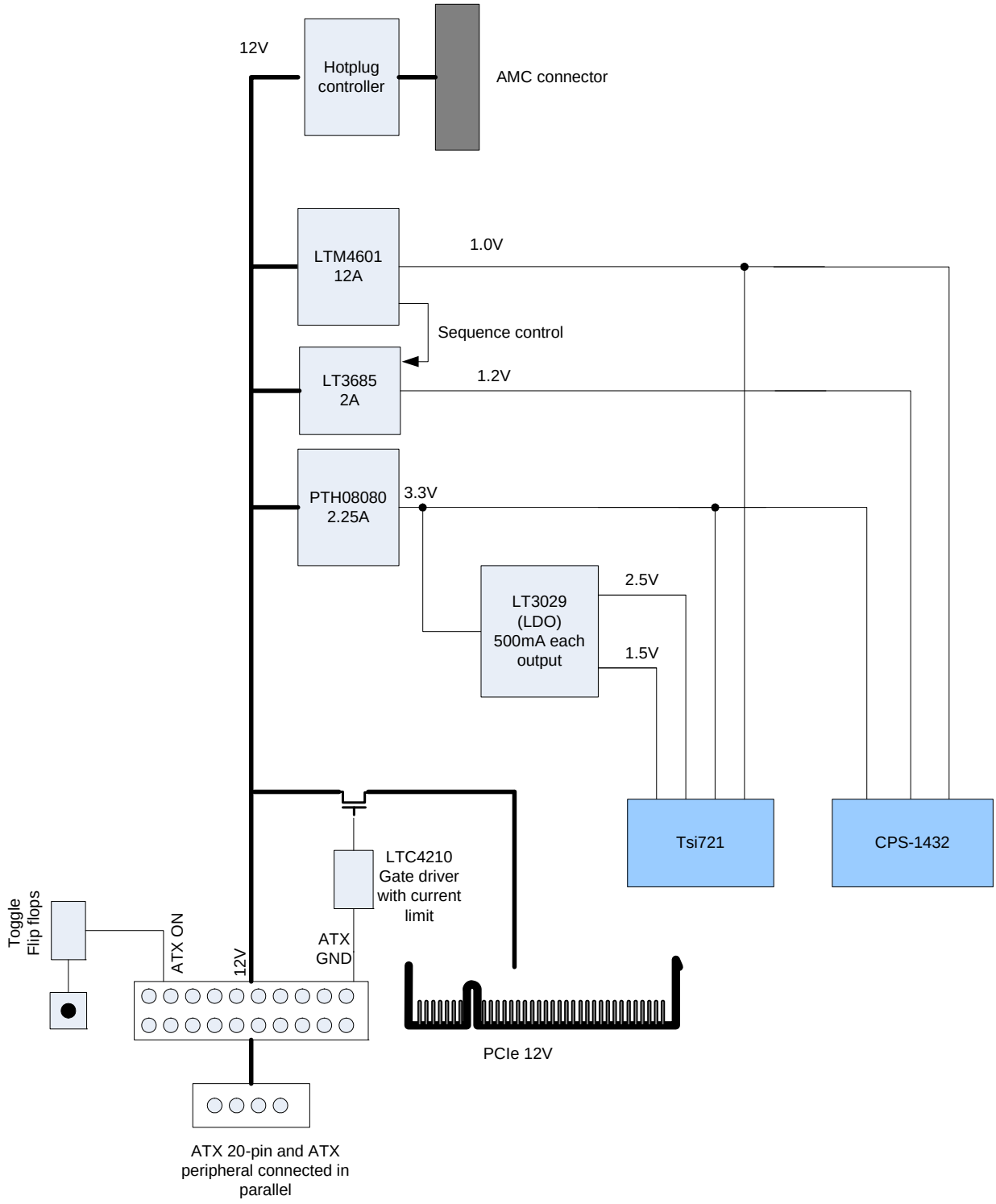
2.6.2 Power Distribution and Sequencing

Figure 10 represents the voltage regulators and associated control circuits as implemented on the PCIe2 to S-RIO2 Evaluation Platform. The CPS-1432 and Tsi721 VDD (1.0V) rails use a common voltage regulators.

The regulator's power-up sequence is controlled such that the 1.2V regulator is enabled after the 1.0V regulator is active.

The 3.3V regulator ramps up freely. It is used to supply a dual LDO regulator for the 2.5V and 1.5V supplies of Tsi721.

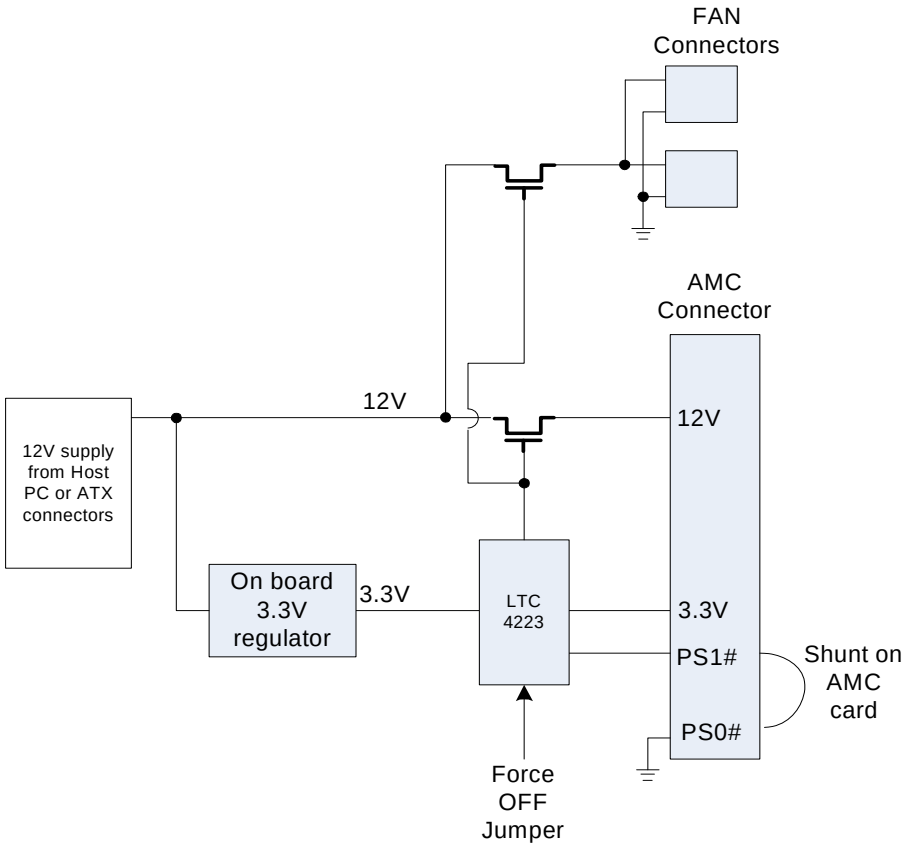
Figure 10: Voltage Regulators



2.7 AMC Connector Power Distribution

The AMC connector provides 12V and 3.3V power to the plug-in AMC modules. The 12V supply is gated with a high current Field Effect Transistor (FET). When inserted, the AMC module shunts the presence signals (PS1# connects to PS0#). When this connection is established, a hot swap controller turns the FET ON in a controlled fashion. In-rush current is limited and high current faults are detected. The hot swap controller can be used to manually keep AMC power OFF. A jumper is provided to force a power-down condition.

Figure 11: AMC Power Controller



2.7.1 AMC Module Current Limit

The hot swap controller provides short circuit protection. The current limit is programmed with a sense resistor in series in the 12V supply. The current limit is set to 6.25A per connector. The 3.3V supply should be used only for management power on the module, and is limited to 165 mA.

2.8 JTAG

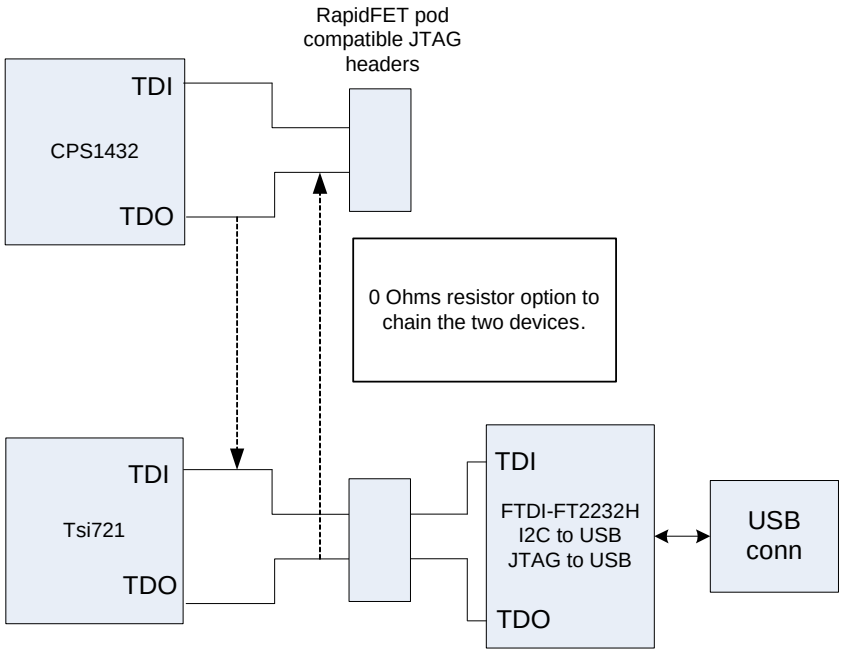
USB to JTAG bridging is supported using a FTDI-FT2232H device. The USB application drivers for Windows and Linux are available for download from www.ftdchip.com.

Only the Tsi721's JTAG port is connected to the FTDI chip. A connector is also provided to permit users to drive the JTAG chain with another type of device. The connector is in parallel with the FTDI chip. Contention between the FTDI chip and the dongle is avoided by disconnecting the USB cable. This effectively powers off the FTDI chip.

The CPS-1432's JTAG port is not connected to the FTDI chip; it is provided with its own JTAG header. There is a provision to chain the Tsi721 and CPS-1432 devices. For information on any restrictions to bridging the JTAG interfaces together, see the Tsi721 and CPS-1432 errata documents.

A mini type A USB connector is provided with access through the faceplate.

Figure 12: JTAG USB Driver



2.9 I2C Bus

The I2C bus interconnects the following devices:

- On-board USB-I2C converter
- Tsi721
- CPS-1432
- Two serial EEPROMS
- A Header for an external Master

2.9.1 Bus Masters

The Tsi721 and the USB-I2C converter can be I2C bus masters. The Tsi721 can be used to access other devices on the I2C bus. Tsi721-based I2C bus transactions require custom software applications. The Tsi721 also masters the I2C bus after reset to read the serial EEPROM.

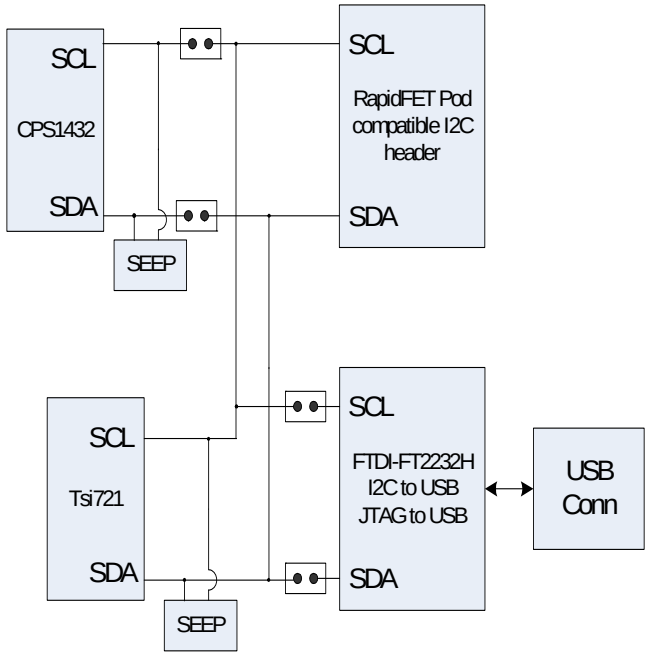
The USB-I2C converter is used to access the Tsi721 and CPS-1432 as slave devices. It is also used to program the serial EEPROM. The FTDI2232H that is used for USB to I2C conversion is not I2C compliant; it does not drive SDA and SCL (I2C data and clock line) as an open-drain signal. As such, when the USB to I2C converter is active, other masters cannot access the bus.

2.9.2 Bus Slaves

By default, the Tsi721, the CPS-1432, and the two serial EEPROMs, are bus slaves. It is only after reset that the CPS-1432 can master the I2C bus to access a serial EEPROM. Concurrently, the Tsi721 might also master the bus to read a serial EEPROM. Although the Tsi721 and CPS-1432 support multi-masters on the I2C bus, a pair of jumpers can be used to isolate the two devices on their own section of the I2C bus. When isolated, the two devices still have connection to their serial EEPROM.

The FDTI USB-I2C converter can be disconnected from the board's I2C chain with a pair of jumpers (see J41, J42 - I2C Chain On USB Controller).

Figure 13: I2C Block Diagram



The serial EEPROMs installed on the PCIe2 to S-RIO2 Evaluation Platform are AT24C64s. They use 7-bit addressing; the 3 lower bits of their address are common with the CPS-1432's and Tsi721's I2C IDs. They can be programmed on-board through the I2C header or USB cable. Table 3 show the I2C address of each slave device on the bus.

Table 3: I2C Address Map

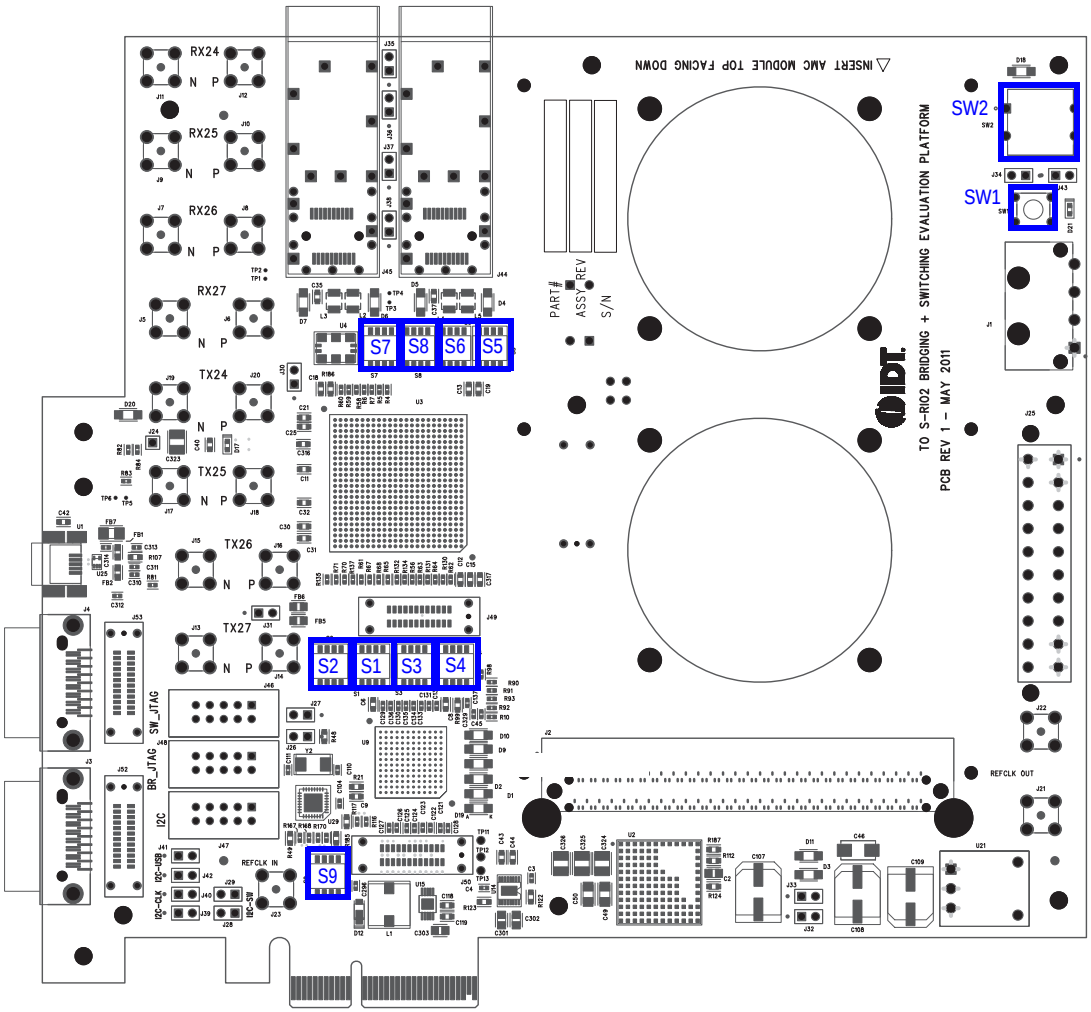
Device	I2C Address
CPS-1432	b110vxyz
EEPROM for CPS-1432	b1010xyz
Tsi721	b011abcd
EEPROM for Tsi721	b10100cd

3. Controls and Configurations

This chapter describes the configuration options on the PCIe2 to S-RIO2 Evaluation Platform.

3.1 Switch Locations

Figure 14: Switch Locations



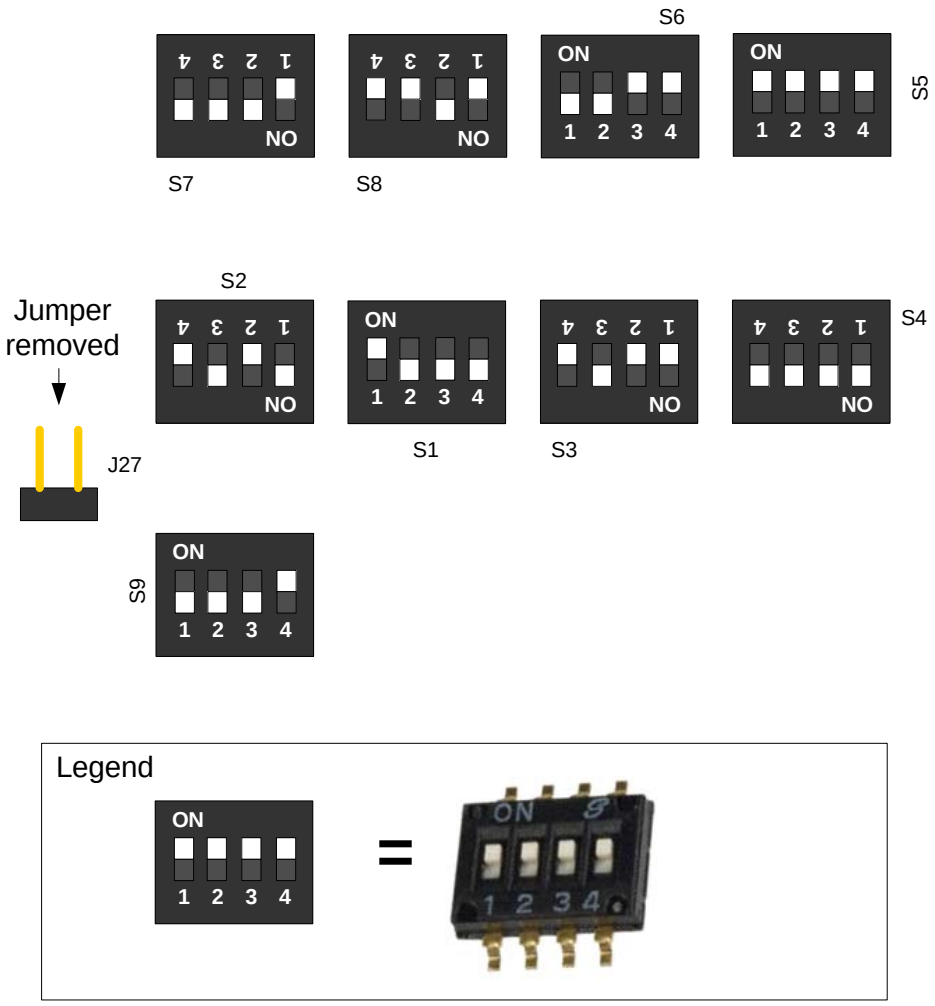
3.2 Default Configuration for Host PC

The PCIe2 to S-RIO2 Evaluation Platform is shipped with switches and jumpers set for operation in a host PC, as follows:

- Enable EEPROM load
- Tsi721 is an S-RIO host
- Tsi721 and CPS-1432 S-RIO bit rate is 3.125 Gbps
- Tsi721 is in PCIe common clock mode
- Tsi721 REFCLK PLLs (for S-RIO) is set for 156.25 MHz
- Tsi721 S-RIO does not start link training until software enables S-RIO
- Clock synthesizer for Tsi721 S-RIO REFCLK is set to 156.25 MHz
- Board reset driven by host PC (J27 is removed)

Figure 15 provides a quick switch setting reference for the configuration as described above.

Figure 15: Default Switch Settings



3.2.1 Stand-Alone Configuration

The PCIe2 to S-RIO2 Evaluation Platform can operate without being connected to a host PC. In this configuration, the Tsi721 does not have a reference clock and system reset from a host. This setup differs from the default configuration as follows:

- Tsi721 is in PCIe non-common clock mode
- Tsi721 PCCLK PLL (for PCIe) is set for 156.25 MHz
- Tsi721 S-RIO started link training after board reset
- J27 is installed

Figure 16: Stand-Alone Configuration Switch Setting

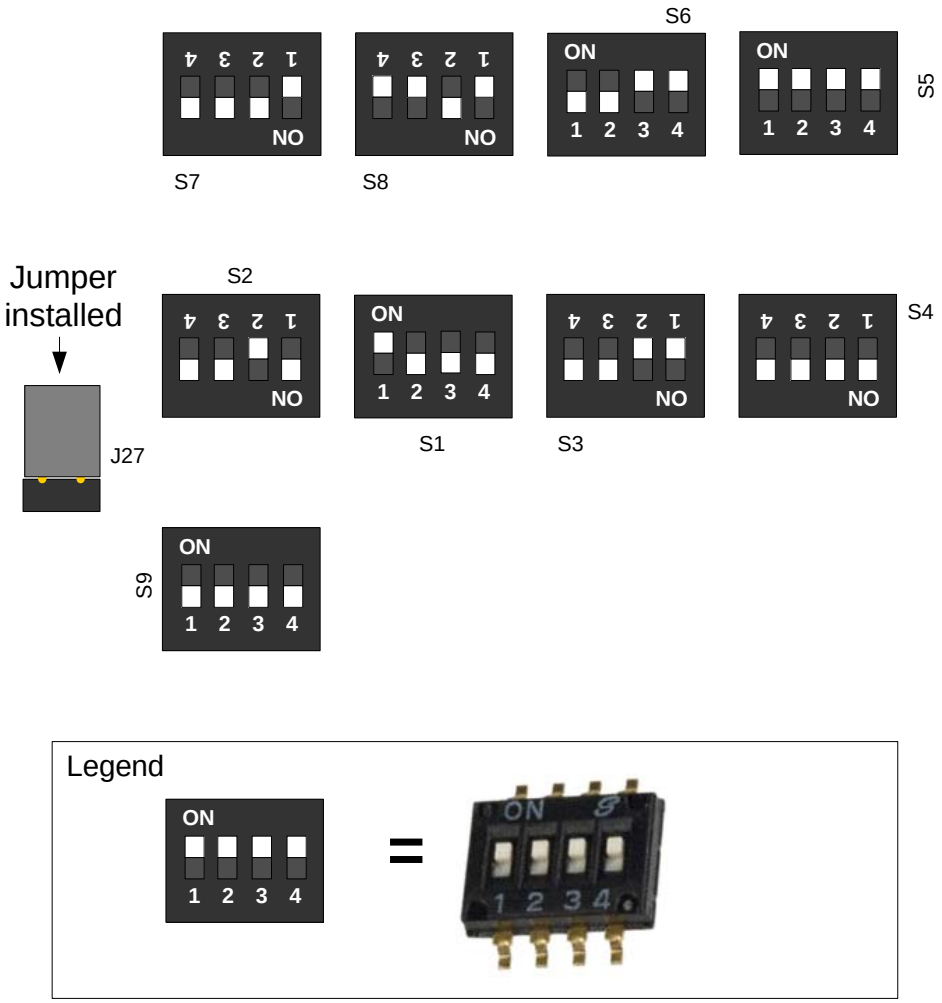


Table 4: S1 Setting (Tsi721)

Switch Number	Signal	Default Setting	Setup Value	Description
1	I2C_Disable	ON	ON = 0 OFF = 1	0 = Enable boot load from EEPROM 1 = Disable boot load from EEPROM
2	I2C_SEL	OFF		0 = The I2C_SA[1:0] pins are ignored and the lower two bits of the EEPROM address default to 00. 1 = The I2C_SA[1:0] pins represent the two LSBs of the 7-bit EEPROM slave address.
3	I2C_MA	OFF		I2C multi-byte address mode. If I2C_DISABLE == 0 (that is, download registers from EEPROM) then: 0 = Tsi721 uses 1-byte addressing for EEPROM 1 = Tsi721 uses 2-byte addressing for EEPROM Else I2C_DISABLE == 1 (do not download from EEPROM) 0 = Tsi721 is boot loaded via PCIe root complex after reset 1 = Tsi721 is boot loaded by an external I2C master after reset
4	SP_HOST	OFF		0 = Tsi721 is an S-RIO slave 1 = Tsi721 is an S-RIO host

Table 5: S2 Setting (Tsi721)

Switch Number	Signal	Default Setting	Setup Value	Description
1	STRAP_RATE[0]	ON	ON = 0 OFF = 1	STRAP_RATE[2:0] sets the RapidIO link rate 111 = 5 Gbaud 110 = 2.5 Gbaud 101 = 1.25 Gbaud 010 = 3.125 Gbaud Others = Reserved
2	STRAP_RATE[1]	OFF		
3	STRAP_RATE[2]	ON		
4	CLKMOD	OFF		0 = Tsi721 uses “PCIe non-common clock mode.” 1 = Tsi721 uses “PCIe common clock mode.”

Table 6: S3 Setting (Tsi721)

Switch Number	Signal	Default Setting	Setup Value	Description
1	SP_DEVID	OFF	ON = 0 OFF = 1	S-RIO base deviceID control 0 = Sets Base ID register to 0xFE 1 = Sets Base ID register to 0bxxxxxxx1 or 0b11111111 depending on SP_HOST
2	CLKSEL[0]	OFF		REFCLKP/REFCLKN clock frequency select: 0b11 = 125 MHz 0b10 = 100 MHz 0b01 = 156.25 MHz Others = Reserved When a 100-MHz clock is used, S-RIO SerDes rates of 1.25/2.5/5 Gbaud are supported. When a 125/156.25-MHz clock is used, S-RIO SerDes rates of 1.25/2.5/3.125/5 Gbaud are supported
3	CLKSEL[1]	ON		
4	SR_BOOT	ON	ON = 1 OFF = 0	0 = The Tsi721 S-RIO link can start training only after software sets the DEVCTL[SRBOOT_CMPL]. 1 = The Tsi721 S-RIO link can start training immediately after a fundamental reset and Tsi721 automatically sets the DEVCTL[SRBOOT_CMPL].

Table 7: S4 Setting (Tsi721)

Switch Number	Signal	Default Setting	Setup Value	Description
1	I2C_SA[0]	ON	ON = 0 OFF = 1	The values on these pins represent the lower 4 bits for the 7-bit address of the Tsi721 when acting as an I2C slave. These signals, in combination with the I2C_SEL signal, determine the address of the EEPROM to boot from. EEPROM address = 0b10100,SA[1],SA[0]
2	I2C_SA[1]	ON		
3	I2C_SA[2]	ON		
4	I2C_SA[3]	ON		

Table 8: S5 - Quadrant Configuration [3:0] (CPS-1432)

Switch Number	Signal	Default Setting	Setup Value	Description
1	QCFG0	ON	ON = 0 OFF = 1	Quadrant 0 port width: QCFG[1:0] 0:0 Lanes[0–3] in 4x Lanes[16–19] in 4x 0:1 Lanes[0–1] in 2x Lanes[2–3] in 2x Lanes[16–19] in 4x 1:0 Undefined 1:1 Undefined
2	QCFG1	ON		
3	QCFG2	ON	ON = 0 OFF = 1	Quadrant 1 port width: QCFG[3:2] 0:0 Lanes[4–7] in 4x Lanes[20–23] in 4x 0:1 Lanes[4–5] in 2x Lanes[6–7] in 2x Lanes[20–23] in 4x 1:0 Undefined 1:1 Undefined
4	QCFG3	ON		

Table 9: S6 - Quadrant Configuration [7:4] (CPS-1432)

Switch Number	Signal	Default Setting	Setup Value	Description
1	QCFG4	OFF	ON = 0 OFF = 1	Quadrant 2 port width: QCFG[5:4]] 0:0 Lanes[8–11] in 4x Lanes[24–27] in 4x 0:1 Lanes[8–9] in 2x Lanes[10–11] in 2x Lanes[24–27] in 4x 1:0 Lanes[8–9] in 2x Lanes[10–11] in 2x Lanes[24–25] in 2x Lanes[26–27] in 2x 1:1 Lanes[8–9] in 2x Lane[10] in 1x Lane[11] in 1x Lanes[24–27] in 4x
2	QCFG5	OFF		

Table 9: S6 - Quadrant Configuration [7:4] (CPS-1432)

Switch Number	Signal	Default Setting	Setup Value	Description
3	QCFG6	ON	ON = 0 OFF = 1	Quadrant 3 port width: QCFG[7:6] 0:0 Lanes[12–15] in 4x Lanes[28–31] in 4x 0:1 Lanes[12–13] in 2x Lanes[14–15] in 2x Lanes[28–31] in 4x 1:0 Lanes[12–13] in 2x Lanes[14–15] in 2x Lanes[28–29] in 2x Lanes[30–31] in 2x 1:1 Lanes[12–13] in 2x Lane[14] in 1x Lanes[15] in 1x Lanes[28–31] in 1x
4	QCFG7	ON		

Table 10: S7 - I2C ID (CPS-1432)

Switch Number	Signal	Default Setting	Setup Value	Description
1	ID0	OFF	ON = 0 OFF = 1	Switch I2C AD =0b110[ID3,ID2,ID1,ID0] Serial EPROM AD = 0b1010[ID2,ID1,ID0]
2	ID1	ON		
3	ID2	ON		
4	ID3	ON		

Table 11: S8 - SPD[2:0] (CPS-1432)

Switch Number	Signal	Default Setting	Setup Value	Description
1	SPD2	OFF	ON = 0 OFF = 1	SPEED_SELECT[2:0] sets the RapidIO link rate. 000 = 1.25 Gbaud 001 = 2.5 Gbaud 01X = 5 Gbaud 100 = Reserved 101 = 3.125 Gbaud 11X = 6.25 Gbaud
2	SDP1	ON		
3	SPD0	OFF		
4	FSEL0	OFF		Internal core clock frequency selector 0 = 156.25 MHz (All speeds up to 3.125 Gbaud with IDLE2; all speeds up to 2.5 Gbaud with IDLE1) 1 = 312.5 MHz (Default value; all speeds including 6.25 Gbaud)

Table 12: S9 - Clock Synthesizer Control

Switch Number	Signal	Default Setting	Setup Value	Description
1	FSEL0	OFF	ON = 1 OFF = 0	FSEL[1:0] = Output frequency 0:0 = 156.25 MHz 0:1 = 125 MHz 1:0 = 100 MHz 1:1 = 250 MHz
2	FSEL1	OFF		
3	REF_SEL	OFF		0 = Reference clock from Crystal 1 = Reference clock from J23
4	Clock Source Select	ON	ON = 0 OFF = 1	0 = Tsi721 PCCLK source is from PCIe finger connector 1 = Tsi721 PCCLK source is from on-board oscillator

3.2.2 SW1 - Board Reset

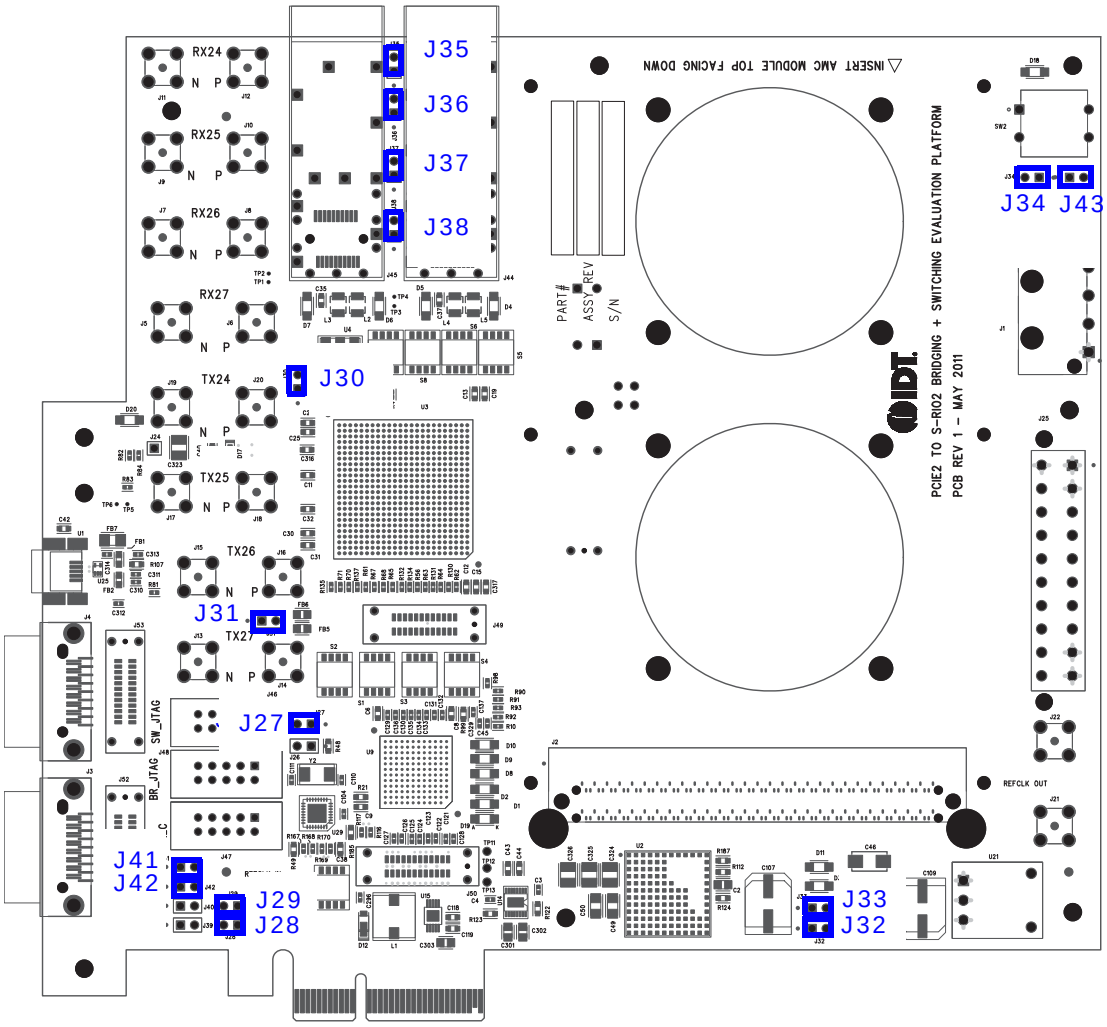
When SW1 is pushed, a debounced board reset is activated.

3.2.3 SW2 - Board Power

SW2 is a tactile push-button switch. Push once to enable the ATX power supply. Push again to disable power. Power for the latch is provided by the 5V standby rail of the ATX power supply.

3.3 Jumpers

Figure 17: Jumper Locations



3.3.1 J27 - PCIe RESET Pull-Up

PCIe Reset should be driven by a host PC. If the platform is not connected in a PC, J27 must be installed to prevent the PCIe Reset input from floating. PCIe Reset is used to reset the platform.

Table 13: J27 - PCIe Reset Pull-Up

Shunt Jumper Location	Description	Default Setting
IN	PCIe Reset is pulled up	OUT
OUT	PCIe Reset is floating and should be driven by a host PC.	

3.3.2 J28, J29 - I2C Chain Disconnect (CPS-1432)

J28 and J29 connect the platform's I2C SDA and SCL to the CPS-1432. They can be removed to avoid having both the Tsi721 and CPS-1432 on the same chain. The serial EEPROM for the CPS-1432 is still connected to the device's I2C port when the jumpers are removed.

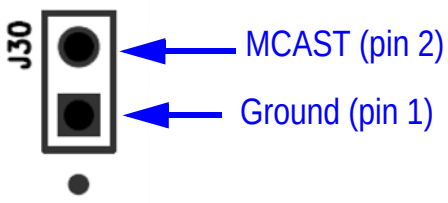
Table 14: J28, J29 - I2C Chain Disconnect (CPS-1432)

Shunt Jumper Location	Description	Default Setting
IN	I2C chain is connected to CPS-1432	IN
OUT	I2C is disconnected from CPS-1432	

3.3.3 J30 - Multicast External Input (CPS-1432)

J30 connects external equipment to the MCAST pin of the CPS-1432. The input voltage on J30 should not exceed 3.3V.

Figure 18: J30 Pin Assignment



3.3.4 J31 - I2C Master or Slave Mode (CPS-1432)

J31 selects the I2C master/slave mode for the CPS-1432.

Table 15: J31 - I2C Mode (CPS-1432)

Shunt Jumper Location	Description	Default Setting
IN	Master mode	OUT
OUT	Slave mode	

3.3.5 J32, J33 - I2C Chain On AMC Connector

J32 and J33 connect the platform's I2C SDA and SCL to the AMC connector's I2C pins. These jumpers should be installed when the I2C chain is required by an AMC module.

Table 16: J32, J33 - I2C Chain on AMC Connector

Shunt Jumper Location	Description	Default Setting
IN	I2C connected to AMC module	OUT
OUT	I2C disconnected from I2C module	

3.3.6 J34 - AMC Power OFF

J34 forces a power off condition on the AMC module.

Table 17: J34 - AMC Power OFF

Shunt Jumper Location	Description	Default Setting
IN	AMC power OFF	OUT
OUT	AMC power under hot swap control	

3.3.7 J35, J36 - SFP (J44) Module Rate Select RS0, RS1

SFP module Rate Select pins (RS0 and RS1) are set with these two jumpers.

Table 18: J35, J36 - SFP (J44) RS0, RS1 Setting

Jumper	Shunt Jumper Location	Description	Default Setting
J35	IN	RS0 = 0	OUT
	OUT	RS0 = 1	
J36	IN	RS1 = 0	OUT
	OUT	RS1 = 1	

3.3.8 J37, J38 - SFP (J45) Module Rate Select RS0, RS1

SFP module Rate Select pins (RS0 and RS1) are set with these two jumpers.

Table 19: J37, J38 - SFP (J45) RS0, RS1 Setting

Jumper	Shunt Jumper Location	Description	Default Setting
J38	IN	RS0 = 0	OUT
	OUT	RS0 = 1	
J37	IN	RS1 = 0	OUT
	OUT	RS1 = 1	

3.3.9 J41, J42 - I2C Chain On USB Controller

J41 and J42 connect the PCIe2 to S-RIO2 Evaluation Platform's I2C SDA and SCL to the USB Controller. These jumpers should be installed when the I2C chain is controlled by a PC host via USB.

Table 20: J41, J42 - I2C Chain on USB Controller

Shunt Jumper Location	Description	Default Setting
IN	I2C driven by USB controller	IN
OUT	I2C disconnected from USB controller	

3.3.10 J43 - Force ATX Power ON

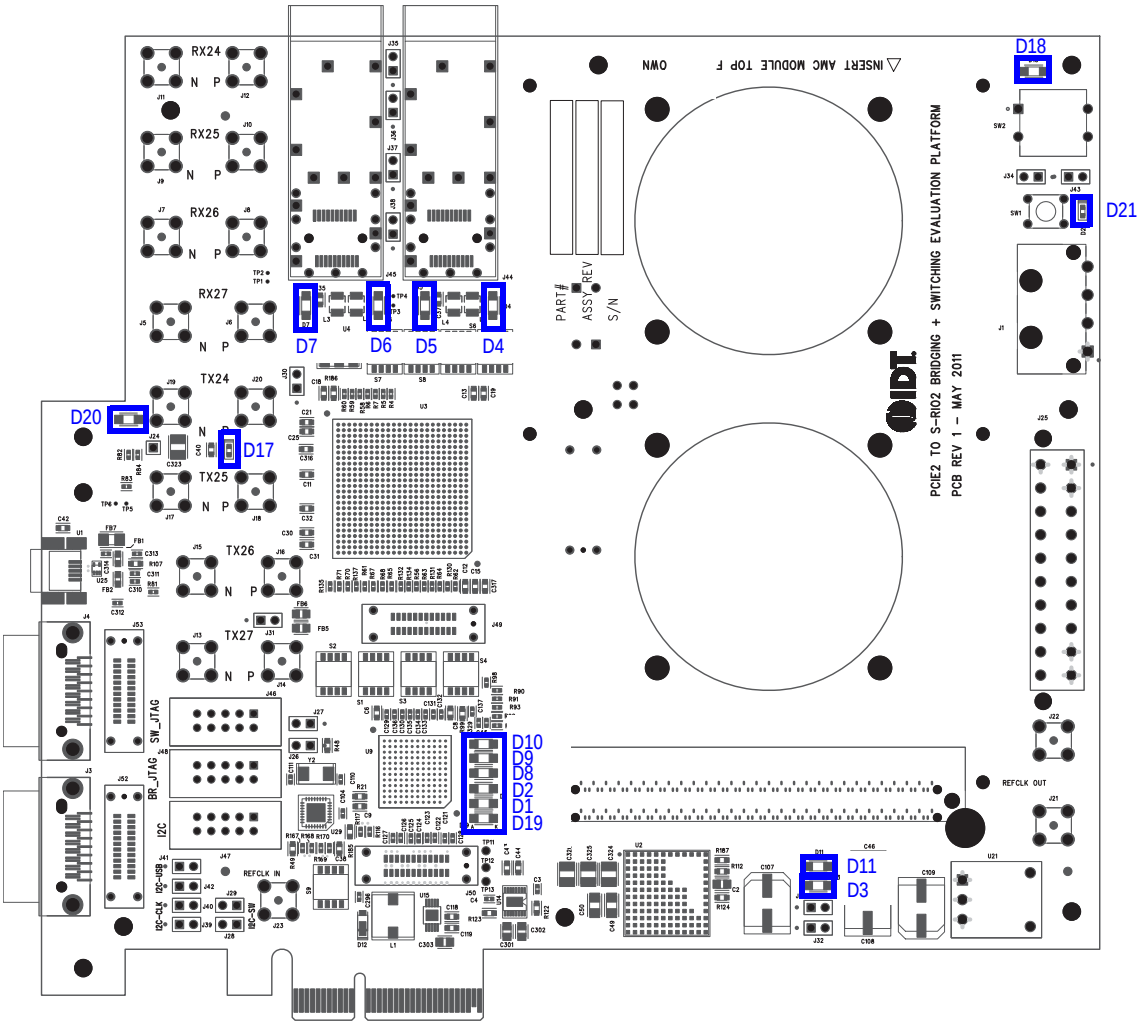
Use J43 for the ATX supply ON.

Table 21: J43 - Force ATX Power ON

Shunt Jumper Location	Description	Default Setting
IN	Force the ATX supply ON	OUT
OUT	Normal operation. ATX supply is turned ON/OFF by push button SW2.	

3.4 Displays (LEDs)

Figure 19: LED Locations



3.4.1 D1 - PCIe LINK STATUS

D1 indicates the status of the PCIe link.

Table 22: D1 LED

Location	Color	Description
D1	Green	ON = PCIe link active OFF = PCIe link not active

3.4.2 D2 - User LED

D2 is tied to GPIO[3] of the Tsi721. It can be used by software to test access to GPIO configuration registers.

Table 23: D2 LED

Location	Color	Description
D2	Green	ON = GPIO[3] set to 1 OFF = GPIO[3] set to 0

3.4.3 D3 - AMC Enable Status LED

D3 indicates the status of the AMC module power.

Table 24: D3 LED

Location	Color	Description
D3	Green	ON = 12V and 3.3V Power is ON OFF = Power is OFF

3.4.4 D4, D5 - SFP Module (J44) Status LED

D4 and D5 are tied to the LOS and FAULT status pins from the SFP module.

Table 25: D4, D5 LEDs

Location	Color	Description
D4	Green	ON = TX_FAULT is normal (no fault) OFF = TX_FAULT is indicating a fault
D5	Green	ON = RX_LOS is normal (no loss of signal) OFF = RX_LOS is indicating loss of signal

3.4.5 D6, D7 - SFP Module (J45) Status LED

D6 and D7 are tied to the LOS and FAULT status pins from the SFP module.

Table 26: D6, D7 LEDs

Location	Color	Description
D6	Green	ON = TX_FAULT is normal (no fault) OFF = TX_FAULT is indicating a fault
D7	Green	ON = RX_LOS is normal (no loss of signal) OFF = RX_LOS is indicating loss of signal

3.4.6 D8 - Tsi721 Error

D8 indicates an uncorrectable error has occured in the Tsi721.

Table 27: D8 LED

Location	Color	Description
D8	Red	ON = Error(s) occured OFF = Normal operation

3.4.7 D9 - Tsi721 S-RIO RESET OUT

D9 indicates the status of the SRRSTOn pin of the Tsi721.

Table 28: D9 LED

Location	Color	Description
D9	Red	ON = S-RIO Reset symbol received by Tsi721 OFF = Normal operation

3.4.8 D10 - Tsi721 PCIe RESET OUT

D10 indicates the status of the PCRSTOn pin of the Tsi721.

Table 29: D10 LED

Location	Color	Description
D10	Red	ON = PCIe port detects Hot Reset or the PCIe link is in DL_DOWN state OFF = Normal operation

3.4.9 D11 - AMC Power Fault

D10 indicates the AMC hot plug controller has detected an over-current condition on 3.3V or 12V supply to the AMC connector.

Table 30: D11 LED

Location	Color	Description
D11	Red	ON = Power fault OFF = Normal operation

3.4.10 D17 - Interrupt Pending LED (CPS-1432)

D17 indicates the interrupt pin on the CPS-1432 is low, indicating an interrupt pending.

Table 31: D17 LED (CPS-1432)

Location	Color	Description
D17	Orange	ON = Interrupt pending OFF = No interrupt

3.4.11 D18 - ATX 12V Power LED

D18 indicates the status of the ATX power supply 12V rail.

Table 32: D18 LED

Location	Color	Description
D18	Green	ON = 12V Power is ON OFF = 12V Power is OFF

3.4.12 D19 - Tsi721 Interrupt

D19 indicates the Tsi721 has a pending interrupt.

Table 33: D19 LED

Location	Color	Description
D19	Yellow	ON = Interrupt pending OFF = No interrupt

3.4.13 D20 - USB Power LED

D20 indicates the status of the power supplied by the host PC to the USB circuit. This LED must be on in order for the on-board USB to JTAG and USB to I2C controller to function properly.

Table 34: D20 LED

Location	Color	Description
D20	Green	ON = USB Power (from Host PC) is ON OFF = USB Power is not present

3.4.14 D21 - Board Reset Status LED

D21 indicates the status of the on-board reset circuit. Reset is controlled by a push button and the on-board voltage supervisors.

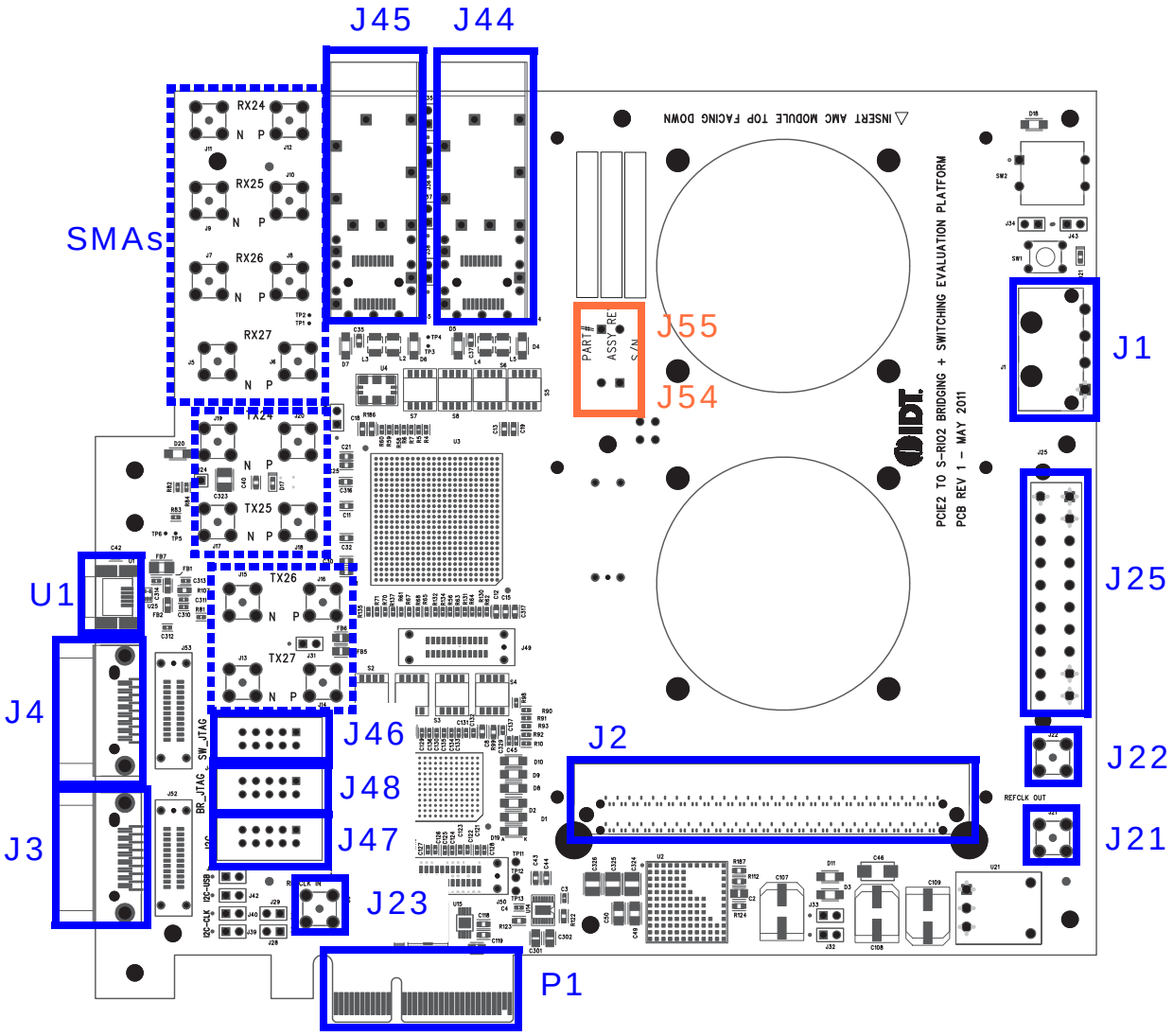
Table 35: D21 LED

Location	Color	Description
D21	Blue	ON = Board is out of reset OFF = Board is in reset

4. Connectors

This chapter describes the connectors on the PCIe2 to S-RIO2 Evaluation Platform.

4.1 Connector Locations



4.2 Connector Specification

This section describes the platform's connectors and their pin assignments.

4.2.1 P1 - PCIe Finger Connector

The PCIe finger connector matches the mechanical and pin assignments of *PCI Express Card Electromechanical Specification Revision 2.0*. It is intended to be plugged directly in a host PC.

Figure 20: P1 - PCIe Finger Connector (Side B Shown)

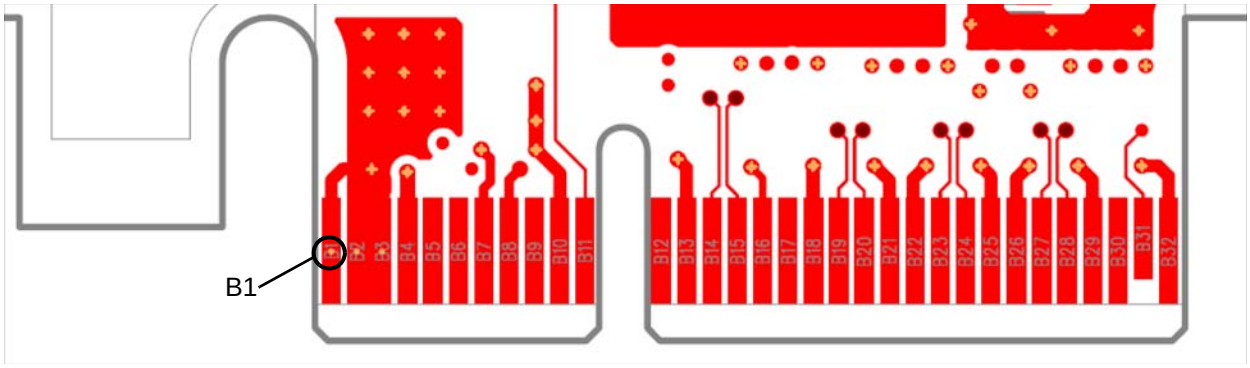


Table 36: PCIe Finger Connector Signal Assignment

Pin Number	Side B		Side A	
	Name	Description	Name	Description
1	+12V	12V power	PRSNT1#	Hot-plug presence detect
2	+12V	12V power	+12V	12V power
3	+12V	12V power	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	Not used	JTAG2	Not used
6	SMDAT	Not used	JTAG3	Connected to JTAG4
7	GND	Ground	JTAG4	Connected to JTAG3
8	+3.3V	3.3V power	JTAG5	Not used
9	JTAG1	Not used	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for link reactivation	PERST#	Fundamental reset
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Connected to Tsi721 PCIE_RX0	REFCLK-	
15	PETn0		GND	Ground

Table 36: PCIe Finger Connector Signal Assignment

Pin Number	Side B		Side A	
	Name	Description	Name	Description
16	GND	Ground	PERp0	Connected to Tsi721 PCIE_TX0
17	PRSNT2#	Not used	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Connected to Tsi721 PCIE_RX1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Connected to Tsi721 PCIE_TX1
22	GND	Ground	PERn1	
23	PETp2	Connected to Tsi721 PCIE_RX2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Connected to Tsi721 PCIE_TX2
26	GND	Ground	PERn2	
27	PETp3	Connected to Tsi721 PCIE_RX3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Connected to Tsi721 PCIE_TX3
30	RSVD	Reserved	PERn3	
31	PRSNT2#	Hot-plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

4.2.2 J2 - AMC Connector

The AMC connector is from Yamaichi: CN074-170-0005 [CONN AMC B+ MEZZ 170POS 0.75MM]. It is installed on the PCB using Compression Mount Technology. As such it is not soldered on the platform. The electrical contacts are established through the compression of the connector's micro contacts on the PCB by screwing a compression plate on the back of the connector. The connector is specified to support 12.5 Gbaud.

The *PICMG AMC.0 R2.0 Specification* defines the connectors' pin mapping - AMC carrier connector pin assignment for the B+ footprint. S-RIO lane mapping for AMC connectors is defined by AMC.4 Fabric Port Assignment on Basic and Extended Connectors. In addition, AMC lanes 17–20 are also connected as per the SCOPE Alliance proposed mapping.

4.2.2.1 AMC Connector Pinout

Table 37: J2 - AMC Connector Signal Assignment

Pin Number	AMC Signal	J2 Signal	Description
B2	MB_PWR	12V rail	Payload Power
B3	MB_PS1#	Pull up to 3.3V	Presence 1
B4	MB_MP	Hot Swap Controller 3.3V (170 mA)	Management Power
B5	MB_GA0	NC	Geographic Addr. 0
B6	MB_RSRVD6	NC	Reserved, not connected
B8	MB_RSRVD8	NC	Reserved, not connected
B9	MB_PWR	12V rail	Payload Power
B11	MB_Rx0+	NC	Port 0 Receiver +
B12	MB_Rx0-	NC	Port 0 Receiver -
B14	MB_Tx0+	NC	Port 0 Transmitter +
B15	MB_Tx0-	NC	Port 0 Transmitter -
B17	MB_GA1	GND	Geographic Addr. 1
B18	MB_PWR	12V rail	Payload Power
B20	MB_Rx1+	NC	Port 1 Receiver +
B21	MB_Rx1-	NC	Port 1 Receiver -
B23	MB_Tx1+	NC	Port 1 Transmitter +
B24	MB_Tx1-	NC	Port 1 Transmitter -
B26	MB_GA2	GND	Geographic Addr. 2
B27	MB_PWR	12V rail	Payload Power
B29	MB_Rx2+	NC	Port 2 Receiver +
B30	MB_Rx2-	NC	Port 2 Receiver -
B32	MB_Tx2+	NC	Port 2 Transmitter +
B33	MB_Tx2-	NC	Port 2 Transmitter -
B35	MB_Rx3+	NC	Port 3 Receiver +
B36	MB_Rx3-	NC	Port 3 Receiver -
B38	MB_Tx3+	NC	Port 3 Transmitter +
B39	MB_Tx3-	NC	Port 3 Transmitter -

Table 37: J2 - AMC Connector Signal Assignment ***(Continued)***

Pin Number	AMC Signal	J2 Signal	Description
B41	MB_ENABLE#	Hot Swap Controller and Board Reset Circuit	AMC Enable
B42	MB_PWR	12V RAIL	Payload Power
B44	MB_Rx4+	Lane 20 Rx+	Port 4 Receiver +
B45	MB_Rx4-	Lane 20 Rx-	Port 4 Receiver -
B47	MB_Tx4+	Lane 20Tx+	Port 4 Transmitter +
B48	MB_Tx4-	Lane 20 Tx-	Port 4 Transmitter -
B50	MB_Rx5+	Lane 21 Rx+	Port 5 Receiver +
B51	MB_Rx5-	Lane 21 Rx-	Port 5 Receiver -
B53	MB_Tx5+	Lane 21 Tx+	Port 5 Transmitter +
B54	MB_Tx5-	Lane 21 Tx-	Port 5 Transmitter -
B56	MB_SCL_L	Board SCL	IPMB-L Clock
B57	MB_PWR	12V rail	Payload Power
B59	MB_Rx6+	Lane 22 Rx+	Port 6 Receiver +
B60	MB_Rx6-	Lane 22 Rx-	Port 6 Receiver -
B62	MB_Tx6+	Lane 22 Tx+	Port 6 Transmitter +
B63	MB_Tx6-	Lane 22 Tx-	Port 6 Transmitter -
B65	MB_Rx7+	Lane 23 Rx+	Port 7 Receiver +
B66	MB_Rx7-	Lane 23 Rx-	Port 7 Receiver -
B68	MB_Tx7+	Lane 23 Tx+	Port 7 Transmitter +
B69	MB_Tx7-	Lane 23 Tx-	Port 7 Transmitter -
B71	MB_SDA_L	Board SDA	IPMB-L Data
B72	MB_PWR	12V rail	Payload Power
B74	MB_TCLKA+ (CLK1)	NC	Telecom Clock A +
B75	MB_TCLKA- (CLK1)	NC	Telecom Clock A -
B77	MB_TCLKB+ (CLK2)	NC	Telecom Clock B +

Table 37: J2 - AMC Connector Signal Assignment ***(Continued)***

Pin Number	AMC Signal	J2 Signal	Description
B78	MB_TCLKB- (CLK2)	NC	Telecom Clock B -
B80	MB_FCLKA+ (CLK3)	NC	Fabric Clock A +
B81	MB_FCLKA- (CLK3)	NC	Fabric Clock A -
B83	MB_PS0#	GND	Presence 0
B84	MB_PWR	12V rail	Payload Power
B87	MB_Tx8-	Lane 16 Tx+	Port 8 Transmitter -
B88	MB_Tx8+	Lane 16 Tx-	Port 8 Transmitter +
B90	MB_Rx8-	Lane 16 Rx+	Port 8 Receiver -
B91	MB_Rx8+	Lane 16 Rx-	Port 8 Receiver +
B93	MB_Tx9-	Lane 17 Tx+	Port 9 Transmitter -
B94	MB_Tx9+	Lane 17Tx-	Port 9 Transmitter +
B96	MB_Rx9-	Lane 17 Rx+	Port 9 Receiver -
B97	MB_Rx9+	Lane 17 Rx-	Port 9 Receiver +
B99	MB_Tx10-	Lane 18 Tx+	Port 10 Transmitter -
B100	MB_Tx10+	Lane 18 Tx-	Port 10 Transmitter +
B102	MB_Rx10-	Lane 18 Rx+	Port 10 Receiver -
B103	MB_Rx10+	Lane 18 Rx-	Port 10 Receiver +
B105	MB_Tx11-	Lane 19 Tx+	Port 11 Transmitter -
B106	MB_Tx11+	Lane 19 Tx-	Port 11 Transmitter +
B108	MB_Rx11-	lane 19 Rx+	Port 11 Receiver -
B109	MB_Rx11+	Lane 19 Rx-	Port 11 Receiver +
B111	MB_Tx12-	NC	Port 12 Transmitter -
B112	MB_Tx12+	NC	Port 12 Transmitter +
B114	MB_Rx12-	NC	Port 12 Receiver -
B115	MB_Rx12+	NC	Port 12 Receiver +
B117	MB_Tx13-	NC	Port 13 Transmitter -
B118	MB_Tx13+	NC	Port 13 Transmitter +

Table 37: J2 - AMC Connector Signal Assignment ***(Continued)***

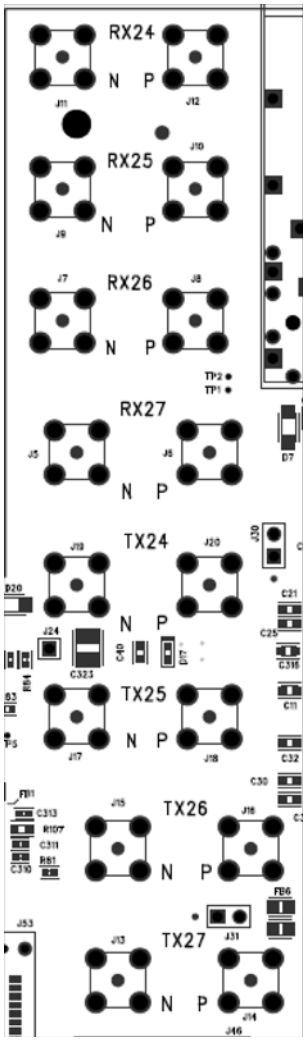
Pin Number	AMC Signal	J2 Signal	Description
B120	MB_Rx13-	NC	Port 13 Receiver -
B121	MB_Rx13+	NC	Port 13 Receiver +
B123	MB_Tx14-	NC	Port 14 Transmitter -
B124	MB_Tx14+	NC	Port 14 Transmitter +
B126	MB_Rx14-	NC	Port 14 Receiver -
B127	MB_Rx14+	NC	Port 14 Receiver +
B129	MB_Tx15-	NC	Port 15 Transmitter -
B130	MB_Tx15+	NC	Port 15 Transmitter +
B132	MB_Rx15-	NC	Port 15 Receiver -
B133	MB_Rx15+	NC	Port 15 Receiver +
B135	MB_TCLKC-	NC	Telecom Clock C -
B136	MB_TCLKC+	NC	Telecom Clock C +
B138	MB_TCLKD-	NC	Telecom Clock D -
B139	MB_TCLKD+	NC	Telecom Clock D +
B141	MB_Tx17-	Lane 7 Tx+	Port 17 Transmitter -
B142	MB_Tx17+	Lane 7 Tx-	Port 17 Transmitter +
B144	MB_Rx17-	Lane 7 Rx+	Port 17 Receiver -
B145	MB_Rx17+	Lane 7 Rx-	Port 17 Receiver +
B147	MB_Tx18-	Lane 6 Tx+	Port 18 Transmitter -
B148	MB_Tx18+	Lane 6 Tx-	Port 18 Transmitter +
B150	MB_Rx18-	Lane 6 Rx+	Port 18 Receiver -
B151	MB_Rx18+	Lane 6 Rx-	Port 18 Receiver +
B153	MB_Tx19-	Lane 5 Tx+	Port 19 Transmitter -
B154	MB_Tx19+	Lane 5 Tx-	Port 19 Transmitter +
B156	MB_Rx19-	Lane 5 Rx+	Port 19 Receiver -
B157	MB_Rx19+	Lane 5 Rx-	Port 19 Receiver +
B159	MB_Tx20-	Lane 4 Tx+	Port 20 Transmitter -
B160	MB_Tx20+	Lane 4 Tx-	Port 20 Transmitter +
B162	MB_Rx20-	Lane 4 Rx+	Port 20 Receiver -

Table 37: J2 - AMC Connector Signal Assignment ***(Continued)***

Pin Number	AMC Signal	J2 Signal	Description
B163	MB_Rx20+	Lane 4 Rx-	Port 20 Receiver +
B165	MB_TCK	NC	JTAG Test clock Input
B166	MB_TMS	NC	JTAG Test Mode Select In
B167	MB_TRST#	NC	JTAG Test Reset Input
B168	MB_TDO	NC	JTAG Test clock Output
B169	MB_TDI	NC	JTAG Test clock Input

4.2.3 SMA Connectors

Figure 21: Signal Distribution on SMA Connectors



The switch lane connected to SMA connectors are assigned as follows:

- Each TX+ connects to one SMA
- Each TX- connects to one SMA adjacent to TX+
- Each RX+ connects to one SMA
- Each RX- connects to one SMA adjacent to RX+

In total, there are 16 SMA connectors. The lanes are identified on the PCB as shown in Figure 21.

4.2.4 J3, J4 - CX4 InfiniBand Connectors

Fujitsu's MicroGIGaCN FCN268-D008G/1D (CX4) InfiniBand connectors extend out on the PCI faceplate. A wide range of cables are available for these connectors. When selecting a cable type for the InfiniBand connectors, verify that they are specified for the desired bit rate.

Switch lane to connector mapping is displayed in Table 38. The connector pinout is shown in Figure 22. S(1) and S(2) are connected to a differential pair. There are eight differential pairs on the connector. The switch lane to connector connection is wired to match the InfiniBand connectivity specification. As such, it is possible to connect to any other InfiniBand compatible board using an InfiniBand crossover cable.

Figure 22: InfiniBand Connector Pin Assignment

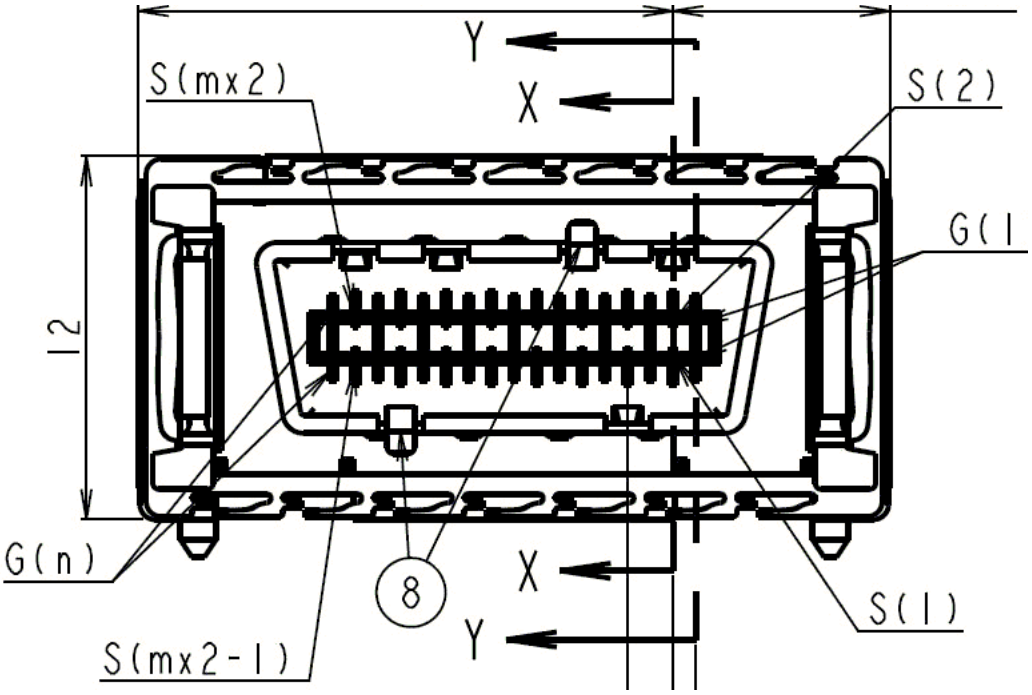


Table 38: J3 - J4 InfiniBand Connector to Switch Lane Mapping

Connector Pin Number	InfiniBand Signal Name	CPS-1432	
		J3	J4
S1	IBtxIp(0)	Lane 28 Rx+	Lane 12 Rx+
S2	IBtxIn(0)	Lane 28 Rx-	Lane 12 Rx-
S3	IBtxIp(1)	Lane 29 Rx+	Lane 13 Rx+
S4	IBtxIn(1)	Lane 29 Rx-	Lane 13 Rx-
S5	IBtxIp(2)	Lane 30 Rx+	Lane 14 Rx+
S6	IBtxIn(2)	Lane 30 Rx-	Lane 14 Rx-
S7	IBtxIp(3)	Lane 31 Rx+	Lane 15 Rx+

Table 38: J3 - J4 InfiniBand Connector to Switch Lane Mapping ***(Continued)***

Connector Pin Number	InfiniBand Signal Name	CPS-1432	
		J3	J4
S8	IBtxIn(3)	Lane 31 Rx-	Lane 15 Rx-
S9	IBtxOn(3)	Lane 31 Tx-	Lane 15 Tx-
S10	IBtxOp(3)	Lane 31 Tx+	Lane 15 Tx+
S11	IBtxOn(2)	Lane 30 Tx-	Lane 14 Tx-
S12	IBtxOp(2)	Lane 30 Tx+	Lane 14 Tx+
S13	IBtxOn(1)	Lane 29 Tx-	Lane 13 Tx-
S14	IBtxOp(1)	Lane 29 Tx+	Lane 13 Tx+
S15	IBtxOn(0)	Lane 28 Tx-	Lane 12 Tx-
S16	IBtxOp(0)	Lane 28 Tx+	Lane 12 Tx+

4.2.5 J44 - J45 SFP Connectors

There are two SFP connectors on the platform. Each SFP is connected as indicated in Table 39. The SFP+ connector is part number 1888247-1 from Tyco. The cage is part number 1489962-3 from Tyco. Signal assignment is based on the SFP+ (SFF-8431) Multi Source Agreement.

Figure 23: SFP Cage

Table 39: J44, J45 - SFP Connectors

Pin Number	SFF-8431 Signal Name	Function	J44	J45
1	VeeT	Transmitter Ground	GND	
2	TX Fault	Transmitter Fault Indication	Fault LED	
3	TX Disable	Transmitter Disable	GND (always enabled)	
4	SDA	2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i)	NC	NC

Table 39: J44, J45 - SFP Connectors ***(Continued)***

Pin Number	SFF-8431 Signal Name	Function	J44	J45
5	SCL1	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)	NC	NC
6	Mod ABS	Module Absent, connected to VeeT or VeeR in the module	NC	NC
7	RS0	Rate Select 0, optionally controls SFP+ module receiver	Pull-up with shunt jumper J35 to GND	Pull-up with shunt jumper J38 to GND
8	RX_LOS	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	LOS LED	
9	RS1	Rate Select 1, optionally controls SFP+ module transmitter	Pull-up with shunt J36 jumper to GND	Pull-up with shunt J37 jumper to GND
10	VeeR	Receiver Ground	GND	
11	VeeR	Receiver Ground	GND	
12	RD-	Inv. Received Data Out	RX8_p	RX10_p
13	RD+	Received Data Out	RX8_n	RX10_n
14	VeeR	Receiver Ground	GND	
15	VccR	Receiver Power	3.3V	
16	VccT	Transmitter Power	3.3V	
17	VeeT	Transmitter Ground	GND	
18	TD+	Transmit Data In	TX8_p	TX10_p
19	TD-	Inv. Transmit Data In	TX8_n	TX10_n
20	VeeT	Transmitter Ground	GND	

4.3 J23 - Optional 25-MHz Clock Input

The SMA connector at J23 can provide an external 25-MHz clock to the clock synthesizer. Use the REF_SEL setting on S9.3 to select the external source. The external clock source must be 3.3V LVTTL or LVCMOS levels.

4.4 J21, J22 - Clock Synthesizer LVDS Clock Outputs

Use J21 and J22 to monitor the output of the clock synthesizer connected to Tsi721's PCCLK. They are LVDS differential signals and are not AC coupled.

- J22 is output clock +
- J21 is output clock -

4.5 J1, J25 - ATX Power Connectors

Use a standard 20-pin ATX power supply to connect to J25.

Figure 24: J25 - ATX Power Connector Pinout

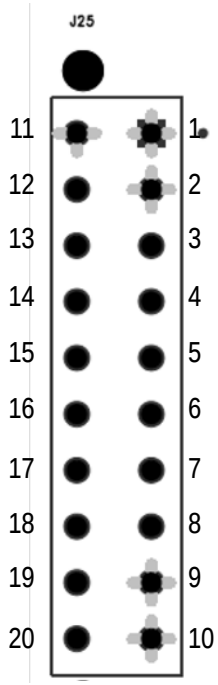


Table 40: J25 - ATX Power Connector Signal Description

Pin Number	Description	Pin Number	Description
1	3.3V (Not used	11	3.3V (Not used)
2	3.3V (Not used)	12	-12V (Not used)
3	GND	13	GND
4	5V	14	PS ON
5	GND	15	GND
6	5V (Not used)	16	GND
7	GND	17	GND

Table 40: J25 - ATX Power Connector Signal Description

Pin Number	Description	Pin Number	Description
8	POWER OK (Not used)	18	-5V (Not used)
9	5VSB	19	5V (Not used)
10	12V	20	5V (Not used)

Figure 25: J1 - Optional 12V ATX Supply

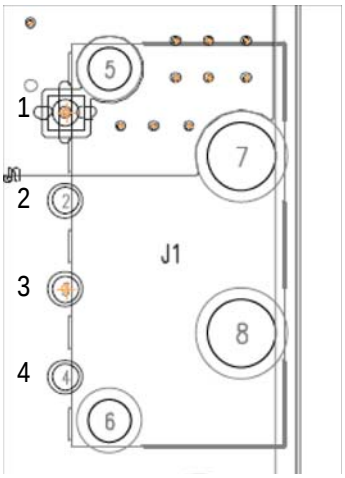


Table 41: J1 - Signal Description

Pin Number	Description
1	12V
2	GND
3	GND
4	5V (Not used)

4.6 J46, Switch JTAG Header

J46 is used to connect an external JTAG pod to the CPS-1432. J46 connects directly to the switch; it is not daisy-chained to other devices.

4.7 J48, Bridge JTAG Header

J48 is used to connect an external JTAG pod to the Tsi721. When an external JTAG pod is used, the USB cable (U1) must be disconnected; otherwise, there will be contention between the external pod and the on-board USB-JTAG controller.

Figure 26: J46, J48 - JTAG Header

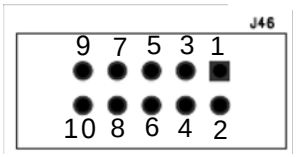


Table 42: J46, J48 - Signal Description

Pin Number	Description
1	TRST#
2	GND
3	TDI
4	GND
5	TDO
6	GND
7	TMS
8	GND
9	TCK
10	GND

4.8 J47 - I2C Header

J47 is used to connect the platform's I2C chain to an external I2C pod. When an external I2C pod is used, the USB cable (U1) must be disconnected; otherwise, there will be contention between the external pod and the on-board USB-I2C controller.

Figure 27: J47 - I2C Header

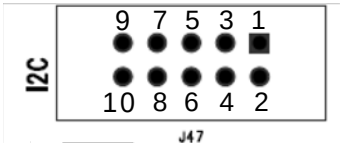


Table 43: J47 - Signal Description

Pin Number	Description
1	SCL
2	GND
3	SDA
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	GND

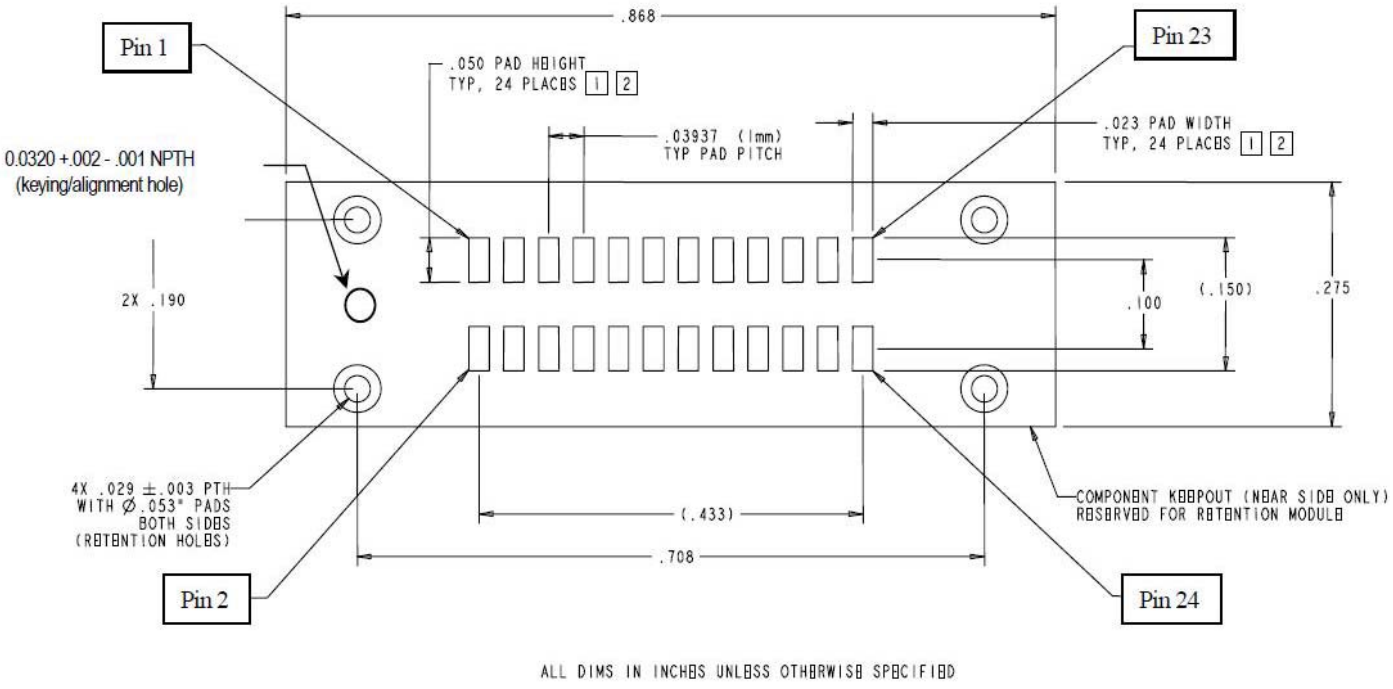
4.9 U1 - USB Connector

Use a standard USB type-B (mini) cable to connect a host PC to the on-board USB controller. The on-board USB controller uses power for the USB host (the PC). When the platform is powered off, the USB controller can still be detected by the host PC.

4.10 Logic Analyzer Pads

Most S-RIO lanes are connected to a logic analyzer pad. Use the board schematic to identify the location and the lanes on the logic analyzer pads. The footprint for the logic analyzer probe is compatible with Nexus Technology's Mid-bus Serial Probe.

Figure 28: Logic Analyzer Footprint



4.11 J54, J55 - Fan Power Connector

J54 and J55 are installed on the back of the platform. They are used to power the fans for the AMC module. The fans use 12V.

Table 44: J54, J55 - Signal Description

Pin Number	Description
1	12V
2	GND

5. PCB and Mechanical

This chapter describes the PCB and mechanical characteristics of the PCIe2 to S-RIO2 Evaluation Platform.

5.1 Board Stack-Up

The PCIe2 to S-RIO2 Evaluation Platform is built with FR4-08 material. The PCB is composed of ten layers, as displayed in Figure 29. Of the ten layers, four are used for routing signals, two are grounds, and four are power planes.

Figure 29: Board Stack-Up

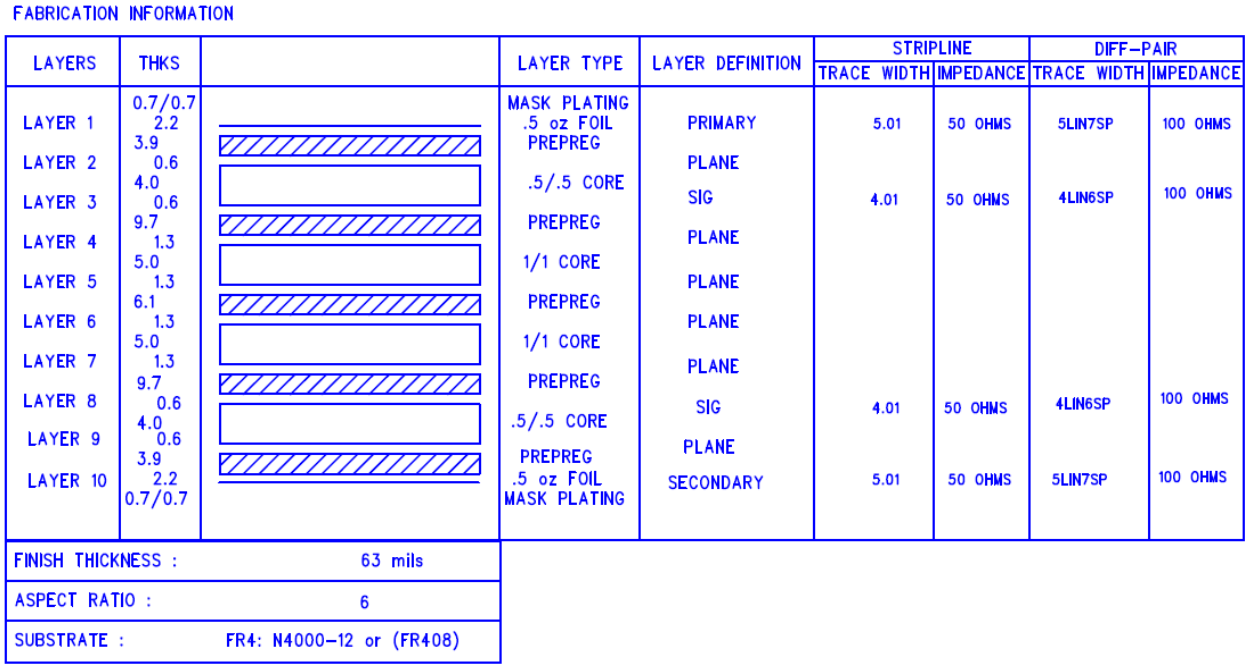


Table 45: Layer Assignment

Layer Number	Designation	Assignment
1	TOP	Most Components Differential Traces
2	GND1	Solid, continuous ground plane
3	SIG1	Differential Traces Low frequency signals
4	PWR1	Power, 1.0V, 2.5V, 12V
5	PWR2	Power, 1.0V and 3.3V

Table 45: Layer Assignment ***(Continued)***

Layer Number	Designation	Assignment
6	PWR3	Power, 1.2V, 12V
7	PWR4	Power, 3.3V, 1.5V
8	SIG2	Differential Traces Low frequency signals
9	GND2	Solid, continuous ground plane
10	BOTTOM	Decoupling and passive Differential Traces

5.2 Board Form Factor

The board form factor is based on a standard PCI Express plug-in card, but it has several exceptions:

- The board is taller than the specification
- The AMC connector exceeds the maximum width of a PCIe slot
- Back-mounted fans exceed the width of the back keepout of a PCIe plugin card

5.3 Thermal

AMC fans are mounted on the back of the board.The upper fan is above the standard PCI card plug-in area and should not hit adjacent cards. The lower fan will hit any adjacent card but can be removed if required.

Fan part# KDE1205PFV1 11.MS.A.GN SUNON FANs. The fans will turn on only when an AMC module is inserted.

5.3.1 CPS-1432 Thermal

The CPS-1432 maximum power draw is 6.2W. With no heatsink or airflow, the junction temperature may rise up to 90.5°C above ambient. The maximum junction temperature could be exceeded without the use of a heatsink.

Figure 30: Heatsink for CPS-1432

Malico HA25-21 with Talon clip
21 mm tall

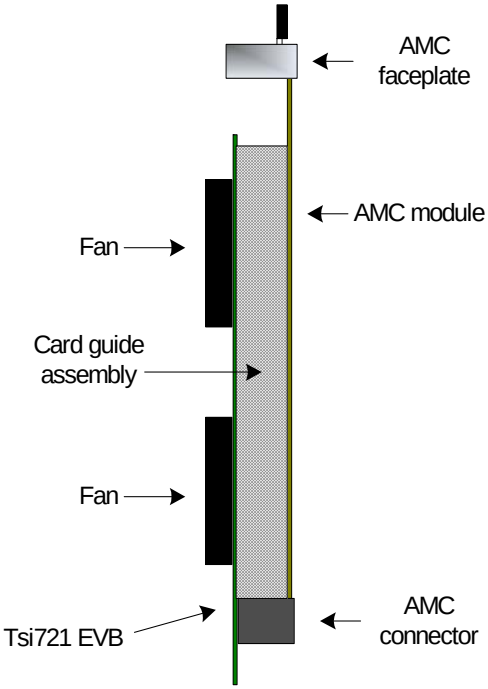
5.3.2 Tsi721 Thermal

At 2.5W typical power draw, the Tsi721's junction temperature is expected to rise to 30°C above ambient temperature with no air flow. For example, if the ambient temperature is 25°C, the junction temperature should not exceed 55°C. In a normal interior environment a heatsink is not required.

5.4 AMC Bay and Card Guide Assembly

The AMC bay provides card guides for proper support of the modules. AMC modules are inserted in the card guide upside-down. This implies that only mid-size modules can be used.

Figure 31: AMC Module Insertion Orientation



5.4.1 Top-Side Clearance

The maximum component height allowed on a standard PCIe card is 0.57" above the PCB. The tallest component on the board is the AMC connector at 0.9".

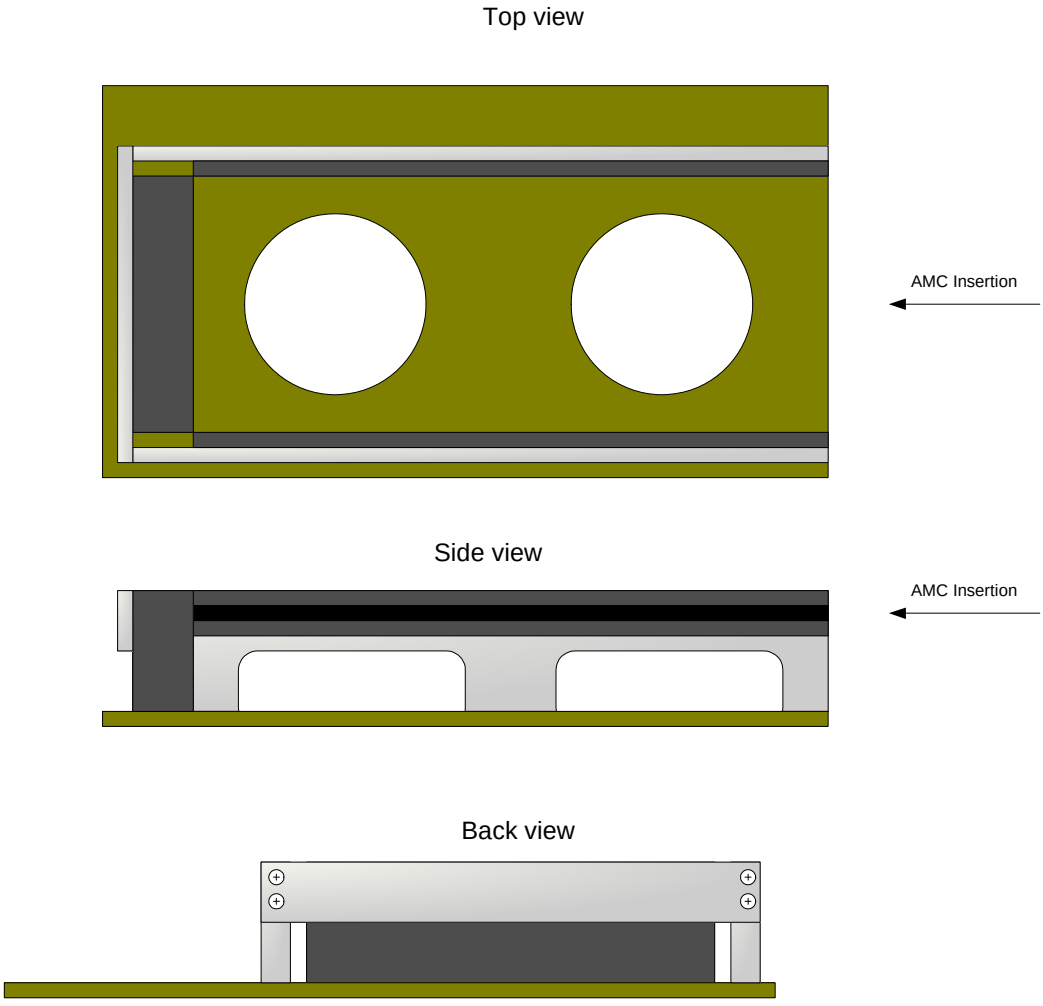
5.4.2 Bottom-Side Clearance

The bottom-side component maximum height on a standard PCIe card 0.105". This height will be exceeded by the fans (0.5") and the AMC connector back pin (0.135").

5.4.3 AMC Card Guide Assembly

The AMC card guide assembly is made with custom aluminium parts plastic card guides.The card guides and the AMC connector are attached with standard screws. All mechanical items and the AMC connector can be removed if required.

Figure 32: Card Guide Drawing



6. Recommended Cables

This chapter discusses the recommended cables to use with the PCIe2 to S-RIO2 Evaluation Platform.

6.1 CX4 Infiniband Cable Assemblies

Infiniband cables are offered in various length and signaling rate specification.

Single Data Rate (SDR) infiniband cables are specified for 2.5 Gbps signaling rate. They are suitable for the CPS-1432 switch at bit rates up to 6.25 Gbps, and in lengths up to 2 meters. Longer SDR cables (2–5 meters) may also be suitable for 5 and 6.25 Gbps bit rates with the CPS-1432. However, the switch's SerDes will likely require signal strength and post/pre-emphasis adjustments.

Double Data Rate (DDR) infiniband cables are specified for 5 Gbps signaling rate. They are better suited for bit rates higher than 3.125Gbps and length longer than 2 meters.

Table 46: Infiniband Cable Vendors

Vendor	Product Description	Part Number
FCI	EyeMax Infiniband 4x cable assembly, 1 meter	10007290-N0100CULF
Molex	LaneLink Infiniband 4x cable assembly, 1 meter	74506-3002
Amphenol	4X SDR InfiniBand cable with Fujitsu InfiniBand connectors (SFF-8470 Latch), 1 meter	NW-28INFINI4X-001 (www.cablesondemand.com)

6.2 SFP+ Passive (Unequalized) Cables

SFP+ cables are typically specified for 10 Gbps and faster signal rates. SFP+ cables of various length are suitable for the CPS-1432 switch.

Table 47: SFP Cable Vendors

Vendor	Product Description	Part Number
FCI	SFP+ cable assembly, 32 AWG, 1 meter, passive	10110818-1010LF
3M	Cable assemblies for SFP+ applications, 1410 series, 1 meter	1410-P-15-00-1.00
Molex	SFP+ passive cable assembly, 10 Gbps, 28 AWG cable, Pull-to-release plunger style latch, 1 meter	74752-2101
Tyco	Cable assembly sub-type; SFP+, 1 meter	2127934-2
Amphenol	SFP+ cable - amphenol 10 GbE SFP+ Direct attach copper cable, 1 meter	SFPP2EPASS-001

6.3 SMA Cables

SMA cables are made of SMA type connectors and a 50 Ohm coaxial cable. Cable assemblies are available in various length and RF characteristics. When selecting a coaxial cable, consider the insertion loss of the cable at 3.125 GHz (for bit rates of 6.25 Gbps). Use cables that have total insertion loss of less than 10dB. Use cables that are length matched (±3 mm or better) within a differential pair. Length matching is not required, however, between lanes of the same port.

Table 48: SMA Cable Vendors

Vendor	Website
Lighthorse	www.rfconnector.com
Rosenberger	www.rosenbergerna.com
Amphenol Connex	www.amphenolconnex.com
Samtec	www.samtec.com

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