



IDT™ 89EBPES32H8 Evaluation Board Manual

(Eval Board: 18-625-000)

February 2007

6024 Silver Creek Valley Road, San Jose, California 95138
Telephone: (800) 345-7015 • (408) 284-8200 • FAX: (408) 284-2775
Printed in U.S.A.
©2007 Integrated Device Technology, Inc.

DISCLAIMER

Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

Boards that fail to function should be returned to IDT for replacement. Credit will not be given for the failed boards nor will a Failure Analysis be performed.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

IDT, the IDT logo, and Integrated Device Technology are trademarks or registered trademarks of Integrated Device Technology, Inc.



Notes

Description of the EB32H8 Eval Board

Introduction 1-1
 Board Features 1-2
 Feature List 1-2
 Performance Summary 1-2
 Software 1-3
 Other 1-3
 Revision History 1-3

Installation of the EB32H8 Eval Board

EB32H8 Installation 2-1
 PCI Express Adapter Card 2-1
 Hardware Description 2-2
 Host System 2-2
 Reference Clocks 2-3
 Power Sources 2-6
 PCI Express Serial Data Transmit Termination Voltage Converter 2-7
 PCI Express Digital Power Voltage Converter 2-7
 PCI Express Analog Power Voltage Converter 2-7
 Core Logic Voltage Converter 2-7
 3.3V I/O Power Module 2-8
 Power-up Sequence 2-8
 Required Jumpers 2-8
 Heatsink Requirement 2-8
 Reset 2-8
 Fundamental Reset 2-8
 Downstream Reset 2-8
 Boot Configuration Vector 2-9
 SMBus Interfaces 2-11
 SMBus Slave Interface 2-11
 SMBus Master Interface 2-12
 JTAG Header 2-13
 Attention Buttons 2-13
 Miscellaneous Jumpers, Headers 2-13
 LEDs 2-15
 PCI Express Connectors 2-16
 PCI Express Personality Module 2-19
 EB32H8 Evaluation Board Block Diagram 2-20

Software for the EB32H8 Eval Board

Introduction 3-1
 Device Management Software 3-1

Schematics

Schematics 4-1

Notes



Notes

Table 2.1 Clock Source Selection 2-3

Table 2.2 Clock Frequency Selection 2-4

Table 2.3 Clock Spread Spectrum Selection 2-4

Table 2.4 SMA Connectors - Onboard Reference Clock 2-4

Table 2.5 EPS12V 24_pin Power Connector - J2 2-7

Table 2.6 EPS12V 8-Pin Connector - J1 2-7

Table 2.7 Downstream Reset Selection 2-9

Table 2.8 Boot Configuration Vector Signals 2-9

Table 2.9 Boot Configuration Vector Switches S3 & S12 (ON=0, OFF=1) 2-10

Table 2.10 Slave SMBus Interface Connector 2-11

Table 2.11 SMBus Slave Interface Address Configuration 2-11

Table 2.12 PES32H8 SMBus Slave Interface Address Setting 2-12

Table 2.13 EEPROM SMBus Address Setting 2-12

Table 2.14 JTAG Connector Pin Out 2-13

Table 2.15 Attention Buttons 2-13

Table 2.16 Miscellaneous Jumpers, Headers 2-13

Table 2.17 LED Indicators 2-15

Table 2.18 PCI Express x16 Connector Pinout 2-16

Table 2.19 PES32H8 Personality Module Locations 2-19

Notes



List of Figures

Notes

Figure 1.1	Function Block Diagram of the EB32H8 Eval Board	1-1
Figure 2.1	PCIe Adapter	2-1
Figure 2.2	SuperMicro X6DH8-G2 Motherboard	2-3
Figure 2.3	Clock Distribution Block Diagram	2-5
Figure 2.4	Power Distribution Block Diagram	2-6
Figure 2.5	EB32H8 Eval Board Block Diagram	2-20

Notes



Description of the EB32H8 Eval Board

Notes

Introduction

The 89HPES32H8 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES32H8 is a 32-lane, 8-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high-performance applications where multiple peer-to-peer traffic flows are simultaneously transmitted.

The 89EBPES32H8 Evaluation Board (also referred to as EB32H8 in this manual) provides an evaluation platform for the PES32H8 switch. The EB32H8 has two x4 ports which can be merged to provide one x8 upstream port on a standard x16 PCI Express connector. This port is used to connect an adaptor card with a cable to another adaptor card in the root complex or host system. Alternatively, the upstream port can be configured as a x4 port allowing for seven downstream ports.

The downstream slots conform to the x8 and x4 connector pin assignments but are populated with x16 connectors. The unused lane bits on the x16 connectors are unconnected. The core and IO power for the PES32H8 PCI Express Switch (PES32H8) is derived from the 12V power supply connector from a 12VEPS type power supply with a 24-pin connector and a 8-pin connector with 12V. The downstream slot power is controlled through hot-plug controllers with power provided from the 12VEPS power supply connector with 12V. A personality module is used to optionally merge two x4 ports into one x8 downstream port connector. The PES32H8 Evaluation board block diagram is shown in Figure 1.1.

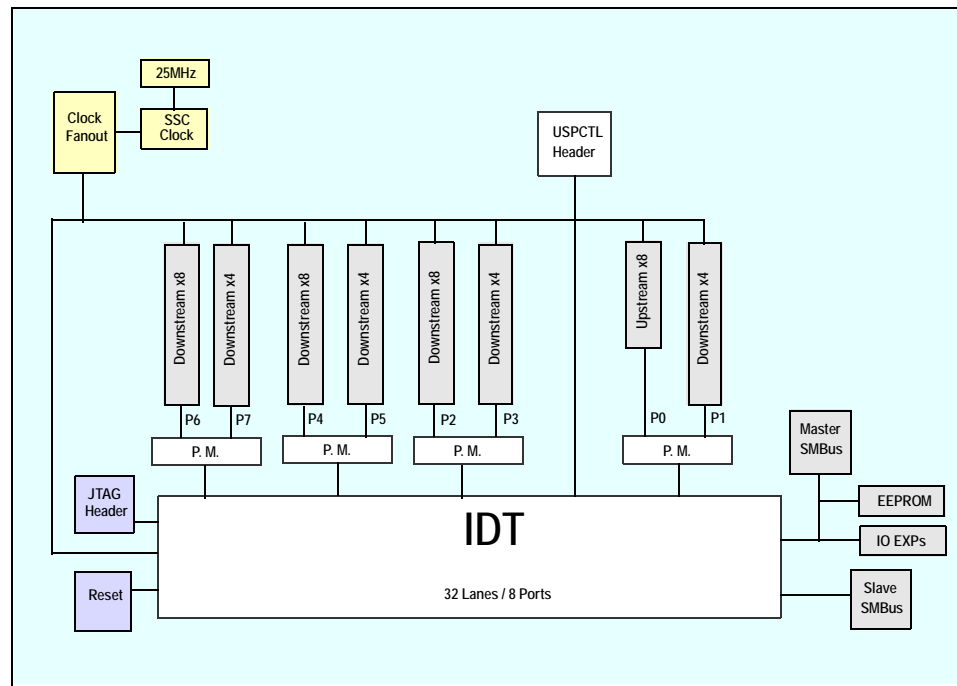


Figure 1.1 Function Block Diagram of the EB32H8 Eval Board

Notes

Board Features

Feature List

- ◆ The EB32H8 has one x8 (or x4) PCI Express upstream port to the root complex provided by a PCI Express adaptor board to a cable that connects to another adaptor board in the root complex or host system.
- ◆ The EB32H8 provides seven downstream connectors with x4 ports. Two x4 downstream slots can be configured as one x8 port through the personality modules.
- ◆ All seven downstream slots have hot-plug support through power isolation controlled by a hot-plug controller and IO expanders on the Master SMBUS. The Master SMBUS is controlled by the PES32H8 through configuration registers.
- ◆ The EB32H8 has a 12V to 2.5V DC-DC converter that uses the 12V power from an external 12VEPS power supply connector with 12V. The 2.5V provides power to the DC-DC converters for the PES32H8 core power.
- ◆ JTAG connector to the PES32H8 JTAG pins.
- ◆ Serial EEPROM on the PES32H8 master SMBUS interface.
- ◆ Provides an SMBUS connector on the PES32H8 slave SMBUS interface.
- ◆ Has a fundamental cold and warm reset mechanism and a reset push button switch.
- ◆ Provides a clock reference to the seven downstream ports from the upstream clock reference or from an on-board clock generator. The clock generator has spread spectrum clocking option and SMA connectors are provided to monitor the clock.
- ◆ Has LED displays to indicate power is applied, reset condition, port status, and downstream slot power.
- ◆ Has card present detect pins implemented on upstream and downstream slots.
- ◆ Has ATTN push button switches and LED displays for each downstream slot.
- ◆ Has a +12V fan connector for the integrated heatsink for the socket and soldered device.

Performance Summary

- ◆ Provides up to 8-ports with 32 PCIe lanes
- ◆ Integrated SerDes support 2.5 Gbps operation
- ◆ Delivers up to 16 GBps (128 Gbps) of aggregate bandwidth
- ◆ Sub 280ns latency through the switch
- ◆ Supports two virtual channels
- ◆ Compliant with PCI Express Base Specification Rev1.1
- ◆ Flexible Architecture with Numerous Configuration Options
- ◆ Four x8 PCIe ports
- ◆ Each port can be independently bifurcated into two x4 PCIe ports
- ◆ Supports automatic per port link width negotiation(e.g., x8/x4/x2/x1 for a x8 port)
- ◆ Automatic lane reversal detection
- ◆ Independent per port crosslink support
- ◆ Supports lock transactions, allowing use of PCI Express with legacy software
- ◆ Ability to load device configuration from serial EEPROM
- ◆ Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems
- ◆ Supports external signal for power management event notification

Notes

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES32H8 within host systems running popular operating systems.

- ◆ Installation programs
 - Operating Systems Supported: Windows2000, WindowsXP, Linux
- ◆ GUI based application for Windows and Linux
 - Allows users to view and modify registers in the PES32H8
 - Binary file generator for programming the serial EEPROMs attached to the SMBUS

Other

An external power supply may be required under some conditions.

An SMBUS cable may be required for certain evaluation exercises.

SMA connectors are provided on the EB32H8 board for specific test points.

Revision History

February 5, 2007: Published production release board revision 0.9.

Notes



Installation of the EB32H8 Eval Board

Notes

EB32H8 Installation

This chapter discusses the steps required to configure and install the EB32H8 evaluation board. All available DIP switches and jumper configurations are explained in detail. The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Connect a PCI Express adapter card in an upstream port with a cable to another PCI Express adaptor card in the root complex or host system, as shown in Figure 2.1.
4. Turn the power switch on the eval board (located at S13) to ON.
5. Apply power to the host system.

The EB32H8 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

PCI Express Adapter Card

The PCI Express adapter card contains eight PCI Express lanes (see Figure 2.1). The lower four lanes are routed to an Infiniband connector J2 and the upper four lanes to J3. The differential REFCLKp and REFCLKn pins are routed to J5 and J6, respectively. The JTAG interface and PERST# pins are routed to J4 although only PERST# pin is actually used. Two PCI Express Adapter cards are required to connect the EB32H8 evaluation board to the host PC and remember to match the connector connection between two cards.

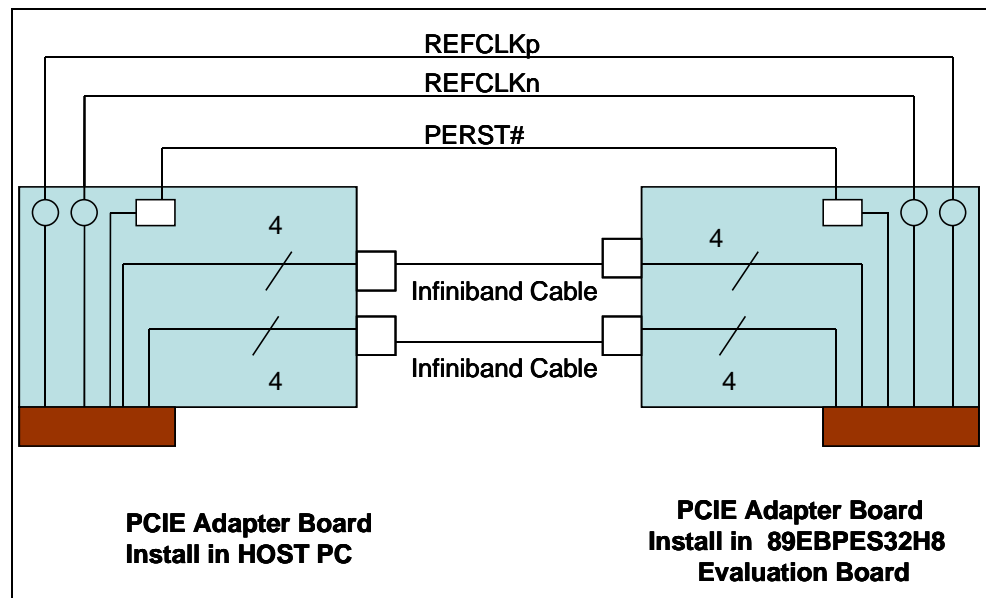


Figure 2.1 PCIe Adapter

Notes

Hardware Description

The PES32H8 is a 32-lane, 8-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 7 downstream ports or peer-to-peer switching between downstream ports.

The EB32H8 has 7 PCI Express downstream ports, accessible through seven x16 connectors. Three specific ports are capable of negotiating a x1, x2, x4, or x8 link width and all seven ports are capable of negotiating a x1, x2, x4 link width. All endpoint cards connected to the PES32H8 must support at least one of these link widths. A personality module can be used to provide a single x8 downstream port by merging two specific x4 ports (see section PCI Express Personality Module on page 2-19).

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot. (If your host system does not offer a x8 slot, please contact ssdhelp@idt.com for alternative solutions.)
- x1, x2, x4, or x8 PCI Express Endpoint Cards.

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x8 configuration through a PCI Express x8 slot is required to take full advantage of the PES32H8's capabilities. One such system is the SuperMicro X6DH8-G2 motherboard equipped with an Intel E7520 chipset which was introduced in 2004 to deploy dual-processor server chipset technology. The board has three PCI Express slots. All slots have x8 connectors, but only two are electronically connected for a x8 link width (J15 and J16). The remaining slots are electronically connected for a x4 link width configuration. Care must be taken to avoid using the EB32H8 in the x4 slot (J17). Figure 2.2 shows the proper connectors.

Notes

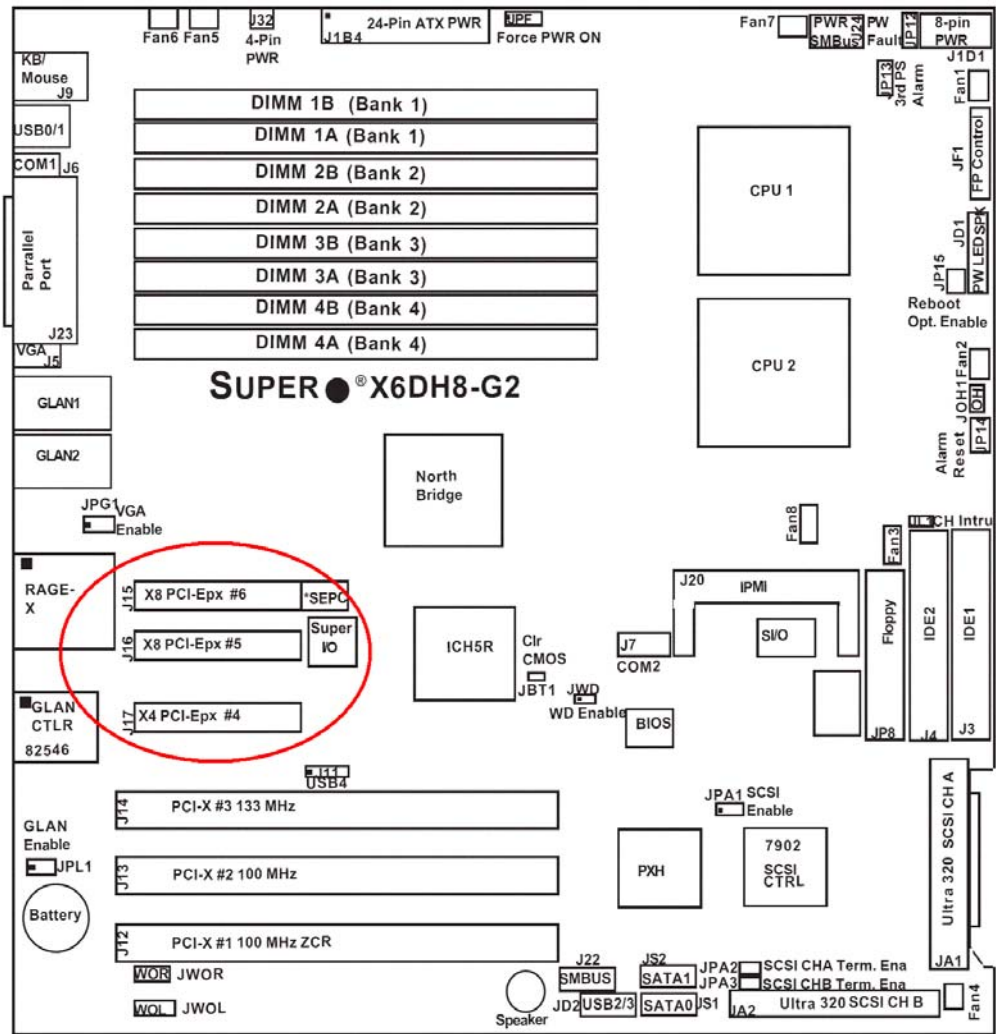


Figure 2.2 SuperMicro X6DH8-G2 Motherboard

Reference Clocks

The PES32H8 requires four differential reference clocks. The EB32H8 derives these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
Install	Clock Source
R36, R37	Onboard Reference Clock – Use onboard clock generator
R35, R148	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS9FG104 clock generator device (U14) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB32H8 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S2[4:2]			
S2[4]	S2[3]	S2[2]	Clock Frequency
ON	ON	ON	100 MHz (Default)
ON	ON	OFF	125 MHz

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[1]	
S2[1]	Spread
ON	No Spread (Default)
OFF	Spread Enable

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock must be used instead.

The output of the two onboard clock generator is accessible through four SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J5, J3, J15, J8	
J5, J15	Positive Reference Clock
J3, J8	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Figure 2.3 illustrates the clock distribution block diagram for the EB32H8 evaluation board.

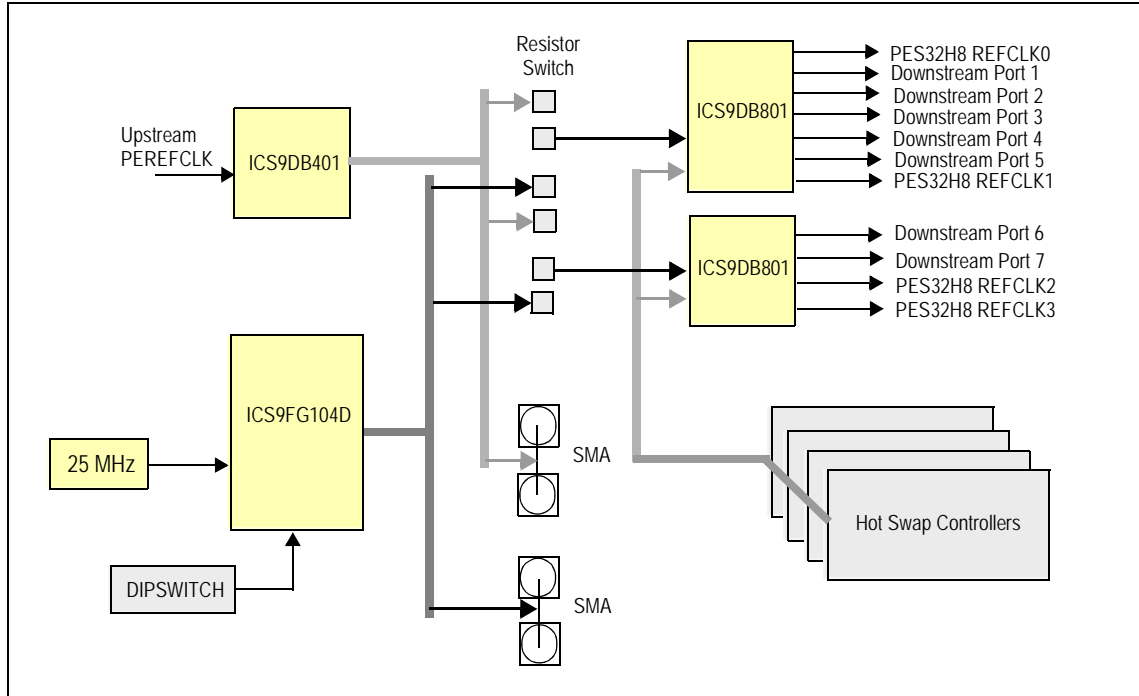


Figure 2.3 Clock Distribution Block Diagram

Power Sources

Power for the PES32H8 and all downstream ports is generated from the 12V from an external power connector. See Figure 2.4. A 12V to 2.5V DC-DC converter is used to provide power to four LDO linear regulators to generate V_{DDCORE} , V_{DDPE} , V_{DDAPE} , and V_{TTPE} voltages. The 3.3V from the DC-DC converter is used to power the clock buffers and V_{DDIO} .

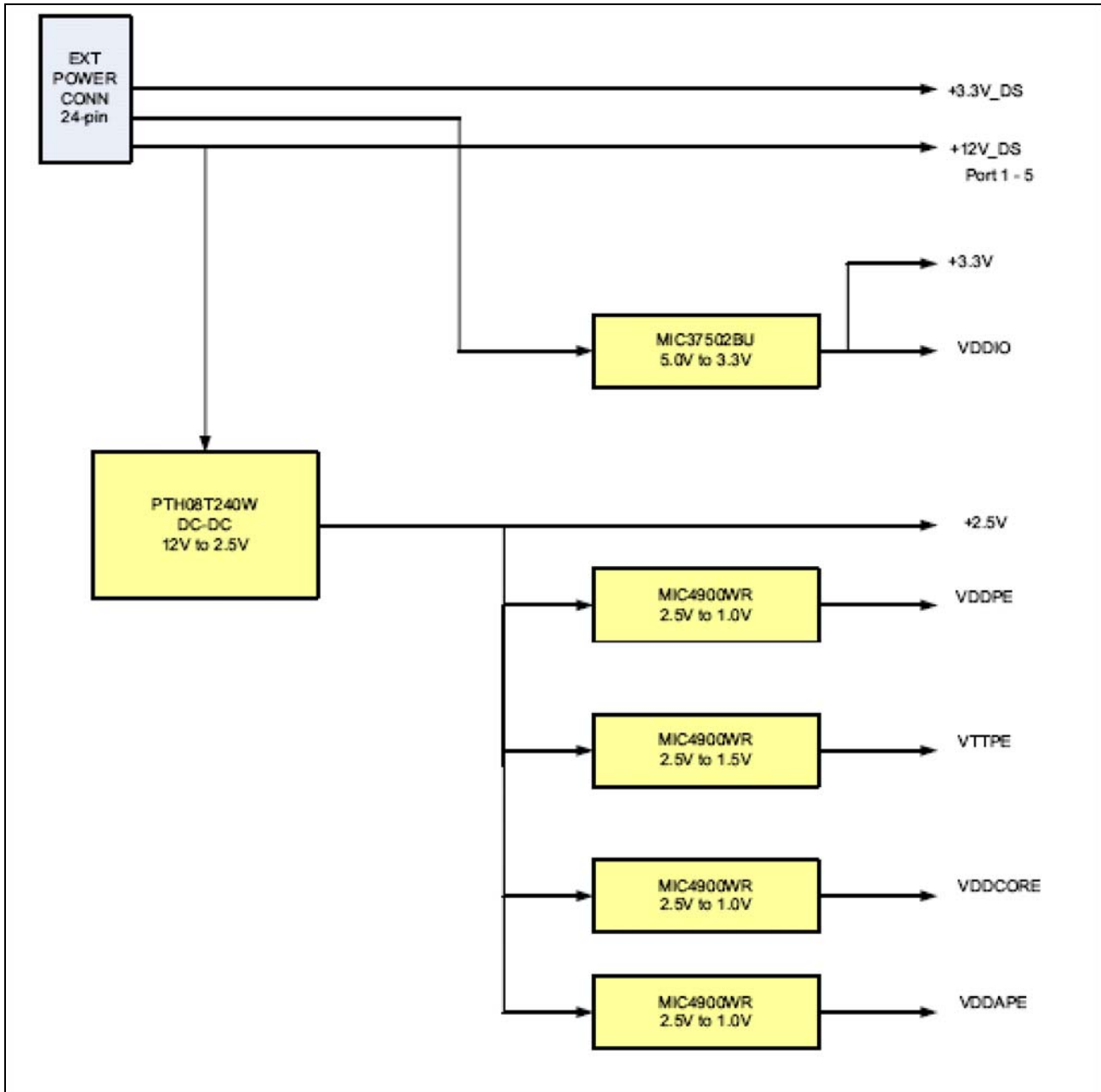


Figure 2.4 Power Distribution Block Diagram

Notes

The external power supply connectors are a 24-pin (J2) and an 8-pin (J1) molex connector as described in Table 2.5 and Table 2.6. The +12V3 is used to power PES32H8 and downstream ports 1 through 3. The +12V1 is used to power downstream ports 4 and 5. The +12V2 is used to power downstream ports 6 and 7.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.5 EPS12V 24_pin Power Connector - J2

Pin	Signal	Pin	Signal
1	GND	5	+12V1
2	GND	6	+12V1
3	GND	7	+12V2
4	GND	8	+12V2

Table 2.6 EPS12V 8-Pin Connector - J1

The power on switch located at S13 can be used to control the supply power from the external power supply connector. Add a shunt to W19 to enable power on switch.

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U5) provides a 1.5V PCI Express serial data transmit termination voltage (VTT) to the PES32H8.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES32H8.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U28) provides a 1.0V PCI Express analog power voltage (VDDAPE) to the PES32H8.

Core Logic Voltage Converter

A separate DC-DC converter (U3) provides the 1.0V core voltage (VDDCORE) to the PES32H8.

Notes

3.3V I/O Power Module

A separate DC-DC converter (U17) provides the 3.3V I/O voltage (VDDIO) to the PES32H8.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements.

Required Jumpers

To deliver power to the PES32H8 switch, the following jumpers must be shunted: W88, W91, W92, W93, W94. These jumpers were implemented so that the power consumption of the PES32H8 can be measured.

Heatsink Requirement

TBD

Reset

The PES32H8 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES32H8, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES32H8 User Manual. The EB32H8 evaluation board provides seamless support for Hot Reset.

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB32H8 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES32H8.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
 - Pressing a push-button switch (S1) located on EB32H8 board
 - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB32H8. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 (default) to pin 2-3 on W1.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES32H8 while power is on.

Downstream Reset

The PES32H8 provides a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.7.

Notes

Port #	Jumper	Selection
1	W45	[1-2] Software controlled reset through GPIO6 [2-3] Fundamental reset PERST# (default)
2	W47	[1-2] Software controlled reset through GPIO7 [2-3] Fundamental reset PERST# (default)
3	W74	[1-2] Software controlled reset through GPIO8 [2-3] Fundamental reset PERST# (default)
4	W86	[1-2] Software controlled reset through GPIO9 [2-3] Fundamental reset PERST# (default)
5	W85	[1-2] Software controlled reset through GPIO10 [2-3] Fundamental reset PERST# (default)
6	W54	[1-2] Software controlled reset through GPIO11 [2-3] Fundamental reset PERST# (default)
7	W84	[1-2] Software controlled reset through GPIO12 [2-3] Fundamental reset PERST# (default)

Table 2.7 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.8 is sampled by the PES32H8 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S3 and S12 as defined in Table 2.9.

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that a common clock is being used between the downstream device and the downstream port. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. Default: 0x0
P01MERGEN	Port 0 and 1 Merge: When this pin is asserted (i.e. low), port 1 is merged with port 0 to form a single x8 port. Default: 0x1
P23MERGEN	Port 2 and 3 Merge: When this pin is asserted (i.e. low), port 2 is merged with port 3 to form a single x8 port. Default: 0x1
P45MERGEN	Port 4 and 5 Merge: When this pin is asserted (i.e. low), port 4 is merged with port 5 to form a single x8 port. Default: 0x1
P67MERGEN	Port 6 and 7 Merge: When this pin is asserted (i.e. low), port 6 is merged with port 7 to form a single x8 port. Default: 0x1

Table 2.8 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES32H8 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0
SWMODE[3:0]	Switch Mode. These configuration pins determine the PES32H8 switch operating mode. Default: 0x1 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x7 - Reserved 0x8 - Normal switch mode with upstream port failover (port 0 selected as the upstream port) 0x9 - Normal switch mode with upstream port failover (port 2 selected as the upstream port) 0xA - Normal switch mode with Serial EEPROM and upstream port failover (port 0 selected as the upstream port) 0xB - Normal switch mode with Serial EEPROM and upstream port failover (port 2 selected as the upstream port) 0xC through 0xF - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[4:1]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.8 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S12[1]	CCLKDS	OFF
S12[2]	CCLKUS	OFF
S12[3]	MSMBSMODE	ON
S12[4]	P01MERGEN	ON
S12[5]	P23MERGEN	OFF
S12[6]	P45MERGEN	OFF
S12[7]	P67MERGEN	OFF
S12[8]	RSTHALT	ON
S3[1]	SWMODE[0]	ON
S3[2]	SWMODE[1]	ON
S3[3]	SWMODE[2]	ON
S3[4]	SWMODE[3]	ON
S3[5]	REFCLKM	ON
S3[6]	MSMBADDR[0]	ON
S3[7]	MSMBADDR[1]	ON
S3[8]	MSMBADDR[2]	ON

Table 2.9 Boot Configuration Vector Switches S3 & S12 (ON=0, OFF=1)

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I²C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES32H8 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the EB32H8 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.10.

Slave SMBus Interface Connector J7	
Pin	Signal
1	N/C
2	SSMBCLK
3	GND
4	SSMBDATA

Table 2.10 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES32H8 slave interface is **0b1110111** by default and is configurable using jumpers W37, W38, W39, and W41 as described in Tables 2.11 and 2.12.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.11 SMBus Slave Interface Address Configuration

Notes

SMBUS Slave Interface Address Setting				
W37 SSMBADDR[5]	W38 SSMBADDR[3]	W39 SSMBADDR[2]	W41 SSMBADDR[1]	Slave Interface Bus Address
OFF	OFF	OFF	OFF	0b1110111 (Default)
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.12 PES32H8 SMBus Slave Interface Address Setting

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are 7 16-bit I/O Expanders (Maxim MAX7311) and a serial EEPROM (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through I/O Expander 10 are fixed through the stuffing resistor as 0x0, 0x1, 0x2, 0x3, 0x8, 0x9 and 0xA, respectively.

The bus address for the selected EEPROM device is **0b1010_000** by default and is configurable using W12 and the switch S3 as described in Table 2.13.

W12	S3[8]	S3[7]	S3[6]	Bus Address
ON	ON	ON	ON	0b1010_000 (Default)

Table 2.13 EEPROM SMBus Address Setting

Notes

JTAG Header

The PES32H8 provides a JTAG connector J9 for access to the PES32H8 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.14 for the JTAG Connector J9 pin out.

JTAG Connector J9					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.14 JTAG Connector Pin Out

Attention Buttons

The PES32H8 features seven attention buttons, shown in Table 2.15. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S7	Port 1 Attention Button
S8	Port 2 Attention Button
S9	Port 3 Attention Button
S10	Port 4 Attention Button
S4	Port 5 Attention Button
S5	Port 6 Attention Button
S6	Port 7 Attention Button

Table 2.15 Attention Buttons

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W14, W48 through W51	Header	Shunted	Bypass hot-plug controller - Enable REFCLK to downstream ports (Default)
W36	Header	Shunted	Disable EEPROM Write protect feature (Default)
W19 / S13	Header	Open	Enable Power On Switch (Default)

Table 2.16 Miscellaneous Jumpers, Headers (Part 1 of 3)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W2	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 1 (Default)
W4	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 2 (Default)
W13	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 3 (Default)
W67	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 4 (Default)
W68	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 5 (Default)
W3	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 6 (Default)
W11	Header	Shunted	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 7 (Default)
W16	Header	2-3 Shunted	2-3: Port 1, 3.3Vaux source from External Power (Default) 1-2: Port 1, 3.3Vaux source from hot-plug controller
W89	Header	2-3 Shunted	2-3: Port 2, 3.3Vaux source from External Power (Default) 1-2: Port 2, 3.3Vaux source from hot-plug controller
W90	Header	2-3 Shunted	2-3: Port 3, 3.3Vaux source from External Power (Default) 1-2: Port 3, 3.3Vaux source from hot-plug controller
W69	Header	2-3 Shunted	2-3: Port 4, 3.3Vaux source from External Power (Default) 1-2: Port 4, 3.3Vaux source from hot-plug controller
W70	Header	2-3 Shunted	2-3: Port 5, 3.3Vaux source from External Power (Default) 1-2: Port 5, 3.3Vaux source from hot-plug controller
W46	Header	2-3 Shunted	2-3: Port 6, 3.3Vaux source from External Power (Default) 1-2: Port 6, 3.3Vaux source from hot-plug controller
W60	Header	2-3 Shunted	2-3: Port 7, 3.3Vaux source from External Power (Default) 1-2: Port 7, 3.3Vaux source from hot-plug controller
W34	Header	2-3 Shunted	2-3: Port 1, +12V source from External Power (Default) 1-2: Port 1, +12V source from hot-plug controller
W83	Header	2-3 Shunted	2-3: Port 2, +12V source from External Power (Default) 1-2: Port 2, +12V source from hot-plug controller
W72	Header	2-3 Shunted	2-3: Port 3, +12V source from External Power (Default) 1-2: Port 3, +12V source from hot-plug controller
W81	Header	2-3 Shunted	2-3: Port 4, +12V source from External Power (Default) 1-2: Port 4, +12V source from hot-plug controller
W79	Header	2-3 Shunted	2-3: Port 5, +12V source from External Power (Default) 1-2: Port 5, +12V source from hot-plug controller
W75	Header	2-3 Shunted	2-3: Port 6, +12V source from External Power (Default) 1-2: Port 6, +12V source from hot-plug controller
W77	Header	2-3 Shunted	2-3: Port 7, +12V source from External Power (Default) 1-2: Port 7, +12V source from hot-plug controller

Table 2.16 Miscellaneous Jumpers, Headers (Part 2 of 3)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W40	Header	2-3 Shunted	2-3: Port 1, +3.3V source from External Power (Default) 1-2: Port 1, +3.3V source from hot-plug controller
W71	Header	2-3 Shunted	2-3: Port 2, +3.3V source from External Power (Default) 1-2: Port 2, +3.3V source from hot-plug controller
W73	Header	2-3 Shunted	2-3: Port 3, +3.3V source from External Power (Default) 1-2: Port 3, +3.3V source from hot-plug controller
W82	Header	2-3 Shunted	2-3: Port 4, +3.3V source from External Power (Default) 1-2: Port 4, +3.3V source from hot-plug controller
W80	Header	2-3 Shunted	2-3: Port 5, +3.3V source from External Power (Default) 1-2: Port 5, +3.3V source from hot-plug controller
W76	Header	2-3 Shunted	2-3: Port 6, +3.3V source from External Power (Default) 1-2: Port 6, +3.3V source from hot-plug controller
W78	Header	2-3 Shunted	2-3: Port 7, +3.3V source from External Power (Default) 1-2: Port 7, +3.3V source from hot-plug controller

Table 2.16 Miscellaneous Jumpers, Headers (Part 3 of 3)

LEDs

There are several LED indicators on the EB32H8 which convey status feedback. A description of each is provided in Table 2.17.

Location	Color	Definition
DS19	Green	Port1: Power-is-good indicator
DS41	Green	Port2: Power-is-good indicator
DS18	Green	Port3: Power-is-good indicator
DS74	Green	Port4: Power-is-good indicator
DS73	Green	Port5: Power-is-good indicator
DS27	Green	Port6: Power-is-good indicator
DS17	Green	Port7: Power-is-good indicator
DS9	Yellow	Port1: Attention Indicator
DS4	Yellow	Port2: Attention Indicator
DS5	Yellow	Port3: Attention Indicator
DS6	Yellow	Port4: Attention Indicator
DS7	Yellow	Port5: Attention Indicator
DS8	Yellow	Port6: Attention Indicator
DS11	Yellow	Port7: Attention Indicator
DS10	Green	Port1: Power Indicator
DS20	Green	Port2: Power Indicator

Table 2.17 LED Indicators (Part 1 of 2)

Notes

Location	Color	Definition
DS21	Green	Port3: Power Indicator
DS22	Green	Port4: Power Indicator
DS23	Green	Port5: Power Indicator
DS24	Green	Port6: Power Indicator
DS25	Green	Port7: Power Indicator
DS3	Green	Port0: Active Status Output
DS50	Green	Port1: Active Status Output
DS51	Green	Port2: Active Status Output
DS52	Green	Port3: Active Status Output
DS53	Green	Port4: Active Status Output
DS54	Green	Port5: Active Status Output
DS55	Green	Port6: Active Status Output
DS56	Green	Port7: Active Status Output
DS42	Green	Port0: Link Up Status Output
DS43	Green	Port1: Link Up Status Output
DS44	Green	Port2: Link Up Status Output
DS45	Green	Port3: Link Up Status Output
DS46	Green	Port4: Link Up Status Output
DS34	Green	Port5: Link Up Status Output
DS35	Green	Port6: Link Up Status Output
DS36	Green	Port7: Link Up Status Output
DS15	Red	Hot Plug Controller1: Power Fault Indicator
DS65	Red	Hot Plug Controller2: Power Fault Indicator
DS14	Red	Hot Plug Controller3: Power Fault Indicator
DS13	Red	Hot Plug Controller4: Power Fault Indicator
DS2	Green	Board Power Indicator (3.3V)
DS1	Red	Board Reset Indicator

Table 2.17 LED Indicators (Part 2 of 2)

PCI Express Connectors

Pin	Side A		Side B	
	1	+12V	12V power	PRSNT1#
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground

Table 2.18 PCI Express x16 Connector Pinout (Part 1 of 4)

Notes

Pin	Side A		Side B	
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential

Table 2.18 PCI Express x16 Connector Pinout (Part 2 of 4)

Notes

Pin	Side A		Side B	
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground
50	PETp8	Transmitter differential	RSVD	Reserved
51	PETn8	pair, Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential
53	GND	Ground	PERn8	pair, Lane 8
54	PETp9	Transmitter differential	GND	Ground
55	PETn9	pair, Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential
57	GND	Ground	PERn9	pair, Lane 9
58	PETp10	Transmitter differential	GND	Ground
59	PETn10	pair, Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential
61	GND	Ground	PERn10	pair, Lane 10
62	PETp11	Transmitter differential	GND	Ground
63	PETn11	pair, Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential
65	GND	Ground	PERn11	pair, Lane 11
66	PETp12	Transmitter differential	GND	Ground
67	PETn12	pair, Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential
69	GND	Ground	PERn12	pair, Lane 12
70	PETp13	Transmitter differential	GND	Ground
71	PETn13	pair, Lane 13	GND	Ground
72	GND	Ground	PERp13	Receiver differential
73	GND	Ground	PERn13	pair, Lane 13
74	PETp14	Transmitter differential	GND	Ground
75	PETn14	pair, Lane 14	GND	Ground
76	GND	Ground	PERp14	Receiver differential

Table 2.18 PCI Express x16 Connector Pinout (Part 3 of 4)

Notes

Pin	Side A		Side B	
77	GND	Ground	PERn14	pair, Lane 14
78	PETp15	Transmitter differential	GND	Ground
79	PETn15	pair, Lane 15	GND	Ground
80	GND	Ground	PERp15	Receiver differential
81	PRSNT2#	Hot-Plug presence detect	PERn15	pair, Lane 15
82	RSVD	Reserved	GND	Ground

Table 2.18 PCI Express x16 Connector Pinout (Part 4 of 4)

Note: These x16 PCI Express connectors comply with the PCIe specification. However, the downstream ports on the EB32H8 are electronically connected in either a x8 configuration (ports 2, 4, 6) or a x4 configuration (ports 1 through 7).

PCI Express Personality Module

The PES32H8 supports port merging in a static manner during a fundamental reset. A PCI Express personality module is used in the EB32H8 to merge two consecutive x4 even and odd ports into a single x8 port, e.g., ports 0 and 1, ports 2 and 3, etc., finishing with ports 6 and 7. When side 1 of the personality module is inserted into the personality module connector (see Table 2.19 below for connector locations), four PCI Express lanes are routed to each port. When side 2 of the personality module is inserted into the personality module connector, eight PCI Express lanes are routed to the even port and the odd port is disconnected. Note that all four connectors must have a personality module inserted, whether all side 1, all side 2, or a combination. If all four personality module cards have side 1 plugged in, all 8 ports are in use. If all cards have side 2 plugged in, only 4 ports are in use.

Merged Ports	Personality Module Location
0/1	J10
2/3	J17
4/5	J14
6/7	J18

Table 2.19 PES32H8 Personality Module Locations

EB32H8 Evaluation Board Block Diagram

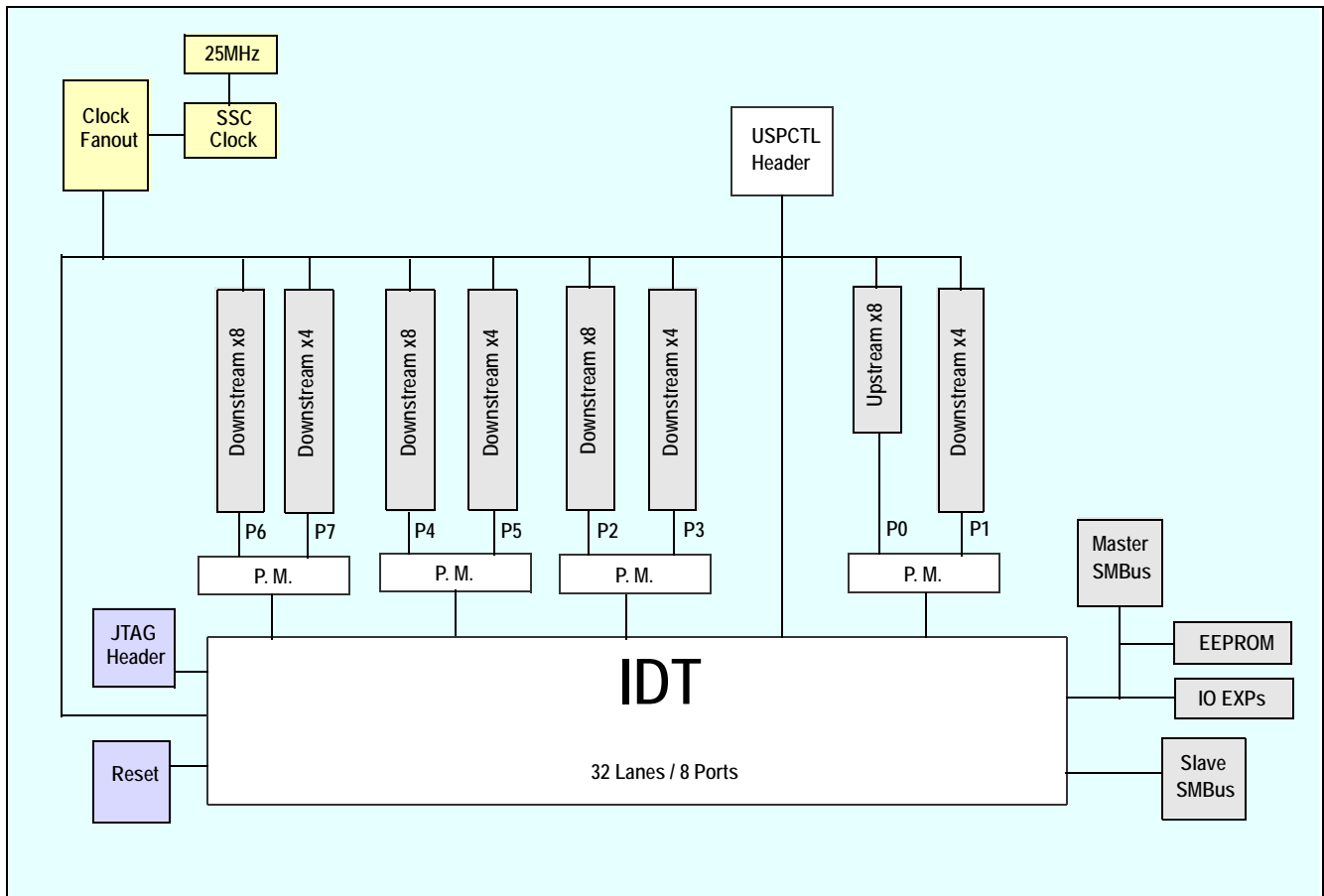


Figure 2.5 EB32H8 Eval Board Block Diagram



Software for the EB32H8 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB32H8 evaluation board using the device management software. Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES32H8 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES32H8.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES32H8, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES32H8 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes



Schematics

Notes

Schematics



B 7 6 5 4 3 2 1

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
STGC-0100R01	1.0	INITIAL RELEASE	2007-02-06	J. CARRILLO

SHEET DESCRIPTION

1	TABLE OF CONTENTS
2	BLOCK DIAGRAM
3	PES32H8 VSS
4	PES32H8 POWER
5	DECOUPLING CAPS
6	CLOCK REFERENCE
7	CLOCK DISTRIBUTION P1-5
8	CLOCK DISTRIBUTION P6-7
9	POWER SUPPLY
10	SMBUS REFCLK
11	PES32H8
12	IO EXPANDER P1 - P7
13	IO EXPANDER LINK STATUS
14	IO EXPANDER ATTN AND LEDS
15	HOT PLUG CONTROL PORT 2/3
16	HOT PLUG CONTROL PORT 4/5
17	HOT PLUG CONTROL PORT 6/7
18	HOT PLUG CONTROL PORT 1
19	PM PORT 0/1
20	PORT 0 CONNECTORS
21	PORT 1 CONNECTORS
22	PM PORT 2/3
23	PORT 2 CONNECTORS
24	PORT 3 CONNECTORS
25	PM PORT 4/5
26	PORT 4 CONNECTORS
27	PORT 5 CONNECTORS
28	PM PORT 6/7
29	PORT 6 CONNECTORS
30	PORT 7 CONNECTORS
31	WAKE

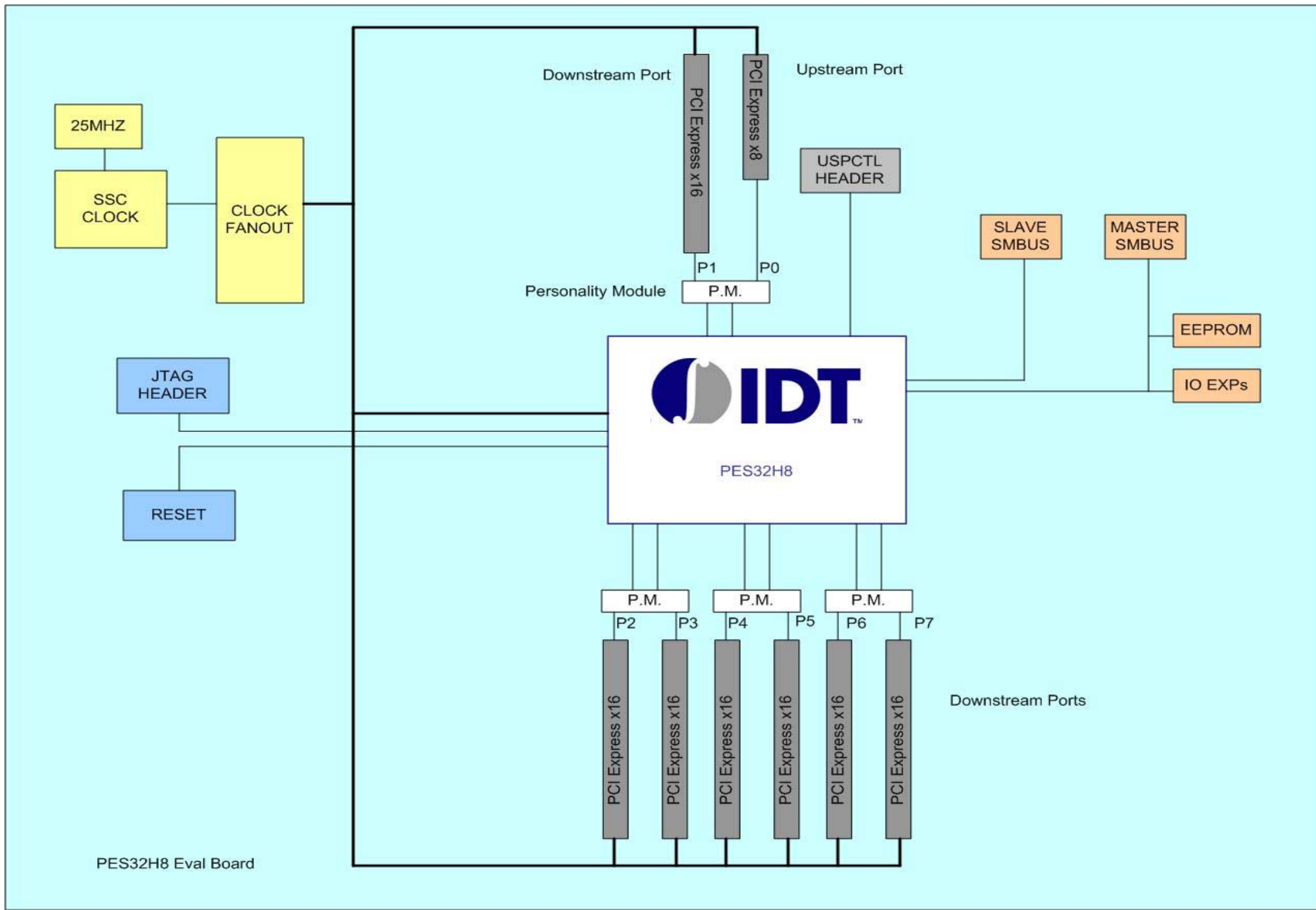


CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Tue Feb 06 09:32:08 2007			SHEET 1 OF 31

6 5 4 3 2 1

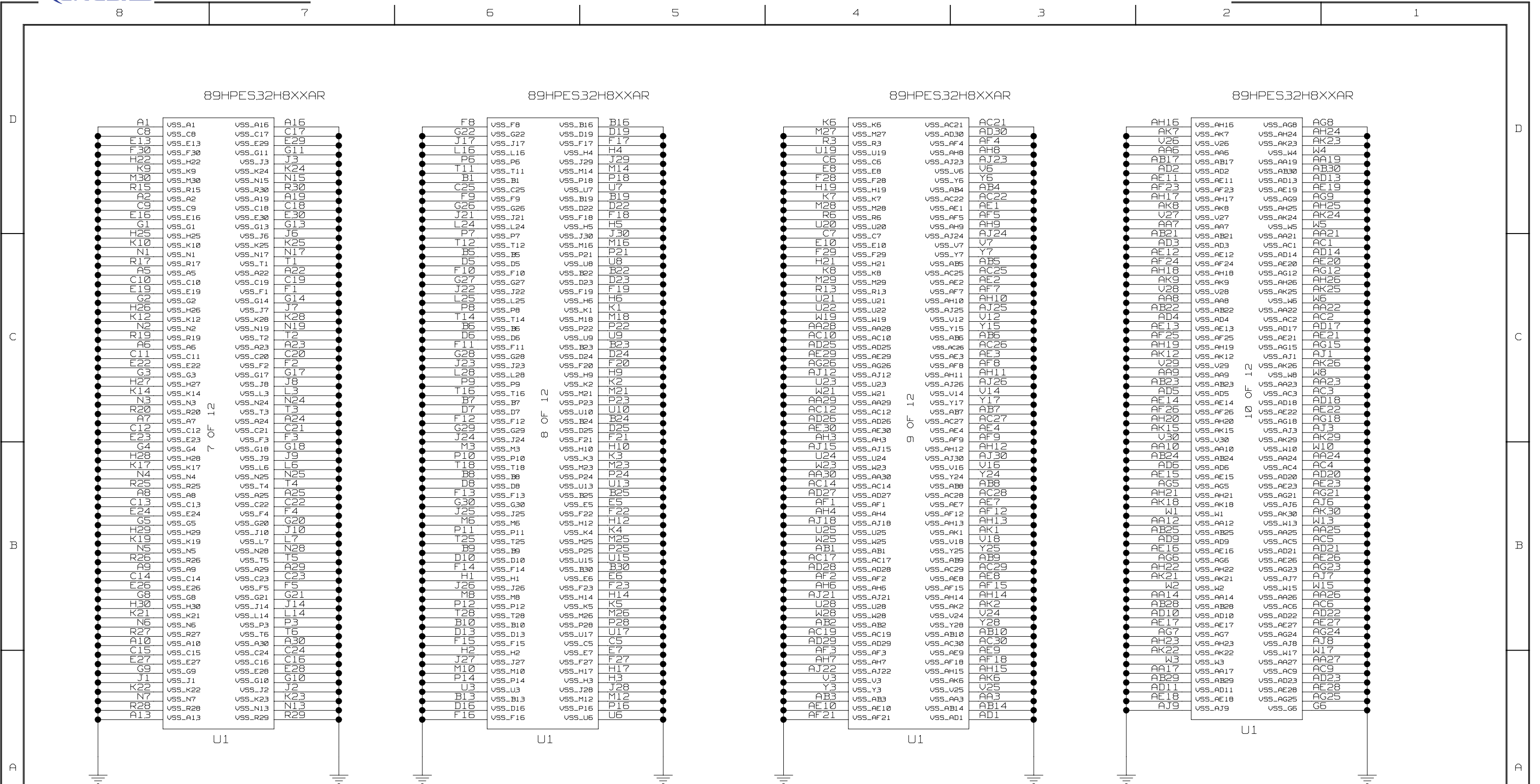
BLOCK DIAGRAM



PES32H8 Eval Board

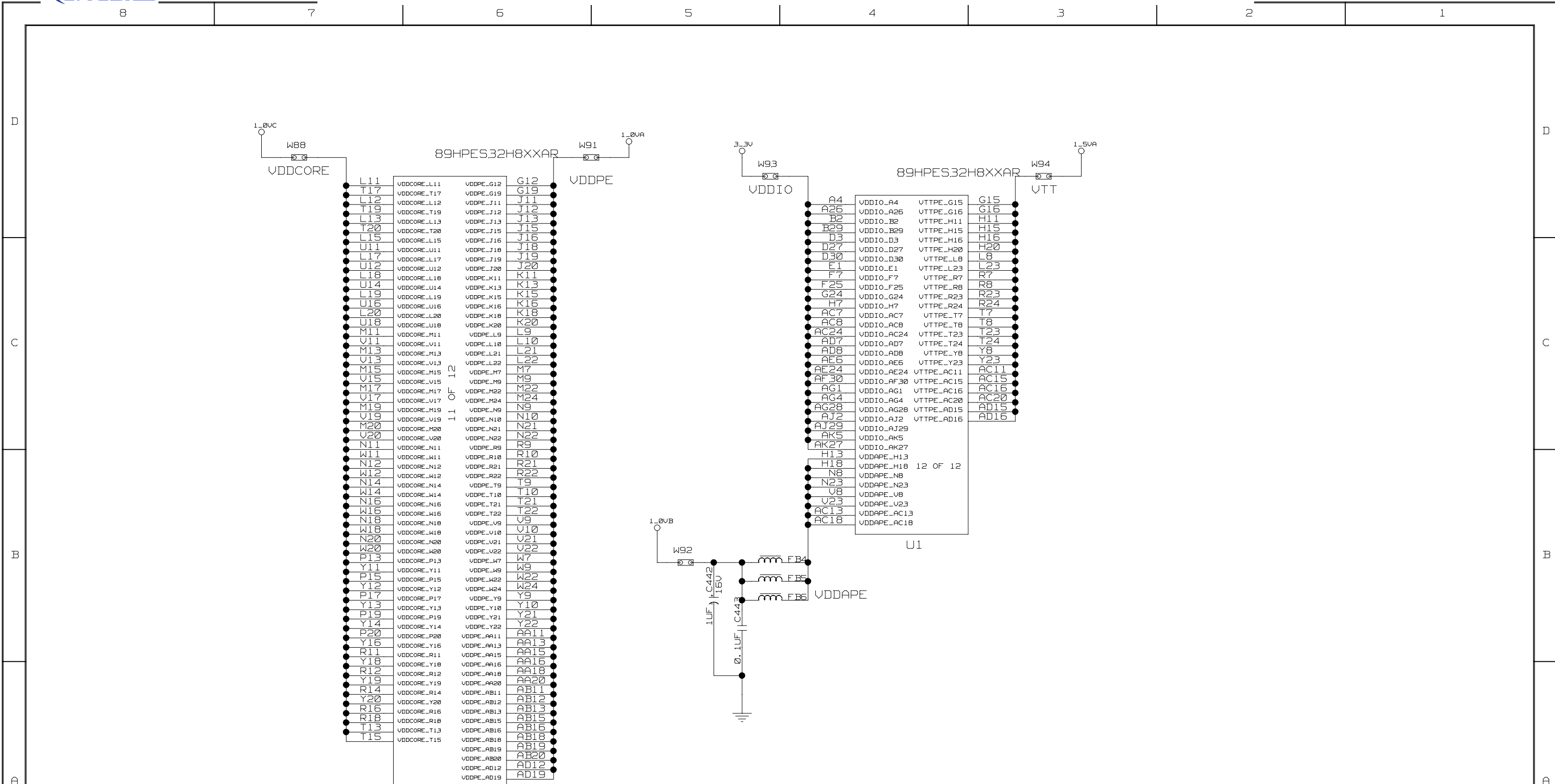
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 5024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
BLOCK DIAGRAM			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:43:39 2007			SHEET 2 OF 31



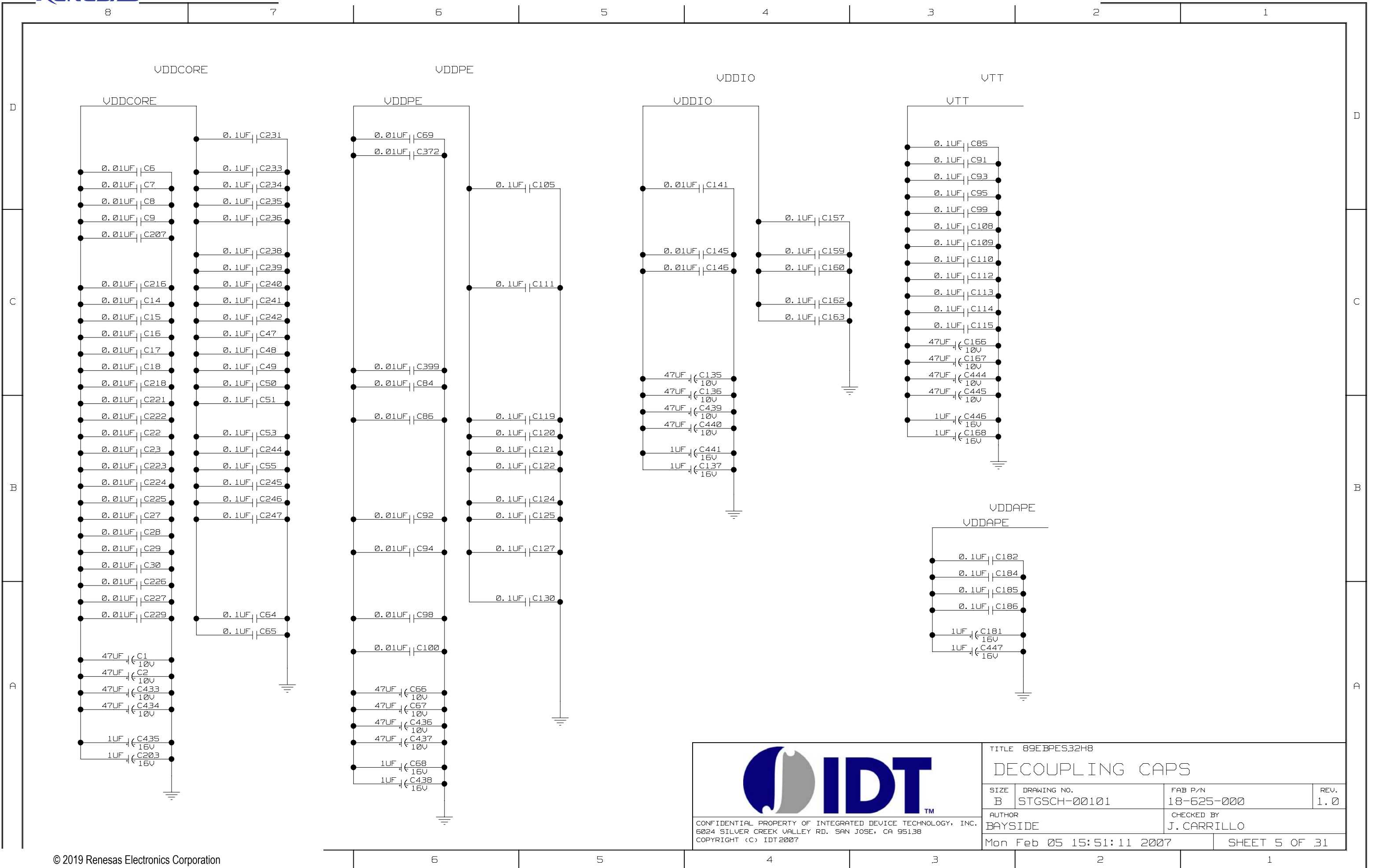
		TITLE 89E32H8	
		PES32H8 VSS	
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Tue Feb 06 09:32:19 2007		SHEET 3 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 5024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT 2007



		TITLE 89EBPES32H8		
		PES32H8 POWER		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00101	18-625-000	1.0	
AUTHOR		CHECKED BY		
BAYSIDE		J. CARRILLO		
Tue Feb 06 09:32:32 2007		SHEET 4 OF 31		

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



		TITLE 89EBPES32H8		
		DECOUPLING CAPS		
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0	
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO		
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT2007		Mon Feb 05 15:51:11 2007	SHEET 5 OF 31	



8 7 6 5 4 3 2 1

D

D

C

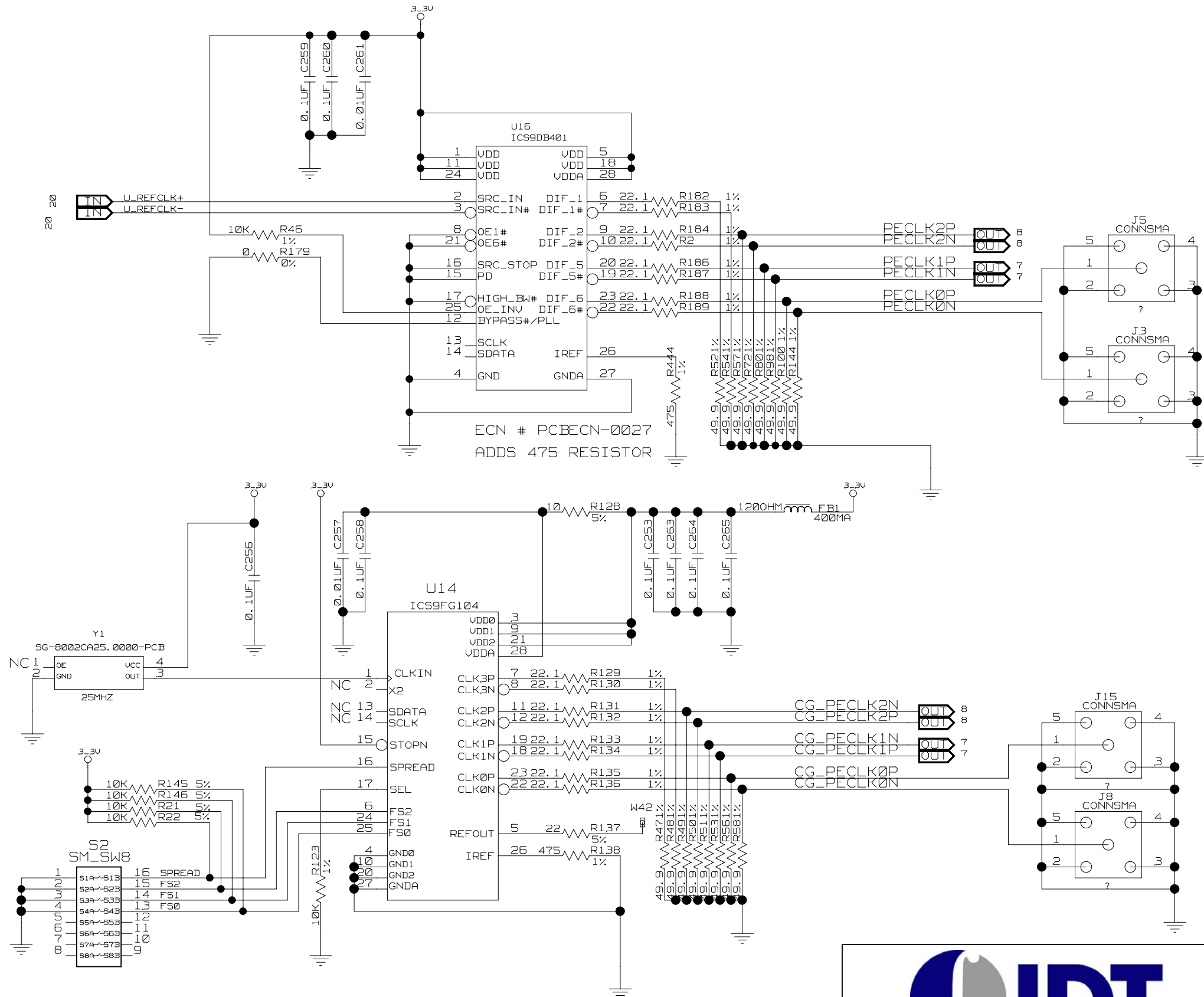
C

B

B

A

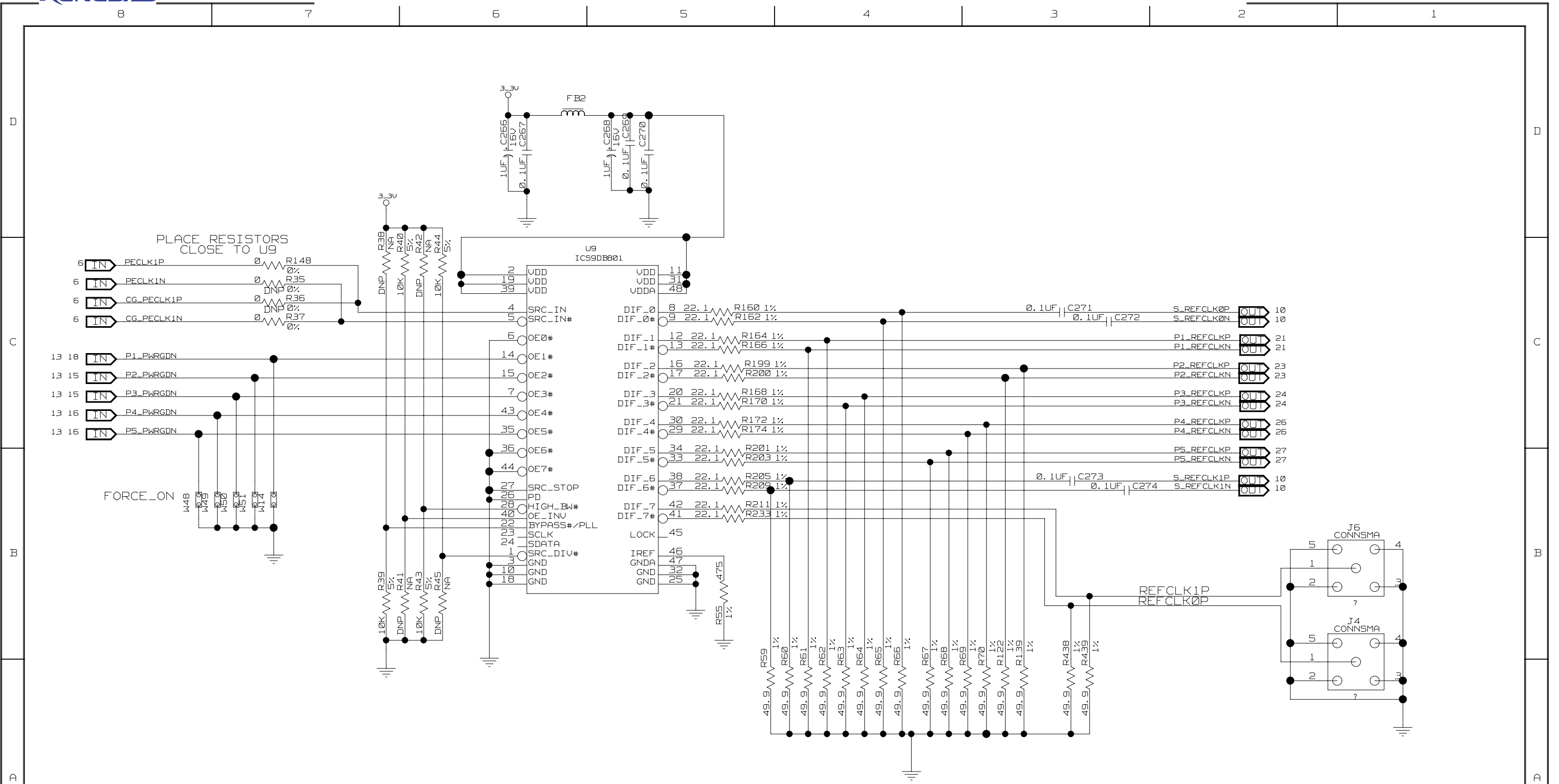
A



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

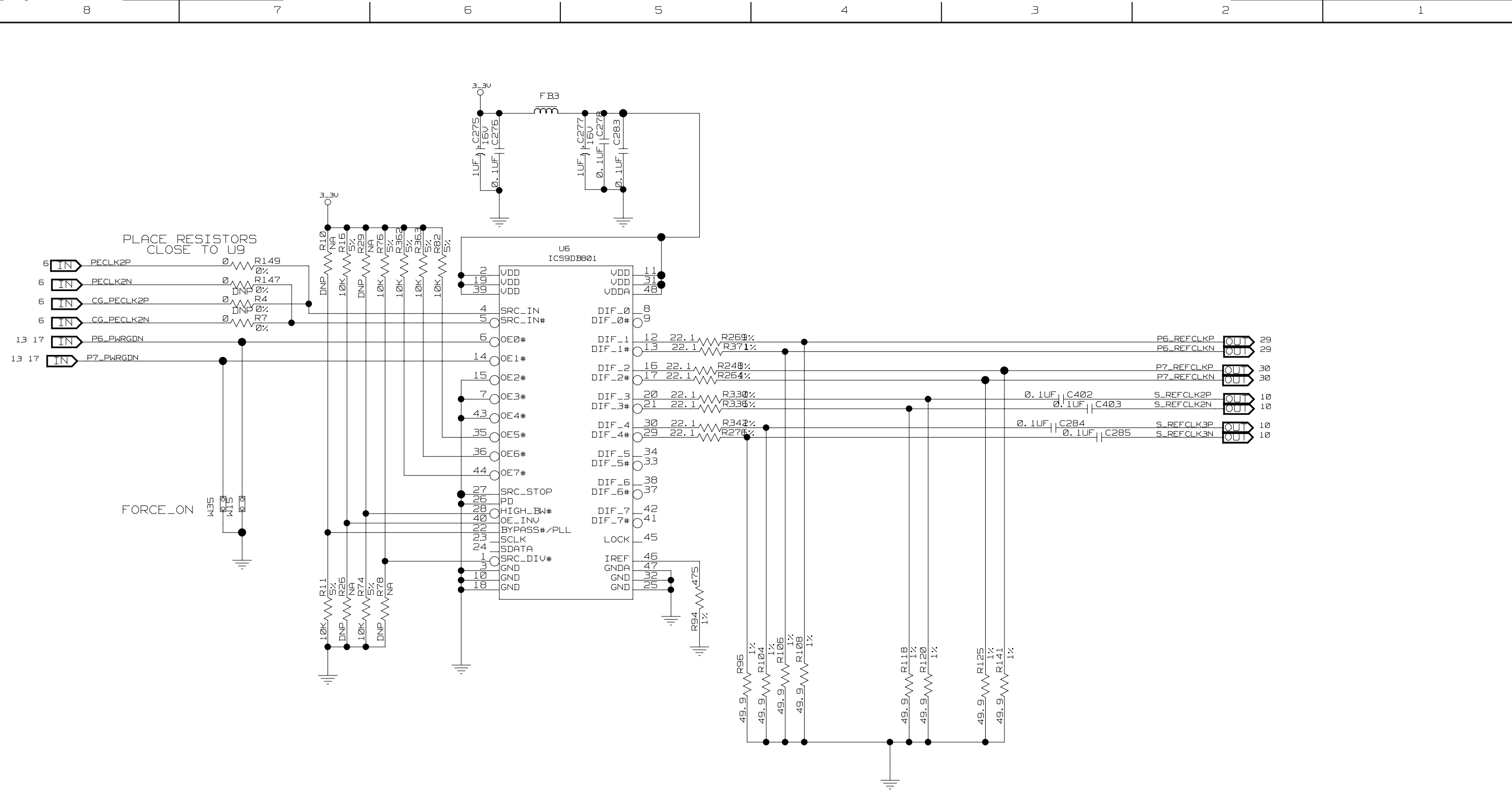
TITLE 89EBPES32H8			
CLOCK REFERENCE			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:51:06 2007			SHEET 6 OF 31

6 5 4 3 2 1



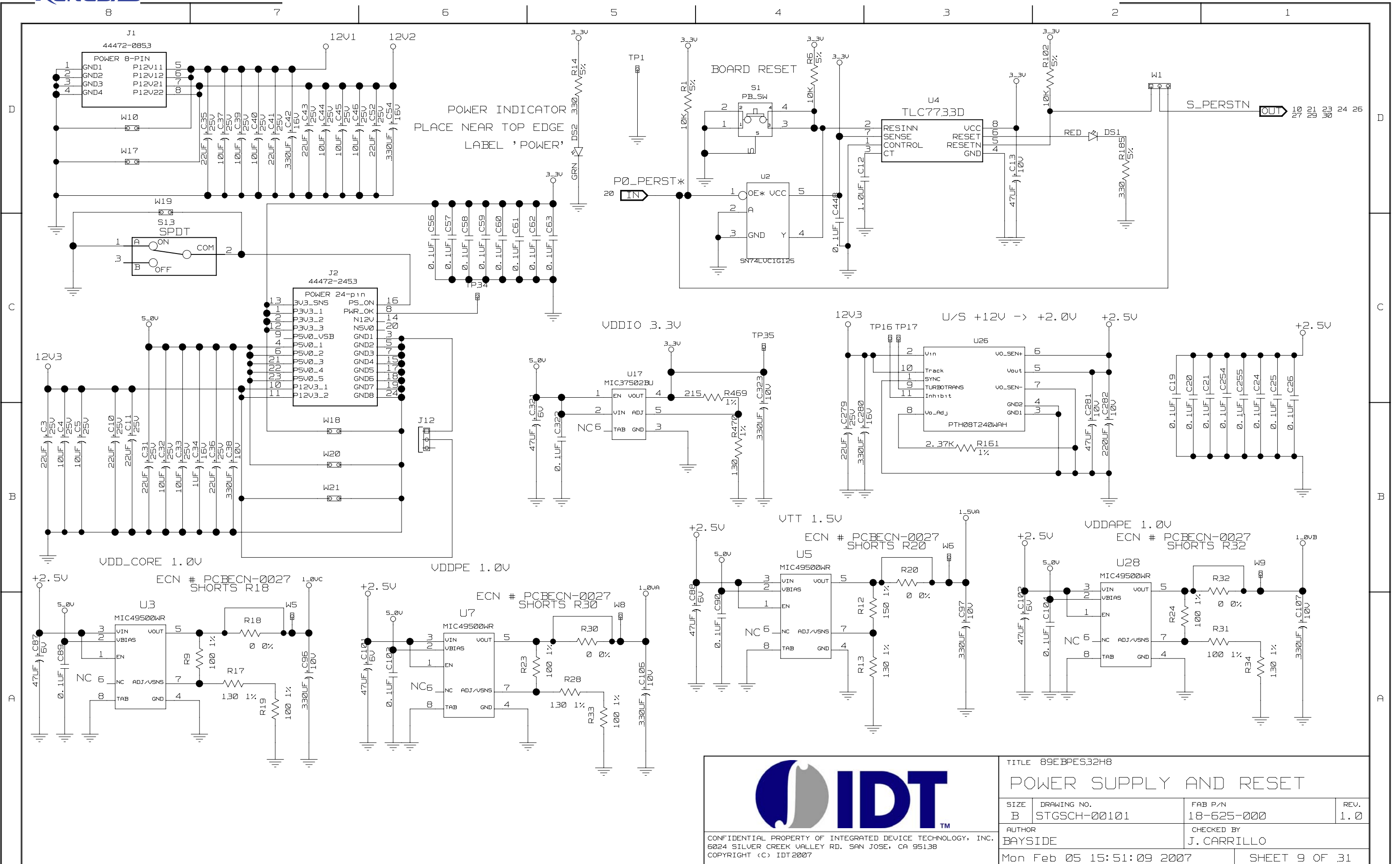
		TITLE 89EBPES32H8		
		CLOCK DISTRIBUTION P1-5		
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0	
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO		
Mon Feb 05 15:51:07 2007		SHEET 7 OF 31		

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



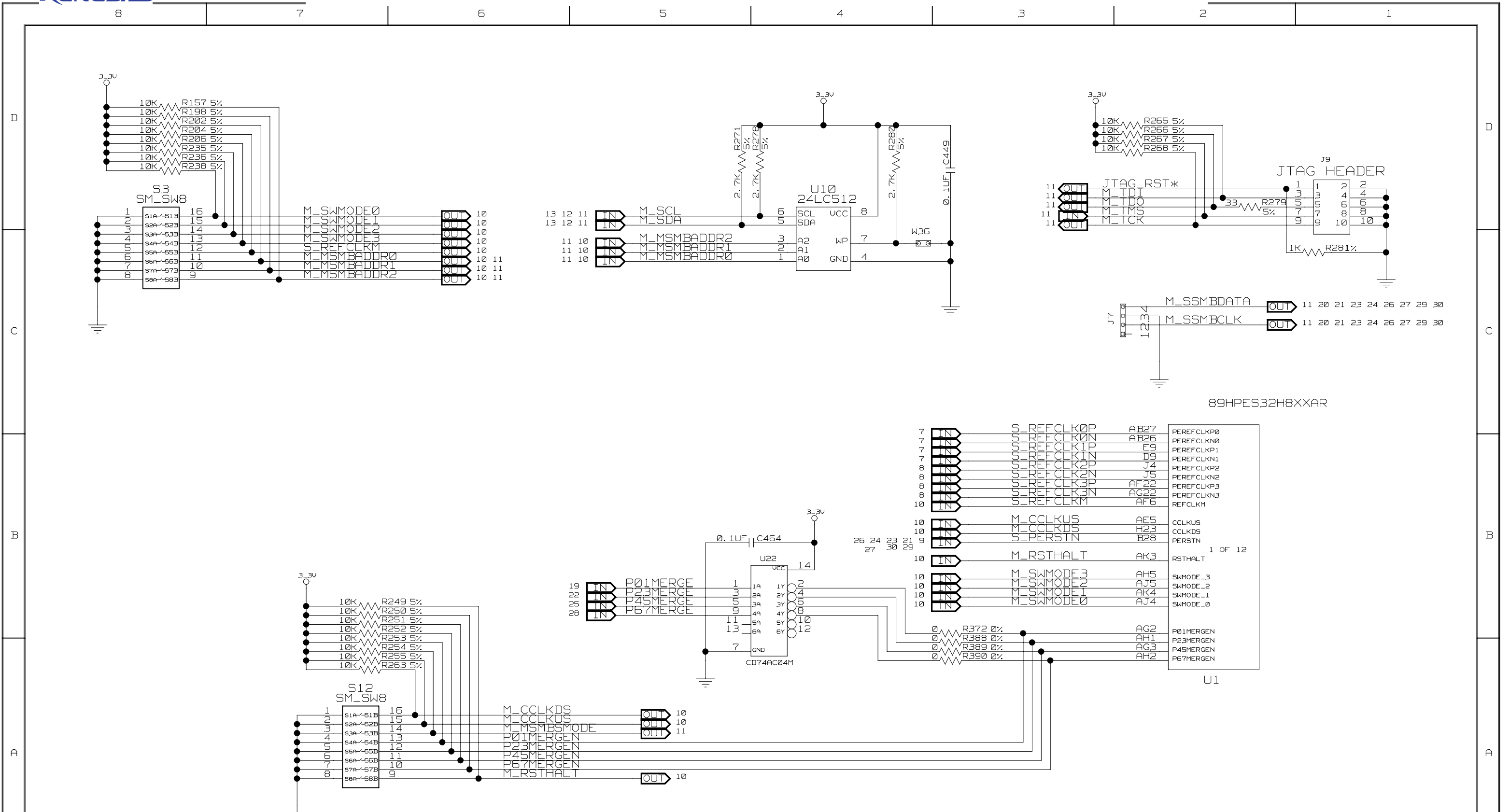
		TITLE 89EBPES32H8		
		CLOCK DISTRIBUTION P6-7		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00101	18-625-000	1.0	
AUTHOR		CHECKED BY		
BAYSIDE		J. CARRILLO		
Mon Feb 05 15:51:08 2007			SHEET 8 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

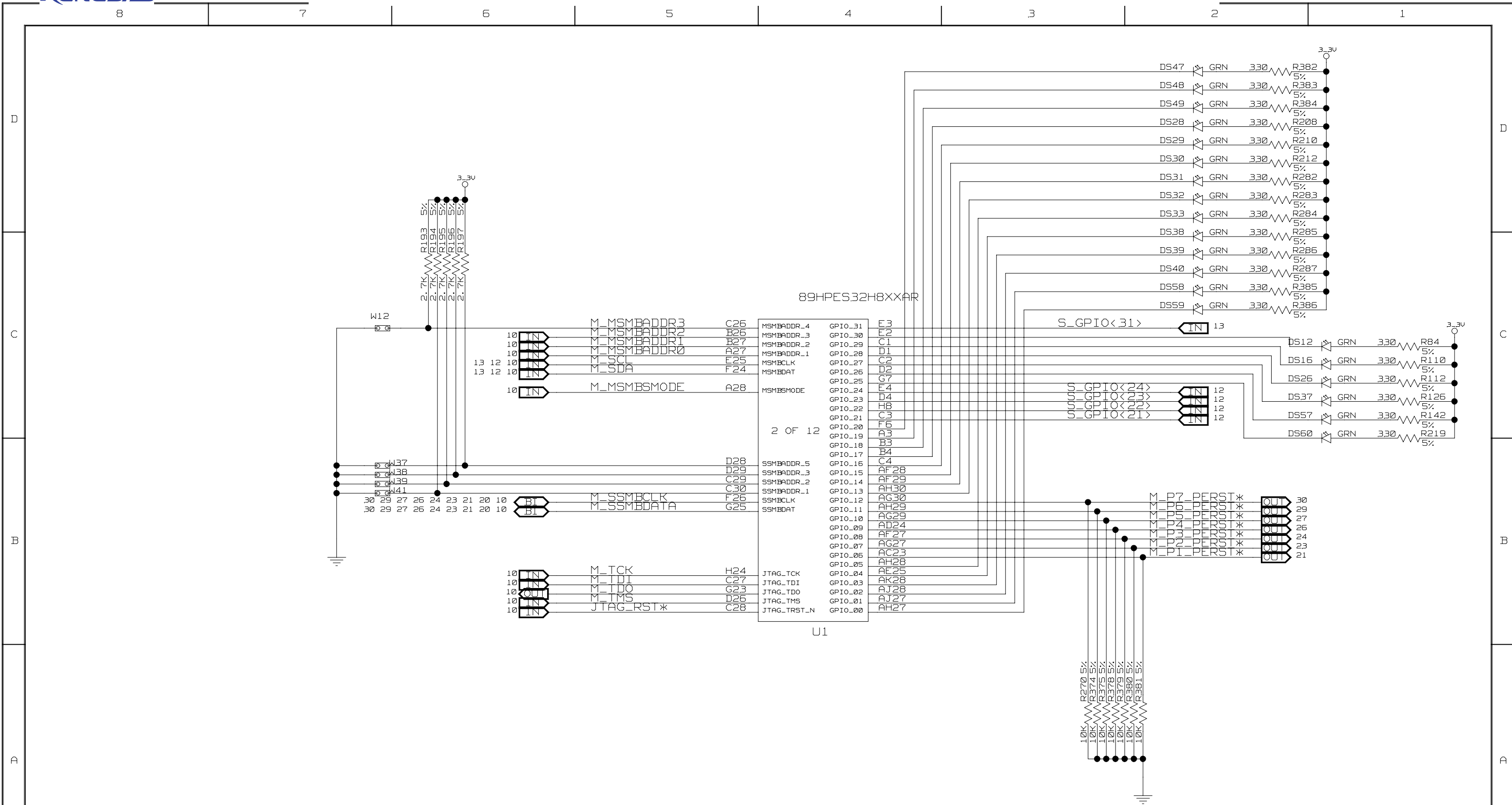


		TITLE 89EBPES32H8	
		POWER SUPPLY AND RESET	
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:51:09 2007		SHEET 9 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
COPYRIGHT (C) IDT2007

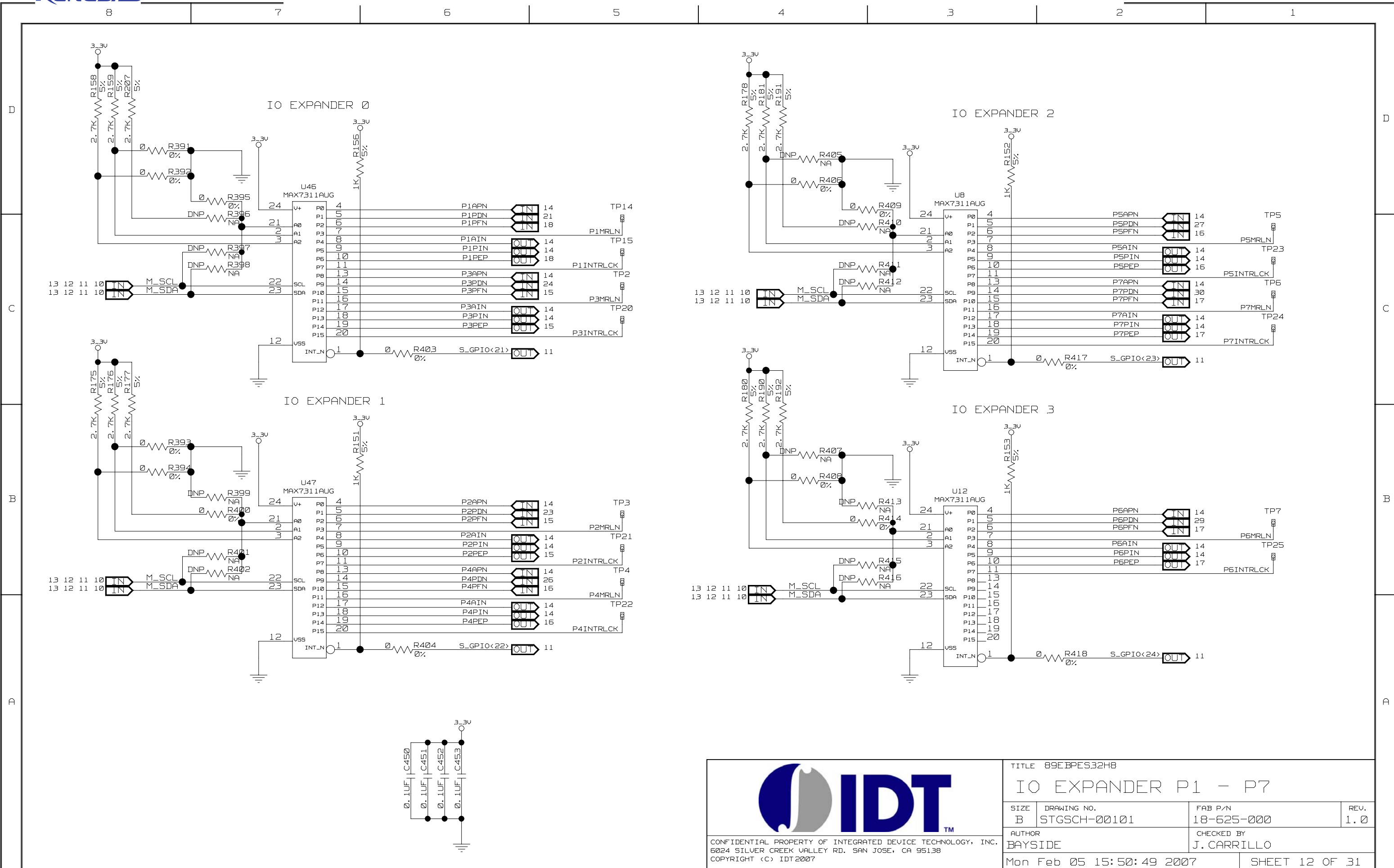


		TITLE 89EBPES32H8	
		SMBUS REFCLK	
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT2007		Mon Feb 05 15:50:47 2007	SHEET 10 OF 31



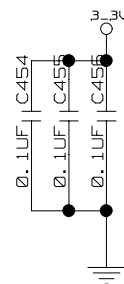
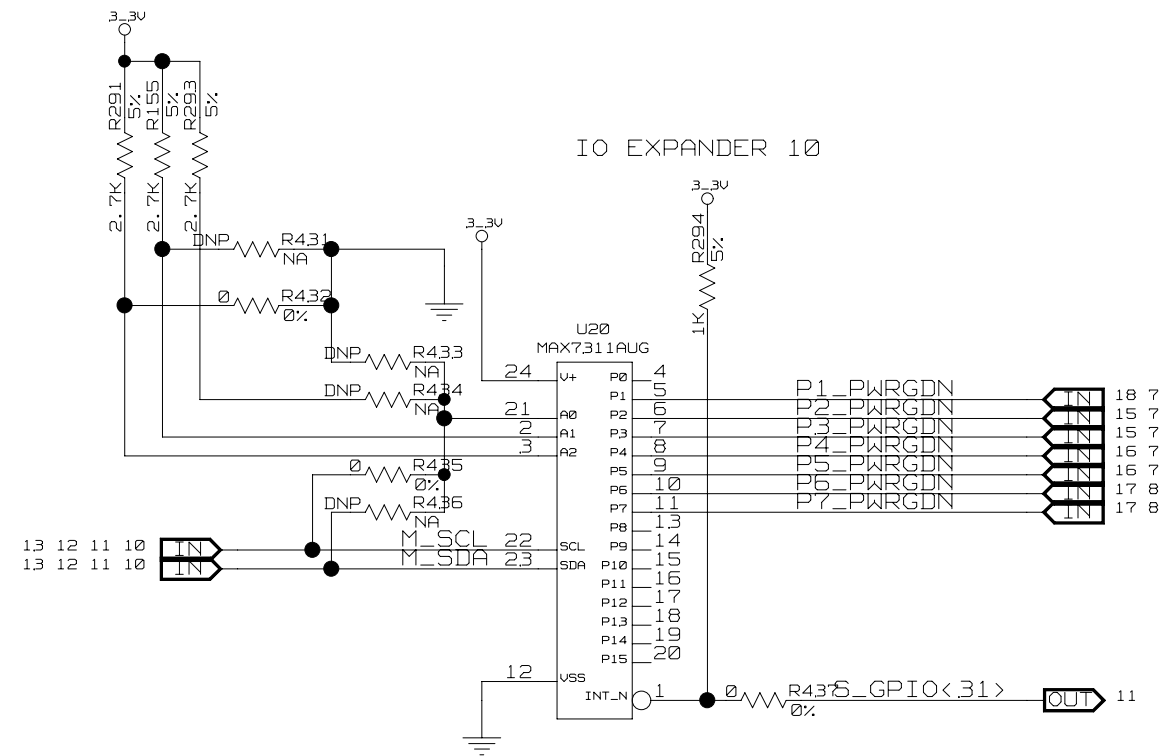
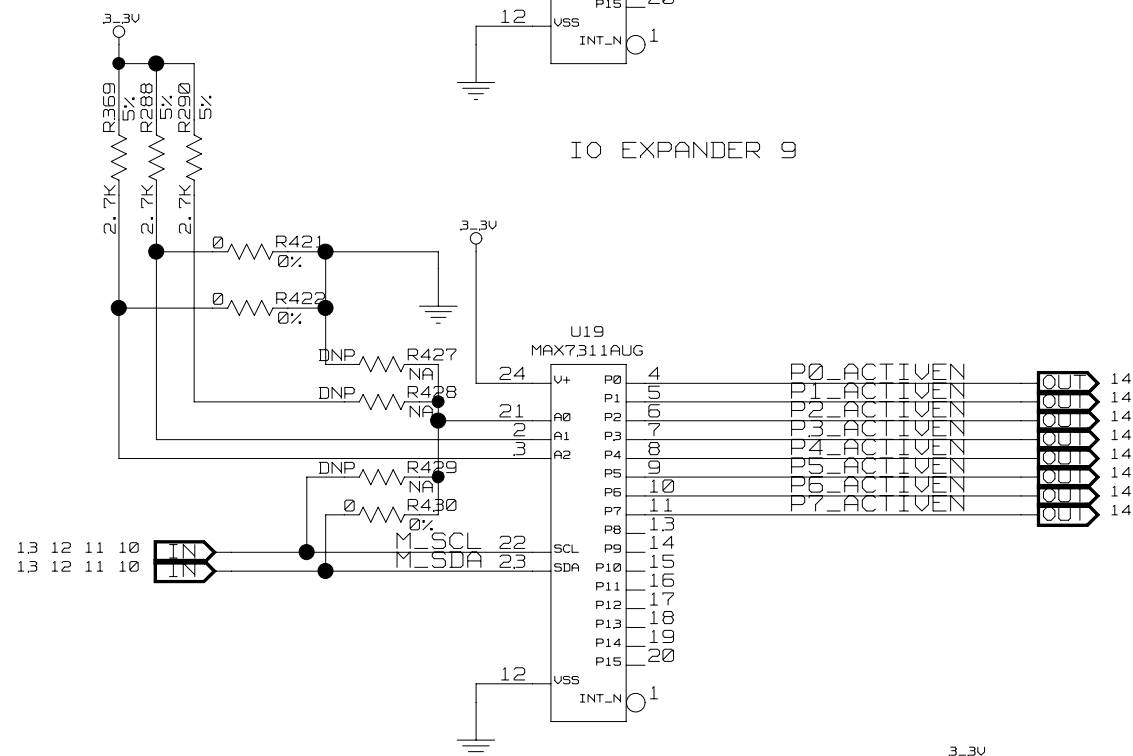
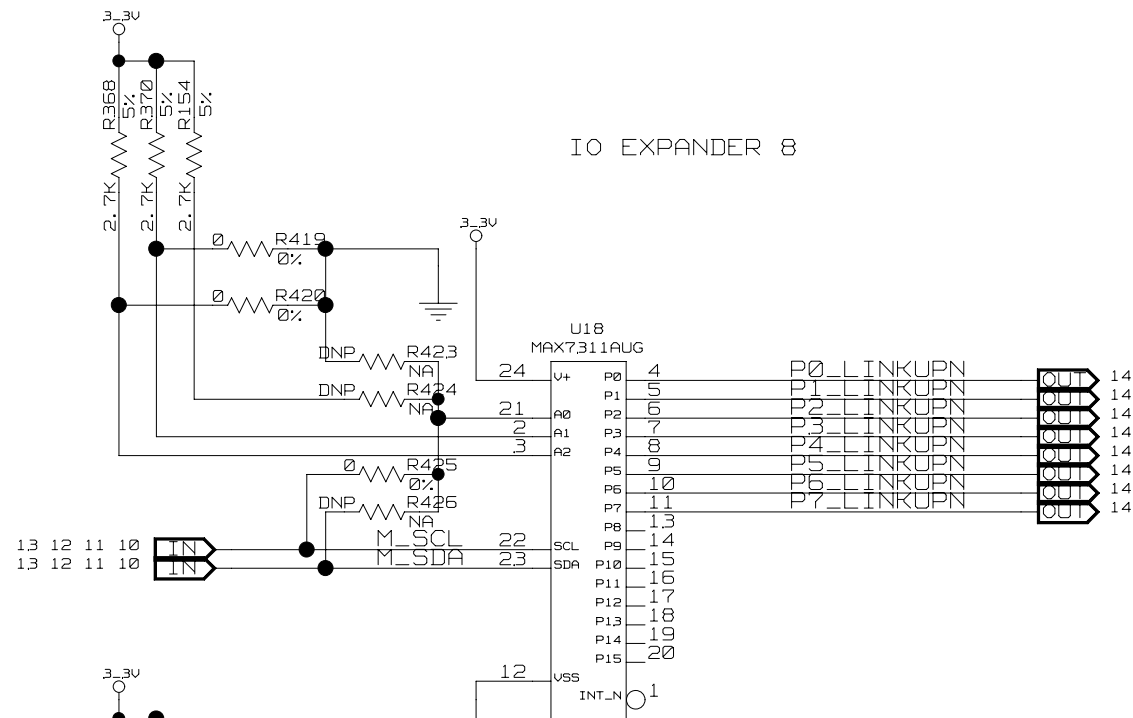
		TITLE 89BPES32H8		
		PES32H8		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00101	18-625-000	1.0	
AUTHOR		CHECKED BY		
BAYSIDE		J. CARRILLO		
Mon Feb 05 15:50:48 2007			SHEET 11 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



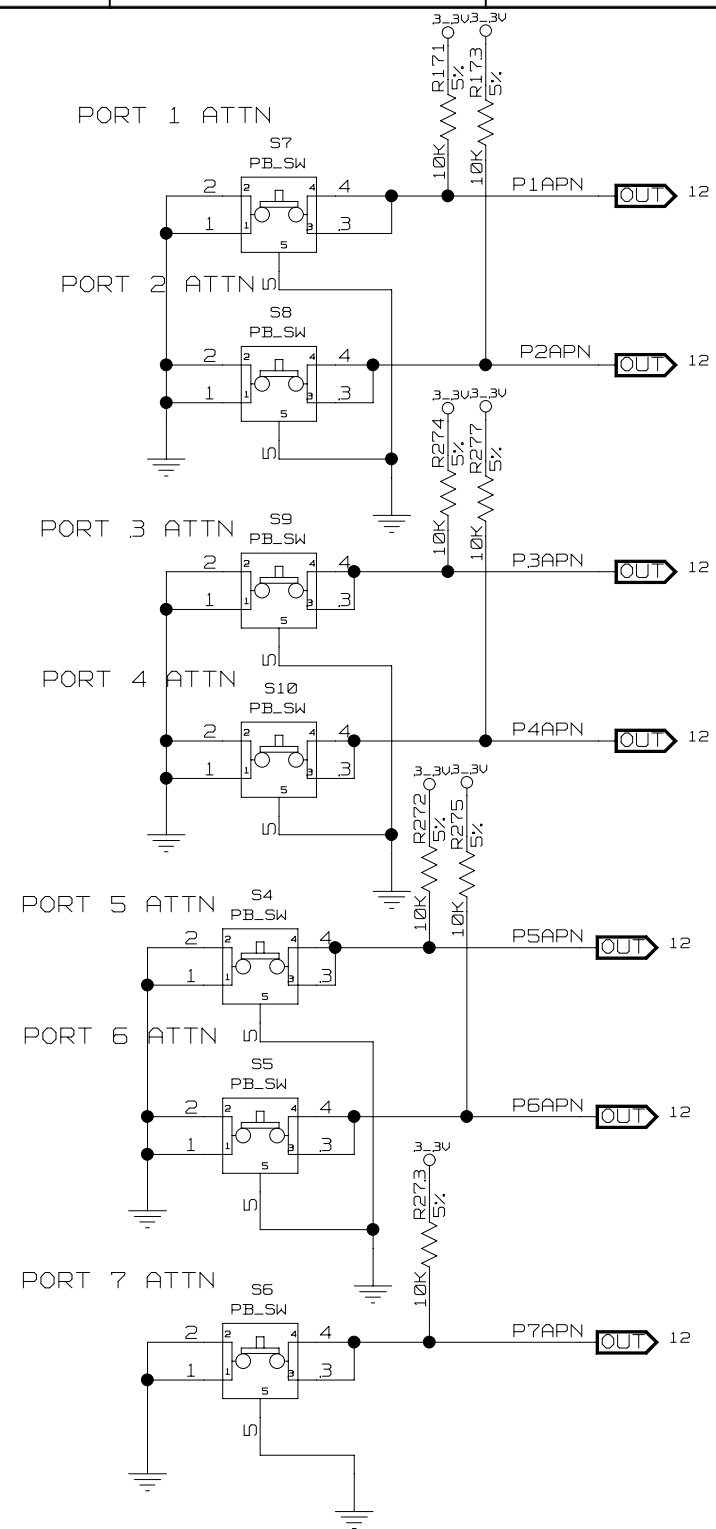
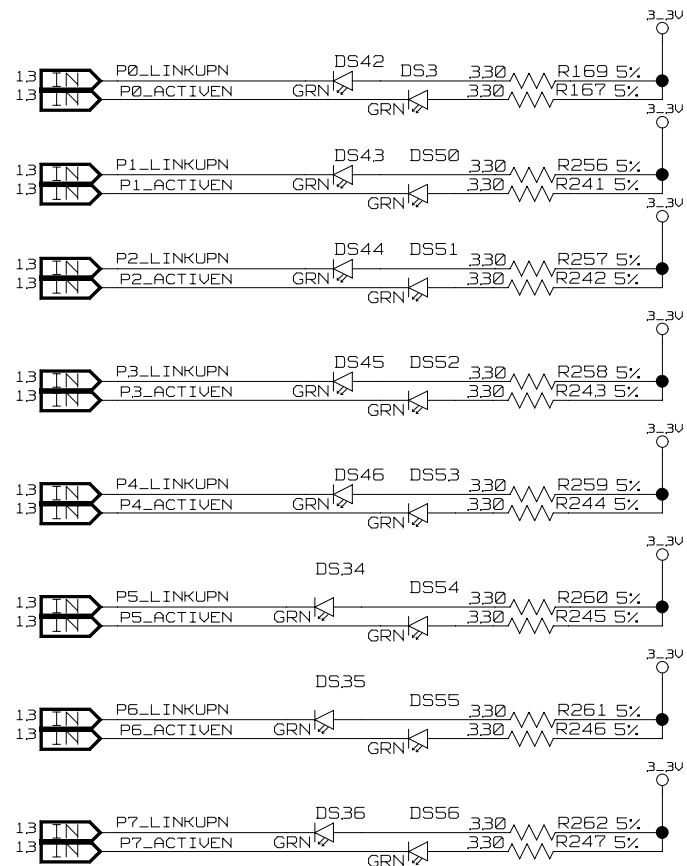
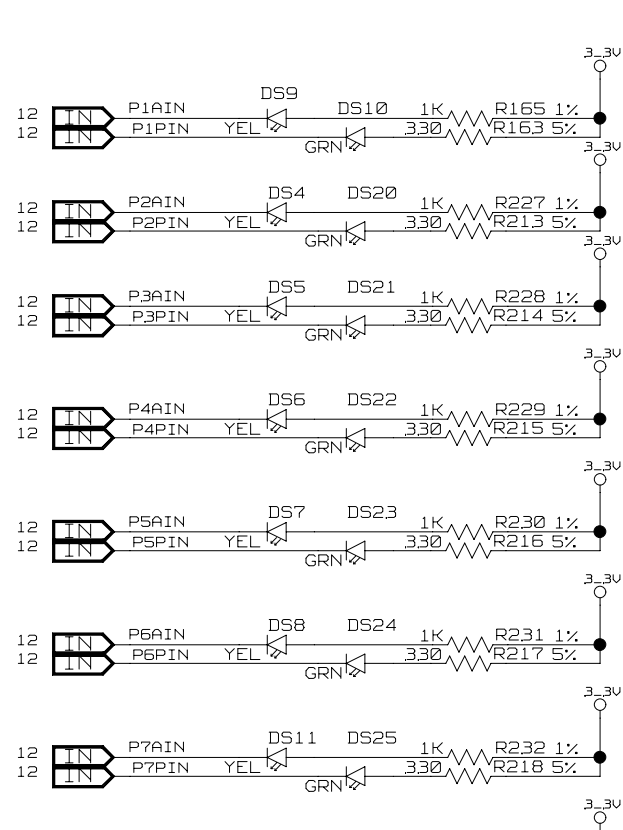
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
IO EXPANDER P1 - P7			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00101	18-625-000	1.0
AUTHOR		CHECKED BY	
BAYSIDE		J. CARRILLO	
Mon Feb 05 15:50:49 2007			SHEET 12 OF 31



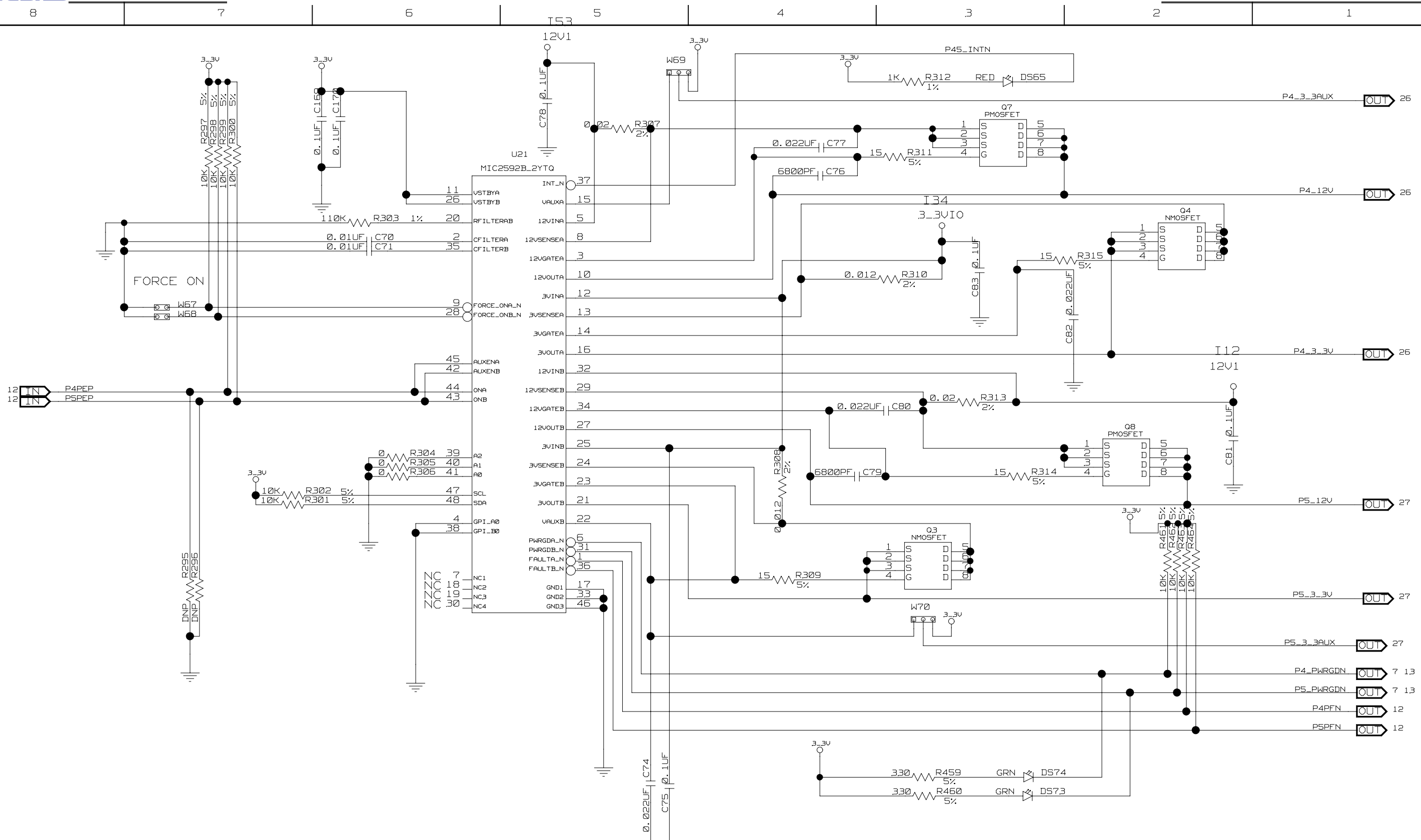
		TITLE 89EBPES32H8		
		IO EXPANDER LINK STATUS		
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0	
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO		
Mon Feb 05 15:50:50 2007		SHEET 13 OF 31		

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

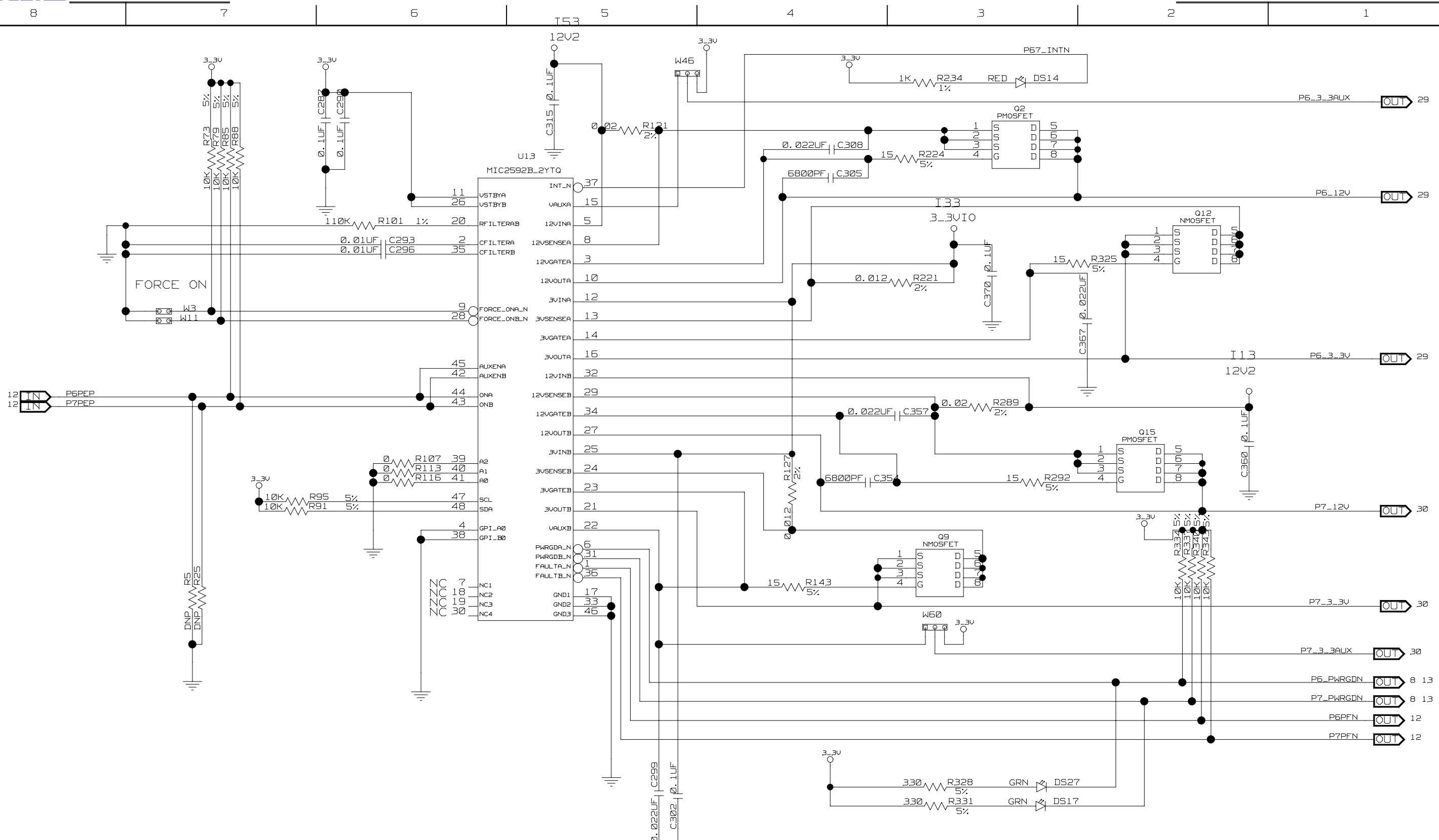


CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
IO EXPANDER ATTN PB/LEDS			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:50:51 2007			SHEET 14 OF 31



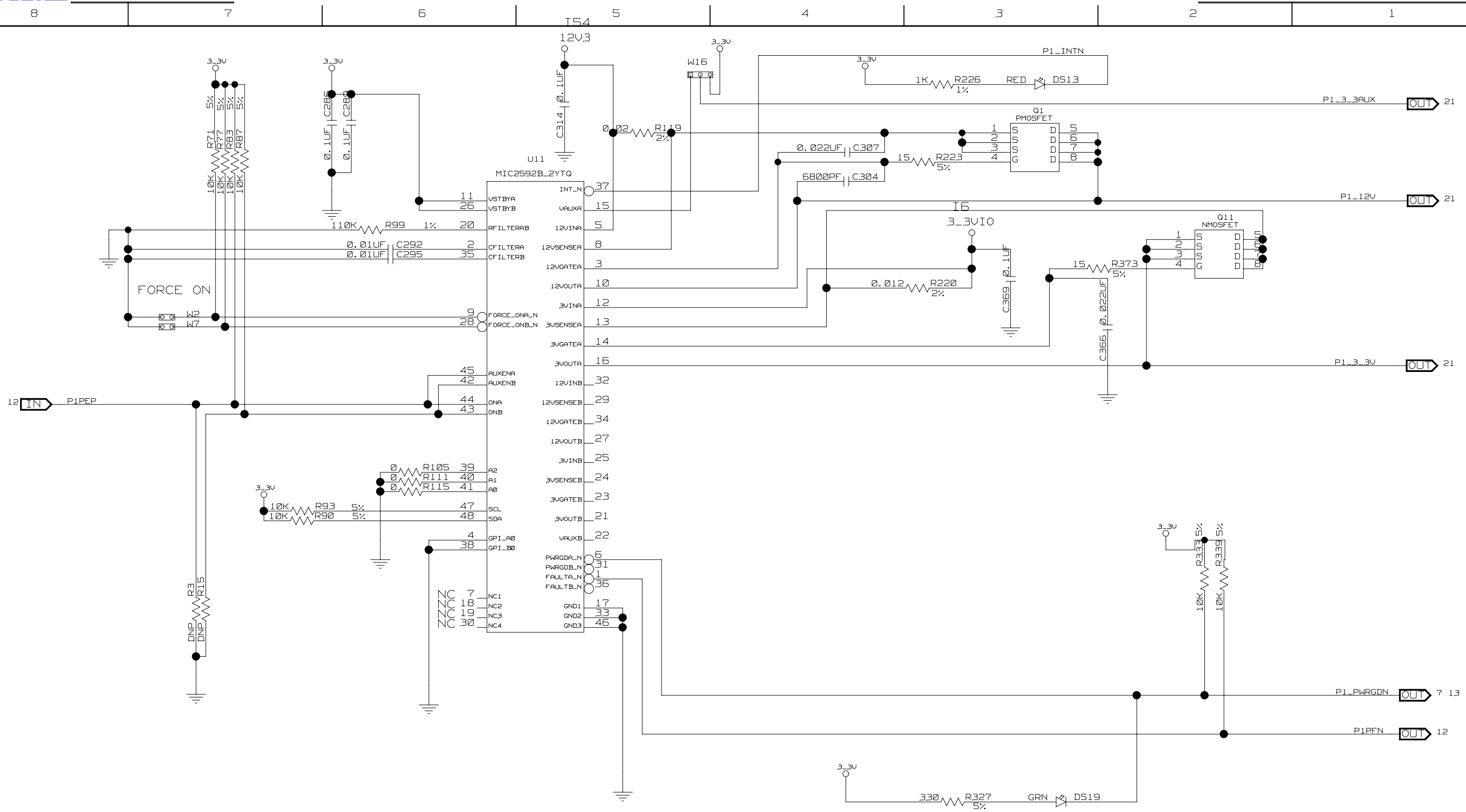
		TITLE 89EBPES32H8		
		HOT PLUG CONTROL PORT 4/5		
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0	
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO		
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT2007		Mon Feb 05 15:50:52 2007 SHEET 16 OF 31		



TITLE 89EBPES32H8
HOT PLUG CONTROL PORT 6/7

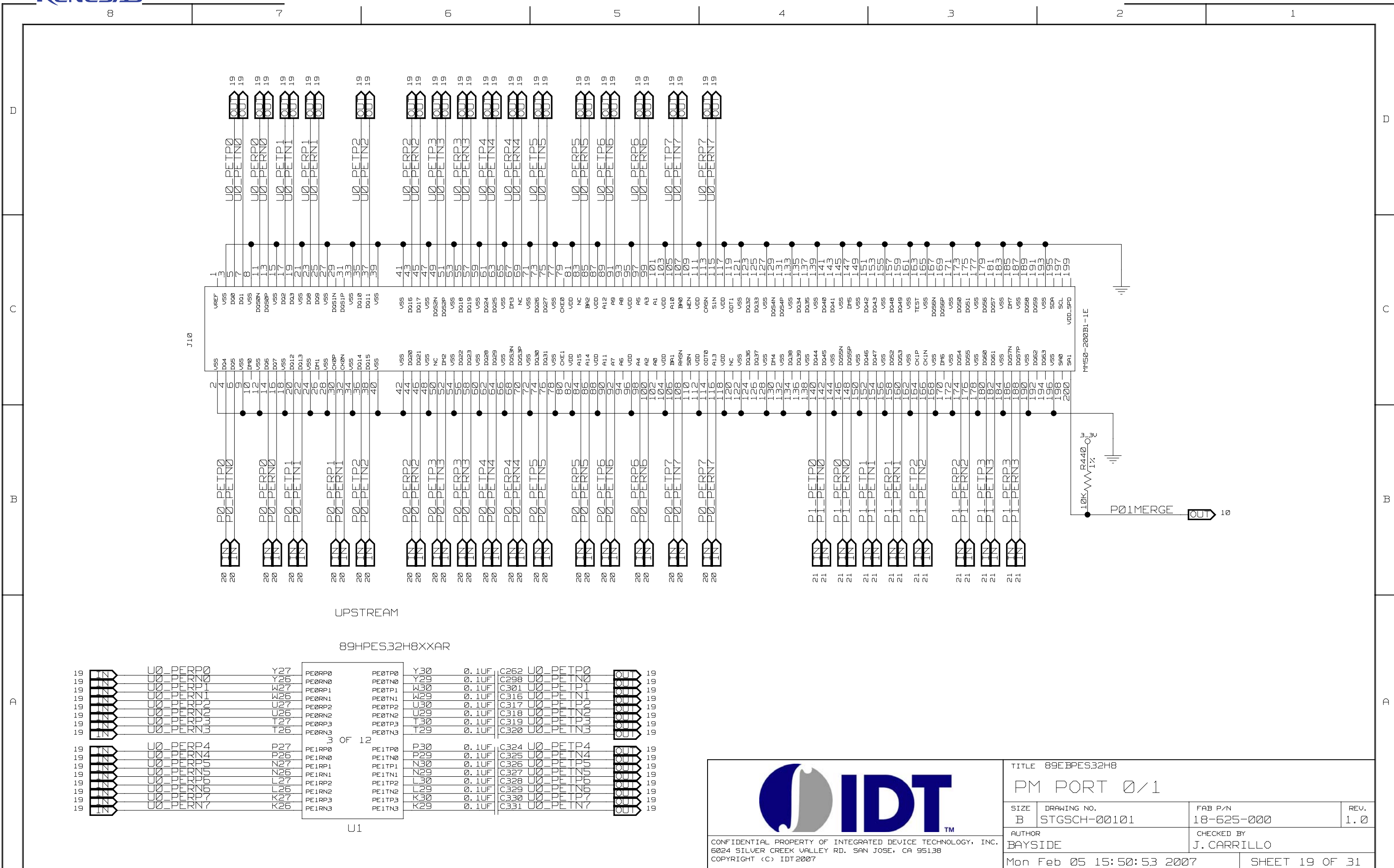
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:51:04 2007			SHEET 17 OF 31

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
COPYRIGHT (C) IDT2007



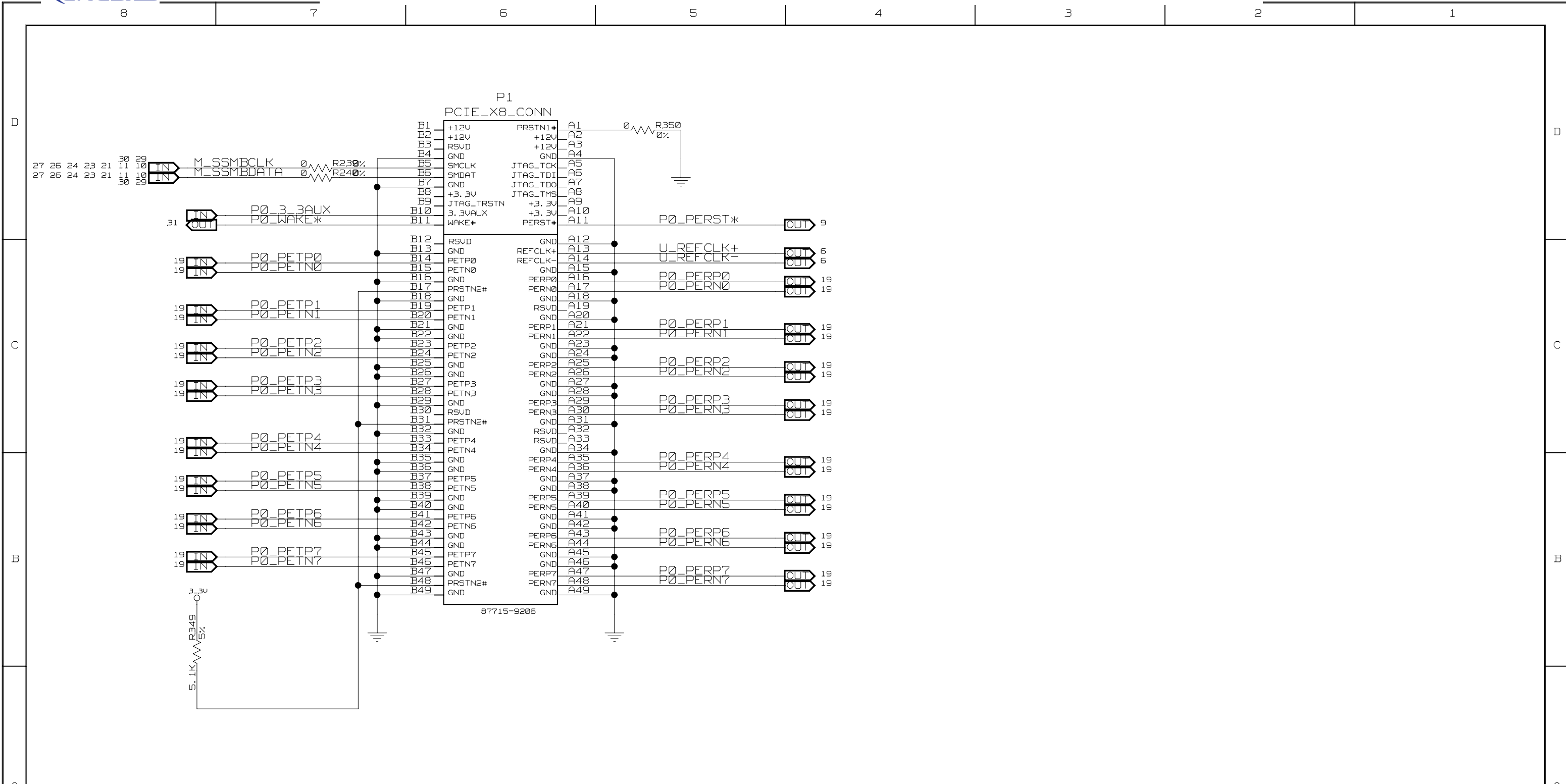
		TITLE 89EBPES32H8		
		HOT PLUG CONTROL PORT 1		
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0	
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO		
Mon Feb 05 15:51:03 2007		SHEET 18 OF 31		

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



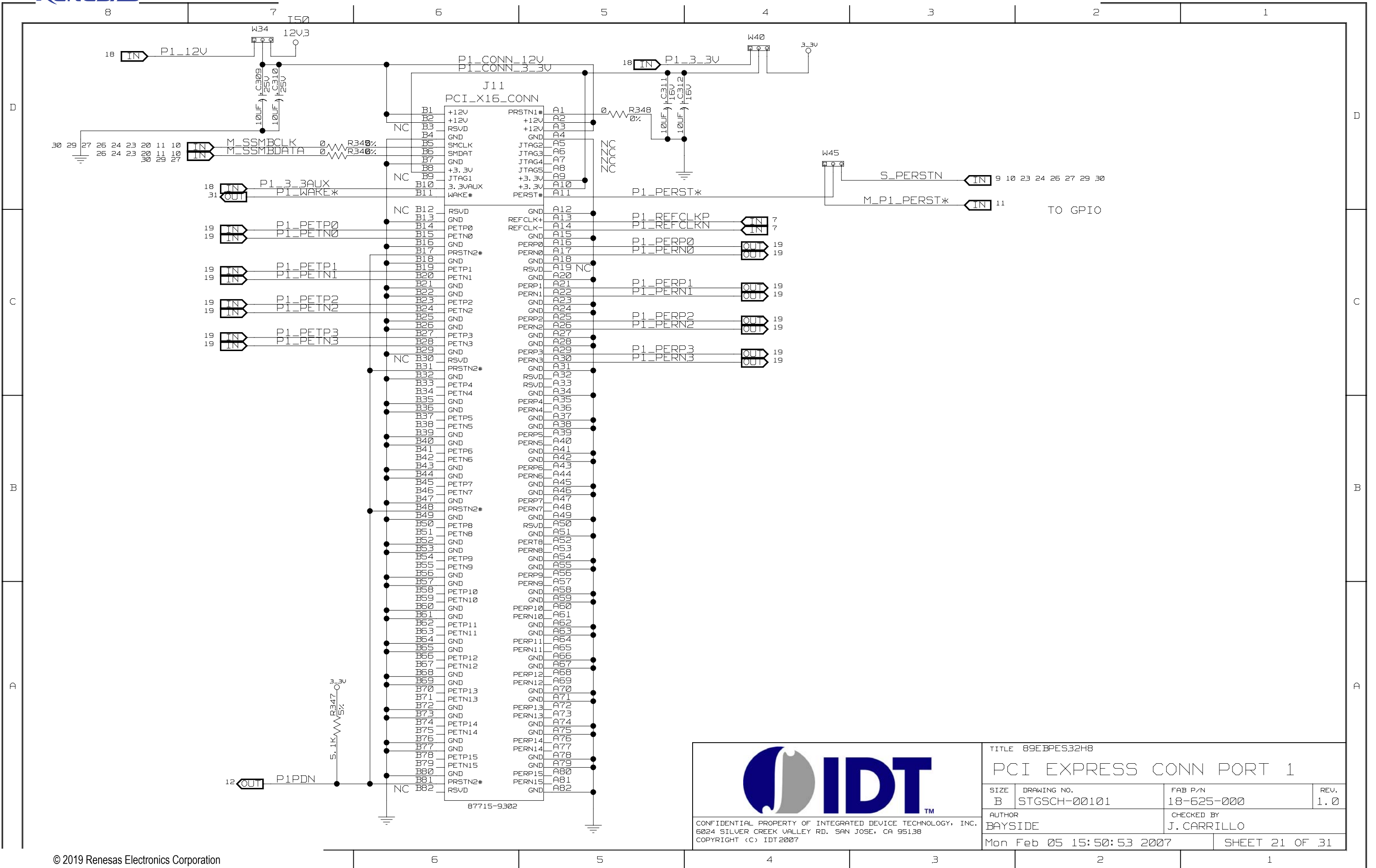
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC. 5024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138 COPYRIGHT (C) IDT2007

TITLE 89EBPES.32H8			
PM PORT 0/1			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:50:53 2007			SHEET 19 OF 31



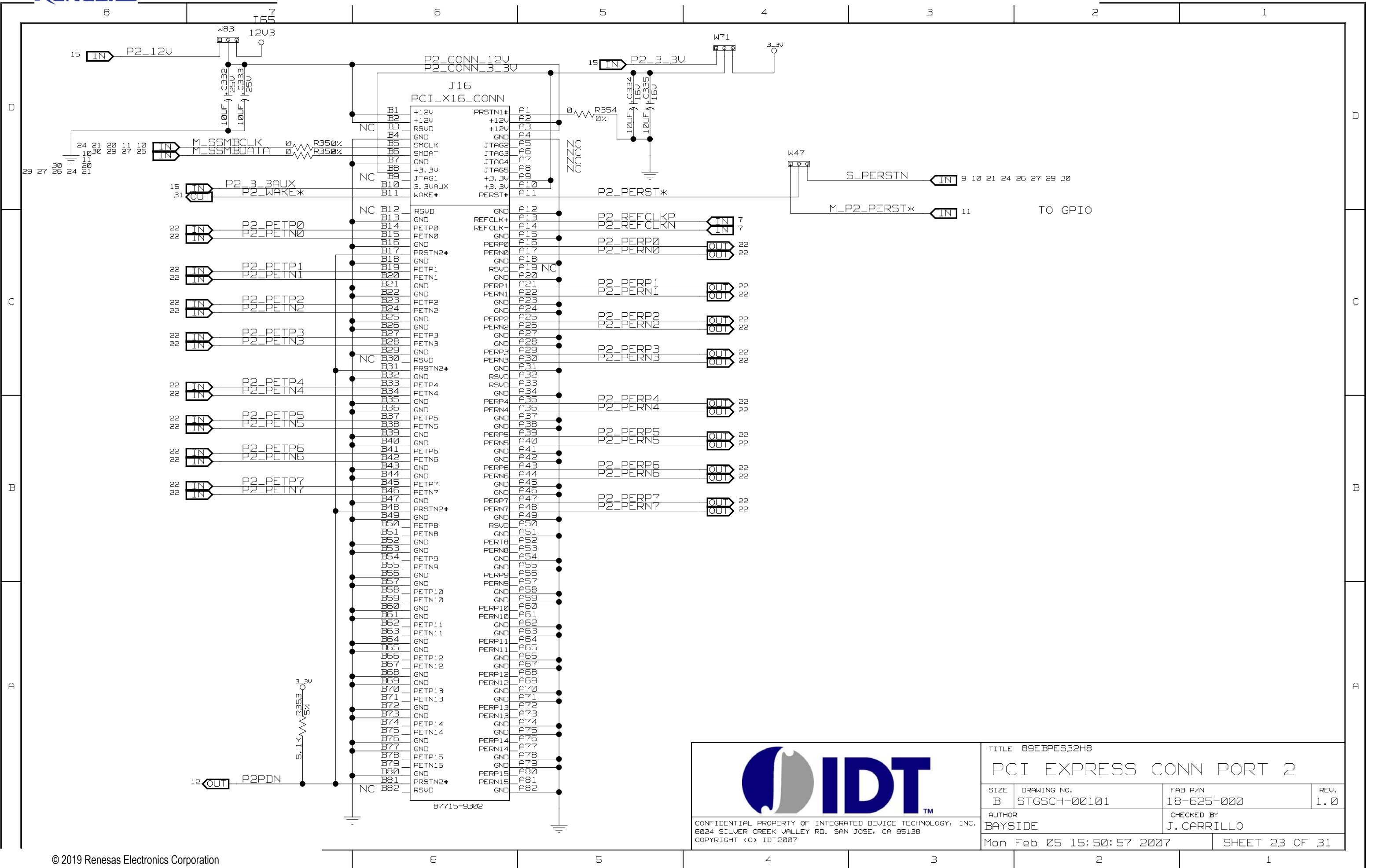
		TITLE 89EBPES32H8		
		UPSTREAM PORT 0		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00101	18-625-000	1.0	
AUTHOR		CHECKED BY		
BAYSIDE		J. CARRILLO		
Mon Feb 05 15:50:54 2007			SHEET 20 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



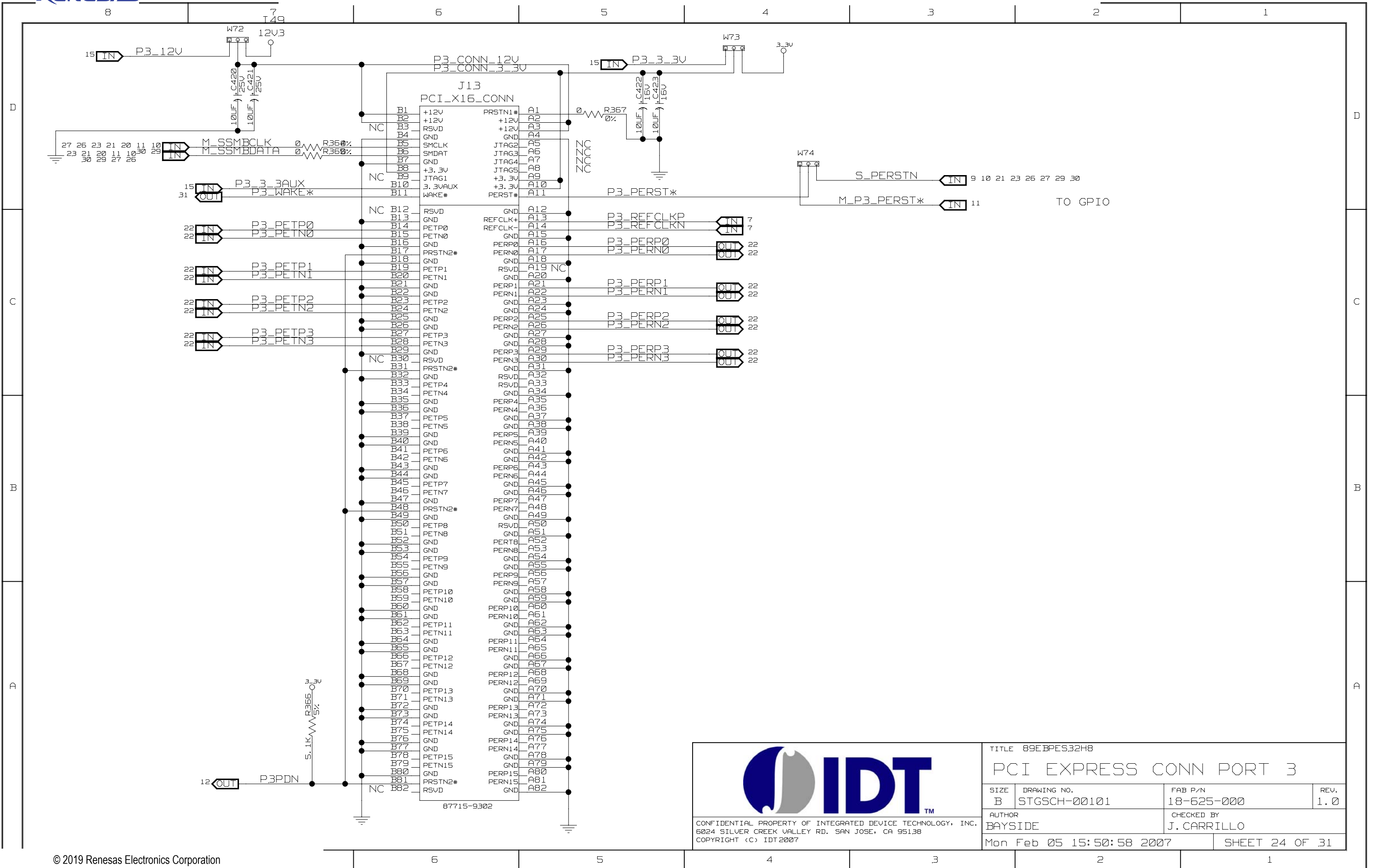
		TITLE 89EBPES32H8	
		PCI EXPRESS CONN PORT 1	
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:50:53 2007		SHEET 21 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



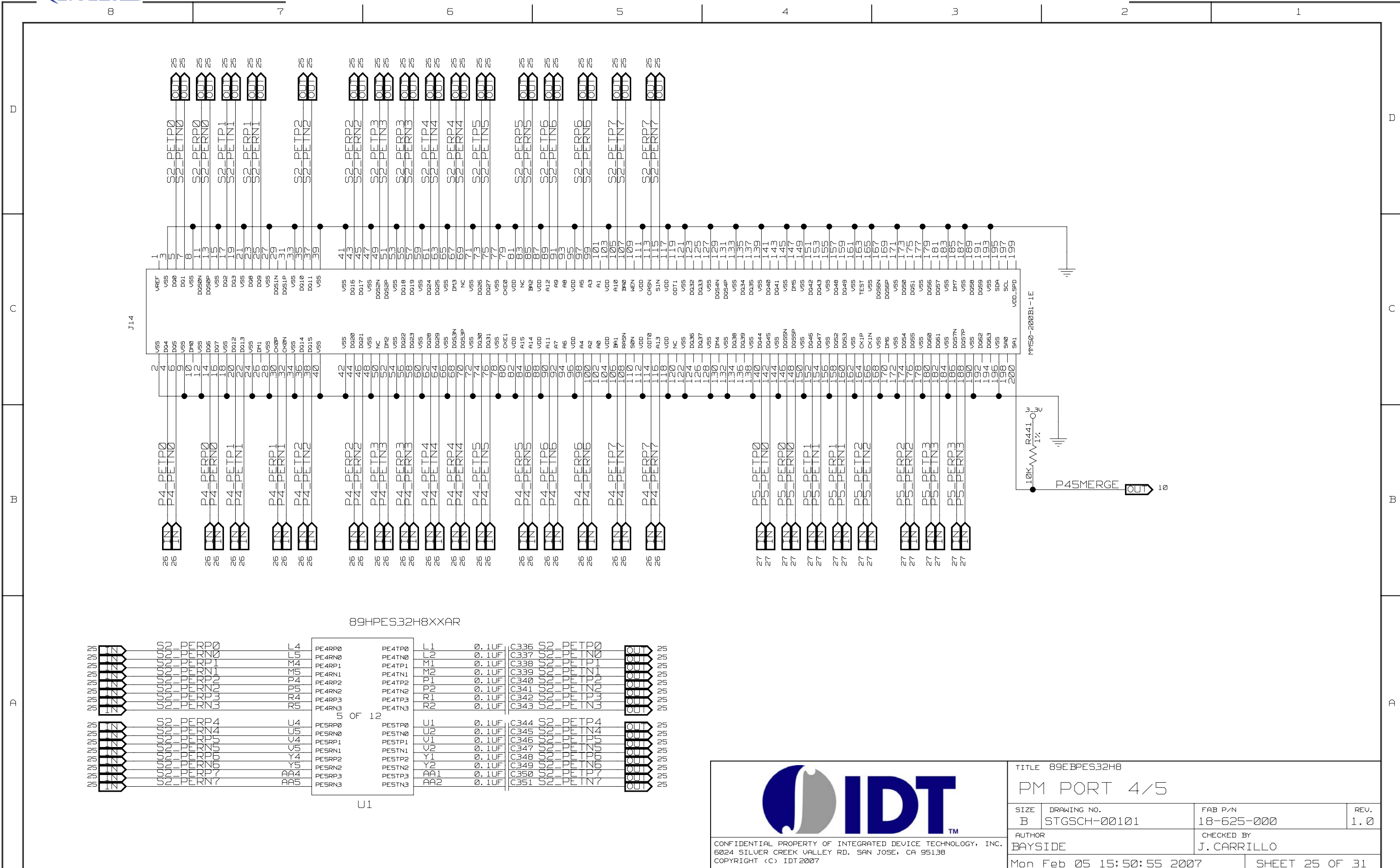
		TITLE 89EBPES32H8		
		PCI EXPRESS CONN PORT 2		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	STGSCH-00101	18-625-000	1.0	
AUTHOR		CHECKED BY		
BAYSIDE		J. CARRILLO		
Mon Feb 05 15:50:57 2007		SHEET 23 OF 31		

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 5024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



		TITLE 89EBPES32H8		
		PCI EXPRESS CONN PORT 3		
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0	
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO		
Mon Feb 05 15:50:58 2007			SHEET 24 OF 31	

CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007



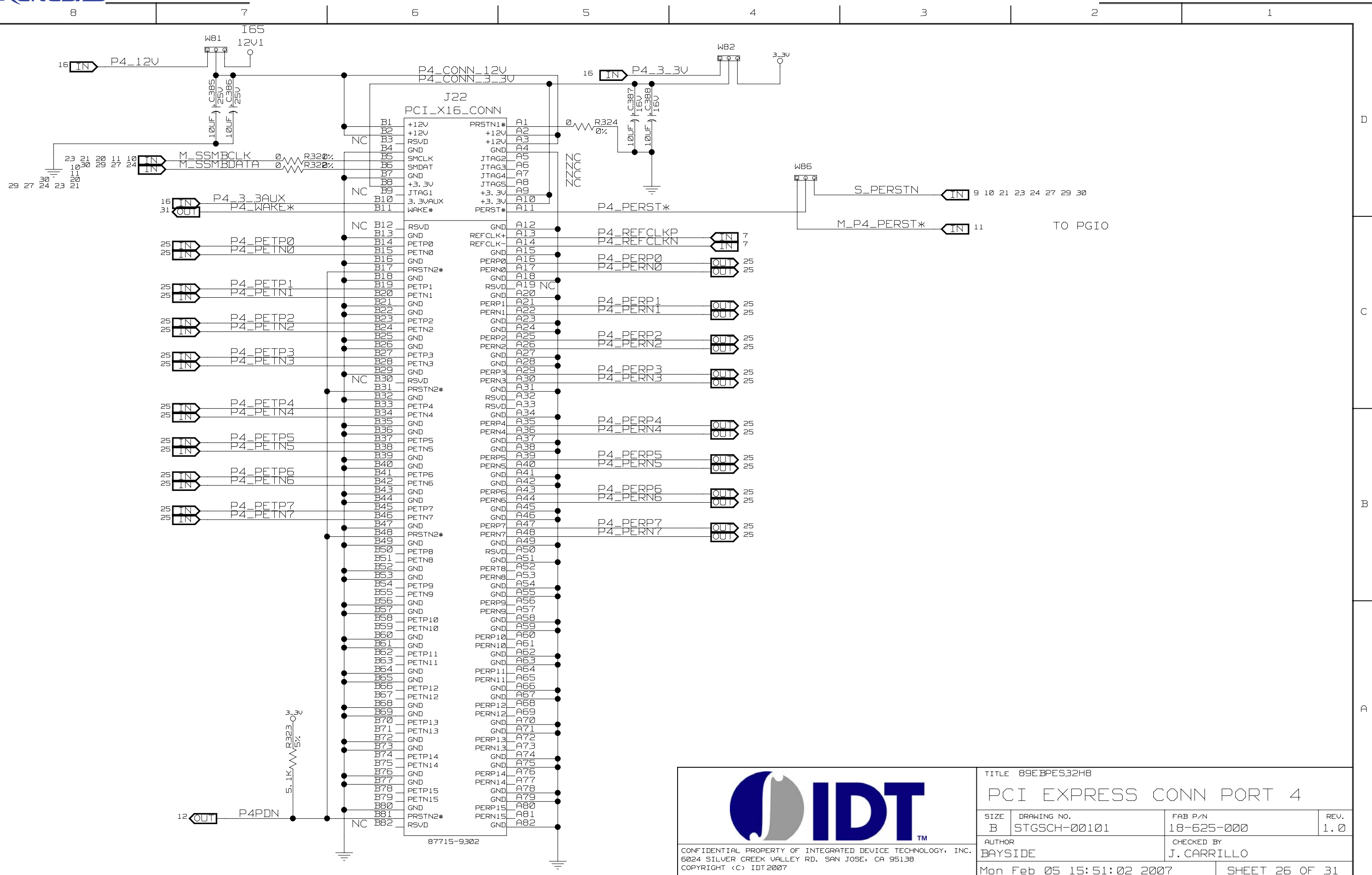
89HPES32H8XXAR

25	PE4RP0	PE4TP0	L1	0.1UF	C336	25
25	PE4RN0	PE4TN0	M1	0.1UF	C337	25
25	PE4RP1	PE4TP1	M2	0.1UF	C338	25
25	PE4RN1	PE4TN1	P1	0.1UF	C339	25
25	PE4RP2	PE4TP2	P2	0.1UF	C340	25
25	PE4RN2	PE4TN2	R1	0.1UF	C341	25
25	PE4RP3	PE4TP3	R2	0.1UF	C342	25
25	PE4RN3	PE4TN3	R3	0.1UF	C343	25
25	PE5RP0	PE5TP0	U1	0.1UF	C344	25
25	PE5RN0	PE5TN0	U2	0.1UF	C345	25
25	PE5RP1	PE5TP1	V1	0.1UF	C346	25
25	PE5RN1	PE5TN1	V2	0.1UF	C347	25
25	PE5RP2	PE5TP2	Y1	0.1UF	C348	25
25	PE5RN2	PE5TN2	Y2	0.1UF	C349	25
25	PE5RP3	PE5TP3	AA1	0.1UF	C350	25
25	PE5RN3	PE5TN3	AA2	0.1UF	C351	25

U1

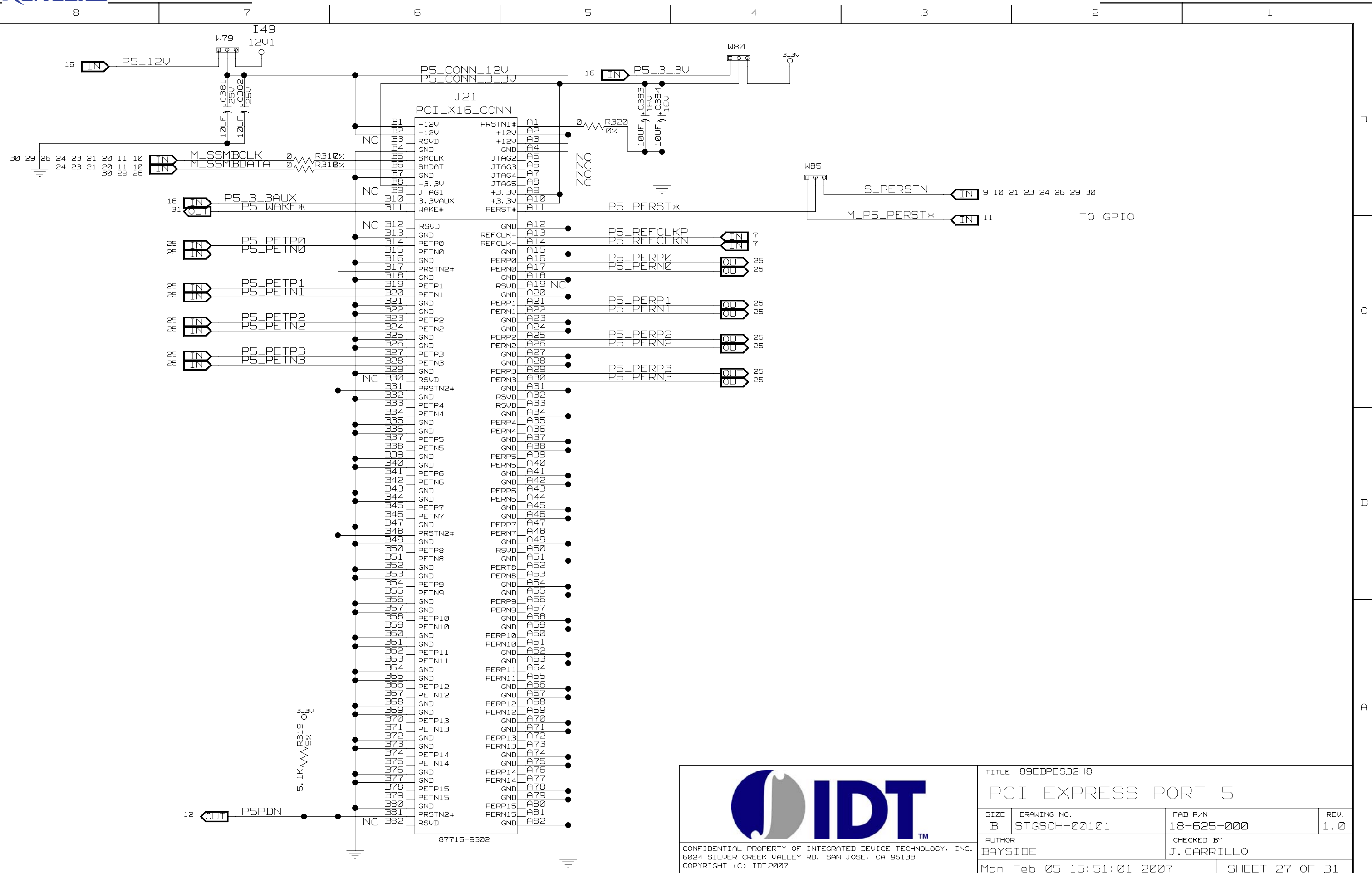
CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007


TITLE 89EBPES32H8			
PM PORT 4/5			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:50:55 2007			SHEET 25 OF 31



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

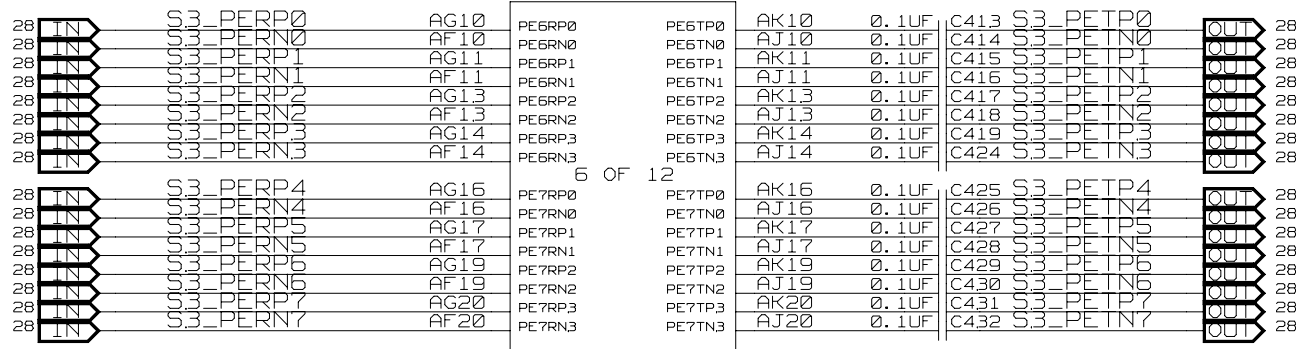
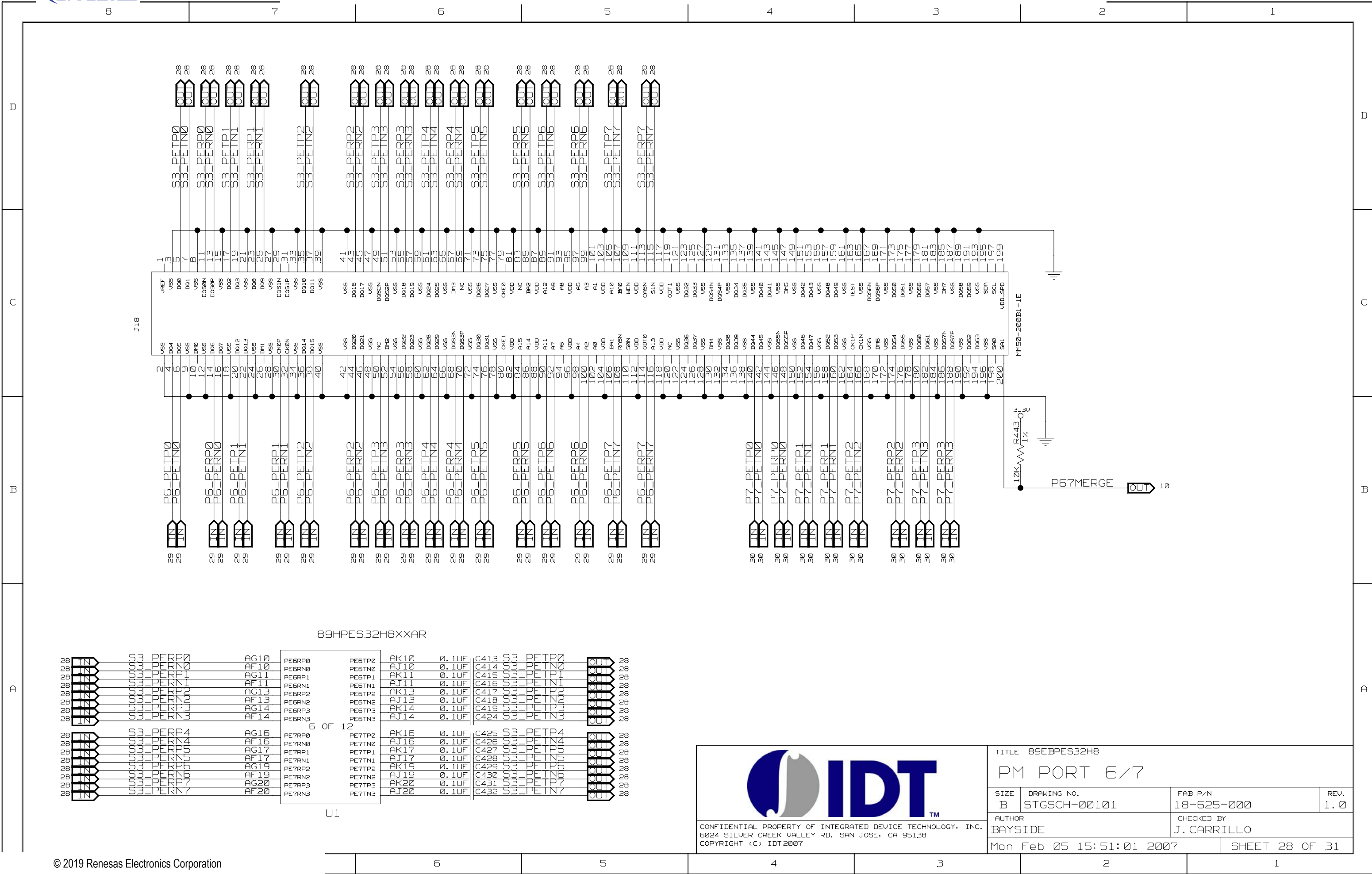
TITLE 89EBPES32H8			
PCI EXPRESS CONN PORT 4			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:51:02 2007			SHEET 26 OF 31





CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
PCI EXPRESS PORT 5			
SIZE	DRAWING NO.	FAB P/N	REV.
A	STGSCH-00101	18-625-000	1.0
AUTHOR		CHECKED BY	
BAYSIDE		J. CARRILLO	
Mon Feb 05 15:51:01 2007			SHEET 27 OF 31

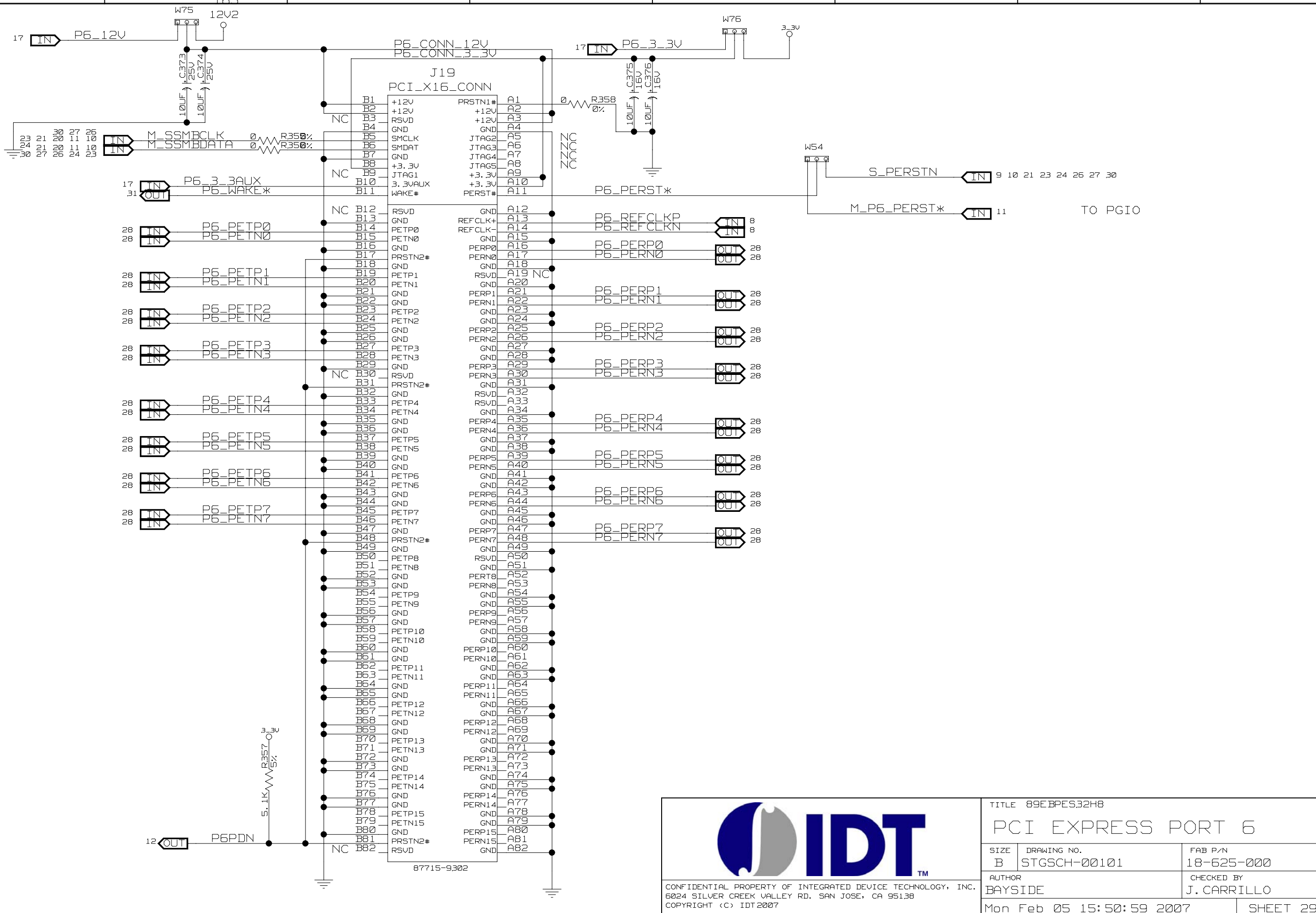


CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES.32H8			
PM PORT 6/7			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:51:01 2007			SHEET 28 OF 31

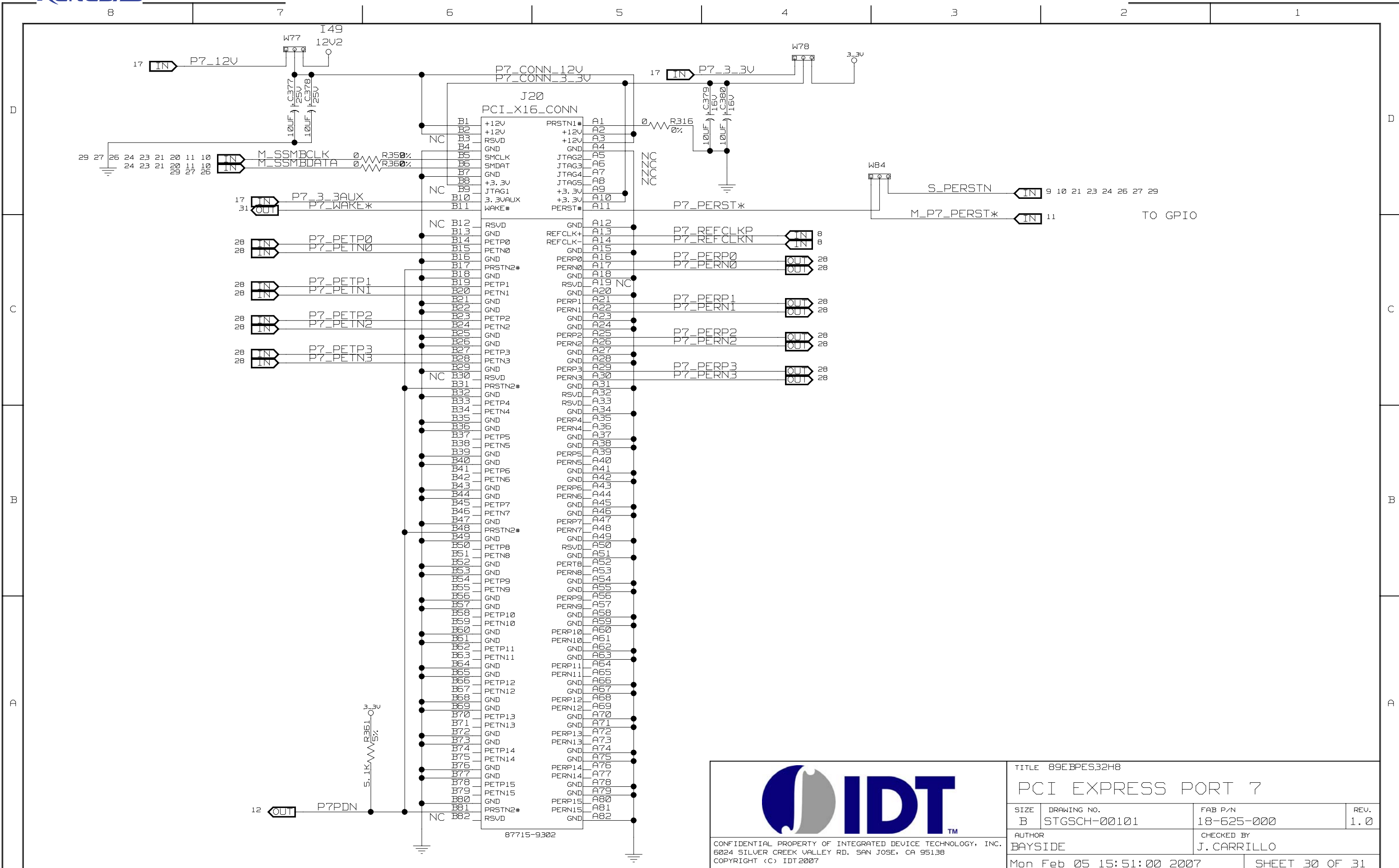


8 7 6 5 4 3 2 1



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 5024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
PCI EXPRESS PORT 6			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:50:59 2007			SHEET 29 OF 31





8 7 6 5 4 3 2 1

D

C

B

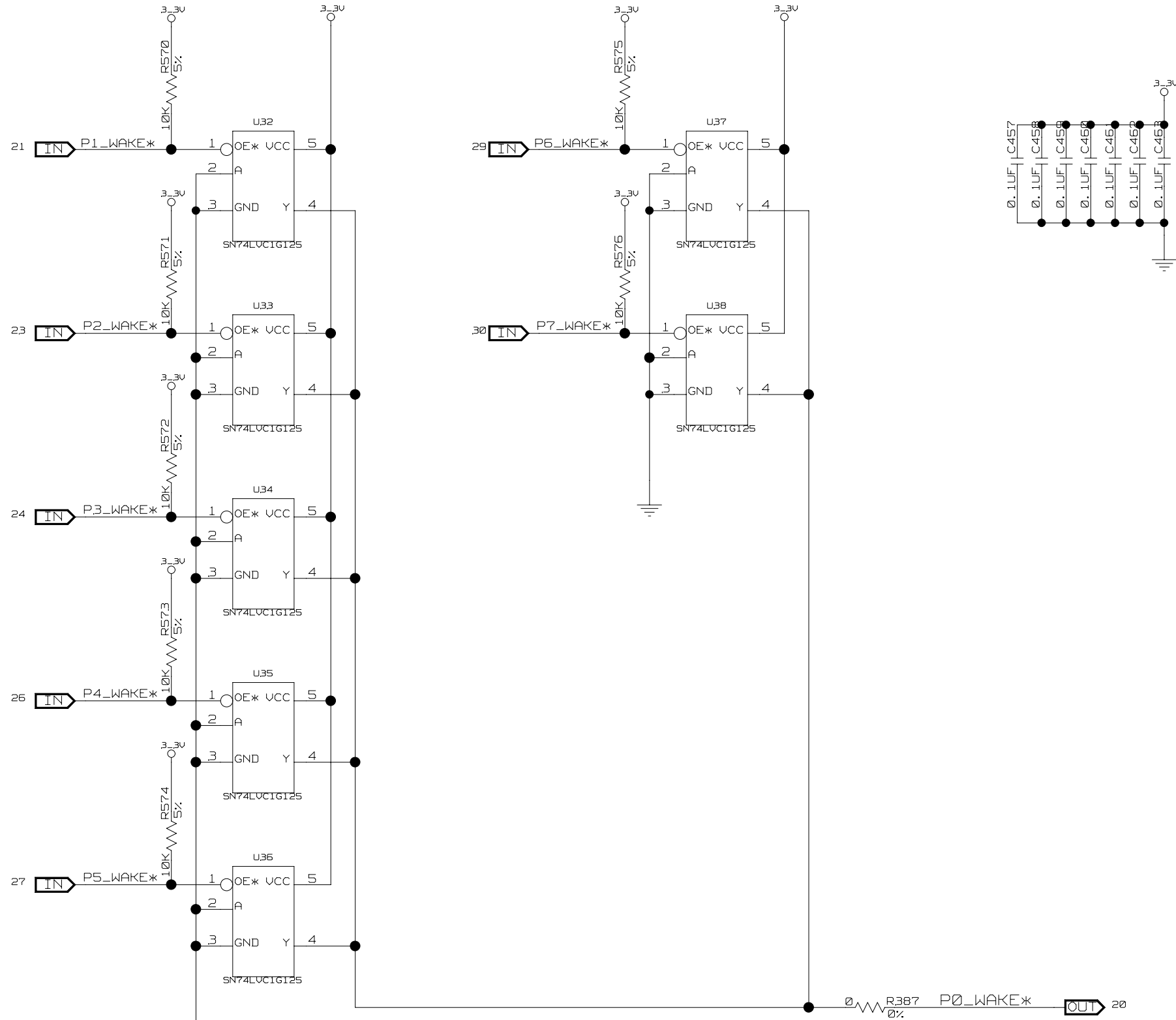
A

D

C

B

A



CONFIDENTIAL PROPERTY OF INTEGRATED DEVICE TECHNOLOGY, INC.
 6024 SILVER CREEK VALLEY RD. SAN JOSE, CA 95138
 COPYRIGHT (C) IDT2007

TITLE 89EBPES32H8			
WAKE			
SIZE B	DRAWING NO. STGSCH-00101	FAB P/N 18-625-000	REV. 1.0
AUTHOR BAYSIDE		CHECKED BY J. CARRILLO	
Mon Feb 05 15:51:03 2007			SHEET 31 OF 31

8 7 6 5 4 3 2 1

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.