LVPECL / LVDS Termination

APPLICATION NOTE

Introduction

Systems requiring higher clock and data rates are often configured using differential signals to enable higher speeds, better noise rejection and lower EMI. Differential signals, though, require special termination to ensure proper integrity and functionality.

This application note will focus on frequently used DC and AC coupled termination options for LVPECL and LVDS output signals. The topologies described below represent typical configurations for LVPECL and LVDS outputs and are recommended only as a guideline.

LVPECL Termination

Standard Termination

Shown below in Figure 1 is the standard LVPECL termination.

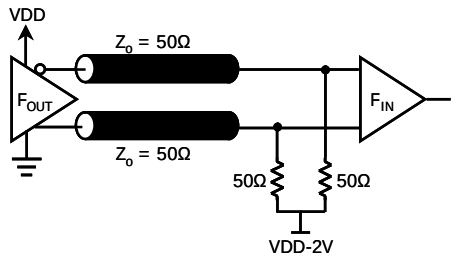

Figure 1

The F_{OUT} signals are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines.

This standard termination scheme is often found on characterization test and evaluation boards, but rarely found on actual system level boards. This is because implementation of this architecture would require an additional VTT = VDD– 2v (1.3V for 3.3V systems) regulator or power supply which would increase the cost and complexity of the final design. Nevertheless, the architecture described in Figure 1 is the reference that all variations of LVPECL termination are based.

Thevenin Termination

A more simplified approach is shown in Figure 2. This method eliminates the need for the additional power supply.

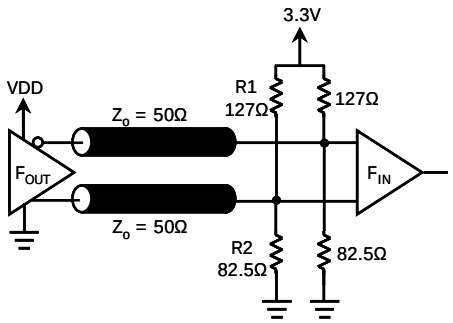

Figure 2

In the circuit of Figure 2, a Thevenin resistor divider is used to generate the appropriate termination offset voltage and is a widely used termination approach for 3.3V LVPECL drivers. The disadvantage to this architecture is that the Thevenin transformation results in requiring two 1% resistors, 82.5 and 127 Ohms for each termination. 82 and 130 Ohms 5% resistors are therefore more commonly found on system boards where tight tolerances are not critical.

Thevenin resistor values can be calculated for any VDD by solving for two conditions at the receiver: (1) the resulting parallel resistor combination must equal 50 ohms and (2) the DC termination voltage must equal VDD-2V.

$$R1 \parallel R2 = 50\Omega \quad (1)$$

$$(VDD - 2V) = VDD\left(\frac{R2}{R1 + R2}\right) \quad (2)$$

Solving the above equation for 2.5V systems produces ideal Thevenin equivalent resistor values of 62.5 and 250 ohms. Commercial 5% E24 resistor tolerances would require 62 and 240 ohm as a practical alternative.

Y - Termination

Another common termination approach is the simplified 3 resistor Y-termination shown below in Figure 3.

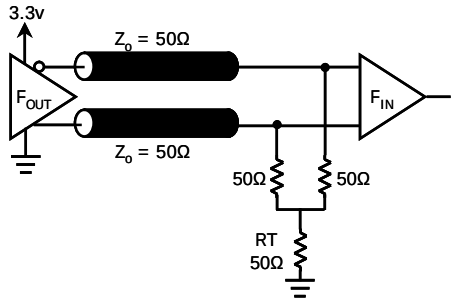

Figure 3

When compared to the four resistor Thevenin termination, the 3-resistors termination scheme is often preferred due to its simplicity and incremental advantages. It slightly improves on power savings, reduces component count, and consolidates all resistors to a single value in 3.3v systems. The single 50 Ohm resistor to ground sets the VDD-2V level at the three resistor junction. Note that although 50 Ohms is used in Figure 3 above, this only applies to 3.3v systems. RT = 18 ohms is used commonly in 2.5v applications.

LVDS Termination

The LVDS output termination architecture is very simple and efficient. Unlike LVPECL, no external DC biasing is necessary when connecting to an LVDS receiver. In addition, the receiver input may sometimes include its own internal termination resistor, eliminating the need for external termination.

Standard DC Termination

Figure 4 illustrates the layout for a typical 2.5V and 3.3V LVDS termination. Typically a single 100 ohm resistor is shunted across the receiver input pins, but two 50 ohm series resistors (shown here) are sometimes used for measurement purposes.

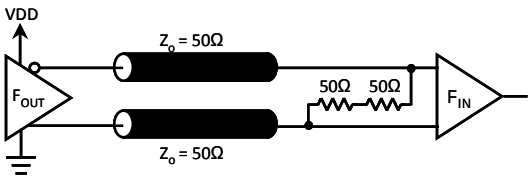

Figure 4

Interfacing to 50Ω Test Equipment

Split Supply Termination (LVPECL)

Although rarely used in end applications, split power supply termination is often used to take advantage of the internal 50 Ohms termination of an oscilloscope or a frequency counter.

Since the LVPECL offset voltage is VDD – 2V, shifting VDD down by 1.3V (3.3V – 2V = 1.3v) yields VTT = 0 V or Ground. This is shown in Figure 5 with the associated power supply configuration.

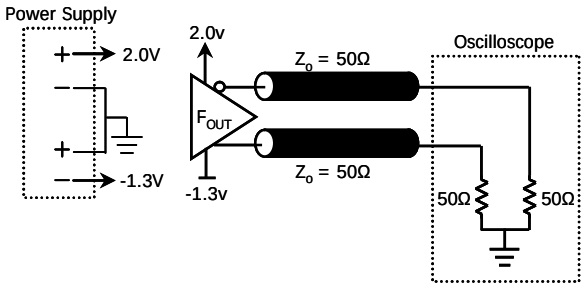

Figure 5

Note that in the above configuration, the power supply and oscilloscope are both tied to the same reference potential (GND), but that the Device Under Test (DUT) is independent of GND (0V) and powered by +2.0V and -1.3V only.

AC Termination (LVPECL)

AC coupling can be used to terminate LVPECL signals through 50Ω to the test equipment GND. In this configuration, capacitors are used to split the DC and AC components of the LVPECL output.

A resistor (R1) terminated to GND provides the LVPECL emitter follower output stage with the required DC path to ground. The value of this resistor is not critical as it only serves to bias the emitter follower output stage. Typically between 130 to 200 ohms is selected to approximate the 25 to 30mA output bias current when terminated through 50 ohms to Vtt.

As can be seen in Figure 6, the resistor provides a constant DC load while the 50 ohm termination in parallel provides the sink/source path for AC currents. Capacitor values should be chosen to meet the required clock speeds.

Because large capacitors appear inductive at higher frequencies, it may be necessary to place a small capacitor in parallel to prevent undesired signal degradation.

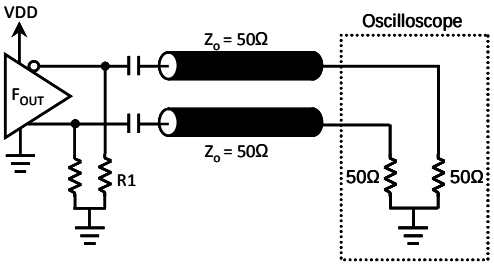

Figure 6

AC Termination (LVDS)

AC coupling of LVDS is as simple as placing inline coupling capacitors at the source. The output signal can now be fed directly into the internal 50 ohm test equipment termination to ground. See Figure 7 below.

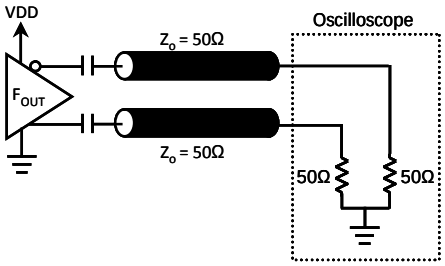

Figure 7

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
+1 408-284-8200
Fax: 408-360-1738

Technical Support
MEMS_Support@idt.com
www.idt.com/go/MEMS