

From the Computing and Multimedia Division of Integrated Device Technology, Inc.

Overview

High performance clock buffers are widely used in digital consumer and communications applications for distribution of clock signals. A critical parameter for these buffers is Additive phase noise that can degrade system performance and reliability. This application note briefly explains the theory behind measuring additive phase noise for IDT clock buffers and summarizes the additive phase jitter results for several widely used IDT clock buffers. Other AC parameters of interest for buffers are input to output propagation delay and output to output skew. For tighter skew requirements refer to the application note on [zero delay buffers](#).

Introduction

In synchronous systems where timing and performance of the system is dependent on the clock, integrity of the clock signal is important. Designers must optimize board layout, use clean power supplies and follow recommended decoupling and termination schemes for the outputs in order to meet the EMI and timing budgets for their application.

IDT has a large variety of low skew clock distribution devices to meet all your application needs. Figure 1 shows a typical set top box application where an IDT clock buffer is used to distribute 33 MHz PCI clocks to multiple PCI slots.

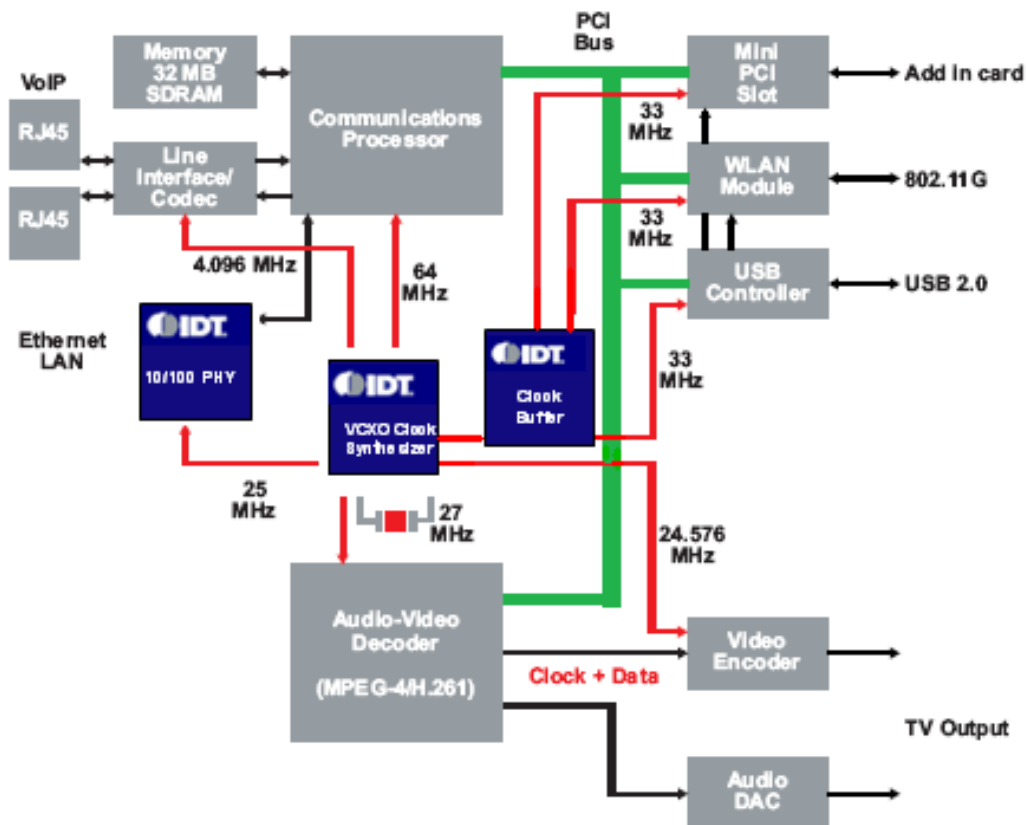


Figure 1. Set Top Box Application Diagram using IDT Clock Buffer

Phase Noise Measurement

Phase Noise is the frequency domain representation of fluctuations in the phase of a waveform due to jitter. It is measured using a Phase Noise Analysis system such as Aeroflex and is usually expressed in dBc/Hz at various offsets from the carrier frequency.

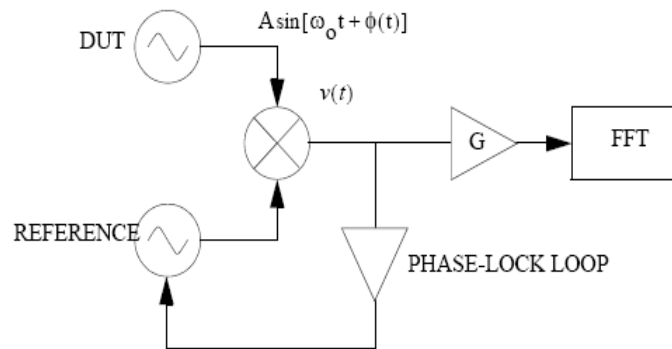
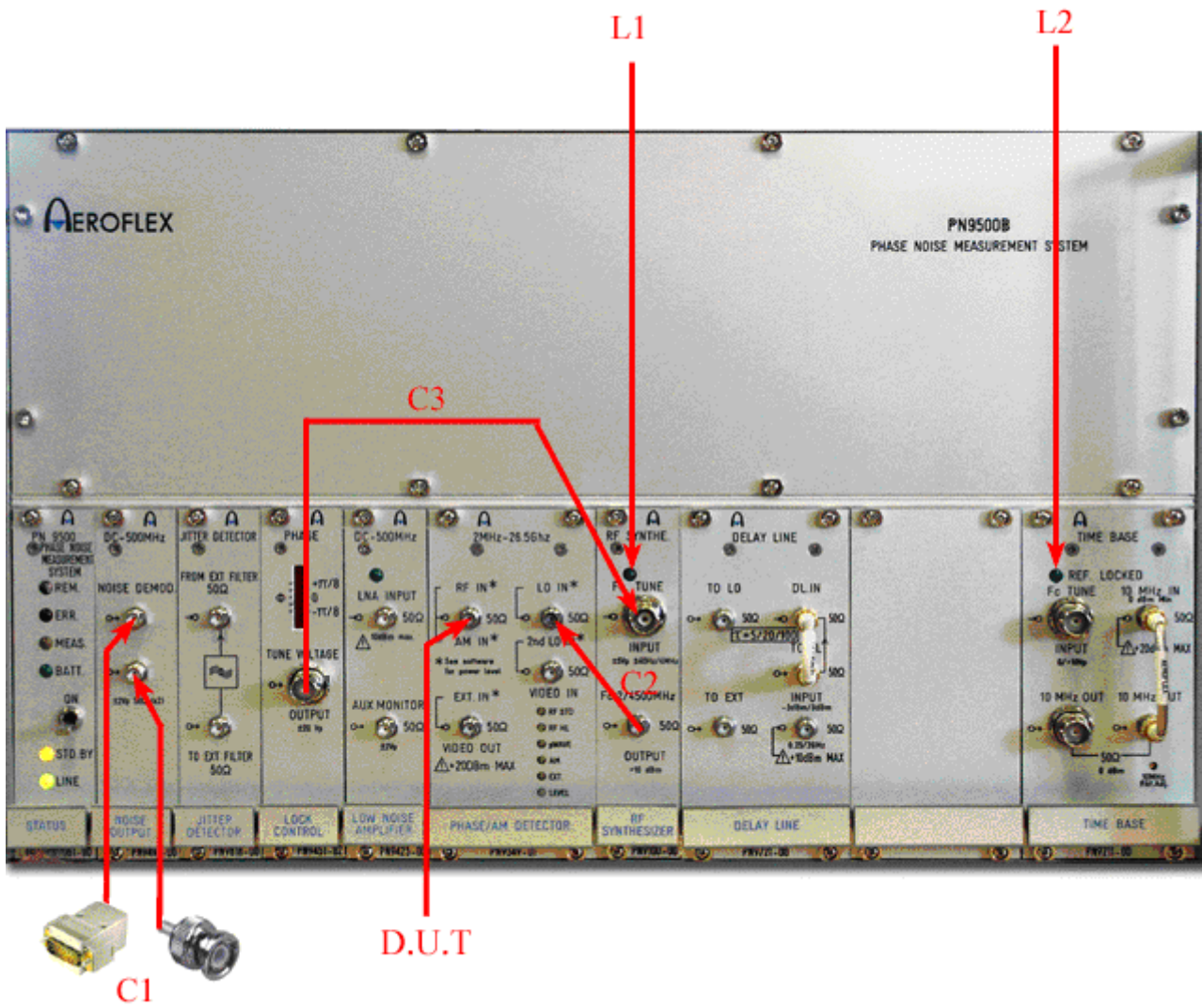


Figure 2. Block Diagram of PN-9000

Figure 2 shows a simplified block diagram of the Aeroflex PN-9000 system. The PN-9000 demodulates the phase fluctuations of the source under measurement by means of a quadrature locked low noise reference signal. A balanced mixer functions as a phase comparator and produces a signal which comprises of the time representation of the phase fluctuations of the source. The reference is held in phase quadrature with respect to the DUT output frequency by means of the control voltage produced by the phase locked loop. A low noise amplifier with auto-gain feature will adjust the noise level to the optimum dynamic range of the digitizing board. The FFT calculation is done on a companion board located in the computer to which the PN9000 system is connected to and the resulting phase noise is displayed on the monitor hooked up to the computer.

Setup for Measuring Phase Noise using Aeroflex PN9000



Additive Phase Noise

Any component in a signal chain has some amount of noise at its output that is generated internally (not including the contribution due to the external reference noise at the input). It is useful to measure the phase noise at the output of a device in such a way that the phase noise of any external source is cancelled out. The phase noise so measured is specified as the additive phase noise of the device. It is the amount of phase noise that the device (clock buffer in our case) adds to the signal chain.

IDT clock buffers have ultra low additive phase jitter thereby allowing system designers to distribute multiple copies of a clean clock to other devices on their system. The clock signal integrity is maintained thereby eliminating the need for additional jitter cleaning components. By considering the phase noise contribution due to the buffer alone, it is then possible to foretell the degree to which the buffer impacts the total system phase noise when used in conjunction with components such as oscillators and clock sources, each of which contribute to the phase noise of the total system. In many cases, the phase noise of one element in the chain dominates the system phase noise.

Additive Phase Noise Measurement

The measurement setup for additive phase noise (Figure 3) differs a little bit from the phase noise setup that we saw in Figure 1. The PN9000 RF Synthesizer is programmed to output a frequency that is equal to the DUT (IDT clock buffer) input frequency. The Synthesizer output frequency is then passed through a power splitter. One of the outputs of the splitter is fed into a manual phase shifter while the other is the input to the DUT. The output of the DUT is connected to RF IN port and the output of the manual phase shifter is connected to the LO IN port. The phase quadrature between the LO and RF inputs is ensured by setting the phase correctly using the external manual phase shifter. The assumption in this case is that the PN9000 reference synthesizer has a very low phase noise and its contribution to the overall DUT phase noise is negligible. This ensures that the measured phase noise will be purely due to the DUT.

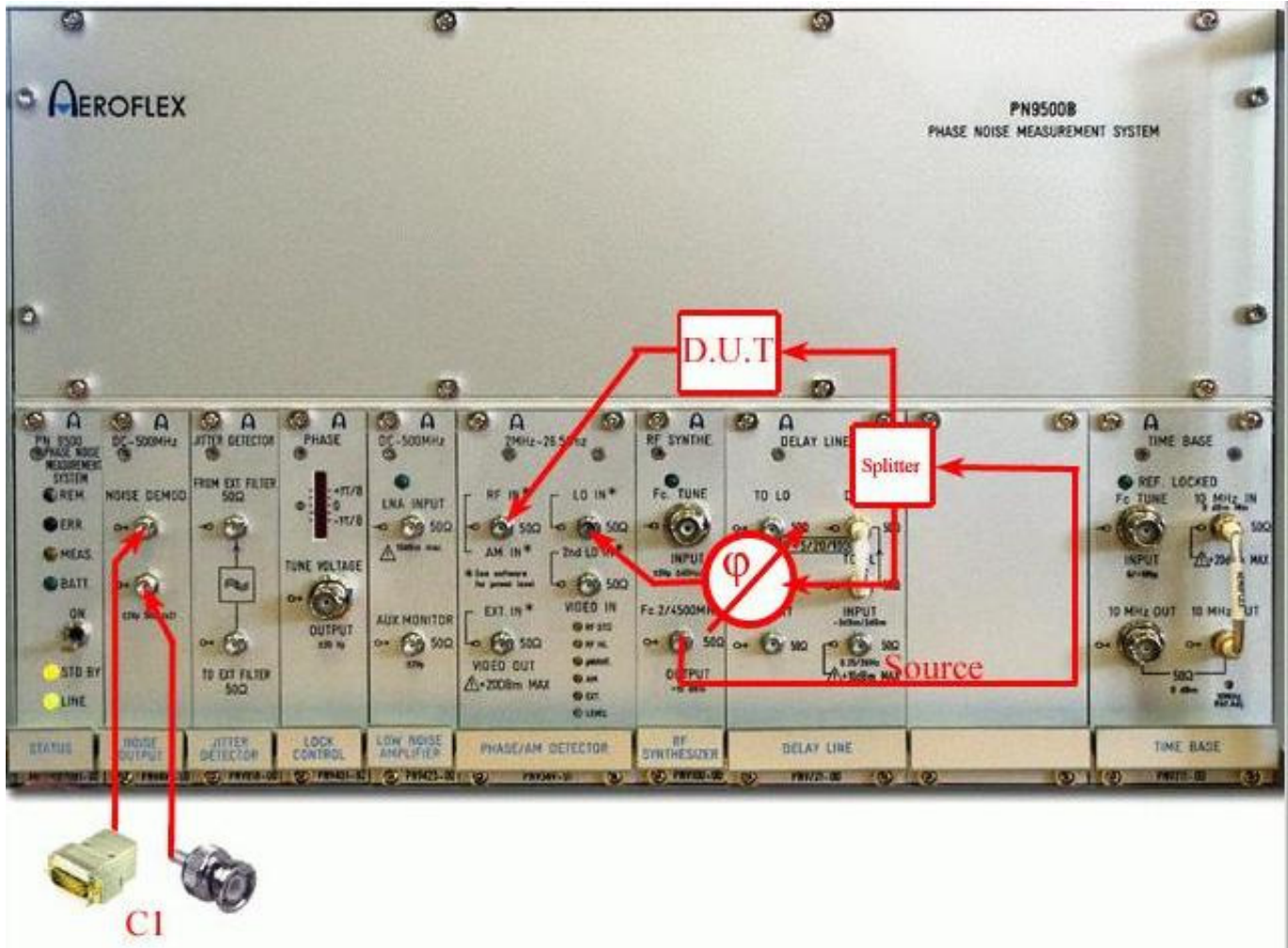


Figure 3. Additive Phase Noise Measurement Setup

Additive Phase Jitter (RMS) Results

Measurements for additive phase jitter (RMS) were taken on six of the most widely used IDT Clock Buffers at three frequencies: 25 MHz, 100 MHz and 125 MHz. All measurements contained in this report are taken at room temperature. All devices unless stated otherwise are operated at VDD = 3.3 V (Figure 2, 3, 4, 5). Measurements for additive phase jitter over a VDD range of 1.8 V - 3.3 V have been taken for ICS524 clock buffer (Figure 6). Table 1 summarizes additive phase jitter measurement results for various IDT clock buffers at different input frequencies. Table 2 shows the summary of additive phase jitter results taken on ICS524 clock buffer over the device operating voltage range.

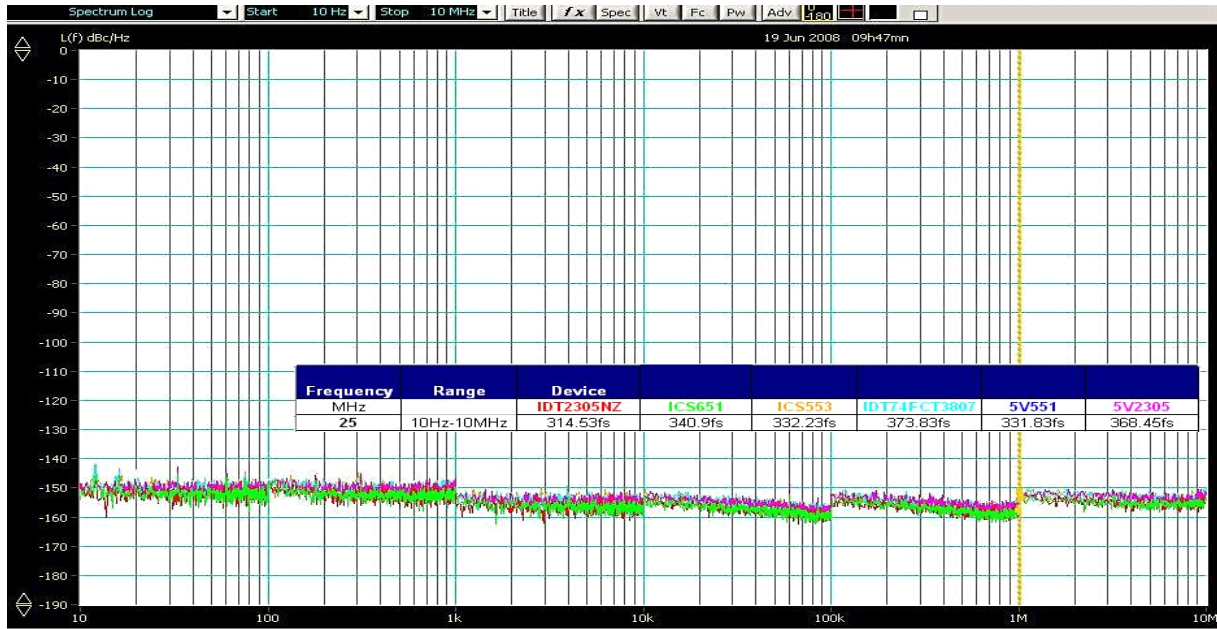


Figure 4. Additive Phase Noise Measurements 25 MHz

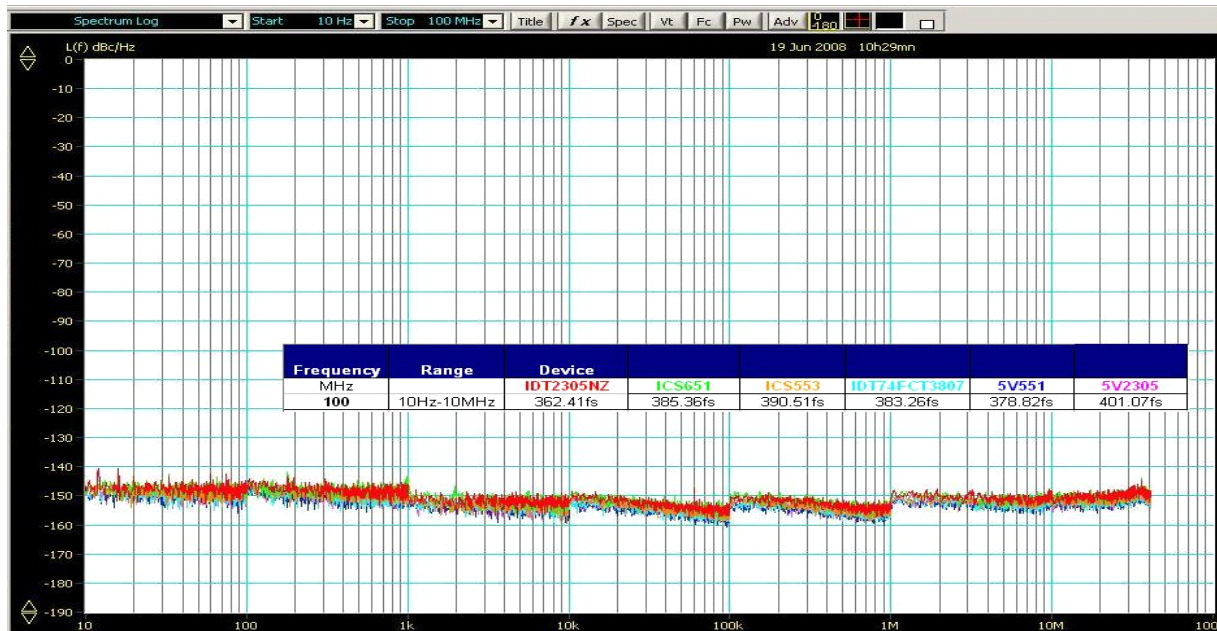


Figure 5. Additive Phase Noise Measurements 100 MHz

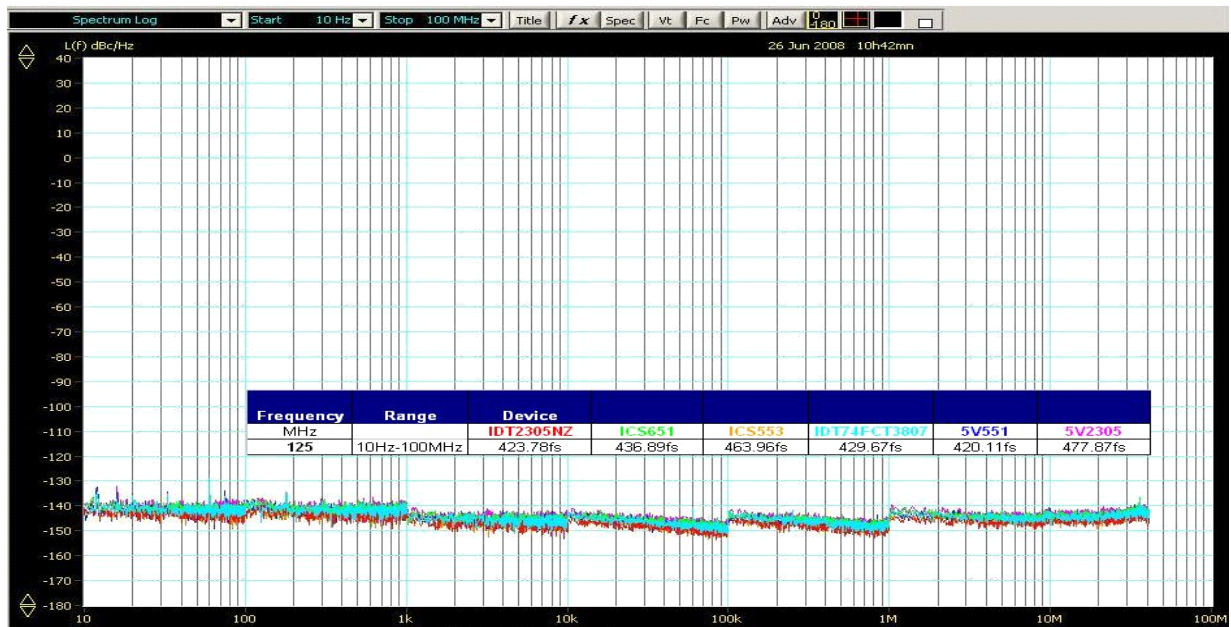


Figure 6. Additive Phase Noise Measurements 125 MHz

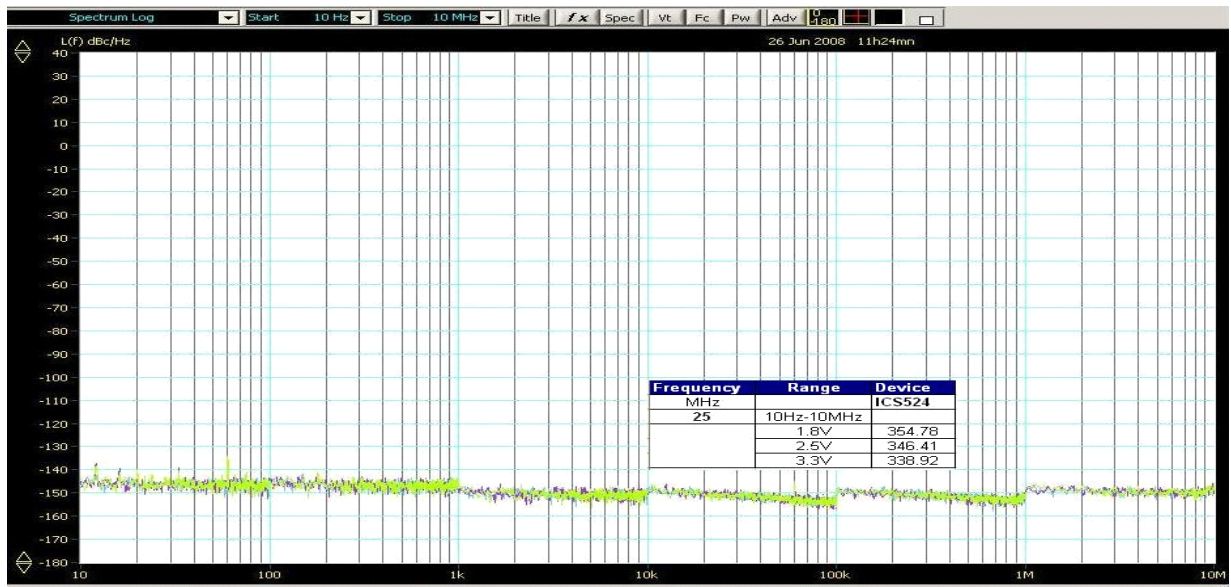


Figure 7. Additive Phase Noise Measurement of ICS524 Over VDD Range of 1.8 V - 3.3 V

Additive Phase Jitter (RMS) Summary of Results

Figures 4, 5, 6 and 7 plot the single sideband phase noise distribution for the buffers. The maximum offset from the carrier frequency for the measurements is limited by the range of the instrument. The total noise power of the sidebands can be determined by integrating the phase noise plot over the frequency band of interest. The RMS phase jitter values reported in figures (4, 5, 6, 7) and tables (1, 2) are in femto seconds.

$$N = \text{Noise Power} = \int_{F1}^{F2} L(f) df$$

F1 = Lower Frequency of Interest

F2 = Upper Frequency of Interest

L(f) = phase noise distribution function

$$\text{RMS Phase Jitter (radians)} = (10^{(N/10)})^{0.5} * 2$$

$$\text{RMS Phase Jitter (secs)} = \text{Jitter (radians)} / (2 * \pi * F_c)$$

F_C = Carrier Frequency

Table 1: Additive Jitter of IDT Clock Buffers Over Frequency Range

Frequency	Range	Device					
MHz		IDT2305NZ	ICS651	ICS553	IDT74FCT3807	5V551	5V2305
25	10 Hz - 10 MHz	314.53 fs	340.9 fs	332.23 fs	373.83 fs	331.83 fs	368.45 fs
100	10 Hz - 10 MHz	362.41 fs	385.36 fs	390.51 fs	383.26 fs	378.82 fs	401.07 fs
125	10 Hz - 100 MHz	423.78 fs	436.89 fs	463.96 fs	429.67 fs	420.11 fs	477.87 fs

Table 2: Additive Jitter of ICS524 Over Voltage Range

Frequency	Range	Device
MHz		ICS524
25	10 Hz - 10 MHz	
	1.8 V	354.78 fs
	2.5 V	346.41 fs
	3.3 V	338.92 fs

In Conclusion

The additive phase-noise measurement results presented in the application note confirm ultra low additive phase jitter across IDT family of clock buffers. The additive phase jitter varies minimally over the buffer input frequency range and operating voltage range.

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