To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

Customer Notification

QB-78K0LX2™

In-Circuit Emulator

Operating Precautions

Target devices
78K0/LE2
78K0/LF2
78K0/LG2

Global Document No. U18120EE2V0IF00 (2nd edition)
Document No. TPS-LE-OP-TQBLX2-2
Date Published March 2006

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Table of Contents

QB-78K0LX2

(A) Table of Operating Precautions

No.	Outline	Control Code Notes 1, 2	QB-78K0LX2		
			A	B	
1	Caution on LCD voltage, when using internal voltage booster (Technical Limitation)		✗	✓	
2	Caution on target voltage during break (Direction of use)		✗	✗	
3	Support of specification change for option byte (Technical Limitation)		✗	✓	
4	Caution on power-on-clear function (Direction of use)		✗	✗	

✓ : Not applicable
✗ : applicable

Notes:
1. The “control code” is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.

2. Form control code “B” onwards a realchip (uPD78F0547 V2.0) is used.

Caution: Pls. refer to and consider the Operating Precautions mentioned in the Customer Notifications of the according devices, to which this Emulator belongs to.

(B) Description of Operating Precautions

No. 1	Caution on LCD voltage, when using internal voltage booster (Technical Limitation)
	When the internal voltage booster of the LCD function is used (VLCON = 1), a LCD drive voltage (V_{LC0},V_{LC1},V_{LC2}) is approximately 20% lower than the typical value. This behavior will be corrected in the next version.

No. 2	Caution on target voltage during break
	Do not decrease the target voltage during a break. If a reset by LVI or POC occurs during a break, the debugger operation may become illegal or a communication error may occur.

No. 3	Support of specification change for option byte (Technical Limitation)
	Details The POC mode (POCMODE) of the option byte is available in control code B or later. Please refer also to item No. 4 “Caution on power-on-clear function.

No. 4	Caution on power-on-clear function (Direction of use)

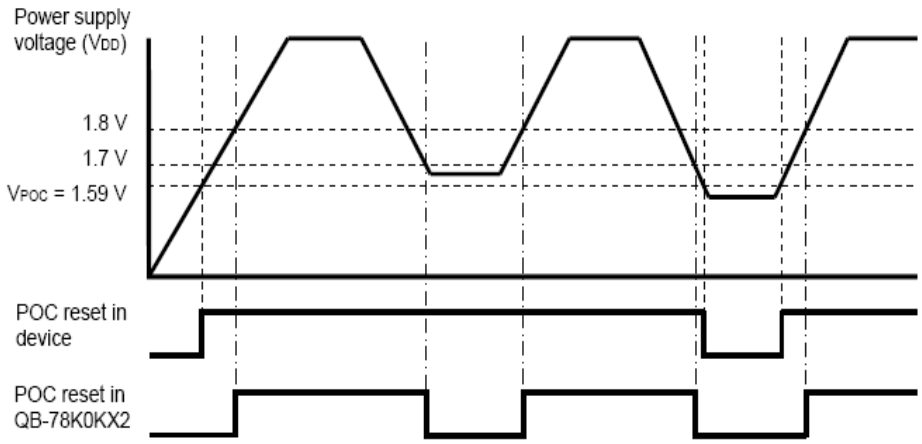
Details

The POC detection voltage differs between the QB-78K0LX2 and the device.

1. In 1.59 V POC mode (option byte: POCMODE = 0)

- Device: An internal reset signal is generated at power application, and the reset state is released when the power supply voltage (V_{DD}) exceeds the detection voltage (V_{POC} = 1.59 V ±0.15 V).
  The power supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared, an internal reset signal is generated when V_{DD} drops lower than V_{POC} (V_{DD} < V_{POC}), and the reset state is released when V_{DD} becomes V_{POC} or higher (V_{DD} ε V_{POC}).

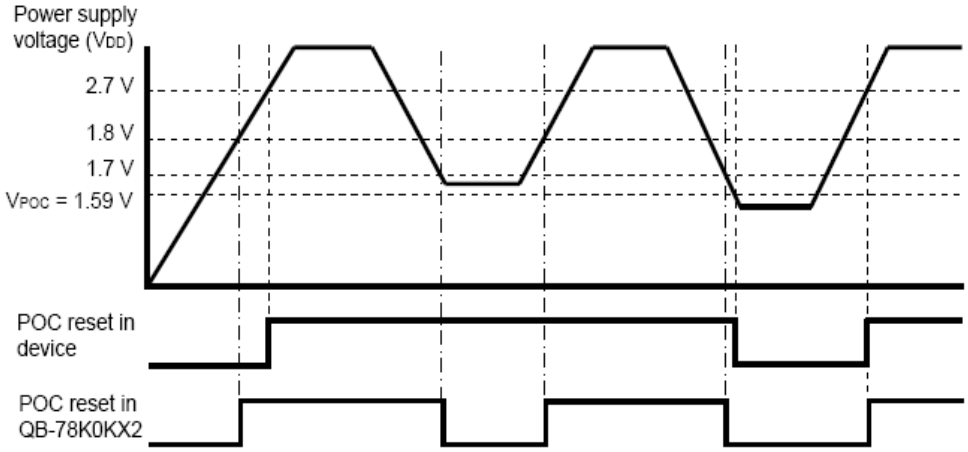
- QB-78K0LX2: An internal reset signal is generated at power application, and the reset state is released when the power supply voltage (V_{DD}) exceeds 1.80 V. An internal reset signal is generated when V_{DD} drops lower than 1.70 V (V_{DD} < 1.70 V), and the reset state is released when V_{DD} becomes 1.80 V or higher (V_{DD} ε 1.80 V).



2. In 2.7 V/1.59 V POC mode (option byte: POCMODE = 1)

- Device: An internal reset signal is generated at power application, and the reset state is released when the power supply voltage (V_{DD}) exceeds V_{POC} (power detection voltage at power application; V_{POC} = 2.7 V ±0.2 V).
  The power supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared, an internal reset signal is generated when V_{DD} drops lower than V_{POC} (V_{DD} < V_{POC}), and the reset state is released when V_{DD} becomes 2.7 V or higher (V_{DD} ε 2.7 V).

- QB-78K0LX2: An internal reset signal is generated at power application, and the reset state is released when the power supply voltage (V_{DD}) exceeds 1.80 V.
  An internal reset signal is generated when the detection voltage (V_{POC} = 1.59 V ±0.15 V) < V_{DD} < 1.70 V, and the reset state is released when V_{DD} becomes 1.80 V or higher (V_{DD} ε 1.80 V).
  If the power supply voltage (V_{DD}) drops to a level of the detection voltage (V_{POC} = 1.59 V ±0.15 V), the reset state is released the next time the power supply voltage (V_{DD}) exceeds V_{POC} (power detection voltage at power application; V_{POC} = 2.7 V ±0.2 V).



(C) Valid Specification

Item	Date published	Document No.	Document Title
1	March, 2005 or later	U17468EJ	User's Manual

(D) Revision History

Item	Date published	Document No.	Comment
1	June 28, 2004	TPS-LE-OP-TQBLX2-1	1st Release
2	March 2006	TPS-LE-OP-TQBLX2-2	2nd Release new control code