JEDEC STANDARD

JEDEC Dictionary of Terms for Solid-State Technology — 6th Edition

JESD88E

(Revision of JESD88D, December 2009)

JUNE 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Foreword

This dictionary was originally prepared and edited by a special Working Group consisting of JEDEC consultants Fred A. Mann and Frank S. Stein, under the direction of the JEDEC Board of Directors, and is periodically updated by JEDEC Committee JC-10 on Terms, Definitions, and Symbols. After the 1st edition, regular contribution has been made by David Sweetman. Publication of the JEDEC Dictionary was approved by the JEDEC Board of Directors under Ballot JCB-00-97.

This Sixth Edition includes definitions from 14 standards that were not included in the Fifth Edition plus revised definitions from 26 additional publications and standards that have been updated. All reported errors and necessary rewording have been taken into account.

Introduction

As new or revised JEDEC and EIA publications* are issued, their definitions are considered for inclusion in this dictionary. All publications with definitions in this edition of the dictionary are listed in Annex A. The following are often not included: (1) terms having a specialized meaning only within the context of a particular publication (usually a test method), e.g., "brush: A toothbrush with a handle made up of nonreactive material …"; and (2) concepts where the publication gives only a symbol and a term but no definition. This dictionary, like any dictionary, is primarily intended to define concepts. For an extensive list of symbols and abbreviations with the corresponding terms for many variations (dc, peak, rms, small signal, large signal, etc.), see JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

All entries are reviewed for punctuation, grammar, and clarity, as well as for accuracy, and reworded if such is considered warranted. If a definition is substantially recast, the date of the source publication is followed by a pound sign (#). The editors have made every effort to ensure that the *intent* of the original definition is retained in all cases. When the same term is defined in more than one source publication in substantially different words having essentially equivalent meanings, the formulation is selected that, in the opinion of the editors, is the most completely and clearly stated, and the pound sign is applied to the references to the other publications. If the same term is defined with different meanings in two or more publications, all forms are given in alphanumeric order by publication reference**.** The definitions are numbered (1), (2), … , but no order of preference is intended.

While most of the conventions used in this dictionary are self-explanatory, two may need further explanation: (1) Terms separated by semicolons (;) are synonyms. (2) Square brackets [ ] enclosing a part of a term and possibly parts of its definition indicate that the words placed between them may replace all or some of the preceding words. Selection of the bracketed part of the term requires the selection of the bracketed parts of the definition. This convention is used to show at first sight the construction of terms having parallel definitions.

* As used in this dictionary, the word "publication" is a generic term that includes standards.

Scope

Each term and definition in this dictionary has been included strictly for application within the solid-state industry. Many of the terms and definitions in this dictionary may have applicability beyond the scope of the JEDEC Solid State Technology Association; however, an assumption of such extended applicability is the responsibility of the user. The goal is to include the appropriate terms and definitions from all JEDEC publications and standards. At the present time, only terms and definitions from the publications listed in Annex A are included.

JEDEC DICTIONARY OF TERMS FOR SOLID-STATE TECHNOLOGY

Terms, abbreviations, letter symbols, and definitions **References**

A

A: See "port A; port B".

A; a: See "anode terminal".

abbreviation: A shortened form of a word or expression. JESD77D, 8/12
JESD99C, 12/12

ABD: See "avalanche breakdown diode".

ABD array: A device having three or more terminals and containing multiple diodes within a single package, with at least one of the diodes being an ABD. JESD77D, 8/12
JESD210, 12/07

NOTE ABD arrays can be classified as 1) devices with multiple discrete semiconductor chips; and 2) devices with multiple diode junctions diffused into a single semiconductor chip.

above-passivation layer (APL): A low-impedance metal plane, built on the surface of a die above the passivation layer, that connects a group of bumps or pins (typically power or ground). JS-001-2012, 4/12

NOTE This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

absolute accuracy error: Synonym for "total error". JESD99C, 12/12

absolute maximum rated junction temperature: The maximum junction temperature of an operating device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology. JESD22-A108D, 11/10#

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

absolute maximum rated temperature: The maximum junction or ambient temperature of an operating device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur. JESD89-1A, 10/07
JESD89-3A, 11/07

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

absolute maximum rated voltage: The maximum voltage that may be applied to a device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology. JESD22-A108D, 11/10#
JESD89-1A, 10/07#
JESD89-2A, 10/07#
JESD89-3A, 11/07#

absolute maximum rating: Synonym for "maximum rating". JESD77D, 8/12

ABTXXXXXX series: A BiCMOS series that includes devices whose input logic levels are TTL-compatible and whose outputs are specified at TTL levels. JESD54, 2/96

accelerated ELF test time (t_A): The duration of the accelerated ELF test. JESD74A, 2/07

accelerated equivalent soak: A soak at a higher temperature for a shorter time (compared to the standard soak) to provide roughly the same amount of moisture absorption. J-STD-020D.1, 3/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

accelerated soft error rate (ASER): A soft error rate in the presence of an intense ionizing radiation source. JESD89, 8/01

acceleration factor (*A*, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition. JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07# JESD85, 7/01# JESD91A, 8/01# JESD94A, 7/08

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used in place of the symbol *A*.

acceleration factor, stress (A_f): The acceleration factor due to the presence of some stress (e.g., current density, electric field, humidity, temperature cycling). JEP122G, 10/11 JEP143C, 7/12

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature. JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07#

NOTE 1 This is the acceleration factor most often referenced. The Arrhenius equation for reliability is commonly used to calculate the acceleration factor that applies to the acceleration of time-to-failure distributions for microcircuits and other semiconductor devices:

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp[(-E_{aa}/k)(1/T_1 - 1/T_2)]$$

where

E_{aa} is the apparent activation energy (eV);
k is Boltzmann's constant (8.62×10^{-5} eV/K);
T_1 is the absolute temperature of test 1 (K);
T_2 is the absolute temperature of test 2 (K);
λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});
λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1}).

NOTE 2 The best-fit linear slope of a plot of the natural log of the time-to-failure as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is equal to the apparent activation energy in electronvolts.

NOTE 3 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s.

acceleration factor, voltage (A_V): The acceleration factor due to changes in voltage. JEP143C, 7/12 JESD74A, 2/07

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

acceleration model: A mathematical formulation of the relationship between (1) the rate (speed) of a degradation mechanism or the time-to-failure and (2) the conditions or stresses that caused the degradation. JEP143C, 7/12 JEP148A, 12/08

acceptance inspection: A sampling inspection or series of sampling inspections used to determine the suitability of a lot of material for shipment. JESD16-A, 4/95

accept number: The maximum number of nonconforming components in the sample for which acceptance of the lot is allowed under the sampling plan. JESD16-A, 4/95

access time: The time interval between the application of a specific input pulse and the availability of valid signals at an output. JESD100-B, 12/99

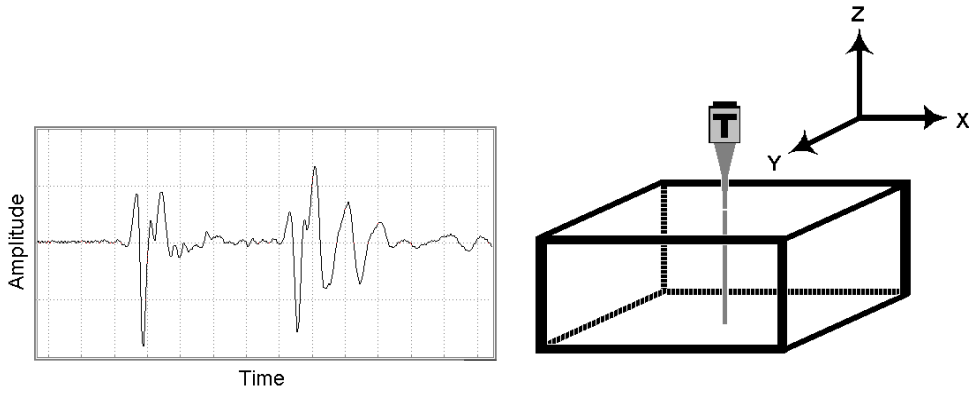
ac controller: A circuit that produces, from an ac input, an ac output that is proportional to a control input. JESD14, 11/86#

accumulator: A register in which one operand of an operation can be stored and subsequently replaced by the result of another operation. (Ref. IEC 824.) JESD100-B, 12/99

accuracy: The difference between the sample estimate and the population parameter being estimated. EIA-557-B, 2/06 JEP132, 7/98

ac noise margin: The maximum transient or pulse voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to deviate from the allowable logic voltage level. RS-390-A, 2/81

acoustic data, A-mode: Acoustic data collected at the smallest X-Y-Z region defined by the limitations of the given acoustic microscope. An A-mode display contains amplitude and phase/polarity information as a function of time of flight at a single point in the X-Y plane. J-STD-035, 5/99

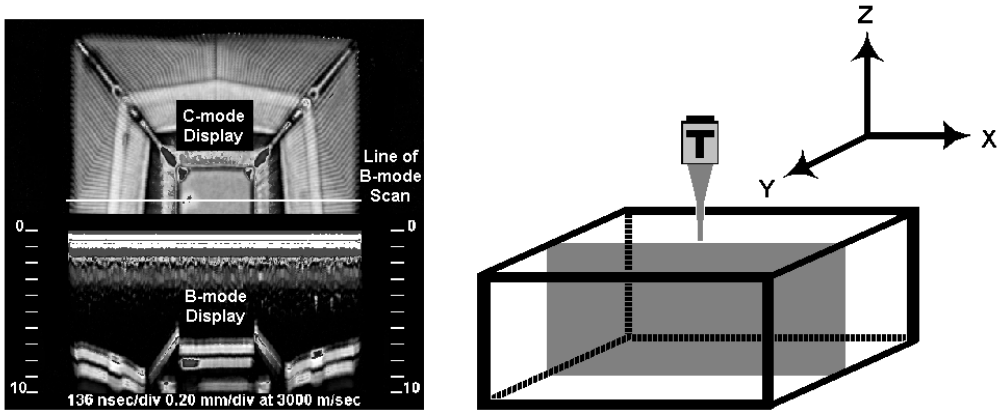


Example of A-mode display

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

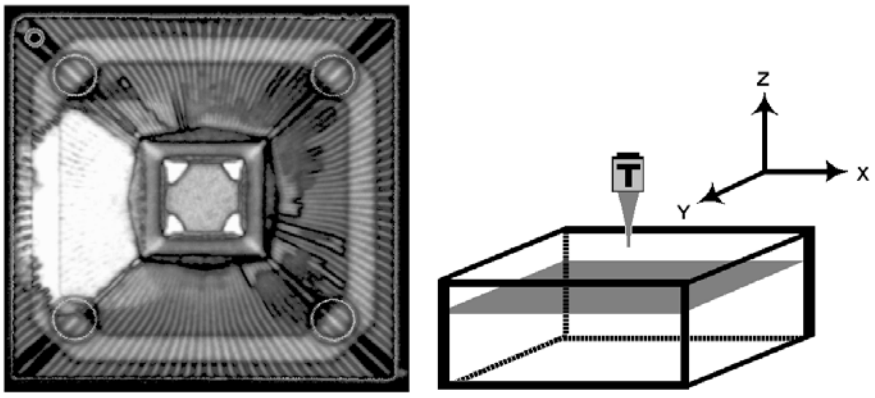
Terms, abbreviations, letter symbols, and definitions **References**

acoustic data, B-mode: Acoustic data collected along an X-Z or Y-Z plane versus depth (Z) using a reflective acoustic microscope. A B-mode scan contains amplitude and phase/polarity information as a function of time of flight at each point along the scan line. A B-mode scan furnishes a two-dimensional (cross-sectional) description along a scan line (X or Y).. J-STD-035, 5/99



Example of B-mode display (bottom half of picture on left)

acoustic data, C-mode: Acoustic data collected in an X-Y plane at depth Z using a reflective acoustic microscope. A C-mode scan contains amplitude and phase/polarity information at each point in the scan plane. A C-mode scan furnishes a two-dimensional (area) image of echoes arising from reflections at a particular depth (Z). J-STD-035, 5/99

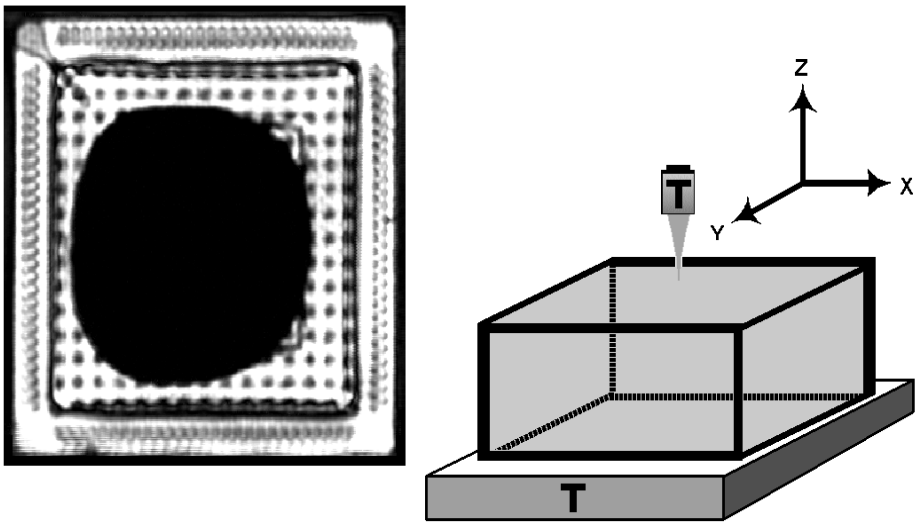


Example of C-mode display

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

acoustic data, through-transmission mode: Acoustic data collected in an X-Y plane throughout the depth (Z) using a through-transmission acoustic microscope. A through-transmission mode scan contains only amplitude information at each point in the scan plane. A through-transmission scan furnishes a two-dimensional (area) image of transmitted ultrasound through the complete thickness/depth (Z) of the sample or component. J-STD-035, 5/99



Example of through-transmission display

a**coustic microscope:** Equipment that creates an image using ultrasound to view a specimen's surface or subsurface features, J-STD-020D.1, 3/08

ac terminal: A terminal that is to be connected to the ac circuit. JESD14, 11/86

ac test: The process of verifying the specified timing of a device. JESD12-1B, 8/93
JESD99C, 12/12

NOTE Testing of propagation delays, minimum setup and hold times, minimum pulse durations, etc., can be performed by using test vectors applied at the specified operating frequency of the device. Propagation delays of critical logic paths for system operation can be measured individually.

activation energy (E_a): The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur. JEP122G, 10/11
JEP143C, 7/12
JESD85, 7/01
JESD91A, 8/01

NOTE The activation energy is used in the Arrhenius equation for the thermal acceleration of physical reactions. The term "activation energy" is not applicable when describing thermal acceleration of time-to-failure distributions, e.g., in the Arrhenius equation for reliability; hence the need for the term "apparent activation energy".

active circuit element: See "circuit element, active".

active desiccant: Desiccant that is either fresh (new) or has been baked according to the manufacturer's recommendations to renew it to original specifications. J-STD-033C, 2/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

active device: A device in which at least one circuit element is an active circuit element. JESD99C, 12/12

active element: See "circuit element, active".

active-pulldown output: A bipolar (three-state or totem-pole) output whose source-current capability significantly exceeds its sink-current capability. JESD99C, 12/12

active-pullup output: A bipolar (three-state or totem-pole) output whose sink-current capability significantly exceeds its source-current capability. JESD99C, 12/12

ac unbalanced voltage: The difference between the peak values of the ac voltages at the two outputs when the circuit is operating in the maximum-output-voltage-swing condition. JESD99C, 12/12

ADC: See "analog-to-digital [A/D] converter".

address: (1) A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172.) JESD100-B, 12/99

(2) To refer to a device or a data item by its address. (Ref. ANSI X3.172.)

address data input/output [ADQ(n)]: The pins that are multiplexed three ways to serve as address input, data input, and data output pins. When the address data input/output numbering is significant for device operation, the addresses are numbered beginning with 0. JESD21-C, 1/97

address inputs [A(n)]: Those inputs that select (address) a particular cell or set of cells within a memory array for presentation on the device outputs. The integer (n) serves to differentiate the address inputs, one from another. When the address number is significant for device operation, the addresses are numbered beginning with 0. JESD21-C, 1/97

address latch enable (AL): An input that, when true, allows the input address to be entered into a register and, when false, causes the address state previously entered to be latched. JESD21-C, 1/97

address register: A register that is used to hold an address. (Ref. IEC 824.) JESD100-B, 12/99

ADQ(n): See "address data input/output".

air ionizer: A source of charged air molecules (ions). JESD625B, 1/12

AL: See "address latch enable".

alignment mark: Synonym for "registration mark". JESD99C, 12/12

"A" limit: The more positive (less negative) limit of a range of some quantity. JESD99C, 12/12

alpha activity (of a source): The number of alpha particles produced by the decay of the alpha source per unit time. JESD89-2A, 10/07

NOTE The preferred SI unit is the becquerel (Bq); to convert curies to becquerels, multiply the number of curies by 3.7×10^{10} Bq (exactly).

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

alternative method: For a device requirement that has a prescribed method to verify compliance, another method that has been verified through test and analysis to adequately verify compliance of the device with that requirement. JESD93, 9/05

ALU: See "arithmetic and logic unit".

ambient temperature; free-air temperature (T_A): The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces. JESD10, 1/76 JESD77D, 8/12 RS-323, 3/66

A-mode: See "acoustic data, A-mode".

A(n): See "address inputs".

analog gate: A gate whose output signal is a linear function of one or more input signals. JESD99C, 12/12

analog-to-digital [A/D] converter (ADC): A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range. JESD99C, 12/12

NOTE This quantization procedure introduces inherent errors of ±½ LSB (least significant bit) in the representation because, within this fractional range, only one analog value can be represented free of error by a single digital output code.

analog-to-digital processor: An integrated circuit providing the analog part of an analog-to-digital converter. JESD99C, 12/12

NOTE Provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

analysis of variance (ANOVA): A statistical tool that allows for the comparison of more than two groups of data and provides valid assumptions. Computations of ANOVA involve partitioning total variation into two components: the variation from differences among group "means", and random variations within the groups known as "error". ANOVA provides for reliable results even when certain assumptions are violated. JEP132, 7/98

annular ring: The metallization pad area around the top or bottom of a castellation hole. JESD9B, 5/11

anode: (1) The p-type region from which the forward current flows within a semiconductor diode. JESD77D, 8/12 JESD282-B, 4/00

NOTE In Schottky diodes, usually the barrier metal replaces the p-type semiconductor region and the remaining semiconductor region is n-type; however, some Schottky diodes have been made with the barrier metal replacing the n-type semiconductor region, in which case the remaining semiconductor region is p-type.

(2) A circuit element to which positive bias is applied. JEP154, 1/08

NOTE For the purpose of JEP154, when the die is the anode the electron flow is from the substrate through the solder bump to the die.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

anode-cathode voltage; anode voltage (of a unidirectional thyristor): The voltage between the anode and cathode terminals. JESD77D, 8/12

NOTE The anode-cathode voltage is called "positive" when the anode potential is higher than the cathode potential and called "negative" when the anode potential is lower than the cathode potential.

anode current: Synonym for "forward current". JESD77D, 8/12

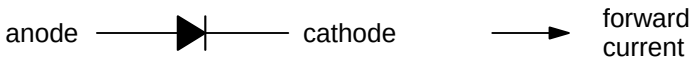
anode terminal (A, a) (1) **(general):** The terminal connected to the p-type region of the p-n junction or, when two or more p-n junctions are connected in series and have the same polarity, to the extreme p-type region. JESD77D, 8/12
JESD210, 12/07
JESD211, 12/09
JESD282-B, 4/00

NOTE 1 See note to "anode".

NOTE 2 This definition does not apply to current-regulator diodes.

NOTE 3 For voltage-reference diodes, any temperature-compensation diodes that may be included shall be ignored in the determination of the anode terminal.

NOTE 4 For unidirectional blocking or low-capacitance ABDs, any rectifier diode(s) that may be included are ignored in the determination of the anode terminal.



JESD77D, 8/12

(2) **(of a current-regulator diode):** The terminal to which current flows from the external circuit when the diode is biased to operate as a current regulator. JESD77D, 8/12

(3) (**of a unidirectional diode thyristor):** The terminal to which the current flows from the external circuit when the thyristor is in the on state. JESD77D, 8/12

(4) (**of a unidirectional triode thyristor):** The main terminal to which the principal current flows from the circuit being controlled when the thyristor is in the on state.

NOTE A second anode terminal may be provided for connecting to the control circuit of an n-gate thyristor.

ANOVA: See "analysis of variance". See also "variance components analysis".

antistatic material: Material that inhibits triboelectric charging. JESD625B, 1/12

NOTE The antistatic property of a material does not necessarily correlate with the resistivity or resistance of the material. Unlike the dissipative and conductive properties, antistatic is not defined by a measurable resistance range.

AOQ: See "average outgoing quality".

APL: See "above passivation layer".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
apparent activation energy (E_{aa}): An energy value, analogous to activation energy, that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions. NOTE 1 An apparent activation energy should be associated with a specific failure mechanism and an observed time-to-failure distribution to calculate the acceleration factor for converting the observed failure rate to the quoted failure rate at a different temperature. NOTE 2 An activation energy is a measure of the heat energy needed to establish the rate of reaction for a specific failure mechanism. The reaction rate and other contributing factors, e.g., radiation, voltage, humidity, magnetic fields, determine the unique time-to-failure distribution for the modeled failure mechanism. NOTE 3 The apparent activation energy is empirically determined from the change in an observed time-to-failure distribution with temperature.	JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07 JESD85, 7/01#
application requirements for quality and reliability: The quality and reliability properties of the product required for the specified use conditions.	JEP148A, 12/08
application-specific integrated circuit (ASIC): An integrated circuit developed and produced for a specific application or function and for a single customer. NOTE ASICs generally use standard cell or gate array design methodology.	JESD99C, 12/12
application-specific standard product (ASSP): An integrated circuit developed and produced for a specific application or function but made available for multiple customers.	JESD99C, 12/12
application use conditions: The full environmental and/or operating ranges that the application is specified to function within.	JEP149, 11/04
arc: A visual anomaly that is a curved scratch.	JESD22-B118, 3/11
area array package: A package that has terminations arranged in a grid on the bottom of the package and contained within the package outline.	J-STD-020D.1, 3/08
arithmetic and logic unit (ALU): The part of a processor that performs arithmetic operations and logic operations. (Ref. IEC 824.)	JESD100-B, 12/99
arithmetic unit: The part of a processor that performs arithmetic operations. (Ref. IEC 824.) NOTE This term is sometimes used for a unit that performs both arithmetic and logic operations.	JESD100-B, 12/99
array density (of a gate array): The number of available gates divided by the entire chip area. NOTE Units are gates per unit area.	JESD12-1B, 8/93 JESD99C, 12/12
array, logic: Synonym for “gate array integrated circuit”.	JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

Arrhenius equation (for reliability): An equation used to calculate thermal acceleration factors for semiconductor device time-to-failure distributions: JEP143C, 7/12 JESD91A, 8/01

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp\left[(-E_{aa}/k)\,(1/T_1 - 1/T_2)\right]$$

where

A_T is the acceleration factor due to changes in temperature;
λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});
λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1});
E_{aa} is the apparent activation energy (eV);
k is Boltzmann's constant (8.62×10^{-5} eV/K);
T_1 is the absolute temperature of test 1 (K);
T_2 is the absolute temperature of test 2 (K).

NOTE 1 The original Arrhenius equation (for atomic or molecular processes and chemical reactions) used the gas constant, not an activation energy, in the exponent. The "Arrhenius equation (for reliability)", used to calculate a thermal acceleration factor for a given observed time-to-failure distribution and E_{aa}, is in the form of the quotient of two Arrhenius equations, so that the acceleration factor from one temperature to another can be calculated.

NOTE 2 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s.

ART: See "auto-load read transfer".

artwork: The original, accurately scaled, oversize drawings and plastic overlays of the microcircuit topological layout that are used to produce the master mask plates. JESD99C, 12/12

NOTE Artwork has largely been supplanted by computer-produced drawings and masks.

ASER: See "accelerated soft error rate".

ASIC: See "application-specific integrated circuit".

assembled state (of a component): The state of a component that has been attached to a second-level assembly. JEP150, 5/05 JEP156, 3/09 JEP158, 11/09

assembly, microelectronic: See "microelectronic assembly".

assignable cause: Synonym for "special cause".

associative memory: Synonym for "content-addressable memory". (Ref. IEC 748-2.) JESD100-B, 12/99

ASSP: See "application-specific standard product".

asymmetry, full-scale (of a digital-to-analog converter with a bipolar analog range) (ΔI_{FSS} or ΔV_{FSS}): The difference between the absolute values of the two full-scale analog values. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
asynchronous circuit: A circuit whose changes of state are not controlled by a single clock.	JESD12-1B, 8/93 JESD99C, 12/12
ATE: Automated test equipment.	JESD89A, 10/06
attachment (noun)**:** A capacitor, substrate cap, heat sink, etc. that is glued, soldered, or mechanically affixed to a device.	JESD22-B101B, 8/09
attribute data: Data that result from counting items or classifying items into distinct nonoverlapping categories. Examples are count data (e.g., the number of nonconforming items), ordinal data (e.g., rank: first, second; classification: excellent, good, poor), nominal data (e.g., unordered groupings such as defect type), or pass/fail data.	EIA-557-B, 2/06
attribute memory select (RG): An input that, when active (low), selects the attribute memory and, when inactive (high), selects the main memory for normal access. NOTE Attribute memory is a separately accessed section of memory on the card and is generally used to record capacity and other configuration and attribute information. Main memory is used to store user data.	JESD21-C, 1/97#
audit: The periodic observation of procedures and performed activities to evaluate compliance with requirements.	EIA-557-B, 2/06
autodoping: The introduction of impurities from the substrate into the epitaxial layer during the process of epitaxy.	JESD99C, 12/12
auto-load read transfer (ART): A split serial-access memory (SAM) data register transfer in which the transfer into each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is emptied.	JESD21-C, 1/97
auto-load write transfer (AWT): A split serial-access memory (SAM) data register transfer in which the transfer from each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is filled.	JESD21-C, 1/97
automatic gain control range (AGC range): The maximum change in gain expressed in dB that may be achieved by application of a specified range of the dc voltages to the AGC input.	JESD99C, 12/12
auxiliary ground: A separate supplemental ground conductor for use other than general equipment grounding.	JESD625B, 1/12
auxiliary terminal (of a semiconductor power-control module): A terminal, other than an ac, dc, or control terminal, that may be provided for a specified purpose.	JESD14, 11/86#
available gates (in a gate array): The total number of potentially usable, unconnected gate equivalents in a given array area.	JESD12-1B, 8/93 JESD99C, 12/12
avalanche breakdown diode (ABD): A transient voltage suppressor that is a semiconductor diode with a single p-n junction (or with multiple p-n junctions none of which interact) whose operation depends in part on its breakdown characteristics.	JESD77D, 8/12 JESD210, 12/07
avalanche current, repetitive peak (I_{AR}): The peak current reached repetitively during device avalanche in an inductive-load switching circuit.	JESD24-8, 8/92#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

avalanche current, single-pulse peak (I_{AS}): The peak current reached during device avalanche in a single-pulse unclamped inductive-load switching circuit. JESD24-5, 8/90#

avalanche duration (t_{av}): The time duration of device avalanche. JESD24-5, 8/90
JESD24-8, 8/92

avalanche energy, repetitive (E_{AR}): The energy sustained by a device in avalanche per repetitive pulse in an inductive-load switching circuit. JESD24-8, 8/92#

avalanche luminescent diode: A light-emitting diode that emits luminous energy when a controlled reverse current in the breakdown region is applied. JESD77D, 8/12

avalanche voltage, drain-source ($V_{DSX(sus)}$): The effective (constant) device drain-source breakdown voltage during avalanche. The instantaneous device breakdown voltage will change with junction temperature during a test. $V_{DSX(sus)}$ can be calculated from a measurement of the avalanche duration, t_{av}. JESD24-5, 8/90

average: The sum of the sample values divided by the number of sample values. A measure of location used to estimate the population mean. EIA-557-B, 2/06

average charge-transfer efficiency: The n^{th} root of overall charge-transfer efficiency, where n is the number of transfers. JESD99C, 12/12

average current: The value of a periodic current averaged over a full cycle unless otherwise specified**.** JESD77D, 8/12
JESD282-B, 4/00

average dark current density (J_D): The average dark current per unit area within the active area of the device. JESD99C, 12/12

NOTE Depending on the type of device, the active area may be defined as either the area of transfer channel or the overall area including channel-defining regions. Other names used are "average leakage current density" and "average thermal generation current density".

average junction temperature ($T_{J(AV)}$): The average value of the virtual junction temperature of a given semiconductor device over an operating cycle. RS-323, 3/66

average noise figure; average noise factor ($\overline{F}$ or $\overline{\mathrm{NF}}$): The ratio of (1) the total output noise power within an output frequency band when the noise temperature of all input terminations is at the reference noise temperature, T_0, at all frequencies that contribute to the output noise to (2) that part of (1) caused by the noise of the signal-input termination within the signal-input frequency band. (Ref. IEC 747-1.) JESD77D, 8/12
JESD99C, 12/12
JESD311A, 11/81

NOTE 1 The abbreviation $\overline{\mathrm{NF}}$ is often used in place of symbol $\overline{F}$; however, symbol $\overline{F}$ is preferred.

NOTE 2 This ratio may be expressed logarithmically in decibels (dB).

average outgoing quality (AOQ): The average lot fraction nonconforming, in parts per million, from a series of lots. JESD16-A, 4/95

average pulse duration: See "pulse duration, average".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
average rectified output current, 50-Hz or 60-Hz sine-wave input, 180° conduction angle (I_O): The output current averaged over a full cycle from a rectifier with a 50-Hz or 60-Hz sine-wave input and a 180° conduction angle.	JESD77D, 8/12 JESD282-B, 4/00
average voltage: The value of a periodic voltage averaged over a full cycle unless otherwise specified.	JESD77D, 8/12 JESD282-B, 4/00
AWT: See "auto-load write transfer".	
axis of measurement (of a photoemitter): The direction from the source of radiant energy, relative to the optical axis, in which the measurement of radiometric and/or spectroradiometric characteristics is performed.	JESD77D, 8/12

B

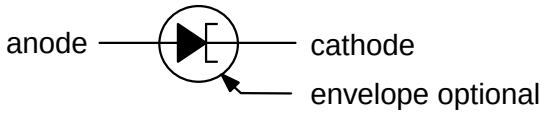
B: See "byte".	
B: See "port A; port B".	
B; b: See "base terminal".	
b: See "bit".	
BA: See "bank address".	
back-end-of-line (BEOL) (adjective)**:** Pertaining to the portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.	JEP156, 3/09 JEP158, 11/09
back end of line (BEOL) (noun)**:** The portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.	JEP156, 3/09 JEP158, 11/09
background charge: A synonym for "bias charge", used mainly in imaging devices.	JESD99C, 12/12
backside of flip chip die: The surface of the device opposite the face to which the solder bump interconnections are attached.	JESD22-B109A, 1/09
back-side substrate view area: The interface between the encapsulant and the back of the substrate within the outer edges of the substrate surface. (Refer to Type IV in Annex A of J-STD-035.)	J-STD-035, 5/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

backward diode: A semiconductor diode in which quantum-mechanical tunneling leads to a current-voltage characteristic with a reverse current greater than the forward current, for equal and opposite applied voltages, in some voltage range centered about the origin. JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



balanced amplifier: An amplifier in which the quiescent dc output voltage (or, if the output is a differential output, the difference between the two quiescent dc output voltages) has been reduced to zero or other specified level. JESD99C, 12/12

ball bond: The adhesion or welding of a thin wire, usually gold, to a die pad metallization, usually an aluminum alloy, using a thermosonic wire bond process. JESD22-B116A, 8/0 JESD99C, 12/12#

NOTE The ball bond includes the enlarged spherical, or nail-head, portion of the wire (provided by the flame-off and first bonding operation in the thermal compression and thermosonic process, or both), the underlying bonding pad and the ball bond-bonding pad intermetallic weld interface.

ball grid array (BGA) package: A package in which the external connections to the package are made via a rectangular array of ball-type connections, all on a common plane. JESD21-C, 1/97 JESD217, 9/10

NOTE See also "grid array package".

bandwidth (*B* or BW): The range of frequencies within which the gain of the amplifier is not more than 3 dB below the value of the midband gain. JESD99C, 12/12

NOTE Midband gain is the gain at a specified frequency or the average gain over a specified frequency range.

bandwidth, maximum output swing (B_{OM}): The range of frequencies within which the maximum output voltage swing is above the specified value at a specified load impedance. JESD99C, 12/12

bandwidth, unity gain: The range of frequencies within which the open-loop amplification is greater than unity. JESD99C, 12/12

bank address (BA): In a RAM that has multiple banks in its architecture, the address used to select any one of the available banks. JESD21-C, 1/97

bar code label: A label that includes information in a code consisting of parallel bars and spaces or a 2-D matrix format. J-STD-033C, 2/12

NOTE 1 See also "linear bar code label".

NOTE 2 For the purpose of J-STD-033, the bar code label is on the lowest level shipping container and includes information that describes the product, e.g., part number, quantity, lot information, supplier identification, and moisture-sensitivity level.

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Terms, abbreviations, letter symbols, and definitions **References**

bar code symbol: A symbol that gives information in a code consisting of parallel bars and spaces of various specific widths. JESD22-B114A, 5/11

base (nonspecific)**:** The overall combination of base region, base terminal, and the interface between them. JESD77D, 8/12

NOTE This term should be used in this manner only when no confusion is likely to occur.

base (of a package): The part of a package that includes the surface on which a chip is intended to be mounted. JESD9B, 5/11# JESD99C, 12/12

base-emitter saturation voltage: See "saturation voltage, base-emitter".

base materials: The laminates and/or the prepregs used to fabricate a PCB. J-STD-609A.01, 2/11

NOTE A prepreg is a sheet of material that has been impregnated with a resin cured to an intermediate stage, i.e., B-staged resin. (Ref. IPC-T-50).

base metal: (1) The unplated main metal material of which the metal package, lead, or braze is constructed. JESD9B, 5/11

(2) A metal alloy residing beneath all surface finish(es) and/or underplate. JESD201A, 8/08

base plane (of a package): A plane parallel to the seating plane through the lowest point on the body of the package. It may coincide with the seating plane. RS-308-A, 8/81 Rescinded 5/09

base region (of a unijunction transistor): A region of a semiconductor device into which majority carriers are injected. JESD77D, 8/12

base region, functional: A control region through which the principal current passes and in which the concentration of principal-current charge carriers is the result of an applied base current. JESD77D, 8/12

NOTE 1 The principal current is the result of diffusion and impurity concentration gradient drift.

NOTE 2 This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

base region, physical: (1) A region that lies between an emitter and a collector of a transistor and into which minority carriers are injected. (Ref. 60 IRE 28.S1.) JESD10, 1/76

(2) The physical region that is located between the collector junction and the emitter junction and contains the control region. JESD77D, 8/12

base terminal (B, b): The specified externally available point of connection to the base region. JESD77D, 8/12

basic dimension: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. Permissible variations from the basic dimension are established by tolerances on associated dimensions, in notes, or in feature control frames. JESD95-1, 3/97

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Terms, abbreviations, letter symbols, and definitions	References
bathtub curve: A plot of failure rate versus time or cycles that exhibits three phases of life: infant mortality (decreasing failure rate), intrinsic or useful life (relatively constant failure rate), and wearout (increasing failure rate).	JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07 JESD85, 7/01 JESD91A, 8/01
battery voltage detect [BD(n)]: The signals BD1 and BD2 generated by the memory card as an indication of the condition of the battery on the memory card. Both signals are kept asserted when the battery is in good condition. When BD2 is negated while BD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the card is still assured. If BD1 is negated with BD2 either asserted or negated, the battery is no longer serviceable and data is lost.	JESD21-C, 1/97
baud: A unit of signaling speed equal to the number of discrete conditions or signal events per second. (Ref. ANSI X3.172.)	JESD100B.01, 12/02
NOTE For example, one baud equals one bit per second in a train of binary signals or one 3-bit value per second in a train of signals each of which can assume one of eight (2^3) different states.	
BBD: See "bucket-brigade device".	
BCCD: See "buried-channel charge-coupled device".	
BCD: See "bipolar-and-CMOS-and-DMOS technology".	
BCXXX series: A BiCMOS series that includes devices whose input logic levels are TTL-compatible and whose outputs are specified at TTL levels; the low-level output voltage is specified at 24 mA and 48 mA.	JESD54, 2/96#
BD(n): See "battery voltage detect".	
BDRAM: See "burst DRAM".	
beam lead: A thick-film lead formed on and attached to the chip interconnection pattern and projecting cantilevered beyond the chip periphery for attachment to a substrate.	JESD99C, 12/12
behavioral description: The algorithms or equations defining a function.	JESD12-1B, 8/93 JESD99C, 12/12
benchmark: A standard by which something can be judged.	EIA-599-A, 6/98
BFR/CFR: See "brominated/chlorinated flame retardants".	
BG: See "byte-mode enable".	
BGA: See "ball grid array package".	
bias: (1) A voltage or current applied to an electronic device to establish a reference level for operation.	Merriam-Webster's Collegiate Dict.
(2) The difference between the mean (or expectation) of an estimator, T, and the true value, θ, of a parameter: $E(T) - \theta$.	JESD37, 10/92

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Terms, abbreviations, letter symbols, and definitions **References**

bias charge; circulating bias charge (for analog signal applications): A charge that defines the no-signal level. JESD99C, 12/12

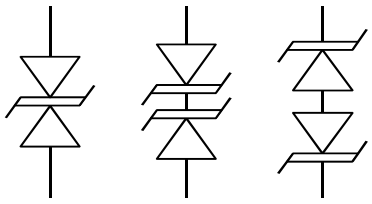
NOTE This charge is inserted into all potential wells electrically or by radiation.

BiCMOS: See "bipolar-and-CMOS technology".

BiCMOS series: A series that includes devices combining bipolar and silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit. JESD54, 2/96

bidirectional ABD: A two-terminal ABD with a voltage-current avalanche breakdown characteristic in both directions, which can be either symmetrical or asymmetrical. JESD77D, 8/12
JESD210, 12/07

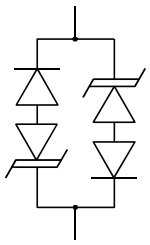
NOTE Large transient currents will be clamped for voltage of either polarity across two similar p-n junctions in series connected in opposite directions. During a transient current event in this operating mode, one of the two p-n junctions is always in avalanche breakdown and the other is in the forward-conducting, low-voltage mode. The voltage across the bidirectional ABD is the sum of these two voltages. The avalanche breakdown voltage is substantially the same in both directions for a symmetrical bidirectional ABD; however, it may also be intentionally different or asymmetrical by design for special applications. Since multiple p-n junction capacitances in series reduce the overall total capacitance, the bidirectional ABD has lower capacitance than its unidirectional counterpart.



Bidirectional ABD symbol options

bidirectional low-capacitance ABD: A two-terminal device comprising two anti-parallel unidirectional-blocking low-capacitance ABD devices. JESD77D, 8/12
JESD210, 12/07

NOTE The rectifier p-n junctions have low capacitance and must have a reverse blocking voltage greater than the avalanche breakdown voltage of the anti-parallel unidirectional ABD element.



bidirectional thyristor surge protective device: A thyristor surge protective device having substantially the same switching characteristics in the first and third quadrants. JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

BiFET: See "bipolar-and-FET technology".

big endian: The format in which the most significant bit of a word is transferred first and the least significant bit is transferred last. JESD96, 4/04

BiMOS: See "bipolar-and-MOS technology".

binomial distribution: A specific discrete probability distribution for attributes data. EIA-557-B, 2/06

bipolar-and-CMOS-and-DMOS (BCD) technology: A technology for combining bipolar transistors, silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices, and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit. JESD99C, 12/12

bipolar-and-CMOS (BiCMOS) technology: A technology for combining bipolar transistors and silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit. JESD55, 5/96#
JESD99C, 12/12

bipolar-and-FET (BiFET) technology: A technology for combining bipolar transistors and junction-gate field-effect transistors (JFET) in a single-chip integrated circuit. JESD99C, 12/12

bipolar-and-MOS (BiMOS) technology: A technology for combining bipolar transistors and metal-gate metal-oxide-semiconductor (MOS) or metal-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit. JESD99C, 12/12

bipolar output: An output having internal connections through two active devices to two supply voltages so that, according to the relative states of the active devices, the output can source or sink current through the load. JESD99C, 12/12

bipolar technology: A technology for producing devices in which electrical conduction depends on the flow of both majority and minority carriers. JESD77D, 8/12
JESD99C, 12/12

bipolar transistor (general)**:** A transistor in which, in the operating mode, the controlling input consists of charge carriers that are injected into the control region and are of a polarity that is opposite to the polarity of the principal-current charge carriers, and in which the magnitude of the principal current depends on the magnitude of the control current. JESD77D, 8/12

bistable logic function: A sequential logic function that has two and only two stable internal output states. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

bit (b): (1) In the binary numeration system, either of the digits 0 or 1. (Ref. ANSI X3.172.) JESD100B.01, 12/02

NOTE Abbreviated form of "binary digit".

(2) The unit of storage capacity that corresponds to a single memory cell.

bit plane: In a semiconductor memory device having a data interface that is wider than one bit, those storage cells and associated circuitry that are associated with a given bit in the data interface. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
bit slice; slice: A partition of a microprocessor that enables several identical units to be paralleled or cascaded and augmented by control logic to realize the central processing unit.	JESD100-B, 12/99
bit-slice processor: A central processing unit constructed of an array of identical units, each of which operates simultaneously upon one or more adjacent bits. (Ref. IEC 824.)	JESD100-B, 12/99
bit-wide device: A device that has only a single-bit data interface.	JESD21-C, 1/97# JESD100B.01, 12/02
blackbody: Ideally, a body that would absorb all and reflect none of the radiant energy falling upon it; its reflectivity would be zero and its absorptivity (and consequently, its emissivity) would be 100%. In practice, a radiator of uniform temperature whose radiant emittance in all parts of the spectrum is the maximum obtainable from any radiator at the same temperature, or a radiator whose spectral radiant emittance conforms with Planck's law of radiation.	JESD51-1, 12/95# JESD51-13, 6/09# JESD77D, 8/12
blemish: A visual anomaly that is an area of inconsistent finish.	JESD22-B118, 3/11
"B" limit: The less positive (more negative) limit of a range of some quantity.	JESD99C, 12/12
blistering: Detachment of material from a surface creating a bubble-like shape.	JESD9B, 5/11
BLM: See "under-bump metal"**.**	
block: A continuous range of memory addresses. (Ref. IEC 748-2.)	JESD100-B, 12/99
NOTE The number of addresses included in the range is frequently equal to 2^n, where n is the number of bits in the address.	
blocking: A term describing the state of a semiconductor device or junction that imposes high resistance to the passage of current.	JESD77D, 8/12 JESD282-B, 4/00
blocking period (of a rectifier circuit element): The part of an alternating-voltage cycle during which the current flows in the reverse direction.	JESD282-B, 4/00
NOTE The blocking period is not necessarily the same as the reverse period because of the effect of circuit parameters and semiconductor rectifier diode characteristics.	
block select (BS): A group of input signals that enable individual bit blocks of the data interface.	JESD21-C, 1/97
block write, no mask (BW): A RAM write cycle in which four bits are written into each bit plane as defined by the contents of the color register. The four bits are those locations controlled by the two least significant bits (LSB) of the column address.	JESD21-C, 1/97
block write with new mask (BWNM): A block-write cycle in which the data written is also controlled by the write mask supplied on the DQ(n) terminals in that cycle.	JESD21-C, 1/97
block write with old mask (BWOM): A block-write cycle in which the data written is controlled by the contents of the write-mask register that was previously loaded in a load-write-mask cycle.	JESD21-C, 1/97
B-mode: See "acoustic data, B-mode".	

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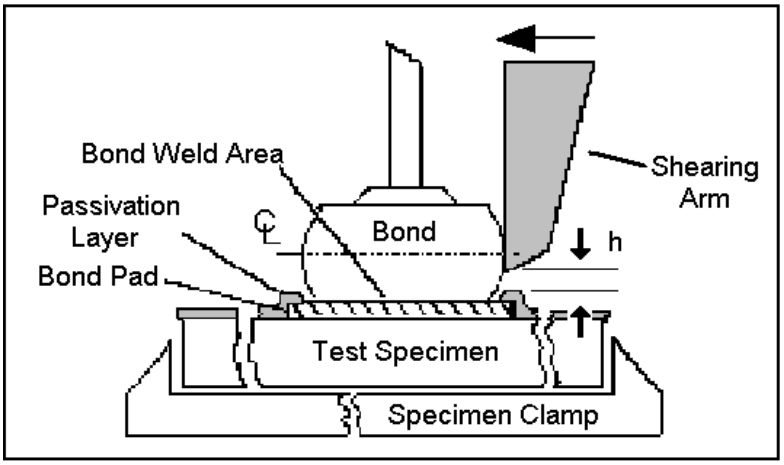
Terms, abbreviations, letter symbols, and definitions	References
body (of a package): That part of the package or device excluding electrical terminals, studs, leads, etc.	RS-308-A, 8/81 Rescinded 5/09
body (of a semiconductor device): The semiconductor portion of a device limited by the physical extent of the crystalline or amorphous semiconductor material and including any associated oxide layers and metallization.	JESD77D, 8/12 JESD99C, 12/12
Boltzmann's constant (*k*): A constant equal to 1.38×10^{-23} joule per kelvin or 8.62×10^{-5} electronvolt per kelvin.	JEP122G, 10/11 JEP143C, 7/12
bond and assembly (B&A) process: A process associated with connecting chips (dice) to other package elements and assembling semiconductor-device packages.	JEP156, 3/09 JEP158, 11/09
bond, ball: See "ball bond	
bond, chip: The attachment of the circuit chip to a hybrid or package substrate. NOTE The attachment serves as a mechanical support, a thermal path, and sometimes an electrical contact.	JESD99C, 12/12
bond, die: Synonym for "semiconductor chip bond".	JESD99C, 12/12
bond, face: A bond directly between a chip bonding pad and a mounting substrate for the purpose of making electrical contact.	JESD99C, 12/12
bond footprint (of a wedge bond): The area of the wire that has a physical bond interface (intermetallic or recrystallized) with respect to the compressed area of the wire.	JESD22-B116A, 8/09
bonding (critical) area: The surface on a lead or package to which wires will be bonded (i.e., the wire-bond area). NOTE 1 This term is not to be confused with the "die bond area" which is specified as the "die-attach area" in this specification. NOTE 2 The critical wirebond area on a ceramic package is a metallization trace whose length is 0.381 mm (0.015 inch) and whose width is 80% of the width of the designed wire-bond trace, as specified in the applicable procurement document.	JESD9B, 5/11
bonding surface: Either 1) the die pad metallization or 2) the package surface metallization to which the wire is ball-, wedge-, or stitch-bonded.	JESD22-B116A, 8/09
bonding trace; wire-bond trace: A metallized path on a package or substrate to which a bond wire is wire-bonded.	JESD9B, 5/11
bonding wire: A wire that is bonded to a chip bonding pad in order to connect the chip to any other point within the device package.	JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

bond shear: A process in which an instrument uses a chisel-shaped tool to shear or push a ball or wedge bond off the bond pad (see figure below). JESD22-B116A, 8/09

NOTE The force required to cause this separation is recorded and is referred to as the bond shear force. The bond shear force of a gold ball bond, when correlated to the diameter of the ball bond, is an indicator of the quality of the metallurgical bond between the gold ball bond and the bond pad metallization. The bond shear force of an aluminum wedge bond, when compared to the manufacturer's tensile strength of the wire, is an indicator of the integrity of the weld between the aluminum wire and the bond pad or package surface metallization.



bond-shear code for ball and wedge bond, type 1 — bond lift: A separation of the entire wire bond from the bonding surface with only an imprint being left on the bonding surface and very little evidence of intermetallic formation or welding or of disturbance of the bonding surface metallization. JESD22-B116A, 8/09

bond-shear code for ball and wedge bond, type 2 — bond shear: A separation of the wire bond in which 1) a thin layer of the bonding surface metallization remains with the wire bond and an impression is left in the bonding surface, 2) intermetallics remain on the bonding surface and with the wire bond, or 3) a major portion of the wire bond remains on the bonding surface. JESD22-B116A, 8/09

bond-shear code for ball and wedge bond, type 3 — cratering: A condition under the die pad metallization in which the insulating layer (oxide or interlayer dielectric) and the bulk material (silicon) separate or chip out. JESD22-B116A, 8/09

NOTE 1 Separation interfaces that show pits or depressions in the insulating layer (not extending into the bulk) are not considered craters.

NOTE 2 Cratering can be caused by several factors including the wire bonding operation, the post-bonding processing, and even the act of shear testing itself.

NOTE 3 Cratering present prior to the shear test operation denotes a pre-existing condition that must be addressed. Any bonds with preexisting cratering are invalid for this test method and shall not be included with the shear data.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
bond-shear code for ball and wedge bond, type 4 — arm contacts specimen bonding surface contact: A condition produced when the shear tool contacts the bonding surface. NOTE This condition may be due to improper placement of the specimen, a low shear height, or instrument malfunction. This bond shear type is an invalid result and shall be eliminated from the shear data.	JESD22-B116A, 8/09
bond-shear code for ball and wedge bond, type 5 — shearing skip: A condition produced when the shear tool removes only the topmost portion of the ball or wedge bond. NOTE This condition may be due to improper placement of the specimen, a high shear height or instrument malfunction. This bond shear type is an invalid result and shall be eliminated from the shear data.	JESD22-B116A, 8/09
bond-shear code for ball and wedge bond, type 6 — bond pad (or bonding surface) lift: A separation between the bonding surface metallization and the underlying substrate or base material. There is evidence of bonding surface metallization remaining attached to the ball or wedge bond.	JESD22-B116A, 8/09
bond, stitch: A thermocompression bond in which a capillary tube is used for both feeding the wire and forming the bond.	JESD99C, 12/12
bond, thermocompression: A bond in which two members are joined through the combined application of heat and pressure.	JESD99C, 12/12
bond, ultrasonic: A bond in which two members are joined through the combined application of pressure and an ultrasonic oscillatory lateral motion.	JESD99C, 12/12
bond, wedge: A thermocompression bond in which a wedge-shaped tool is used to apply pressure to the wire being attached.	JESD99C, 12/12
bond, wire: The attachment between a bonding wire and a chip bonding pad or package terminal.	JESD99C, 12/12
boundary scan: A design methodology in which the I/O buffers of a circuit or functional block are observed and controlled by scan cells. NOTE The Boundary Scan standard was developed by the Joint Test Action Group (JTAG) and is embodied in IEEE Standard 1149-1.	JESD12-1B, 8/93 JESD99C, 12/12
braze: A metallic material used to join two metals or metallized components.	JESD9B, 5/11
braze climb: The distance from the surface of the package to the top of the braze line on a lead, not including braze flash.	JESD9B, 5/11
braze flash: The braze material that has flowed over or out of the designed contained braze area and is less than 0.0254 mm (0.001 inch) thick.	JESD9B, 5/11
braze run-out: The braze material that has flowed over or out of the designed contained braze area, not including braze flash.	JESD9B, 5/11
braze, undercut: The braze material recessed from the package surface at the interface of the package wall and the package base.	JESD9B, 5/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
breakdown: The phenomenon, occurring in a reverse-biased semiconductor junction, whose initiation is observed as a transition from a region of high small-signal resistance to a region of substantially lower small-signal resistance for an increasing magnitude of reverse current.	JESD10, 1/76 JESD24, 7/85 JESD77D, 8/12 JESD282-B, 4/00
breakdown current: A current in a breakdown region.	JESD77D, 8/12 JESD282-B, 4/00
breakdown region (1) **(of a thyristor surge protective device):** The portion of the characteristic that starts with the transition from the high dynamic resistance off state to a substantially lower dynamic resistance and extending to the switching point.	ESD77D, 8/12 JESD210, 12/07
(2) **(of a voltage regulator diode):** The portion of the voltage-current characteristic beyond the initiation of breakdown where the current increases rapidly for any additional increase in reverse voltage. NOTE In this region the voltage remains essentially constant for increases in reverse current, up to a specified current and power dissipation rating.	JESD211, 12/09
(3) **(reverse):** The portion of the voltage-current characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current.	JESD10, 1/76# JESD24, 7/85# JESD77D, 8/12 JESD282-B, 4/00
breakdown voltage: A voltage in a breakdown region.	JESD10, 1/76# JESD24, 7/85# JESD77D, 8/12 JESD282-B, 4/00#
breakdown voltage, collector-base, emitter open ($V_{(BR)CBO}$) (formerly BV_{CBO}): The breakdown voltage between the collector and base terminals when the collector terminal is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited.	JESD10, 1/76 JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

breakdown voltage, collector-emitter, base open ($V_{(BR)CEO}$) (formerly BV_{CEO}): JESD10, 1/76
breakdown voltage, collector-emitter, base short-circuited to emitter ($V_{(BR)CES}$) (formerly BV_{CES}): JESD77D, 8/12
breakdown voltage, collector-emitter, circuit between base and emitter ($V_{(BR)CEX}$) (formerly BV_{CEX}):
breakdown voltage, collector-emitter, resistance between base and emitter ($V_{(BR)CER}$) (formerly BV_{CER}):
breakdown voltage, collector-emitter, voltage between base and emitter ($V_{(BR)CEV}$) (formerly BV_{CEV}):
The breakdown voltage between the collector and emitter terminals when the collector terminal is biased in the reverse direction* with respect to the emitter terminal, and the base terminal is, respectively,

— open-circuited.
— short-circuited to the emitter terminal.
— returned to the emitter terminal through a specified circuit.
— returned to the emitter terminal through a specified resistance.
— returned to the emitter terminal through a specified voltage.

*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for npn transistors or negative for pnp transistors with respect to the emitter terminal.

breakdown voltage, drain-source, with circuit between gate and source ($V_{(BR)DSX}$): JESD24, 7/85
The breakdown voltage between the drain terminal and the source terminal when the gate terminal is returned to the source terminal through a specified circuit.

breakdown voltage, drain-source, with gate short-circuited to source ($V_{(BR)DSS}$): JESD24, 7/85
The breakdown voltage between the drain terminal and the source terminal when the gate terminal is short-circuited to the source terminal.

breakdown voltage, drain-source, with resistance between gate and source ($V_{(BR)DSR}$): JESD24, 7/85
The breakdown voltage between the drain terminal and the source terminal when the gate terminal is returned to the source terminal through a specified resistance.

breakdown voltage, drain-source, with voltage between gate and source ($V_{(BR)DSV}$): JESD24, 7/85
The breakdown voltage between the drain terminal and the source terminal when the gate terminal is returned to the source terminal through a specified voltage.

breakdown voltage, emitter-base, collector open ($V_{(BR)EBO}$) (formerly BV_{EBO}): JESD10, 1/76
The breakdown voltage between the emitter and base terminals when the emitter terminal is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE Std 255.)

breakdown voltage, forward gate-source ($V_{(BR)GSSF}$): The breakdown voltage between the gate terminal and the source terminal with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal. JESD24, 7/85

NOTE The symbol $V_{(BR)GSSF}$ should be used with insulated-gate transistors having shunting diodes or similar voltage-limiting devices.

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Terms, abbreviations, letter symbols, and definitions **References**

breakdown voltage, gate-source ($V_{(BR)GSS}$): The breakdown voltage between the gate terminal and the source terminal when the drain terminal is short-circuited to the source terminal. JESD24, 7/85

NOTE The symbol $V_{(BR)GSS}$ is used primarily with junction-gate field-effect transistors.

breakdown voltage, reverse gate-source ($V_{(BR)GSSR}$): The breakdown voltage between the gate terminal and the source terminal with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal. JESD24, 7/85

NOTE The symbol $V_{(BR)GSSR}$ should be used with insulated-gate transistors having shunting diodes or similar voltage-limiting devices.

breakover point (of a thyristor): In a quadrant in which switching can occur, the point for which the differential resistance is zero and the off-state voltage reaches a maximum value. JESD77D, 8/12

bridge (output): Synonym for "full-bridge (output)". JESD99C, 12/12

bridge rectifier circuit: A double-way rectifier circuit in which (1) each terminal of the alternating-voltage circuit is connected to the anode of one rectifier element in a set of elements whose cathodes are all connected to the positive output of the circuit, (2) each terminal of the alternating-voltage circuit is also connected to the cathode of one rectifier element in another set of elements whose anodes are all connected to the negative output, and (3) the load is connected between the positive and negative outputs. JESD77D, 8/12

NOTE The term is derived from the similarity in layout of a single-phase four-element bridge rectifier to that of a Wheatstone bridge.

bright tin: A tin film with higher internal stresses than matte tin, grain sizes of 0.5 µm to 0.8 µm, and a carbon content of 0.2% to 1.0%. JP002, 3/06

brominated/chlorinated flame retardants (BFR/CFR): Flame retardants that contain bromine and/or chlorine. JS709A, 5/12

NOTE These compounds are typically added to or reacted into polymers such as certain epoxy resins and thermoplastics to reduce their flammability. Examples include, but are not limited to, tetrabromobisphenol-A (TBBPA), brominated epoxy resins, and polybrominated diphenyl ethers (PBDEs).

BS: See "block select".

bubble, subsurface: A bubble, in the glass-to-metal seal, that is below the top surface of the seal and is not open or cannot be opened with a wood probe. JESD9B, 5/11

bubble, surface; open-surface bubble: A bubble in the glass-to-metal seal that is the top surface of the seal and is either open or can be opened with a wood probe. JESD9B, 5/11

bucket-brigade device (BBD): A charge-transfer device that stores charge in discrete regions in a semiconductor and transfers this charge as a packet through a series of switching devices that interconnect these regions. JESD99C, 12/12

NOTE This term and its abbreviation may be preceded by bipolar, JFET, MOS, SIS, etc., according to the technology used for the switching devices.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

buffer: (1) An isolating circuit used to minimize the effects of a driven circuit on the driving circuit. (Adapted from ANSI/IEEE Std 100.and ANSI X3.172.) JESD99C, 12/12 JESD100B.01, 12/02

(2) A routine or storage used to compensate for a difference in the rate of flow of data or in the time of occurrence of events, when transferring data from one device to another. (Ref. ANSI X3.172.) JESD100B.01, 12/02

buffered (output): An output whose on-state impedance is independent of any valid input logic conditions, both preceding and present. JESD13-B, 5/80#

buffer storage: Storage used to compensate for a difference in the rate of flow of data between components of an automatic data processing or communications system, or in the time of occurrence of events in the components. (Adapted from ANSI X3.172.) JESD100B.01, 12/02

built-in electric field (in a transition region): The internal electric field in the absence of bias. JESD77D, 8/12

bulk-channel charge-coupled device (BCCD): Synonym for "buried-channel charge-coupled device". JESD99C, 12/12

bulk characteristics (of a semiconductor material): The characteristics of a piece of semiconductor material that has uniform properties throughout the whole piece, as measured in those parts of the piece in which the measured value of a characteristic is not modified by the proximity of the boundaries of the piece. JESD77D, 8/12

NOTE Bulk characteristics for pieces smaller than required by the definition are those that would be measured for a sufficiently large piece having the same technological properties.

bulk current, dc (I_B): The direct current into the bulk contact. JESD28-A, 12/01 JESD60A, 9/04 JESD90, 11/04

bulk reflow: Reflow of multiple components, with simultaneous attachment, by an infrared (IR), convection/IR, convection, or vapor phase reflow (VPR) process. J-STD-033C, 2/12

bulk-source voltage, dc (V_{BS}): The dc bulk-to-source voltage. JESD28-A, 12/01 JESD60A, 9/04 JESD90, 11/04

bump-limiting metal: Synonym for "under-bump metal".

buried channel: A transfer channel beneath the surface of a semiconductor. JESD99C, 12/12

buried-channel charge-coupled device (BCCD); bulk-channel charge-coupled device (BCCD); peristaltic charge-coupled device: A charge-coupled device that confines the flow of charges to a channel lying beneath the surface of the semiconductor. JESD99C, 12/12

burn mark: A visual anomaly with a burned appearance. JESD22-B118, 3/11

burr (on a package): A fragment of excess material or foreign particle adhering to a surface. JESD27, 8/93 Rescinded 5/11

burst DRAM (BDRAM): A DRAM that has burst-mode-data capability. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

bus: A common path along which power or signals travel from one or several sources to one or several destinations. (Adapted from IEC 824.) — JESD100-B, 12/99

bus driver: A line driver used for fan-out to multiple receivers via a transmission line. — JESD99C, 12/12

bus receiver: A line receiver intended to be driven from a bus. — JESD99C, 12/12

busy (BY): The output that, on some devices, signifies that some internal asynchronous operation is still in process and that the device is not available for normal functions. This signal is normally implemented so that multiple devices can be OR-tied. — JESD21-C, 1/97

busy signal: Synonym for "wait signal". — JESD100-B, 12/99

BW: See "bandwidth".

BW: See "block write, no mask".

BWNM: See "block write with new mask".

BWOM: See "block write with old mask".

Bxxx: A device name (e.g., BDRAM) whose first letter (B) indicates that the device has a "burst" data capability. — JESD21-C, 1/97#

BY: See "busy".

byte (B): (1) A binary character string operated upon as a unit and usually shorter than a computer word. (Ref. ANSI X3.172.) — JESD100-B, 12/99

NOTE A byte is usually eight bits.

(2) The unit of storage capacity equal to eight bits.

byte-mode enable (BG): An input that, when true, causes a word-wide device to operate in the byte mode and to present the high or low byte on a predefined data pin set. Truth tables are provided to define the details of the operation. — JESD21-C, 1/97

byte-wide device: A device that has a parallel data interface of eight bits, possibly with additional bits appended to provide parity or error-detection capability. — JESD21-C, 1/97# JESD100-B, 12/99

byte [word] identifier (x): In the pin names and their definitions in section 2 of JESD21-C, an alphabetic identifier for the byte [word] being accessed. — JESD21-C, 1/97

C

C: See "output clock".

C; c: See "collector terminal".

CA: See "column address".

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Terms, abbreviations, letter symbols, and definitions	References
cache memory: A special buffer storage, smaller and faster than main storage, that is used to hold a copy of data or instructions that have been obtained automatically from main storage and are likely to be needed soon by the processor. (Adapted from ANSI X3.172.) NOTE It is placed between the CPU and main storage to make main storage look like fast memory.	JESD100-B, 12/99
CAM: See "content-addressable memory".	
can package: Generally, a cylindrical package whose terminals exit from one end parallel to the axis of the package.	JESD30E, 8/08
capability: The natural variation of the process due to common causes.	EIA-557-B, 2/06 EIA-599-A, 6/98
capability analysis: The study of a process to determine the probability that the characteristics of its output will fall within a previously defined set of constraints.	JEP132, 7/98
capability index: A measure of the relationship between the specification limits and the capability. See EIA-738, *Guideline on the Use and Application of Cpk* and *The Use and Abuse of Cpk* by Berton H. Gunter.	EIA-557-B, 2/06
capacitance: The capacitance between the two terminals of a diode at a specified voltage.	JESD211, 12/09
card detect [CD(n)]: The two signals, CD1 and CD2, that provide for proper memory card insertion detection and are positioned at opposite ends of the connector to facilitate the detection process. The signals are connected to ground internally on the memory card; thus they will be forced low whenever a card is placed in a host socket. The host socket interface circuitry shall provide 10-kΩ pull-up resistors to VCC on each of these signal pins.	JESD21-C, 1/97
carrier: A pocket tape, tray, tube or other fixture used to store and transport devices and components.	JESD22-B101B, 8/09# J-STD-033C, 2/12#
carrier, (charge) (in a semiconductor): A mobile (i.e., free) conduction electron or mobile hole. (Ref. IEC 747-1.)	JESD77D, 8/12
CAS: See "column enable".	
case: Synonym for "package".	
case temperature (T_C): The temperature measured at a specified location on the case of a device.	JESD10, 1/76 JESD77D, 8/12
case-to-ambient thermal resistance: See "thermal resistance, case-to-ambient".	
CAS latency (for an SDRAM): Synonym for "read latency".	JESD100-B, 12/99
castellation: A semicircular or crown-shaped metallized surface.	JESD9B, 5/11
catastrophic failure: A failure that has serious consequences for the failed device or other components associated with it in the circuit (e.g., input shorted to power supply or ground, power-supply-to-ground short circuit, destructive latch-up, etc.).	JEP134, 9/98

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Terms, abbreviations, letter symbols, and definitions	References
cathode: (1) The n-type region to which the forward current flows within a semiconductor diode.	JESD77D, 8/12 JESD282-B, 4/00
NOTE In Schottky diodes, usually the barrier metal replaces the p-type semiconductor region and the remaining semiconductor region is n-type; however, some Schottky diodes have been made with the barrier metal replacing the n-type semiconductor region, in which case the remaining semiconductor region is p-type.	
(2) A circuit element to which negative bias is applied.	JEP154, 1/08
NOTE For the purpose of JEP154, when the die is the cathode, the electron flow is from the die through the solder bump to the substrate.	
cathode current: Synonym for "reverse current".	JESD77D, 8/12
cathode terminal (K, k) (1) **(general):** The terminal connected to the n-type region of the p-n junction or, when two or more p-n junctions are connected in series and have the same polarity, to the extreme n-type region.	JESD77D, 8/12 JESD210, 12/070 JESD211, 12/09 JESD282-B, 4/00
NOTE 1 See note to "cathode".	
NOTE 2 This definition does not apply to current-regulator diodes.	
NOTE 3 For voltage-reference diodes, any temperature-compensation diodes that may be included shall be ignored in the determination of the cathode terminal.	
NOTE 4 For unidirectional blocking or low-capacitance ABDs, any rectifier diode(s) that may be included are ignored in the determination of the cathode terminal.	JESD77D, 8/12
(2) **(of a current-regulator diode):** The terminal from which current flows into the external circuit when the diode is biased to operate as a current regulator.	JESD77D, 8/12
(3) **(of a unidirectional diode thyristor):** The terminal from which the current flows to the external circuit when the thyristor is in the on state.	JESD77D, 8/12
(4) **(of a unidirectional triode thyristor):** The main terminal from which the principal current flows to the circuit being controlled when the thyristor is in the on state.	
NOTE A second cathode terminal may be provided for connecting to the control circuit of a p-gate thyristor.	
cause-and-effect diagram: A tool for individual or group problem-solving that uses a graphic description of the various process elements to analyze potential sources of process variation. Also called a "fishbone diagram" (after its appearance) or "Ishikawa diagram" (after its developer).	JEP132, 7/98 EIA-557-B, 2/06
cavity package: A package containing a cavity that is intended to be occupied by a chip.	JESD22-B103B, 6/02# JESD22-B104C, 11/04#
CBGA: Ceramic ball grid array package.	JESD217, 9/10
CCD: See "charge-coupled device".	
CCGA: Ceramic column grid array package.	JESD217, 9/10

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

CDM: See "charged-device model".

CD(n): See "card detect".

CE: See "column enable".

cell-based integrated circuit: An integrated circuit fabricated with a unique full set of mask information and comprising one or more macrocells that can be selectively placed and interconnected to perform an electrical function. JESD12-1B, 8/93 JESD99C, 12/12

cell compiler: A tool that automatically generates the physical layout to meet the specified parameters and that may generate a symbol and timing and functional models. JESD12-1B, 8/93 JESD99C, 12/12

censored data: A set of data for which a portion of the test samples had testing discontinued prior to failing or survived until the end of the test. JEP154, 1/08

centerline: A reference line on a control chart about which the chart points are expected to cluster in the absence of a special cause. It is usually set at the average, median, or mode of the points being plotted, or (for a tunable process) at an achievable target value (to detect deviations from the value thought most desirable). EIA-557-B, 2/06

central processing unit; processing unit (CPU): A functional unit that consists of one or more processors and their internal storage. (Ref. ANSI X3.172.) JESD100-B, 12/99

certified process: A process that, through demonstration and validation, has been determined to produce product capable of consistently achieving or exceeding customer requirements. EIA-599-A, 6/98

CFF: See "cumulative fraction failing".

C^4D: See "conductivity-connected charge-coupled device".

change, (product or process): An alteration to the product or process, which may be a major change or a minor change. JESD46D, 12/11

NOTE 1 A major change is a change that may affect the form, fit, or function of the product or adversely affect the quality or reliability of the product.

NOTE 2 A minor change is a change that does not affect the form, fit, function, quality, or reliability of the product.

channel: (1) A thin semiconductor layer, between the source region and the drain region, in which the current is controlled by the gate potential. JESD24, 7/85

(2) A region of semiconductor material in which current flow is influenced by a transverse electrical field. JESD99C, 12/12

NOTE 1 A channel may physically be an inversion layer, a diffused layer, or bulk material.

NOTE 2 The type of channel, i.e., p-channel or n-channel, is determined by the type of majority carrier during conduction.

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Terms, abbreviations, letter symbols, and definitions	References
channel: Both a set of physically discrete connections within the Wide I/O interface and a logically discrete, independently controlled partition of the Wide I/O interface.	JESD229, 12/11
NOTE The Wide I/O interface supports four physical and four logical channels. Each physical channel contains all the control, data, and clock signals necessary to independently control each of the four logical channels in the Wide I/O interface. Aside from a few global configuration options, each logical channel has its own set of mode registers, can have different DRAM pages open, can be independently clocked, and can even be in different power states. The physical channel also contains power and ground signals, but all power and ground signals on all physical channels must be at their appropriate levels for any portion of the Wide I/O device to operate correctly. The physical channel also contains a reset signal, but the Wide I/O interface defines reset to be per slice rather than per channel.	
channeled gate array: A gate array configuration that contains a predetermined and dedicated area for logic interconnection.	JESD12-1B, 8/93 JESD99C, 12/12
channelless gate array: A gate array configuration that contains no predetermined and dedicated area for logic interconnection.	JESD12-1B, 8/93 JESD99C, 12/12
channel region (1) **(of an IGFET):** A control region through which the principal current passes and in which the concentration of principal-current charge carriers is determined by voltage applied to a gate, the principal current being the result of an applied drift field.	JESD77D, 8/12
NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.	
(2) **(of a JFET):** A control region through which the principal-current charge carriers pass and whose cross-section is determined by the voltage applied to a gate, the principal current being the result of an applied drift field.	JESD77D, 8/12
NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.	
characteristic: (1) A distinguishing feature of a process or its output on which variables or attributes data can be collected.	EIA-557-B, 2/06 EIA-599-A, 6/98 JEP131B, 4/12 JEP132, 7/98 JESD659B, 2/07
(2) An inherent and measurable property of a device. (Ref. IEC 134.)	JESD77D, 8/12 JESD99C, 12/12
NOTE Such a property may be electrical, mechanical, thermal, hydraulic, electromagnetic, or nuclear and may be expressed as a value for stated or recognized conditions.	
(3) A set of related values, usually shown in graphical form. (Ref. IEC 134.)	JESD77D, 8/12 JESD99C, 12/12
characteristic life (for the Weibull distribution)(η): The time at which F(t) equals ($1 - e^{-1}$) (≈63.2%).	JESD74A, 2/07

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Terms, abbreviations, letter symbols, and definitions	References
characteristic, (static) (1) **(of a bidirectional diode thyristor):** A function, usually represented graphically, relating the thyristor voltage to the thyristor current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium. NOTE The word "static" is usually omitted except when a distinction between static and dynamic characteristics is necessary.	JESD77D, 8/12
(2) **(of a unidirectional diode thyristor):** A function, usually represented graphically, relating the anode voltage to the anode current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium. NOTE The word "static" is usually omitted except when a distinction between static and dynamic characteristics is necessary.	JESD77D, 8/12
characterization: A description of the characteristics of a product or process by mathematical modeling, design of experiments, or statistical data evaluation. NOTE Methods of statistical data evaluation are described in EIA-557 and JEP132.	EIA-557-B, 2/06 JEP153,1/08
charge-coupled device (CCD): A charge-transfer device that stores charge in potential wells and transfers this charge almost completely as a packet by translating the position of the potential wells.	JESD99C, 12/12
charge-coupled image sensor: A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.	JESD99C, 12/12
charged-device model (CDM): A specified circuit characterizing an electrostatic discharge (ESD) event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.	JESD22-C101E, 12/09
charge-handling capacity; full-well capacity: The maximum amount of charge that can be stored in a potential well and transferred without overflow into adjacent wells.	JESD99C, 12/12
charge packet: The portion of the total charge that is transferred from one position to the next position.	JESD99C, 12/12
charge pump: (1) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected in series with that source to make available a voltage greater than that of the source. NOTE This type of dc-to-dc converter is sometimes called a voltage doubler or, when several stages are cascaded, a voltage multiplier. (2) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected to make available a voltage whose polarity is opposite to that of the source.	JESD99C, 12/12
charge-regeneration stage (of a digital circuit): A region of a charge-transfer device that is used to refresh stored digital information.	JESD99C, 12/12

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Terms, abbreviations, letter symbols, and definitions **References**

charge-transfer device (CTD): A device in which operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface or through the interconnections on the semiconductor surface. JESD99C, 12/12

charge-transfer efficiency (CTE) (η): The fraction of the signal charge that is transferred from one storage region to the next storage region. JESD99C, 12/12

charge-transfer inefficiency (CTI) (ε); incomplete charge-transfer coefficient: The fraction of the signal charge that fails to be transferred from one storage region to the next storage region. JESD99C, 12/12

charge-transfer loss (δ): The fractional loss of signal charge that occurs when a charge packet is transferred from one storage region to the next storage region and that packet is preceded by one or more packets of zero charge. JESD99C, 12/12

NOTE The loss of charge is that charge necessary to replenish all interface states or bulk traps that have emptied since the last passage of charge through the device. It is not charge that is left behind as it is in the case of charge-transfer inefficiency.

charge-transfer time (of a charge-transfer device): The time required to move a specified fraction of a charge packet from one storage region to the next. JESD99C, 12/12

check list: A simplified listing of the specified criteria that may be checked off during an audit or inspection. EIA-557-B, 2/06

check sheet: A form for data collection. EIA-557-B, 2/06

chip (1) **(semiconductor):** A separated part of a wafer (or, in some cases, a whole wafer) intended to perform a function or functions in a device. JESD77D, 8/12
JESD99C, 12/12

(2) **(in a package):** An area along an edge or corner where some material has broken off. JESD27, 8/93
Rescinded 5/11

chip attach(ment): See "die bond".

chip, beam-lead: A chip employing electrical terminations in the form of tabs extending beyond the edge of the chip for direct bonding to a mounting substrate. JESD99C, 12/12

chip carrier: A package whose chip cavity or mounting area occupies a major fraction of the package area and whose terminals consist of metal pad surfaces (on leadless versions) or leads formed around the sides and under the package or out from the package (on leaded versions). JESD99C, 12/12

NOTE The term "chip carrier" has been replaced by "quad flatpack" (for terminals on three or four sides) and "small-outline package" (for terminals on one or two sides).

chip enable (E): The input that, when true, permits active operation including the input and/or output of data and, when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

chip-enable input: A control input that, when active, permits operation of the integrated circuit and, when inactive, causes the integrated circuit to be in a reduced-power standby mode. (Ref. IEC 748-2.) JESD100-B, 12/99

NOTE A chip-enable input is a clock or strobe input that significantly affects the power dissipation of the integrated circuit. For example, it may be the cycle control input of a dynamic memory or a power-reduction input of a static memory.

chip, face-down: A chip whose electrical terminations are on the side that is intended to be attached to the mounting substrate. JESD99C, 12/12

chip, face-up: A chip whose electrical terminations are on the side opposite the one that is intended to be attached to the mounting substrate. JESD99C, 12/12

chip, flip: A chip with bump contacts spaced around the device and intended for face-down mounting. JESD99C, 12/12

chip-out (1) **(in a package):** An area where a crack has allowed a portion of the insulator to break away, leaving a void in the insulator at the metal interface. JESD9B, 5/11

(2) **(in a wafer or die):** A visual anomaly that is a pit resulting from the removal of a volume of material by mechanical impact. JESD22-B118, 3/11

chip-package interaction (CPI): (1) The interaction between the semiconductor package stresses and the semiconductor device. JEP156, 3/09

NOTE Package stresses are caused by thermal, mechanical, or chemical mechanisms.

(2) For the purpose of JEP158, the interaction between stresses induced by the semiconductor package and the semiconductor chip whether alone or within the semiconductor 3-D chip stack. JEP158, 11/09

chip-scale package: A package whose area is generally no greater than 120% of the area of the semiconductor device it contains. JESD30E, 8/08

NOTE The package size does not necessarily change with changes in the size of the die.

chip select [S(n)(x)]: The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating, Z) for MOS and TTL devices and low (L) for ECL devices, and the device becomes insensitive to a write command. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the value of "a", "b", "c", etc. JESD21-C, 1/97

chip-select input: A control input that, when active, permits operation of the integrated circuit and, when inactive, prevents input or output of data to or from the integrated circuit. (Ref. IEC 748-2.) JESD100-B, 12/99

chip stack: A group of interconnected silicon chips stacked vertically to make a 3-D structure. JEP158, 11/09

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Terms, abbreviations, letter symbols, and definitions	References
chip-to-chip interconnect; level D interconnect: The structure that connects one chip in a 3-D stack to another chip in that 3-D stack. NOTE Examples of this structure include, but are not limited to, solder bumps and copper pads	JEP158, 11/09
chip-to-substrate-interconnect; level 1 (L1) interconnect: The structure that connects a chip to a substrate. NOTE 1 Examples of this structure include, but are not limited to, solder bumps and copper columns. NOTE 2 Level 1 (L1) interconnect is not associated with JP001 Foundry Level 1 Qualification (L1).	JEP156, 3/09 JEP158, 11/09
circuit element: Any constituent part of a circuit that contributes directly to its operation and performs a definable function. NOTE 1 Examples include transistors, resistors, capacitors, inductors, and interconnections. NOTE 2 The definition in JESD12-1B excludes interconnections.	JESD12-1B, 8/93# JESD93, 9/05 JESD99C, 12/12
circuit element, active: A circuit element that contributes qualities to a circuit function other than those contributed by a passive circuit element, e.g., rectification, switching, gain, or conversion of energy from one form to another. NOTE 1 Examples include diodes, transistors, active integrated circuits, and light-sensing or light-emitting devices. NOTE 2 Active physical circuit elements may also be used to act as passive physical circuit elements, e.g., to provide resistance and/or capacitance to a circuit function.	JESD93, 9/05 JESD99C, 12/12
circuit element, parasitic: A circuit element that is an unavoidable adjunct of one or more other circuit elements.	JESD99C, 12/12
circuit element, passive: A circuit element primarily contributing resistance, capacitance, inductance, ohmic interconnection, or a combination of these to a circuit function. NOTE Examples include resistors, capacitors, inductors, passive filters, and interconnections.	JESD93, 9/05 JESD99C, 12/12
circuit initialization: A sequence of stimuli that set internal nodes of a circuit to a predictable state.	JESD12-5, 8/88
circulating bias charge: Synonym for “bias charge”.	JESD99C, 12/12
CISC: See “complex-instruction-set computer”.	
CK: See “input and output clock”.	
CKE: See “clock enable”.	
CL: See “clear (CL)”.	

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

clamped package: A package for high-current devices, in the form of a cylinder with a flat, circular, high-current terminal on each end, that is intended to be clamped between two busbars acting as heat sinks. JESD30E, 8/08

class: A categorization of similar characteristics for the purpose of reporting ppm nonconforming. Examples of classes include functional (ppm1), electrical (ppm2), visual/mechanical (ppm3), and hermetic (ppm4). JESD16-A, 4/95

classification temperature: The maximum body temperature at which the component manufacturer guarantees the component moisture sensitivity level as noted on the caution and/or bar code label per J-STD-033. J-STD-020D.1, 3/08

clear: To preset a storage or memory device to a prescribed state, usually that denoting zero. (Ref. IEEE Std 100.) JESD100-B, 12/99

NOTE In the field of nonvolatile memories, "clear" conventionally means to set the outputs of the memory to the high logic level.

clear (CL): An input that, when true, causes all cells in the memory array to be cleared to their zero state. JESD21-C, 1/97

clear algorithm (for a flash EEPROM): The timed sequence of signals necessary to clear the memory. JESD100-B, 12/99

clearance distance: The shortest external distance measured through air from the anode terminal to the cathode terminal of a rectifier diode, or from the anode terminal to the cathode or gate terminal of a thyristor. JESD4, 11/83

clear disturb: The corruption of data in one location caused by the clearing of data at another location. JESD100-B, 12/99

clock cycle: The time period, generally derived from an oscillator, that is used for sequencing data flow and synchronizing one or more functions. (Ref. IEC 824.) JESD100-B, 12/99

clock distribution network: The structure by which clock signals are distributed within a device. JESD12-1B, 8/93
JESD99C, 12/12

clock driver: A driver intended for use with clock signals. JESD99C, 12/12

clock enable (CKE): In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function. JESD21-C, 1/97

clock frequency, maximum (f_{max}): The highest frequency at which a clock input of an integrated circuit can be driven while maintaining proper operation. JESD12-1B, 8/93
JESD99C, 12/12

clock skew: The difference in the arrival times of a common clock edge at any two circuit elements. JESD12-1B, 8/93
JESD99C, 12/12

C-mode: See "acoustic data, C-mode".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
CMOS-and-DMOS (C/DMOS) technology: A technology for combining complementary metal-oxide-semiconductor (CMOS) field-effect devices and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.	JESD99C, 12/12
coaxial package: A transistor package designed to mount directly into coaxial lines.	RS-435, 4/76
cold plate: A heat absorber usually operating at some known or fixed temperature.	JESD51-1, 12/95 JESD51-13, 6/09
collected charge: The charge collected at a particular device node during and immediately after the passage of a particle. NOTE 1 This amount of charge is determined by measurement immediately after the passage of a particle. NOTE 2 The amount of collected charge is dependent on the geometry and doping of the node, the particle mass, energy, and trajectory, and the density and type of material in the volume penetrated by the incident radiation.	JESD89A, 10/06
collecting junction: A semiconductor junction in an operating condition in which the net flow of charge carriers of each type across the junction is in the direction from the region where they are minority carriers to the region where they are majority carriers, i.e., in the direction of the force resulting from the internal electric field.	JESD77D, 8/12
collection region (within a semiconductor device): A functional region that receives the principal current leaving the control region.	JESD77D, 8/12
collector (nonspecific)**:** The overall combination of collector transition region, collector region, collector terminal, and the interface between them. NOTE This term should be used in this manner only when no confusion is likely to occur.	JESD77D, 8/12
collector-base time constant ($r_b'C_c$): The product of the intrinsic base resistance and collector capacitance under specified small-signal conditions.	JESD10, 1/76
collector-base voltage, emitter open (V_{CBO}): The voltage between the collector and base terminals when the emitter terminal is open-circuited.	JESD10, 1/76 JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

collector cutoff current, base open (I_{CEO}):
collector cutoff current, base short-circuited to emitter (I_{CES}):
collector cutoff current, circuit between base and emitter (I_{CEX}):
collector cutoff current, resistance between base and emitter (I_{CER}):
collector cutoff current, voltage between base and emitter (I_{CEV}):
The dc current into the collector terminal when it is biased in the reverse direction* with respect to the emitter terminal, and the base terminal is, respectively, JESD10, 1/76 JESD77D, 8/12

— open-circuited.
— short-circuited to the emitter terminal.
— returned to the emitter terminal through a specified circuit.
— returned to the emitter terminal through a specified resistance.
— returned to the emitter terminal through a specified voltage.

*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for npn transistors or negative for pnp transistors with respect to the emitter terminal.

collector cutoff current, emitter open (I_{CBO}): The dc current into the collector terminal when it is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited. JESD10, 1/76 JESD77D, 8/12

collector-emitter saturation voltage: See "saturation voltage, collector-emitter".

collector junction (of a thyristor): The junction across which the polarity of the voltage reverses when switching occurs. (Ref. EIA-397.) JESD77D, 8/12

collector region, functional: A collection region that acquires principal-current charge carriers from a controlling base region through an associated collecting junction. JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal. In the normal operating mode, this functional region is located in the collector region; in the inverse operating mode, it is located in the emitter region.

collector region, physical: (1) A region through which a primary flow of charge carriers leaves the base. (Ref. 60 IRE 28.S1.) JESD10, 1/76

(2) The physical region that is designed by the manufacturer to contain the collection region in the normal operating mode and, in a simple discrete transistor, is externally accessible by the designated collector terminal. JESD77D, 8/12

collector terminal (C, c): The specified externally available point of connection to the collector region. JESD77D, 8/12

color temperature: The temperature of a blackbody having the same visible color as that of a given non-blackbody radiator. JESD77D, 8/12

column address (CA): In an address-multiplexed DRAM, the address field that is captured by the column enable clock, CAS. When the column address numbering is significant for device operation, the addresses are numbered beginning with 0. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

column enable (CAS; CE): An enable signal that on some dynamic RAMs actuates only the column-oriented internal circuits and the data input/output circuits. Most devices normally require the RAS signal to be present for the CAS signal to be effective. In some newer designs, however, special sequences of the RAS and CAS signals are used to actuate certain special device control functions. For devices that have one CAS per output, the CASs are numbered beginning with 0. For two-byte devices that have one CAS per byte, the CASs are designated LCAS and UCAS. LCAS affects DQ0–DQ7, and UCAS affects DQ8–DQ15. For devices that have more than two bytes and one CAS per byte and for all modules that have one CAS per byte, the CASs are numbered beginning with 0. CAS0 affects DQ0–DQ7, CAS1 affects DQ8–DQ15, CAS2 affects DQ16–DQ23, and CAS3 affects DQ24–DQ31. JESD21-C, 1/97

combinational fault: A functional fault that is not affected by the sequence of the input stimuli. JESD12-5, 8/88

combinational logic function: A logic function in which there exists one and only one resulting combination of states of the outputs for each possible combination of input states. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

NOTE The words “combinative” and “combinatorial” have also been used in place of combinational.

common cause: A source of natural variation that affects all the individual values of the process output being studied. In control chart analysis it appears as part of the random process variation. EIA-557-B, 2/06 JEP132, 7/98 JESD659B, 2/07

common-mode input voltage (V_{IC}): The average of the voltages at two input terminals of a circuit. JESD99C, 12/12

common-mode input voltage range (V_{ICR}): The range of common-mode input voltage that, if exceeded, will cause the total harmonic distortion of the output signal resulting from the common-mode input to exceed a specified maximum value. JESD99C, 12/12

common-mode output voltage (V_{OC}): (1) The average of the voltages at two output terminals of a circuit. JESD99C, 12/12

(2) The ac voltage between two output terminals (or the output terminals and ground for circuits with one output) when ac signals of identical phase and amplitude are applied to the input terminals.

common-mode rejection ratio (k_{CMR} or CMRR): The ratio of the differential voltage amplification to the common-mode voltage amplification. JESD99C, 12/12

common-mode voltage: The average voltage level of the two signals on a differential line. JESD96, 4/04

common-source small-signal (forward transfer, input, output, reverse transfer) conductance (g_{fs}, g_{is}, g_{os}, g_{rs}): The real part of the corresponding common-source small-signal admittance y_{fs}, y_{is}, y_{os}, or y_{rs}. JESD24, 7/85 JESD77D, 8/12

NOTE Symbols in the forms of g_{xx} and $y_{xx(real)}$ are equivalent.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

common-source small-signal short-circuit forward transfer admittance (y_{fs}): The ac rms drain current divided by the ac rms gate-source voltage with the drain-source voltage held constant. JESD24, 7/85 JESD77D, 8/12

NOTE The fact that the drain-source voltage is held constant implies that the drain terminal is ac short-circuited to the source terminal.

common-source small-signal short-circuit input admittance (y_{is}): The ac rms gate current divided by the ac rms gate-source voltage with the drain-source voltage held constant. JESD24, 7/85 JESD77D, 8/12

NOTE The fact that the drain-source voltage is held constant implies that the drain terminal is ac short-circuited to the source terminal.

common-source small-signal short-circuit output admittance (y_{os}): The ac rms drain current divided by the ac rms drain-source voltage with the gate-source voltage held constant. JESD24, 7/85 JESD77D, 8/12#

NOTE The fact that the gate-source voltage is held constant implies that the gate terminal is ac short-circuited to the source terminal.

common-source small-signal short-circuit reverse transfer admittance (y_{rs}): The ac rms gate current divided by the ac rms drain-source voltage with the gate-source voltage held constant. JESD24, 7/85 JESD77D, 8/12

NOTE The fact that the gate-source voltage is held constant implies that the gate terminal is ac short-circuited to the source terminal.

commutation: The transfer of unidirectional current between rectifier circuit elements that conduct in succession. JESD282-B, 4/00

companding DAC: A digital-to-analog converter whose transfer function complies with a compression or expansion law. JESD99C, 12/12

NOTE 1 The corresponding analog-to-digital coverter normally consists of such a companding DAC and additional external circuitry.

NOTE 2 The compression or expansion law is usually a logarithmic function, e.g., A-law or μ-law.

comparator, differential voltage: A device that compares an input voltage with a reference voltage and indicates which is greater by means of a digital output. JESD99C, 12/12

comparison unit (CU): (1) The change in a temperature-sensitive parameter divided by the change in a dependent heating-condition parameter. JESD51-1, 12/95

(2) For an integrated circuit, the change in temperature-sensing diode forward junction voltage under measurement conditions divided by the change in heating current, $\Delta V_F/\Delta I_H$. This allows for thermal comparison of one device to another when the heating voltage remains constant.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

complementary integrated circuit technology: The technology, as applied to integrated circuits, whereby active elements of both polarities are fabricated as single-chip elements on or within the same substrate. JESD99C, 12/12

NOTE For example, a complementary bipolar semiconductor integrated circuit is one that employs both npn and pnp bipolar transistors in the same semiconductor substrate, and a complementary MOS integrated circuit is one that employs both n-channel and p-channel field-effect transistors in the same semiconductor substrate.

complementary metal-oxide semiconductor (CMOS) technology: A technology for combining p-channel and n-channel metal-oxide-semiconductor field-effect transistors in a single-chip integrated circuit. JESD99C, 12/12

complete data: All available data from all units in the stress test, including those in the failure set. JESD37, 10/92

complex-instruction-set computer (CISC): A microcomputer or microprocessor that performs multiple tasks per complex instruction, usually requiring multiple clock cycles. JESD100-B, 12/99

compliance: (1) **(general):** Conformity in fulfilling official requirements. Merriam-Webster's Collegiate Dict.

(2) **(of test equipment):** The maximum current- or voltage-forcing capability of the test equipment. JESD35-A, 4/01

compliance, current (of a digital-to-analog converter) ($\Delta I_{O(op)}$): The permissible range of output current within which the specifications are valid. JESD99C, 12/12

compliance, voltage (of a digital-to-analog converter) ($\Delta V_{O(op)}$): The permissible range of output voltage within which the specifications are valid. JESD99C, 12/12

component: (1) A constituent part. JESD77D, 8/12
JESD99C, 12/12

NOTE 1 Examples include source and drain regions as components of transistors, lead frames and dice as components of packaged integrated circuits, resistors and integrated circuits as components of printed circuit boards, motherboards as components of computers, LCD screens as components of monitors, ac and dc components of complex waveforms, and loops and algorithms as components of software programs.

NOTE 2 Unless the context identifies the thing of which a component is a part, a descriptive prepositional phrase identifying the thing should follow the word "component".

NOTE 3 The classification of an item as a device or as a component depends upon the intention of the owner at the time of classification.

(2) An individual part such as a connector, capacitor, integrated circuit, socket, multichip module, hybrid circuit, etc. J-STD-609.01, 2/11

component (of a hybrid integrated circuit): A part that is mounted within the package and that contributes to the composition of the circuit. JESD99C, 12/12

NOTE For electronic components, a distinction is made between integrated components and discrete components.

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Terms, abbreviations, letter symbols, and definitions	References
component, active (of a hybrid integrated circuit): A component in which at least one circuit element is an active circuit element.	JESD99C, 12/12
component, discrete (of a hybrid integrated circuit): A discrete device that serves as a component of a hybrid integrated circuit.	JESD99C, 12/12
component, integrated (of a hybrid integrated circuit): An integrated circuit, completed or partially completed, that serves as a component of a hybrid integrated circuit.	JESD99C, 12/12
component, passive (of a hybrid integrated circuit): A component in which all circuit elements are passive.	JESD99C, 12/12
component problem: Any problem related to the supplier's component that causes failure during, or interruption to, the customer's production flow or failures of their products in the final application, e.g., a) administrative problems (wrong product, wrong quantity, packing/materials, orientation, date code, paperwork, shipping damage, shipping error, labeling, etc.), b) electrical problems (functional, parametric, timing, continuity, programming, etc.), and c) visual/mechanical problems (marking, leads, package body, solderability, contamination, etc.).	JESD671B, 6/12
component, (semiconductor): A packaged semiconductor device.	IPC/JEDEC-9702, 6/04 JEP140, 6/02 JESD22-B104C, 11/04 JESD22-B110A, 11/04 JESD22-B111, 7/03 JESD89A, 10/06
concave warpage: Negative (-) warpage resulting in the package corners being farther from the contact plane than the center of the bottom surface of the package substrate.	JESD22-B112A, 10/09
concentric: Having a common center point.	JESD9B, 5/11
conducting [conduction] period (of a rectifier circuit element): The part of an alternating-voltage cycle during which the current flows in the forward direction. NOTE The forward period is not necessarily the same as the conducting period because of circuit parameters and semiconductor rectifier diode characteristics.	JESD282-B, 4/00
conductive material: A material that has a surface or volume resistance less than 1×10^4 ohms. NOTE A conductive material is not necessarily antistatic.	JESD625B, 1/12
conductivity-connected charge-coupled device (C^4D): A charge-coupled device that uses doped regions between the potential wells and hence becomes a hybrid between the charge-coupled device and a bucket-brigade device.	JESD99C, 12/12
configure: Synonym for “program”.	JESD32, 6/96

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Terms, abbreviations, letter symbols, and definitions **References**

connection, electrical (within a semiconductor device): An electrically conducting element that functions as a pathway between other elements, including terminals, and whose primary purpose is to conduct electric current in a confined manner. JESD99C, 12/12

NOTE The connection may either consist of a separate conductive entity such as a wire or metallic film or be an integral part of the body.

connect (state): A state in a switch device characterized by a minimal series impedance of the designated electrical path. JESD73, 6/99
JESD73-1, 8/01
JESD73-2, 8/01
JESD73-3, 8/01
JESD73-4, 11/01

constant-current threshold voltage ($V_{T(ci)}$): The gate-source voltage at which the drain current is equal to a constant current, appropriate for a given technology, times the ratio of gate width (W) to gate length (L). $V_{T(ci)}$ can be calculated using JESD28-A, 12/01#
JESD60A, 9/04
JESD90, 11/04

$$V_{T(ci)} = V_{GS} \text{ (at } I_D = I_{D0}\, W/L)$$

where W and L are the gate width and gate length as printed on the wafer.

NOTE I_{D0} is selected for a given technology such that $V_{T(ci)}$ is in the subthreshold region of the device. For N-MOSFET devices, JESD28-A suggests 0.1 μA; for P-MOSFET devices, JESD60 suggests –0.025 μA.

contact, bump; ball contact; raised pad; pedestal: (1) A contacting pad that rises substantially above the surface level of the chip. JESD99C, 12/12

(2) A raised pad on the substrate that contacts a flat land area of the chip.

contact plane: A plane parallel to the reference plane passing through the lowest contact point on the package substrate. JESD22-B112A, 10/09

containment: Interim action(s) taken to minimize the effects of component problems on customers until corrective actions are implemented. JESD671B, 6/12

content-addressable memory (CAM): A memory that responds with all the data in a storage zone if a portion of that data matches the data used for addressing the memory. (Ref. IEC 748-2.) JESD100-B, 12/99

continuous improvement: The methodology whereby quality improvement tools (e.g., statistical process control (SPC), Ishikawa diagram, design of experiments (DOE), etc.) are applied to a process to improve measurable attributes (e.g., repeatability, efficiency, predictability, etc.). JEP132, 7/98

contrast (of a mark on a device): The difference in luminance ("brightness") between the mark and the surrounding device surface. JESD22-B114A, 5/11

NOTE Contrast is typically quantified by comparison of minimum and maximum reflectance values

control: A corrective action process based on feedback. JEP131B, 4/12

control bus: A bus carrying the signals that regulate system operations. (Ref. ANSI X3.172.) JESD100-B, 12/99

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Terms, abbreviations, letter symbols, and definitions	References
control-charge region (within a semiconductor device): A functional region that contains the controlling charge and that may or may not be the path for the principal current.	JESD77D, 8/12
control chart: A graphic representation of a process characteristic showing plotted values of some statistic gathered from that characteristic, a central line, and one or two statistically derived control limits. Two basic uses are to determine whether a process has been operating in statistical control and to aid in maintaining statistical control.	EIA-557-B, 2/06 JEP132, 7/98
control current: Current at the control terminals.	JESD14, 11/86
controllability: The ability of a node to be established at specific logic state(s) by applying stimuli to the circuit's externally accessible node(s).	JESD12-5, 8/88
controlled edge: The output signal edge that is locked to the phase-locked loop (PLL) trigger reference.	JESD65B, 9/03
controlled SPCM: A semiconductor power-control module (thyristor SPCM, transistor SPCM, thyristor-diode SPCM, or transistor-diode SPCM) with internal control-signal processing circuitry that may have provisions for external adjustment.	JESD14, 11/86
control limits: The maximum allowable variation of a process characteristic due to common causes alone. Variation beyond a control limit may be evidence that special causes are affecting the process. Control limits are calculated from process data and are usually represented as a line (or lines) on a control chart. They are not to be confused with engineering specification limits.	EIA-557-B, 2/06 JEP132, 7/98 JESD659B, 2/07
control loop: A corrective action system based on a feedback procedure.	EIA-557-B, 2/06
control region (within a semiconductor device): A functional region through which the principal-current charge carriers flow and are controlled in the manner for which the device is intended.	JESD77D, 8/12
control terminals: The terminals to which the external control signal is applied.	JESD14, 11/86
control voltage: The voltage at the control terminals.	JESD14, 11/86
convection oven: A controlled-temperature chamber in which the heat is transferred by air flow, rather than by conduction or radiation. NOTE The chamber must be capable of maintaining specified temperatures over the entire working area.	JEP153,1/08
conversion code (1) **(of an analog-to-digital converter):** The set of correlations between each of the fractional parts of the total analog input range and the corresponding digital output codes. NOTE Examples of analog-to-digital converter output code formats are straight binary, 2s complement, and binary-coded decimal.	JESD99C, 12/12
(2) **(of a digital-to-analog converter):** The set of correlations between each of the digital input codes and the corresponding analog output values.	JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

conversion efficiency (1) **(of a photon-emitting device):** The maximum available luminous or radiant flux output divided by the total input power. JESD77D, 8/12

(2) **(of a photovoltaic diode):** The maximum available power output resulting from photovoltaic operation divided by the total incident radiant flux. JESD77D, 8/12

conversion loss (of a mixer, mixer diode, or harmonic generator) (L_C): The ratio of available input power at a single frequency to the available signal-output power, not including intrinsic mixer noise or power converted from other than the signal-input frequency. JESD77D, 8/12 JESD311A, 11/81

NOTE Delivered signal-output power may be used, in which case the loss is referred to as "conversion insertion loss".

conversion rate (of an externally controlled analog-to-digital converter) (f_c): The number of conversions per unit time. JESD99C, 12/12

NOTE 1 The maximum conversion rate should be specified for full resolution.

NOTE 2 The conversion rate is usually expressed as the number of conversions per second.

NOTE 3 Because of settling or recovery time, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

conversion time (of an analog-to-digital converter) (t_c): The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog value. JESD99C, 12/12

convex warpage: Positive (+) warpage resulting in the package corners being closer to the contact plane than the center of the bottom surface of the package substrate. JESD22-B112A, 10/09

cool-down time: The period of time between successive applications of trigger pulses, or the period of time between the removal of the V_{supply} voltage and the application of the next trigger pulse. JESD78D, 11/11

coplanarity: The condition where an interrupted surface, or two or more surfaces, have all their elements in one plane. The tolerance zone is established by two parallel planes between which all elements of the interrupted surface must lie. This is analogous to the flatness requirement for a continuous surface. JESD95-1, 3/97

NOTE See also "deviation from coplanarity".

coplanarity, deviation from: See "deviation from coplanarity".

coprocessor: A processing unit that extends the capabilities of its main processor, directly accesses the memory of that processor, and does not operate autonomously. (Ref. IEC 824.) JESD100-B, 12/99

core-limited integrated circuit: An integrated circuit whose chip size is determined by the gate core area required for the functional implementation. JESD12-1B, 8/93 JESD99C, 12/12

corrective action: Actions taken to eliminate the root cause(s) of an existing nonconformity or other undesirable situation. JESD671B, 6/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
corrective action request: A formal request from a customer to a supplier requiring an investigation into the root cause of a specific problem and the steps taken to prevent recurrence.	JEP146A, 1/09
corrosion: The breaking down or destruction of a material, especially a metal, through a chemical reaction. NOTE The most common form of corrosion is rusting, which occurs when iron combines with oxygen and water.	JESD9B, 5/11
countable failure: A failure due to an inherent defect in an electronic device during early-life-failure (ELF) stress tests. NOTE Failures due to electrical overstress (EOS), electrostatic discharge (ESD), mechanical damage, etc., are not counted, but the failing devices are considered to have completed testing through the last successful readout when computing device-hours.	JESD74A, 2/07
coupled non-supply terminal pair; coupled non-supply pin pair: Two terminals, such as differential amplifier inputs or low-voltage differential signaling (LVDS) terminals, that have between them an intended direct current path, such as a pass gate or resistor. NOTE These pairs include analog and digital differential pairs and other special function pairs (e.g., D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN, etc.).	JS-001-2012, 4/12#
cover: A lid that is hermetically sealed to a package by a process such as soldering, seam-sealing, projection welding, etc.	JESD9B, 5/11
CPI: See “chip package interaction”.	
CPU: See “central processing unit”.	
crack (1) **(in a wafer or die):** A fracture in within the bulk material.	JESD22-B118, 3/11
(2) **(in a package):** A line of fracture without complete separation.	JESD27, 8/93 Rescinded 5/11
(3) **(within a bulk material)**: A separation.	J-STD-020D.1, 3/08
crack, circumferential (in a package): A crack that appears on the surface of an insulator and follows the shape of the package hole.	JESD9B, 5/11
crack, meniscus (in a package): A crack confined to the meniscus area of the seal above the average low point of the insulator.	JESD9B, 5/11
crack, radial (in a package): A crack that appears on the surface of the insulator and either starts at the package and extends towards the lead or starts at the lead and extends towards the package beyond the average low point of the insulator.	JESD9B, 5/11
crazing: Multiple minute cracks that appear on the surface of the insulator.	JESD9B, 5/11
creepage distance: The shortest path measured over the external insulator surface, from the anode terminal to the cathode terminal of a rectifier diode, or from the anode terminal to the cathode or gate terminal of a thyristor.	JESD4, 11/83

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

critical: Pertaining to that which significantly impacts product quality and/or reliability. EIA-599-A, 6/98

critical area (of a wafer or die): An area for which the inspection criteria are more stringent. JESD22-B118, 3/11

NOTE The critical area should be stipulated by the appropriate drawing or specification.

critical charge (Q_c): The minimum amount of collected charge that will cause a device node to change state. JESD57, 12/96#
JESD89A, 10/06
JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

critical failure mechanism: In semiconductor devices, any potential physical failure mechanism that exhibits one or more of the following: intermittency (e.g., bond lifts), increasing failure rate (e.g., electromigration), and inconsistent or unpredictable failure kinetics (e.g., stress-induced metal voiding). JESD659B, 2/07

critical moisture limit: The maximum safe equilibrium moisture content for a specific encapsulated device at reflow assembly or rework. JEP160, 11/11

critical path: A signal path that determines the performance of a design. JESD12-1B, 8/93
JESD99C, 12/12

critical (process) node: A node in the process flow whose output has a significant impact on the process. EIA-557-B, 2/06
JEP132, 7/98
JESD93, 9/05

critical sealant (on a chip or substrate): A polymeric material designed to completely or partially cover, intimately adhere to, and protect critical electrical features such as metal wire-bonds, metal leadframe, metal fan-out on a substrate, or the chip active face and diced edges. JESD22-B101B, 8/09

crossover: A crossing where a portion of an interconnect pattern passes over a portion of another interconnect pattern and is separated from it by a thin dielectric layer. JESD99C, 12/12

cross section (in SEE testing) (σ): The number of events per unit fluence. JESD57, 12/96

NOTE If the depth of the sensitive volume is small compared to its lateral dimensions, the SEE cross section (σ) can be calculated as follows:

$$\sigma = \text{number of events} / (\text{fluence} \times \cos\theta)$$

where θ is the angle of incidence of the ion.

crossunder: A crossing where a conductive path fabricated into the active substrate for the sole purpose of interconnection passes under a portion of an interconnect pattern and is separated from it by a thin dielectric layer. JESD99C, 12/12

CSSP: See "customer-specific standard product".

CTD: See "charge-transfer device".

CU: See "comparison unit".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

cumulative distribution function of the time-to-failure; cumulative mortality function [F(t)]: The probability that a device will have failed by a specified time t_1, or the fraction of units that have failed by that time. JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07 JESD85, 7/01

NOTE 1 The value of this function is given by the integral of f(t) from $t = 0$ to $t = t_1$ and is generally expressed in percent (%) or in parts per million (ppm) for a defined early-life failure period. See "probability density function of the time-to-failure" for f(t).

NOTE 2 The abbreviation CDF is often used; however, the symbol F(t) is preferred.

cumulative fraction failing (CFF): The total fraction failing based on the starting sample size over a given time interval. JEP143C, 7/12 JESD74A, 2/05

NOTE This value is generally expressed in percent (%) or in parts per million (ppm).

cumulative hazard function [H(t)]: The fraction of units that have failed referenced to the survivors (not to the initial number of units). JEP122G, 10/11 JEP143C, 7/12 JESD85, 7/01#

NOTE The value of this function at a specified time t_1 is given by the integral of h(t) from $t = 0$ to $t = t_1$. See "instantaneous failure rate; hazard rate" for h(t).

cumulative reliability function [R(t)]: The probability that a device will still be functional at a specified time t_1, or the fraction of units surviving to that time. JEP122G, 10/11 JEP143C, 7/12 JESD85, 7/01

NOTE R(t) = 1 – F(t). See "cumulative distribution function of the time-to-failure" for F(t).

current, dc [base terminal (I_B), collector terminal (I_C), emitter terminal (I_E)]: The value of the dc current into the terminal indicated by the subscript. JESD10, 1/76

current delay time (of a transistor) (t_{di}): The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the collector current waveform rises to 10% of its on-state amplitude, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance. JESD77D, 8/12

current density at failure (J_F): The value of the last recorded current density in the narrowest region of the test structure during the control cycle before the failure criterion, R_{FC}, is satisfied. JEP119A, 8/03

current density, starting (J_S): The current density in the narrowest region of the test structure at the initial application of the forcing current for SWEAT stressing. JEP119A, 8/03

current fall time (of a transistor) (t_{fi}): The time interval during which the collector (or drain) current changes from 90% to 10% of its peak on-state value, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance. JESD77D, 8/12

current, instantaneous total value [base terminal (i_B), collector terminal (i_C), emitter terminal (i_E)] terminal (i_E)]: The instantaneous total value of alternating current into the terminal indicated by the subscript. JESD10, 1/76

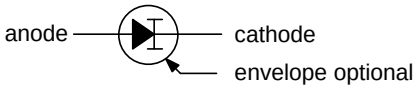
The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

current-limit sense voltage (of a voltage regulator): The current-sense voltage at which current limiting occurs. JESD99C, 12/12

current-regulator diode: A diode that limits current to an essentially constant value over a specified voltage range. JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



current return path: The configuration of conductors, in series with the lead under test, that closes the current loop needed to perform inductance measurements. JEP123, 10/95

current rise time (of a transistor) (t_{ri}): The time interval during which the collector (or drain) current changes from 10% to 90% of its peak off-state value, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance. JESD24, 7/85
JESD77D, 8/12

current, rms value of alternating component [base terminal (I_b), collector terminal (I_c), emitter terminal (I_e)]: The root-mean-square value of alternating current into the terminal indicated by the subscript. JESD10, 1/76

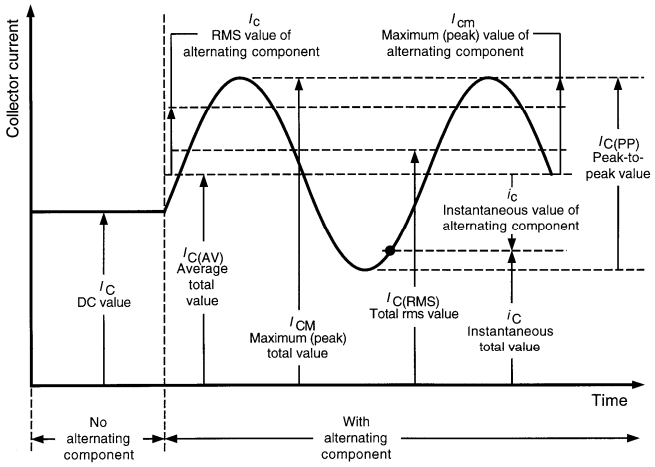


Illustration of the proper use of symbols

current-sense voltage (of a voltage regulator): The voltage that is a function of the load current and is normally used for control of the current-limiting circuitry. JESD99C, 12/12

current tail time (t_{ti}): The time interval following current fall time during which the drain current changes from 10% to 2% of its peak on-state value, ignoring spikes that are not charge-carrier induced. JESD24, 7/85

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Terms, abbreviations, letter symbols, and definitions **References**

current turn-off time ($t_{off(i)}$): The sum of current turn-off delay time and current fall time, i.e., $t_{d(off)i} + t_{fi}$. JESD24, 7/85

current turn-on time ($t_{on(i)}$): The sum of current turn-on delay time and current rise time, i.e., $t_{d(on)i} + t_{ri}$. JESD24, 7/85

customer-processed component: A component that has been soldered to, or de-soldered from, a circuit board or other mounting surface by the customer. JESD22-B101B, 8/09

customer-specific standard product (CSSP): An integrated circuit developed and produced for a single customer but for multiple applications or functions. JESD99C, 12/12

custom integrated circuit: An integrated circuit developed or produced to conform to unique requirements. JESD99C, 12/12

NOTE The terms "full custom" and "semicustom" refer to layout methodologies. The choice of term is subjective, depending on the interpretation of the ratio of unique layouts to standard macrocell layouts from a library.

cusum chart: A statistical process control (SPC) chart in which cumulative deviation from a target is plotted. EIA-557-B, 2/06

cutoff frequency: The frequency at which the voltage amplification is 3 dB below the voltage amplification at a specified frequency. JESD99C, 12/12

cycle: (1) A sequence of operations in which one set of events is completed. JESD100-B, 12/99

(2) Any set of operations that is repeated regularly in the same sequence.

NOTE The operations may be subject to variations on each repetition. (Ref. ANSI X3.172.)

cycles to acquire PLL lock (n_L): The number of input clock cycles required for a phase-locked loop (PLL) to lock when operating in the guaranteed operating range with a stable input reference clock frequency. JESD65B, 9/03

cycle time: The time interval between the start and the end of a cycle. JESD100-B, 12/99

NOTE The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

cycle-to-cycle period jitter ($t_{jit(cc)}$): The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs. JESD65B, 9/03

cycling pool: The erase blocks used by a solid-state drive (SSD) during read, program, or erase operations at a specific point in time. JESD218A, 2/11

NOTE The SSD may have additional erase blocks, besides those in the current cycling pool, that may be used as spares or for other purposes. The cycling pool is typically larger than the user-accessible logical block address count.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

D

D; d: See “drain terminal”.

DAC: See “digital-to-analog [D/A] converter”.

damage response: All irreversible changes caused by exposure to a reflow soldering profile. J-STD-020D.1, 3/08

dark condition: The condition attained when the electrical parameter under consideration approaches a value that cannot be altered by further irradiation shielding. JESD77D, 8/12

dark current (I_D): The output current under dark conditions. JESD99C, 12/12

dark current spike: A variation of the dark current that exceeds some specified level above the average value. JESD99C, 12/12

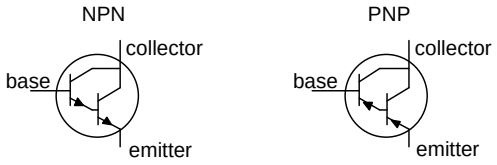
Darlington transistor: A compound semiconductor device consisting of two transistors in which the collectors are connected together and the emitter of the first transistor is connected to the base of the second transistor. JESD77D, 8/12

NOTE 1 The two transistors connected in this manner may be regarded as a compound transistor with three terminals.

NOTE 2 The circuit may include a biasing network.

NOTE 3 The presence of a terminal to provide direct access to the base of the second transistor is optional.

Graphic symbols (ref. IEEE Std 315):



NOTE In the graphic symbols, the envelope is optional if no element is shown connected to the envelope.

data bar polling: A method, used to determine whether the write operation in a memory is complete, wherein the memory is put into the read mode after initiating the write mode; if writing is complete, the outputs take on the addressed stored data, or if writing is not complete, the specified output(s) take on the complement of the last bit(s) written. JESD100-B, 12/99

NOTE If writing is not complete: (a) in older devices, normally all outputs take on the complement of the last bits written; (b) in more modern byte-wide memories, only the most significant output takes on the complement of the last bit written; (c) in word-wide memories, the most significant output of the least significant byte, the most significant output of the entire word, or both of these outputs take on the complement of the last bit written.

data bus: A bus used to communicate data internally and externally to and from processing units, storage devices, or peripheral devices. (Adapted from ANSI X3.172.) JESD100-B, 12/99

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Terms, abbreviations, letter symbols, and definitions **References**

data change: An event in which at least one bit of data is caused to change. JESD100-B, 12/99

NOTE This event may be used as a unit of endurance for erasable programmable read-only memories.

data cycle: A cycle in which each bit changes to its opposite state and back to its original state. JESD100-B, 12/99

NOTE 1 These changes may occur for all bits in parallel or in series, e.g., by page, block, word, byte, or bit.

NOTE 2 This cycle may be used as a unit of endurance for erasable programmable read-only memories.

data error: A type of failure in which the drive fails to return correct data to the host. JESD218A, 2/11

NOTE One data error occurs if a read of a logical sector causes the drive to return an unrecoverable error message or to return incorrect data. Data errors are counted as such even if they are transient.

data input [D(n)(x)]: Those inputs whose states represent the data that is to be written into the selected address on a write cycle of an alterable memory device. When the numbering of the data inputs is significant for device operation, the data inputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc. JESD21-C, 1/97

data input/output [DQ(n)(x)]: The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state. On devices having both serial and parallel access ports, these pins provide access to the parallel RAM port data channels. The suffix (n) is a numeric value indicating the number assignment of a particular pin with numbering starting at 0. In some situations the letter "U" or "L" is used to indicate that the pins are assigned to the upper or lower byte of a two-byte data interface. In devices where the standard supports an optional 9th bit that may be used as a parity bit, the suffix P may be used in lieu of a numeric value. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc. JESD21-C, 1/97

data matrix (symbol): A two-dimensional bar code matrix symbol. JESD22-B114A, 5/11

data output [Q(n)(x)]: The outputs whose states represent the data read from the selected cells. When the device is not selected or enabled, the outputs are usually in a floating (Z, high-impedance) state. When the numbering of the data outputs is significant for device operation, the data outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc. JESD21-C, 1/97

data pattern: The mix of 1s and 0s in the memory and their physical or logical positions. JESD22-A117B, 3/09

NOTE Logical and physical locations often have a fixed relationship; however, the relationship and the physical locations may not be known for some devices.

data point: A value that is either observed or calculated. EIA-557-B, 2/06
JEP132, 7/98

data retention (in a solid-state drive): The ability of an SSD to retain data over time. JESD218A, 2/11

data-retention mode: A standby or battery mode of operation in which the integrity of stored data is maintained although the supply voltage is below that specified for reading or writing. JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

data-retention supply current (of an SRAM offering a data-retention mode) ($I_{CC(DR)}$, $I_{DD(DR)}$, etc.): The supply current in the data-retention mode. JESD99C, 12/12

data-retention supply voltage (of an SRAM offering a data-retention mode) ($V_{CC(DR)}$, $V_{DD(DR)}$, etc.): The supply voltage in the data-retention mode. JESD99C, 12/12

data-retention time: Synonym for "retention time". JESD100-B, 12/99

data rewrite: An operation including one data cycle or at least one data change, in which data is written into an array. JESD100B.01, 12/02

data-transfer/output-enable input [DT/OE(n), TRG(n)]: The input of a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry or enables the data outputs of the parallel port. JESD21-C, 1/97

datum: A theoretically exact point, axis, or plane that is established by tooling and is used in conjunction with a datum feature. The location or geometric characteristics of features of a part are established in relation to the datum. JESD95-1, 3/97

datum feature: The physical portion of a part that, in conjunction with suitable tooling, establishes the datum. JESD95-1, 3/97

NOTE A centerline, by itself, cannot be a datum. It must be the centerline of a physical feature such as a hole or boss, etc. In these cases, it is the diameter of the hole or the width of the boss that is designated as the datum. The point of reference is the centerline of these physical features.

DC: See "diagnostic clock".

dc controller: A circuit that produces, from a dc input, a dc output that is proportional to a control input. JESD14, 11/86#

dc noise margin: The maximum dc voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst–case input level without causing the output voltage to deviate from the allowable logic voltage level. RS-390-A, 2/81

dc power dissipation (P_D): The total dc power supplied to a device less any power delivered from the device to a load. JESD99C, 12/12

dc terminal: A terminal that is to be connected to a dc circuit. JESD14, 11/86

dc test: A test during which only steady-state voltages and currents are applied to the device. JESD99C, 12/12

NOTE DC tests are generally used to determine input levels, output levels, or dissipation characteristics of devices.

dc trigger point (on the gate characteristic of a thyristor): The point on the gate characteristic $V_{FG} = f(I_{FG})$ at which, for continuously rising gate current or gate voltage, the thyristor switches from the off state to the on state. JESD77D, 8/12

dead-bug (orientation): The orientation of the package with the terminals facing up. J-STD-020D.1, 3/08

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Terms, abbreviations, letter symbols, and definitions **References**

decade: The interval between two frequencies that have a ratio of 10 to 1. JESD22-B103B, 6/02#

NOTE The number of decades, D, between two frequencies, f1 and f2, is given by D = |log (f2/f1)|.

decoder: A matrix of logic elements that selects one or more output channels according to the combination of input signals present. (Ref. ANSI/IEEE Std 100.) JESD99C, 12/12

defect density: The number of defects on a chip divided by its area. JEP148A, 12/08

defect, (physical): A physical anomaly that adversely affects function or performance. JEP143C, 7/12
JEP148A, 12/08

degradation defect: A physical defect created by the natural changes in the properties of materials over time that is manifested after some period of operation. JEP143C, 7/12

delamination: (1) The detachment of a sheet-like layer of material from a surface. JESD9B, 5/11

(2) A failure found during tensile pull of flip chip solder joints wherein the solder bump interconnection metallization is at least partially removed from either the substrate or the die, with the solder bump remaining continuous. JESD22-B109A, 1/09

(3) An interfacial separation between two materials that were intended to be bonded. J-STD-020D.1, 3/08

delay time (1) **(general) (t_d):** The time interval between a reference point on one waveform and a reference point on another waveform. JESD77D, 8/12
JESD99C, 12/12
JESD100-B, 12/9

(2) **(between input and output):** The time interval between a transition at an input and a resultant change at an output. JESD77D, 8/12

(3) **(of an integrated circuit) (t_d, t_{dr},** and **t_{df}):** The time interval between a step-function change of the input signal level and the instant at which the magnitude of the output signal passes through a specified value (normally 10% for t_{dr} or 90% for t_{df}) close to its initial value. (Ref. IEC 748-3.) JESD99C, 12/12

(4) **(of a transistor) (t_d):** (A) The time interval from the point at which the leading edge of the input pulse has reached 10% of its maximum amplitude to the point at which the leading edge of the output pulse has reached 10% of its maximum amplitude. JESD10, 1/76

(B) Synonym for "current delay time, t_{di}". JESD77D, 8/12

delay time, (digital) (of a linear or **a multiplying digital-to-analog converter) (t_d** or **t_{dd}):** The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches. JESD99C, 12/12

NOTE For a multiplying digital-to-analog converter, the full term and the additional subscript *d* must be used to distinguish between the digital and the reference delay times.

delay time, reference (of a multiplying digital-to-analog converter) (t_{dr}): The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value. JESD99C, 12/12

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Terms, abbreviations, letter symbols, and definitions	References
delivery and lead time rating: An assessment of the metrics established to evaluate delivery of product.	JEP146A, 1/09
depletion layer, collector(-base): Synonym for "space-charge region, collector(-base)".	JESD77D, 8/12
depletion layer, emitter(-base): Synonym for "space-charge region, emitter(-base)".	JESD77D, 8/12
depletion-mode operation: The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value decreases the magnitude of the drain current. (Ref. IEC 747-8.)	JESD24, 7/85 JESD77D, 8/12
depletion-type field-effect transistor: A field-effect transistor having appreciable channel conductance for zero gate-source voltage; the channel conductance may be increased or decreased according to the polarity of the applied gate-source voltage. (Ref. IEC 747-8.)	JESD24, 7/85 JESD77D, 8/12
deposition: The process of applying a material to a substrate by means of vacuum, electrical, chemical, screening, or vapor methods.	JESD99C, 12/12
deposition, vapor-phase: The deposition of conductive, resistive, insulating, or semiconductor films onto a substrate from a source material in the vapor phase by physical deposition or chemical reaction.	JESD99C, 12/12
derating (thermal) (relating to reliability): The practice of using an electronic device in a narrower environmental and/or operating envelope than its manufacturer-designated limits.	JEP149, 11/04
desiccant: An absorbent material used to maintain a low relative humidity.	J-STD-033C, 2/12
design FMEA (DFMEA): A systematic method to assess the risks of the elements of a product or process of record (POR) and their interactions in terms of functionality as defined by product or POR specification.	JEP131B, 4/12
design module: A software description of a functional block describing the function and performance.	JESD12-1B, 8/93 JESD99C, 12/12
design of experiments (DOE): (1) An efficient method of experimentation that identifies factors that affect the mean and variation with minimum testing.	JEP131B, 4/12
(2) A systematic approach to varying the input-controllable variables in the process and analyzing the effects of these process variables on the outputs. When employed in conjunction with statistical process controls, it can minimize process variability.	JEP132, 7/98
design rules: The basic rules and regulations for circuit design with electrical and geometrical parameters specified for the range of application conditions and time.	JEP148A, 12/08
detectable fault: A functional fault for which a test pattern can be created that will always cause the effects of the fault to be observable at an externally accessible node.	JESD12-5, 8/88
detected fault: A functional fault that causes effects that are observed at an externally accessible node when the circuit is exercised by the existing test pattern.	JESD12-5, 8/88

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

detector diode: A diode, often associated with microwave circuits, that converts rf energy into dc or video output. — JESD77D, 8/12

deviation from coplanarity: The distance between the intended contact point of a terminal and the established seating plane or regression plane. — JESD22-B108B, 9/10

NOTE Contrast with "deviation from planarity".

deviation from planarity: The difference in height between the highest point and the lowest point on the package substrate bottom surface measured with respect to the reference plane. — JESD22-B112A, 10/09

NOTE Contrast with "deviation from coplanarity".

device: A piece of equipment, a mechanism, or another entity designed to serve a special purpose or perform a special function. — JESD77D, 8/12; JESD99C, 12/12

NOTE 1 In JEDEC documents, the word "device" is often used as an abbreviated reference to the type or types of solid-state devices that are within the scope of those documents. Context could indicate otherwise; e.g., in the phrase "the device used to hold the device under test", the first usage of the word "device" refers to a mechanism; the second to a solid-state device.

NOTE 2 The classification of an item as a device or as a component depends upon the intention of the owner at the time of classification.

device-level description: A structural description using circuit elements as primitives. — JESD12-1B, 8/93; JESD99C, 12/12

dewetting: A condition that results when molten solder coats a surface and then recedes to leave irregularly shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed. (Ref. IPC-T-50.) — J-STD-002B, 2/03

DFMEA: See "design FMEA".

diac: An alternative term for "thyristor, bidirectional diode". — JESD77D, 8/12

NOTE Most devices designated as "diac" have been three-layer devices (npn or pnp), but others have had five layers. Some early versions were unidirectional, and a 1975 IEEE definition included them as well as bidirectional types.

diagnostic clock (DC): The input that, on some devices, invokes and controls any built-in diagnostic test features. — JESD21-C, 1/97

dice; dies: Alternative plurals of "die". — JEP158, 11/09; JESD22-B118, 3/11; JESD77D, 8/12; JESD99C, 12/12

diced wafer: A wafer that has been separated into individual dice. — JESD22-B118, 3/11

die: (1) A separated part of a wafer (or, in some cases, a whole wafer) intended to perform a function or functions in a device. — JESD22-B118, 3/11

(2) Synonym for "chip (1)".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
die (attach) area: An area of a package used for die placement and typically located on the bottom inside surface of the base of the package. NOTE For ceramic package cavities, the die attach area is defined as the area that is within a 0.508-mm (0.020-inch) perimeter from the die attach cavity wall.	JESD9B, 5/11
die attach(ment): See "die bond".	
die-attach pad: A central metalplate, often used in a semiconductor package to support the active device.	JEP123, 10/95
die attach view area: The interface between the die and the die attach adhesive and/or the die attach adhesive and the die attach substrate. (Refer to Type II in Annex A of J-STD-035.)	J-STD-035, 5/99
die backside: The side of a die that does not contain fabricated semiconductor circuits or circuit elements.	JESD22-B118, 3/11
die bond; die attach(ment); chip attach(ment): The process or method of physically mounting a die [chip] on a surface, substrate, header, etc.	JESD51-1, 12/95 JESD51-13, 6/09
die-bond material: Material used to attach the die to the rest of the package. NOTE The most common material is epoxy, but solder is often used for high-power devices.	JESD51-13, 6/09
die fracture: A failure found in tensile pull of flip chip solder joints wherein the body of the die is fractured and damaged before all the solder bumps are separated from it.	JESD22-B109A, 1/09
die lot: A quantity of dice that are processed together as a batch under a given set of conditions.	JESD22-B118, 3/11
die-pad fracture: A fracture in the far-back-end-of-line (FBEOL) die structure.	JESD22-B109A, 1/09
die-size package: A chip-scale package whose area is generally equal to the area of the semiconductor device it contains. NOTE 1 Usually, but not necessarily, some portion of the silicon IC is exposed. The device is then also an uncased device. NOTE 2 The package size will change with changes in the size of the die.	JESD30E, 8/08
die surface view area: The interface between the encapsulant and the active side of the die. (Refer to Type 1 in Annex A of J-STD-035.)	J-STD-035, 5/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

differential flux: The particle flux density per unit energy incident on a surface; i.e., the number of radiant-energy particles incident on a surface during a given period of time divided by the product of the area of that surface, the characteristic energy of the incident particles, and the given period of time. JESD89A, 10/06

NOTE 1 The term "differential flux" is used in JESD89A whereas other standards use the term "differential flux density" for the same meaning.

NOTE 2 The equation "differential flux density = $N/(A \cdot E \cdot t)$" applies, where N, A, E, and t represent the quantities number of particles, area, energy, and time.

NOTE 3 The unit symbol (e.g., $cm^{-2} \cdot MeV^{-1} \cdot s^{-1}$) does not identify particle type. The particle name may be placed before the term, e.g., "proton differential flux", or in the spelled-out unit name, e.g., "protons per square centimeter megaelectronvolt second".

NOTE 4 The use of the terms "spectral flux" and "spectral flux density" for this concept is deprecated because "spectral" usually applies only to a specific wavelength, wavelength band, or function of wavelength.

differential inputs: A pair of ungrounded input terminals between which a signal is applied. JESD99C, 12/12

differential input voltage (V_{ID}): The voltage applied between two input terminals of a circuit. JESD99C, 12/12

differential line receiver: A line receiver that has a differential input. JESD99C, 12/12

differential outputs: A pair of ungrounded output terminals between which the output signal appears. JESD99C, 12/12

differential output voltage (V_{OD}): The voltage between two output terminals of a circuit. JESD99C, 12/12

differential video amplifier: A video amplifier with differential input and differential output terminals. JESD99C, 12/12

diffusion, impurity: A process used to introduce desired impurities into a semiconductor crystal to alter its electrical properties; it is accomplished by introducing suitable dopants to the surface of the semiconductor wafer under precisely controlled conditions, usually at high temperatures. JESD99C, 12/12

diffusion (of charge carriers): The movement of charge carriers caused only by a charge carrier concentration gradient. JESD77D, 8/12

NOTE In the case of transfer across a p-n junction, the amount of transfer depends on the internal electric field resulting from the built-in electric field and applied bias.

digital image correlation: A 3-D imaging technique utilizing multiple triangulated cameras and computerized image matching.. JESD22-B112A, 10/09

digital-to-analog [D/A] converter (DAC): A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values. JESD99C, 12/12

NOTE Examples of input code formats are straight binary, 2s complement, and binary-coded decimal.

DIMM: See "dual-in-line memory module".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

dimple: A visual anomaly that is a shallow dip. JESD22-B118, 3/11

ding: A visual anomaly that is an indentation made by mechanical impact. JESD22-B118, 3/11

diode, barrier: Synonym for "diode, Schottky". JESD99C, 12/12

diode, hot-electron: Synonym for "diode, Schottky". JESD99C, 12/12

diode, Schottky: A diode formed by depositing a metal film on a semiconductor surface of sufficiently high resistivity to form an energy barrier. JESD99C, 12/12

NOTE A Schottky diode is sometimes used as part of a bipolar transistor structure.

diode, semiconductor: In its simplest form, any p-n junction but, in microcircuits, often a modified bipolar transistor. JESD99C, 12/12

NOTE Modifications include shorting the base to the collector, shorting the emitter to the collector, using the emitter-base diode with the collector open, or using the collector-base diode with the emitter open.

DIP: See "dual-in-line package".

disable time (general): The time interval between the transition of the disabling signal and the cessation of the affected operation. JESD100-B, 12/99

disable time, chip-enable to data-retention: The time interval between the transition of the disabling signal and the instant when the data-retention mode is entered. JESD100B.01, 12/02

NOTE This interval is defined with respect to specified reference points on the chip-enable and supply-voltage waveforms.

disable time, chip-enable to power-down: The time interval between the transition of the disabling signal and the instant when the supply current has decreased from its active value to its maximum standby value. JESD100B.01, 12/02

NOTE This interval is defined with respect to specified reference points on the chip-enable and supply-current waveforms.

disable time from the high level (of a three-state or **H-type open-circuit output) (t_{PHZ}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined high level to a high-impedance (off) state. JESD99C, 12/12

NOTE 1 Open-collector, open-emitter, open-drain, and open-source outputs are collectively referred to as open-circuit outputs. For the purposes of these definitions, the subclassification H-type is used for pnp open-collector, npn open-emitter, p-channel open-drain, and n-channel open-source outputs because, without the aid of external components, the only on-state level they can produce is the high level. The subclassification L-type is used for npn open-collector, pnp open-emitter, n-channel open-drain, and p-channel open-source outputs for analogous reasons.

NOTE 2 Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "high-to-low-level propagation time" and the symbol t_{PHL} are frequently used with these outputs for this parameter.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

disable time from the low level (of a three-state or **L-type open-circuit output) (t_{PLZ}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined low level to a high-impedance (off) state. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "low-to-high-level propagation time" and the symbol t_{PLH} are frequently used with these outputs for this parameter.

disable time, output (of a three-state, open-collector, open-emitter, open-drain, or **open-source output):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state. JESD99C, 12/12
JESD100-B, 12/99

disable transition time from the high level (of a three-state or **H-type open-circuit output) (t_{THZ}):** The transition time between specified reference points on the output voltage waveform with the output changing from the defined high level to a high-impedance (off) state. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "high-to-low-level transition time" and the symbol t_{THL} are frequently used with these outputs for this parameter.

disable transition time from the low level (of a three-state or **L-type open-circuit output) (t_{TLZ}):** The transition time between specified reference points on the output voltage waveform with the output changing from the defined low level to a high-impedance (off) state. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "low-to-high-level transition time" and the symbol t_{TLH} are frequently used with these outputs for this parameter.

discoloration (of a package): Change in color caused by residue from processing or by chemical attack or heat. JESD27, 8/93#
Rescinded 5/11

disconnect (state): A state in a switch device characterized by a high series impedance of the designated electrical path. JESD73, 6/99
JESD73-1, 8/01
JESD73-2, 8/01
JESD73-3, 8/01
JESD73-4, 11/01

discrepancy: Synonym for "nonconformance" and "nonconformity (2)".

discrepant material: Material that does not conform to specifications. EIA-557-B, 2/06

NOTE See also "nonconforming unit".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

discrete (semiconductor) device: A semiconductor device that is specified to perform an elementary electronic function and is not divisible into separate components functional in themselves. JESD77D, 8/12 JESD99C, 12/12

NOTE 1 Diodes, transistors, rectifiers, thyristors, and multiple versions of these devices are examples. Other semiconductor structures having the physical complexity of integrated circuits but performing elementary electronic functions (e.g., complex Darlington transistors) are usually considered to be discrete semiconductor devices.

NOTE 2 If a semiconductor device is not considered to be an integrated circuit in both complexity and functionality, it is considered to be a discrete device.

discretionary wiring: A technique for interconnecting subarrays on a single wafer in which each subarray is electrically tested by probing and the desired array function is attained by the use of a metallization pattern that connects only usable subarrays. JESD99C, 12/12

discrimination: The ability of the measuring equipment to differentiate between characteristic values. The equipment discrimination should be small (e.g., less than 10%) compared to the process variability and/or control limits. JEP132, 7/98

disk-button package: A package shaped like a disk or button whose terminals exit radially from the periphery of the disk (like spokes of a wheel) or axially from the center of the disk. JESD30E, 8/08

dislocation: An atomic imperfection or fault in the crystalline lattice structure. JESD99C, 12/12

NOTE 1 The two types are edge dislocations (if a row of atoms is removed or displaced and the slippage is at right angles to the displacement) and screw dislocations (if the slippage is parallel).

NOTE 2 If dislocations appear at the surface of the crystal, they are sometimes referred to as surface dislocations.

displacement damage: Damage induced by the displacement of atoms in a crystalline lattice, typically silicon, caused by the interaction of the incident neutrons, protons, or other energetic particles or ions with the crystalline lattice atoms. JEP133C, 1/10#

disposition: The act of determining the future course of action for nonconforming material, e.g., scrap, use-as-is, retest, rework, and other. JESD671B, 6/12

dissolution of termination metallization; leaching: The loss or removal of metallization from an area on the basis or substrate material during immersion in molten solder. J-STD-002B, 2/03

distance to neutral point (DNP): The physical distance from the stress-neutral point to the point of interest on the die. JEP158, 11/09

distributed delay model: A model constructed from primitive models, each having specified delay. JESD12-1B, 8/93 JESD99C, 12/12

DMA: See “dynamic mechanical analysis”.

DNP: See “distance to neutral point”.

D(n)(x): See “data input”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

DOE: See “design of experiments”.

dopant: A chemical element that is introduced into the lattice structure as an impurity to form desired properties. JESD99C, 12/12

NOTE Examples are phosphorus and boron used to create n- and p-regions, respectively, in silicon.

dose rate burnout: The catastrophic failure of a circuit caused by the very large currents produced by a high-intensity pulse of ionizing radiation. JEP133C, 1/10

dose rate upset: The disruption of a device caused by a high-intensity pulse of ionizing radiation that produces a change in stored data, a change of operating state, or a transient output signal that is large enough to affect other circuit elements. JEP133C, 1/10

double-buffered read transfer (DRT): A read transfer in an array that contains two full SAM data registers that are used alternately. Each one is loaded while the contents of the other is being transferred to the SDQ(n) port. The selection of the two SAM registers is automatic. JESD21-C, 1/97

double-diffused MOS (DMOS) technology: A technology for producing silicon-gate metal-oxide semiconductor field-effect transistors such that 1) the threshold voltage, V_T, is determined by the intersection of two doping profiles, and 2) the device channel length is defined by the diffusion characteristics rather than by a photolithographic self-aligned gate structure. JESD99C, 12/12

double-sided PCB assembly: A printed circuit board assembly with components mounted on both sides of the board. JESD22-B111, 7/03

double-way rectifier circuit: A circuit in which the current flows in both directions from each terminal of the alternating-voltage circuit to the rectifier circuit elements connected to each terminal. JESD77D, 8/12
JESD282-B, 4/00

NOTE The terms “single-way” and “double-way” provide a means for describing the effect of the rectifier circuit on current in the transformer windings connected to the rectifier circuits. Most rectifier circuits may be classified into these two general types. Many double-way circuits are also referred to as bridge circuits.

double word: A character string or binary element string that, in a given system, has twice the length of a word. JESD100-B, 12/99

downbond area: An area for a wire bond on the die paddle, whose dimensions equal those of a single bond pad on the die. J-STD-020D.1, 3/08

DPM: See “dual-port memory”.

DPSRAM: See “dual-port static RAM”.

DQM: See “input/output data mask”.

DQ(n)(x): See “data input/output”.

drain (D; d): A region into which majority carriers flow from the channel. JESD24, 7/85

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

drain current, dc (I_D): The direct current into the drain terminal. JESD24, 7/85 JESD28-A, 12/01 JESD60A, 9/04 JESD90, 11/04

drain cutoff current ($I_{D(off)}$): The direct current into the drain terminal of a depletion-type transistor with a specified reverse gate-source voltage applied to bias the device to the off-state. JESD24, 7/85

drain-gate voltage, dc (V_{DG}): The dc voltage between the drain terminal and the gate terminal. JESD24, 7/85

drain leakage current ($I_{D(leak)}$): The drain current when the transistor is biased in its off state. JESD60A, 9/04 JESD90, 11/04

NOTE $I_{D(leak)}$ may have contributions from channel off-state current, gate-induced drain leakage, and drain-to-gate tunneling currents.

drain power voltage (VDD): The primary power voltage on MOS devices that require a potential that differs from the normal system logic voltage. The term VDD is used interchangeably with VCC on devices that use 5-V supplies. JESD21-C, 1/97

drain region: A collection region that acquires principal-current charge carriers from a channel, the current being due to a voltage applied to the drain. JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

drain-source capacitance (C_{ds}): The capacitance between the drain and source terminals with the gate terminal connected to the guard terminal of a three-terminal bridge. JESD24, 7/85

drain-source voltage, dc (V_{DS}): The dc voltage between the drain terminal and the source terminal. JESD24, 7/85 JESD28-A, 12/01 JESD60A, 9/04 JESD90, 11/04

drain supply voltage, dc (V_{DD}): The dc supply voltage applied to a circuit connected to the drain terminal. JESD24, 7/85

drain terminal (D, d): The specified externally available point of connection to the drain region. JESD77D, 8/12

DRAM: See “dynamic (random-access) memory”.

drift: The maximum absolute change in a parameter over a period of time. JESD99C, 12/12

NOTE The change may or may not be normalized to the initial value of the parameter. The specific term should be “(parameter) drift”.

driver: An amplifier or gate with increased ability to drive a load. JESD99C, 12/12

DRT: See “double-buffered read transfer”.

DSF: See “special-function enable input”.

DT/OE(n): See “data-transfer/output-enable input”.

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Terms, abbreviations, letter symbols, and definitions	References
dual-gate field-effect transistor: Synonym for "tetrode field-effect transistor".	JESD24, 7/85 JESD77D, 8/12
dual-in-line package (DIP): A device package configuration that has two parallel rows of pins that are spaced nominally 0.3 inch, 0.4 inch, or 0.6 inch apart with the pins on 0.1-inch centers. NOTE See also "in-line package".	JESD21-C, 1/97
dual-in-line memory module (DIMM): A packaging arrangement of memory devices on a socketable substrate.	JESD206, 1/07
dual-port memory (DPM): Any memory that has two essentially identical data ports.	JESD21-C, 1/97
dual-port static RAM (DPSRAM): A static RAM that contains two sets of identical random-access address and data ports.	JESD21-C, 1/97
duplex transmission: Data transmission in both directions simultaneously. (Ref. ANSI X3.172.)	JESD100-B, 12/99
DUT: Device under test.	JESD24-8, 8/92 JESD51-1, 12/95 JESD51-13, 6/09 JESD57, 12/96 JESD78D, 11/11 JESD89A, 10/06 JESD89-3A, 11/07
duty cycle jitter ($t_{jit(duty)}$): The magnitude of the deviation in time duration between the primary threshold crossing and the secondary threshold crossing in a cycle over a random sample of cycles.	JESD65B, 9/03
duty cycle, power: The ratio of the power-on time duration per cycle to the total cycle time. NOTE Power duty cycle is usually expressed as a percentage.	JESD22-A105C, 1/04
DV: See "design validation/verification".	
dynamic device: A device requiring clocking in order to guarantee a stable state while being tested.	JESD78D, 11/11
dynamic mechanical analysis (DMA): A technique used to characterize materials by applying a sinusoidal stress to measure the strain, allowing the complex modulus and viscoelastic behavior to be determined. NOTE 1 "Dynamic mechanical analysis" is also known as "dynamic mechanical spectroscopy". NOTE 2 The temperature of the sample or the frequency of the stress are often varied, leading to variations in the complex modulus; this approach can be used to locate the glass transition temperature of the material, as well as to identify transitions corresponding to other molecular motions.	JESD22-B113A, 9/12
dynamic phase offset ($t_{(\phi)dyn}$): The incremental phase offset between the input reference clock and the feedback input signal of a phase-locked loop (PLL) resulting from modulation of the input reference clock.	JESD65B, 9/03

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

dynamic random-access memory (DRAM): A dynamic memory that permits access to any of its address locations in any desired sequence with similar access time to each location. JESD21-C, 1/97 JESD100B.01, 12/02

dynamic range (of a charge-transfer device): The range of useful linear operation expressed as the ratio of the saturation input signal to the noise equivalent signal. JESD99C, 12/12

dynamic (read/write) memory: A volatile read/write memory in which the cells require the repetitive application of control signals generated inside or outside the integrated circuit to retain stored data. (Adapted from IEC 748-2.) JESD100-B, 12/99

NOTE 1 The words "read/write" may be omitted from the term when no misunderstanding is likely.

NOTE 2 Each repetitive application of the control signals is normally called a refresh operation or cycle.

NOTE 3 A dynamic memory can use static addressing or sensing circuits.

NOTE 4 Contrast with "static (read/write) memory".

E

E: See "chip enable".

E; e: See "emitter terminal".

early life: The period of initial use by the customer. JEP143C, 7/12 JESD74A, 2/07#

NOTE This period typically ranges from three months to one year of operation.

early-life-failure rate (ELFR): The failure rate that may occur during the period of initial use by the customer. JEP143C, 7/12 JESD74A, 2/07#

early-life-failure (ELF) test: An accelerated test designed to measure the early-life-failure rate (ELFR). JEP143C, 7/12 JESD74A, 2/07#

NOTE The calculation procedure is specified in JESD74, sample sizes are noted in JESD47, and stress methods are identified in JESD22-A108 and other documents in the JESD22 series.

early-life period (t_{ELF}): The specified early-life period as defined by the user or the supplier. JEP143C, 7/12 JESD74A, 2/07

ECC: See "error correction code (ECC)".

EDAC: See "error correction code (ECC)**;** error detection and correction (EDAC)".

EEPROM: See "electrically erasable programmable read-only memory".

EEPROM redundancy: See "redundancy (in a memory)".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

effective average input noise temperature (T_e): The noise temperature in kelvins which, assigned to the input impedance termination(s) at all frequencies of a noise-free equivalent of the transistor, would yield the same total noise power in an output termination as that of an actual transistor connected to noise-free equivalents of the input termination(s). JESD311A, 11/81

effective LET (for particle radiation) [LET(θ)]: The linear energy transfer (LET) modified to account for the change in total energy transferred from an incident ion as it traverses a sensitive volume when the path of the ion is not normal to the irradiated surface of that volume. JESD57, 12/96#

NOTE 1 The cosine dependence may be applicable for this modification. Caution must be used; see annex B of JESD57.

$$\mathrm{LET}(\theta) = \mathrm{LET}(0°) / \cos\theta$$

where θ is the angle of incidence of the ion (i.e., the angle between the ion path and the normal at the point of incidence).

NOTE 2 Many modern devices do not follow the above equation, so the experimenter may have to determine the LET(θ) from the topology of a particular device.

NOTE 3 The equation in note 1 is valid only when the depth of the sensitive volume is less than the other two dimensions in the rectangular parallelepiped (RPP) model.

efficiency (of a process): The measure of the ability of a process to produce a desired output (through a common method), as a percentage of the required input (e.g., time, materials, etc.). JEP132, 7/98

electrical characterization: The description of behavior of the electrical parameters of a device based on statistical analysis of experimental data and under predefined operating conditions. JESD86A, 10/09

NOTE This includes the distribution of an electrical parameter as a function of other parameter(s) variation.

electrical connection (within a semiconductor device): An electrically conducting element that is intended to function as a pathway between other elements, including terminals, and whose primary purpose is to conduct electric current in a confined manner. JESD77D, 8/12

NOTE The connection may consist of a separate conductive entity such as a wire or metallic film or be an integral part of the body.

electrical device: A device whose operation depends on the conduction of electrons in a conductor. JS709A, 5/12

NOTE Examples of electrical devices include wires, resistors, capacitors, inductors, relays, sockets, and connectors.

electrical distribution: A distribution of an electrical parameter measured on a random sample of devices from a population. JESD86A, 10/09

electrical length of signal path: The time interval required for an electrical signal to traverse the conductor from end to end. JEP123, 10/95

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
electrically erasable programmable read-only memory (EEPROM): A reprogrammable read-only memory in which the cells at each address can be erased electrically and reprogrammed electrically.	JESD21-C, 1/97 JESD22-A117B, 3/09 JESD100-B, 12/99
electrical model parameter: An electrical characteristic value, such as inductance or capacitance, that, when used in a simulation process, will produce signal transfer characteristics reproducing those measured.	JEP123, 10/95
electrical parameter drift: The absolute change in an electrical parameter over a period of time.	JESD86A, 10/09
NOTE 1 The change may be measured as a shift from the original value of a single device or as a shift in the statistical distribution for a group of devices. When changes are to be studied on an individual device basis, the study is called "parametric drift of individuals" and serialization of individual units is required. When changes are studied on a group of devices, the study is referred to as "parametric drift of distributions" and serialization of individual units is not required. The cause of the change may be use and/or environmental conditions in the field application or as simulated by accelerated stress testing.	
NOTE 2 Multiple structures can be constructed within a single device; in this type of design, each structure (array or chain) can be characterized independently and measured against a predetermined design specification.	
electrical test failure after stressing: Synonym for "post-stress electrical failure".	
electrode (of a semiconductor device): (1) An electrical and mechanical contact to a region of a semiconductor device.	JESD10, 1/76
(2) An element that performs one or more functions of emitting or collecting electrons or holes, or of controlling their movements by an electric field.	JESD77D, 8/12 JESD99C, 12/12 JESD282-B, 4/00
electronic device: A device whose operation depends on the conduction of electrons in a vacuum, gas, or semiconductor.	JS709A, 5/12
NOTE Examples of electronic devices include transistors, integrated circuits, hybrids, and modules.	
electronic product: An item containing one or more electronic devices performing major functions.	JS709A, 5/12
NOTE An electronic product will also contain electrical devices.	
electrostatic charge: Electric charge at rest.	JESD625B, 1/12
electrostatic discharge (ESD): A sudden transfer of electrostatic charge between bodies or surfaces at different electrostatic potentials.	JEP143C, 7/12 JESD22-C101E, 12/09 JESD625B, 1/12
NOTE The definition in JESD625B omits the word "sudden:.	

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
electrostatic-discharge-sensitive device: A discrete device or integrated circuit that may be permanently damaged by electrostatic potentials encountered in routine handling, testing, and shipping.	JESD77D, 8/12 JESD99C, 12/12
NOTE In some earlier documents of the IEC and CENELEC, the abbreviation ESDS stood for "electrostatic-discharge-sensitive device"; in the USA, ESDS stands merely for "electrostatic discharge sensitive" or "electrostatic discharge sensitivity", and "ESDS device" is not further abbreviated. The abbreviation ESD stands for "electrostatic discharge".	
electrostatic-discharge shielding: A barrier or enclosure that limits the passage of an electrostatic discharge current to the stored or contained devices.	JESD625B, 1/12
electrostatic field: The lines of force surrounding an electrically charged object.	JESD625B, 1/12
element (of a discrete device): Any constituent part of the discrete device that contributes directly to its operation and performs a definable function.	JESD77D, 8/12
NOTE The definition includes electrical interconnections between elements or between elements and terminals.	
element, (circuit): See "circuit element".	
element, distributed circuit: The physical realization of an element incorporating more than one primary electrical characteristic (resistance, capacitance, inductance, gain, etc.) dispersed along the length of the element.	JESD99C, 12/12
ELFR: See "early-life-failure rate".	
elimination of nonvalued activities: The deletion or elimination of costed steps, within a prescribed process, that do not measurably contribute to the ability of that process to produce the defined output.	JEP132, 7/98
embedded gate array: A gate array masterslice in which some of the array circuit elements are replaced by one or more cell-based functions.	JESD12-1B, 8/93 JESD99C, 12/12
embedding: A process using polymers or similar materials that can be hardened to produce a body enclosing, and in contact with, the electronic assembly, for example, casting, potting, dip-coating, and transfer molding.	JESD99C, 12/12
emissivity: The ratio of the radiant energy emitted by a surface to that emitted by a blackbody at the same temperature.	JEP138, 9/99# JEP140, 6/02 JESD51-1, 12/95 JESD51-13, 6/09
emitter-base voltage, collector open (V_{EBO}): The dc voltage between the emitter terminal and the base terminal with the collector terminal open-circuited.	JESD10, 1/76
emitter cutoff current, collector open (I_{EBO}): The dc current into the emitter terminal when it is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE Std 255.)	JESD10, 1/76

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

emitter follower: An output circuit whose output load is connected in the emitter circuit of a transistor and whose input is applied between the base and the remote end of the emitter load, which may be at ground potential. JESD99C, 12/12

NOTE The term "emitter follower", as applied to linear circuits, usually refers to passive-pulldown or passive-pullup (bipolar) outputs; as applied to emitter-coupled logic (ECL) circuits, to open-emitter (unipolar) outputs.

emitter (nonspecific): The overall combination of emitter transition region, emitter region, emitter terminal, and the interface between them. JESD77D, 8/12

NOTE This term should be used in this manner only when no confusion is likely to occur.

emitter power voltage (VEE): For ECL interface devices, the primary and most negative power supply terminal. JESD21-C, 1/97

emitter region (of a unijunction transistor): A region of a semiconductor device from which charge carriers that are minority carriers in a base region are injected into a base region. JESD77D, 8/12

emitter region, functional: A supply region that delivers principal-current charge carriers into a controlling base region through an associated emitting junction. JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal. In the normal operating mode, this functional region is located in the emitter region; in the inverse operating mode, it is located in the collector region.

emitter region, physical: (1) A region from which charge carriers that will become minority carriers in the base are injected into the base. (Ref. 60 IRE 28.S1.) JESD10, 1/76

(2) The physical region that is designed by the manufacturer to contain the supply region in the normal operating mode and, in a simple discrete transistor, is externally accessible by the designated emitter terminal. JESD77D, 8/12

emitter terminal (E, e): The specified externally available point of connection to the emitter region. JESD77D, 8/12

emitting junction: A semiconductor junction in an operating condition in which the net flow of charge carriers of each type across the junction is in the direction from the region where they are majority carriers to the region where they are minority carriers, i.e., in the direction opposite to the force resulting from the internal electric field. JESD77D, 8/12

empty zero; real zero (in a charge-transfer device): A condition in which there is no bias charge or low-level charge. JESD99C, 12/12

enable time (general): The time interval between the transition of the enabling signal and the commencement of the intended operation. JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

enable time, chip-enable to power-up: The time interval between the transition of the enabling signal and the instant when the supply current has increased from its standby value to its active value. JESD100B.01, 12/02

NOTE This interval is defined with respect to specified reference points on the chip-enable and supply-current waveforms.

enable time, output (of a three-state, open-collector, open-emitter, open-drain, or **open-source output) (t_{en}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low). JESD99C, 12/12
JESD100-B, 12/99

enable time to the high level (of a three-state or **H-type open-circuit output) (t_{PZH}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined high level. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "low-to-high-level propagation time" and the symbol t_{PLH} are frequently used with these outputs for this parameter.

enable time to the low level (of a three-state or **L-type open-circuit output) (t_{PZL}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined low level. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "high-to-low-level propagation time" and the symbol t_{PHL} are frequently used with these outputs for this parameter.

enable transition time to the high level (of a three-state or **H-type open-circuit output) (t_{TZH}):** The transition time between specified reference points on the output voltage waveform with the output changing from a high-impedance (off) state to the defined high level. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "low-to-high-level transition time" and the symbol t_{TLH} are frequently used with these outputs for this parameter.

enable transition time to the low level (of a three-state or **L-type open-circuit output) (t_{TZL}):** The transition time between specified reference points on the output voltage waveform with the output changing from a high-impedance (off) state to the defined low level. JESD99C, 12/12

NOTE 1 See note 1 to "disable time from the high level …".

NOTE 2 Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "high-to-low-level transition time" and the symbol t_{THL} are frequently used with these outputs for this parameter.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

encoder: A network or system in which only one input is excited at a time and each input produces a unique combination of output signals. (Ref. ANSI/IEEE Std 100.) JESD99C, 12/12

end-product parameter: A parameter that characterizes the product (e.g., piece parts, subassemblies, and/or assemblies) at the finished product stage. EIA-599-A, 6/98

endurance (of a reprogrammable read-only memory or solid-state drive): The ability to withstand data rewrites and still comply with applicable specifications. JESD22-A117B, 3/09 JESD100-B, 12/99 JESD218A, 2/11

endurance failure: A failure that arises during endurance cycling. JESD22-A117B, 3/09 JESD218A, 2/11

NOTE 1 Endurance failures may be data errors or functional errors.

NOTE 2 In an endurance cycling, some failures may occur that are unrelated to endurance. For example, a solder joint could fail. A failure is considered unrelated to endurance if it was not caused by the endurance cycling itself (i.e., if it was not caused by the repetitive writing of data to the device). Such nonendurance failures are not considered as part of endurance verification.

NOTE 3 A number of distinct failure mechanisms are responsible for endurance failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters. For example, in floating-gate memories, failure may be caused by charge trapping (normally accelerated by lower temperatures) in the charge transfer dielectric or by oxide rupturing (normally accelerated by higher temperatures) in the transfer dielectric or in peripheral dielectrics. For these reasons, endurance may depend on temperature, but it is not known a priori whether high temperature is worse than low temperature or vice-versa.

endurance rating; terabytes written (TBW) rating: The number of terabytes that may be written to a solid-state drive such that the SSD meets the specified requirements. JESD218A, 2/11

NOTE Several factors impact the endurance rating including how optimally the wear leveling has been implemented, write amplification factor, and the cycling capability of the NAND components. The relationship between TBW rating, write amplification factor, and the wear-leveling efficiency are highly dependent on the workload applied for the characterization of endurance.

enhanced low-dose-rate sensitivity (ELDRS): For a fixed response, any device characteristic that reflects an increased radiation sensitivity at very low dose rates (i.e., generally at or below 10 $mrd(Si)\cdot s^{-1}$) than at higher dose rates (i.e., 50-300 $rd(Si)\cdot s^{-1}$). JEP133C, 1/10

NOTE The increased radiation sensitivity may be a result of true dose-rate effects and/or time-dependent effects.

enhancement-mode operation: The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value increases the magnitude of the drain current. (Ref. IEC 747-8.) JESD24, 7/85 JESD77D, 8/12

enhancement-type field-effect transistor: A field-effect transistor having substantially zero channel conductance for zero gate-source voltage; the channel conductance may be increased by the application of a gate-source voltage of appropriate polarity. (Ref. IEC 747-8.) JESD77D, 8/12

environmental relative humidity: The relative humidity in the area immediately surrounding a specified component in an application. JESD94A, 7/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
environmental temperature cycle: A temperature cycle in an application resulting from environmental temperature changes.	JESD94A, 7/08
environmental temperature range: The temperature range found in the area or enclosure surrounding an application.	JESD94A, 7/08
epitaxial layer: A monocrystalline layer formed by epitaxy, which is normally of a different conductivity type or resistivity from the substrate material.	JESD99C, 12/12
epitaxial peak: An irregular raised point of epitaxial material on an epitaxial surface.	JESD99C, 12/12
epitaxy: Deposition of a monocrystalline layer of material on a substrate material such that the layer thus formed has the same crystal orientation as the substrate. NOTE Examples are silicon on silicon and silicon on sapphire.	JESD99C, 12/12
EPROM: See "erasable programmable read-only memory".	
equilibrium wetting: The degree of wetting in which the forces of wetting are in equilibrium with the forces of gravity. NOTE Visible indication of this is when the wetting balance curve flattens out and approaches zero slope.	J-STD-002B, 2/03
equipment ground: The entire low-impedance path (electrically equivalent to the equipment grounding conductor) from a piece of electrical equipment to a hard-ground electrode, e.g., the third wire (typically green) terminal of a receptacle.	JESD625B, 1/12
equivalent drop height: The free-fall drop height from which an object at rest must fall, in vacuum under standard gravity, to attain a velocity equal to the velocity change stated in the test specification.	JESD22-B104C, 11/04# JESD22-B110A, 11/04#
erasable programmable read-only memory (EPROM): A reprogrammable read-only memory in which all cells can be simultaneously erased using ultraviolet light, after which the cells at each address can be reprogrammed electrically.	JESD21-C, 1/97 JESD100-B, 12/99
erase: To remove information from a memory. (Ref. IEC 748-2.) NOTE In the field of electrically erasable programmable read-only memories, "erase" conventionally means the removal of electrons from the floating gate of the memory cell.	JESD100-B, 12/99
erase algorithm (for a flash EEPROM): The timed sequence of signals necessary to erase the memory.	JESD100-B, 12/99
erase block: The smallest addressable unit for erase operations, typically consisting of multiple pages.	JESD218A, 2/11
erase disturb: The corruption of data in one location caused by the erasing of data at another location.	JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

erase-program cycle: The event of writing a memory cell from the erased state to the programmed state and back to the erased state. JESD100-B, 12/99

NOTE This event may be used as a unit of measurement for endurance. Within a sequence, erase-program cycles are indistinguishable from program-erase cycles.

error band (B_E)†: (1) The band centered around the target time to failure, t_{FT}, within which the SWEAT algorithm will not permit the feedback control loop to adjust the forcing current, and whose boundaries ($t_{FT} + B_E$ and $t_{FT} - B_E$) constitute the limits for the estimated time to failure, t_{FE}, where B_E is half the width of the error band. JEP119A, 8/03

† The symbol B_E has different meanings in definitions (1) and (2). In (1) it means half the width of the error band, but in (2) it means the full width of the error band.

(2) A band of test-line temperatures centered on T_{test}, i.e., JESD61A.01, 10/07

$$T_{test} - B_E/2 \leq T \leq T_{test} + B_E/2$$

where the isothermal algorithm will consider the test-line temperature to be equal to T_{test}, as required during the stress.

NOTE A typical value for B_E is 1 ºC. However, the feedback control loop will continue to adjust the forcing current to keep a constant target stress temperature, T_{test}, even when the test-line temperature is within the error band.

error correction code (ECC); error detection and correction (EDAC): An algorithm that requires adding redundant bits to a nibble, byte, or word to provide the information to allow data correction if one or more of the data bits have been erroneously changed. JESD89A, 10/06#
JESD89-3A, 11/07#

ESD: See "electrostatic discharge".

ESD design window: The ESD protection design space for meeting a specific ESD target level while maintaining the required I/O performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced-technology node. JEP155A.01, 3/12
JEP157, 10/09

ESD ground: The point, electrodes, bus bar, metal strips, or other system of conductors that form a path from a statically charged person or object to ground. JESD625B, 1/12

NOTE This ground may be an AC ground, an auxiliary ground, or an equipotential bonding system.

ESD-protected work station: A work position with the necessary materials, tools, and equipment capable of controlling static electricity to a level that minimizes damage to electrostatic-discharge-susceptible items. JESD625B, 1/12

ESD-protective packaging: A packaging system that provides electrostatic shielding and limits triboelectric charging to levels that do not result in device damage. JESD625B, 1/12

ESD-protective work surface: A table top or other surface that minimizes damage to ESD-susceptible items. JESD625B, 1/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

ESD robustness: The capability of a device to withstand the required ESD-specification tests and still be fully functional. JEP155A.01, 3/12 JEP157, 10/09

ESDS: See "electrostatic-discharge susceptibility [sensitivity]".

ESDS device: Abbreviation for "electrostatic-discharge-sensitive device". JESD625B, 1/12

ESD withstand voltage: The highest voltage level that does not cause device failure, with the device passing all tests performed at lower voltages. JS-001-2012, 4/12

NOTE See note to "failure window".

ESD-work area: A defined location with the necessary materials, tools, and equipment capable of reducing static electricity to a level that minimizes damage to electrostatic-discharge-susceptible items**.** JESD625B, 1/12

ESR: The lumped parameter device resistance in series with the device gate-source capacitance. JESD24-11, 8/96

estimated time to failure (t_{FE}): The time it takes for the combined stress of temperature and current density to result in a prescribed increase in resistance of the test structure (definition of failure) as determined from Black's Equation: JEP119A, 8/03

$$t_{FE} = A \cdot J^{-n} e^{E_a/kT}$$

where

A is an empirically determined constant, provided by the user;
J is the current density (A/cm^2);
n is the current density factor, provided by the user;
E_a is the activation energy of the metallization, provided by the user (eV);
k is Boltzmann's constant (8.62×10^{-5} eV/K);
T is the mean temperature of the test structure (K).

etchant: A solution used for etching. JESD99C, 12/12

etching: A process in which a controlled quantity or thickness of material is removed (often selectively) from a surface by chemical reaction, electrolysis, or other means. JESD99C, 12/12

etching, plasma: A process in which material is removed by a reaction with chemically active radicals created by an ion bombardment in a glow discharge. JESD99C, 12/12

NOTE A mask is usually used in order to remove only selected areas.

etch mark (on a wafer or die): A visual anomaly resulting from an etch that has left a discolored or hazy appearance. JESD22-B118, 3/11

etch pit: A small peak or hole produced by chemical etching at the site of an imperfection in a semiconductor or other surface and caused by the differing etch rate at the point of imperfection. JESD99C, 12/12

EWMA: See "exponentially weighted moving average (chart)".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

excursion: A sudden recordable electrical event that falls outside (above or below) the characteristic response of its electrical distribution. JESD86A, 10/09

NOTE This nonconformity is repeatedly observed during a given period of time.

execution time (for an instruction): The time, normally expressed in clock cycles, required to carry out an instruction. JESD100-B, 12/99

expert systems: A computer-based form of artificial intelligence that provides decision-making capabilities within a system, based on a preprogrammed decision tree founded on knowledge of the process parameters and their interaction. JEP132, 7/98

exponentially weighted moving average (EWMA) chart: A statistical process control (SPC) chart based on weights assigned to past observations. JEP132, 7/98#
EIA-557-B, 2/06#

extrapolated threshold voltage ($V_{T(ext)}$): The threshold voltage extrapolated from measurement of the maximum slope $g_{m(max)}$ of the I_D-V_{GS} curve, as described in ASTM F617-86. $V_{T(ext)}$ can be calculated using JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

$$V_{T(ext)} = V_{GS(gm(max))} - I_{D(gm(max))}/g_{m(max)}$$

where

$V_{GS(gm(max))}$ is the gate voltage at the point of the maximum slope of the I_D-V_{GS} curve;
$I_{D(gm(max))}$ is the drain current at the point of the maximum slope of the I_D-V_{GS} curve;
$g_{m(max)}$ is the maximum slope of the I_D-V_{GS} curve in the linear region.

extrinsic failure mechanism: (1) A failure mechanism caused by an error occurring during the design, layout, fabrication, or assembly process or by a defect in the fabrication or assembly materials. JESD659B, 2/07

(2) A failure mechanism that is directly attributable to a defect created during manufacturing.

extrinsic semiconductor: A semiconductor with charge-carrier concentration dependent upon impurities or other imperfections. (Ref. IEC 747-1.) JESD77D, 8/12

eyelet: A ring of metal used as the outside member of a hermetic lead seal to hold a feed-through in place, typically soldered into the package. JESD9B, 5/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

F

F: See "refresh (F)".

failure: (1) The loss of the ability of a device to meet the electrical, functional, or physical performance specifications that (by design or testing) it was intended to meet.

JEP131B, 4/12
JEP143C, 7/12
JESD22-A117B, 3/09
JESD86A, 10/09
JESD659B, 2/07

NOTE 1 The term *failure* is often qualified by an adjective describing the type of failure. For example, a device is called a "functional failure" if it fails to function and a "parametric failure" if it functions but does not meet a data sheet specification for a parameter such as power consumption.

NOTE 2 Failures may be called "firm" or "transient". A firm failure is a device that fails sometime during a reliability stress and also fails at the final test at the end of that same stress. A transient failure is a device that fails during a reliability stress but passes in the final test at the end of that stress. Sometimes "firm failures" are called "hard failures" and "transient failures" are called "soft failures".

(2) A device or component that has failed.

JEP131B, 4/12
JEP143C, 7/12
JESD86A, 10/09
JESD659B, 2/07

(3) The lack of the ability of a device to meet the electrical or physical performance specifications that (by design or testing) it was intended to meet.

JEP143C, 7/12
JESD218A, 2/11#

NOTE Notes 1 and 2 above also apply here.

failure analysis: (1) A methodical process of testing, dissecting, and inspecting a semiconductor device that is suspected of malfunctioning, with the goals of locating the failure site and determining the cause of failure.

JEP134, 9/98

(2) Investigation to determine the failure mechanism of an electrical or visual/mechanical nonconforming component.

JESD671B, 6/12

failure-analysis laboratory turnaround time: The time period beginning with receipt in the failure-analysis laboratory of a failed device and associated background information and ending with submission of a failure-analysis report and closure with the customer.

JEP134, 9/98

failure analyst: A person, employed by either the manufacturer of the failed device or an independent laboratory, skilled in failure analysis of semiconductor devices.

JEP134, 9/98

failure cause: The physical process that created the failure mechanism.

JEP143C, 7/12
JESD91A, 8/01

NOTE See note 3 to "failure mode (1) (general)".

failure cross section: The number of failures detected per unit beam fluence expressed as area per event.

JESD89-3A, 11/07#

failure kinetics: The characteristics of failure for a given physical failure mechanism, including (where applicable) acceleration factor, derating curve, activation energy, median life, standard deviation, characteristic life, instantaneous failure rate, etc.

JEP143C, 7/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
failure mechanism: The physical, chemical, electrical, or other process that has led to a nonconformance. NOTE 1 A failure mechanism may be characterized by how a degradation process proceeds, including the driving force, e.g., oxidation, diffusion, electric field, current density. When the driving force is known, a mechanism may be described by an explicit failure rate model. NOTE 2 See note 3 to "failure mode (1) (general)".	JEP122G, 10/11 JEP143C, 7/12 JEP156, 3/09 JEP158, 11/09 JESD91A, 8/01 JESD671B, 6/12
failure mechanism from assembly: A physical failure mechanism in which all products with the same assembly technology, including assembly material, assembly construction, and package type, and built on the same assembly line are treated as a homogeneous population for the purpose of statistical reliability monitoring independent of fabrication process and line.	JESD659B, 2/07
failure mechanism from fabrication processes: A physical failure mechanism in which all products with the same wafer fabrication process, design rules, and processing line are treated as a homogeneous population for the purpose of statistical reliability monitoring independent of package technology, material, construction, and type.	JESD659B, 2/07
failure mode (1) **(general):** The way in which a failure mechanism manifests itself in a failing component. NOTE 1 Examples of failure modes are a visual blemish, a bent lead, a foreign particle or material, an incorrect dopant profile or grain size, a scratch, an electrical fault (open, short, leakage, inadequate slew rate or noise margin, stuck at high or low, etc.). NOTE 2 Failure rate distributions for a given failure mode can be modeled only when the failure mechanism and the relevant independent variables (forcing functions) are known. NOTE 3 The relationship among the four terms is illustrated by the following: if the *failure mode* is input leakage, the *failure mechanism* is oxide rupture, the *failure cause* is ongoing application of a voltage field across an oxide containing an interstitial dislocation, and the *root cause* is a contaminant in the oxide growth furnace.	JEP122G, 10/11 JEP143C, 7/12 JEP156, 3/09 JEP158, 11/09 JESD91A, 8/01 JESD671B, 6/12
(2) **(in a BGA ball shear test):** The type or location of failure observed after the solder ball is sheared.	JESD22-B117A, 10/07
failure mode and effect analysis (FMEA): A systematized group of activities intended to recognize, evaluate, and prioritize the potential failure modes of a product or process and the effects of a failure, and then to identify actions that could reduce the probability of occurrence of each failure mode, listed in the order of seriousness of a potential failure in the customer's application. NOTE 1 The FMEA provides a structured analysis in order to assess the probability of occurrence of a failure from the failure mode as well as the effect of the failure. NOTE 2 A fully developed FMEA is continuously maintained and updated to reflect the latest actions and changes to the design or process.	EIA-557-B, 2/06# JEP131B, 4/12# JEP132, 7/98#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

failure rate (λ): The fraction of a population that fails within a specified interval, divided by that interval. JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07 JESD91A, 8/01

NOTE 1 Standard methods of reporting failure rates of semiconductor devices include 1) percent failed per 1000 hours and 2) FITs.

NOTE 2 The interval may be expressed in operating hours, storage hours, operating cycles, or other units of interval measurement.

NOTE 3 Typically, the term "failure rate" means the instantaneous failure (hazard) rate.

NOTE 4 The statistical upper limit estimate of the failure rate is usually calculated using the χ^2 (chi-squared) function.

failure resistance criterion (R_{FC}): The resistance at or above which a structure is considered to have failed. JEP119A, 8/03

failure set: The subset of the sample that fails the defined test criterion during the stress time. JESD37, 10/92

failures in time (FITs): The number of failures per 10^9 device hours. JEP122G, 10/11 JEP143C, 7/12 JESD74A, 2/07 JESD85, 7/01 JESD89A, 10/06 JESD91A, 8/01

failure window: An intermediate range of stress conditions that can induce failure in a particular device type while the device type can pass some stress conditions both more and less strenuous than this range. JS-001-2012, 4/12

NOTE For example, a component with a failure window may pass a 500-V test, fail a 1000-V test, and pass a 2000-V test. Hence, the failure window of the device is between 500 V and 2000 V. The withstand voltage of this device is 500 V.

fall time (t_f) (1) **(general):** The time interval between one reference point on a waveform and a second reference point of smaller magnitude on the same waveform. JESD77D, 8/12

NOTE The first and second reference points are usually 90% and 10%, respectively, of the steady-state amplitude of the waveform existing before the transition, measured with respect to the steady-state amplitude existing after the transition.

(2) **(of an analog integrated circuit):** For a step-function change of the input signal level, the time interval between the end of the delay time (normally 90%) and that instant at which the magnitude of the output signal first passes through a specified value (normally 10%) close to its final value. (Ref. IEC 747-3.) JESD99C, 12/12

(3) **(of a digital integrated circuit):** Synonym for "transition time, high-to-low level". JESD99C, 12/12 JESD100-B, 12/99

(4) **(of a transistor):** (A) The time interval during which the amplitude of the trailing edge of a pulse decreases from 90% to 10% of its maximum amplitude. JESD10, 1/76

(B) Synonym for "current fall time, t_{fi}". JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

fall time charge (Q_{rrf}): That part of the recovered charge that is recovered from the diode during the reverse recovery fall time. JESD77D, 8/12 JESD282-B, 4/00

NOTE The time intervals t_{rrf} and t_{rrr} are defined so that their sum is equal to the reverse recovery time t_{rr}, whereas the recovered charge Q_{rr} is defined for an integration time t_i. As a consequence, the sum of the partial charges Q_{rrf} and Q_{rrr} will differ from Q_{rr} unless t_{rr} equals t_i.

false-write protection: Synonym for "inadvertent-write protection". JESD100-B, 12/99

fan-in: The number of output ports on a net. JESD12-1B, 8/93 JESD99C, 12/12

fan-out: The number of input ports on a net. JESD12-1B, 8/93 JESD99C, 12/12

far-back-end-of-line (FBEOL) (adjective)**:** Pertaining to the portion of the semiconductor processing line that creates the metal layer, e.g., the under bump metallization (UBM) or redistribution layer, and associated interconnect structures forming the connection between on-chip and off-chip wiring. JEP156, 3/09 JEP158, 11/09

far back end of line (FBEOL) (noun)**:** The portion of the semiconductor processing line that creates the metal layer, e.g., the under bump metallization (UBM) or redistribution layer, and associated interconnect structures forming the connection between on-chip and off-chip wiring. JEP156, 3/09 JEP158, 11/09

fault: A defect that may cause a failure in the circuit operation and/or timing. JESD12-5, 8/88

NOTE Subclassifications of faults may not be mutually exclusive.

fault coverage: The percentage of possible faults detected by a set of test vectors. JESD12-1B, 8/93 JESD99C, 12/12

fault detectability ratio: The ratio of detectable faults to the sum of detectable and undetectable faults. JESD12-5, 8/88

fault grading: The process of determining the test-pattern fault coverage of a circuit. JESD12-5, 8/88

fault simulation: The process of applying test vectors to a circuit or circuit model to obtain fault-coverage information. JESD12-1B, 8/93 JESD99C, 12/12

fault-tolerant design: A design approach intended to enhance the ability of a circuit to remain operational after the occurrence of a fault. JESD12-5, 8/88

NOTE Fault-tolerant design techniques may impact fault detection.

FBEOL: See "far-back-end-of-line (adjective)" and "far back end of line (noun)".

FCBGA: See "flip chip ball grid array package".

FCT series: A fast CMOS series that includes devices whose input logic levels are TTL-input-compatible and whose outputs are specified at TTL levels. JESD18-A, 1/93#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

FCTXXX series: An FCT series of fast CMOS devices with a complementary output stage. These are generally referred to as devices with CMOS output swing. JESD18-A, 1/93#

FCTXXXT series: An FCT series of fast CMOS devices with reduced output swing. These devices are generally referred to as devices with TTL output swing. JESD18-A, 1/93#

feature: A physical portion of a part, such as a surface, hole, or slot. JESD95-1, 3/97

feedback sense voltage (of a voltage regulator): The voltage that is a function of the output voltage and is used for feedback control of the regulator. JESD99C, 12/12

feedthrough capacitance (of a multiplying digital-to-analog converter) (C_F): The value of the capacitance for a specified value of resistance in an equivalent circuit for the calculation of the feedthrough error. JESD99C, 12/12

NOTE The equivalent circuit consists of a high-pass R-C filter between the reference input and analog output.

feedthrough error (of a multiplying digital-to-analog converter) (E_F): An error in analog output, due to variation in the reference voltage, that appears as an offset error and is proportional to the frequency and amplitude of the reference signal. JESD99C, 12/12

NOTE 1 The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2 This error may also be expressed as a peak-to-peak analog value.

FEEPROM: See “flash EEPROM”.

FEOL: See “front-end-of-line (adjective)” and “front end of line (noun)”.

FET: See “field-effect transistor”.

FIC: See “integrated circuit, film”.

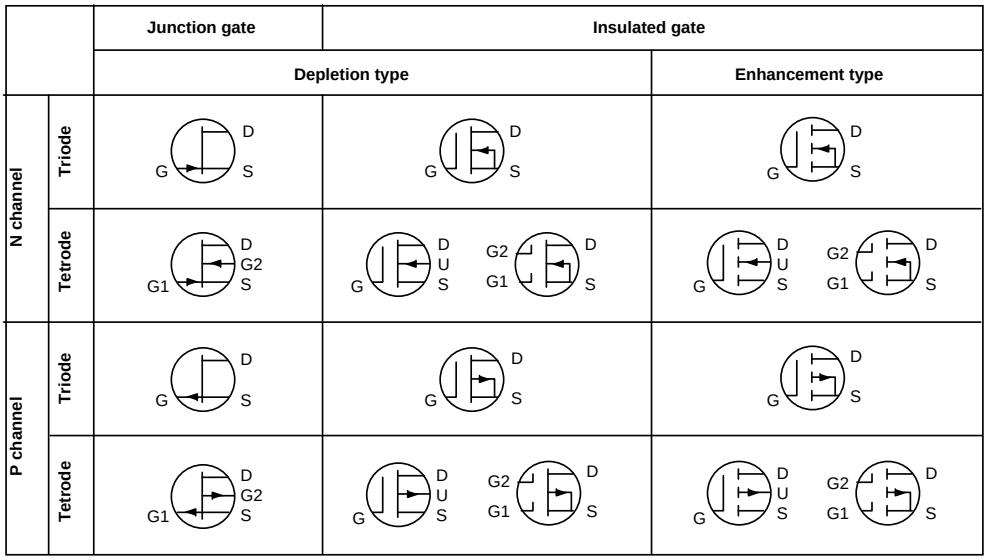
fiducial mark: Synonym for “registration mark”. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

field-effect transistor (FET): A transistor in which the conduction is due entirely to the flow of majority carriers through a conduction channel controlled by an electric field arising from a voltage applied between the gate and the source. JESD24, 7/85 JESD77D, 8/12

Grapic symbols (ref. IEEE Std Std 315)



NOTE In the graphic symbols, the envelope is optional if no element is shown connected to the envelope.

field failure: Any failure that occurs after the completion of all the manufacturer's documented procedures and technology-conformance testing. JEP121A, 10/06

field-induced charging: A charging method using electrostatic induction. JESD22-C101E, 12/09

field lifetime: The expected time a product will function or be needed in the field determined. JESD94A, 7/08

field of view: The area of the test sample under metrological examination. JESD217, 9/10

field-programmable gate array (FPGA): A gate array integrated circuit that can be electrically programmed. JESD12-1B, 8/93 JESD99C, 12/12

field-programmable logic array (FPLA): Synonym for “programmable logic array”. JESD99C, 12/12

field-programmable logic sequencer (FPLS): Synonym for “programmable logic sequencer”. JESD99C, 12/12

field-programmable read-only memory: A read-only memory that, after being manufactured, can have the data content of each memory cell altered. (Ref. IEC 748-2.) JESD100-B, 12/99

film: A thin layer of a substance that has a specified edge or boundary and thickness ranging from indiscernible to measurable. JESD22-B118, 3/11

film (of a film integrated circuit): A layer of solid material formed by any deposition process upon the substrate or upon other films deposited on the substrate. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

film integrated circuit: See "integrated circuit, film".

film microcircuit: Synonym for "integrated circuit, film".

film, plated: A film obtained through chemical and/or electrochemical deposition. JESD99C, 12/12

film technology, thick-: The technology with which electronic circuits or elements are formed by applying a liquid, solid, or paste coating through a screen or mask in a selective pattern onto a supporting material. JESD99C, 12/12

NOTE This technology also includes films deposited by any other means when the films so formed are five micrometers or greater in thickness.

film technology, thin-: The technology with which electronic circuits or elements are formed by vapor deposition, vacuum deposition, or sputtering of films onto a supporting material. JESD99C, 12/12

NOTE This technology also includes similar techniques when the films so formed are less than five micrometers in thickness.

film, thick (of a film integrated circuit): A film produced by a printing process, serigraphy, or other related techniques. JESD99C, 12/12

film, thin (of a film integrated circuit): A film produced by an accretion process such as vapor-phase deposition or sputtering. JESD99C, 12/12

fin (on a package): A fine-feather-edge protrusion occurring at an edge. JESD9B, 5/11

fin, hanging: A fin that can be moved with a probe but is still connected to the surface. JESD9B, 5/11

finite population analysis (FPA): A special case of signature analysis where the signature occurs in a particular finite population of devices. JEP136, 7/99

firing: A process of thick-film formation whereby the screened film is subjected to a precisely controlled high-temperature condition that oxidizes and vaporizes organic binders and modifies the film microstructure to achieve desired properties, including adherence to the substrate. JESD99C, 12/12

firmware: The program instructions stored in a read-only memory. JESD100-B, 12/99

NOTE Computer programs stored on disks, including hard drives and CD-ROMs, are customarily referred to as software.

first-in, first-out (FIFO) memory: A memory from which data can be read only in the same order as entered, although not necessarily at the same rate. JESD100-B, 12/99

fishbone: See "cause and effect diagram".

fit: The external dimensions and associated tolerances of the product, as specified by the supplier and/or customer. JESD46D, 12/11

FITs: See "failures in time".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

fixed freezer: A controlled-temperature chamber capable of maintaining specified subfreezing temperatures over the entire working area. JEP153,1/08

fixed interconnect pattern: A metallization pattern that interconnects circuit elements and is defined by a single, predesigned mask. JESD99C, 12/12

fixed-program read-only memory: A read-only memory in which the data content of each cell is determined during manufacture and is thereafter unalterable. (Ref. IEC 748-2.) JESD100-B, 12/99

flag bit: An information bit that indicates the occurrence of special conditions such as overflow, carry, or interrupt. JESD100-B, 12/99

flaking: The detachment of a sheet-like layer of material from a surface. JESD9B, 5/11

flange-mount package: A package having a flange-mounted heat sink that is an integral part of the package and extends beyond the package body to provide mechanical mounting to a packaging interconnect structure or cold plate. JESD30E, 8/08

flash EEPROM (FEEPROM): An EEPROM in which clearing can be performed only on blocks or on the entire array. JESD21-C, 1/97
JESD100B.01, 12/02

NOTE There are no restrictions on the block architecture in the definition of FEEPROM. The blocks within a device may be of various capacities ranging from a single address to the entire memory array.

flash write with mask (FWM): A write cycle in which the contents of an entire row of the memory array can be selectively set to the stated value. The "mask" value determines which bit planes are to be altered while the "color register" contains the data value to be written. The color register is loaded in a previous load-color-register cycle with a persistent value. The mask value is supplied during the cycle on the DQ(n) terminals. A new mask value must be supplied for each cycle performed. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered. JESD21-C, 1/97

flatpack: A package whose leads project parallel to, and are designed primarily to be attached parallel to, the seating plane. JESD99C, 12/12

NOTE The term "flatpack" has been replaced by "quad flatpack" (for terminals on three or four sides) and "small-outline package" (for terminals on one or two sides).

flattened [nonhierarchical] layout: A geometric description in which all geometries are contained at the lowest hierarchical level. JESD12-1B, 8/93
JESD99C, 12/12

flattened [nonhierarchical] netlist: A netlist in which all logic elements are connected at the lowest hierarchical level. JESD12-1B, 8/93
JESD99C, 12/12

flight delay (of a sgnal): Propagation time of the signal on a transmission line. JESD96, 4/04

flip chip: See "chip, flip".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

flip chip ball grid array (FCBGA) package: A type of ball grid array (BGA) package that consists of a facedown die (flip chip FC) on the organic substrate of a package. JESD217, 9/10

NOTE FCBGA packages typically have a filled epoxy that is dispensed between the die and the substrate.

flip chip die: An unpackaged die whose electrical interconnections to a substrate are formed through solder joints. JESD22-B109A, 1/09

floating gate: A gate electrode that has no ohmic connection and is isolated from the semiconductor by an insulating layer or junction. JESD99C, 12/12

NOTE 1 The potential on the floating gate depends on the quantity of electrical charge stored in a potential well under the surface.

NOTE 2 Floating gates are typically used in signal detection or regeneration circuits.

floating node: A signal line that is not actively forced to a defined high or low level. JESD12-1B, 8/93
JESD99C, 12/12

NOTE In a high-impedance state, the charge (or lack of charge) is trapped at the node with no path to supply or ground voltages.

floating region; floating diffusion: A high-conductivity doped region without ohmic connection into or from which charge packets are transferred by overlapping or adjacent transfer gates. JESD99C, 12/12

NOTE A floating region can be used as the sense node for the charge signal in detection or regenerating circuits.

floor life: The allowable time period after removal from a moisture-barrier bag, dry storage, or dry bake and before the solder reflow process. J-STD-020D.1, 3/08
J-STD-033C, 2/12

floorplanning: The process of defining the physical placement of circuit elements. JESD12-1B, 8/93
JESD99C, 12/12

flow charting; process mapping: Creating a chart that details a chronological sequence of process steps, which provides an opportunity to identify areas for improvement in efficiency and effectivity. JEP132, 7/98#

flow through (FT): A control input that, when true, places the RAM register into the flow-through mode and, when false, places the RAM register into the register mode. JESD21-C, 1/97

fluence (of particle radiation): The number of radiant-energy particles emitted from or incident on a surface during a given period of time, divided by the area of the surface. JESD57, 12/96#
JESD89A, 10/06#
JESD89-3A, 11/07

NOTE 1 The equation **"**fluence = N/A" applies, where N and A represent the quantities number of particles and area. Fluence can be calculated by integrating the flux density over the given period of time, e.g., a run.

NOTE 2 The unit symbol (e.g., cm^{-2}) does not identify particle type because there are no standardized unit symbols for "particle" and types of particles. The particle name may be placed before the term, e.g., "neutron fluence", or in the spelled-out unit name, e.g., "neutrons per square centimeter".

NOTE 3 Fluence of particle radiation incident on a surface is maximized when the surface is perpendicular to the direction of the incident particle flow.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

flux (1) **(luminous):** The time rate of flow of luminous energy. JESD77D, 8/12

(2) **(radiant):** The time rate of flow of radiant energy. JESD77D, 8/12

(3) **(of particle radiation):** Used as a synonym for "flux density" only in JESD57 and JESD89A. JESD57, 12/96# JESD89A, 10/06#

flux density (1) **(luminous):** The luminous flux at a surface divided by the area of the surface. (See also "illuminance" and "luminous exitance".) JESD77D, 8/12

(2) **(radiant):** The radiant flux at a surface divided by the area of the surface. (See also "irradiance" and "radiant exitance".) JESD77D, 8/12

(3) **(of particle radiation):** The time rate of flow of radiant-energy particles emitted from or incident on a surface, divided by the area of that surface. JESD89-2A, 10/07 JESD89-3A, 11/07

NOTE 1 The equation "flux density = $N/A \cdot t$" applies, where N, A, and t represent the quantities number of particles, area, and time.

NOTE 2 The unit symbol (e.g., $cm^{-2} \cdot s^{-1}$) does not identify particle type. The particle name may be placed before the term, e.g., "neutron flux density", or in the spelled-out unit name, e.g., "neutrons per square centimeter second".

NOTE 3 Flux density is maximized when the surface is perpendicular to the direction of the emitted or incident particle flow.

FMEA: See "failure mode and effect analysis".

focal length (in water): The distance in water at which the spot size of the transducer is at a minimum. J-STD-035, 5/99

focus plane; focal plane: The X-Y plane at a depth (Z) in which the amplitude of the acoustic signal is maximized. J-STD-035, 5/99

foil: A relatively thin layer of solid material that can be handled independently of a substrate. JESD99C, 12/12

foldback current limiting: A type of overload protection for voltage regulators wherein, under overload conditions, the load current is reduced to some low level relative to a limiting load current. JESD99C, 12/12

footprint (of a package): The pattern of package leads that is used to define the land patterns on a mating printed circuit board. JESD30E, 8/08

NOTE The footprint may include features necessary for mechanical mounting of the package.

foreign film: A visual anomaly that is a film not stipulated by design, specification, or applicable product drawings, nor intentionally introduced by specified processing. JESD22-B118, 3/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

foreign material (1) **(on a package):** Any adhering material or residue not intentionally added nor included in the piece part composition by design. JESD9B, 5/11

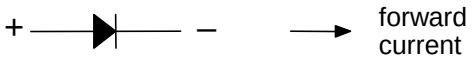
(2) **(on or in a wafer or die surface):** Any adhering material that is not part of the wafer or die under inspection and cannot be removed without damaging the surface, by brushing, by a gas blow-off, and/or by vacuum. JESD22-B118, 3/11

foreign stain: A visual anomaly that is a stain not stipulated by design, specification, or applicable product drawings, nor intentionally introduced by specified processing. JESD22-B118, 3/11

form: The visual appearance including shape, color, marking, and surface finish of the product, as specified by the supplier and/or customer. JESD46D, 12/11

form factor (of a waveform): The ratio of the root-mean-square value of the wave to the average value. JESD282-B, 4/00

forward bias: The bias that tends to produce forward current. JESD77D, 8/12



forward-conducting diode thyristor surge protective device: A two-terminal internally triggered thyristor surge protective device that switches only for negative terminal-2 (cathode) voltage and conducts large currents at positive terminal-2 (cathode) voltages comparable in magnitude to the on-state voltage. JESD77D, 8/12

NOTE 1 In conventional thyristor terminology, this device would be called a reverse-conducting diode thyristor.

NOTE 2 When terminal 2 (cathode) is positive, the device characteristics are similar to those of a forward-biased diode.

NOTE 3 When terminal 2 (cathode) is negative, the device characteristics are similar to those of a breakover-triggered SCR.

forward-conducting region: The portion of the voltage-current characteristic of a forward-biased p-n junction that exhibits a low small-signal resistance to the passage of current. JESD77D, 8/12
JESD210, 12/07
JESD211, 12/09

forward-conducting triode thyristor surge protective device: A three-terminal thyristor surge protective device that switches only for negative main terminal-2 (cathode) voltage and conducts large currents at positive main terminal-2 (cathode) voltages comparable in magnitude to the on-state voltage. JESD77D, 8/12

NOTE 1 In conventional thyristor terminology, this device would be called a reverse-conducting triode thyristor.

NOTE 2 Application of an appropriate fixed gate voltage allows switching to take place at voltages well below the intrinsic breakover value.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

forward current (1) **(in a p-n junction):** The current flowing from the p-type region to the n-type region. JESD77D, 8/12

(2) **(in a semiconductor diode):** The current flowing from the external circuit into the anode terminal. JESD77D, 8/12
JESD282-B, 4/00

forward direction (1) **(general):** The direction of a (positive) forward current. JESD77D, 8/12
JESD282-B, 4/00

(2) **(in an avalanche-junction transient voltage suppressor):** The direction of current that results when the p-type semiconductor region connected to one terminal is at a positive potential relative to the n-type region connected to the other terminal. JESD77D, 8/12

NOTE Any capacitance-reduction diodes that may be included shall be ignored in the determination of forward direction.

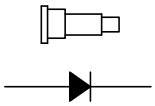
forward gate current (I_{GF}): The direct current into the gate terminal with a forward gate-source voltage applied. JESD24, 7/85
JESD77D, 8/12

forward gate current, drain short-circuited to source (I_{GSSF}): The direct current into the gate terminal of an insulated gate field-effect transistor with a forward gate-source voltage applied and the drain terminal short-circuited to source terminal. JESD24, 7/85
JESD77D, 8/12

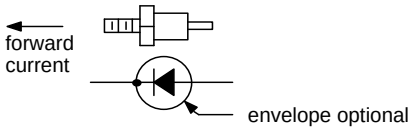
forward mode: The mode in which the drain-to-source polarity during test is the same as that during the application of stress. JESD28-A, 12/01

forward period (of a rectifier circuit element): The part of an alternating-voltage cycle during which forward voltage appears across the rectifier circuit element. JESD282-B, 4/00

forward-polarity (microwave) diode: A microwave diode in which the anode is connected to the base (i.e., the larger-diameter terminal) of the package. JESD77D, 8/12



forward-polarity rectifier diode with heat sink: A rectifier diode whose cathode is connected to the mounting stud or heat sink. JESD77D, 8/12



forward power dissipation: The power dissipation resulting from forward current. JESD77D, 8/12
JESD282-B, 4/00

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
forward recovery time (t_{fr}): The time interval between the instant when the forward voltage rises through a specified first value, usually 10% of its final value, and the instant when it falls from its peak value, V_{FRM}, to a specified low second value, V_{FR}, upon the application of a step current following a zero-voltage or a specified reverse-voltage condition.	JESD77D, 8/12 JESD282-B, 4/00
forward voltage (1) **(across a p-n junction):** The voltage between the p-type region and the n-type region when the p-type region is at a positive voltage relative to the n-type region.	JESD77D, 8/12
(2) **(across a semiconductor diode):** A positive anode-cathode voltage.	JESD77D, 8/12 JESD282-B, 4/00
(3) **(across a voltage regulator diode):** The positive anode-cathode voltage at a specified forward current, I_F.	JESD211, 12/09
FPGA: See "field-programmable gate array".	
FPLA: See "field-programmable logic array".	
FPLS: See "field-programmable logic sequencer".	
fraction nonconforming: The unknown nonconforming proportion of the total population of components. Estimates of fraction nonconforming are derived from samples.	JESD16-A, 4/95
free-air temperature: Synonym for "ambient temperature".	
free-standing state (of a component): The state of a component that is not attached to the next level of assembly packaging.	JEP156, 3/09 JEP158, 11/09
frequency-locked [lock (f)]: The condition of a phase-locked loop (PLL) device where the frequency of the feedback input is equal to the averaged reference input frequency within a designated tolerance.	JESD65B, 9/03
fringe projection: The projection of structured light on the sample utilizing image processing to determine package surface displacement.	JESD22-B112A, 10/09
front-end-of-line (FEOL) (adjective)**:** Pertaining to the portion of the semiconductor processing line that creates active devices, ending with the gate conductors.	JEP156, 3/09 JEP158, 11/09
front end of line (FEOL) (noun**):** The portion of the semiconductor processing line that creates active devices, ending with the gate conductors.	JEP156, 3/09 JEP158, 11/09
FT: See "flow through".	
full body hot air rework: The process of heating a package by directing heated gas at the package body in order to melt only that package's solder connections.	J-STD-020D.1, 3/08
full-bridge (output): Two half-bridge outputs with the load connected between them.	JESD99C, 12/12
NOTE The outputs are normally operated in a complementary fashion; i.e., as one output goes high, the other goes low. If one or both outputs are three-state outputs or if the operation is not complementary, the load current can be turned off.	

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

full-duplex transmission: Synonym for "duplex transmission". JESD100-B, 12/99

full scale (of a unipolar analog-to-digital converter [digital-to-analog converter]): A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep [step] value has the highest absolute value. JESD99C, 12/12

NOTE 1 The subscript for the letter symbol of a characteristic at full scale is "FS".

NOTE 2 In place of a letter symbol, the abbreviation "FS" is commonly used.

full-scale error (of a linear analog-to-digital converter [digital-to-analog converter]) (E_{FS}): The difference between the actual midstep [step] value and the nominal midstep [step] value at specified full scale. JESD99C, 12/12

NOTE Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

full scale, negative (of a bipolar analog-to-digital converter [digital-to-analog converter]): A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep [step] value has the most negative value. JESD99C, 12/12

NOTE 1 The subscript for the letter symbol of a characteristic at negative full scale is "FS–" (e.g., $V_{FS–}$, $I_{FS–}$).

NOTE 2 In place of a letter symbol, the abbreviation "FS–" is commonly used.

full scale, positive (of a bipolar analog-to-digital converter [digital-to-analog converter]): A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep [step] value has the most positive value. JESD99C, 12/12

NOTE 1 The subscript for the letter symbol of a characteristic at positive full scale is "FS+" (e.g., V_{FS+}, I_{FS+}).

NOTE 2 In place of a letter symbol, the abbreviation "FS+" is commonly used.

full-scale range, nominal (of a linear analog-to-digital converter or **digital-to-analog converter) (V_{FSRnom}** or **I_{FSRnom}):** The total range in analog values that can be coded with uniform accuracy by the total number of steps, with this number rounded up to the next higher power of 2. JESD99C, 12/12

NOTE In place of the letter symbols "V_{FSRnom}" and "I_{FSRnom}", the abbreviation "FSR(nom)" is commonly used.

EXAMPLE Using a straight binary n-bit code format, it follows that

FSR(nom) = 2^n x (nominal value of step width), for an analog-to-digital converter, and

FSR(nom) = 2^n x (nominal value of step height), for a digital-to-analog converter.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

full-scale range, (practical) (of a linear analog-to-digital converter or **digital-to-analog converter) (V_{FSR}** or **I_{FSR}) (V_{FSRpr}** or **I_{FSRpr}):** The total range of analog values that correspond to the ideal straight line. JESD99C, 12/12

NOTE 1 The qualifying adjective "practical" may nearly always be deleted from this term, provided that the term "nominal full-scale range" is not also shortened by deleting "nominal". This permits use of the shorter letter symbols or abbreviations. (See note 2.)

NOTE 2 In place of the letter symbols "V_{FSR}" and "I_{FSR}", the abbreviation "FSR" is commonly used; in place of the letter symbols "V_{FSRpr}" and "I_{FSRpr}", the abbreviation "FSR(pr)" is commonly used.

NOTE 3 The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

EXAMPLE Using a straight binary n-bit code format, it follows that

FSR = $(2^n - 1)$ x (nominal value of step width), for an analog-to-digital converter, and

FSR = $(2^n - 1)$ x (nominal value of step height), for a digital-to-analog converter.

full-scale value, nominal (of an analog-to-digital converter or **a digital-to-analog converter) (V_{FSnom}** or **I_{FSnom}):** An analog value derived from the nominal full-scale range: JESD99C, 12/12

— for a unipolar converter, $V_{FSnom} = V_{FSRnom}$; ($I_{FSnom} = I_{FSRnom}$)

— for a bipolar converter, $V_{FSnom} = ½\ V_{FSRnom}$; ($I_{FSnom} = ½\ I_{FSRnom}$).

NOTE 1 In some data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range.

NOTE 2 In place of the letter symbols "V_{FSnom}" and "I_{FSnom}", the abbreviation "FS(nom)" is commonly used.

full-wave rectifier circuit: A circuit that changes single-phase alternating current into pulsating unidirectional current utilizing both halves of each cycle. JESD282-B, 4/00

full-well capacity: Synonym for "charge-handling capacity". JESD99C, 12/12

function: The electrical, mechanical, and thermal performance characteristics of the product, as specified by the supplier and/or customer. JESD46D, 12/11

functional block: A part of a circuit having a defined function that can be designated by a single symbol in a schematic representation. JESD12-1B, 8/93 JESD99C, 12/12

functional density: The number of gates used divided by the entire chip area. JESD12-1B, 8/93 JESD99C, 12/12

NOTE Units are gates used per unit area.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

functional failure: (1) Failure of a device to deliver correct output data or signals during operation (e.g., stuck-high or stuck-low output, open input or output, logic error, etc.). — JEP134, 9/98

(2) A solid-state drive that fails to function properly in a way that is more severe than having a data error. — JESD218A, 2/11

functional failure requirement (of a solid-state drive): The allowed cumulative functional failures over the endurance rating. — JESD218A, 2/11

functional fault: A fault that causes improper logical operation of a circuit. — JESD12-5, 8/88

functional library: The functional models of a set of macros. — JESD12-1B, 8/93
JESD99C, 12/12

functional region (within a semiconductor material): An identifiable volume whose boundaries depend on operating conditions. — JESD77D, 8/12

EXAMPLES space-charge region, channel region.

functional simulation: The process of exercising a particular netlist and functional models by applying input stimuli to observe the functional responses without regard to timing. — JESD12-1B, 8/93
JESD99C, 12/12

functional test: The process of verifying the specified functions of a device without regard to timing. — JESD12-1B, 8/93#
JESD99C, 12/12

function table: A tabulation relating all output digital levels to all necessary or possible input digital levels for sufficient successive time intervals (t_n, t_{n+1}) to completely characterize the static and dynamic functions of the digital integrated circuit. — JESD99C, 12/12

NOTE 1 Digital levels may be expressed in electrical values directly or by predefined symbolic equivalents.

NOTE 2 Contrast with “truth table”.

FWM: See “flash write with mask”.

G

G: See “giga (as a prefix to units of semiconductor storage capacity)”.

G; g: See “gate terminal”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

gain error (of a linear analog-to-digital converter [digital-to-analog converter]) (E_G): The difference between the actual midstep [step] value and the nominal midstep [step] value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. JESD99C, 12/12

NOTE 1 The terms "gain error" and "offset error" should be used only for errors that can be adjusted to zero. Otherwise, the terms "zero-scale error" and "full-scale error" should be used.

NOTE 2 Usually the specified steps for the specification of gain error and offset error are the steps at the end of the practical full-scale range.

NOTE 3 The midstep value of a step is defined (for an analog-to-digital converter) as the value for a point ½ LSB apart from the adjacent transition.

gain point (of an adjustable analog-to-digital converter [digital-to-analog converter]): The point in the transfer diagram corresponding to the midstep [step] value of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed. JESD99C, 12/12

NOTE Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

gate: The electrode associated with the region in which the electric field due to the control voltage is effective. JESD24, 7/85

gate array integrated circuit: A digital integrated circuit containing a fixed topology of circuit elements used to form macrocells and macro functions that are or can be interconnected to implement a logic function. JESD12-1B, 8/93
JESD99C, 12/12

gate capacity (of a gate array): Synonym for "usable gates". JESD12-1B, 8/93
JESD99C, 12/12

gate core area (of a cell-based integrated circuit): The physical area occupied by the logic gates and intercell routing excluding the pad cell area. JESD12-1B, 8/93
JESD99C, 12/12

gate core area (of a gate array): The physical area occupied by the available logic gates and intercell routing excluding the pad cell area. JESD12-1B, 8/93
JESD99C, 12/12

gate core density (1) **(of a cell-based integrated circuit):** The number of gates in the gate core area divided by the gate core area. JESD12-1B, 8/93
JESD99C, 12/12

NOTE Units are gates per unit area.

(2) **(of a gate array):** The number of available gates in the gate core area divided by the gate core area.

NOTE Units are gates per unit area.

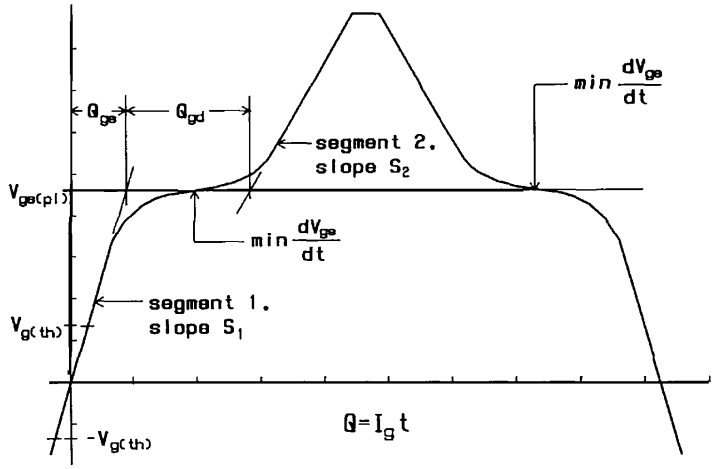
gate current (of a thyristor): The (control) current into the gate terminal. JESD77D, 8/12

gate current, dc (I_G): The direct current into the gate terminal. JESD24, 7/85
JESD60A, 9/04
JESD90, 11/04

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

gate-drain charge; Miller charge (Q_{gd}): The gate charge at $V_{gs(pl)}$ on the calculated line segment 2 less Q_{gs}. (See the figure below.) JESD24-2, 1/91



Turn-on gate waveform

gate-drain voltage, dc (V_{GD}): The dc voltage between the gate terminal and the drain terminal. JESD24, 7/85

gate equivalency of a function (GEF): The number of gate equivalents used to implement a function. JESD12-1B, 8/93
JESD99C, 12/12

gate equivalent (1) **(for CMOS):** The minimum circuitry necessary to implement a two-input NAND gate. JESD12-1B, 8/93
JESD99C, 12/12

(2) **(for ECL):** One-eleventh of the minimum circuitry necessary to implement a single-bit full-adder.

gate-level description: A structural description using logic gates as primitives. JESD12-1B, 8/93
JESD99C, 12/12

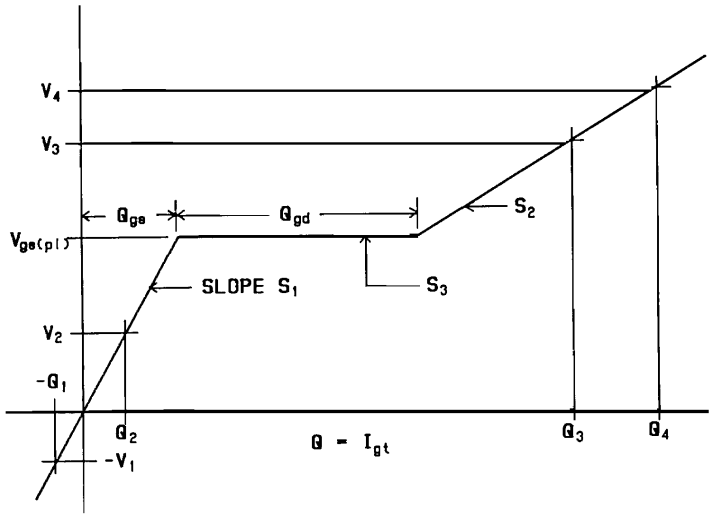
gate, (logic): A combinational logic function consisting of a number of inputs and outputs and performing one of the Boolean functions AND, OR, exclusive OR, NAND, NOR, or exclusive NOR. JESD12-1B, 8/93#
JESD99C, 12/12

NOTE For the purpose of specifying complexity, (1) buffers and inverters are counted as gates and (2) exclusive OR and exclusive NOR gates, some high-input-count gates, and memory functions are counted as multiple gates.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

gate plateau voltage ($V_{gs(pl)}$): The gate-source voltage when dV_{gs}/dt first reaches a minimum during the turn-on switching transition, for a constant-gate-current drive condition. During turn-off, it is the gate-source voltage at the last minimum dV_{gs}/dt observed. JESD24-2, 1/91



Gate plateau voltage

gate region (1) **(of an IGFET):** A control region that determines the surface charge-carrier concentration in the channel region as a function of the gate voltage. JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

(2) **(of a JFET):** A control region that determines the cross-sectional area of the channel region as a function of the gate voltage. JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

(3) **(of a thyristor):** A control region in which a momentary injection of controlling charge causes a regenerative turn-on action. JESD77D, 8/12

NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.

gate-source capacitance (C_{gs}): (1) The capacitance between the gate and source terminals with the drain terminal connected to the guard terminal of a three-terminal bridge. JESD24, 7/85

(2) The capacitance between the gate and source terminals with the drain terminal open-circuited. JESD24-11, 8/96#

gate-source charge (Q_{gs}): The gate charge necessary to reach $V_{gs(pl)}$ on the calculated line segment 1. (See the figure with "gate-drain charge".) JESD24-2, 1/91

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

gate-source threshold charge ($Q_{g\ (th)}$): The gate charge necessary to reach a minimum specified gate threshold voltage. JESD24-2, 1/91

gate-source voltage, dc (V_{GS}): The dc voltage between the gate terminal and the source terminal. JESD24, 7/85
JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

gate terminal (G, g) (1) **(of a field-effect transistor):** The specified externally available point of connection to the gate region. JESD77D, 8/12

(2) **(of a programmable unijunction transistor):** The terminal whose bias conditions determine the values of the unijunction characteristics. JESD77D, 8/12

(3) **(of a thyristor):** The terminal unique to the control circuit. JESD77D, 8/12

gate utilization (in a gate array): The ratio of the number of used gates to available gates. JESD12-1B, 8/93
JESD99C, 12/12

NOTE Gate utilization is usually expressed as a percentage.

gauge repeatability and reproducibility (GR&R): The determination of the capability of a measurement (or test result) by establishing its repeatability and reproducibility. JESD86A, 10/09

Gaussian random vibration: Vibration characterized by having acceleration and frequency values that occur in a stochastic manner over an interval of time, with the acceleration values following a normal (Gaussian) probability density function and frequency values following a uniform distribution. JESD22-B103B, 6/02

GEF: See "gate equivalency of a function".

general-purpose register: A register, usually explicitly addressable, within a set of registers, that can be used for different applications, such as an accumulator, an index register, or a special handler of data. (Ref. IEC 824.) JESD100-B, 12/99

generated defect: A physical defect created during installation or operation. JEP143C, 7/12

NOTE Generated defects are usually created by physical means (e.g., improper handling, electrostatic discharge) or by violation of maximum ratings.

geometric description: A representation of a function in terms of its physical implementation. JESD12-1B, 8/93
JESD99C, 12/12

giga (G) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1 073 741 824 (2^{30} or K^3, where K = 1024). JESD100-B, 12/99

NOTE 1 Contrast with the SI prefix giga (G) equal to 10^9, as in a 1-Gb/s data transfer rate, which is equal to 1 000 000 000 bits per second.

NOTE 2 See note 2 to "mega (M)".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

gigabyte (GB) (in reference to solid-state drive capacity): A memory capacity approximately equal to 1×10^9 bytes. JESD218A, 2/11

NOTE Contrast with gigabyte commonly used as a prefix to units of semiconductor storage capacity and meaning 2^{30} [1 073 741 824] bytes.

glitch (of a digital-to-analog converter): A short, undesirable transient in the analog output following a code change at the digital input. JESD99C, 12/12

glitch area (of a digital-to-analog converter): The time integral of the analog value of the glitch transient. JESD99C, 12/12

NOTE 1 Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2 Instead of a letter symbol, the abbreviation "GA" is in use.

glitch energy (of a digital-to-analog converter): The time integral of the electrical power of the glitch transient. JESD99C, 12/12

NOTE 1 Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2 Instead of a letter symbol, the abbreviation "GE" is in use.

G(n): See "output enable".

GND: See "ground" and "ground reference or source power voltage (pin)".

GNDQ: See "output stage source power voltage or output stage ground reference (pin)".

golden part: A sample device with known characteristics used to monitor the consistency of the beam and tester setup. JESD89-3A, 11/07

GRAM: See "graphics DRAM".

graphics DRAM (GRAM): A DRAM that contains special graphics features similar to those contained in an MPDRAM. (See also "synchronous graphics DRAM (SGRAM)".) JESD21-C, 1/97

grid-array package: A package whose terminals are located on one surface in a matrix of at least three rows and three columns. JESD30E, 8/08

NOTE 1….Terminals may be missing from some row-column intersections.

NOTE 2….See also "ball-grid array".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
ground (GND): (1) The common or zero-potential pin(s) of the device under test.	JESD78D, 11/11
NOTE 1 Ground pins are not latch-up tested.	
NOTE 2 A ground pin is sometimes called VSS.	
(2) A conducting connection, whether intentional or accidental, between an electrical circuit or equipment and the earth or some conducting body that serves in place of earth.	JESD625B, 1/12
(3) The portion of an electrical circuit at zero potential with respect to the earth.	JESD625B, 1/12
(4) A conducting body, such as the earth or the hull of a steel ship, used as a return path for electric currents and as an arbitrary zero-reference point.	JESD625B, 1/12
groundable point: A designated connection, location, or assembly used on an electrostatic-discharge-protective (ESD-protective) material or device that is intended to accommodate electrical connection from the device to an ESD ground.	JESD625B, 1/12
ground reference or source power voltage (pin) (VSS; GND): The ground reference voltage pin for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the term VSS is often used interchangeably with the term GND.	JESD21-C, 1/97
group: A subdivision of a class based on inspection conditions or criteria (e.g., device type, product family, test temperature, sample size). Lots that are members of the same group receive the same set of inspections in that group.	JESD16-A, 4/95
GS: See "synchronous output enable".	
GSF: See "transfer acknowledge output".	
Gunn diode: A transferred-electron diode intended to operate at a frequency determined by the transit time of charge packets or "domains" that are formed due to the transferred-electron effect.	JESD77D, 8/12
H	
half-bridge (output): A bipolar (three-state or totem-pole) power-driver output.	JESD99C, 12/12
half-duplex transmission: Data transmission in either direction, one direction at a time. (Ref. ANSI X3.172.)	JESD100-B, 12/99
half-period jitter ($t_{jit(hper)}$): The magnitude of the deviation in time duration between half-cycle threshold crossings of a signal over a random sample of half cycles.	JESD65B, 9/03
half-wave rectifier circuit: A circuit that changes single-phase alternating current into pulsating unidirectional current utilizing only one half of each cycle.	JESD282-B, 4/00
halogen-free board: Printed board resins plus a reinforcement matrix that contain maximum total halogens of 1500 ppm with less than 900 ppm bromine and less than 900 ppm chlorine. (Ref. IEC 61249-2-21.)	J-STD-609A.01, 2/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

handheld electronic product: An electronic product that can conveniently be stored in a pocket (of sufficient size) and operated when held in the user's hand. JESD22-B111, 7/03 JESD22-B113A, 9/12

NOTE Included in the concept of "handheld electronic products" are cameras, calculators, cell phones, pagers, palm-size PCs (formerly called "pocket organizers"), PCMCIA cards, smart cards, mobile phones, personal digital assistants (PDAs), and other communication devices.

hard error: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events). JESD89A, 10/06 JESD89-1A, 10/07 JESD89-2A, 10/07

NOTE The error is called "hard" because the data is lost and the device or circuit no longer functions properly, even after power reset and re-initialization.

hard macro: Synonym for "macrocell". JESD12-1B, 8/93 JESD99C, 12/12

hardware: Physical equipment, as opposed to programs, procedures, rules, and associated documentation. (Ref. ANSI X3.172.) JESD100-B, 12/99

NOTE Contrast with "software".

hardware accelerator: A system that uses software-configurable hardware to speed up software models that are used to model the network being simulated. JESD12-1B, 8/93 JESD99C, 12/12

NOTE The objective is to achieve faster simulation than can be achieved with software simulators.

harmonic content (of a nonsinusoidal periodic wave): The order and magnitude of the harmonic components. JESD282-B, 4/00

hazard rate: Synonym for "instantaneous failure rate".

haze: A visual anomaly having a partially opaque or cloudy appearance. JESD22-B118, 3/11

HBM: See "human body model".

HBM ESD tester; HBM simulator: Equipment that applies a human body model (HBM) ESD to a device. JS-001-2012, 4/12

HBM simulator: See "HBM ESD tester".

H bridge: Synonym for "full-bridge (output)".

heat dissipater: See "heat sink".

heating current (I_H): A current supplied to the device under test to cause the junction temperature to rise. JESD51-1, 12/95 JESD51-13, 6/09

heating power (P_H): The product of heating current, I_H, and heating voltage, V_H; it causes the junction temperature of the device under test to rise. JESD51-1, 12/95 JESD51-13, 6/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

heating pulse width (t_H): The length of time electrical power, P_H, is applied to the device under test to cause the junction temperature to rise. JESD24-3, 11/90# JESD24-4, 11/90# JESD24-6, 10/91# JESD51-1, 12/95 JESD51-13, 6/09

heating voltage (V_H): The voltage across the device under test during the application of heating current, I_H. JESD51-1, 12/95 JESD51-13, 6/09

heat sink; heat dissipater: A separable element or integral part of the package that aids in dissipating the heat produced within the package. JESD51-1, 12/95# JESD51-13, 6/09# JESD99C, 12/12

heat sink (material): A heat exchange material, typically metal or ceramic, designed to absorb and dissipate excess heat from one or more devices in a circuit. JESD9B, 5/11

heterojunction: A region of transition between two different semiconductor materials, usually with a negligible discontinuity in the crystalline structure. JESD77D, 8/12

NOTE A heterojunction can be between materials of the same conductivity type (isotype heterojunction) or of the opposite conductivity type (anisotype heterojunction).

HIC: See "humidity indicator card" and "integrated circuit, hybrid".

hierarchical description: A description containing two or more nested levels of primitives. JESD12-1B, 8/93 JESD99C, 12/12

hierarchical layout: The layout of a design that exists in multiple hierarchical levels. JESD12-1B, 8/93 JESD99C, 12/12

high-impedance-state output current (I_{OZ}): The current into the output terminal with input conditions applied that, according to the product specification, will establish a high-impedance state at the output. JESD99C, 12/12

high-level input current (I_{IH}): The current into an input terminal when a specified high-level voltage is applied to that input. JESD99C, 12/12

high-level input voltage, "A" limit (V_{IHA}); high-level input voltage, maximum (V_{IH}max): The most positive (least negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected. JESD99C, 12/12

high-level input voltage, "B" limit (V_{IHB}); high-level input voltage, minimum (V_{IH}min): The least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected. JESD99C, 12/12

high-level output current (I_{OH}): The current into the output terminal with input conditions applied that, according to the product specification, will establish a high level at the output. JESD99C, 12/12

high-level output voltage (V_{OH}): The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output. JESD99C, 12/12

high-side driver: A source driver whose primary connection within the integrated circuit is through an active device to a positive supply voltage. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

high-speed carry: In parallel addition, any procedure for speeding up the processing of carries. (Ref. IEC 824.) JESD100-B, 12/99

EXAMPLE Standing-on-nines carry.

histogram: A graph obtained by dividing the range of the data set into equal intervals and plotting the number of data points in each interval against the interval number. EIA-557-B, 2,06#

hold (input) signal: A signal that causes a central processing unit to stop its activity and to relinquish control over the bus until the signal is removed. (Ref. IEC 824.) JESD100-B, 12/99

hold time, (input) (t_h): The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. JESD99C, 12/12
JESD100B.01, 12/02

NOTE 1 The input hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

NOTE 2 The input hold time may have a negative value, in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

hold time, output: Synonym for "valid time, output data-". JESD100-B, 12/99

hole (in a semiconductor material): A mobile vacancy in the electronic valence structure that acts like a positive electron charge with a positive mass. IEEE Std 100

homogeneous material: A material of uniform composition throughout that cannot be mechanically separated into different materials. JIG-101 Ed 2.0, 4/09
J-STD-609A.01, 2/11

NOTE 1 Examples of "homogeneous materials" are certain types of plastics, ceramics, glass, metals, alloys, paper, board, resins, and coatings.

NOTE 2 Methods of mechanical separation include cutting, crushing, grinding, and abrasive processes.

host: The computer system, test system, or other device that writes data to, and reads data from, a memory device. JESD218A, 2/11

host system: A programming system as described in the purpose and scope of JESD32. JESD32, 6/96

host writes: Data transmitted through the primary solid-state drive (SSD) interface to be written to the SSD. JESD218A, 2/11

H switch: Synonym for full-bridge (output). JESD99C, 12/12

NOTE The term "H switch" is usually applied to forward-off-reverse-switching (using one or two three-state outputs) or forward-reverse-switching applications.

human body model (HBM) ESD: An electrostatic discharge (ESD) event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being to a grounded device. JS-001-2012, 4/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

humidity indicator card (HIC): A card on which a moisture-barrier chemical is printed such that it will undergo a significant, perceptible change in color (hue), typically from blue (dry) to pink (wet) when the indicated relative humidity is exceeded. J-STD-033C, 2/12

NOTE The HIC is packed inside the moisture-sensitive bag, along with a desiccant, to aid in determining the level of moisture to which the moisture-sensitive devices have been subjected.

hybrid integrated circuit: See "integrated circuit, hybrid".

hybrid microcircuit: Synonym for "integrated circuit, hybrid".

hysteresis voltage (V_{hys}): The difference between the positive-going and the negative-going input threshold voltages. JESD99C, 12/12

I

I^2t: The product of the square of the rms current and the time for an on-state (or forward) nonrepetitive surge current not exceeding 10 ms in duration for a single discrete element. JESD14, 11/86

IC: See "integrated circuit".

ideal straight line (of a linear analog-to-digital converter [digital-to-analog converter]): In the transfer diagram, a straight line between the specified points for the most positive (least negative) and most negative (least positive) nominal midstep [step] values. JESD99C, 12/12

NOTE The ideal straight line passes through all the points for nominal midstep [step] values.

identification [ID(n)]: A group of output terminals nominally used to convey information about the configuration or other attributes of the device when plugged into a system. The function of these outputs is similar to those of the PD(n) terminals, but the latter often have different electrical interface characteristics. JESD21-C, 1/97

ID(n): See "identification".

IEMP: See "internal electromagnetic pulse".

IGBT: See "insulated-gate bipolar transistor".

IGFET: See "insulated-gate field-effect transistor".

ignore: To place a device in a chain into a "bypass" mode, meaning that no operations are performed on that device. This would be done if devices in a chain were to be selectively programmed, for example. JESD32, 6/96

ILD: See "inter level dielectric".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

illuminance, illumination (E_v): The density of the luminous flux incident on a surface, i.e., the luminous flux divided by the area of the illuminated surface — JESD77D, 8/12

imaginary part of the small-signal open-circuit output admittance, common-emitter [Im(h_{oe})]: The ac collector current divided by the out-of-phase (imaginary) component of the small-signal collector-emitter voltage with the base terminal open-circuited to the emitter for ac. — JESD10, 1/76#

imaginary part of the small-signal short-circuit input impedance, common-emitter [Im(h_{ie})]: The out-of-phase (imaginary) component of the small-signal ac base-emitter voltage divided by the ac base current with the collector terminal short-circuited to the emitter terminal for ac. — JESD10, 1/76#

IMC: See "intermetallic compound".

IMPATT [impact avalanche and transit-time] diode; avalanche diode operating in the IMPATT mode: A semiconductor microwave diode that, when its junction is biased into avalanche, exhibits a negative resistance over a frequency range determined by the transit time of charge carriers through the depletion region. — JESD77D, 8/12

impulse waveshape, standard: A waveform that has a defined virtual front time and a defined virtual time to half peak value. — JESD77D, 8/12 JESD210, 12/07

NOTE 1 Impulse waveshapes may be given for either voltage or current.

NOTE 2 Virtual front time is the time interval between the virtual origin and the instant when the extrapolated leading edge reaches its peak; the extrapolation is made through the 10% and 90% amplitude points for current and the 30% and 90% points for voltage.

NOTE 3 Virtual time to half-peak value is the time interval between the virtual origin and the instant when the amplitude of the trailing edge reaches 50%. This is expressed as a combined front time and time to half-peak value such as 8/20 μs or 10/1000 μs.

inadvertent-write protection: The circuitry used to prevent writing from occurring when the control signals of the memory enter an indeterminate state during power on, power off, or noise transients. — JESD100-B, 12/99

incomplete charge-transfer coefficient: Synonym for "charge-transfer inefficiency".

indentation: A notch or deep recess in a surface. — JESD9B, 5/11

index area (on a package): The area in which a portion or all of the visual or mechanical indexes must lie. — RS-308-A, 8/81 Rescinded 5/09

individual: A single unit or a single measurement of a characteristic. — EIA-557-B, 2/06

infant mortality: The phase in the life of a device during which the mortality function is decreasing. — JEP143C, 7/12

NOTE….As typically used with the bathtub curve, the infant mortality phase precedes the useful life of the device.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

infrared-emitting diode (IRED): A diode capable of emitting radiant energy in the infrared region of the spectrum as a result of the recombination of electrons and holes. (Ref. IEC 747-5.) JESD77D, 8/12

inherent electric field (in a transition region): Synonym for "built-in electric field". JESD77D, 8/12

initial defect: A physical defect inherent in the process architecture, design, or layout, or created during manufacturing (wafer fabrication or assembly) that is manifested during testing or screening. JEP143C, 7/12

initialize input (I): A control input that provides a preassigned manufacturer- or user-defined code to be set into the data register. If the code is all 0s, it can be called "clear", and if all 1s, then "preset". JESD21-C, 1/97#

initialize input (synchronous) (IS): A control input that provides a preassigned manufacturer- or user-defined code to be presented to the data register for subsequent setting by a clock input. If the code is all 0s, it can be called "clear", and if all 1s, then "preset". JESD21-C, 1/97#

ink mark: A mark, on a device, created using applied ink, paint, or other pigment. JESD22-B114A, 5/11

in-line module: A microelectronic assembly whose terminals consist of metal pad surfaces located on one or both sides of a circuit board designed for insertion into an edge connector. JESD30E, 8/08

in-line package: A package having a single row or parallel rows of leads designed primarily for insertion (through-hole) mounting perpendicular to the seating plane. JESD30E, 8/08

NOTE….The leads may emerge from a single side or from two parallel sides with the leads formed to produce parallel rows.

in-process predict parameter: A parameter that characterizes the product prior to the finished product stage. EIA-599-A, 6/98

input and output clock (CK): An input that controls the activation of both input and output circuitry, normally storage registers or latches. JESD21-C, 1/97

input bias current (I_{IB}): The current into the input or the average of the currents into the inputs when the device is in the quiescent or balanced state. JESD99C, 12/12

input buffers: Cells or macros that accept inputs from sources external to the integrated circuit and produce outputs to cells or macros internal to the integrated circuit. JESD12-4, 4/87

input clamp current (I_{IK}): An input current in a region of relatively low differential resistance that serves to limit the voltage swing. JESD99C, 12/12

input clamp voltage (V_{IK}): An input voltage in a region of relatively low differential resistance that serves to limit the voltage swing. JESD99C, 12/12

input clock (K): The input that, on devices that contain input buffer registers, causes the address on the A(n) pins, the data on the D(n) pins, and/or certain control inputs to be set into the register. JESD21-C, 1/97

input current: The current at the input terminals. JESD14, 11/86

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Terms, abbreviations, letter symbols, and definitions	References
input impedance, common-mode (z_{ic}): The parallel equivalent of the small-signal impedances between each input terminal of a differential amplifier and ground.	JESD99C, 12/12
input impedance, differential (z_{id}): The small-signal impedance between two ungrounded input terminals of a differential amplifier.	JESD99C, 12/12
input impedance, single-ended (z_{is}): The small-signal impedance between one input terminal of a differential amplifier and ground with the other input terminal ac-grounded.	JESD99C, 12/12
input load: The load (usually specified in unit loads) represented by a given input.	JESD12-1B, 8/93 JESD99C, 12/12
input offset current (I_{IO}): The difference between the currents into the input terminals of a differential-input device in the balanced state.	JESD99C, 12/12
input offset voltage (V_{IO}): The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other specified level.	JESD99C, 12/12
input/output (I/O): A generic term for an otherwise undefined signal pin that can operate as either an input or an output. This term is not used as a specific pin name but only as a generic indicator of the nature of the function of the pin.	JESD21-C, 1/97#
input/output data mask (DQM): A control signal, used primarily on SDRAMs, that acts as a mask for reading and writing functions. In some instances, the DQM term includes a prefix "U" or "L" indicating upper or lower byte control. In devices where more than two data bit groupings have a data mask applied, an "x" is applied, where "x" takes the values of a, b, c, etc.	JESD21-C, 1/97
input-output voltage differential ($V_I - V_O$): The difference between the input voltage and the output voltage.	JESD99C, 12/12
input pins: All address, data-in, control, V_{ref}, and similar pins.	JESD78D, 11/11
input protective voltage (V_{IP}): An input voltage in a region of relatively low differential resistance that serves to limit the voltage swing for the purpose of input protection.	JESD99C, 12/12
input resistance (r_i): The small-signal resistance between an input terminal and ground or between differential input terminals.	JESD99C, 12/12
inputs for modeling: The substantive and quantifiable attributes or input of a process model that, when combined into a common process or methodology, can be utilized to simulate the desired output.	JEP132, 7/98
input threshold voltage (V_{IT}): The input voltage level that, when crossed, enables an output to change its logic state.	JESD99C, 12/12
input (to a process): Variables or steps that can alter, enhance, and/or validate a process.	JEP132, 7/98
input voltage: The voltage at the input terminals.	JESD14, 11/86
input voltage (of a voltage regulator) (V_I): The supply voltage to be regulated.	JESD99C, 12/12

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Terms, abbreviations, letter symbols, and definitions **References**

insertion loss: The ratio of power delivered to a load with no ABD in the circuit to that delivered after the ABD is inserted. JESD77D, 8/12 JESD210, 12/07

NOTE Insertion loss is generally expressed in decibels. It is frequency-dependent due to the inductance, capacitance, and resistance of the ABD.

inspection: The assessment of a characteristic and its comparison to a standard. EIA-557-B, 2/06 JESD16-A, 4/95

NOTE Examples of inspections include low-temperature electrical tests, room-temperature tests, and visual inspection.

inspection lot: A number of samples from a wafer or die lot that are used for evaluation. JESD22-B118, 3/11

instability, long-term (accuracy) ($\Delta E_{(\Delta t)}$ or $\Delta E_{(t)}$): The additional error caused by the ageing of the components and specified for a relatively long period of time. JESD99C, 12/12

instantaneous failure rate; hazard rate [h(*t*)]: The rate at which devices are failing referenced to the survivors (not to the initial number of units). JEP122G, 10/11 JEP143C, 7/12 JESD85, 7/01

NOTE….h(t) = f(t)/R(t). See "probability density function of the time-to-failure" for f(t) and "cumulative reliability function" for R(t).

instruction register: A register that is used to hold an instruction for interpretation. (Ref. IEC 824.) JESD100-B, 12/99

instruction set (of a microprocessor): All the instructions that can be executed by a given microprocessor. JESD100-B, 12/99

insulated-gate bipolar transistor (IGBT): A three-terminal (collector, emitter, and gate), four-layer (pnpn/npnp) semiconductor device with an MOS-gated channel connecting the two n-type regions (for n-channel types), or the two p-type regions (for p-channel types), and in which the conductance of the high-resistance collector region is modulated (enhanced) by the injection of minority carriers from an opposite-polarity semiconductor region adjacent to the collector and opposite the channel region. JESD77D, 8/12

NOTE 1 The IGBT is a compound semiconductor structure with input characteristics similar to those of a vertical power MOSFET, but containing an additional bipolar component that conductivity-modulates the drain region of the MOSFET section.

NOTE 2 The conductivity modulation of the vertical DMOS power MOSFET drain region substantially reduces the inherent rise in collector-emitter resistance that results with increasing collector-emitter voltage capability.

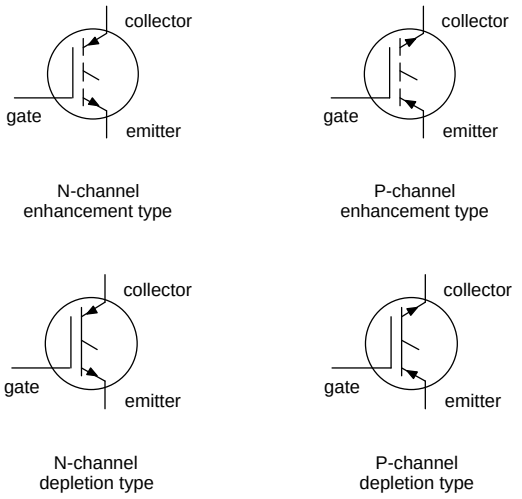
NOTE 3 The IGBT is similar in basic structure to an MOS-gated thyristor but exhibits a fundamental operational difference in that it maintains gate control, i.e., it does not latch, over a wide range of collector current and collector-emitter voltage.

NOTE 4 The term "insulated-gate bipolar transistor" (IGBT) is the generic name for the entire class of conductivity-enhanced MOS-gated pnpn/npnp devices. Other names used to identify these types of devices include conductivity-modulated field-effect transistor (COMFET), gain-enhanced MOS field-effect transistor (GEMFET), insulated-gate transistor (IGT), and insulated-gate rectifier (IGR).

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

Insulated-gate bipolar transistor graphic symbols (ref. IEC 617-5):



NOTE In the graphic symbols, the envelope is optional if no element is shown connected to the envelope.

insulated-gate field-effect transistor (IGFET): A field-effect transistor having one or more gate electrodes that are electrically insulated from the channel. (Ref. IEC 747-8.) JESD24, 7/85 JESD77D, 8/12

NOTE For graphical symbols, see "field-effect transistors".

insulative material: A material having a surface or volume resistance equal to or greater than 1×10^{11}ohms. JESD625B, 1/12

insulator (on a package): A lead seal material (typically matched glass, compression glass, or brazed ceramic) that electrically isolates a lead from the package and creates a hermetic seal. JESD9B, 5/11

insulator climb (on a package): The length of insulator along the lead, measured from the surface of the package to the top of the insulator line on the lead. JESD9B, 5/11

insulator overflow (on a package): Insulator that flows over or out of the designed contained insulator region, which is typically the package hole. JESD9B, 5/11

insulator splatter (on a package): Small particles of insulator that adhere to the surfaces of the package or lead during fusing and remain attached after cleaning or plating or both. JESD9B, 5/11

insulator webbing: The joining of overflow between adjacent seals. JESD9B, 5/11

intct; INTCT: Alternative abbreviations for the word ''interconnect.'' J-STD-609A.01, 2/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

integrated circuit (IC): A circuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purposes of construction and commerce. (Ref. IEC 748-1.) JESD99C, 12/12

NOTE 1 JEDEC and IEC standards on semiconductor integrated circuits generally refer to integrated circuits that are designed as microcircuits.

NOTE 2 To further define the nature of an integrated circuit, additional qualifiers may be prefixed. Examples include

— single-chip integrated circuit,
— multichip integrated circuit,
— thin-film integrated circuit,
— thick-film integrated circuit,
— hybrid film integrated circuit, and
— hybrid semiconductor integrated circuit.

integrated circuit, active hybrid film: A hybrid film integrated circuit in which at least one circuit element is active. JESD99C, 12/12

integrated circuit, analog: A type of linear integrated circuit intended to be used so that the output is a continuous mathematical function of the input. JESD99C, 12/12

NOTE An operational amplifier is an example of an analog integrated circuit.

integrated circuit, application-specific: See "application-specific integrated circuit".

integrated circuit, binary: A digital integrated circuit limited to two logic states at each of its input and output terminals. JESD99C, 12/12

NOTE The high-impedance state of a three-state output is not considered to be a logic state.

integrated circuit, custom: See "custom integrated circuit".

integrated circuit, digital: A type of integrated circuit that is intended to accept particular logic states, changes between logic states, or sequences of logic states at its input terminals, and convert these to logic states at its output terminals according to a set of logic equations or function tables. JESD99C, 12/12

integrated circuit, film (FIC): An integrated circuit whose circuit elements, including the interconnections, are extclusively film elements formed on the surface of an insulating substrate. JESD93, 9/05
JESD99C, 12/12

integrated circuit, hybrid (HIC): An integrated circuit that contains two or more of a single type or a combination of types of the following elements, with at least one of the elements being active: film microcircuit, monolithic microcircuit, discrete semiconductor device, passive chip, or passive element printed or deposited on a substrate. JESD93, 9/05

integrated circuit, hybrid film: A film integrated circuit in which the main parts of the circuit elements are produced as film elements on a substrate and that is completed by mounting additional components on the substrate or elsewhere in the package. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

integrated circuit, hybrid semiconductor: A semiconductor integrated circuit in which the main parts of the circuit elements are produced as semiconductor circuit elements and that is completed by mounting additional components in the package. JESD99C, 12/12

integrated circuit, interface: An integrated circuit that accomplishes the linkage of two systems or parts of a system that would otherwise be incompatible. JESD99C, 12/12

NOTE The signals present at the inputs and the outputs of the interface integrated circuit may take any one of the following forms:

a) digital inputs, analog outputs;

b) analog inputs, digital outputs;

c) analog inputs, analog outputs; or

d) digital inputs, digital outputs. (In this case, the levels of the digital signals at the inputs and the outputs are dissimilar.)

Some circuits of types a, b, and c may also be classified as linear integrated circuits.

integrated circuit, linear: Through common usage, an integrated circuit that is not purely digital. JESD99C, 12/12

NOTE Some circuits of this type may also be classified as interface integrated circuits.

integrated circuit, monolithic (semiconductor): Deprecated synonym for "integrated circuit, single-chip". JESD99C, 12/12

integrated circuit, multichip: A semiconductor integrated circuit containing two or more chips (dice). JESD99C, 12/12

NOTE The use of the term "polylithic semiconductor integrated circuit" is deprecated.

integrated circuit, passive hybrid film: A hybrid film integrated circuit in which all circuit elements are passive. JESD99C, 12/12

integrated circuit, semiconductor: A semiconductor device designed as an integrated circuit. JESD99C, 12/12

integrated circuit, single chip: An integrated circuit or microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate. JESD99C, 12/12
JESD93, 9/05

integrated circuit, thick-film: A film integrated circuit whose circuit elements are thick-film elements. JESD99C, 12/12

integrated circuit, thin-film: A film integrated circuit whose circuit elements are thin-film elements. JESD99C, 12/12

NOTE Usually, thin-film elements are formed by vacuum-deposition techniques, possibly supplemented by other deposition techniques.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

integrated circuit, very-high-speed (VHSIC): An integrated circuit meeting the following goals for speed and density established by the U.S. Department of Defense: JESD99C, 12/12

Phase 1 goals

product of operating frequency and equivalent gate density	5×10^{11} Hz·gates/cm^2 minimum
clock frequency	25 MHz minimum

Phase 2 goals

product of operating frequency and equivalent gate density	1×10^{13} Hz·gates/cm^2 minimum
clock frequency	100 MHz minimum

intentionally added: Deliberately used in the formulation of a product to provide a specific characteristic, appearance, property, or attribute. JIG-101 Ed 2.0, 4/09

interactive layout: The manual modification or influence used in the pattern layout, cell placement, or interconnect routing in an otherwise automatic layout tool. JESD12-1B, 8/93 JESD99C, 12/12

interconnection unit capacitance: The capacitance per unit length attributable to a specified interconnection layer. JESD12-1B, 8/93 JESD99C, 12/12

interconnect layer: A conductive layer used for electrical interconnection of circuit elements on an integrated circuit. JESD12-1B, 8/93 JESD99C, 12/12

interface integrated circuit: See "integrated circuit, interface".

interlevel dielectric (ILD): The dielectric material used to electrically separate closely spaced interconnect lines arranged in several levels (multilevel metallization) in an advanced integrated circuit. JEP160, 11/11

intermetallic compound (IMC): A substance formed when solder comes in contact with another metal at elevated temperature. JEP154, 1/08

NOTE The IMC is composed of multiple constituents from the solder and the other metal. This material has unique mechanical and electrical properties, which are different from those of the initial solder and the other metallization.

intermetallic fracture: A failure found in tensile pull of flip chip solder joints wherein any portion of the fracture surface occurs at an intermetallic formed between the solder and the device or substrate metallization. JESD22-B109A, 1/09

internal circuits: Cells or macros that communicate only with other cells or macros on the same cell-based integrated circuit. JESD12-4, 4/87

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Terms, abbreviations, letter symbols, and definitions **References**

internal electric field (in a transition region): The electric field due to the presence of space charges in the transition region. JESD77D, 8/12

NOTE This field is dependent on the impurity profile of the transition region and on the bias applied between the two adjacent neutral regions.

internal electromagnetic pulse (IEMP): An electromagnetic pulse generated by electrons that are ejected from the surfaces interior to an enclosure with conducting walls due to the interaction of a pulse of energetic photons with the surface material(s). JEP133C, 1/10

internal equivalent temperature: Synonym for "virtual-junction temperature". JESD99C, 12/12

interrupt; interruption: A suspension of a process, such as the execution of a computer program, caused by an event external to that process and performed in such a way that the process can be resumed. (Ref. IEC 824.) JESD100-B, 12/99

interrupt mask: A central processing unit (CPU) feature that allows the computer to ignore (mask) an interrupt request until the mask bit is disabled. JESD100-B, 12/99

interrupt request: An external signal that requests a temporary suspension of the normal program operation in order to permit processing of a higher-priority operation. JESD100-B, 12/99

NOTE Multiple interrupt capability requires establishment of an interrupt-priority system.

intrinsic failure mechanism: (1) A failure mechanism caused by a natural deterioration in the materials or by the manner in which the materials are combined during fabrication or assembly processes that are within specification limits. JESD659B, 2/07

(2) A failure mechanism attributable to natural deterioration of materials processed per specification.

I/O: See "I/O (bidirectional) pins" and "input/output".

I/O (bidirectional) pin: A device pin that can be made to operate as an input or an output or in a high-impedance state. JESD78D, 11/11

ion implantation: A method for doping semiconductors wherein the desired dopant is ionized and accelerated by an electric field, penetrates the surface, and is deposited within the semiconductor material. JESD99C, 12/12

$\boldsymbol{I_R}$**:** See "reverse current".

IRED: See "infrared-emitting diode".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

irradiance (E_e): The density of the radiant flux incident on a surface, i.e., the radiant flux divided by the area of the irradiated surface. JESD77D, 8/12

IS: See "initialize input (synchronous)".

isolation, dielectric: Electrical isolation of one or more elements of a single-chip semiconductor integrated circuit, achieved by surrounding the elements with an insulating barrier such as semiconductor oxide. JESD99C, 12/12

isolation, junction: Electrical isolation of one or more elements of a single-chip semiconductor integrated circuit, achieved by surrounding the element(s) with a region of the conductivity type that forms a junction and reverse-biasing that junction. JESD99C, 12/12

isolation voltage: The rms ac or dc voltage that may be applied continuously between the mounting surface and all of the terminals and also between the terminals of isolated circuits. JESD14, 11/86

isolation withstand voltage: The rms ac or dc voltage used for short-time testing of the insulation between the mounting surface and all of the terminals and also between terminals of isolated circuits. JESD14, 11/86

It2: Failure current under ESD time domain. JEP155A.01, 3/12

NOTE See preferred symbol, term, and definition under "second breakdown trigger current (I_{t2})".

I-test: A latch-up test that supplies positive and negative current pulses to the pin under test. JESD78D, 11/11

i-type [intrinsic] semiconductor: A nearly pure and ideal semiconductor in which the electron and hole densities are nearly equal under conditions of thermal equilibrium. (Ref. IEC 747-1.) JESD77D, 8/12

I_Z: See "regulator [Zener] current, dc".

I_{ZK}: See "regulator [Zener] current near breakdown knee, dc".

I_{zk}: See "regulator [Zener] current near breakdown knee, rms component".

I_{ZM}: See "maximum regulator [Zener] current".

I_{ZRM}: See "repetitive peak reverse surge current".

I_{ZSM}: See "nonrepetitive peak reverse surge current".

I_{ZT}: See "regulator [Zener] current at specified test point, dc".

I_{zt}: See "regulator [Zener] current at specified test point, rms component".

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Terms, abbreviations, letter symbols, and definitions **References**

J

JFET: See "junction-gate field-effect transistor".

jitter: The time deviation of a phase-locked-loop-generated (PLL-generated) controlled edge from its nominal position. JESD65B, 9/03

junction (in a semiconductor device) (general term)**:** A transition region between semiconductor regions of different electrical properties, or a physical region between a semiconductor region and a region of a different type; it is characterized by a potential barrier that impedes the movement of charge carriers from the region of higher concentration to the region with lower concentration. JESD10, 1/76 JESD24, 7/85# JESD77D, 8/12 JESD282-B, 4/00

junction, collector(-base): The transition region between the collector region and the base region. JESD77D, 8/12

junction diode: A semiconductor diode consisting of two physical regions of opposite conductivity type separated by a p-n transition region. JESD77D, 8/12

junction, emitter(-base): (1) **(of a junction transistor)** (A) A semiconductor junction normally biased in the low-resistance direction to inject minority carriers into the base. (Ref. 60 IRE 28.S1.) JESD10, 1/76

(B) The transition region between the emitter region and the base region. JESD77D, 8/12

(2) **(of a unijunction transistor)**: The transition region between the emitter region and a base region. JESD77D, 8/12

junction-gate charge-coupled device: A buried-channel charge-coupled device that uses a diffused junction to isolate the transfer gate. JESD99C, 12/12

junction-gate field-effect transistor (JFET): A field-effect transistor whose gate regions form p-n junctions with the channel. JESD24, 7/85 JESD77D, 8/12

NOTE For graphical symbols, see "field-effect transistors".

junction temperature (T_J): (1) The temperature of a semiconductor junction. JESD10, 1/76 JESD77D, 8/12 JESD99C, 12/12

NOTE In data sheets it is common practice to use this term to mean virtual-junction temperature.

(2) The temperature of the operating portion of a semiconductor device. JESD51-1, 12/95 JESD51-13, 6/09

junction-to-ambient [case] [lead] [mounting-surface](transient) thermal impedance:
See "thermal impedance, junction-to-ambient [case] [lead] [mounting-surface]".

junction-to-ambient [mounting-surface] thermal resistance:
See "thermal resistance, junction-to-ambient [mounting-surface]".

junction-to-case [lead] thermal resistance:
See "thermal resistance, junction-to-case [lead]".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

junction transistor, (bipolar): A bipolar transistor consisting of three succeeding physical regions of alternating conductivity type (npn or pnp) that include the supply region, control region, and collection region and that are separated from each other by two transition regions. JESD77D, 8/12

K

K: (1) A thermal calibration factor equal to the reciprocal of the temperature coefficient of base-emitter voltage (α_{VBE}). JESD24-4, 11/90

(2) A thermal calibration factor equal to the reciprocal of the temperature coefficient of gate-emitter on-state voltage (VTC). JESD24-6, 10/91

K: See "input clock".

K: See "kilo (as a prefix to units of semiconductor storage capacity)".

K, k: See "cathode terminal".

***k*:** See "Boltzmann's constant".

K factor: The change in junction temperature divided by the change in a temperature-sensitive parameter (TSP) in the linear region of the TSP-temperature characteristic. JESD51-1, 12/95#
JESD51-13, 6/09#

K factor calibration: The measurement and data-reduction process that results in values of K factor for the semiconductor device under test. JESD51-1, 12/95
JESD51-13, 6/09

kilo (K) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1024 (2^{10}). JESD21-C, 1/97#
JESD100-B, 12/99

NOTE 1 Contrast with the SI prefix kilo (k) equal to 10^3, as in a 1-kb/s data transfer rate, which is equal to 1000 bits per second.

NOTE 2 See note 2 to "mega (M)".

known good die: A die that has been processed through test with or without burn-in prior to final assembly to guarantee functionality. JESD22-B118, 3/11

L

L: See "latch enable".

L: See "lower byte".

LAR: See "lot acceptance rate".

large-signal insertion power gain, common-emitter (G_{PE}): The ratio, usually expressed in dB, of the signal power delivered to the load to the large-signal power delivered to the input. JESD10, 1/76

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
large-signal output power, common-emitter (P_{OE}): The product of the large-signal ac output current and voltage in the common-emitter circuit configuration.	JESD10, 1/76
laser mark: A mark, on a device, created by using a laser to ablate or melt the device surface, to bond a contrasting labeling material, or to activate a pigmented coating.	JESD22-B114A, 5/11
laser reflectometry: Use of a confocal microscope to determine focal plane and thereby measure the displacement of a surface.	JESD22-B112A, 10/09
last-in, first-out (LIFO) memory: Synonym for "pushdown storage".	JESD100-B, 12/99
latched PROM (LPROM): A PROM that contains a latch register for the output data.	JESD21-C, 1/97
latch enable (L): On devices containing a latch register**,** an input that causes the data to be latched into the register.	JESD21-C, 1/97
latch-up: A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition.	JESD78D, 11/11 JESD99C, 12/12
NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.	
NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.	
latch-up (of a voltage regulator): A condition in which a regulator has been driven into the foldback limiting mode and will not respond to the removal of the overload.	JESD99C, 12/12
latent defect: A physical defect inherent in the process architecture, design, or layout, or created during manufacturing (wafer fabrication or assembly) that is manifested after some period of operation.	JEP143C, 7/12
layer, accumulation: A surface region of a semiconductor device whose conductivity type is the same as that produced by the net fixed charge density of ionized donors and acceptors and whose net carrier density is higher than that necessary for neutralization due to charge carrier attraction.	JESD99C, 12/12
NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.	
layer, buried: A distinguishable region introduced under a semiconductor circuit element, for example, under the collector region of a transistor to reduce the series collector resistance.	JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

layer, depletion (1) **(associated with a p-n semiconductor junction):** A region whose conductivity type on each side of the junction is the same as that produced by the net fixed charged density of ionized donors and acceptors but whose net carrier density is insufficient for neutralization due to the built-in potential barrier of the p-n junction and, if present, an applied reverse bias. JESD99C, 12/12

(2) **(associated with a surface):** A surface region of a semiconductor device whose conductivity type is the same as that produced by the net fixed charge density of ionized donors and acceptors but whose net carrier density is insufficient for neutralization due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

layer, diffused: The region of a semiconductor into which impurity dopants have been diffused to a concentration of at least the background concentration. JESD99C, 12/12

NOTE The region is often delineated by a p-n junction.

layer, enhancement: Synonym for "accumulation layer". JESD99C, 12/12

layer, inversion: A surface region of a semiconductor device whose conductivity type has been reversed from that produced by the net fixed charge density of ionized donors and acceptors due to charge carrier attraction. JESD99C, 12/12

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

LB: See "lower byte enable".

LBA: See "logical block address".

LBO: See "linear burst order".

LCR: See "load color register".

leaching: Synonym for "dissolution of termination metallization". J-STD-002B, 2/03

lead: A flexible, semi-flexible, or solid/rigid conductor extending from the microcircuit and used for electrical and mechanical connections. JESD9B, 5/11

NOTE 1 Leads may be classified as round (pin, nail-head pin, terminal, etc.) or flat (etched or stamped planar, etc.).

NOTE 2 Leads are typically surrounded by an insulator for electrical connections isolated from the metal package or brazed directly to the metal package for electrical (ground) connections to the package. They are typically brazed directly to the braze pad for electrical connections to a ceramic package.

lead-conduction-cooled device: A device at least 90% of whose internal power losses are dissipated by thermal conduction through the leads to the mounting connections. RS-323, 3/66

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

leaded solder: A solder sphere composed primarily of tin (Sn) and lead (Pb) elements. JESD217, 9/10

NOTE 63%/37% (SnPb) and 60%/40% (SnPb) are predominant formulations and are commonly referred to as eutectic solder.

lead frame (of a package): A metal frame providing external terminals and mechanical support to align them. JESD99C, 12/12

leadframe (L/F) view area: The imaged area that extends from the outer leadframe edges of the package to the leadframe "tips" (the wedge-bond/stitch-bond region of the innermost portion of the leadframe). (Refer to Type V in Annex A of J-STD-035.) J-STD-035, 5/99

lead-free: See "Pb-free".

lead head: On a ceramic package, the portion of the lead intended to be brazed to the braze pad. JESD9B, 5/11

lead-location gauge plane: A plane perpendicular to the terminal leads that may be coincident with the seating plane or located at a defined distance from it. The locations of the terminals are measured at the gauge plane. RS-308-A, 8/81 Rescinded 5/09

leakage current (I_{Ikg}): The current that results from nonideal conditions. JESD99C, 12/12

NOTE Examples of such conditions include surface contamination or rupture of an insulator and cracks or metal inclusions in semiconductor junctions.

least material condition (LMC): A feature of size that contains the least amount of material, e.g., minimum shaft diameter or maximum hole diameter. JESD95-1, 3/97

LED: See "light-emitting diode".

LED array: Two or more individual LED chips mounted in a package or on a substrate in a manner such that any device in the array can be powered through series, parallel, series/parallel, or individual connections while the other devices in the array may or may not be operating. JESD51-51, 4/04

NOTE The individual LED chips may also each consist of an array of LED junctions on a chip.

legibility: The ability of a character or symbol to be read or deciphered. JESD22-B114A, 5/11

LET: See "linear energy transfer" and also "effective LET" and "threshold LET".

letter symbol (for a quantity or a unit): One or more letters written successively and without spacing, in a specified style and often provided with additional marks, by convention representing a quantity or a unit. (Ref. ANSI Y10.1 and IEC 27-1.) JESD77D, 8/12 JESD99C, 12/12

NOTE In a few special cases, nonalphanumeric signs are considered as letters in this connection, e.g., the sign ° (degree), which is used as a letter symbol for a unit of angle and in the letter symbol °C for a unit of temperature.

level 1 (L1) interconnect: Synonym for "chip-to-substrate-interconnect".

level D interconnect: Synonym for "chip-to-chip interconnect".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

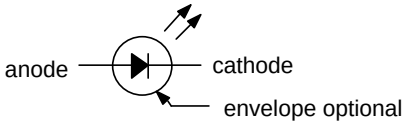
Terms, abbreviations, letter symbols, and definitions **References**

library: A set of circuit cells including their design parameters. JEP148A, 12/08

light: Radiant energy within the limits of the visible spectrum. JESD77D, 8/12

light-emitting diode (LED): A diode capable of emitting luminous energy resulting from the recombination of electrons and holes. (Ref. IEC 747-5.) JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



limiting cross section: Synonym for "saturated cross section".

linear ADC: An analog-to-digital converter having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values. JESD99C, 12/12

NOTE Ideally, the width of each end step is one half the width of any other step.

linear bar code label: A label that gives information in a code consisting of parallel bars and spaces. J-STD-609A.01, 2/11

NOTE See also "bar code label".

linear burst order (LBO): A control input that,when true, causes the burst counter to generate addresses in sequential order and, when false, to generate addresses in a specified interleaved order. JESD21-C, 1/97

linear DAC: A digital-to-analog converter having steps ideally of equal height. JESD99C, 12/12

linear drain current ($I_{D(lin)}$): The drain current measured when the transistor is biased in the linear region. JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

linear drain voltage ($V_{DS(lin)}$): The drain-to-source voltage for linear region measurements. JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

linear energy transfer (LET): The amount of energy per unit length deposited or transferred by radiation traversing a material. JEP133C, 1/10 JESD57, 12/96#

NOTE 1 The energy carried away by the secondary electrons that are produced must be taken into account when calculating the energy deposition.

NOTE 2 The energy deposition or charge transfer mechanism will depend on the type and energy of the radiation, e.g., pair-production, Compton scattering, Bremsstrahlung, collisions, photoelectric effect, and radiative capture.

NOTE 3 LET is strictly defined in terms of energy divided by distance, e.g., MeV/cm, eV/nm, keV/μm. However, since the energy lost is directly proportional to the density of the material traversed, it is useful to divide the LET by the density of the material. For the purposes of certain publications, this derived quantity, whose units are typically expressed as MeV·cm^2/mg (i.e., MeV/cm divided by mg/cm^3), is often also referred to as linear energy transfer (LET) but more often has been loosely designated as "LET effective", which is not to be confused with "effective LET".

linearity: The difference in the accuracy/bias values through the expected operating range of the gauge. JEP132, 7/98

linearity error, best-straight-line (of a linear and adjustable analog-to-digital converter) ($E_{L(adj)}$) ($E_{L(adj)}$): The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. JESD99C, 12/12

NOTE 1 The inherent quantization error is not included in the best-straight-line linearity error of an analog-to-digital converter. The ideal value for the transition corresponds to the nominal midstep value ±½ LSB.

NOTE 2 For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error.

linearity error, best-straight-line (of a linear and adjustable digital-to-analog converter) ($E_{L(adj)}$) ($E_{L(adj)}$): The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. JESD99C, 12/12

NOTE For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error.

linearity error, differential (of a linear analog-to-digital converter [digital-to-analog converter]) (E_D) converter]) (E_D): The difference between the actual step width [height] and the ideal value (1 LSB). JESD99C, 12/12

NOTE A differential linearity error greater than 1 LSB can lead to missing codes in an analog-to-digital converter or to nonmonotonicity of an analog-to-digital converter [a digital-to-analog converter].

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

linearity error, end-point (of a linear and adjustable analog-to-digital converter) (E_L): The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero. JESD99C, 12/12

NOTE 1 The shortened term "linearity error" is commonly used and is sufficient if no ambiguity with the term "best-straight-line linearity error" is likely to occur.

NOTE 2 The inherent quantization error is not included in the linearity error of an analog-to-digital converter. The ideal value for the transition corresponds to the nominal midstep value ±½ LSB.

linearity error, end-point (of a linear and adjustable digital-to-analog converter) (E_L): The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero. JESD99C, 12/12

NOTE The shortened term "linearity error" is commonly used and is sufficient if no ambiguity with the term "best-straight-line linearity error" is likely to occur.

line driver: A circuit designed for driving a data transmission line. JESD99C, 12/12

line receiver: A circuit designed for receiving data from a transmission line. JESD99C, 12/12

line regulation ($\Delta V_{O(\Delta VI)}$): The change in output voltage, usually expressed as a percentage of output voltage, for a change in input voltage. JESD99C, 12/12

line-transient recovery time (of a voltage regulator) (t_{RVI}): The time interval between a step-function change of the input level and that instant at which the magnitude of the output level enters for the last time a specified level range containing the final output level. JESD99C, 12/12

little endian: The format in which the least significant bit of a word is transferred first and the most significant bit is transferred last. JESD96, 4/04

live-bug (orientation): The orientation of the package when resting on its terminals. J-STD-020D.1, 3/08

LMC: See "least material condition".

load color register (LCR): A nonmemory cycle in which the color register is loaded with a new value for use in subsequent special cycles that utilize its contents. JESD21-C, 1/97

load current (I_L); output current (I_O) (of a voltage regulator): The current that is supplied to the load by the regulator. JESD99C, 12/12

load map: A map of the positions where devices are placed for testing within the working area. JEP153,1/08

load regulation ($\Delta V_{O(\Delta IL)}$ and $\Delta V_{O(\Delta IO)}$): The change in output voltage, usually expressed as a percentage of output voltage, for a change in load current. JESD99C, 12/12

load-transient recovery time (of a voltage regulator) (t_{RIL} and t_{RIO}): The time interval between a step-function change of the load current and that instant at which the magnitude of the output level enters for the last time a specified level range containing the final output level. JESD99C, 12/12

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Terms, abbreviations, letter symbols, and definitions **References**

load write mask register (LWR): A nonmemory cycle in which the write mask register is loaded with a new value for use in subsequent masked write cycles. JESD21-C, 1/97

location: The typical value or central tendency of a distribution. EIA-557-B, 2/06

locus conditions: The envelope established by the combined effects of tolerance of size or form and location. Two such conditions exist: JESD95-1, 3/97

a) outer locus (OL)

1) For a male feature, the worst-case (largest) boundary or envelope of the outer surface of the feature as it moves around the tolerance zone of position.

OL = MMC + positive tolerance

2) For a female feature, the worst-case (largest) boundary or locus formed outside of the surface of the feature as it moves around the tolerance zone of position.

OL = LMC + positive tolerance

where MMC is maximum material condition and LMC is least material condition.

b) inner locus (IL)

1) For a male feature, the worst-case (smallest) boundary or locus formed inside the surface of the feature as it moves around the tolerance zone of position.

IL = LMC – positive tolerance

2) For a female feature, the worst-case (smallest) boundary or envelope of the inner surface of the feature as it moves around the tolerance zone of position.

IL = MMC – positive tolerance

logarithmic sweep: A continuous varying of the frequency in a manner such that within any portion of the frequency range, a fixed number of decades is traversed in a fixed length of time. JESD22-B103B, 6/02

logical block address (LBA): The logical address used to reference a data sector (block) in the drive. JESD218A, 2/11

NOTE 1 LBA is synonymous with the data sector itself.

NOTE 2 A block in the drive is a logical construct separate from that of an erase block in a nonvolatile memory.

NOTE 3 A data sector is a logical address space containing one or more pages or erase blocks.

logic feedback: A circuit configuration in which the output of a logic circuit controls an input signal to the same circuit. JESD12-1B, 8/93
JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

logic function: A definition of the relationships that hold among a set of input and output logic variables. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

logic-high: A level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states. JESD78D, 11/11

NOTE 1 For digital devices, the maximum value of the high logic level voltage is used for latch-up testing.

NOTE 2 For nondigital devices, the maximum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

logic level: Any level within one of two nonoverlapping ranges of values of a physical quantity used to represent the logic states. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

NOTE A logic variable may be equated to any physical quantity for which two distinct ranges of values can be defined. In this standard, these distinct ranges of values are referred to as logic levels and are denoted as the high level and the low level.

logic-level converter; logic-level translator: A circuit used to convert logic voltage levels of one family to corresponding logic levels of another family, such as from ECL to TTL. JESD99C, 12/12

logic-low: A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states. JESD78D, 11/11

NOTE 1 For digital devices, the minimum value of the low logic level voltage is used for latch-up testing.

NOTE 2 For nondigital devices, the minimum operating voltage that can be applied to that pin as defined in the device specification is used for latch-up testing.

logic power voltage (VCC): (1) The more positive of the two logic supply voltage pins. The name VCC is used for the memory device supply voltage pin when the supply voltage is nominally 5 V. JESD21-C, 1/97

(2) The ground reference power supply voltage for ECL interface devices.

logic setup (LS): A special nonmemory cycle in which the logic state of the device is set up to actuate the desired mode of operation for future memory cycles. The selected mode is normally persistent until canceled by some subsequent special control cycle. JESD21-C, 1/97

logic state: One of two possible abstract states that may be taken on by a logic (binary) variable. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

logic synthesis: The process of transforming behavioral, structural, or register-transfer-level descriptions into structural descriptions based on a given set of implementation criteria. JESD12-1B, 8/93
JESD99C, 12/12

logic unit: The part of a processor that performs logic operations. (Ref. IEC 824.) JESD100-B, 12/99

lognormal distribution: The assumed distribution of the failure time for the parent population from which samples are taken. The logarithms of the failure times are assumed to follow a normal distribution. JESD37, 10/92

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Terms, abbreviations, letter symbols, and definitions	References
long-form package: A cylindrical or elliptical tubular package having terminal endcaps or axial leads.	JESD30E, 8/08
long-term capability: The process capability under normal operating conditions over an extended period of time.	EIA-557-B, 2/06
long-term storage (LTS): Uninterrupted storage for which the conditions and requirements of J-STD-033 do not apply; e.g., safe storage, shelf life, floor life. NOTE Allowable storage durations will vary by form factor (e.g., packing materials, shape) and storage conditions. In general, long-term storage is greater than one year.	JEP160, 11/11
look-ahead carry: A high-speed carry procedure in which a group of carry digits is formed in parallel from the respective input bits of the two groups that are to be added and, if it exists, from the most significant carry digit that immediately precedes those groups. (Ref. IEC 824.)	JESD100-B, 12/99
lot: An aggregate of components from which the sample is selected.	JESD16-A, 4/95
lot acceptance rate, (estimated) (LAR): An estimate of the probability of lot acceptance under the sampling plan, i.e., the probability that the sample contains no more than the "accept number" of nonconforming components.	JESD16-A, 4/95
low-capacitanceABD: A two-terminal device that has at least one unidirectional ABD with at least one rectifier p-n junction connected in series with each ABD in the opposite polarity in order to reduce capacitance. NOTE The rectifier p-n junction(s) operate only in their forward-conducting mode during a transient event.	JESD77D, 8/12 JESD210, 12/07
lower byte (L): An indicator used in conjunction with a data or control term to signify that the combined term applies to the lower byte of a two-byte data interface device; e.g., LW means write enable, lower byte.	JESD21-C, 1/97
lower byte enable (LB): On word-wide devices, an input that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.	JESD21-C, 1/97
lower byte write enable (LW): On word-wide devices, an input that, when true, causes the data present on the lower byte input/output, terminals DQ0 through DQ7, to be written into the addressed cells of the device.	JESD21-C, 1/97
low-frequency limit: A frequency-dependent electrical model parameter value asymptotically projected to very low frequency, at which various high-frequency phenomena (e.g., skin effect in the lead, parasitic coupling to neighboring elements, effects of capacitance in inductors and inductance in capacitors) have negligible effect. Such a value is often used in single-lump models.	JEP123, 10/95
low-halogen: Meeting the criteria established in JS709.	JS709A, 5/12

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Terms, abbreviations, letter symbols, and definitions **References**

low-level charge (for digital signal applications of a charge-transfer device): A charge that defines the low level of the digital signal. JESD99C, 12/12

NOTE 1 This charge is inserted into all potential wells, usually electrically but occasionally by radiation.

NOTE 2 The term "fat zero" has often been used but is deprecated.

low-level input current (I_{IL}): The current into an input terminal when a specified low-level voltage is applied to that input. JESD99C, 12/12

low-level input voltage, "A" limit (V_{ILA}); low-level input voltage, maximum (V_{IL}max): The most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected. JESD99C, 12/12

low-level input voltage, "B" limit (V_{ILB}); low-level input voltage, minimum (V_{IL}min): The least positive (most negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected. JESD99C, 12/12

low-level output current (I_{OL}): The current into the output terminal with input conditions applied that, according to the product specification, will establish a low level at the output. JESD99C, 12/12

low-level output voltage (V_{OL}): The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output. JESD99C, 12/12

low-side driver: A sink driver whose primary connection within the integrated circuit is through an active device to the circuit common. JESD99C, 12/12

LPROM: See "latched PROM".

LS: See "logic setup".

LSA [limited space-charge accumulation] diode: A transferred-electron diode similar to the Gunn diode except that it is intended to operate at frequencies that are determined by the microwave cavity in which the diode is mounted and that are several times higher than the transit-time frequency so that the formation of charge packets (or domains) is limited. JESD77D, 8/12

NOTE Compared to the Gunn diode, higher output power at higher frequency is achievable.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

LSB: (1) The abbreviation for "least significant bit", that is, for the bit that has the lowest positional weight in a natural binary numeral. JESD99C, 12/12

EXAMPLE In the natural binary numeral "1010", the rightmost bit "0" is the LSB.

(2) The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

EXAMPLE "½ LSB" means an analog quantity equal to one half of the analog resolution.

NOTE The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral. In this case, the identity "1 LSB equals the analog resolution" leads, for an n-bit resolution, to

$$1\,\mathrm{LSB} = \frac{\mathrm{FSR}}{2^n - 1} = \frac{\mathrm{FSR(nom)}}{2^n}.$$

LSI: Large-scale integration. JESD99C, 12/12

LTS: See "long-term storage".

LTS packaged hardware: The wafers, dice, or encapsulated devices that have additional packaging for storage to protect from moisture and mechanical impact and for ease of identification and handling. JEP160, 11/11

LTS storeroom: An area containing wafers, dice, or packaged devices that have additional packaging for storage to protect from moisture or from mechanical impact or for ease of identification or handling. JEP160, 11/11

luminous exitance (M_v): The density of the luminous flux leaving an emitter surface, i.e., the luminous flux divided by the area of the emitting surface. JESD77D, 8/12

LW: See "lower byte write enable".

LWR: See "load write mask register".

M

M: See "mask/mode".

M: See "mega (as a prefix to units of semiconductor storage capacity)".

M: See "mode control".

MA: See "match".

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Terms, abbreviations, letter symbols, and definitions **References**

machine cycle: The sequence of operations that corresponds to one memory cycle, input/output (I/O) cycle, or equivalent internal operation in a central processing unit (CPU). (Ref. IEC 824.) JESD100-B, 12/99

NOTE An instruction may require one or more machine cycles for its execution. A machine cycle usually contains more than one clock cycle.

macrocell; hard macro: A characterized fixed layout and interconnection of primitives that implement an electrical function. JESD12-1B, 8/93 JESD99C, 12/12

NOTE Characterization may be done either by measurement of fabricated devices or by computer simulation or by both. Characterization may include the following aspects: physical dimensions, logic functionality, testability, layout-rule compliance, ac and dc electrical performance, and reliability.

macrocell area: The physical cell area contained within a polygon (often a rectangle) that circumscribes the cell. (See also "unit gate size".) JESD12-1B, 8/93 JESD99C, 12/12

macro function; soft macro: An interconnection of primitives and/or macrocells that implements an electrical function but has no predetermined physical layout. JESD12-1B, 8/93 JESD99C, 12/12

main storage: The part of internal storage into which instructions and other data must be loaded for subsequent execution or processing. (Ref. ANSI X3.172.) JESD100B.01, 12/02

main terminal 1 (MT1) (of a bidirectional triode thyristor): The main terminal intended by the thyristor manufacturer to conduct the control current in addition to the principal current. JESD77D, 8/12

NOTE Some bidirectional triode thyristors are completely symmetrical, e.g., SBS thyristors. For these, the choice for the manufacturer is arbitrary, and the user can return the control circuit to whichever main terminal will provide the required polarity of gate current.

main terminal 2 (MT2) (of a bidirectional triode thyristor): The other main terminal after main terminal 1 has been designated by the thyristor manufacturer. JESD77D, 8/12

main terminals (of a thyristor): The two terminals through which the principal current flows. JESD77D, 8/12

majority carrier: The type of carrier constituting more than half of the total charge-carrier concentration. JESD77D, 8/12

manufacturer's exposure time (MET): The maximum cumulative time after bake that devices may be exposed to ambient conditions prior to shipment to the end user. J-STD-020D.1, 3/08 J-STD-033C, 2/12

manufacturing: All areas and operations where products or services are processed, stored, or handled. EIA-557-B, 2/06

manufacturing process change acceptance, surface finish: Acceptance testing of a change to a surface finish manufacturing process already accepted by a *technology acceptance* (q.v.). JESD201A, 8/08

mark (on a device): One or more symbols and/or characters intended to provide information and located on a surface of a device. JESD22-B114A, 5/11

NOTE A mark can give information on such items as terminal location, country of origin, manufacturer, date code, lot number, and device identification, e.g., a part number.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

mask: A patterned screen of any of several materials and types used in shielding selected areas of a semiconductor, photosensitive layer, or substrate from radiation during processing, so that the unshielded areas can be further processed to reproduce the chosen pattern. JESD99C, 12/12

NOTE The type of mask can be designated either by type (e.g., oxide mask or metal mask) or by function (e.g., diffusion mask or vapor-deposition mask).

masked write transfer (MWT): A write transfer in which the transfer of new data from the serial register into the memory array is controlled by a write mask that is supplied on the DG(n) terminals. This mask allows the selective writing of new data into one or more of the data bit planes of the storage array corresponding to the data bits of the parallel array. In a normal implementation, a high M value enables the writing of new data while a low M inhibits the writing and leaves the existing data unchanged. A new mask value must be supplied for each masked write cycle. JESD21-C, 1/97

mask/mode (M): An indicator used in conjunction with other symbols to create a new pin name to signify that the pin function is either mask- or mode-related. JESD21-C, 1/97

mask-programmed read-only memory: A fixed-program read-only memory in which the data content of each cell is determined during manufacture by the use of a mask. (Ref. IEC 748-2.) JESD100-B, 12/99

mass storage: Nonvolatile auxiliary storage of large capacity used for storage of data to which infrequent reference need be made. JESD100-B, 12/99

master slice: An unmetalized wafer containing arrays of circuit elements as determined by subsystem requirements. JESD99C, 12/12

NOTE These circuit elements can be interconnected in a variety of ways to achieve different functions.

match (MA): An output signal that, when true, indicates that there has been a match (logic compare equal) between data stored in the memory and data presented on a set of input pins as defined in the individual device standard. JESD21-C, 1/97

matched pair (of microwave diodes): A pair of microwave diodes identical in outline dimensions and with matched electrical characteristics as described in EIA-370. JESD77D, 8/12

NOTE The two diodes may both be forward polarity, or one forward and one reverse polarity, or both reverse polarity.

material: The one or more substances of which something is made; e.g., an alloy is a material, which in turn is made up of a number of substances. JIG-101 Ed 2.0, 4/09

material category: Solder paste, lead/terminal finish, or terminal material/alloy of the solder balls used to make the second-level interconnect. J-STD-609A.01, 2/11

matte tin: A tin film with lower internal stresses than bright tin, grain sizes typically of 1 µm or greater, and a carbon content of less than 0.050%. JP002, 3/06

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

maverick product: Product that exhibits significant anomalous characteristics that may cause a higher-than-normal level of failure anywhere in the user's application or user's manufacturing line. JESD50B.01, 11/08

NOTE 1 In this definition, "product" includes the electronic component, the first level packing (e.g., tray, tube, and tape and reel), the shipping container, labeling, and paperwork.

NOTE 2 These significant anomalous characteristics can include initial quality defects, time-dependent reliability defects, defects that affect next level of manufacturing, defects in the product delivery process (such as labeling or shipping media), and defects in the business process (such as shipping information). The characteristics may or may not be part of an existing product or process monitor, test, or inspection activity.

NOTE 3 Maverick product may come from known noncompliant product, from compliant product that has a significant difference when compared to "typical" product (but is still within specification limits), or from "normal" product due to some previously unknown or unmonitored cause.

maximum component temperature: The temperature that a component should not exceed during assembly as measured on the top side of the component body. J-STD-609A.01, 2/11

maximum limit: (1) The higher-magnitude limit of a range of some quantity. JESD99C, 12/12

(2) For logic levels and temperatures only, the more positive (less negative) limit.

maximum linear transconductance ($g_{m(max)}$): The maximum slope of the I_D-V_{GS} curve in the linear region. JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

NOTE 1….The gate voltage is varied in increments no greater than 20 mV from below the turn-on voltage to a value great enough to ensure that the maximum slope point has been reached.

NOTE 2….The slope is calculated using a three-point linear least-squares best-fit algorithm as defined in ASTM F617-86.

maximum material condition (MMC): A feature of size that contains the maximum amount of material, e.g., maximum shaft diameter or minimum hole diameter. JESD95-1, 3/97

maximum on-state gate-source charge (Q_{gm}): The gate charge necessary to reach a specified maximum gate-source voltage. JESD24-2, 1/91

NOTE The magnitudes of gate charge and voltage are referred to the coordinate origin (0,0).

maximum operating junction temperature: The maximum-rated junction temperature at which the diode may operate. JESD90, 11/04
JESD211, 12/09

maximum operating (supply) voltage: The maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification. JESD22-A108D, 11/10#
JESD78D, 11/11
JESD89-2A, 10/07
JESD89-3A, 11/07

NOTE 1 "Maximum" refers to the magnitude of the supply voltage with the indicated polarity.

NOTE 2 The maximum operating voltage is not the absolute maximum-rated voltage, i.e., the voltage beyond which permanent damage is likely.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

maximum output current swing (I_{OM}): The peak positive or negative output current swing, referred to zero, that can be obtained without waveform clipping. JESD99C, 12/12

maximum output voltage swing (V_{OM}): The peak positive or negative output voltage swing, referred to zero, that can be obtained without waveform clipping. JESD99C, 12/12

maximum peak-to-peak output voltage swing ($V_{O(PP)}$): The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent dc output voltage is set at a specified reference level. JESD99C, 12/12

maximum rating: A rating that establishes either a limiting capability or a limiting condition beyond which damage to the device may occur. (Ref. IEC 747-1.) JESD77D, 8/12
JESD99C, 12/12

NOTE 1 A limiting condition may be either a maximum or a minimum.

NOTE 2 IEC 747-1 refers to such a limiting condition as a "rating (limiting value)".

maximum regulator [Zener] current (I_{ZM}): The dc reverse current through the diode when it is biased to operate in its breakdown region at a specified current based on the maximum-rated power. JESD211, 12/09

maximum regulator [Zener] voltage (V_{ZM}): The voltage across a diode at a specified current I_{ZM} in the breakdown region. JESD211, 12/09

maximum steady-state power dissipation: The maximum-rated value of continuous dc power dissipation. JESD211, 12/09

NOTE The maximum steady-state power dissipation is calculated by multiplying the rated maximum regulator [Zener] current by the maximum regulator [Zener] voltage.

maximum stress voltage (MSV): The maximum voltage allowed to be placed on any given terminal during latch-up immunity testing without causing catastrophic damage to the device due to electrical over-stress (EOS) not related to latch-up. JESD78D, 11/11

NOTE 1 MSV is higher than the maximum operating voltage.

NOTE 2 MSV is not the same as the absolute maximum voltage rating from the device data sheet. MSV applies to latch-up testing only, protecting the DUT from physical damage due to stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage for a terminal resulting in EOS damage. MSV may be different for each terminal and each polarity during testing, depending on process technology and circuit topology. Further, the MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should take into account the pulse width as well as process technology and circuit topology.

maximum use condition: The upper limit of an application use condition. JEP149, 11/04

maximum V_{supply}: See "maximum operating (supply) voltage".

MBB: See "moisture barrier bag".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

MBU: See "multiple-bit upset".

MCH: See "must connect high".

MCL: See "must connect low".

MCM: See "multichip module".

MCP: *See* "multi-chip package".

MCU: See "microcontroller" and "multiple-cell upset".

mean: The sum of the population values divided by the number of values in the population. A measure of location (central tendency) equal to the center of gravity of the population. EIA-557-B, 2/06

mean operating junction temperature during life test: The mean value of the individual average junction temperatures, $T_{J(AV)}$, of a sample of semiconductor devices when the devices are operated under specified life-test conditions. RS-323, 3/66

mean partial power loss: The mean value of the instantaneous power loss in a particular period of the cycle, averaged over the full cycle. JESD77D, 8/12

NOTE The term "power dissipation" has been used in the past as a true synonym for "power loss". This is no longer recommended. The term "loss" should refer to the electrical loss (*IR* drop) at the place of its origin, and the term "dissipation" should refer to the heat that is dissipated from the surface of the device into the environment. Different terms must be provided for the two quantities because, due to internal storage of heat, the two differ with time.

As an exception, "mean power dissipation" may still be used as a synonym for "mean power loss", but only when appropriate, i.e., if the differences with time have no influence on the mean values of the two. This is the case for mean values that are averaged over a cycle. In the latter case, the subscript "(AV)" is usually omitted from the letter symbols.

mean time between failures (MTBF): The average time between failures in repairable or redundant systems. JEP122G, 10/11
JEP143C, 7/12

mean time to failure (MTTF): The average time to failure for components or nonrepairable systems. JEP122G, 10/11
JEP143C, 7/12

NOTE….The MTTF is often the reciprocal of the hazard rate when the hazard rate is described by the Poisson or equivalent exponential function, e.g., in the constant or flat portion of the useful life region of the bathtub curve.

measured leak rate: The leak rate of a given package as measured under specified conditions and employing a specified test medium. Measured leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm-cm^3/s). JESD22-A109-A, 7/01

measurement current: The current applied to a device under test for the measurement of some parameter. JESD51-1, 12/95#
JESD51-13, 6/09#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

measurement delay time: The length of the time interval from removal of some applied condition to the start of the measurement sample window. JESD51-1, 12/95# JESD51-13, 6/09#

mechanical index (on a package): A mark, chamfer, notch, tab, flat, or similar feature that allows mechanical, optical, electrical, or pneumatic sensing during mechanized handling. It may or may not identify the number-one terminal position. RS-308-A, 8/81 Rescinded 5/09

median: The middle value in a group of measurements when arranged from lowest to highest. When the number of measurements is an even number, the average of the two middle values is used as the median. A measure of location. EIA-557-B, 2/06

mega (M) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1 048 576 (2^{20} or K^2, where K = 1024). JESD21-C, 1/97 JESD100-B, 12/99

NOTE 1 Contrast with the SI prefix mega (M) equal to 10^6, as in a 1-Mb/s data transfer rate, which is equal to 1 000 000 bits per second.

NOTE 2 The definitions of kilo, giga, and mega based on powers of two are included only to reflect common usage. IEEE/ASTM SI 10-1997 states "This practice frequently leads to confusion and is deprecated." Further confusion results from the popular use of a "megabyte" consisting of 1 024 000 bytes to define the capacity of the familiar "1.44-MB" diskette. An alternative system is found in Amendment 2 to IEC 60027-2: *Letter symbols to be used in electrical technology – Part 2:*

Prefixes for binary multipliers

Factor	Name	Symbol	Origin	Derivation
2^{10}	kibi	Ki	kilo + binary: $(2^{10})^1 = 1\ 024$	kilo: $(10^3)^1$
2^{20}	mebi	Mi	mega + binary: $(2^{10})^2 = 1\ 048\ 576$	mega: $(10^3)^2$
2^{30}	gibi	Gi	giga + binary: $(2^{10})^3 = 1\ 073\ 741\ 824$	giga: $(10^3)^3$
2^{40}	tebi	Ti	tera + binary: $(2^{10})^4 = 1\ 099\ 511\ 627\ 776$	tera: $(10^3)^4$

IEC suggests that, in English, the first syllable of the name of the binary-multiplier prefix should be pronounced in the same way as the first syllable of the name of the corresponding SI prefix and that the second syllable should be pronounced as "bee".

MSL: See "moisture sensitivity level".

memory cell: The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved. (Ref. IEC 748-2.) JESD100-B, 12/99

memory integrated circuit: An integrated circuit consisting of memory cells and usually including associated circuits such as those for signal amplification and address selection. (Ref. IEC 748-2.) JESD100-B, 12/99

memory location: A subdivision of a memory, including one or several memory cells, that is the smallest part of the memory that can be addressed. JESD100-B, 12/99

NOTE The content of a memory location is usually called a bit, a byte, or a word, as appropriate.

memory organization: The arrangement of memory cells, either by geometrical arrangement in rows and columns or by organization of the data to be stored. (Ref. IEEE Std 641.) JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

meniscus: The region of insulator that wicks/wets up the lead above the average low point of the seal at the lead and package (on both sides of the seal) at the lead and/or package interface. JESD9B, 5/11

MESFET: See "metal-semiconductor field-effect transistor".

MET: See "manufacturer's exposure time".

metal-insulator-semiconductor (MIS) technology: A technology for producing circuits and circuit elements having the form of a semiconductor-insulator-metal layered structure. JESD99C, 12/12

NOTE Field-effect transistors, capacitors, varactors, nonlinear resistors, variable-threshold diodes, and similar circuit elements can be produced with this technology.

metallization: A thin-film metallic conductor or network of such conductors used to interconnect microcircuit elements. JESD33B, 2/04#
JESD99C, 12/12

metallization, bottom: The metallization on the bottom surface of a chip that permits bonding it to a mounting substrate. JESD99C, 12/12

metallization, multilayer: A metallization pattern in which the conductive network is fabricated in more than one plane and separated, except at desired contact points, by thin dielectric films. JESD99C, 12/12

metal-nitride-oxide-semiconductor (MNOS) technology: A subcategory of metal-insulator-semiconductor (MIS) technology in which the insulation employed is a nitride-oxide layer. JESD99C, 12/12

metal-oxide-semiconductor field-effect transistor (MOSFET): An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material and the gate is metal or another highly conductive material. (Ref. IEC 747-8.) JESD24, 7/85
JESD28-A, 12/01
JESD60A, 9/04
JESD77D, 8/12
JESD90, 11/04

metal-oxide-semiconductor (MOS) technology: A subcategory of metal-insulator-semiconductor (MIS) technology in which the insulator employed is an oxide of the semiconductor substrate material. JESD99C, 12/12

NOTE The term MOS is often misused to include other categories of insulated-gate technology such as MNOS (metal-nitride-oxide-semiconductor) and SIS (silicon-gate-insulator semiconductor).

metal-oxide varistor (MOV): A varistor having a sintered metal-oxide element. JESD77D, 8/12

NOTE The device exhibits a symmetrical voltage-current characteristic.

metal-semiconductor field-effect transistor (MESFET): A field-effect transistor in which a metal-semiconductor rectifying contact is used for the gate electrode. JESD77D, 8/12

NOTE 1 Typically the structure is fabricated in gallium arsenide and the term GaAs MESFET may be used.

NOTE 2 Both depletion-type and enhancement-type devices have been manufactured. The acronyms are D-MESFET and E-MESFET, respectively.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
metric: (1) A standard of measurement.	EIA-599-A, 6/98
(2) A quantitative measure of an activity, results, and/or reaction.	JEP146A, 1/09
(3) Of, relating to, or using the metric system.	Merriam-Webster's Collegiate Dict.
MFR code: A code assigned by JEDEC that identifies manufacturers. JEP-106 is the publication containing the codes.	JESD32, 6/96
microcircuit: A microelectronic device that has a high circuit-element and/or component density and that is considered to be a single unit. (Ref. IEC 748-1.) (See also "integrated circuit".)	JESD99C, 12/12
microcircuit, analog: Synonym for "integrated circuit, analog".	JESD99C, 12/12
microcircuit, binary: Synonym for "integrated circuit, binary".	JESD99C, 12/12
microcircuit, digital: Synonym for "integrated circuit, digital".	JESD99C, 12/12
microcircuit, film: Synonym for "integrated circuit, film".	JESD99C, 12/12
microcircuit, hybrid: Synonym for "integrated circuit, hybrid".	JESD99C, 12/12
microcircuit, interface: Synonym for "integrated circuit, interface".	JESD99C, 12/12
microcircuit, linear: Synonym for "integrated circuit, linear".	JESD99C, 12/12
microcircuit, logic: Synonym for "integrated circuit, digital".	JESD99C, 12/12
microcircuit module: An assembly of microcircuits, or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions and so constructed that, for the purpose of specification, testing, commerce, and maintenance, it is considered to be indivisible.	JESD99C, 12/12
microcircuit, multichip: Synonym for "integrated circuit, multichip".	JESD99C, 12/12
microcomputer (µC): A computer system whose central processing unit (CPU) is a microprocessor.	JESD100-B, 12/99
NOTE A basic microcomputer includes a microprocessor, memory, and input/output ports; these may or may not be on the same chip. See also "microcontroller".	
microcontroller (MCU): A microcomputer on a single chip.	JESD100-B, 12/99
NOTE A microcontroller is generally dedicated to a single task defined by a fixed program in internal ROM.	

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

microelectronic assembly: An assembly of unpackaged (uncased) microcircuits and/or packaged microcircuits so constructed on a packaging interconnect structure that it is considered to be an indivisible component for the purpose of specification, testing, commerce, and maintenance. JESD30E, 8/08 JESD99C, 12/12

NOTE….The assembly may also include discrete devices. These and the microelectronic devices may be mounted on either one or two sides of the packaging interconnect structure, and the external terminals usually exit from one side of the assembly. Various package sizes, shapes, and external terminal forms may be used.

microelectronics: That field of science and engineering that deals with highly miniaturized electronic components and their use. (Ref. IEC 748-1.) JESD99C, 12/12

microprocessing unit (MPU): The name sometimes used for the central processing unit (CPU) of a microcomputer. JESD100-B, 12/99

microprocessor (integrated circuit) (µP): An integrated circuit capable of all of the following: JESD100-B, 12/99

a) operating on coded instructions;

b) carrying out, in accordance with the instructions:

1) the acceptance of coded data for processing and/or storage,
2) arithmetic and logical operations on the input data together with any relevant data stored in the internal registers of the microprocessor integrated circuit and/or in external memories, and
3) the delivery of coded data; and

c) accepting and/or delivering signals controlling and/or describing the operation or state of the microprocessor integrated circuit. (Ref. IEC 748-2.)

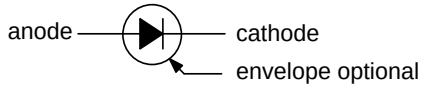
NOTE The instructions may be fed in, built in, or held in an internal memory.

microprogrammable computer: A computer in which the microprogram (microinstructions) in the read-only memory (ROM) used for instruction decoding can be changed, thus changing the computer's instruction set. JESD100-B, 12/99

microstrain value: A dimensionless quantification of strain expressed as 10^6 times the change in length divided by the original length. JESD22-B113A, 9/12

microwave diode: A two-terminal device that is responsive in the microwave region of the electromagnetic spectrum, commonly regarded as extending from 1 GHz to 300 GHz. JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

midstep value (of an analog-to-digital converter): The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values. JESD99C, 12/12

NOTE For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width.

midstep value, nominal (of an analog-to-digital converter): A specified analog value within a step that is ideally represented free of error by the corresponding digital output code. JESD99C, 12/12

military product: Any product that is offered to customers by the manufacturer for use in US military and similar types of system applications (e.g., QPL, QML, MIL-STD-883, standard microcircuit drawings, specification or source control drawings, selected or altered item drawings). JESD31D, 9/10

Miller charge: Synonym for "gate-drain charge".

minicycle: A temperature cycle in an application resulting from a small change in the operational temperatures (e.g., due to PC program variations). JESD94A, 7/08

minimization: The process of eliminating redundancy in logic implementation. JESD12-1B, 8/93
JESD99C, 12/12

minimum limit: (1) The lower-magnitude limit of a range of some quantity. JESD99C, 12/12

(2) For logic levels and temperatures only, the less positive (more negative) limit.

minimum operating (supply) voltage: The minimum supply voltage at which a device is specified to operate in compliance with the applicable device specification. JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

NOTE "Minimum" refers to the magnitude of the supply voltage with the indicated polarity.

minority carrier: The type of carrier constituting less than half of the total charge-carrier concentration. JESD77D, 8/12

MIS: See "metal-insulator-semiconductor technology".

missing code (of an analog-to-digital converter): An intermediate code that is absent when the changing analog input to an analog-to-digital converter causes a multiple code change in the digital output. JESD99C, 12/12

mixer diode: A diode, often associated with microwave circuits, that combines rf signals at two frequencies to generate an rf signal at a third frequency. JESD77D, 8/12

MMC: See "maximum material condition".

M(n): See "mode select".

MNOS: See "metal-nitride-oxide-semiconductor technology".

mode: The most frequently occurring value in a group of measurements. A measure of location. EIA-557-B, 2/06

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

mode control (M): A control input that implements special functions. It may be a dc or active input signal but is always intended to be tied to a logic high level or not connected by the user unless otherwise specified. JESD21-C, 1/97

model: A representation of an electronic circuit. JESD12-1B, 8/93 JESD99C, 12/12

modeling: A methodology that attempts to describe characteristics of a process or some aspect of a process. Once a satisfactory model is chosen, predictions about future output of the process can be made. Process variability, or error, is included to assess how well the model fits the true process and to bound future process predictions. JEP132, 7/98

mode select [M(n)]: Input signals that, when true, select an alternative mode of operation for the device. The alternative modes available must be defined in the applicable device standard. JESD21-C, 1/97

MODFET: See "modulation-doped field-effect transistor".

modulation-doped field-effect transistor (MODFET): A metal-semiconductor field-effect transistor in which a doped material forms a heterojunction with an undoped channel; the doped material supplies electrons to the undoped channel whose high electron mobility results in enhanced channel conductance. JESD77D, 8/12

NOTE 1 Typically an aluminum gallium arsenide layer is grown on an undoped gallium arsenide layer by an epitaxial growth technique.

NOTE 2 Other popularly used acronyms for this device are HEMT for high-electron-mobility transistor, SDHT for selectively doped heterostructure transistor, and TEGFET for two-dimensional electron-gas field-effect transistor.

module generator: A tool that, when given a high-level description of a desired function and relevant parameters, produces a specified implementation (for example, behavioral, structural, or geometric description, etc.) of the function to be used within an integrated circuit design. JESD12-1B, 8/93 JESD99C, 12/12

NOTE Some functions commonly produced by module generators are RAM, ROM, ALU, and datapath.

moisture-barrier bag (MBB): A bag designed to restrict the transmission of water vapor and used to pack moisture-sensitive devices. J-STD-033C, 2/12

moisture/reflow sensitivity classification: The characterization of a device's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. J-STD-020D.1, 3/08

moisture-sensitive device (MSD): Any device that exhibits moisture absorption or moisture retention and whose quality or reliability is affected by moisture. JEP160, 11/11

moisture-sensitive identification (MSID) A symbol indicating that the contents are moisture-sensitive. J-STD-033C, 2/12

moisture sensitivity level (MSL): A rating indicating a device's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. J-STD-020D.1, 3/08

monitoring: Using a program for observing, and often controlling, a device or equipment. JEP153,1/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

monolithic microcircuit: Synonym for “integrated circuit, single-chip”.

monotonicity (of an analog-to-digital converter [a digital-to-analog converter]): A property of the transfer function that ensures the consistent increase or decrease of the digital [analog] output in response to a consistent increase or decrease of the analog [digital] input. JESD99C, 12/12

NOTE An intermediate increment with the value of zero does not invalidate monotonicity.

morphology, integrated: The structural characterization of an electronic component in which the current- or signal-modifying areas, patterns, or volumes have lost their identities in the integration of electronic materials, in contrast to an assembly of devices performing the same function. JESD99C, 12/12

morphology, translational: The structural characterization of an electronic component in which the areas or patterns of resistive, conductive, dielectric, and active materials in or on the surface of the structure can be identified in a one-to-one correspondence with devices assembled to perform an equivalent function. JESD99C, 12/12

mortality function: Synonym for “probability density function of the time-to-failure”.

MOS: See “metal-oxide-semiconductor technology”.

MOSFET: See “metal-oxide-semiconductor field-effect transistor”.

mounting surface: The external region of the package on which the package will be mounted to the end-application PCB, heat sink, etc. JESD9B, 5/11

NOTE The mounting surface is typically on the external, opposite side of the package cavity die attach or substrate attach area.

EDITOR’S NOTE JESD9B “Terms and Definitions” incorrectly lists “mounting surface” and “seating plane” as synonyms but uses the terms elsewhere within the document with different meanings.

MOV: See “metal-oxide varistor”.

MPDRAM: See “multiport DRAM”.

MPM: See “multiport memory”.

MPRAM: See “multiport RAM”.

MPU: See “microprocessing unit”.

MSD: See “moisture sensitive device”.

MSI: Medium-scale integration. JESD99C, 12/12

MSID: See “moisture sensitive identification”.

MSL: See “rated moisture sensitivity level”.

MSV: See “maximum stress voltage”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

MT1: See “main terminal 1”.

MT2: See “main terminal 2”.

MTBF: See “mean time between failures”.

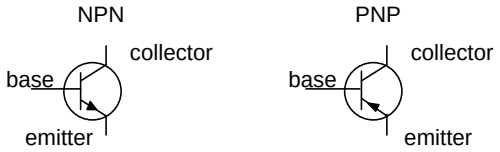
MTTF: See “mean time to failure”.

multichip module (MCM): A multichip integrated circuit or hybrid microcircuit that contains two or more microcircuits. JESD93, 9/05

multi-chip package (MCP): A package containing more than one heat source. JESD51-31, 7/08

multijunction transistor: A transistor having a base and two or more junctions. JESD77D, 8/12

Graphic symbols for triode transistors (ref. IEEE Std 315):



NOTE In the graphic symbols, the envelope is optional if no element is shown connected to the envelope.

multilayer(-connection) film circuit: A circuit having more than one layer of film interconnections separated by at least one insulating film or gap. JESD99C, 12/12

multiple-bit upset (MBU): Two or more single-event-induced bit errors occurring in the same nibble, byte, or word. JEP133C, 1/10
JESD89A, 10/06
JESD891A, 10/07
JESD892A, 10/07
JESD893A, 11/07

NOTE An MBU cannot be corrected by a simple ECC (such as single-bit error correction).

multiple-cell upset (MCU): A single event that induces several bits in an IC to fail at the same time. JESD89A, 10/06#
JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

NOTE The error bits are usually, but not always, physically adjacent.

multiplexed (MX): A term describing a device that has pins used for different purposes at different times as a function of one or more of its control inputs. The signal groups that are multiplexed onto a common pin set are given together, as in AA MX signifying address multiplexed with address or ADQ MX signifying address multiplexed with data in and data out. JESD21-C, 1/97

multiplying DAC: A digital-to-analog converter having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

multiport DRAM (MPDRAM): A dynamic RAM that contains, in addition to the conventional random-access data and address port, a serial-access port that allows serial access to a portion of the stored data in a way that is independent of the normal RAM data terminals and in which simultaneous serial and random operations may be executed. This type of memory has been referred to as "Video RAM" because of its primary field of application. JESD21-C, 1/97

multiport memory (MPM): Any memory array that has two or more data ports that do not have the same architecture. The most common form of MPM is one in which there is a random-access port and a serial-access port. JESD21-C, 1/97

multiport RAM (MPRAM): A RAM that has two or more ports for data, address, and control, that are not identical in nature. Normally at least one port provides parallel access while one other provides serial access. (See also "synchronous MPDRAM (SMPDRAM)".) JESD21-C, 1/97

must connect high (MCH): A pin that must be connected to a voltage that is interpreted as a logic high or "true" signal. JESD21-C, 1/97

must connect low (MCL): A pin that must be connected to a voltage that is interpreted as a logic low or "false" signal. JESD21-C, 1/97

MWT: See "masked write transfer".

MX: See "multiplexed".

N

native film (on a wafer or die): An incidental film or a film, stipulated by design, that was created by specified processing. JESD22-B118, 3/11

NOTE The film may be spotty or exhibit rainbow coloration or other differences in color shading and may cover localized areas or a large area.

native stain (on a wafer or die): A visual anomaly consisting of an incidental stain that was created by specified processing. JESD22-B118, 3/11

NOTE The stain may be spotty or exhibit rainbow coloration or other differences in color shading and may cover localized areas or a large area.

natural-air-cooled environment: An environment of a semiconductor device in which the power loss in the device is dissipated by means of air currents whose velocity is less than 120 feet per minute, by radiation losses from the surface of the device, and by an unspecified amount of conduction losses through the leads to the electrical connections. RS-323, 3/66

NBTI: Negative bias temperature instability. JESD90, 11/04

NC: See "no (internal) connection (pin)".

n-channel charge-coupled device: A charge-coupled device fabricated so that the charges stored in the potential wells are electrons. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

n-channel field-effect transistor: A field-effect transistor that has an n-type conduction channel. (Ref. IEC 747-8.) JESD24, 7/85 JESD77D, 8/12

negative-breakdown-resistance thyristor surge protective device: A thyristor surge suppressor whose static characteristic has a negative-resistance slope between the breakover point and a higher-current, lower-voltage point at which switching occurs. JESD77D, 8/12

negative differential-resistance region: Any portion of the characteristic within which the differential resistance is negative. JESD77D, 8/12

negative-going input threshold voltage (V_{IT-}): The input threshold voltage when the input voltage is falling. JESD99C, 12/12

negative logic: The representation of the logic 1-state and the logic 0-state by the low and high levels, respectively. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

net (of a circuit): A unique interconnection of specific circuit elements. JESD12-1B, 8/93 JESD99C, 12/12

NOTE The primary inputs and primary outputs are considered to be circuit elements.

netlist: A list of all nets of a circuit. JESD12-1B, 8/93 JESD99C, 12/12

netlist translation: The conversion of a netlist from one format to another. JESD12-1B, 8/93 JESD99C, 12/12

next-level assembly: The attachment of a die or packaged device to the next level of assembly packaging. JEP160, 11/11

NF: See “no function”.

nibble: A binary character string operated upon as a unit and shorter than a byte. JESD100-B, 12/99

NOTE A nibble is usually four bits.

nibble-wide device: A device that has a parallel four-bit data interface. JESD21-C, 1/97 JESD100-B, 12/99#

NOTE For memory devices, this term should not be confused with “nibble mode”, which refers to a serial-data-access mode.

nick: A small notch, groove, chip, dent, etc., in a surface, typically due to mechanical damage. JESD9B, 5/11

no connect terminal; no connect pin: A package interconnect terminal (pin, bump, or ball) that is not electrically connected to a die. JS-001-2012, 4/12

NOTE 1 In practice there are some terminals that are labeled as “no connect” but that are actually connected to the die and, therefore, should not have been classified as “no connect terminals”. Connection to such a terminal could cause the device to malfunction in all or some data sheet operating modes or conditions.

NOTE 2 See also “no (internal) connection (pin) (NC)”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
node: (1) A definable point in the process at which form, fit, or function of the product or service is altered.	EIA-557-B, 2/06 JEP131B, 4/12 JESD659B, 2/07
(2) The end-point of a branch in a network or a point at which two or more branches meet.	JESD12-5, 8/88
(3) Within a circuit, a point of interconnection between two or more components.	JEP155A.01, 3/12
no function (NF): An input that is electrically connected to the device but for which the signal has no function in the device operation.	JESD21-C, 1/97
no (internal) connection (pin) (NC): A terminal that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of the wiring) does not exceed the highest supply voltage rating of the circuit. NOTE 1 If higher voltages are acceptable, this should be stated. NOTE 2 The IEC equivalent term is "blank terminal"; nevertheless, the IEC abbreviation is "NC".	JESD21-C, 1/97# JESD77D, 8/12 JESD78D, 11/11# JESD99C, 12/12
noise current, equivalent input (of a two-port device) (I_n): The current of an ideal current source (i.e., one having infinite internal impedance) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source. NOTE In the definition, the equivalent input noise voltage, which would be needed for a complete and precise description of the device noise, is neglected. If the external source impedance is infinite, the noise current represents the total noise.	JESD77D, 8/12 JESD311A, 11/81
noise equivalent signal (of a charge-transfer device): The rms input signal or illumination power level needed to increase the output power to twice the value obtained with no input signal or illumination.	JESD99C, 12/12
noise margin: The maximum voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to deviate from the allowable logic voltage level. NOTE The term "input", as used here, refers to logic input terminals, power supply terminals, or ground reference terminals.	JESD99C, 12/12 RS-390-A, 2/81
noise temperature (T_n): The uniform physical absolute temperature at which a network (and all its sources, if it is a multiport network) would have to be maintained if it (and its sources) were passive, in order to make available (or deliver) the same random noise power per unit bandwidth (spectral density) at a given frequency that is actually available (or delivered) from the network. (Ref. IEC 747-1.)	JESD77D, 8/12 JESD99C, 12/12 JESD311A, 11/81

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

noise voltage, equivalent input (of a two-port device) (V_n): The voltage of an ideal voltage source (i.e., one having zero internal impedance) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source. JESD77D, 8/12 JESD311A, 11/81

NOTE In the definition, the equivalent input noise current, which would be needed for a complete and precise description of the device noise, is neglected. If the external source impedance is zero, the noise voltage represents the total noise.

nominal bulk supply voltage (V_{BB}): The nominal bulk voltage for a given technology. JESD28-A, 12/01 JESD60A, 9/04 JESD90, 11/04

nominal I_{supply} (I_{nom}): The measured dc supply current for each V_{supply} pin (or pin group) with the device under test biased at the test temperature as defined in JESD78D. JESD78D, 11/11

nominal power supply voltage (V_{DD}): The nominal (drain) supply voltage for a given technology. JESD28-A, 12/01 JESD60A, 9/04 JESD90, 11/04

NOTE….V_{DD} is positive for both n-channel and p-channel MOSFETs.

noncompliant product: Product that fails to comply with one or more user requirements, manufacturer's specifications, or statistical process control levels that the supplier has deemed critical to reliability. JESD50B.01, 11/08

nonconducting region: The portion of the voltage-current characteristic of a reverse-biased p-n junction that exhibits a high resistance to the passage of current. JESD211, 12/09

nonconformance: A component characteristic that does not conform to a specified criterion. JESD16-A, 4/95

nonconforming: Not conforming to specification(s), procedures, or requirements. EIA-557-B, 2/06

nonconforming unit: A unit that does not conform to a specification. EIA-557-B, 2/06

NOTE See also "discrepant material".

nonconformity: (1) A single component that has one or more nonconformances. JESD16-A, 4/95

(2) A specific occurrence of a condition that does not conform to specification. EIA-557-B, 2/06 JESD659B, 2/07

NOTE 1….Such an occurrence is sometimes called a discrepancy.

NOTE 2….See also "nonconformance".

noncritical area (of a wafer or die): An area of a wafer or die (typically at the edge) for which the inspection criteria are less stringent. JESD22-B118, 3/11

nondestructive test: A test that evaluates a device feature without degrading the device function or strength although the appearance may be altered. RS-308-A, 8/81 Rescinded 5/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

nonlinear ADC [DAC]: An analog-to-digital converter [A digital-to-analog converter] with a specified nonlinear transfer function between the nominal midstep [step] values and the corresponding step widths [heights]. JESD99C, 12/12

NOTE The function may be continuously nonlinear or piecewise linear.

nonoperating lifetime: The cumulative length of time that a component is not operating in an application. JESD94A, 7/08

NOTE….The nonoperating lifetime may be calculated by subtracting the power-on hours (POH) from the field lifetime.

nonrepetitive peak reverse surge current (I_{ZSM}): The peak reverse current in the breakdown region including all nonrepetitive transient currents but excluding all repetitive transient currents. JESD211, 12/09

nonrepetitive peak reverse voltage (V_{RSM}): The peak reverse voltage including all nonrepetitive transient voltages but excluding all repetitive voltages. JESD77D, 8/12
JESD282-B, 4/00

non-supply terminal; non-supply pin: A terminal that is not categorized as a supply terminal or a no connect. JS-001-2012, 4/12

NOTE Non-supply terminals include terminals such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref terminals, and VPP terminals on EPROM memories. Most non-supply terminals transmit or receive information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

nonusable terminal; not usable (terminal) (NU): A terminal that is not to be used in normal applications and that may or may not have an internal connection. JESD21-C, 1/97#
JESD77D, 8/12
JESD99C, 12/12

nonvolatile enable (NE): On an NVRAM, the input that enables the nonvolatile functions ST and RC as determined by the states of chip select, chip enable, output enable, and write enable. JESD21-C, 1/97

nonvolatile memory (NVM): A memory in which the data content is retained when power is no longer supplied to it. JESD100-B, 12/99
JESD218A, 2/11

nonvolatile random-access memory (NVRAM): An SRAM in which provisions exist on chip for the state of the cells to be saved when power is removed. JESD21-C, 1/97

nonwet solder bump: A solder bump that does not bond to the substrate pad metallization during the solder reflow process. JESD22-B109A, 1/09

NOTE A nonwet solder bump is detected as an area on the substrate pad where, after tensile pull, the substrate pad metallization displays the original color and texture with no evidence of solder fusion. Depopulated areas, where no solder joint formation is expected, are excluded.

nonwetting, solder: The partial adherence of molten solder to a surface that it has contacted while leaving some basis metal exposed. (Ref. IPC-T-50.) J-STD-002B, 2/03

no pin (NP): A pin position on a package where the pin has been purposely left blank or removed after assembly. No physical pin is allowed in this position. JESD21-C, 1/97

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Terms, abbreviations, letter symbols, and definitions **References**

normal distribution: A continuous, symmetrical, bell-shaped frequency distribution for variables data. EIA-557-B, 2/06

NOTE When measurements have a normal distribution, about 68.26% of all individuals lie within plus or minus one standard deviation unit of the mean; about 95.44% lie within plus or minus two standard deviation units of the mean; and about 99.73% of all individuals lie within plus or minus three standard deviation units of the mean.

not usable (terminal): Synonym for "nonusable terminal". JESD21-C, 1/97#

NOVRAM: Acronym for "nonvolatile random-access memory". See also "NVRAM". JESD100-B, 12/99

NP: See "no pin".

n-type semiconductor: An extrinsic semiconductor in which the conduction-electron density exceeds the mobile-hole density. (Ref. IEC 747-1.) JESD77D, 8/12

NU: See "nonusable terminal".

NVM: See "nonvolatile memory".

NVRAM: Abbreviation for "nonvolatile random-access memory". See also "NOVRAM". JESD100-B, 12/99

n-well-to-source voltage: The voltage between the n-well and the source. JESD90, 11/04

NOTE….The n-well is the bulk of a P-MOSFET.

O

objective evidence: Information that can be verified, based on factors obtained through observation, measurement, test, or other means. EIA-599-A, 6/98

observability: The ability to determine the logic state(s) of a node at the circuit's externally accessible node(s). JESD12-5, 8/88

observed failure rate (λ_o): The failure rate determined from a product or test vehicle subjected to an accelerating stress that may produce failures attributable to one or more failure mechanisms. JEP122G, 10/11
JEP143C, 7/12

octave: The interval between two frequencies that have a ratio of 2 to 1. JESD22-B103B, 6/02#

NOTE….The number of octaves, N, between two frequencies, f1 and f2, is given by N = |log (f2/f1)| / log 2.

OE(n): See "output enable".

off impedance (of a thyristor): The small-signal impedance between the terminals through which the principal current flows when the thyristor is in the off state. (Ref. EIA-397.) JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

offset error (of a linear analog-to-digital converter [digital-to-analog converter]) (E_O): The difference between the actual midstep [step] value and the nominal midstep [step] value at the offset point. — JESD99C, 12/12

NOTE See notes 1, 2, and 3 under "gain error".

offset point (of an adjustable analog-to-digital converter [digital-to-analog converter]): The point in the transfer diagram corresponding to the midstep [step] value of the step about which the transfer diagram rotates when the gain is adjusted. — JESD99C, 12/12

NOTE Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer curve.

off-state current (I_{off}): The current into a circuit node when the device or a portion of the device affecting that circuit node is in the off state. — JESD99C, 12/12

NOTE When additional subscripts are used, the off-state current is identified by "off" in parentheses following the additional subscripts, e.g., $I_{O(off)}$ for off-state output current.

off state (1) **(of a thyristor):** The state of a thyristor, in a quadrant in which switching can occur, that corresponds to the portion of the characteristic between the origin and the breakover point. — JESD77D, 8/12

(2) (**of a thyristor surge protective device):** The state of a thyristor surge protective device, in a quadrant in which switching can occur, that corresponds to the high dynamic-resistance portion of the characteristic between the origin and the beginning of the breakdown region. — JESD77D, 8/12

ohmic region: The region of the drain voltage-current characteristic curve in which a change in drain-source voltage causes a proportional change in drain current. — JESD24, 7/85 JESD77D, 8/12

1-state: The logic state represented by the binary number 1 and usually standing for an active or true logic condition. (Ref. ANSI/IEEE Std 91.) — JESD99C, 12/12

ongoing process analysis (OPA): The application of signature analysis to an unknown (assumed to be infinite) population of failures collected over time from multiple lots, events, or labs. — JEP136, 7/99

on impedance (of a thyristor): The small-signal impedance between the terminals through which the principal current flows when the thyristor is in the on state. (Ref. EIA-397.) — JESD77D, 8/12

on-state drain current ($I_{D(on)}$): The direct current into the drain terminal with a specified forward gate-source voltage applied to bias the device to the on-state. — JESD24, 7/85

on-state gate-source charge ($Q_{g(on)}$): The gate charge necessary to reach a gate-source voltage that will support a minimum specified on-state drain current. — JESD24-2, 1/91

on state (of a thyristor): The state of a thyristor, in a quadrant in which switching can occur, that corresponds to the low-resistance, low-voltage portion of the characteristic. — JESD77D, 8/12

on-state resistance (r_{on}): The resistance between specified terminals with input conditions applied that, according to the product specification, will establish minimum resistance (the on-state) between those terminals. — JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

OP: See "optional".

open circuit: A circuit having a terminating impedance sufficiently high that halving its magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. JESD10, 1/76 JESD24, 7/85 JESD77D, 8/12

open-circuit fault: In a circuit, a fault that alters the number of nodes by breaking a node into two or more nodes. JESD12-5, 8/88

open-circuit input capacitance (C_{ibo}): The capacitance measured across the input terminals (emitter and base) with the collector open-circuited for ac. (Ref. IEEE Std 255.) JESD10, 1/76

open-circuit output capacitance (C_{obo}): The capacitance measured across the output terminals (collector and base) with the input open-circuited to ac. (Ref. IEEE Std 255.) JESD10, 1/76

open-circuit output (of an integrated circuit): A unipolar output whose only connection within the integrated circuit is through an active device, usually a transistor, to one of the supply voltages. JESD99C, 12/12

NOTE 1 For the purpose of this definition, the presence of any parasitic components and freewheeling, flyback, and clamp diode is ignored.

NOTE 2 When the active device is in its on state, the output voltage approaches the voltage of the supply to which it is connected (through the active device); when the device is in its off state, the output impedance to any other terminal of the integrated circuit is high and the output voltage is determined by the external circuit to which the output is connected.

NOTE 3 Outputs of this generic class are usually classified according to the name of the element of the active device to which they are connected within the integrated circuit, e.g., open-collector output, open-drain output, etc.

NOTE 4 For graphic symbols, see "sink driver" and "source driver".

open-circuit voltage [floating potential], emitter-base ($V_{EB(fl)}$): The dc open-circuit voltage (floating potential) between the emitter terminal and the base terminal when the collector terminal is biased in the reverse direction with respect to the base terminal. (Ref. IEEE Std 255.) JESD10, 1/76

open-collector output: An open-circuit output whose internal connection is to the collector of a bipolar transistor. JESD99C, 12/12

NOTE For graphic symbols, see "sink driver" (for npn) or "source driver" (for pnp).

open-drain output: An open-circuit output whose internal connection is to the drain of a field-effect transistor. JESD99C, 12/12

NOTE For graphic symbols, see "sink driver" (for n-channel outputs) or "source driver" (for p-channel outputs).

open-drain output buffer: An output buffer that has one low-impedance output logic level and a high-impedance output state. JESD12-4, 4/87

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Terms, abbreviations, letter symbols, and definitions **References**

open-element output (of an integrated circuit): Synonym for "open-circuit output (of an integrated circuit)". JESD99C, 12/12

open-emitter output: An open-circuit output whose internal connection is to the emitter of a bipolar transistor. JESD99C, 12/12

NOTE For graphic symbols, see "source driver" (for npn) or "sink driver" (for pnp).

open-source output: An open-circuit output whose internal connection is to the source of a field-effect transistor. JESD99C, 12/12

NOTE For graphic symbols, see "source driver" (for p-channel outputs) or "sink driver" (for n-channel outputs).

open-surface bubble: Synonym for "bubble, surface".

operating lifetime: The cumulative length of time that a component is expected to function in an application at or below the predicted failure rate, stated in power-on hours (POH). JESD94A, 7/08

operating temperature cycle range: The temperature range of a component caused by power cycling. JESD94A, 7/08

optical axis: A line about which the radiant-energy or sensitivity pattern is centered. (Ref. IEC 747-5.) JESD77D, 8/12

NOTE 1 The radiant-energy or sensitivity pattern may be nonsymmetrical.

NOTE 2 The optical axis may deviate from the mechanical axis.

optimization (of a process): The methodology of making a process as efficient as possible. JEP132, 7/98

optimization (of logic): The process by which a given logic representation is reduced to a superior equivalent functional representation with respect to some system or chip-level design objective such as speed, device utilization, level of logic, etc. JESD12-1B, 8/93
JESD99C, 12/12

optional (OP): The designation for pins for which the manufacturer has the freedom to supply a specialized function not previously defined in the standard without affecting compliance with the standard. JESD21-C, 1/97

optocoupler; photocoupler; optoisolator: An optoelectronic device designed for the transformation of electrical signals by utilizing optical radiant energy to provide coupling with electrical isolation between the input and the output. (Ref. IEC 747-5.) JESD77D, 8/12

optoelectronic device: (1) A device that is responsive to or that emits or modifies electromagnetic radiation in the visible, infrared, and/or ultraviolet spectral regions. JESD77D, 8/12

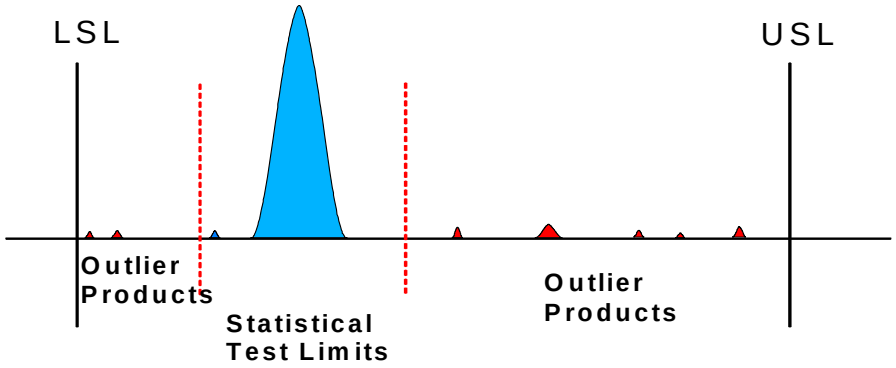
(2) A device that utilizes electromagnetic radiation in the visible, infrared, and/or ultraviolet spectral regions for its internal operation. (Ref. IEC 747-5.)

outlier defect: A physical defect that is not correlated with a known process, equipment, or procedure and cannot be described by a probability-density function of time or location. JEP143C, 7/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

outlier product: Product that meets manufacturer specifications and user requirements but exhibits anomalous characteristics with respect to a normal population and may be subject to a higher-than-normal level of failures in the user's application. JESD50B.01, 11/08



Depiction of eight outliers, seven of which are outlier products

output: The end result of a process that is dependent on the input. JEP132, 7/98

output buffer: A cell or macro that accepts inputs from cells or macros internal to the integrated circuit and propagates signals external to the integrated circuit. JESD12-4, 4/87

output clamp current (I_{OK}): An output current in a region of relatively low differential resistance that serves to limit the voltage swing. JESD99C, 12/12

output clamp voltage (V_{OK}): An output voltage in a region of relatively low differential resistance that serves to limit the voltage swing. JESD99C, 12/12

output clock (C): The input that, on some devices containing an output data register, causes the data to be set into the register. JESD21-C, 1/97

output current (I_O) (1) **(general):** The current into the output terminals. JESD14, 11/86

(2) **(of a voltage regulator):** Synonym for "load current". JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

output enable (1) **(general):** A control input to an integrated circuit that, depending on the logic level applied to it, either permits or prevents the output of data from the device. JESD100-B, 12/99

NOTE When disabled, the outputs assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

(2) **(of a memory) [**pin name **G(n); OE(n)]:** the input that, when false, disables the outputs and causes them to go to an inactive state but does not affect the writing function. JESD21-C, 1/97

NOTE When disabled, the inactive state is floating (Z, high-impedance) for MOS and TTL devices, and low (L) for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

output impedance (of a voltage regulator) (z_o): The small-signal impedance between the regulator output terminal and ground. JESD99C, 12/12

output impedance control (ZQ): An analog signal input that sets the output buffer impedance and the operating mode. JESD21-C, 1/97

output impedance, differential (z_{od}): The small-signal impedance between two ungrounded output terminals of a differential amplifier. JESD99C, 12/12

output impedance, single-ended (z_{os}): The small-signal impedance between one output terminal of a differential amplifier and ground with the other output terminal ac-grounded. JESD99C, 12/12

output load: The load on an output (usually specified in unit loads). JESD12-1B, 8/93
JESD99C, 12/12

output noise voltage (of a voltage regulator) (V_n): The rms output noise voltage with constant load and no input ripples. JESD99C, 12/12

output offset voltage (V_{OO}): The dc voltage between two output terminals (or the output terminal and ground for circuits with one output) when the input terminal(s) are grounded. JESD99C, 12/12

output pin: A device pin that generates a signal or voltage level as a normal function during the normal operation of the device. JESD78D, 11/11

NOTE Output pins, though left in an open (floating) state during testing of other pin types, are latch-up tested.

output resistance (r_o): The small-signal resistance between an output terminal and ground or between differential output terminals. JESD99C, 12/12

output stage drain power voltage (VDDQ): The power pin that is intended to supply power to the output transistors of the device to provide the potential and energy to drive the load applied to the data output (Q) pins or data input/output (DQ) pins. Other, non-data, output transistors may also be designated to be supplied by this power pin. The potential of VDDQ may be specified the same as or different from that of the primary device power pins (VDD). JESD21-C, 1/97#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

output stage logic power voltage (VCCQ): The power pin that is intended to supply power to the output transistors of the device to provide the potential and energy to drive the load applied to the data output (Q) pins or data input/output (DQ) pins. Other, non-data, output transistors may also be designated to be supplied by this power pin. The potential of VCCQ may be specified the same as or different from that of the primary device power pins (VCC). VCCQ is restricted to 5-V applications only. JESD21-C, 1/97#

output stage source power voltage or output stage ground reference (pin) (VSSQ; GNDQ): The ground reference voltage for the data output (Q) or input/output (DQ) pins. Other, non-data, output transistors may also be designated to be referenced to this ground pin. Internal to the device, this pin shall be dc-isolated from the primary ground reference (VSS) pin and any other ground reference pin. External to the device, it must be dc-common with the primary ground reference. JESD21-C, 1/97

output voltage: The voltage at the output terminals. JESD14, 11/86

output voltage drift ($\Delta V_{O(\Delta t)}$): The change in output voltage, usually expressed as a percentage of output voltage, over a period of time. JESD99C, 12/12

output voltage (of a voltage regulator) (V_O): The regulated voltage presented at the output of a regulator (or current-sensing resistor, if used). JESD99C, 12/12

overall average noise figure (of a mixer diode) ($\overline{F}_O$): The average noise figure of the cascaded combination of a mixer and an IF amplifier. JESD77D, 8/12
JESD311A, 11/81

overall charge-transfer efficiency: The fraction of the input signal charge that is transferred as a packet to the output. JESD99C, 12/12

overall symbol grade: The overall quality measure of a two-dimensional bar code symbol determined by machine scanning equipment per guidelines of ISO/IEC 15415 or ANSI INCITS 182-1990. JESD22-B114A, 5/11

NOTE The grades range from 0 (low) to 4 (high) for ISO/IEC 15415 and from F (low) to A (high) for ANSI INCITS 182-1990.

overlapping-gate charge-coupled device: A charge-coupled device formed so that adjacent transfer gates overlap and are insulated from one another. JESD99C, 12/12

overload forward current ($I_{FM(OV)}$): A current whose continuous application would cause the maximum-rated virtual junction temperature to be exceeded, but that is limited in duration such that this temperature is not exceeded. JESD77D, 8/12
JESD282-B, 4/00

NOTE Devices may be subjected to overload currents as frequently as called for by the application while being subjected to normal operating voltages. (Ref. IEC 747-2.)

overload recovery time (t_{or}): The time interval required for an amplifier to recover its ability to perform amplification within stated specification limits after the output voltage amplitude has been distorted by the application of a specified input voltage in excess of rated amplitude or rated rate of change. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

overshoot factor: The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal. (Ref. IEC 748-3.) JESD99C, 12/12

oxide, deposited: An oxide layer formed on a surface by methods not requiring the substrate to participate in the reaction. JESD99C, 12/12

NOTE Various methods such as pyrolysis, evaporation, or sputtering may be employed.

oxide, grown: An oxide layer formed on a semiconductor surface by the reaction of the semiconductor material with oxygen. JESD99C, 12/12

oxide step: A sharp variation of the plane of the oxide on the surface of a planar device. JESD99C, 12/12

P

P: A suffix that may be added to the names of any additional data pins that may be used as parity bits when these additional pins are allowed by JESD21-C (e.g., DQP). JESD21-C, 1/97#

P: See “program or program enable”.

package: See “ball-grid array”, “can package”, “chip carrier”, “chip-scale package”, “clamped package”, “die-size package”, “disk-button package”, “dual-in-line package”, “flange-mount package”, “flatpack”, “grid-array package”, “in-line module”, “in-line package”, “long-form package”, “microelectronic assembly”, “post-mount package”, “press-fit package”, “press-pack”, “quad flatpack”, “single-in-line package”, “small-outline package”, “special-shape package”, “stud-mount package”, “uncased chip”, “vertical surface-mount package”, and “wafer-level package”.

package (of a semiconductor device): An enclosure for one or more semiconductor chips (dice), film elements, or other components, that allows electrical connection and provides mechanical and environmental protection. JESD9B, 5/11#
JESD99C, 12/12

packaged device: A semiconductor device within an enclosure that allows electrical connection to, and provides mechanical and environmental protection for, that device. JEP156, 3/09
JEP158, 11/09

package exterior: The exterior of the package that will be exposed to the usage and storage environment. JESD9B, 5/11

package hole: A hole in the package intended by design, typically an external mounting hole or feed-through hole filled with a glass or ceramic seal. JESD9B, 5/11

package interior; package cavity: The interior of the package that will become the sealed cavity containing and protecting the product circuitry connected to the leads that extend to the interior of the package. JESD9B, 5/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
package plane: A low-impedance metal layer built into an IC package connecting a group of bumps or terminals (typically power or ground). NOTE There may be multiple package planes (sometimes referred to as islands) for each power and ground group.	JS-001-2012, 4/12
package thickness: The device thickness excluding external terminals (balls, bumps, lands, leads) and/or nonintegral heat sinks.	J-STD-020D.1, 3/08
package warpage: The maximum distance between the contact plane and the bottom package surface within the measurement area.	JESD22-B112A, 10/09
pad, bonding: An area on a chip to which a connection can be made.	JESD99C, 12/12
pad, braze: A metallized pad on the ceramic microcircuit package used to braze a lead for electrical and mechanical connections.	JESD9B, 5/11
pad cell area: The physical area available for external electrical and mechanical interfaces.	JESD12-1B, 8/93 JESD99C, 12/12
pad, contact: A metallized pad on the outer edge of the ceramic microcircuit package used for electrical and mechanical connections, typically a castellation.	JESD9B, 5/11
paddle: Synonym for "die-attach pad".	JEP123, 10/95
pad-limited integrated circuit: An integrated circuit whose chip size is determined by the number of pads required.	JESD12-1B, 8/93 JESD99C, 12/12
page: (1) In virtual memory, a fixed-length block that is transferred as a unit between main storage and auxiliary storage. (Adapted from ANSI X3.172.)	JESD100-B, 12/99
(2) A segment of a memory addressed by a subset of its full address field, usually with speed and/or power benefits relative to access by the full address.	JESD100-B, 12/99
(3) A subunit of an erase block consisting of a number of bytes that can be read from, and written to, in single operations through the loading or unloading of a page buffer and the issuance of a program or read command.	JESD218A, 2/11
page mode: An operating mode in which all accesses to a memory occur within a defined page boundary. NOTE For example, for a dynamic random-access memory, the page may be defined by the row address with the column addresses entered on the active transitions of the column address strobe. See also "static-column page mode".	JESD100-B, 12/99
page reset (PR): The input on a page select memory that, when true, unconditionally causes the page select address register to be reset to zero and the corresponding page to be selected.	JESD21-C, 1/97
page select (PS): The input on a page-select memory that, when true, causes one of the pages of memory to be selected as identified by the inputs on the DQ pins (as defined in the appropriate function table) and also causes this page address to be stored in an internal register.	JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
parallel operation: A processing mode in which operations are performed concurrently in one or more devices. (Ref. ANSI X3.172.)	JESD100-B, 12/99
NOTE Contrast with serial operation.	
parallel transmission: The simultaneous transmission on separate channels or bus lines of all the bits necessary to complete a clock cycle.	JESD100-B, 12/99
parameter: A measurable characteristic.	EIA-557-B, 2/06# EIA-599-A, 6/98# JESD659B, 2/07
parameterized macrocell: A macrocell produced by a module generator.	JESD12-1B, 8/93 JESD99C, 12/12
parameterized macro function: A macro function produced by a module generator.	JESD12-1B, 8/93 JESD99C, 12/12
parametric failure: An out-of-tolerance current or voltage level at an input, output, or power-supply terminal of a component. Parametric failures are usually detected during input-leakage, output-voltage, power-supply-current, timing/switching, and capacitance tests.	JEP134, 9/98
parametric fault: In a circuit, a fault that results in failure to meet ac or dc specifications but does not cause functional failure.	JESD12-5, 8/88
parametric test: The process of verifying the specified dc parameters of a device.	JESD12-1B, 8/93 JESD99C, 12/12
Pareto analysis: A technique for problem-solving in which all potential problem areas or sources of variation are ranked according to their contribution.	EIA-557-B, 2/06 JEP131B, 4/12
partition: The process by which a design is mapped into multiple components or functional blocks within a device.	JESD12-1B, 8/93 JESD99C, 12/12
party-line driver: Synonym for “bus driver”.	JESD99C, 12/12
passivation: The formation of an insulating layer directly over a semiconductor surface to protect the surface from contaminants, moisture, and particles.	JESD99C, 12/12
NOTE Usually an oxide of the semiconductor is used; however, deposition of other materials is also used.	
passivation-to-UBM fracture: A fracture between the passivation and the solder underbump metallurgy (UBM).	JESD22-B109A, 1/09
passive circuit element: See “circuit element, passive”.	
passive device: A device in which all circuit elements are passive.	JESD99C, 12/12

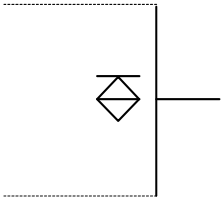
The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

passive-pulldown output: An output similar to an open-circuit except that, in addition to having an internal connection through an active device to a supply voltage, it also has an internal connection through a passive device, usually a resistor, to a second supply voltage that is more negative (less positive) than the first supply voltage. JESD99C, 12/12

NOTE According to the state of the active device, the output voltage can swing between levels approaching the two supply voltages.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):

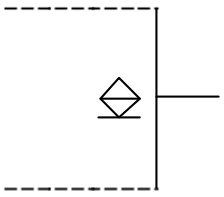


NOTE The bar above the diamond indicates that the output is at the high logic level when the active device is in its on state.

passive-pullup output: An output similar to an open-circuit output except that, in addition to having an internal connection through an active device to a supply voltage, it also has an internal connection through a passive device, usually a resistor, to a second supply voltage that is more positive (less negative) than the first supply voltage. JESD99C, 12/12

NOTE According to the state of the active device, the output voltage can swing between levels approaching the two supply voltages.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



NOTE The bar below the diamond indicates that the output is at the low logic level when the active device is in its on state.

Pb-free; lead-free: Having a concentration of lead (Pb) with a maximum concentration value of 0.1% by weight in each homogeneous material. J-STD-609A.01, 2/11

NOTE Component and end-product suppliers may desire to clarify this important distinction between 0% and 0.1% lead (Pb) with their customers.

Pb-free symbol: A symbol that can be used in place of the phrases ‘‘Pb-free” or “lead-free”. J-STD-609A.01, 2/11

PBGA: Plastic ball grid array package. JESD217, 9/10

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

PC133: A JEDEC designation for systems with a 133-MHz front-side bus using SDRAM main memory technology, running at a nominal clock frequency of 133 MHz. JESD82-2, 7/01

PCB: See "printed circuit board".

PCB component cleanliness: The absence of chemical residues on or in the surface of components on printed circuit boards. JEP122G, 10/11

NOTE These residues may react with the environmental moisture or processing conditions and have either positive or negative impact on product performance.

p-channel charge-coupled device: A charge-coupled device fabricated so that the charges stored in the potential wells are holes. JESD99C, 12/12

p-channel field-effect transistor: A field-effect transistor that has a p-type conduction channel. (Ref. IEC 747-8.) JESD24, 7/85
JESD77D, 8/12

PCN: See "product or process change notice".

PCSE: See "soft error, power cycle".

PD(n): See "presence detect".

peak acceleration: The maximum acceleration during the dynamic motion of the test apparatus. JESD22-B104C, 11/04
JESD22-B111, 7/03

peak junction temperature ($T_{J\ (peak)}$): The highest temperature on the semiconductor chip due to power dissipation internal to the semiconductor chip. JESD51-1, 12/95
JESD51-13, 6/09

peak package body temperature (during MSL classification**):** The highest temperature that an individual package body reaches during moisture sensitivity level (MSL) classification. J-STD-020D.1, 3/08

peak point (1) **(of a programmable unijunction transistor characteristic):** The point on the current-voltage characteristic corresponding to the lowest current at which $dv_{AK}/di_A = 0$ when the gate is biased from a resistive voltage divider. JESD77D, 8/12

(2) **(of a unijunction transistor characteristic):** The point on the emitter current-voltage characteristic corresponding to the lowest current at which $dv_{EB1}/di_E = 0$. JESD77D, 8/12

peak reflow temperature: The maximum package reflow temperature as specified in J-STD-020 depending on package dimensions and whether the product is intended for eutectic Sn-Pb or Pb-free reflow soldering temperature. JESD22-B112A, 10/09

peak reverse recovery current ($I_{RM(REC)}$): The maximum instantaneous value of reverse current that occurs when switching from a forward current condition to a reverse voltage condition. JESD41, 5/95

peak-to-peak noise voltage (of a voltage regulator) ($V_{N(PP)}$): The peak-to-peak output noise voltage with constant load and no input ripples. JESD99C, 12/12

p-e cycle: See "program-erase cycle".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

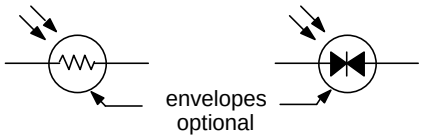
Terms, abbreviations, letter symbols, and definitions	References
pedestal error (of an analog-to-digital converter or **a digital-to-analog converter) (E_p):** A dynamic offset error produced in the commutation process.	JESD99C, 12/12
peeling: The detachment of a sheet-like layer of material from a surface.	JESD9B, 5/11
percent ripple current: See "ripple current, percent".	JESD282-B, 4/00
percent ripple voltage: See "ripple voltage, percent".	JESD282-B, 4/00
performance requirements: The critical process and end-product parameters.	JEP132, 7/98
period jitter ($t_{jit(per)}$): The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.	JESD65B, 9/03
peripheral driver: A circuit designed to interface a digital device with an external nondigital device such as a lamp, light-emitting diode, or data bus.	JESD99C, 12/12
peripheral equipment: In a data processing system, any equipment, distinct from the central processing unit, that may provide the system with outside communication or additional facilities. (Ref. ANSI X3.172.)	JESD100-B, 12/99
peripheral-leaded surface-mount component: A component with a metal frame that provides external surface-mountable terminals located around the periphery of the body of the component.	JEP150, 5/05
peristaltic charge-coupled device: Synonym for "buried-channel charge-coupled device".	JESD99C, 12/12
PFMEA: See "process FMEA".	
phase jitter ($t_{jit(\phi)}$): The deviation in static phase offset, $t_{(\phi)}$, for a controlled edge with respect to the mean value of $t_{(\phi)}$ in a random sample of cycles.	JESD65B, 9/03
phase-locked [lock (ϕ)]: The condition of a phase-locked loop (PLL) device where the reference input and the feedback input remain within the designated static phase offset.	JESD65B, 9/03
phase margin (ϕ_m): The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop voltage amplification is unity.	JESD99C, 12/12
photoconductive diode: A photodiode that is intended to be used as a photoconductive transducer.	JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

photoconductive transducer: A device that is intended to change its conductance as a function of incident radiant flux. JESD77D, 8/12

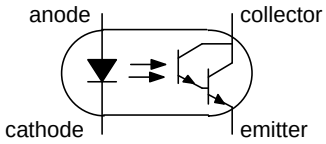
Graphic symbols:



photocurrent: The difference between the light current and the dark current. JESD77D, 8/12

photodarlington coupler: An optocoupler whose photosensitive element is a Darlington phototransistor. JESD77D, 8/12

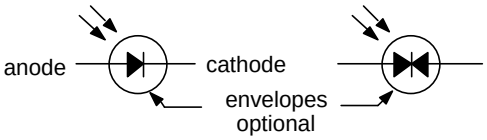
Graphic symbol:



NOTE The base regions may or may not be brought out as electrical terminals.

photodiode: A diode that is intended to be responsive to radiant energy. JESD77D, 8/12

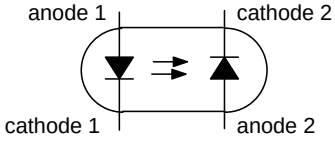
Graphic symbols (ref. IEEE Std 315):



photodiode, avalanche: A photodiode that is intended to take advantage of avalanche multiplication of photocurrent. JESD77D, 8/12

photodiode coupler: An optocoupler whose photosensitive element is a photodiode. JESD77D, 8/12

Graphic symbol:



photoemissive device: Deprecated as a synonym for “photoemitter”. JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

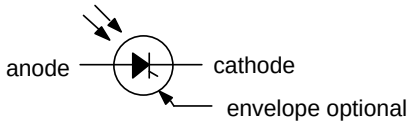
photoemitter: A device that emits electromagnetic radiation in the visible, infrared, and/or ultraviolet spectral regions. JESD77D, 8/12

photoresist: A photosensitive film used in conjunction with photolithography forming a protective mask on a wafer or substrate surface to effect selective process action (e.g., diffusion, etching, etc.). JESD99C, 12/12

photosensitive device: A device that is responsive to electromagnetic radiation in the visible, infrared, and/or ultraviolet spectral regions. JESD77D, 8/12

photothyristor: A thyristor that is intended to be responsive to radiant energy for controlling its operation as a thyristor. JESD77D, 8/12

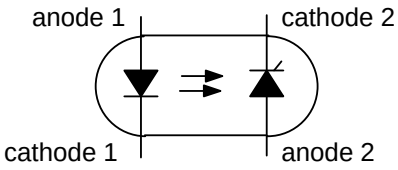
Graphic symbol:



NOTE A gate terminal may or may not be provided.

photothyristor coupler: An optocoupler whose photosensitive element is a photothyristor. JESD77D, 8/12

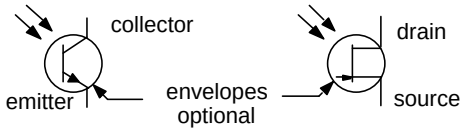
Graphic symbol:



NOTE A gate terminal may or may not be provided.

phototransistor: A transistor that is intended to be responsive to radiant energy. JESD77D, 8/12

Graphic symbols (ref. IEEE Std 315):



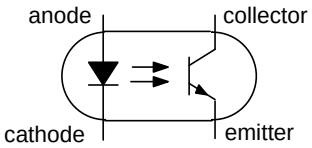
NOTE A base or gate terminal may or may not be provided.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

phototransistor coupler: An optocoupler whose photosensitive element is a phototransistor. JESD77D, 8/12

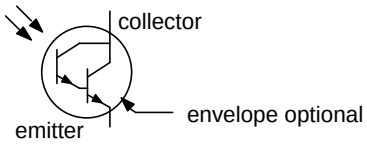
Graphic symbol:



NOTE A base terminal may or may not be provided.

phototransistor, Darlington: A phototransistor whose collector and emitter are connected to the collector and base, respectively, of a second transistor. JESD77D, 8/12

Graphic symbol:



NOTE Base terminals may or may not be provided.

photovoltaic diode: A photodiode that is intended to generate a terminal voltage in response to radiant energy. JESD77D, 8/12

physical failure mechanism: A physical or chemical process that ultimately results in failure. JESD659B, 2/07

physical region (within a semiconductor material): An identifiable volume material whose technological boundaries are fixed by the manufacturing process and independent of operating conditions. JESD77D, 8/12

EXAMPLES Transition region, buried layer, substrate.

physics-of-failure (PoF) concept: An approach to the design and development of reliable product to prevent failure, based on the knowledge of root cause failure mechanisms. JEP148A, 12/08

NOTE….The PoF concept is based on the understanding of the relationships between requirements and the physical characteristics of the product and their variation in the manufacturing processes, and the reaction of product elements and materials to loads (stressors) and interaction under loads and their influence on the fitness for use with respect to the use conditions and time.

pinhole: An imperfection in the form of a small hole that penetrates through a layer of material. (Ref. IPC-T-50.) JESD99C, 12/12
J-STD-002B, 2/03

pin pitch (PP): The nominal center-to-center distance between adjacent pins or terminals along the side of an integrated circuit package. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

pin-to-pin delay model: A model for which delays are specified from input pin(s) to output pin(s). JESD12-1B, 8/93 JESD99C, 12/12

pit (1) **(in a package surface):** A hollow or indentation in a surface, typically caused by a chemical attack. JESD9B, 5/11

(2) **(in a wafer or die):** A visual anomaly that is an indentation. JESD22-B118, 3/11

PLA: See "programmable logic array".

planar (device and **process):** A type of semiconductor device and the process technology used to fabricate it, in which all of the p-n junctions terminate at approximately the same geometric plane on the surface of the semiconductor. JESD99C, 12/12

NOTE Devices using similar technologies, but having one or more diffused areas lying in a slightly different, parallel plane, are also considered planar (e.g., buried collector).

planar fracture: A fracture within the under-bump metallurgy (UBM) layered structure. JESD22-B109A, 1/09

planarity: See "deviation from planarity".

planning activation energy (E_{ap}): A pseudo apparent activation energy, derived from Pareto analysis and experience, using the principles of the physical relationship between stress and failure rate. JEP122G, 10/11 JEP143C, 7/12

NOTE 1….E_{ap} can be used to estimate sample sizes and test times.

NOTE 2….The planning activation energy cannot be calculated as the average value of the apparent activation energies of the various failure mechanisms because different failure mechanisms have different weighting factors and the apparent activation energy values affect the acceleration factor exponentially rather than linearly.

plastic: Any of a group of synthetic or natural organic compounds produced by polymerization, optionally combined with additives (organic or inorganic fillers, modifiers, etc.) into a homogeneous material capable of being molded, extruded, or cast into various shapes and films. JS709A, 5/12

plastic leaded chip carrier (PLDCC): A chip-carrier package that has a molded plastic body and J-formed leads. The often-used abbreviation "PLCC" is ambiguous and is deprecated. JESD21-C, 1/97

plating: A thin coating of metal applied to the base metal or another plating layer by mechanical, chemical, or electrochemical means. JESD9B, 5/11

PLD: See "programmable logic device".

PLDCC: See "plastic leaded chip carrier".

PLL device: A logic device that includes a phase-locked loop and may also include other logic functions, such as counters, registers, and buffers. JESD65B, 9/03

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
PLL lock time after frequency change ($t_{L(\omega)}$): The time interval required for a phase-locked loop (PLL) to lock after the input reference clock frequency has been changed. NOTE The PLL lock time after frequency change is measured from the time the new input reference clock frequency is stable to the time the PLL locks.	JESD65B, 9/03
PLL output duty cycle (ODC): The ratio of the time interval between the phase-locked-loop-controlled (PLL-controlled) edge and the noncontrolled edge, to the time interval between PLL-controlled edges, expressed as a percentage (%).	JESD65B, 9/03
PLL recovery time ($t_{recL(\phi)}$): The time interval required for a phase-locked loop (PLL) to recover phase lock after the input reference clock changes phase.	JESD65B, 9/03
PLL reference zero delay ($t_{(\phi)}$): In JESD65B, this concept has been replaced by the concept "static phase offset ($t_{(\phi)}$)".	JESD65B, 9/03#
PLS: See "programmable logic sequencer".	
p-n boundary: An interface in the transition region between p-type and n-type materials at which the donor and acceptor concentrations are equal.	JESD77D, 8/12
p-n junction; p-n transition region: A junction between p-type and n-type semiconductor regions.	JESD77D, 8/12
pock (on a package): A partially closed cavity on a surface.	JESD27, 8/93 Rescinded 5/11
Poisson distribution: A specific discrete probability distribution often applied to attributes data.	EIA-557-B, 2/06
polymer: Any of various chemical compounds made of smaller, identical molecules (called monomers) linked together, typically used as adhesives for microelectronics assembly.	JESD9B, 5/11
population: The collection of all possible values of a given characteristic.	EIA-557-B, 2/06
population failure distributions: The applicable mortality functions. NOTE….Typically used failure distributions for early-life failures include the Weibull and Poisson (exponential); for useful life and wearout these and the lognormal and Gaussian (normal) distributions are used. The Gaussian is often not appropriate because of the extension to negative times.	JEP143C, 7/12 JESD74A, 2/07 JESD85, 7/01#
POR: See "process of record".	
port A (A); port B (B): The two ports in a dual-port memory device. The letter A or B is appended as a suffix to any pin that is specific to that port.	JESD21-C, 1/97
positive-breakdown-resistance thyristor surge protective device: A thyristor surge suppressor whose static characteristic for the breakdown region has a net positive-resistance slope prior to switching.	JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

positive-going input threshold voltage (V_{IT+}): The input threshold voltage when the input voltage is rising. JESD99C, 12/12

positive logic: The representation of the logic 1-state and the logic 0-state by the high and the low levels, respectively. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

post-mount package: A package, intended for mounting to an interconnect structure or cold plate, that incorporates a threaded stud, threaded hole, or post for that purpose. JESD30E, 8/08

NOTE….A variety of package sizes, shapes, and external terminal forms may be used.

post-stress electrical failure; electrical test failure after stressing: A device that does not meet the individual device specification or other criteria specific to the environmental stress as a result of the stress test. JESD47I, 7/12

potential cause of failure: A property, characteristic, or occurrence that could lead to a failure, described in terms of something that can be corrected or controlled. JEP131B, 4/12

potential failure mode: The manner in which the process could potentially fail to meet the process requirements and/or design intent. JEP131B, 4/12

NOTE Potential failure mode is a description of the nonconformance at that specific operation. It can be a cause associated with a potential failure mode in a subsequent (downstream) operation or an effect associated with a potential failure in a previous (upstream) operation. However, when the failure mode and effect analysis (FMEA) is prepared, the assumption should be made that the incoming part(s)/material(s) are correct.

potential physical failure mechanism: A physical failure mechanism that (1) has been identified through physical experimentation to exist for similar products or (2) can be linked to these products through the scientific study of the product (process) physical characteristics and the physical conditions found to be necessary for the failure mechanism to occur. JEP122G, 10/11
JEP143C, 7/12

potential well (of a charge-coupled device): The region around a local potential-energy minimum that is formed in the semiconductor of a charge-coupled device under control of the voltage applied to the transfer gate and confines any mobile charges that may be present. JESD99C, 12/12

power cycle: A temperature cycle in an application resulting from cycling power on and off. JESD94A, 7/08

NOTE The hibernate, shutdown, and standby modes are classified as power off.

power cycle time: The time interval between one power-on and the next, or from one power-off and the next. JESD22-A105C, 1/04

power gain, (insertion) (G_P): The ratio (usually expressed in dB) of (1) the signal power delivered to the load after insertion of a transducer between the source and the load to (2) the signal power that was delivered to the load when the load was connected directly to the source. JESD99C, 12/12

power gain, transducer (G_T): The ratio (usually expressed in dB) of the signal power delivered to the load to the signal power available from the source. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

power input, dc total, to all terminals (P_T): The sum of the products of the dc input currents and voltages, i.e.,$V_{BE} \cdot I_B + V_{CE} \cdot I_C$ or $V_{EB} \cdot I_E + V_{CB} \cdot I_C$. JESD10, 1/76

power input, instantaneous total to all terminals (p_T): The sum of the products of the instantaneous input currents and voltages. JESD10, 1/76

power input to the base, common-emitter (P_{BE}): The product of the input current and voltage in the common-emitter circuit configuration. JESD10, 1/76

power-up PLL lock time (t_L): During PLL power up, the time required for the phase-locked loop (PLL) to lock after achieving the minimum specified operating voltage. JESD65B, 9/03

PP: See "pin pitch".

ppm: parts per million. JEP143C, 7/12
JESD16-A, 4/95#
JESD74A, 2/07#

NOTE 1….When used to describe average outgoing quality, ppm refers to the number of nonconforming units for each million units.

NOTE 2….When used to describe failure rate, ppm refers to the number of units with reliability failures for each million units.

ppm/time period: The number of failures per million units in the time period of interest. JEP143C, 7/12
JESD74A, 2/07

PR: See "page reset".

precharge time: The time interval between specified transitions at one or more inputs intended to allow the input nodes of the dynamic circuitry to be charged or discharged to predetermined voltage levels prior to the start of a new cycle. JESD100-B, 12/99

NOTE This defines the actual precharge time interval, which is determined by the system in which the device is to operate. A minimum value is specified that is the shortest interval for which correct operation of the device is to be expected.

precision: The measure of natural variation of repeated measurements. EIA-557-B, 2/06

preconditioned pin: A device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the device under test. JESD78D, 11/11

predictability: The ability to determine in advance the quantifiable output of a process (e.g., quantity, cycle time, etc.). JEP132, 7/98

prefix 54: A prefix used with several series of TTL, CMOS, and BiCMOS devices (e.g., 54XXX and 54FCTXXX) to indicate the military temperature range applicable to that series. JESD7-A, 8/86#
JESD18-A, 1/93#
JESD64-A, 10/00#
JESD82-2, 7/01#

prefix 74: A prefix used with several series of TTL, CMOS, and BiCMOS devices (e.g., 74XXX and 74FCTXXX) to indicate the commercial temperature range applicable to that series. JESD7-A, 8/86#
JESD18-A, 1/93#
JESD55, 5/96#
JESD64-A, 10/00#
JESD82-2, 7/01#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References

presence detect [PD(n)]: A group of output pins, normally used on modules or cards, whose state is used to convey information about the capacity, speed, configuration, or other attributes of the device when plugged into a system. JESD21-C, 1/97

press-fit package: A round or elliptical package whose mechanical mounting area is pressed into the packaging interconnect structure or cold plate for purposes of thermal and electrical connection. JESD30E, 8/08

press-pack: Synonym for "press-fit package". JESD30E, 8/08

preventive action: Action taken to modify the management systems, practices, or procedures to prevent recurrence of the current problem and similar problems where applicable. JESD671B, 6/12

primary input: An input driven from outside of the circuit boundary. JESD12-1B, 8/93 JESD99C, 12/12

primary output: An output driving outside the circuit boundary. JESD12-1B, 8/93 JESD99C, 12/12

primary threshold crossing (of a clock signal): The threshold crossing of a clock signal indicating the start of a new cycle and the end of the previous cycle. JESD65B, 9/03

primitive (building block): A basic building block for a specified level of design hierarchy. JESD12-1B, 8/93 JESD99C, 12/12

principal-current charge carriers (within the body of a device): The charge carriers that compose the principal current. JESD77D, 8/12

NOTE The definition excludes charge carriers that are present for control purpose only.

principal current (in a semiconductor device): The current that is switched or controlled by the semiconductor device. JESD77D, 8/12

principal (voltage-current) characteristic, (static) (of a bidirectional [unidirectional] triode thyristor): A function, usually represented graphically, relating the principal [anode] voltage to the principal [anode] current for a specified virtual junction temperature, under conditions of internal electrical and thermal equilibrium. JESD77D, 8/12

NOTE 1 Where applicable, the characteristic may be given with the gate current as a parameter.

NOTE 2 The word "static" is usually omitted except when a distinction between static and dynamic characteristics is necessary.

principal voltage (of a thyristor): The voltage (potential difference) between the main terminals. JESD77D, 8/12

NOTE 1 In the case of unidirectional triode thyristors, the principal voltage is called positive when the anode potential is more positive than the cathode potential and called negative when the anode potential is less positive than the cathode potential. Thus, for these thyristors, "principal voltage" and "anode-cathode voltage" are synonymous.

NOTE 2 In the case of bidirectional thyristors, the principal voltage is called positive when the potential of main terminal 2 is more positive than the potential of main terminal 1.

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Terms, abbreviations, letter symbols, and definitions	References
printed circuit board (PCB): An insulating substrate used to mechanically support and electrically connect electronic components using conductive pathways or signal traces by printing or etching tracks of a conductor such as copper on one or both sides of the substrate. NOTE A PCB is also called a printed wiring board (PWB) or etched wiring board.	JEP122G, 10/11# JEP160, 11/11 JESD217, 9/10#
probability: The relative frequency with which an outcome takes place over a very large number of trials in each of which the outcome could have occurred.	EIA-557-B, 2,06#
probability density function of the time-to-failure; mortality function [f(*t*)]: The distribution of the probabilities of failure as a function of time. NOTE….The probability of failure during the interval Δt that immediately follows the instant t_1 is given by the integral of f(t) from $t = t_1$ to $t = (t_1 + \Delta t)$.	JEP122G, 10/11 JEP143C, 7/12 JESD85, 7/01
probability distribution: A collection of all possible outcomes of a random event, together with their respective probabilities.	EIA-557-B, 2/06
probability distribution function: A mathematical representation of a probability distribution.	EIA-557-B, 2/06
problem analysis: Investigation to determine the root cause of a reported component problem.	JESD671B, 6/12
problem solving: The process of moving from effects to causes (special or common) to actions that improve performance.	EIA-557-B, 2/06
process: (1) A combination of people, procedures, methods, machines, materials, measurement equipment, and/or environment for specific work activities to produce a given product or service. NOTE Only definition (1) appears in JESD46D. (2) A repeatable sequence of activities with measurable inputs and outputs. NOTE Only definition (2) appears in JESD89A.	EIA-557-B, 2/06 EIA-599-A, 6/98# JEP131B, 4/12 JESD46D, 12/11 JESD89A, 10/06 JESD659B, 2/07
process analysis (tools): Tools for process analysis, which include histograms, scatter diagrams, time line charts, bar charts, and control charts (for existing or modified processes).	JEP132, 7/98
process average: The location of the distribution of measured values of a particular process characteristic.	EIA-557-B, 2/06
process capability study: A study that quantifies natural process variability.	EIA-557-B, 2/06#
process change: A change in processing that could alter the capability of the process to meet the design requirements or durability of the product.	JEP131B, 4/12A
process characterization: The determining of relationships between process parameters and process outputs or product characteristics.	EIA-599-A, 6/98

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
process corner characterization: The method of determining the functional robustness of a process by varying parameters across their design limits. NOTE 1 These varied parameters usually involve the operating extremes of the device with respect to power supplies, frequency, and temperature, but other input ac and dc parameters could also be varied. NOTE 2 The samples for process corner characterization could be either taken from the extremes of a random distribution or by varying the input parameter of a process technology to intentionally generate the corner parameters.	JESD86A, 10/09#
processed wafer: A wafer that has had an operation or process performed on it to accomplish a particular objective.	JESD22-B118, 3/11
process FMEA (PFMEA): A systematic method to assess the risks of the elements of a process and their interactions of a production or business process in terms of process requirements.	JEP131B, 4/12
process geometry: The minimum allowable drawn dimensions for designing an integrated circuit using a specified technology.	JESD12-1B, 8/93 JESD99C, 12/12
processing unit: Synonym for "central processing unit".	JESD100-B, 12/99
process lot: A batch of material processed in a given time interval through the same or similar equipment.	JESD91A, 8/01
process mapping: Synonym for "flow charting".	JEP132, 7/98
process of record (POR): (1) A detailed description of the production process flow.	JEP131B, 4/12
(2) The specified manufacturing processes with no changes allowed unless proper approval is obtained in accordance with the requirements of JESD46.	JESD22-B118, 3/11
processor: In a computer, a functional unit, consisting of at least an instruction control unit and an arithmetic unit, that interprets and executes instructions. (Adapted from ANSI X3.172.)	JESD100-B, 12/99
process parameter: A measurable characteristic of a process that impacts product performance but may not be measured on the product.	EIA-599-A, 6/98
process potential: The capability of a parameter over a brief period of time.	EIA-599-A, 6/98
process-programmable gate array: A gate array integrated circuit that is programmed as part of the integrated circuit manufacturing process. NOTE Process-programmable gate arrays are characterized by the ability to inventory partially fabricated wafers prior to interconnection.	JESD12-1B, 8/93 JESD99C, 12/12
process repeatability: A condition wherein the process output is consistent over time and the product characteristics have similar distribution parameters, e.g., mean, sigma, shape, etc.	JEP132, 7/98#
process spread: The extent to which the individual values of a process characteristic vary.	EIA-557-B, 2/06

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Terms, abbreviations, letter symbols, and definitions	References
procurement document: A document, e.g. source-controlled drawing (SCD), specification, statement of work, purchase order, that defines the requirements (mechanical, electrical, etc.) for the item being procured.	JESD9B, 5/11
product: (1) The output of a process.	EIA-599-A, 6/98
(2) A component or service sold to satisfy a particular customer application.	JESD89A, 10/06
(3) An item that the respondent making a material/substance content declaration is supplying to the electrotechnical industry, such as assemblies, subassemblies, components, and raw materials.	JIG-101 Ed 2.0, 4/09
NOTE 1 The term "product" also covers a product family if the products within that family perform the same function and have consistent material declarations.	
NOTE 2 Under the EU REACH regulation (*Registration, Evaluation, Authorization and Restriction of Chemicals*), a product would be called an "article".	
product defect rate: The statistically calculated probability that a product does not meet the specification for some quality characteristic.	JEP121A, 10/06
production tooling: The tool set used during wafer fabrication, assembly, and testing for manufacturing devices.	JESD86A, 10/09
product or process change notice (PCN): A document sent to users describing product or process changes, the reasons for the change, and the projected impact of the change.	JESD46D, 12/11
product performance: The totality of the capability of characteristics of a product.	EIA-557-B, 2/06
product traceability: A methodology for tracing products, forward or backward, through the manufacturing flow to isolate materials that could be similar to product identified as having quality or reliability problems.	JESD50B.01, 11/08
NOTE 1 For forward traceability, all products associated with a process step must be identifiable.	
NOTE 2 Backward traceability is the identification of the product at all stages from shipped product through raw material.	
profile tolerancing: A tolerance zone that lies along the true profile of the part and within which all elements of the profile must lie. Form as well as combinations of form, size, and orientation can be controlled by this tolerance.	JESD95-1, 3/97

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Terms, abbreviations, letter symbols, and definitions **References**

program: (1) A sequence of instructions suitable for processing. (Ref. ANSI X3.172.) JESD100-B, 12/99

(2) To design, write, and test programs. (Ref. ANSI X3.172.)

(3) To enter data into a programmable read-only memory.

NOTE 1 Fixed programming is accomplished during manufacture of the memory, e.g., by using a mask.

NOTE 2 Field programming is accomplished after the manufacturing of the memory device is otherwise complete, e.g., by selectively blowing fuses.

NOTE 3 The programming of an electrically programmable read-only memory is accomplished by injecting electrons into the floating gates of selected cells.

program; configure: To modify the logic connections inside a programmable device, causing its function to change. No assumption is made as to technology (EPROM, EEPROM, SRAM, etc.) or to erasability. The device can implement logic, memory, or control. JESD32, 6/96

program-erase cycle (p-e cycle): (1) The event of writing a memory cell from the programmed state to the erased state and back to the programmed state. (Ref. IEEE Std 100.) JESD100-B, 12/99

(2) The writing of data to one or more pages in an erase block and the erasure of that block, in either order. JESD218A, 2/11

programmable application–specific device: A complex array of logic elements whose interconnection pattern can be field-programmed to fill the needs of specific applications. JESD21-C, 1/97

programmable logic array (PLA): (1) An integrated circuit consisting of an array of combinational logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions. (Ref. IEC 748-2.) JESD99C, 12/12

NOTE The PLA is typically a large set of AND gates driving several OR gates.

(2) A cell that emulates a programmable logic array that has been programmed in a custom integrated circuit. JESD99C, 12/12

programmable logic device (PLD): An integrated circuit consisting of an array of logic elements whose interconnection pattern can be programmed (either mask-programmed or user-programmed) to perform specific logic functions. JESD21-C, 1/97#

programmable logic sequencer (PLS): (1) An integrated circuit consisting of an array of combinational and sequential logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions. JESD99C, 12/12

(2) A cell that emulates a programmable logic sequencer that has been programmed in a custom integrated circuit.

programmable read-only memory (PROM): A field-programmable read-only memory that can have the data content of each memory cell altered only once. JESD21-C, 1/97
JESD100-B, 12/99

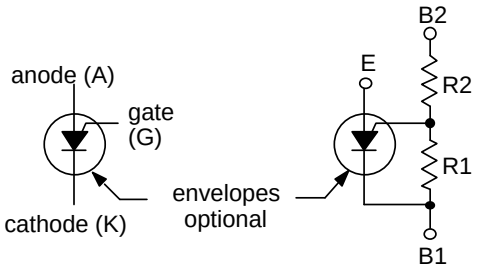
The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

programmable unijunction transistor (PUT): A three-terminal thyristor that, when biased with two external resistors and a voltage source, can provide a negative-resistance characteristic similar to the characteristic of a unijunction transistor. JESD77D, 8/12

NOTE The negative-resistance characteristics are controlled by the resistor and voltage values.

Graphic symbol:



PUT with bias resistors

NOTE B1, B2, and E are the equivalent unijunction terminals with interbase resistance $r_{BB} = R_1 + R_2$ and intrinsic standoff ratio $\eta = R_1/(R_1 + R_2)$.

programming failure: Failure of a nonvolatile memory device, such as a programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), etc., to respond properly during a write and/or read test. JEP134, 9/98

programming power voltage (VPP): A special high-voltage supply that supplies the potential and energy for altering the state of certain nonvolatile memory arrays. On some devices, the presence of VPP also acts as a program enable signal (P). JESD21-C, 1/97

program or program enable (P): The input on a nonvolatile memory device that, when true, causes the data present on the D or DQ pins to be written into the addressed cell(s) of the device. JESD21-C, 1/97

PROM: See "programmable read-only memory".

propagation (delay) time (t_{pd}): The time interval between specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. JESD99C, 12/12
JESD100-B, 12/99

NOTE All of the response times (i.e., access, disable, enable, sense recovery, and output data-valid times) are subsets of propagation times. As integrated circuits have become more complex, the response times have been broken down into more and more specialized subgroups.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

propagation (delay) time, high-to-low-level output (t_{PHL}): The time interval between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level. JESD99C, 12/12

NOTE In IEC 748-2, the reference points on both the input and output waveforms have the same value, which is midway between the maximum low-level input voltage (V_{IL}max) and the minimum high-level input voltage (V_{IH}min).

propagation (delay) time, low-to-high-level output (t_{PLH}): The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to the defined high level. JESD99C, 12/12

NOTE In IEC 748-2, the reference points on both the input and output waveforms have the same value, which is midway between the maximum low-level input voltage (V_{IL}max) and the minimum high-level input voltage (V_{IH}min).

prospective triggering area: In a graphical presentation $V_{FG} = f(I_{FG})$, the area enclosed between the lines for the specified values of upper-limit and lower-limit gate trigger current and gate trigger voltage. JESD77D, 8/12

protection impedance: The turn-on impedance of any ESD clamp during the ESD current flow. JEP155A.01, 3/12

protective coating: A layer of insulating material applied over the circuit elements for the purpose of mechanical and environmental protection and prevention of contamination. JESD99C, 12/12

protrusion: A raised portion that protrudes or projects from a surface, typically indigenous with the surface material. JESD9B, 5/11

protrusion, hanging: A protrusion that can be moved with a probe but is still connected to the surface. JESD9B, 5/11

protrusion, solid: A protrusion that cannot be moved with a probe. JESD9B, 5/11

PS: See “page select”.

pseudostatic (random-access) memory (PSRAM): (1) A combinational form of a dynamic RAM that incorporates various refresh and control circuits on-chip (e.g., refresh address counter and multiplexer, interval timer, arbiter). These circuits allow the PSRAM operating characteristics to closely resemble those of an SRAM. JESD21-C, 1/97

(2) A random-access memory whose internal structure is a dynamic memory with refresh control signals generated internally, in the standby mode, so that it can mimic the function of a static memory. JESD100-B, 12/99

NOTE In practice, unlike so-called self-refresh DRAMs, PSRAMs have nonmultiplexed address lines and pinouts similar to those of SRAMs.

pseudo write transfer (PWT): A nonmemory cycle in which the operational mode of the serial port is changed from an output to an input and the tap pointer is set at the same time. This is a counter that defines the starting point in the serial data register into which data is entered. Data is entered serially from this point, with wraparound when the end is reached. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

PSRAM: See "pseudostatic random-access memory".

p-type semiconductor: An extrinsic semiconductor in which the mobile-hole density exceeds the conduction-electron density. (Ref. IEC 747-1.) JESD77D, 8/12

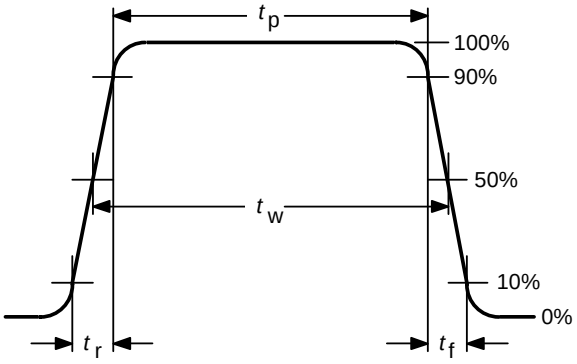
pulse duration; acceleration interval: The time interval between the instant when the acceleration first reaches 10% of its specified peak level and the instant when the acceleration first returns to 10% of the specified peak level after having reached that peak level. JESD22-B104A, 11/04
JESD22-B111, 7/03

pulse duration, average (formerly **pulse average time) (t_w):** The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge. JESD10, 1/76#
JESD77D, 8/12

NOTE If the reference points are not 50% points, the symbol t_p and the term "pulse duration" should be used.

pulse duration (formerly **pulse time) (t_p):** The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform. JESD10, 1/76#
JESD77D, 8/12

NOTE The two reference points are usually 90% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge. If the reference points are 50% points, the symbol t_w and the term "average pulse duration" should be used.



Pulse time symbology

pulse duration [width] (t_w): The time interval between the specified reference points on the two transitions of the pulse waveform. JESD99C, 12/12
JESD100-B, 12/99

pulse width: See preferred term "pulse duration". JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

punch-through voltage (V_{PT}): The reverse-bias voltage applied to the drain terminal that results in significant drain-to-source current even though the transistor is biased in its off state. JESD60A, 9/04 JESD90, 11/04

NOTE….Punch-through is differentiated from junction breakdown in that the current path is from drain to source instead of from drain to substrate, as is the case for junction breakdown.

pushdown stack: Synonym for "pushdown storage". JESD100-B, 12/99

pushdown storage: Storage in which data are ordered in such a way that the next data element to be retrieved is the most recently stored. (Ref. IEC 824.) JESD100-B, 12/99

NOTE The method is "last-in, first-out".

push-pull output: (1) Two open-circuit outputs operating in complementary fashion so that as the resistance of one increases, the resistance of the other decreases JESD99C, 12/12

(2) Originally a synonym for "totem-pole output", this usage is now deprecated.

NOTE The term "push-pull output" is usually applied to linear circuits.

PUT: See "programmable unijunction transistor".

PWT: See "pseudo write transfer".

Q

Q: See "quality factor".

QFD: See "quality function deployment".

QML: See "qualified manufacturers list".

QMP: See "quality management plan".

Q(n)(x): See "data output".

QSY: See "transfer acknowledge output".

quad flatpack: A surface-mount package whose terminals are on four sides and consist of metal pad surfaces (on leadless versions) or leads emerging from the package. JESD21-C, 1/97# JESD30E, 8/08

NOTE 1….The package leads may be formed to facilitate surface mounting.

NOTE 2….The small-outline package is similar except for having terminals on only one side or two opposite sides of the package.

quad word: A character string or binary element string that, in a given system, has four times the length of a word. JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
qualification: The process of demonstrating that an entity is capable of meeting or exceeding the specified requirements. NOTE 1 Examples of an entity are a facility, a process, a product, a service, and a system. NOTE 2 Examples of types of requirements are performance, quality, reliability, environmental, and safety.	EIA-599-A, 6/98# JEP143C, 7/12 JEP148A, 12/08
qualification family: (1) Products sharing the same process technology.	JESD74A, 2/07
(2) A group of solid-state drive (SSD) products that differ only in storage capacity and in minor design details that are directly related to the capacity differences.	JESD218A, 2/11
qualification requirements: The quality and reliability properties of the product that demonstrate compliance with the application requirements.	JEP148A, 12/08
qualified manufacturers list (QML): A list of manufacturers whose production lines have been certified and qualified by the Defense Supply Center Columbus (DSCC) for the production of devices used in military or space applications.	JEP133C, 1/10
qualifying activity: (1) The organizational element that grants certification status; this element may be a part of a) the acquiring activity; b) a quality organization within the manufacturer's company that is independent of the group(s) responsible for the device production, screening, and marketing; or c) an independent third-party organization. (2) The organizational element of the government that grants certification and QML status.	JEP133C, 1/10
quality: Conformance of a product to requirements, or perceived fitness for its intended use(s).	JESD46D, 12/11
quality characteristic: A process or device attribute that may affect the final product quality or reliability.	JEP121A, 10/06
quality factor (*Q*): Two pi (2π) times the ratio of the maximum energy stored per cycle to the energy dissipated per cycle at a given frequency. NOTE The *Q* of an inductor at a frequency is the magnitude of the ratio of its reactance to its effective series resistance at that frequency. (IEEE Std 100.)	JESD10, 1/76
quality function deployment (QFD): (1) A technique for analysis of the interrelationships between different requirements.	EIA-557-B, 2/06
(2) A structured method in which customer requirements are translated into appropriate technical requirements for each stage of product development and production.	JEP132, 7/98#
quality management plan (QMP): A plan described in military specifications (MIL-PRF-19500, MIL-PRF-38534, and MIL-PRF-38535) that describes the methods a supplier uses to assure conformance to the applicable requirements, including design, manufacturing, and verification.	JEP133C, 1/10
quality rating: An assessment of the metrics established to evaluate the quality.	JEP146A, 1/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

quantity symbol: A letter symbol that is used to represent a physical quantity or a relationship between quantities. JESD77D, 8/12 JESD99C, 12/12

NOTE The letter symbol used to designate a quantity or parameter shall be a single letter. This single letter, referred to as the primary symbol, may be modified by subscripts or superscripts.

quantization error, inherent (of an ideal analog-to-digital converter): Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value. JESD99C, 12/12

NOTE 1 This error follows necessarily from the quantization procedure. For a linear analog-to-digital converter, its value equals ±½ LSB.

NOTE 2 Use of the term "resolution error" in place of "inherent quantization error" is deprecated, because "resolution" as a design parameter has a nominal value only.

quantum efficiency (of a photosensitive device): The ratio of the number of effective electron-hole pairs produced within the device to the number of incident photons. JESD77D, 8/12

NOTE For devices that internally amplify or multiply the electron-hole pairs (such as phototransistors or avalanche photodiodes), the effect of the gain is to be excluded from quantum efficiency.

quantum efficiency, external (of a photoemitter): The ratio of the number of photons radiated to the number of electrons flowing into the radiation source. JESD77D, 8/12

quantum efficiency, internal (of a photoemitter): The ratio of the number of photons internally produced to the number of electrons flowing into the radiation source. JESD77D, 8/12

quiescent current: The dc current through a terminal when no signal is applied. JESD99C, 12/12

quiescent output voltages (V_O): The dc voltage at an output terminal with reference to a common terminal, normally ground, when no signal is applied to the input. JESD99C, 12/12

quiescent voltage: The dc voltage at a terminal when no signal is applied. JESD99C, 12/12

quoted failure rate (λ_q): The predicted failure rate for typical operating conditions. JEP122G, 10/11 JEP143C, 7/12

NOTE….The quoted failure rate is calculated from the observed failure rate under accelerated stress conditions multiplied by an acceleration factor; e.g., $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s. When multiple failure mechanisms and thus multiple acceleration factors are involved, then a proper summation technique, e.g., sum-of-the-failure-rates method, is required.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

R

RA: See "row address input".

radiance (L_e): The radiant intensity of any surface in a given direction per unit of projected area of the surface as viewed from that direction. JESD77D, 8/12

NOTE Radiance is typically measured in $W \cdot sr^{-1} \cdot m^{-2}$ (watt per steradian·square meter).

radiant efficiency: The total radiant flux emitted divided by the total input power. JESD77D, 8/12

radiant exitance (M_e): The density of the radiant flux leaving an emitter surface, i.e., the radiant flux divided by the area of emitting surface. JESD77D, 8/12

radiant flux: See "flux (2) (radiant)".

radiant intensity (I_e): The radiant flux per unit solid angle in a given direction. JESD77D, 8/12

radiation: (1) The process of emitting radiant energy in the form of electromagnetic waves or moving nuclear particles. Merriam-Webster's Collegiate Dict.

NOTE 1 Electromagnetic waves include x-rays, gamma rays, light, etc. These forms of radiation all consist of photons, which are quanta of electromagnetic energy.

NOTE 2 Nuclear particles include alpha particles (helium nuclei), beta particles (electrons), neutrons, and other atomic particles that can transfer energy to a material. Subatomic particles such as quarks are not considered.

(2) Energy radiated in the form of electromagnetic waves or moving nuclear particles. Merriam-Webster's Collegiate Dict. JESD51-1, 12/95# JESD51-13, 6/09# JESD89A, 10/06

NOTE See notes to "radiation" (1).

radiation hardening: (1) Increasing the ability of a device to survive one or more types of radiation. JESD99C, 12/12

(2) The process whereby the ability of a device to survive one or more types of radiation is increased.

radiation-hardness assurance (RHA): The aspect of product assurance that ensures that parts continue to perform within specifications or degrade in a specified manner when subjected to given radiation environments. JEP133C, 1/10

radiation-hardness-assured (RHA): Possessing the aspect of product assurance that ensures that parts continue to perform within specifications or degrade in a specified manner when subjected to given radiation environments. JEP133C, 1/10

radiation-hardness-assured capability level (RHACL): The radiation level to which the die manufacturer guarantees satisfactory performance. JEP133C, 1/10

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Terms, abbreviations, letter symbols, and definitions **References**

radio frequency [RF] microwave hybrid: A hybrid microcircuit that meets one or more of the following criteria: JESD93, 9/05

— it contains input and output terminals or connectors with matched impedance;

— it uses specific impedance transmission lines on an insulating substrate;

— its RF performance characteristics are affected by conductor length, width, or topology.

rail-to-rail driver: A bipolar (three-state or totem-pole) output that can swing between voltage levels that are essentially equal to the supply voltages. JESD99C, 12/12

NOTE This is typically accomplished by driving the active devices from boost voltages or charge pumps.

RAM: See "random-access memory".

ramp delay, steady-state (of a multiplying digital-to-analog converter) ($t_{d(ramp)}$): The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed. JESD99C, 12/12

RAM read/write, no mask (RR/RW): A normal RAM read or write access cycle with no SAM or special RAM features or functions actuated. JESD21-C, 1/97

RAM write with new mask (RWNM): A RAM write cycle in which the data bits that are to be written are controlled by a write mask that is supplied at the beginning of the write cycle on the DQ(n) terminals. A high mask bit normally enables the write function for that bit; a low mask bit leaves the data unaltered. JESD21-C, 1/97

RAM write with old mask (RWOM): A RAM write cycle in which the data bits that are to be written are controlled by a write mask register that was loaded in a previous cycle. A high mask bit normally enables the write function for that bit; a low mask bit leaves the data unaltered. JESD21-C, 1/97

random-access memory (RAM): (1) A memory in which access to all storage data can be achieved in essentially the same time, independent of the location. In a multiport memory, this term refers to that portion of the array that contains the memory cell array and its drivers, sense amplifiers, control circuitry, and the circuitry associated with the normal random-access data port. JESD21-C, 1/97

(2) A memory that permits access to any of its address locations in any desired sequence with similar access time to each location. (Adapted from IEC 748-2.) JESD100-B, 12/99

NOTE The term "random-access memory", as commonly used, denotes a read/write memory with unlimited data rewrite capability and similar read and write times.

random defect: A physical defect that is correlated to some known process, equipment, or procedure, and can be described by a probability-density function of time or location. JEP122G, 10/11
JEP143C, 7/12
JESD91A, 8/01

randomness: A condition in which individual values are not predictable, although they may come from a definable distribution. EIA-557-B, 2/06

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

random sample: A set of individuals taken from a population in such a way that each possible individual has an equal chance of being selected. EIA-557-B, 2/06

range: The difference between the maximum and minimum values. A measure of spread. EIA-557-B, 2/06

rank: The portion of memory, from one memory die, that is logically connected to a single channel within a memory stack. JESD229, 12/11

RAS: See "row enable input".

rated moisture sensitivity level (MSL): The moisture sensitivity level as determined by J-STD-020. JESD22-B112A, 10/09

rating: The nominal value of any electrical, thermal, mechanical, or environmental quantity assigned to define the operating conditions under which a component, machine, apparatus, electronic device, etc., is expected to give satisfactory service. (Ref. IEC 747-1.) JESD77D, 8/12
JESD99C, 12/12

NOTE "Rating" is a generic term, but also see "maximum rating".

RC: See "recall".

RCR: See "read color register".

RE: See "row enable input".

reactive ion etching (RIE): A plasma etching process using a relatively low gas pressure and high electric field, in which material is removed primarily by chemical reaction with active radicals although some material may also be removed physically by ion bombardment. JESD99C, 12/12

NOTE 1 A mask is usually used in order to remove only selected areas.

NOTE 2 By convention the wafer is mounted on the "hot" RF electrode.

read: (1) To transfer the configuration data from a programmable logic device (PLD) into a file. This process is similar to verification, except that the contents of the PLD are actually transferred to the programming system. JESD32, 6/96

(2) To acquire or to interpret data from a storage device, from a data medium, or from another source. (Ref. ANSI X3.172.) JESD100-B, 12/99

readability: A subjective measure of the ease with which a character or text may be read. JESD22-B114A, 5/11

read color register (RCR): A nonmemory cycle in which the contents of the color register are interrogated, with the results placed on the RAM data terminals, DQ(n). JESD21-C, 1/97

read disturb: The corruption of data caused by reading the memory. JESD100-B, 12/99

read latency (for an SDRAM): The number of clock cycles occurring between the registration of a read command and the active clock transition coincident with the availability of the first resultant output data. JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

read-only memory (ROM): A memory in which the contents are intended to be read only and not to be altered during normal operation. (Ref. IEC 748-2.) JESD21-C, 1/97# JESD100-B, 12/99

NOTE Unless otherwise qualified, the term "read-only memory" implies that the data content is determined by the structure of the memory and is unalterable.

read transfer (RT): A read operation in which the contents of one row of the memory array is transferred into the SAM data register in parallel. JESD21-C, 1/97

read-write mask register (RWR): A nonmemory cycle in which the contents of the write mask register are interrogated, with the results placed on the RAM data terminals, DQ(n). JESD21-C, 1/97

read/write memory: A memory in which cells associated with each address can be selected by applying appropriate electrical input signals and in which the stored data can be both sensed at appropriate output terminals and changed in response to other electrical input signals. (Adapted from IEC 748-2.) JESD100-B, 12/99

ready (RY): The output that, on some devices, signifies that no internal asynchronous operations are still in process and that the device is available for normal functions. This signal is normally implemented so that multiple devices can be OR-tied. This signal is the inverse of BY (i.e., RY = NOT BY). JESD21-C, 1/97

ready signal: A signal from a device to indicate to another device that (1) it is ready to send or receive data, or (2) the data transfer has been completed. (Ref. IEC 824.) JESD100-B, 12/99

real part of the small-signal open-circuit output admittance, common-emitter [$h_{oe(real)}$; Re(h_{oe})]: The ac rms collector current divided by the in-phase (real) component of the small-signal ac rms collector-emitter voltage and with the base terminal ac open-circuited. JESD10, 1/76# JESD77D, 8/12

real part of the small-signal short-circuit input impedance, common-emitter [$h_{ie(real)}$; Re(h_{ie})]: The in-phase (real) component of the small-signal ac rms base-emitter voltage divided by the ac rms base current with the collector-emitter voltage held constant. JESD10, 1/76# JESD77D, 8/12

NOTE The fact that the collector-emitter voltage is held constant implies that the collector terminal is open-circuited.

real-time soft error rate (RTSER); system soft error rate (SSER): The soft error rate in a naturally occurring alpha particle and neutron environment. JESD89A, 10/06 JESD89-1A, 10/07

NOTE 1 The RTSER is measured using a large number of devices to obtain a statistically significant error count, in contrast to an accelerated SER test, where a single device or a small number of devices is subjected to an intense radiation source.

NOTE 2 The RTSER would be increased at higher altitudes because of the greater neutron flux, but for the purposes of this document, the term "accelerated" is reserved for intense radiation sources that do not occur in natural terrestrial environments.

real zero: Synonym for "empty zero". JESD99C, 12/12

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Terms, abbreviations, letter symbols, and definitions	References
recall (1) **(on an NVRAM) (RC):** The input that transfers the nonvolatile data into the RAM array.	JESD21-C, 1/97
(2) **(of a product):** A public call by a manufacturer for the return of a product that may be defective or contaminated.	Merriam-Webster's Collegiate Dict.
recovered charge (Q_{rr}): The total amount of charge recovered from a diode, including the capacitive component of charge, when the diode is switched from a specified conductive condition to 1) a specified nonconductive condition, or 2) an unspecified nonconductive condition with the measurement ending after a specified integration time, t_I, with other circuit conditions as specified.	JESD77D, 8/12 JESD282-B, 4/00
recovery time, data-retention-mode: The time interval between the termination of the data-retention mode and the initiation of a read or write cycle. NOTE This interval is defined with respect to specified reference points on the supply-voltage and chip-enable waveforms.	JESD100-B, 12/99
recovery time, sense: The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.	JESD100-B, 12/99
recovery time, write: The time interval between the termination of a write pulse and the initiation of a new cycle, this time interval being provided for the memory to recover from a write operation and operate correctly. NOTE Write recovery time is the actual time interval between two signal events and is determined by the system in which the memory operates. A minimum value is specified that is the shortest interval for which correct operation of the memory is to be expected.	JESD100-B, 12/99
rectifier circuit element: One or more semiconductor rectifier diodes or rectifier stacks connected in series, in parallel, or both, to operate as a unit that is bounded by two circuit terminals and conducts current substantially in only one direction.	JESD282-B, 4/00
rectifier stack: An integral assembly of two or more rectifier diodes, including its associated housing and any integral mounting and cooling attachments.	JESD77D, 8/12 JESD282-B, 4/00
rectifying junction: A junction in a semiconductor device that exhibits asymmetrical conductance.	JESD77D, 8/12 JESD282-B, 4/00
reduced-instruction-set computer (RISC): A microcomputer or microprocessor that performs a single task per simple instruction, usually within a single clock cycle.	JESD100-B, 12/99
redundancy (in a memory): The provision of extra memory cells, usually rows or columns, that can be mapped into the memory array to replace defective (or nonconforming) cells. NOTE The mapping may be implemented by fuse, antifuse, or other programming techniques.	JESD100B.01, 12/02

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

reference noise temperature (T_0): A specified absolute temperature to be assumed as a noise temperature at the input ports of a network when calculating certain noise parameters and for normalizing purposes. (Ref. IEC 747-1.)

JESD77D, 8/12
JESD99C, 12/12
JESD311A, 11/81

NOTE A reference noise temperature of 290 K is considered to be standard in the USA.

reference packages or standards: Packages both with and without delamination, for use during equipment setup.

J-STD-035, 5/99

reference plane; regression plane: A least-squares fit of all the bottom-side or top-side measurement points on a package.

JESD22-B112A, 10/09

reference power supply (VREF): A power supply that acts as a reference for determining internal threshold voltages but does not supply any substantial power to the device.

JESD21-C, 1/97

reference voltage (of a voltage regulator) (V_{ref}): The voltage that is compared with the feedback sense voltage to control the regulator.

JESD99C, 12/12

reflectance: The ratio of luminous flux reflected from a surface to the luminous flux incident on that surface.

JESD22-B114A, 5/11

reflective acoustic microscope: An acoustic microscope that uses one transducer as both the pulser and the receiver.

J-STD-035, 5/99

NOTE This apparatus is also known as a pulse/echo system.

refresh (F): An input that, when true, causes the device to enter a data refresh mode.

JESD21-C, 1/97

refresh time interval: The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

JESD100-B, 12/99

NOTE The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is to be expected.

register: (1) A part of internal storage having a specified storage capacity and usually intended for a specific purpose. (Ref. IEC 824.)

JESD100-B, 12/99

(2) An arrangement of bistable circuits by means of which information may be accepted, stored, and retrieved. (Ref. IEC 748-2.)

NOTE The register may form part of another memory and is of a specified capacity.

registered and standard outlines: Outlines that are officially recorded by the JEDEC Type Registration System. The outlines are assigned JEDEC designations and published in JEDEC Publication No. 95.

RS-308-A, 8/81
Rescinded 5/09

registered PROM (RPROM): A PROM that contains a D-type register for the output data.

JESD21-C, 1/97

register-transfer-level (RTL) description: A hybrid between a behavioral description and a structural description at the level of clocked registers.

JESD12-1B, 8/93
JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

registration mark; alignment mark; fiducial mark: A mark, on a wafer or substrate, that is used for aligning successive processing masks. JESD99C, 12/12

regression plane: See "reference plane".

regression plane: A plane that (1) passes through the apex of the terminal that has the greatest perpendicular distance from the package substrate and (2) is parallel to the best-fit plane through the apexes of all terminals determined using the method of least squares. JESD22-B108B, 9/10

NOTE….The regression plane may be used to emulate the package coplanarity during reflow soldering at the point of surface mounting.

regulation: The absolute change in a parameter for a change of a circuit variable from one level to another level. JESD99C, 12/12

NOTE The change is usually normalized as a percentage but need not be normalized. The specific term should be "(circuit variable) regulation".

regulator [Zener] current, dc (I_Z): The dc reverse current through the diode when it is biased to operate in its breakdown region at an operating point between I_{ZK} and I_{ZM}. JESD211, 12/09

regulator [Zener] current at specified test point, dc (I_{ZT}): The dc reverse current through the diode when it is biased to operate in its breakdown region at a specified current between I_{ZK} and I_{ZM} for the purpose of specifying V_Z and Z_{ZT}. JESD211, 12/09

regulator [Zener] current at specified test point, rms component (I_{zt}): A specified rms current for measuring regulator impedance. JESD211, 12/09

NOTE According to JEDEC registration formats, this current should not exceed 10% of the simultaneously applied dc current I_{ZT}.

regulator [Zener] current near breakdown knee, dc (I_{ZK}): The dc reverse current through the diode when it is biased to operate in its breakdown region at a specified current near the breakdown knee. JESD211, 12/09

regulator [Zener] current near breakdown knee, rms component (I_{zk}): A specified rms current for measuring regulator impedance. JESD211, 12/09

NOTE According to JEDEC registration formats, this current should not exceed 10% of the simultaneously applied dc current I_{ZK}.

regulator [Zener] impedance (z_{zt}): The small-signal impedance of a diode when it is biased to operate in its breakdown region at I_{ZT} with a superimposed rms current of I_{zt}. JESD211, 12/09

regulator [Zener] knee impedance (z_{zk}): The small-signal impedance of a diode when it is biased to operate in its breakdown region at I_{ZK} with a superimposed rms current of I_{zk}. JESD211, 12/09

regulator [Zener] voltage (V_Z): The voltage across a diode at a specified current I_{ZT} in the breakdown region. JESD211, 12/09

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Terms, abbreviations, letter symbols, and definitions **References**

relative humidity (RH): The ratio of the amount of water vapor in the air to the maximum amount of water vapor that volume of air can hold at that temperature and pressure. JEP122G, 10/11

NOTE….RH is calculated as the quotient of the vapor density (or vapor pressure) in the air and the value of saturated vapor density (or saturated vapor pressure) at that specific temperature and pressure.

reliability: The ability of a product to perform a required function at or below a stated failure rate for a given period of time. JESD46D, 12/11

reliability qualification: The process of demonstrating that an entity is capable of meeting or exceeding the specified reliability requirements, usually by tests using accelerating conditions and proven models. JEP148A, 12/08

repeatability: The ability to consistently reproduce a given output. Repeatability involves the capabilities of an instrument, test, or process to produce the same output many times. Repeatability is considered interchangeable with the term "precision". Statistical techniques in conjunction with data taken from repeatability studies can be used to determine the process capability of an instrument, test, or process. JEP132, 7/98

repetitive peak forward current (I_{FRM}): The peak forward current including all repetitive transient currents but excluding all nonrepetitive transient currents. JESD77D, 8/12
JESD282-B, 4/00

repetitive peak reverse current (I_{RRM}): The peak reverse current including all repetitive transient currents but excluding all nonrepetitive transient currents. JESD77D, 8/12
JESD282-B, 4/00

repetitive peak reverse surge current (I_{ZRM}): The peak reverse current in the breakdown region including all repetitive transient currents but excluding all nonrepetitive transient currents. JESD211, 12/09

repetitive peak reverse voltage (V_{RRM}): The peak reverse voltage including all repetitive transient voltages but excluding all nonrepetitive transient voltages. JESD77D, 8/12
JESD282-B, 4/00

reportable application: The intended use of a product for which a material/substance content declaration is required. JIG-101 Ed 2.0, 4/09

NOTE This use is defined in the scope of the underlying law. Examples are batteries, textiles, wood, etc.

reproducibility: The variation in averages of measurements made by different operators using the same gauge when measuring identical characteristics of the same parts. Variation in measured averages may also be due to changes in the environment (temperature, humidity, etc.). JEP132, 7/98

reprogrammable read-only memory: A field-programmable read-only memory that can have the data content of each memory cell altered more than once. JESD100B.01, 12/02

NOTE This is a generic term and includes such devices as EEPROMs, EPROMs, and FEEPROMs.

requester: The person, employed by either the organization that uses the component in question (i.e., the customer) or the device manufacturer (e.g., in wafer fabrication), who initiates the request for a failure analysis. JEP134, 9/98

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Terms, abbreviations, letter symbols, and definitions	References
reserved (RSVD): In a family of standards where some devices in the family are subsets of others, terminals that are defined for some devices but not used for others. To allow for upgradeability, the unused terminals are reserved to prevent their being used. NC has often been used in similar situations.	JESD21-C, 1/97
reserved for future use (RFU): A terminal whose function is not currently defined, but that is intended to be defined in some future enhancement of JESD21-C. This terminal should not be used (either internally or externally) until it has been further defined.	JESD21-C, 1/97
reserved pin (of a memory card) (RFU): A pin that has been identified as "reserved for future use" and to which neither memory cards nor host systems shall make electrical connections.	JESD21-C, 1/97
reset (a counter): To cause a counter to take the state corresponding to a specified initial number. (Ref. IEC 824.)	JESD100-B, 12/99
resistance at failure (R_F): The value of the last recorded resistance of the test structure during the control cycle before the failure criterion, R_{FC}, is satisfied.	JEP119A, 8/03
resistor, bulk-collector: A semiconductor resistor formed by isolating a region of the epitaxial material that, in other regions, forms the collectors of the transistors.	JESD99C, 12/12
resistor, diffused: The normal semiconductor resistor formed by diffusing a junction-isolated region of proper length, width, and sheet resistance to provide the desired resistance value.	JESD99C, 12/12
resistor, film: A resistor formed by deposited films, usually metal, on an insulating substrate or the semiconductor oxide on an integrated-circuit chip surface.	JESD99C, 12/12
resistor, pinch: A semiconductor resistor formed by diffusing the opposite conductivity type, normally during the emitter diffusion, into a portion of the diffused resistor length in order to obtain a very high sheet resistance.	JESD99C, 12/12
resolution (1) **(general term):** The degree to which nearly equal values of a quantity can be distinguished or produced. NOTE 1 Resolution as a capability can be expressed in different forms (see "resolution, analog", "resolution, numerical", and "resolution, relative"). NOTE 2 Resolution is a design parameter and therefore has only a nominal value. NOTE 3 The terms for these different forms may all be shortened to "resolution" if no ambiguity is likely to occur (for example, when the dimension of the term is also given).	JESD99C, 12/12
(2) **(of an analog-to-digital converter):** The degree to which nearly equal values of the analog input quantity can be discriminated.	JESD99C, 12/12
(3) **(of a digital-to-analog converter):** The degree to which nearly equal values of the analog output quantity can be produced.	

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Terms, abbreviations, letter symbols, and definitions **References**

resolution, analog (of a linear or **nonlinear analog-to-digital converter [digital-to-analog converter]):** The nominal value of the step width [height]. JESD99C, 12/12

NOTE For a linear analog-to-digital converter [digital-to-analog converter], the constant magnitude of the analog resolution is often used as the reference unit LSB.

resolution, numerical (of an analog-to-digital converter or **a digital-to-analog converter):** The number (n) of digits in the chosen numbering system necessary to express the total number of steps. JESD99C, 12/12

NOTE 1 The numbering system is normally a binary or a decimal system.

NOTE 2 In the binary-coded-decimal numbering system, the term "2 digit" refers to an additional decimal digit with the highest positional value, but limited to the decimal figures "0" or "1" as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other "n" digits.

resolution, relative (of a linear analog-to-digital converter or **digital-to-analog converter):** The ratio of the analog resolution to the full-scale range (practical or nominal). JESD99C, 12/12

NOTE This ratio is normally expressed as a percentage of the full-scale range (% of FSR or % of FSR(nom)). For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

response surface methods: A procedure using a sequential combination of design of experiments (DOE) and regression analysis for determining factor settings that optimize a response. JEP132, 7/98

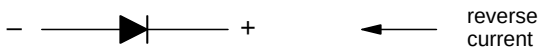
retention: The ability of a nonvolatile cell to retain data over time. JESD22-A117B, 3/09

retention failure: (1) A change of stored data by one or more bits, detected when the device is read in accordance with the data sheet specifications. JESD22-A117B, 3/09

(2) A data error occurring when a solid-state drive is read after an extended interval of time following the previous write. JESD218A, 2/11

retention time: The time interval between the instant data is stored and the instant the data can no longer be read correctly. JESD100-B, 12/99

reverse bias: The bias that tends to produce reverse current. JESD77D, 8/12



reverse-blocking diode thyristor surge protective device: A two-terminal thyristor surge protective device that exhibits a blocking state for positive cathode voltage. JESD77D, 8/12

reverse-blocking state: The state of a reverse-blocking or asymmetrical thyristor that corresponds to a reverse voltage between the origin and the beginning of the reverse breakdown region. JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

reverse-blocking triode thyristor surge protective device: A three-terminal (gated) thyristor surge protective device that exhibits a blocking state for positive cathode voltage. JESD77D, 8/12

reverse-conducting state: The state of a reverse-conducting triode thyristor that corresponds to the third quadrant of the characteristic. JESD77D, 8/12

reverse current (I_R): The current that flows from the external circuit into the cathode terminal at a specified reverse voltage (V_R) below the onset of breakdown. JESD77D, 8/12 JESD211, 12/09 JESD282-B, 4/00

reverse current (1) **(in a p-n junction):** The current flowing from the n-type region to the p-type region. JESD10, 1/76# JESD77D, 8/12

(2) **(in a semiconductor diode):** The current flowing from the external circuit into the cathode terminal. JESD77D, 8/12 JESD282-B, 4/00

reverse direction (1) **(general):** The direction of a (positive) reverse current. JESD77D, 8/12 JESD282-B, 4/00

(2) **(in an avalanche-junction transient voltage suppressor):** The direction of current that results when the n-type semiconductor region connected to one terminal is at a positive potential relative to the p-type region connected to the other terminal. JESD77D, 8/12

NOTE Any capacitance-reduction diodes that may be included shall be ignored in the determination of reverse direction.

(3) **(in a semiconductor junction, excluding backward and tunnel diodes):** The direction of higher resistance to steady direct-current flow through a semiconductor junction. JESD10, 1/76

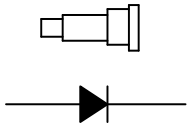
reverse gate current (I_{GR}): The direct current into the gate terminal with a reverse gate-source voltage applied. JESD24, 7/85 JESD77D, 8/12

reverse gate current, drain short-circuited to source (1) **(of an insulated gate field-effect transistor) (I_{GSSR}):** The direct current into the gate terminal with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal. JESD24, 7/85 JESD77C, 10/0

(2) **(of a junction-gate field-effect transistor) (I_{GSS}):** The direct current into the gate terminal with the gate terminal reverse-biased with respect to the source terminal and the drain terminal short-circuited to the source terminal. JESD24, 7/85 JESD77D, 8/12

reverse period (of a rectifier circuit element): The parts of an alternating-voltage cycle during which reverse voltage appears across the rectifier circuit element. JESD282-B, 4/00

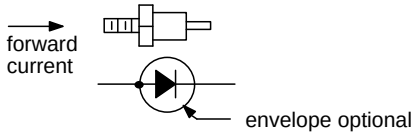
reverse-polarity (microwave) diode: A microwave diode in which the cathode is connected to the base (i.e., the larger-diameter terminal) of the package. JESD77D, 8/12



The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

reverse-polarity rectifier diode with heat sink: A rectifier diode whose anode is connected to the mounting stud or heat sink. JESD77D, 8/12



reverse power dissipation: The power dissipation resulting from reverse current. JESD77D, 8/12
JESD282-B, 4/00

reverse recovery current: The transient reverse current associated with a change from forward current to a reverse condition. JESD77D, 8/12
JESD282-B, 4/00

reverse recovery current fall time (t_{rrf}, t_b): The portion of the reverse recovery time interval after the reverse recovery current has reached its maximum (peak) value. JESD77D, 8/12
JESD282-B, 4/00

reverse recovery current rise time (t_{rrr}, t_a): The portion of the reverse recovery time interval prior to the instant when the reverse recovery current reaches its maximum (peak) value. JESD77D, 8/12
JESD282-B, 4/00

reverse recovery softness factor (RRSF): The absolute value of the ratio of (1) di_{RR}/dt (the rate of rise of the reverse recovery current) when the current is passing through zero at the beginning of the reverse recovery time, to (2) di_{RF}/dt (the maximum value of the rate of fall of the reverse recovery current) after the current has passed through its peak value, I_{RM}. JESD77D, 8/12
JESD282-B, 4/00

NOTE The ratio of reverse recovery current fall time (t_b) to the reverse recovery current rise time (t_a) has been called "recovery softness factor" (RSF); however, RRSF is a more useful measure of the diode softness characteristic.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

reverse recovery time (t_{rr}): The time interval between the instant when the current passes through zero when changing from the forward direction to the reverse direction and, after reverse current reaches its peak value $I_{RM(REC)}$, the instant when

JESD41, 5/95#
[Includes only alternative 3]
JESD77D, 8/12
JESD282-B, 4/00

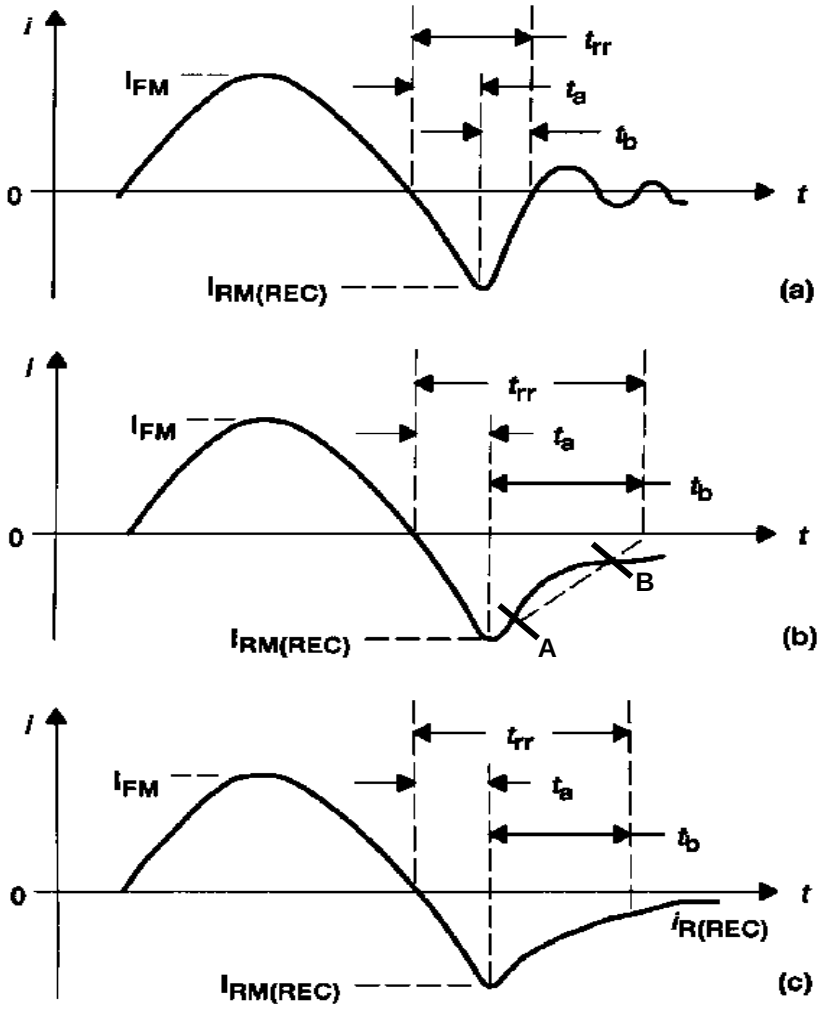
1) the reverse current first intersects the zero-current axis as shown in Figure (a) below, or

2) the extrapolated reverse current reaches zero, as shown in Figure (b) below, or

3) the reverse current reaches a specified low value $I_{R(REC)}$, as shown in Figure (c) below.

NOTE 1 In alternative 2, the extrapolation is carried out with respect to specified points "A" and "B", as shown in generalized form in Figure (b). Point "A" may be specified at a value other than $I_{RM(REC)}$.

NOTE 2 IEC 747-2 includes only alternatives 2 and 3.



Current waveforms during rectifier diode reverse recovery

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

reverse voltage (V_R) (1) **(across a p-n junction):** The voltage between the n-type region and the p-type region when the n-type region is at a positive voltage relative to the p-type region. JESD77D, 8/12

(2) **(across a semiconductor diode):** A positive cathode-anode voltage. JESD77D, 8/12 JESD282-B, 4/00

(3) **(across a voltage regulator diode):** The positive cathode-anode voltage that is specified as a test condition for reverse current (I_R). JESD211, 12/09

rework: (1) The repetition of any operation or process step or sequence that creates or changes a portion of the device's structure, assembly, testing, or packing. JESD50B.01, 11/08

(2) The intentional execution of operations not normally part of the manufacture of the item. JESD50B.01, 11/08

(3) The removal of a component for scrap, reuse, or failure analysis; the replacement of an attached component; or the heating and repositioning of a previously attached component. J-STD-033C, 2/12

rework: To process again or renew for reuse or acceptability. JESD9B, 5/11

RFU: See "reserved for future use" and "reserved pins".

RG: See "attribute memory select".

RH: See "relative humidity".

RHA: See "radiation-hardness assurance/radiation-hardness assured".

RHACL: See "radiation-hardness assured capability level".

RIE: See "reactive ion etching".

ringing: A high-frequency oscillation superimposed on a waveform. JS-001-2012, 4/12

ripple current: The alternating component whose instantaneous values are the difference between the average and instantaneous values of a pulsating unidirectional current. JESD282-B, 4/00

ripple voltage: The alternating component whose instantaneous values are the difference between the average and instantaneous values of a pulsating unidirectional voltage. JESD282-B, 4/00

ripple current, percent: The ratio, in percent, of the effective (root-mean-square) value of the ripple current to the average value of a pulsating unidirectional current. JESD282-B, 4/00

ripple rejection (of a voltage regulator) (k_{VIO}): The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage. JESD99C, 12/12

ripple time (t_{rip}): For a step-function change of the input signal level, the time interval between the end of the rise time or fall time and that instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\varepsilon$) containing the final output signal level. (Ref. IEC 747-3.) JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

ripple voltage, percent: The ratio, in percent, of the effective (root-mean-square) value of the ripple voltage to the average value of a pulsating unidirectional voltage. JESD282-B, 4/00

RISC: See "reduced-instruction-set computer".

rise time (t_r) (1) **(general):** The time interval between one reference point on a waveform and a second reference point of greater magnitude on the same waveform. JESD77D, 8/12

NOTE The first and second reference points are usually 10% and 90%, respectively, of the steady-state amplitude of the waveform existing after the transition, measured with respect to the steady-state amplitude existing before the transition.

(2) **(of an analog integrated circuit):** For a step-function change of the input signal level, the time interval between the end of the delay time (normally 10%) and that instant at which the magnitude of the output signal first passes through a specified value (normally 90%) close to its final value. (Ref. IEC 747-3.) JESD99C, 12/12

(3) **(of a digital integrated circuit):** Synonym for "transition time, low-to-high level". JESD99C, 12/12
JESD100-B, 12/99

(4) **(of a transistor):** (A) The time interval during which the amplitude of the leading edge of a pulse increases from 10% to 90% of its maximum amplitude. JESD10, 1/76

(B) Synonym for "current rise time, t_{ri}". JESD77D, 8/12

rise time charge (Q_{rrr}): That part of the recovered charge that is recovered from the diode during the reverse recovery rise time. JESD77D, 8/12
JESD282-B, 4/00

NOTE The time intervals t_{rrf} and t_{rrr} are defined so that their sum is equal to the reverse recovery time t_{rr}, whereas the recovered charge Q_{rr} is defined for an integration time t_i. As a consequence, the sum of the partial charges Q_{rrf} and Q_{rrr} will differ from Q_{rr} unless t_{rr} equals t_i.

risk and opportunity assessment process: The systematic procedure intended to: 1) proactively avoid problems such as unfulfilled requirements, demands, and expectations; 2) take advantage of capabilities (opportunities) that may exceed the requirements for a given approach; and 3) initiate appropriate measures to exploit opportunities and avoid, reduce, or prevent risks to the user. JEP148A, 12/08

risk priority number (RPN): A parameter to measure the rating of risks. JEP131B, 4/12

robust estimation: A procedure for estimating statistics, e.g., mean and variance, that performs well when there are departures (outliers) from the ideal conditions that have been postulated for the model. JESD50B.01, 11/08

NOTE The estimate of the sample mean and/or variance is often made robust by a rejection-of-outliers procedure or the use of a trimmed mean.

robust mean [robust variance]: A mean [variance] calculated using a robust estimation procedure. JESD50B.01, 11/08

robustness: The capability of functioning correctly or not failing under varying application and production conditions. JEP148A, 12/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

robust (procedure): A procedure that remains in control and capable within the expected variations of inputs. JEP132, 7/98

RoHS: Acronym for the European directive 2002/95/EC *Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment.* JESD97, 5/04 Rescinded 5/07

NOTE RoHS directive 2002/95/EC itself is not a law; rather, it is a direction to the European Union Member States to implement their own laws embodying the requirements of the directive. These laws were required to be in effect as of July 1, 2006. (Ref. J-STD-609.)

roll-over error (of an analog-to-digital converter with decimal output and **autopolarity) (E_{RO}):** The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale). JESD99C, 12/12

ROM: See "read-only memory".

root cause: (1) The primary source of the failure mechanism or cause of an administrative problem. JESD671B, 6/12

(2) See "failure cause". JEP143C, 7/12

EDITOR'S NOTE If that statement in JEP143 implies "root cause" and "failure cause" are synonyms, that implication is wrong. See note 3 to "failure mode".

root cause analysis: The structure procedures for determining the failure cause. JEP143C, 7/12

row address input (RA): In an address-multiplexed DRAM, the address field that is captured by the row-enable signal, RAS. When the numbering of the row-address numbering is significant for device operation, the RA inputs are numbered beginning with 0. JESD21-C, 1/97

row enable input (RAS; RE): A chip enable signal that, on certain dynamic RAMs, actuates only row-address-oriented internal circuitry. In modules that have multiple RAS inputs, the RAS inputs are numbered beginning with 0. JESD21-C, 1/97

RPN: See "risk priority number".

RPROM: See "registered PROM".

RRRF: See "reverse recovery softness factor".

RR/RW: See "RAM read/write, no mask".

RSVD: See "reserved".

RT: See "read transfer".

RTSER: See "real-time soft error rate".

run: A number of consecutive points, usually seven or eight, above or below the centerline. EIA-557-B, 2/06

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

run chart: A time-ordered graphic representation of a characteristic of a process showing plotted values of some statistic gathered from the process and a central line that can be analyzed for runs. EIA-557-B, 2/06

RWNM: See "RAM write with new mask".

RWOM: See "RAM write with old mask".

RWR: See "read-write mask register".

RY: See "ready".

S

S, s: See "source terminal".

SA; SAn: See "sync address".

SAC: A type of lead-free solder made from tin, silver, and copper (S stands for Sn, A for Ag, and C for Cu). (Ref. IPC-7095B) JESD217, 9/10

SAM: See "serial-access memory".

sample: A set of individuals taken from a population. EIA-557-B, 2/06
JESD659B, 2/07

sample holder: A device intended to position the samples in the proper place, keep the samples from moving during the scan, and maintain planarity. J-STD-035, 5/99

sample period: The period of time selected by the manufacturer to accumulate data for the calculation and reporting of average outgoing quality (AOQ). JESD16-A, 4/95

sample window time: The length of the time interval during which a condition-sensitive parameter is measured after the condition is removed. JESD51-1, 12/95#
JESD51-13, 6/09#

saturated cross section; limiting cross section: The maximum observable cross section. JESD57, 12/96

NOTE On many softer devices, the saturated, i.e., limiting, cross section appears as the asymptotic upper section of the linear-energy-transfer (LET) vs cross-section curve. An additional increase in LET will not increase the cross section of the device. On harder devices, the cross section may not reach saturation.

saturation: A base-current and a collector-current condition resulting in a forward-biased collector junction. JESD10, 1/76
JESD77D, 8/12

saturation drain current ($I_{D(sat)}$): The drain current measured when the transistor is biased in the saturation region. JESD28-A, 12/01
JESD60A, 9/04
JESD90, 11/04

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

saturation input signal (1) **(for analog signal applications of a charge-transfer device):** The maximum input signal or illumination power that can be transferred with a specified degree of linearity. JESD99C, 12/12

(2) **(for digital signal applications of a charge-transfer device):** The input signal or illumination power that is required to produce full-well-capacity charge packets. JESD99C, 12/12

saturation output signal (for digital signal applications of a charge-transfer device): The output signal that is produced by full-well-capacity charge packets. JESD99C, 12/12

saturation region (of a field-effect transistor): The region of the drain voltage-current characteristic curve in which a change in drain-source voltage causes a relatively small change in drain current. JESD24, 7/85
JESD77D, 8/12

saturation voltage, base-emitter ($V_{BE(sat)}$): The voltage between the base and emitter terminals for specified base-current and collector-current conditions that are intended to ensure that the collector junction is forward-biased. JESD10, 1/76
JESD77D, 8/12

saturation voltage, collector-emitter ($V_{CE(sat)}$): The voltage between the collector and emitter terminals under conditions of base current or base-emitter voltage beyond which the collector current remains essentially constant as the base current or voltage is increased. (Ref. IEC 747-7.) JESD10, 1/76#
JESD77D, 8/12

NOTE This is the voltage between the collector and emitter terminals when both the base-emitter and base-collector junctions are forward-biased.

SBx: See "sync byte 'x' write enable".

SC: See "serial clock".

scan cell: A bistable element that includes one or more ports used to observe and control that element's state when the port or ports are enabled. JESD12-1B, 8/93
JESD99C, 12/12

scan, full: A methodology of design in which every bistable element is a scan cell. JESD12-1B, 8/93
JESD99C, 12/12

scan insertion: The conversion of bistable elements into scan cells. JESD12-1B, 8/93
JESD99C, 12/12

scan, partial: A methodology of design in which some, but not all, bistable elements are scan cells. JESD12-1B, 8/93
JESD99C, 12/12

scatter diagram: A graph of the value of one characteristic versus another characteristic. EIA-557-B, 2/06

SCCD: See "surface-channel charge-coupled device".

schematic capture: Use of a computer system to enter a graphical representation of the functional blocks and the interconnections of a circuit. JESD12-1B, 8/93
JESD99C, 12/12

Schmitt trigger: A digital circuit designed to have significant hysteresis, i.e., the difference between the positive-going and negative-going input threshold voltages, and usually having only one input. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
Schottky-barrier charge-coupled device: A buried-channel charge-coupled device that uses a Schottky barrier junction to isolate the transfer gate.	JESD99C, 12/12
Schottky diode: See "diode, Schottky".	
SCR: See "semiconductor controlled rectifier".	
scrape (on a package): A location where material has been removed or displaced. NOTE Burnishes and rub marks where material is not displaced are not considered as scrapes. Tool marks in the basis metal, uniformly covered by plated or deposited metal, are not considered as pits or scrapes.	JESD27, 8/93# Rescinded 5/11
scratch (1) **(on a package):** A slight injury, mar, or mark, usually thin and shallow, caused by scratching.	JESD9B, 5/11
(2) **(on a wafer or die):** A visual anomaly consisting of a line or series of lines caused by abrasion.	JESD22-B118, 3/11
scratch-pad memory: A read/write memory (RAM) device or register that is used to temporarily store intermediate results (data) or memory addresses (pointers).	JESD100-B, 12/99
screen-printing (of a thick-film circuit): The deposition of conductive, resistive, or insulating films onto a substrate by pressing pastes ("inks") through screens.	JESD99C, 12/12
SCSOA: See "short-circuit safe operating area".	
scuff: A visual anomaly having a rough appearance caused by abrasion.	JESD22-B118, 3/11
SDQ(n)(x): See "serial data input/output".	
SDRAM: See "synchronous dynamic random-access memory".	
SE: See "serial port enable" and "sync enable".	
seal, ceramic-to-metal: The ceramic material metallized at the package and lead interfaces and brazed to the package and the lead. The ceramic holds the lead in place in the package, creates a hermetic seal, and electrically isolates the lead from the package.	JESD9B, 5/11
seal (critical) area: The package-to-insulator seal hole edge or sealing surface on either the package or the cover where the package and cover are soldered, seam-welded, projection-welded, etc. together and create a hermetic seal.	JESD9B, 5/11
seal, glass-to-metal: The glass material, typically matched glass or compression glass, that surrounds the lead, holds the lead in place in the package, and electrically isolates the lead from the package creating a hermetic seal.	JESD9B, 5/11
seated height (of a package): The distance from the seating plane to the top of the body including any protrusions or rigid terminals. Flexible terminals are not included in determining the seated height.	RS-308-A, 8/81 Rescinded 5/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

seating plane (1) **(of a package, general):** The reference plane that designates the interface between the package or its terminals and the surface on which it is mounted. EIA308-A, 8/81 Rescinded 5/09

(2) **(of a surface-mounted device):** The plane formed by the three terminal apexes that exhibit the greatest perpendicular distance from the package substrate, provided that the triangle formed by those three apexes encompasses the projection of the center of gravity (CoG) of the component. JESD22-B108B, 9/10

SEB: See "single-event burnout".

secondary threshold crossing (of a clock signal): The threshold crossing of a clock signal indicating the second part of the clock cycle. JESD65B, 9/03

second breakdown: A condition of a transistor, resulting from a lateral current instability, in which the electrical characteristics are determined principally by the spreading resistance of a thermally maintained current constriction. The initiation of second breakdown is observed as a decrease in the voltage sustained by the collector. JESD10, 1/76

NOTE Second breakdown differs from thermal failure in that its initiation cannot be predicted from low-voltage thermal-resistance measurements. Unless the current and duration in second breakdown are limited, the high junction temperature at the current constriction will result in failure, usually as a collector-to-emitter short circuit. Second breakdown can occur at positive, negative, or zero base current.

second-breakdown trigger current (I_{t2}): The amount of current at the point in time when a transistor enters its second-breakdown region under ESD pulse conditions and is irreversibly damaged. JEP155A.01, 3/12# JEP157, 10/09

second-level assembly: The attachment of a component to the next level of assembly packaging. JEP150, 5/05 JEP156, 3/09 JEP158, 11/09

second-level interconnect: The connection made by attaching a component to a printed circuit board. J-STD-609A.01, 2/11

NOTE This connection is external to the component, not internal.

second-level interconnect component label: A label placed on boxes and bags that contain components with either Pb-containing or Pb-free terminal materials/finishes. J-STD-609A.01, 2/11

NOTE This label includes the material category and maximum component temperature.

second-level interconnect terminal finish/material: The material at the component second-level termination. J-STD-609A.01, 2/11

NOTE Depending on the component type, this material could refer to the terminal finish or ball material.

sector: Synonym for "block". JESD100-B, 12/99

SEE: See "single-event effect".

SEFI: See "single-event functional interrupt".

SEGR: See "single-event gate rupture".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

SEL: See "single-event latch-up".

semiconductor (nonspecific): A substance whose conductivity due to the charge carriers of both signs is normally in the range between that of metals and that of insulators and in which the charge carrier density can be changed by external means. JESD77D, 8/12 JESD99C, 12/12

semiconductor controlled rectifier (SCR); silicon controlled rectifier (SCR): Synonyms for "thyristor, reverse blocking triode". JESD77D, 8/12

semiconductor device (general term)**:** A device whose essential characteristics are due, in whole or in part, to the flow of charge carriers within a semiconductor. JESD10, 1/76 JESD77D, 8/12 JESD99C, 12/12 JESD282-B, 4/00#

NOTE For specification purposes, a semiconductor device must be considered to be either a discrete semiconductor device or an integrated circuit.

semiconductor diode: A semiconductor device having two electrodes and exhibiting a nonlinear voltage-current characteristic; in more restricted usage, a semiconductor device that has the asymmetrical voltage-current characteristic exemplified by a single p-n junction. (Ref. IEEE Std 100.) JESD77D, 8/12

semiconductor junction: See "junction (in a semiconductor device)".

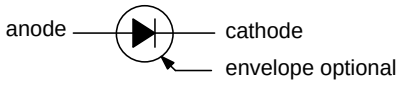
semiconductor (material) (within a semiconductor device): A material in which the electric current is made up of both negative and positive mobile charge carriers (i.e., conduction electrons and holes, respectively). JESD77D, 8/12 JESD99C, 12/12

semiconductor rectifier diode: A semiconductor diode intended to be used for current and voltage rectification. JESD77D, 8/12 JESD282-B, 4/00

NOTE 1 The term "semiconductor rectifier diode" includes the associated housing and any integral mounting and cooling attachments.

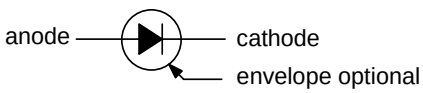
NOTE 2 The term "rectifier cell" is sometimes used as a synonym for "rectifier diode" when the diode is an element of a rectifier stack.

Graphic symbol (ref. IEEE Std 315):



semiconductor signal diode: A semiconductor diode intended to be used for signal processing. JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

sensitive volume: A region, or multiple regions, in which the charge imparted by incident radiation is collected and can then change the state of a node. JESD57, 12/96# JESD89A, 10/06#

NOTE The sensitive volume is dependent on the angle of incident particle radiation, the mass and energy of incident particle radiation, and the density and type of material in the volume being penetrated by the incident radiation.

sensitivity: (1) The degree to which a process metric or output responds to the stimulation of an input. JEP132, 7/98

(2) The change in a parameter divided by the change in a circuit variable other than temperature. JESD99C, 12/12

NOTE This quotient is the average value over the total change of the circuit variable. The change in the parameter may or may not be normalized to a reference value of the parameter. The specific term should be "(circuit variable) sensitivity".

sequential fault: A functional fault that is affected by the sequence of the input stimuli. JESD12-5, 8/88

sequential logic function: A logic function in which there exists at least one combination of input states for which there is more than one possible resulting combination of states at the outputs. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

NOTE The outputs are functions of variables in addition to the present states of the inputs, such as time, previous internal states of the element, etc.

SER: See "soft error rate".

serial-access memory (SAM): (1) A memory (or serial port in a multiport memory) in which data is accessed sequentially and the time for access depends on the location of the data desired. In a multiport memory, this term refers to that portion of the device that is related to the serial-access port and its associated functions. JESD21-C, 1/97

(2) A memory in which data can be accessed only in a predetermined sequence. (Adapted from IEC 748-2.) JESD100-B, 12/99

serial clock (SC): An input, on devices having a serial data access port, that actuates the serial transfer of data, either in or out. JESD21-C, 1/97

serial data input/output [SDQ(n)(x)]: On a device having a serial data access port, the pins that serve as serial data output(s) when in the read mode and as serial data input(s) when in the write mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data input/outputs is significant for device operation, the serial data input/outputs are numbered beginning with 0. For devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc. JESD21-C, 1/97

serial data output [SQ(n)]: On a device having a serial data access port, the pins that serve as serial data output(s) when in the read mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data outputs is significant for device operation, the serial data outputs are numbered beginning with 0. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

serial operation: A processing mode in which two or more operations are performed sequentially or consecutively in a single device. (Adapted from ANSI X3.172.) JESD100-B, 12/99

NOTE Contrast with parallel operation.

serial port enable (SE): The input that, when true, actuates the device's serial-access circuitry. JESD21-C, 1/97

serial port output enable (SG): The input that, when true, actuates the device's serial data output circuitry. JESD21-C, 1/97

serial transmission: The sequential transmission of bits on a single channel or bus line. JESD100-B, 12/99

series control element (series pass element): A circuit element (usually a transistor), in series with the load, that controls the output voltage by dropping a variable portion of the input voltage. JESD99C, 12/12

service rating: An assessment of the metrics established to evaluate the supplier's commitment to servicing the customer. JEP146A, 1/09

settling time (of an analog integrated circuit): Synonym for "total response time". JESD99C, 12/12

settling time, analog (of a digital-to-analog converter) (t_{sa}): The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value. JESD99C, 12/12

settling time, digital (of a linear or **a multiplying digital-to-analog converter) (t_s** or **t_{sd}):** The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value. JESD99C, 12/12

NOTE For a multiplying digital-to-analog converter, the full term and the additional subscript *d* must be used to distinguish between the digital and the reference settling times.

settling time, reference (of a multiplying digital-to-analog converter) (t_{sr}): The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value. JESD99C, 12/12

NOTE Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.

settling time to steady-state ramp (of a multiplying digital-to-analog converter) ($t_{s(ramp)}$): The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output. JESD99C, 12/12

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Terms, abbreviations, letter symbols, and definitions **References**

setup time (t_{su}): The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal. JESD99C, 12/12 JESD100-B, 12/99

NOTE 1 The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

NOTE 2 The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

SEU: See "single-event upset".

SG: See "serial port output enable" and "sync output enable".

SGRAM: See "synchronous graphics DRAM".

SGW: See "sync global write".

shadow (of a package): The maximum overall dimensions on the board that would be occupied by the package. For the ball-grid array package, the shadow is the substrate size. For a quad flat package, the shadow is the lead-tip-to-lead-tip size. JESD51-8, 10/99

shadow moiré: Referring to an optical noncontact method to measure warpage using a moiré fringe pattern resulting from the geometric interference between a flat reference grating and the projected shadow of the grating on a warped test object. JESD22-B112A, 10/09

shape: A general concept for the overall pattern formed by a distribution of values. EIA-557-B, 2/06

SHE: See "single-event hard error".

shear (force) (1) **(general):** Internal force tangential to the section on which it acts. Merriam-Webster's Collegiate Dict.

(2) **(applied to a BGA solder ball):** The force applied to a BGA solder ball in a direction parallel to the device planar surface JESD22-B117A, 10/06

shear tool: A rigid tool that presses directly against the solder ball during shearing. JESD22-B117A, 10/06

NOTE….The shear tool is integrated with a sensing element so that shear force can be measured.

shear tool; shear arm: A tungsten carbide, or equivalent, chisel with specific angles on the bottom and back of the tool to ensure a shearing action. JESD22-B116A, 8/09

sheet resistance: The electrical resistance of a diffused layer or of a thin sheet of material with uniform thickness as measured across opposite sides of a square pattern. JESD99C, 12/12

NOTE Sheet resistance is usually expressed in ohms per square.

shelf life: The minimum time that a dry-packed moisture-sensitive device can be stored in an unopened moisture-barrier bag (MBB) such that a specified interior bag ambient humidity is not exceeded. J-STD-033C, 2/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
shipping environment: The temperature and relative humidity to which a component is exposed while being shipped.	JESD94A, 7/08
shock and vibration condition: The shock and vibration experienced by an application in manufacturing, shipment, operation, and user handling (user transportation and/or regular operation).	JESD94A, 7/08
short circuit: A circuit having a terminating impedance sufficiently low that doubling its magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.	JESD10, 1/76 JESD77D, 8/12
short-circuit current limit (of a voltage regulator) (I_{OS}): The output current of the regulator with the output shorted to ground.	JESD99C, 12/12
short-circuit fault: A fault that alters the number of nodes of a circuit by connecting two or more nodes together.	JESD12-5, 8/88
short-circuit input capacitance, common source (C_{iss}): The capacitance between the input terminals (gate and source) with the drain short-circuited to the source for alternating current.	JESD24, 7/85 JESD24-11, 8/96#
short-circuit output capacitance, common source (C_{oss}): The capacitance between the output terminals (drain and source) with the gate short-circuited to the source for alternating current.	JESD24, 7/85
short-circuit output current (I_{OS}) (1) **(of a digital integrated circuit):** The current into an output terminal when the output is short-circuited to ground with input conditions applied that, according to the product specification, will establish the output logic furthest from ground potential.	JESD99C, 12/12
(2) **(of an analog integrated circuit):** The output current with the output shorted to ground or other specified point.	JESD99C, 12/12
short-circuit reverse transfer capacitance, common source (C_{rss}): The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three-terminal bridge.	JESD24, 7/85
short-circuit safe operating area (SCSOA): All combinations of collector current and collector-emitter voltage that are permitted to occur during nonrepetitive turn-off of short-circuit current in the transistor without endangering its survival. NOTE 1 This information is normally presented graphically. NOTE 2 The SCSOA is defined for nonrepetitive operation. This means that it applies for a limited number of occurrences in the life of a device and that all equilibrium conditions must be reestablished before a second occurrence.	JESD77D, 8/12
short-circuit withstand time (t_{sc}): The time interval between the instant when the device drive rises to 50% of its peak value and the instant when it falls to 50% of its peak value.	JESD24-9, 8/92

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

shorted non-supply terminal; shorted non-supply pin: A non-supply terminal (typically an I/O terminal) that is metallically connected (typically less than 3 ohms) on the chip or within the package to another non-supply terminal (or set of non-supply terminals). JS-001-2012, 4/12

short-term capability: The process capability under controlled conditions over a brief period of time. EIA-557-B, 2/06

shutdown current (of a voltage regulator) ($I_{L(sd)}$ and $I_{O(sd)}$): The load current available during the shutdown mode. JESD99C, 12/12

shutdown mode (of a voltage regulator): A condition in which the series control element of the regulator is turned off. JESD99C, 12/12

NOTE This is an optional feature usually employed for remote control.

sidewall: One of the walls of a package creating a cavity. JESD9B, 5/11

NOTE Sidewalls are typically brazed to a base of similar material or a solid block of material is machined to create a cavity with solid sidewalls.

signal, analog: A signal that is used in such a manner that any change in magnitude of some characteristic conveys information. JESD99C, 12/12

NOTE The characteristic may be the amplitude, phase, frequency, etc., of a quantity such as voltage, current, impedance, etc.

signal charge (in a charge-transfer device): A quantity of electric charge representing the signal. JESD99C, 12/12

signal, digital: A signal that is used in such a manner that changes between ranges in a finite set of nonoverlapping ranges of the magnitude of some characteristic convey information. JESD99C, 12/12

NOTE 1 The characteristic may be the amplitude, phase, frequency, etc., of a quantity such as voltage, current, impedance, etc.

NOTE 2 For convenience, each range of values can be represented by a single value, i.e., the nominal value.

signature (of a failure): The necessary and sufficient information about a failure that establishes a strong relationship between failure characteristics and failure mechanism. JEP136, 7/99

NOTE 1 This necessary and sufficient information can include emission microscopy results, morphology data, test data, IV-curves, environmental history, etc., and therefore can be either electrical or physical in nature.

NOTE 2 The scope of application can be time-based, lot-based, package-based, design-based, etc.

signature analysis (SA): The process of assigning the most likely failure mechanism to a countable failure based on its unique electrical failure characteristics and an established physical analysis database for that mechanism. JEP136, 7/99#
JEP143C, 7/12
JESD74A, 99#

NOTE The objective is to reduce the number of comprehensive failure analyses.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

silicon carbide varistor: A varistor having a silicon carbide element. JESD77D, 8/12

NOTE The device exhibits a symmetrical voltage-current characteristic.

silicon-compiled integrated circuit: An integrated circuit generated entirely by a silicon compiler. JESD12-1B, 8/93
JESD99C, 12/12

silicon compiler: A design automation system that, when given a high-level description (behavioral, register transfer level, etc.) of desired functionality, will generate sufficient information for manufacture and verification of an integrated circuit design. JESD12-1B, 8/93
JESD99C, 12/12

silicon-gate-insulator-semiconductor (SIS) technology: A technology similar to metal-insulator-semiconductor (MIS) technology except that the gate is silicon instead of metal. JESD99C, 12/12

silicon-nitride-oxide-semiconductor (SNOS) technology: A subcategory of silicon-gate-insulator-semiconductor (SIS) technology in which the insulation employed is a nitride-oxide layer. JESD99C, 12/12

silicon-on-sapphire (SOS) technology: The technology whereby monocrystalline films of silicon are epitaxially deposited onto a single-crystal sapphire substrate to provide the basic structure for the fabrication of dielectrically isolated active and/or passive elements. JESD99C, 12/12

silicon-oxide-nitride-oxide-semiconductor (SONOS) technology: A subcategory of silicon-gate-insulator-semiconductor (SIS) technology in which the insulation employed is an oxide-nitride-oxide layer. JESD99C, 12/12

silo memory: Preferred term is “first-in, first-out memory”. JESD100-B, 12/99

similar devices: For the purpose of periodic sample testing and design qualification, devices that meet any of the following conditions: JESD93, 9/05

— they are designed and manufactured with the same basic process flow, using the same or fewer fabrication and assembly processes and materials as a primary parent device type;

— they are assembled with the same active elements and the same passive elements, using no greater quantity of either;

— they are subject to the same process and material control monitoring, e.g., device screening, process control, reliability assessment, etc.;

— they are designed to generate the same or fewer functions using the same or less functional circuitry; e.g., a 4-bit A/D converter may be considered to be similar to a 10-bit A/D converter, but not vice versa.

similarity acceptance, surface finish: Acceptance of a change to a surface finish manufacturing process based upon similarity and data available from previous tin whisker *technology acceptance* (q.v.) and *manufacturing process change acceptance* (q.v.) tests. JESD201A, 8/08

SIMM: See “single-in-line-memory-module”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

simple daisy chain: A daisy chain consisting of a single series of bumps in a chain. JEP154, 1/08

NOTE A current through the series of bumps will alternate in direction in successive bumps. The number of bumps where electrons flow out of the die and the number of bumps where electrons flow into the die are equal.

simultaneously switching outputs: Multiple output buffers that change state within a defined short time interval. JESD12-1B, 8/93
JESD99C, 12/12

simultaneous surge: An impulse current pulse applied simultaneously to multiple terminals of a single-chip ABD array. JESD77D, 8/12
JESD210, 12/07

NOTE A simultaneous surge test may be used to determine the worst-case impulse current through an array of p-n junction ABDs having a common chip connection where current crowding may cause a failure or degradation of the device.

single-chip integrated circuit: See "integrated circuit, single-chip".

single-chip microcircuit: Synonym for "integrated circuit, single-chip".

single-ended input voltage (V_{IS}): The signal voltage that is applied to one input of a differential amplifier with the other input terminal at signal ground. JESD99C, 12/12

single-ended input voltage range (V_{ISR}): The range of single-ended input voltage that, if exceeded at any input terminal, will cause the total harmonic distortion of the output signal resulting from the single-ended input to exceed a specified maximum value. JESD99C, 12/12

single-ended output voltage (V_{OS}): The signal voltage between one output terminal and ground of a circuit having differential outputs. JESD99C, 12/12

single-event burnout (SEB): An event in which a single energetic-particle strike induces a localized high-current state in a device, resulting in catastrophic failure. JEP133C, 1/10
JESD57, 12/96#
JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

single-event effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from the passage of a single energetic particle. JEP133C, 1/10
JESD57, 12/96#
JESD89A, 10/06
JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

NOTE Single-event effects include single-event upset (SEU), single-bit upset (SBU), multiple-bit SEU (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR).

single-event functional interrupt (SEFI): A soft error that causes the component to reset, lock up, or otherwise malfunction in a detectable way but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL) or single-event burnout (SEB). JESD57, 12/96#
JESD89A, 10/06
JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

NOTE An SEFI is often associated with an upset in a control bit or register.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

single-event gate rupture (SEGR): An event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET. JEP133C, 1/10 JESD57,12/96# JESD89-1A, 10/07 JESD89-2A, 10/07 JESD89-3A, 11/07

NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

single-event hard error (SHE): An irreversible change in operation resulting from a single radiation event and typically associated with permanent damage to one or more elements of a device (e.g., gate oxide rupture). JESD57, 12/96# JESD89-1A, 10/07 JESD89-2A, 10/07 JESD89-3A, 11/07

single-event latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality. JEP133C, 1/10 JESD57, 12/96# JESD89A, 10/06 JESD89-1A, 10/07 JESD89-2A, 10/07 JESD89-3A, 11/07

NOTE 1 SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.

NOTE 2 An example of SEL in a CMOS device occurs when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

single-event transient (SET): A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by the passage of a single energetic particle. JEP133C, 1/10 JESD89A, 10/06 JESD89-1A, 10/07 JESD89-2A, 10/07 JESD89-3A, 11/07

single-event upset (SEU): A soft error caused by the signal induced by the passage of a single energetic particle. JEP133C, 1/10 JESD57, 12/96# JESD89A, 10/06 JESD89-1A, 10/07 JESD89-2A, 10/07 JESD89-3A, 11/07

single-event upset (SEU) cross-section: The number of single-event upsets produced per unit fluence. JESD89A, 10/06#

NOTE 1 Device SEU cross-section is expressed in terms of area per device.

NOTE 2 Bit SEU cross-section is expressed in terms of area per bit.

single-event upset (SEU) rate: The rate at which single-event upsets occur. JESD89A, 10/06

single-in-line memory module (SIMM): A multichip module in which the body has a SIP form and is made up primarily of memory devices. (See also "ZIP/SIMM".) JESD21-C, 1/97

single-in-line package (SIP): A rectangular package with the leads along one side, normally one of the long sides. JESD21-C, 1/97

NOTE….See also "in-line package".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

single-lump model parameter value: A model parameter determined so that the whole electrical signal path is represented by a single inductance or capacitance value. Such model parameters will generally be useful at relatively low frequencies and fail to yield acceptable simulation results as the frequency of operation is increased and the interconnect takes on a more distributed nature. JEP123, 10/95

single-phase bridge converter: A circuit that produces a variable dc output from a single-phase ac input by means of a bridge circuit. JESD14, 11/86

single-phase center tap, (bi-phase) converter: A circuit that produces a variable dc output from a single-phase ac input and a transformer with a center-tap connection. JESD14, 11/86

single-phase inverter: A circuit that produces a single-phase ac output from a dc input. JESD14, 11/86

single-sided PCB assembly: A printed circuit board assembly with components mounted on only one side of the board. JESD22-B111, 7/03
JESD22-B113A, 9/12

single-way rectifier circuit: A circuit in which the current flows in only one direction from each terminal of the alternating-voltage circuit to the rectifier circuit element connected to each terminal. JESD282-B, 4/00

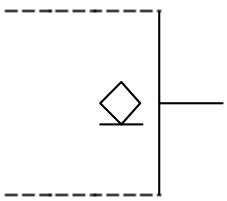
NOTE The terms “single-way” and “double-way” provide a means for describing the effect of the rectifier circuit on current in the transformer windings connected to rectifier circuits. Most rectifier circuits may be classified into these two general types.

sink driver, (current-): A unipolar output whose primary connection within the integrated circuit is through an active device to the least positive (most negative) supply voltage (typically the circuit common). JESD99C, 12/12

NOTE 1 When the active device is in its on state, the output voltage approaches the voltage of the supply to which it is connected by the active device; when the device is in its off state, the output is pulled up to the most positive (least negative) supply voltage through the external circuit to which the output is connected.

NOTE 2 Examples of sink drivers are npn open-collector, pnp emitter-follower, pnp open-emitter, n-channel open-drain, p-channel open-source, and p-channel source-follower outputs.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



NOTE The bar below the diamond indicates that the output is at the low logic level when the active device is in its on state.

SIP: See “single-in-line package”.

SIP/SIMM; SIP/SIMM module: Synonyms for “single-in-line memory module (SIMM)”. JESD21-C, 1/97#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

SIS: See "silicon-gate-insulator-semiconductor technology".

skewing time, internal (of a digital-to-analog converter): The difference in internal delay between the individual output transitions for a given change of digital input. JESD99C, 12/12

NOTE The internal (as well as external) skew has a major influence on the settling time for critical changes in the digital input, e.g., a 1-LSB change from 011...111 to 100...000, and is an important source of commutation noise.

skew (time) (general) (t_{sk}): The magnitude of the time difference between two events that ideally would occur simultaneously. JESD65B, 9/03
JESD99C, 12/12

skew (time), bank ($t_{sk(b)}$): The output skew time between outputs with a single driving input terminal. JESD65B, 9/03
JESD99C, 12/12

skew (time), input ($t_{sk(i)}$): The magnitude of the difference in propagation delay times between two inputs and a single output of an integrated circuit at identical operating conditions. JESD99C, 12/12

skew (time), inverting ($t_{sk(inv)}$): The skew time between two outputs of a single integrated circuit with all driving inputs switching simultaneously and the outputs switching in opposite directions while driving identical loads. JESD65B, 9/03
JESD99C, 12/12

skew (time), limit ($t_{sk(l)}$): The difference between (1) the greater of the maximum specified values of propagation delay times t_{PHL} and t_{PLH}, and (2) the lesser of the minimum specified values of propagation delay times t_{PHL} and t_{PLH}. JESD99C, 12/12

skew (time), multiple-frequency ($t_{sk(\omega)}$): The skew time between the controlled-edge position of two different output frequencies on a phase-locked loop (PLL) or counting device that has more than one output frequency, when both signals are rising or both signals are falling. JESD65B, 9/03

skew (time), output ($t_{sk(o)}$): The skew time between specified outputs of a single integrated circuit with all driving inputs switching simultaneously and the outputs driving identical loads. JESD65B, 9/03
JESD99C, 12/12

skew (time), output, high-to-low ($t_{sk(HL)}$): The skew time between specified outputs of a single logic device switching from the high level to the low level while driving identical loads. JESD65B, 9/03
JESD99C, 12/12#

NOTE Each input-to-output propagation delay time may be measured individually, and the difference is the skew time.

skew (time), output, low-to-high ($t_{sk(LH)}$): The skew time between specified outputs of a single logic device switching from the low level to the high level while driving identical loads. JESD65B, 9/03
JESD99C, 12/12#

NOTE Each input-to-output propagation delay time may be measured individually, and the difference is the skew time.

skew (time), part-to-part ($t_{sk(pp)}$): The magnitude of the difference in propagation delay times between any specified terminals of two integrated circuits at identical operating conditions. JESD65B, 9/03#
JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

skew (time), process ($t_{sk(pr)}$): The part-to-part skew time between corresponding terminals of two samples of an integrated circuit from a single manufacturer. JESD65B, 9/03 JESD99C, 12/12

skew (time), pulse ($t_{sk(p)}$): The magnitude of the difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch. JESD65B, 9/03 JESD99C, 12/12

sleep-mode enable (ZZ): A control input that logically deselects RAM and places it in the sleep mode. Devices that implement the sleep mode may require several cycles to implement "go-to-sleep" or "wake-up." JESD21-C, 1/97

slew rate (SR): The time rate of change of the closed-loop amplifier output voltage for a step-signal input. JESD99C, 12/12

NOTE Slew rate is normally measured between specified output levels using the largest input voltage step for which amplifier performance remains linear with feedback adjusted for unity amplification.

slew rate, (digital) (of a linear or **a multiplying digital-to-analog converter) (S_{OM}** or **S_{OMD}):** The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value. JESD99C, 12/12

NOTE 1 For a multiplying digital-to-analog converter, the full term and the additional subscript D must be used to distinguish between the digital and the reference slew rates.

NOTE 2 The abbreviations "SR" and "SR(dig)" are also used.

slew rate, reference (of a multiplying digital-to-analog converter) (S_{OMR}): The maximum rate of change of the analog output following a large step change of the reference voltage. JESD99C, 12/12

NOTE The abbreviation "SR(ref)" is also used.

slice: Synonym for "bit slice". JESD100-B, 12/99

slice: One memory chip in a stack of memory chips. JESD229, 12/11

small-outline gull-wing (package) (SOG; SOP): A surface-mount package that conforms to the "small-outline" concept and has the leads formed into a "gull-wing" configuration. JESD21-C, 1/97

small-outline J-lead (package) (SOJ): A surface-mount package that conforms to the "small-outline" concept and has the leads formed into a "J" configuration. JESD21-C, 1/97

small-outline package: A package whose chip cavity or mounting area occupies a major fraction of the package area and whose terminals are on one or two (normally opposite) sides and consist of metal pad surfaces (on leadless versions) or leads formed around the sides and under the package or extending out from the package (on leaded versions). JESD30E, 8/08

NOTE 1 On leaded versions, the lead form is usually gull wing but other lead forms may be used.

NOTE 2 The quad flatpack is similar except for having terminals on four sides of the package.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

small signal: A signal that, when doubled in magnitude, does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. JESD10, 1/76 JESD77D, 8/12 RS-371, 2/70# RS-372, 5/70# RS-435, 4/76

small-signal drain-source on-state resistance ($r_{ds(on)}$): The small-signal resistance between drain and source terminals with a specified gate-source voltage applied to bias the device to the on-state. JESD24, 7/85

NOTE For a depletion-type device, the gate-source voltage may be zero.

small-signal open-circuit output admittance, common-emitter (h_{oe}): The ac collector current divided by the small-signal ac collector-emitter voltage with the base terminal open-circuited to the emitter for ac. (Ref. MIL-S-19500D.) JESD10, 1/76#

small-signal short-circuit forward current transfer ratio, common-emitter (h_{fe}): The ratio of the ac collector current to the small-signal ac base current with the collector short-circuited to the emitter for ac. (Ref. MIL-S-19500D.) JESD10, 1/76

small-signal short-circuit forward current transfer ratio cutoff frequency, common-emitter (f_{hfe}): The lowest frequency at which the magnitude of the small-signal short-circuit forward current transfer ratio is 0.707 times its value at a specified low-frequency (usually 1 kHz or lower). (Ref. IEEE Std 255.) JESD10, 1/76

small-signal short-circuit input impedance, common-emitter (h_{ie}): The small-signal ac base-emitter voltage divided by the ac base current with the collector short-circuited to the emitter for ac. (Ref. MIL-S-19500D.) JESD10, 9/81#

SMD: Surface-mount device. J-STD-033C, 2/12

NOTE For the purpose of J-STD-033, the abbreviation SMD is restricted to include only plastic-encapsulated SMDs and other packages made with moisture-permeable materials.

SMPDRAM: See “synchronous MPDRAM”.

SMT: See “surface mount process technology”.

SMT IC: Abbreviation for “surface-mount-technology integrated circuit”. JESD22-B113A, 9/12

snapback: In an NMOS device, a high-current regenerative state that can be induced by a single heavy-ion strike or by a high-dose-rate pulse. JEP133C, 1/10

SNOS: See “silicon-nitride-oxide-semiconductor technology”.

S(n)(x): See “chip select”.

soak: The exposure of a device for a specified time at a specified temperature and humidity. J-STD-020D.1, 3/08

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Terms, abbreviations, letter symbols, and definitions **References**

soft error: (1) An erroneous signal, from a device, that can be corrected by performing one or more normal functions of the device. JEP143C, 7/12

NOTE 1 The error is called "soft" because the device or circuit behaves normally after the correction is made.

NOTE 2 See also "soft error, device" for use in a radiation context.

(2) An error in a device or circuit cell that can be corrected.

NOTE See note 1 to "soft error" (1).

soft error, device: An erroneous output signal, from a latch or memory cell, that can be corrected by performing one or more normal functions of the device containing the latch or memory cell. JEP133C, 1/10
JESD89A, 10/06
JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

NOTE 1 As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.

NOTE 2 Soft errors can be generated from SEU, SEFI, MBU, MCU, and/or SET. The term SER, which includes a variety of soft error mechanisms, has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc., are typically used by the avionics, space, and military-electronics communities.

soft error, power-cycle (PCSE): A soft error that is not corrected by repeated reading or writing but can be corrected by the removal of power (e.g., nondestructive latch-up). JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

soft error rate (SER): The rate at which soft errors occur. JESD89A, 10/06

soft error, static: A soft error that is not corrected by repeated reading but can be corrected by rewriting without the removal of power. JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

soft error, transient: A soft error that can be corrected by repeated reading without rewriting and without the removal of power. JESD89-1A, 10/07
JESD89-2A, 10/07
JESD89-3A, 11/07

soft macro: Synonym for "macro function". JESD12-1B, 8/93
JESD99C, 12/12

software: The computer programs, procedures, rules, and possibly associated documentation concerned with the operation of a data processing system. (Ref. ANSI X3.172.) JESD100-B, 12/99

NOTE 1 Contrast with "hardware" and "firmware".

NOTE 2 Computer programs stored on disks, including hard drives and CD-ROMs, are customarily referred to as software.

SOG: See "small-outline gull-wing (package)".

SOJ: See "small-outline J-lead (package)".

solderability: The ability of a metal to be wetted by molten solder. (Ref. IPC-T-50.) J-STD-002B, 2/03

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
solder bump: A discrete amount of solder, attached to the die external metallization, that is intended to form an interconnection to a substrate.	JESD22-B109A, 1/09
solder connection pinhole: A small hole that penetrates from the surface of a solder connection to a void of indeterminate size within the solder connection. (Ref. IPC-T-50.)	J-STD-002B, 2/03
solder pull fracture: A fracture within the bulk of the solder bump column.	JESD22-B109A, 1/09
solder reflow: A solder attachment process in which previously applied solder or solder paste is melted to attach a component to a printed circuit board.	J-STD-033C, 2/12
solder void: A cavity within a solder joint that exposes device or substrate metallization.	JESD22-B109A, 1/09
solder void area (of a BGA solder ball or joint): The area of the solder void region within the X-ray image.	JESD217, 9/10
solid-state (within the scope of JEDEC): Relating to, or utilizing, those electrical, magnetic, optical, thermal, and/or chemical properties of semiconductors that are based on the arrangement or behavior of atoms, ions, molecules, nucleons, electrons, holes, and/or imperfections.	JESD77D, 8/12 JESD99C, 12/12
solid-state circuit: Synonym for "integrated circuit, single-chip".	JESD99C, 12/12
solid-state component: A solid-state device that is, or is intended to be, a constituent part of a higher order assembly. NOTE Examples of solid-state components include DRAMs as parts of memory modules and microprocessors as parts of motherboards.	JESD77D, 8/12 JESD99C, 12/12
solid-state device: An electronic device whose operation depends on the properties of the integral solid semiconductor materials. NOTE 1 Examples of solid-state devices include discrete transistors, discrete thyristors, discrete transient voltage suppressors, discrete semiconductor pressure sensors, integrated circuits, modules consisting mainly of integrated circuits such as multichips and hybrids, and memory modules such as DIMMs and SIMMs. NOTE 2 Electromechanical devices, e.g., solenoids, breakers, wire relays, are not considered to be solid-state devices.	JESD77D, 8/12 JESD99C, 12/12
solid-state drive: A nonvolatile storage device including a controller and one or more solid-state memories, typically using traditional hard disk drive (HDD) interfaces (protocol and physical) and form factors.	JESD99C, 12/12 JESD218A, 2/11
solid-state industry: Those companies and organizations whose primary function is associated with design, fabrication, assembly, test, inspection, and/or distribution of solid-state devices.	JESD77D, 8/12 JESD99C, 12/12
solid-state memory: An integrated circuit, or a portion thereof, whose primary function is storage.	JESD99C, 12/12
solid-state physics: The study of the physical properties of solids, with special emphasis on the electrical, magnetic, optical, thermal, and chemical properties of semiconducting materials in relation to their electronic structure.	JESD77D, 8/12 JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

solid-state technology: The applied sciences and skills of developing and manufacturing solid-state devices. JESD77D, 8/12 JESD99C, 12/12

SONOS: See "silicon-oxide-nitride-oxide-semiconductor technology".

SOP: See "small-outline gull-wing (package)".

SOS: See "silicon-on-sapphire technology".

source alpha activity: See "alpha activity (of a source)".

source current, dc (I_S): The direct current into the source terminal. JESD24, 7/85

source cutoff current ($I_{S(off)}$): The direct current into the source terminal of a depletion-type transistor with a specified gate-drain voltage applied to bias the device to the off-state. JESD24, 7/85

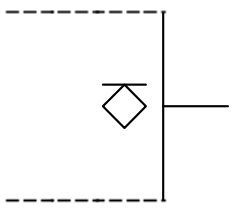
source-drain voltage, dc (V_{SD}): The dc voltage between the source terminal and the drain terminal. JESD24, 7/85

source driver, (current-): A unipolar output whose primary connection within the integrated circuit is through an active device to the most positive (least negative) supply voltage. JESD99C, 12/12

NOTE 1 When the active device is in its on state, the output voltage approaches the voltage of the supply to which it is connected by the active device; when the device is in its off state, the output is pulled down to the least positive (most negative) supply voltage through the external circuit to which the output is connected.

NOTE 2 Examples of source drivers are pnp open-collector, npn emitter-follower, npn open-emitter, p-channel open-drain, n-channel open-source, and n-channel source-follower outputs.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



NOTE The bar above the diamond indicates that the output is at the high logic level when the device is in its on state.

source follower: An output circuit whose output load is connected in the source circuit of a field-effect transistor and whose input is applied between the gate and the remote end of the source load, which may be at ground potential. JESD99C, 12/12

NOTE The term "source follower" as applied to linear circuits, usually refers to passive-pulldown or passive-pullup (bipolar) outputs; as applied to logic circuits, to open-source (unipolar) outputs.

source-gate voltage, dc (V_{SG}): The dc voltage between the source terminal and the gate terminal. JESD24, 7/85

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
source region: (1) A region from which majority carriers flow into the channel.	JESD24, 7/85
(2) A supply region that supplies principal-current charge carriers into a controlled channel.	JESD77D, 8/12
NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.	
source supply voltage, dc (V_{SS}): The dc supply voltage applied to a circuit connected to the source terminal.	JESD24, 7/85
source terminal (S, s): The externally available point of connection to the source region.	JESD77D, 8/12
space-charge region (1) **(of a semiconductor device):** A functional region in which the net charge density is significantly different from zero. (Ref. ANSI/IEEE Std 100.)	JESD77D, 8/12 JESD99C, 12/12
NOTE 1 The net charge is caused by electrons, holes, and ionized acceptors and donors.	
NOTE 2 The space-charge regions of a semiconductor device include accumulation (enhancement), depletion, and inversion layers.	
(2) **(of a p-n junction):** A space-charge region contained between two neutral regions of types p and n.	JESD77D, 8/12
space-charge region, collector(-base): The space-charge region between the functional collector region and the functional base region.	JESD77D, 8/12
space-charge region, emitter(-base): The space-charge region between the functional emitter region and the functional base region.	JESD77D, 8/12
spatial resolution: The diameter of a spot whose size is determined from the half-power points resulting from a point infrared source.	JEP138, 9/99 JESD51-1, 12/95 JESD51-13, 6/09
SPC: See “statistical process control”.	
SPCM: Semiconductor power-control module.	JESD14, 11/86
SPD: See “surge protective device”.	
special cause; assignable cause: A source of variation that is intermittent, unpredictable, or unstable and affects only some of the individual values of the process output being studied.	EIA-557-B, 2/06 JESD659B, 2/07
special-cause signal: A process variation outside the random or predictable pattern of the process.	JEP121A, 10/06
special-function enable input (DSF): The input on a device that, when true, actuates certain special operational functions. In devices and modules that have multiple DSFs, the DSFs are numbered beginning with 0.	JESD21-C, 1/97
special-function enable voltage (VHH): A special high-voltage logic level (super voltage) that enables special on-chip functions.	JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

special read transfer: A read transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal RAM-to-SAM data transfers. JESD21-C, 1/97

special-shape package: A package whose outline style is not otherwise specified in JESD30. JESD30E, 8/08

special write transfer: A write transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal SAM-to-RAM data transfers. JESD21-C, 1/97

specification limits: The boundaries for judging acceptability of a particular characteristic. EIA-557-B, 2,06#

split read transfer (SRT): A read transfer in which the SAM data register is split into two halves and the data is transferred from the RAM data bus separately into each half of the SAM register as it is needed for transfer to the SDQn terminals. JESD21-C, 1/97

split write transfer (SWT): A write transfer in which the SAM data register is split into two halves and the data is transferred to the RAM data bus separately after each half of the SAM register is filled. JESD21-C, 1/97

spot noise figure; spot noise factor (*F* or NF): The ratio of (1) the total output noise power per unit bandwidth (spectral density) at a single output frequency when the noise temperature of all input terminations is at the reference noise temperature, T_0, at all frequencies that contribute to the output noise to (2) that part of (1) caused by the noise of the signal-input termination at the signal-input frequency. JESD77D, 8/12
JESD99C, 12/12
JESD311A, 11/81
RS-353, 4/68

NOTE 1 The abbreviation NF is often used in place of symbol *F*; however, symbol *F* is preferred.

NOTE 2 These quantities may be expressed logarithmically in decibels (dB).

sputter cleaning; back sputtering: A process in which material is physically removed from a designated surface by bombardment of ions generated in a plasma. JESD99C, 12/12

NOTE The gas used is generally inert or nonreactive, e.g., argon or helium.

sputtering: A process for forming thin films in which ion bombardment is used to free particles from a solid source that are then deposited onto another nearby surface. JESD99C, 12/12

SQ(n): See “serial data output”.

SQC: See “statistical quality control”. 6

SRAM: See “static (random-access) memory”.

SRM: See “statistical reliability monitoring”.

SRMF: See “statistical reliability monitor family”.

SRT: See “split read transfer”.

SSER: See “system soft error rate”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

SSI: Small-scale integration. JESD99C, 12/12

SSRAM: See "synchronous static RAM".

SSx; SS: See "sync byte 'x' select".

ST: See "store".

stability: (1) The absence of special causes of variation; the property of being in statistical control. EIA-557-B, 2/06

(2) The measurable ability of an attribute or output of a process to remain constant within prescribed boundaries. JEP132, 7/98

stable process: A process that is in statistical control. EIA-557-B, 2/06

stack: All of the memory chips in a memory system taken together in one assembly. JESD229, 12/11

NOTE This Wide I/O specification supports memory stacks that include up to four memory chips.

stack (storage): Synonym for "pushdown storage". JESD100-B, 12/99

stain: A visual anomaly consisting of a discolored foreign material area that has a definite edge or boundary but has no measurable thickness. JESD22-B118, 3/11

staining: A discoloration produced by foreign matter having penetrated into or chemically reacted with a material, typically not easily removed. JESD9B, 5/11

standard cell: A macrocell used in the context of cell-based integrated circuits. JESD12-1B, 8/93
JESD99C, 12/12

standard deviation: A measure of the spread or variation in a probability distribution (population standard deviation) or in a sample of values measured on the output from a process (sample standard deviation). EIA-557-B, 2,06

standard impulse waveshape: See "impulse waveshape, standard".

standard overall average noise figure (of a mixer diode) ($\overline{F}_{os}$): The overall average noise figure when the average noise figure of the IF amplifier is a specified standard value (usually 1.5 dB) and the passband of the IF amplifier is sufficiently narrower than that of the mixer so that the mixer conversion loss and output noise temperature are essentially constant over the IF passband. JESD77D, 8/12
JESD311A, 11/81

standard product, (integrated circuit): An integrated circuit developed and produced for multiple applications or functions and made available for multiple customers. JESD99C, 12/12

standard wafer-level electromigration accelerated test (SWEAT): An accelerated electromigration test performed on microelectronic metallization. It uses a feedback control loop to adjust the stress current applied to the metallization such that the temperature and current density of the structure maintain the target time to failure within a programmed error band. JEP119A, 8/03

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

standby current (of a voltage regulator) ($I_{I(standby)}$): The supply current drawn by the regulator with no output load and no reference voltage load. JESD99C, 12/12

standoff: An insulator or support that supports an item above a surface. JESD9B, 5/11

standoff (nonconducting) region: The portion of the voltage-current characteristic of a reverse-biased p-n junction that exhibits a high resistance to the passage of current. JESD77D, 8/12 JESD210, 12/07

static: A short form of "electrostatic" JESD625B, 1/12

static-column page mode: An operating mode in which all accesses to a dynamic random-access memory occur within a page boundary defined by the row address and column addresses are entered while the column address strobe remains active. JESD100-B, 12/99

NOTE See also note to "page mode".

static dissipative material: A material having a surface or volume resistance between 1×10^4 ohms and 1×10^{11} ohms. JESD625B, 1/12

NOTE A static-dissipative material is not necessarily antistatic.

static drain-source on-state resistance ($r_{DS(on)}$): The dc resistance between the drain and source terminals with a specified gate-source voltage applied to bias the device to the on-state. JESD24, 7/85

NOTE For a depletion-type device, the gate-source voltage may be zero.

static forward current transfer ratio, common-emitter (h_{FE}): The dc collector current divided by the dc base current. (Ref. MIL-S-19500D.) JESD10, 1/76#

static input resistance, common-emitter (h_{IE}): The dc base-emitter voltage divided by the dc base current. (Ref. MIL-S-19500D.) JESD10, 1/76#

static phase offset ($t_{(\phi)}$): The time interval between similar points on the waveforms of the averaged input reference clock and the averaged feedback input signal when the phase-locked loop (PLL) is locked and the input reference frequency is stable. JESD65B, 9/03

NOTE 1 PLL jitter may cause excursions of $t_{(\phi)}$ beyond the specified maximum.

NOTE 2 The term "PLL reference zero delay" has been used for this concept but its use is deprecated.

static random-access memory (SRAM): A static memory that permits access to any of its address locations in any desired sequence with similar access time to each location. JESD21-C, 1/97# JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

static (read/write) memory: A volatile read/write memory in which the data is retained in the absence of control signals generated inside or outside the integrated circuit. (Adapted from IEC 748-2.) JESD100-B, 12/99

NOTE 1 The words "read/write" may be omitted from the term when no misunderstanding is likely.

NOTE 2 A static memory can use dynamic addressing or sensing circuits.

NOTE 3 Contrast with "dynamic (read/write) memory".

static value: (1) A nonvarying value or quantity of measurement at a specified fixed point. JESD24, 7/85
JESD77D, 8/12

(2) The slope of the line from the origin to the operating point on the appropriate characteristic curve.

statistic: A value calculated from or based upon sample data used to make inferences about a parameter of the population from which the sample came. EIA-557-B, 2/06

statistical control: The conditions describing a process from which all special causes of variation have been eliminated and only common causes remain. EIA-557-B, 2/06

statistical process control (SPC): The conversion of data to information using statistical techniques to document, correct, and improve process performance. EIA-557-B, 2/06

statistical quality control (SQC): Statistical methods and procedures used to document and ensure compliance with requirements. EIA-557-B, 2/06

statistical reliability monitor family (SRMF): A product or group of products whose process similarities make them a homogeneous population for the purpose of statistical reliability monitoring. JESD659B, 2/07

NOTE 1 A homogeneous population of product from one SRMF will have similar propensity towards the physical failure mechanisms being monitored when that product is stressed by accelerated tests or operated in its intended system application.

NOTE 2 Each product in an SRMF will have the same failure rate for each mechanism only if the factors affecting a failure mechanism are identical for each product type.

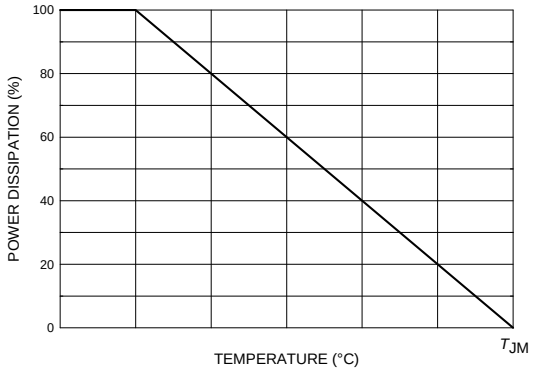
statistical reliability monitoring (SRM): A statistically based methodology for monitoring and improving reliability involving identification and classification of failure mechanisms, development and use of monitors, and investigation of failure kinetics, allowing prediction of failure rates at use conditions. JESD659B, 2/07

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

steady-state power dissipation derating curve: A graphical presentation showing how a power rating stated at a particular temperature is reduced at higher temperatures. JESD211, 12/09

NOTE The steady-state power-derating curve is derived from $P_D = (T_{JM} - T_X)/ R_{\theta JX}$, where the subscript "X" can indicate L (for lead), C (for case), EC (for end cap), or A (for ambient). The usual power-derating curve is drawn with a slope of $-1/R_{\theta JX}$ from 0% at $T_X = T_{JM}$ up to 100% at a value of temperature equal to or above 25 °C, but below T_{JM}. A typical derating curve for a regulator diode is shown.



step (of an analog-to-digital or **digital-to-analog conversion):** Any of the individual correlations in the conversion code or any part of the diagram equating to an individual correlation in the transfer diagram. JESD99C, 12/12

NOTE 1 For an analog-to-digital converter, a step represents both a fractional range of analog input values and the corresponding digital output code.

NOTE 2 For a digital-to-analog converter, a step represents both a digital input code and the corresponding discrete analog output value.

step height [step size] (of a digital-to-analog converter): The absolute value of the difference in step values between two adjacent steps in the transfer diagram. JESD99C, 12/12

NOTE For companding digital-to-analog converters, the term "step size" is in general use.

step stress test hardening: Increasing the ability of a device to withstand ESD voltage stress by applying stress incrementally from relatively low voltage to higher values. JS-001-2012, 4/12

NOTE This hardening occurs when a device subjected to increasing ESD voltage stresses is able to withstand higher stress levels than a device from the same device family not previously stressed.

step value (of a digital-to-analog converter): The value of the analog output representing a digital input code. JESD99C, 12/12

step value, nominal (of a digital-to-analog converter): A specified step value that exactly represents the corresponding digital input code. JESD99C, 12/12

step width (of an analog-to-digital converter): The absolute value of the difference between the two ends of the range of analog values corresponding to one step. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

stitch bond: Synonym for "wedge bond".

storage element: A circuit or device into which data has been or can be entered, in which that data is or can be stored, and from which that data can be retrieved. JESD89A, 10/06#

NOTE Examples include DRAM cells, SRAM cells, and flip-flops.

storage environment: The temperature and relative humidity to which a component is exposed while being stored in a nonoperating state. JESD94A, 7/08

storage gate: A gate electrode, isolated from the channel by an insulating layer or junction, to which voltage is applied in order to store charge. JESD99C, 12/12

storage lifetime: The length of time that a component is in storage prior to use in an application. JESD94A, 7/08

storage temperature (T_{stg}): The temperature at which the device, without any power applied, is stored. JESD10, 1/76
JESD77D, 8/12

storage time (t_s): The time interval from a point 90% of the maximum amplitude on the trailing edge of the input pulse to a point 90% of the maximum amplitude on the trailing edge of the output pulse. JESD10, 1/76

store (ST): On an NVRAM, the input that initiates the nonvolatile data storage of the entire RAM array. JESD21-C, 1/97

stored charge (Q_s): The total amount of charge recovered from a diode minus the capacitive component of charge when the diode is switched from a specified conductive condition to a specified nonconductive condition with other circuit conditions specified. JESD77D, 8/12
JESD282-B, 4/00

straight-line approximation of the on-state characteristic: An approximation of the current versus voltage on-state characteristic by means of a straight line that crosses this characteristic at two specified points. JESD77D, 8/12

straight-line approximation of the reverse-conducting characteristic: An approximation of the current versus voltage reverse-conducting characteristic by means of a straight line that crosses this characteristic at two specified points. JESD77D, 8/12

strain: The deformation of a material body under the action of an applied force. JESD22-B113A, 9/12

strain gage: A planar foil pattern, typically adhered to an underlying surface, that exhibits a change in resistance when subjected to a strain. JESD22-B113A, 9/12

strain gage element: The sensing area of a strain gage defined by the active serpentine grid pattern. JESD22-B113A, 9/12

strain value: A dimensionless quantification of strain calculated as the change in length divided by the original length. JESD22-B113A, 9/12

stratum; tier: An individual layer of silicon in a chip stack. JEP158, 11/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
stress: The application for some period of a forced condition that is outside of the usual operating range.	JEP143C, 7/12
strike distance: The shortest distance in air between specified terminals or between a specified terminal and a mounting surface.	JESD14, 11/86
stripline package: A transistor package having all of its leads in a single plane.	RS-435, 4/76
NOTE This includes beam leads.	
structural description: A definition of a function in terms of an interconnection of primitives.	JESD12-1B, 8/93 JESD99C, 12/12
stuck-at-1 fault: A fault in a digital circuit characterized by a node remaining at a logic high (1) state regardless of changes in input stimuli.	JESD12-5, 8/88
stuck-at-0 fault: A fault in a digital circuit characterized by a node remaining at a logic low (0) state regardless of changes in input stimuli.	JESD12-5, 8/88
stud: The tool that is attached to the backside of a flip chip die to perform tensile pull test.	JESD22-B109A, 1/09
stud-mount package: Synonym for "post-mount package".	JESD30E, 8/08
subchannel region (of an IGFET): A control region within which the channel is formed and in which control charge determines threshold voltage, the control charge being the result of an applied subchannel voltage.	JESD77D, 8/12
NOTE This definition applies for the actual operating mode of the device regardless of the name of any associated terminal.	
subcontractor: An individual or business firm contracting to perform part or all of another's contract.	JEP146A, 1/09
subelement: A distinguishable portion of a microcircuit element.	JESD99C, 12/12
EXAMPLE The emitter, collector, and base of an integrated bipolar transistor are subelements of an integrated circuit.	
substance: A chemical element or compound, e.g., lead (a chemical element), lead oxide (a compound), polyvinyl chloride (a compound).	JIG-101 Ed 2.0, 4/09
NOTE Registry numbers of the Chemical Abstracts System of the American Chemical Society (CAS numbers) have been assigned to all chemical elements and most of their compounds and should be used for their identification. CAS numbers are provided in an annex to JIG-101.	
substrate (of a package): A platform that mechanically supports a bumped silicon die within a package and electrically connects the solder bump landing pads to external terminals, using layered dielectric materials and conductive traces.	JEP154, 1/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
substrate (of a semiconductor device) (1) **(general):** The supporting material upon which or within which the elements of a semiconductor device are fabricated or attached.	JEP156, 3/09 JESD24, 7/85
(2) **(of a film integrated circuit):** A piece of material forming a supporting base for film circuit elements and possibly additional components.	JESD99C, 12/12
(3) **(for semiconductor dice):** The supporting material upon which one or more semiconductor dice are attached.	JESD22-B109, 6/02
(4) **(original substrate):** The original semiconductor material being processed.	JESD77D, 8/12 JESD99C, 12/12
NOTE The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.	JESD77D, 8/12 JESD99C, 12/12
(5) **(remaining substrate):** The part of the original material that remains essentially unchanged when the device elements are formed upon or within the original material.	
NOTE The intended meaning will usually be clear from the context in which the term is used. If necessary, distinction can be made between the "original substrate" and the "remaining substrate".	
substrate, active: A substrate in which active elements are implemented within the substrate material.	JESD99C, 12/12
substrate (attach) area: An area of package used for substrate placement, typically on the bottom inside surface of the base of the package.	JESD9B, 5/11
substrate fracture: A failure found in tensile pull of flip chip solder joints wherein the substrate is fractured and damaged before all the solder bumps are separated from it.	JESD22-B109A, 1/09
substrate, passive: A substrate that serves primarily as a structural support or mounting surface for functional circuit elements.	JESD99C, 12/12
substrate power voltage (VBB): A bias voltage that maintains the substrate at a potential that is negative with respect to GND or VSS in an NMOS or CMOS part.	JESD21-C, 1/97
substrate (to which packaged components are attached): A ceramic block or laminate card having one or more wired layers, to which one or more components are electrically connected.	JESD22-B101B, 8/09
suffix (for the FCT series): A letter (e.g., A, B, C), immediately following the device number, that indicates the speed grade for the device.	JESD18-A, 1/93
NOTE 1 For example, FCT244A refers to the "A" speed version of the "244" function with CMOS output swing, and FCT244AT refers to the "A" speed version of the "244" function with TTL output swing.	
NOTE 2 The slowest speed grade has no such suffix.	
sum-of-the-failure-rates method: The adding of observed failure rates for different failure mechanisms to obtain a total failure rate for a given product and technology, based on the assumption that the failure mechanisms are independent of each other.	JEP122E, 3/09 JEP143C, 7/12
supplier: An individual or business firm that provides goods or services to another.	JEP146A, 1/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

supplier performance rating: An assessment of the metrics established to evaluate a supplier's performance. JEP146A, 1/09

supplier report card: A document that conveys to a supplier an evaluation of their performance based on criteria as defined by the customer and agreed to by the supplier. JEP146A, 1/09

supply current, high-level output (I_{CCH}, I_{DDL}, I_{EEL}, etc.): The current into a supply terminal of an integrated circuit when the output is (all outputs are) at a high-level voltage. JESD99C, 12/12

supply current, low-level output (I_{CCH}, I_{DDL}, I_{EEL}, etc.): The current into a supply terminal of an integrated circuit when the output is (all outputs are) at a low-level voltage. JESD99C, 12/12

supply region (within a semiconductor device): A functional region that delivers principal-current charge carriers to the control region of the device. JESD77D, 8/12

supply terminal; supply pin: A package terminal that transfers operating voltage and current to a circuit within the package. JS-001-2012, 4/12#

NOTE Supply terminals typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current reference levels). For the purpose of ESD testing, power and ground terminals are treated as supply terminals.

supply voltage, [base (V_{BB}), collector (V_{CC}), emitter (V_{EE})]: The supply voltage applied to a circuit connected to the reference terminal. JESD10, 1/76

supply voltage rejection ratio (k_{SVR}): The absolute value of the ratio of the change in one supply voltage (with all remaining supply voltages held constant) to the resulting change in input offset voltage. JESD99C, 12/12

NOTE 1 See the reciprocal definition under "supply voltage sensitivity".

NOTE 2 This concept is sometimes referred to as "power supply rejection ratio".

NOTE 3 The abbreviations SVRR and PSRR are often used in place of symbol k_{SVR}; however, symbol k_{SVR} is preferred.

supply voltage sensitivity (k_{SVS}) (1) **(of an analog integrated circuit):** The absolute value of the ratio of the change in input offset voltage to the corresponding change in value of one supply voltage with all remaining supply voltages held constant. JESD99C, 12/12

NOTE See the reciprocal definition under "supply voltage rejection ratio".

(2) **(of a digital-to-analog converter):** The change in full-scale output current (or voltage) caused by a change in supply voltage. JESD99C, 12/12

NOTE This sensitivity is usually expressed as the ratio of the percentage change of full-scale current (or voltage) to the percentage change of supply voltage.

surface channel: A transfer channel created at the semiconductor-insulator interface. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
surface-channel charge-coupled device (SCCD): A charge-coupled device in which potential wells are created at the semiconductor-insulator interface and charge is transferred along that interface.	JESD99C, 12/12
surface corrosion (of a tin finish): A localized corrosion of a silver-colored tin surface finish appearing in an optical microscope as nonreflective dark spots ranging in size from about 25 micrometers on the longest dimension to the entire terminal.	JESD22-A121A, 7/08 JESD201A, 8/08
NOTE….While tin oxide is ubiquitous on tin surface finishes, surface corrosion creates a locally thick layer of tin oxide that may span from the substrate to the surface of the deposit at the dark spot.	
surface finish roughness: The texture or roughness of a surface.	JESD9B, 5/11
surface mount process technology (SMT): A process technology for constructing electronic printed circuit boards in which components (small or large devices) are placed onto solder paste (or flux) in specified locations and exposed to reflow process window with varying sets of elevated temperature and time that allow solder coalescence and metallization.	JESD217, 9/10
surface resistance: The dc voltage between two electrodes of specified configuration on an insulative surface, divided by the current passing through them.	JESD625B, 1/12
NOTE Surface resistance is expressed in ohms.	
surface state: The energy levels associated with charge that resides on the surface of a semiconductor.	JESD99C, 12/12
surface-state charge density: The net charge density on the surface of a semiconductor.	JESD99C, 12/12
NOTE Both the charge density and the energy levels may be influenced by such factors as the insulation layer, surface discontinuities, chemicals, ultraviolet radiation, and electrical or magnetic fields.	
surge peak forward current (I_{FSM}): The peak forward current including all nonrepetitive transient currents but excluding all repetitive transient currents.	JESD77D, 8/12 JESD282-B, 4/00
surge protective device (SPD): Synonym for “transient voltage suppressor”.	JESD77D, 8/12
suspended items; suspensions: Items that had testing discontinued prior to failing or that survived until the end of the test.	JEP154, 1/08

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Terms, abbreviations, letter symbols, and definitions **References**

sustaining voltage, collector-emitter, base open ($V_{CEO(sus)}$):
sustaining voltage, collector-emitter, base short-circuited to emitter ($V_{CES(sus)}$):
sustaining voltage, collector-emitter, circuit between base and emitter ($V_{CEX(sus)}$):
sustaining voltage, collector-emitter, resistance between base and emitter ($V_{CER(sus)}$):
sustaining voltage, collector-emitter, voltage between base and emitter ($V_{CEV(sus)}$):
The collector-emitter breakdown voltage at relatively high values of collector current at which the breakdown voltage is relatively insensitive to changes in collector current, when the base terminal is, respectively, JESD10, 1/76 JESD77D, 8/12

— open-circuited.
— short-circuited to the emitter terminal.
— returned to the emitter terminal through a specified circuit.
— returned to the emitter terminal through a specified resistance.
— returned to the emitter terminal through a specified voltage.

NOTE This is the transient voltage between the collector and emitter terminals during switching with an inductive load from a forward-biased base-emitter to one of the external conditions described above.

SVRAM: See “synchronous VRAM”, synonym for “synchronous MPDRAM”.

SW: See “sync write”.

SWEAT: See “standard wafer-level electromigration accelerated test”.

switch device: A semiconductor logic device designed to connect and disconnect busses or other signals, without active drivers in the connection path. JESD73, 6/99 JESD73-1, 8/01 JESD73-2, 8/01 JESD73-3, 8/01 JESD73-4, 11/01

switching quadrant: A quadrant of the principal voltage-current characteristic in which a device is intended to switch between the off state and the on state. JESD77D, 8/12

switching safe operating area (SwSOA): All combinations of collector current and collector-emitter voltage that are permitted to occur during turn-off of the transistor without endangering its survival. JESD77D, 8/12

NOTE This information is normally presented graphically.

switch-level description: A structural description using switches as primitives. JESD12-1B, 8/93 JESD99C, 12/12

SwSOA: See “switching safe operating area”.

SWT: See “split write transfer”.

SWx: See “sync byte (group) ‘x’ write”.

Sxx (synchronous input function): For a synchronous memory device, a signal name for any input term that is synchronized by a clock, where the first letter “S” indicates that synchronization; e.g., SG = synchronous output enable, SW = synchronous write enable. JESD21-C, 1/97#

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
Sxxx: A memory type name starting with the letter "S" where "S" means "static" as in SRAM, "serial" as in SAM, or "synchronous" as in SDRAM and SGRAM.	JESD21-C, 1/97#
symbol library: The graphical symbols for a set of macrocells and/or macro functions.	JESD12-1B, 8/93 JESD99C, 12/12
sync address (SAn; SA): One of the clocked address inputs. In devices where the address order is significant, the SAn form is used with the values SA0 thru SAn, where "n" is the binary numerical order of the address or data bit.	JESD21-C, 1/97
sync byte (group) "x" write (SWx): A clocked control input that writes byte (group) "x". "x" takes the values of a, b, c, d, etc. For devices where the write control is applied to bit groupings that are other than a "byte", the definition still applies.	JESD21-C, 1/97
sync byte "x" select (SSx; SS): A clocked control input that logically selects byte "x" for reads and writes. If no "x" designator is given, the signal selects all bits of the device.	JESD21-C, 1/97
sync byte "x" write enable (SBx): A clocked control input that enables writes to byte "x" in conjunction with the SW input. SBx has no effect on read cycles.	JESD21-C, 1/97
sync enable (SE): A clocked control input that logically selects the RAM and removes it from power-down mode.	JESD21-C, 1/97
sync global write (SGW): A clocked control input that writes all bytes regardless of status of sync byte select (SSx) or sync byte write enable (SBx) inputs.	JESD21-C, 1/97
synchronous circuit: A circuit whose changes of state are controlled by a single clock signal.	JESD12-1B, 8/93 JESD99C, 12/12
synchronous dynamic random-access memory (SDRAM): A dynamic random-access memory that has a clocked synchronous interface.	JESD21-C, 1/97 JESD100-B, 12/99
synchronous graphics DRAM (SGRAM): A graphics DRAM (GRAM) that has a synchronous interface.	JESD21-C, 1/97
synchronous MPDRAM (SMPDRAM); synchronous VRAM (SVRAM): A multiport DRAM (MPDRAM) that has a synchronous interface on all ports.	JESD21-C, 1/97
synchronous operation: The use of a common timing source (clock) to time circuit operations or data transfer operations.	JESD100-B, 12/99
synchronous output enable (GS): An output enable input that is synchronized by a clock signal, K.	JESD21-C, 1/97
synchronous static RAM (SSRAM): An SRAM that has input and/or output buffers (either register or latch) that are controlled by an externally supplied clock (or clocks).	JESD21-C, 1/97
synchronous VRAM (SVRAM): Synonym for "synchronous MPDRAM".	JESD21-C, 1/97
sync output enable (SG): A clocked control input that enables output drivers.	JESD21-C, 1/97

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Terms, abbreviations, letter symbols, and definitions **References**

sync write (SW): A clocked control input that writes all bytes or, on devices with sync byte select (SItem) or sync byte write enable (SBx) inputs, writes all selected or enabled bytes. JESD21-C, 1/97

systematic defect: A defect found in a failing electronic component that is attributed to process variation, such as a metal contact open due to a photomask problem. JESD91A, 8/01

system soft error rate (SSER): Synonym for "real-time soft error rate (RTSER)". JESD89A, 10/06

T

T1: See "terminal 1".

T2: See "terminal 2".

table drop height: The free-fall drop height of the drop table needed to attain the prescribed peak acceleration and pulse duration. JESD22-B111, 7/03

tangential sensitivity (S_T): The input signal power to a circuit that produces a 6-dB signal-to-noise ratio at the output. JESD99C, 12/12

target: The desired value for a statistic of a characteristic or parameter of a process node. EIA-557-B, 2/06

target stress temperature (T_{test}): The desired mean temperature of the test line during the stress phase of the test. JESD61A.01, 10/07

target time to failure (t_{FT}): The desired time it should take for the resistance of the test structure to first equal or exceed the failure resistance criterion, R_{FC}, while the structure is under stress from the SWEAT algorithm. JEP119A, 8/03

TBW rating: See "endurance rating".

TCA: See "temporary chip attach".

TCK: See "test port clock".

TCR(T): See "temperature coefficient of resistance".

TDI: See "test data in".

TDO: See "test data out".

technical review board (TRB): A supplier's dedicated team of experts that is responsible for the implementation of the quality management program, maintenance of all certified and qualified processes, process change control, reliability data analysis, failure analysis, device recall procedures, and qualification status of the technology. JEP133C, 1/10

technology acceptance, surface finish: Acceptance testing of surface finish material set and manufacturing processes that include a defined set of base metals, underplating metals, surface finish alloy, surface finish bath chemistry, and process flow steps. JESD201A, 8/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

technology rating: An assessment of the metrics established to evaluate technology attributes. JEP146A, 1/09

temperature at failure (T_F): The value of the last recorded estimated mean temperature of the test structure during the control cycle before the failure criterion, R_{FC}, is satisfied. JEP119A, 8/03

temperature coefficient: The change in a parameter divided by the change in temperature. JESD77D, 8/12
JESD99C, 12/12

NOTE This quotient is the average value over the total temperature change. The change in the parameter may or may not be normalized to a reference value of the parameter. The specific term should be "temperature coefficient of (parameter)".

temperature coefficient of input bias current (α_{IIB}): The change in input bias current divided by the change in temperature. JESD99C, 12/12

NOTE This quotient is the average value for the total temperature change. The change in input bias current is usually not normalized to the initial value of input bias current.

temperature coefficient of input offset current (α_{IIO}): The change in input offset current divided by the change in temperature. JESD99C, 12/12

NOTE This quotient is the average value of the total temperature change. The change in input offset current is usually not normalized to the initial value of input offset current.

temperature coefficient of input offset voltage (α_{VIO}): The change in input offset voltage divided by the change in temperature. JESD99C, 12/12

NOTE This quotient is the average value for the total temperature change. The change in input offset voltage is usually not normalized to the initial value of input offset voltage.

temperature coefficient of output voltage (α_{VO}): The change in output voltage, usually expressed as a percentage of the output voltage, divided by the change in temperature. JESD99C, 12/12

NOTE This is the average value for the total temperature change.

temperature coefficient of regulator [Zener] voltage (α_{VZ}): The change in regulator voltage divided by the change in temperature that caused it. JESD211, 12/09

NOTE This quotient may be expressed as mV/°C, mV/K, %/°C, or %/K and is the average value for the total temperature change.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

temperature coefficient of resistance [TCR(T_{ref})]: The fractional change in resistance of the test line per unit change in temperature at a specified temperature, T_{ref}, as described in the following equation: JEP119A, 8/03 JESD33B, 2/04# JESD61A.01, 10/07

$$TCR(T_{ref}) = \frac{1}{R(T_{ref})}\frac{\Delta R}{\Delta T}$$

where

$R(T_{ref})$ {Ω} is the resistance of the test line at the reference temperature

T_{ref} {ºC}; ΔR {Ω} is the change in resistance; ΔT {ºC} is the change in temperature that caused the change in resistance.

NOTE 1 Two choices of T_{ref} are in common use: 0 °C and ambient temperature (typically from 24 °C to 27 °C). They are equivalent as long as self-consistent definitions are used. The choice of 0 °C is preferred, since it facilitates a first-glance comparison of interlaboratory experiments and of experiments conducted at different times in the same laboratory.

NOTE 2 For aluminum-based metallizations, the change in resistance of the test line with temperature, $\Delta R/\Delta T$, is approximately constant from room temperature to about 420 °C. For copper-based metallizations, a variation in $\Delta R/\Delta T$ value becomes evident at temperatures as low as 200 °C. Hence, if the TCR is used to calculate the temperature of a copper test line at higher temperatures, a correction factor, F_{corr}, is needed.

temperature coefficients of analog characteristics (α) JESD99C, 12/12

NOTE 1 The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic, e.g., α_{EG} for the temperature coefficient of the gain error.

NOTE 2 Temperature coefficients of analog characteristics are usually specified in "parts per million (relative to the full-scale value) per degree Celsius", that is, in "ppm/ºC".

temperature-compensated voltage-reference diode: A voltage-regulator diode that is designed to have minimal changes in the regulated voltage over a broad temperature range. (Ref. JESD211.) JESD77D, 8/12 JESD211, 12/09

NOTE A temperature-compensated voltage-reference diode is often provided with one or more forward-biased p-n junctions placed in series with a Zener p-n junction to offset or compensate the positive temperature coefficient of the Zener. This series combination may also involve more than one Zener p-n junction within the temperature-compensated voltage-reference diode, particularly for higher voltages.

temperature cycle time: The time interval between one high-temperature extreme and the next, or from one low-temperature extreme and the next. JESD22-A105C, 1/04

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

temperature derating: A specification showing how a rating stated at a particular temperature is reduced at higher temperatures. JESD77D, 8/12 JESD210, 12/07

NOTE 1 Derating is usually expressed graphically or in terms of derating factors (e.g., mA/°C or mW/°C).

NOTE 2 For ABDs, derating applies to ratings for peak pulse current (I_{PPSM}), peak pulse power (P_{PPSM}), and average power dissipation ($P_{M(AV)}$).

NOTE 3 Average power ratings are derated to zero at the maximum-rated junction temperature. Peak pulse power ratings may exceed zero at the maximum-rated junction temperature.

temperature profile: (1) A graphical portrayal of temperature experienced by an assembly as it passes through a soldering process. JEP153,1/08

(2) A graphical portrayal of the spatial temperature distribution in an oven.

temperature-sensitive parameter (TSP) (used for the measurement of thermal characteristics): An electrical parameter of a semiconductor device that varies directly with junction temperature in a linear or very nearly linear fashion. JESD51-1, 12/95 JESD51-13, 6/09

temporary chip attach (TCA): The processes used to temporarily join a die to a substrate and then to remove the die from the substrate. JESD22-B118, 3/11

NOTE The attachment is usually used to perform test and/or burn-in to produce a known good die.

terabyte (TB) (in reference to solid-state drive capacity): A memory capacity approximately equal to 1×10^{12} bytes. JESD218A, 2/11

NOTE Contrast with terabyte commonly used as a prefix to units of semiconductor storage capacity and meaning 2^{40} [1 099 511 627 776] bytes.

terabytes written (TBW) rating: Synonym for “endurance rating”.

terminal (1) **(of a semiconductor device):** An externally available point of connection. JESD10, 1/76# JESD22-B108B, 9/10 JESD30E, 8/08 JESD77D, 8/12 JESD99C, 12/12 JESD282-B, 4/00

NOTE The use of the term “termination” as a synonym is deprecated because that term denotes the external elements connected to the terminal.

(2) **(for outline drawing purposes):** That part of the package or device used primarily for making an electrical, mechanical, or thermal connection. Examples of terminals are flexible leads, rigid leads, and studs. RS-308-A, 8/81 Rescinded 5/09

terminal 1 (T1) (of a bidirectional diode thyristor): The terminal that is designated “1” by the manufacturer. JESD77D, 8/12

terminal 2 (T2) (of a bidirectional diode thyristor): The terminal that is designated “2” by the manufacturer. JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
terminal apex: The point on the terminal surface that exhibits the greatest perpendicular distance from the package substrate.	JESD22-B108B, 9/10
terminal capacitance (deprecated)**:** The term "terminal-to-ground capacitance" is preferred.	JESD99C, 12/12
test: The measurement of a parameter and the comparison to a standard.	JEP143C, 7/12
test conditions: The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, and preconditioning vectors applied to a device being tested.	JESD78D, 11/11
test data in (TDI): Serial scan test data input.	JESD21-C, 1/97
test data out (TDO): Serial scan test data output.	JESD21-C, 1/97
test environment: The configuration of conductors and dielectrics used to bring test signals to the device under test in a consistent manner.	JEP123, 10/95
tester strobe time: The time interval from the beginning of a test clock cycle to the instant when an output of a device is observed and compared to an expected result.	JESD12-1B, 8/93 JESD99C, 12/12
test function (TF): On a memory, the input that, when true, causes built-in on-chip test logic to be actuated and the part to go into its test mode of operation.	JESD21-C, 1/97
test line: A metallization line, of specified dimensions, whose length is defined by the position of the two voltage taps for single-level structures or, for multi-level structures, by the position of the vias that locate the taps in a different metal level. NOTE 1 The major portion of the test-line is assumed to have a uniform cross-sectional area without significant voids. This implies approximately uniform temperature along the length except at the forcing ends, where the temperature gradient should be minimized by proper design to ensure that the test structure is suitable for isothermal tests. NOTE 2 The cross-sectional area of the test line may be either the mean geometrical cross-sectional area or the cross-sectional area calculated from electrical measurements (see 6.3.2 of JESD202).	JESD33B, 2/04# JESD61A.01, 10/07
test method: The instructions for executing a test or applying a stress.	JEP143C, 7/12
test mode select (TMS): A control input that enables the scan test clock and is used to select test modes.	JESD21-C, 1/97
test pattern: (1) A set of test vectors.	JESD12-5, 8/88
(2) A circuit or elements processed in the semiconductor wafer to act as test sites for monitoring fabrication processes.	JESD99C, 12/12
test-pattern fault coverage: The ratio of the total number of detected faults to the total number of detectable faults.	JESD12-5, 8/88
test port clock (TCK): Serial scan test clock input.	JESD21-C, 1/97
test port reset (TRST): Serial scan test port reset	JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

test program: A test pattern and instructions suitable for use on automatic test equipment. JESD12-5, 8/88

NOTE A test program may be used to perform functional and parametric (ac, dc, or other) tests.

test signal: The nature of the electrical signal used to measure electrical model parameters. It can be characterized by risetime, pulse shape, frequency, amplitude, etc. JEP123, 10/95

test structure: A passive metallization structure, including a test line, that is fabricated on a semiconductor wafer by procedures used to manufacture microelectronic integrated devices. JESD33B, 2/04# JESD61A.01, 10/07

NOTE Connections are provided to make Kelvin-like resistance measurements of the test line, i.e., two taps for sensing voltage when two other terminals force a current through the line. Typically, these terminals are located at the ends of the test line in single-level structures, while multi-level structures have vias that connect the ends of the test line to the over- or underlying metal level in which the terminals are located.

test synthesis: Creation and insertion of test circuitry to improve testability of a design. JESD12-1B, 8/93 JESD99C, 12/12

test vector: A single instance of input stimuli and expected output responses. JESD12-5, 8/88

test vehicle: A circuit or integrated circuit designed for the purpose of evaluating one or more device characteristics. JESD89A, 10/06

NOTE 1 For the purposes of JESD89, the characterization is the soft-error sensitivity of a particular process technology, but the test vehicle can incorporate other structures used to characterize different parameters, such as yield, speed, voltage margin, etc.

NOTE 2 This test vehicle is not typically a product but is a dedicated component or section of an integrated circuit chip designed to be used in predicting the soft error rate of a product.

tetrode field-effect transistor: A field-effect transistor having two independent gate regions, a source region, and a drain region. (Ref. IEC 747-8.) JESD24, 7/85 JESD77D, 8/12

NOTE 1 A substrate terminated externally and independently of other elements is considered a gate for the purposes of this definition.

NOTE 2 If no confusion is likely, the term may be abbreviated to “field-effect tetrode”.

TF: See “test function”.

thermal impedance, (transient) (Z_{θ}, $Z_{\theta(t)}$, or Z_{th}) (formerly $\theta_{(t)}$): The change in temperature difference between two specified points or regions that occurs during a time interval divided by the step-function change in power dissipation that occurred at the beginning of the interval and caused the change in temperature difference. JESD10, 1/76# JESD51-1, 12/95# JESD51-13, 6/09# JESD77D, 8/12 JESD282-B, 4/00

thermal impedance, junction-to-ambient ($Z_{\theta JA}$, $Z_{\theta JA(t)}$, or Z_{thJA}) (formerly $\theta_{J\text{-}A(t)}$): The transient thermal impedance from the semiconductor junction(s) to the ambient. JESD10, 1/76 JESD77D, 8/12

thermal impedance, junction-to-case ($Z_{\theta JC}$, $Z_{\theta JC(t)}$, or Z_{thJC}) (formerly $\theta_{J\text{-}C(t)}$): The transient thermal impedance from the semiconductor junction(s) to a stated location on the case. JESD10, 1/76 JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

thermal impedance, junction-to-lead ($Z_{\theta JL}$ or Z_{thJL}): The transient thermal impedance from the semiconductor junction(s) to a stated location on a lead. JESD77D, 8/12

thermal impedance, junction-to-mounting-surface ($Z_{\theta JM}$ or Z_{thJM}): The transient thermal impedance from the semiconductor junction(s) to a stated location on the mounting surface. JESD77D, 8/12

thermal impedance, junction-to-reference point ($Z_{\theta JX}$): The transient thermal impedance from the junction to a reference point. For a specified power pulse duration, $Z_{\theta JX}$ is given by JESD24-3, 11/90
JESD24-4, 11/90

$$Z_{\theta JX} = (T_{Jf} - T_{Ji} - \Delta T_X) / P_H$$

where

T_{Jf} is the junction temperature at the end of the power pulse;

T_{Ji} is the junction temperature before the start of the power pulse;

ΔT_X is the change in reference point temperature during the heating pulse. For short heating pulses, e.g., during die attach evaluation, this term is normally negligible;

P_H is the magnitude of the heating power pulse applied to the device under test, i.e., the product of I_H and V_H.

thermal resistance, (steady-state) (R_θ or R_{th}) (formerly θ): The temperature difference between two specified points or regions divided by the power dissipation, under conditions of thermal equilibrium. JESD10, 1/76
JESD24, 7/85
JESD51-1, 12/95#
JESD51-13, 6/09#
JESD77D, 8/12
JESD99C, 12/12
JESD282-B, 4/00

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

thermal resistance (of a test line used for electromigration stressing): The change in mean temperature of the test line divided by the change in power dissipation in the line, as described in the following equation: JESD61A.01, 10/07

$$R_{th} = \Delta T/\Delta P$$

where

R_{th} is the thermal resistance (ºC/W);
ΔT is the change in mean temperature (ºC);
ΔP is the change in power dissipation that caused the change in mean temperature (W).

NOTE 1 It is assumed that any electromigration damage that may occur during the isothermal test does not affect the thermal resistance of the line to the first order.

NOTE 2 The thermal resistance R_{th} is defined assuming temperature uniformity along the test line and the linear dependence of T on P: in a plot of T versus P, R_{th} is the slope of the straight line. R_{th} is dependent on the geometry of the test structure and on the thermal conductance between the test line and the ambient. On the other hand, because the thermal conductance of the materials in the path of the heat flow from the test structure is temperature dependent, the T-versus-P relationship is not linear; i.e., the slope of this curve will gradually decrease with increasing power dissipation. In other words, R_{th} is temperature dependent. Therefore, over a limited range of temperatures (typically 50 °C), the T-versus-P relationship can still be considered linear,

$$T = T_0 + R_{th} \times P.$$

As a consequence, a best straight-line fit of equation (2), using some measured (T, P) data pairs in this limited temperature range, can be used to estimate the thermal resistance value, R_{th} , and the thermal resistance intercept, T_0.

thermal resistance, case-to-ambient ($R_{\theta CA}$ or R_{thCA}): The thermal resistance from the device case to the ambient. JESD77D, 8/12
JESD99C, 12/12

thermal resistance, junction-to-ambient ($R_{\theta JA}$ or R_{thJA}) (formerly θ_{JA}): The thermal resistance from the virtual junction [operating protion] of a semiconductor device to a natural convection [still-air] environment surrounding the device. JESD10, 1/76#
JESD51-1, 12/95
JESD51-13, 6/09
JESD77C, 10/09
JESD99C, 12/12

thermal resistance, junction-to-case ($R_{\theta JC}$ or R_{thJC}) (formerly θ_{JC}): (1) The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a stated location on the case. JESD10, 1/76
JESD77C, 10/09
JESD99C, 12/12

(2) The thermal resistance from the virtual junction(s) of a semiconductor device to the outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface. JESD51-1, 12/95
JESD51-13, 6/09

thermal resistance, junction-to-defined environment ($R_{\theta JX}$) (formerly θ_{JX}): The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a defined nonstandard environment surrounding the device. JESD51-1, 12/95
JESD51-13, 6/09

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
thermal resistance, junction-to-fluid: The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a fluid environment surrounding the device. NOTE See also "thermal resistance, junction-to-liquid".	JESD51-13, 6/09
thermal resistance, junction-to-lead ($R_{\theta JL}$ or R_{thJL}): The thermal resistance from the semiconductor junction(s) to a stated location on a lead.	JESD77D, 8/12
thermal resistance, junction-to-lead ($R_{\theta JL}$ or R_{thJL}): The thermal resistance from the semiconductor junction(s) to a stated location on a lead.	JESD77D, 8/12 JESD51-13, 6/09#
thermal resistance, junction-to-liquid ($R_{\theta JL}$) (formerly θ_{JL}): The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a liquid environment surrounding the device. NOTE See also "thermal resistance, junction-to-fluid".	JESD51-1, 12/95
thermal resistance, junction-to-mounting-surface ($R_{\theta JM}$ or R_{thJM}): The thermal resistance from the semiconductor junction(s) to a stated location on the mounting surface.	JESD10, 1/76 JESD77D, 8/12
thermal resistance, junction-to-moving air ($R_{\theta JMA}$) (formerly θ_{JMA}): The thermal resistance from the operating portion of a semiconductor device to a forced convection (moving-gas) environment surrounding the device; the gas is assumed to be air unless otherwise defined.	JESD51-1, 12/95 JESD51-13, 6/09
thermal resistance, junction-to-reference point ($R_{\theta JR}$) (formerly θ_{JR}): The thermal resistance from the virtual junction [operating portion] of a semiconductor device to a defined reference point within the specified environment surrounding the device.	JESD51-1, 12/95 JESD51-13, 6/09
thermocouple: A temperature measurement sensor comprising two dissimilar metals intimately joined together in a bead at one end that produces a small thermoelectric voltage, corresponding to the temperature of the bead.	JEP140, 6/02
thermomechanical analysis (TMA): A technique used to characterize materials by varying temperature, force, and atmosphere, and then measuring the change in properties, e.g. dimensions.	JESD22-B113A, 9/12
thermometry sensor: A device and/or material used in measuring the temperature of a system or the ability of systems to transfer heat.	JEP140, 6/02
thinned wafer: A wafer that is reduced in thickness to a specified value.	JESD22-B118, 3/11
3-D chip stack: Two or more chips vertically connected to form a unified electrical structure in a single package.	JEP158, 11/09
three-phase bridge converter: A bridge circuit that produces a variable dc output from a three-phase ac input.	JESD14, 11/86
three-phase [four-phase] [multiphase] charge-coupled device: A charge-coupled device in which the direction of the charge packet flow is determined by the sequence of the three [four] [five or more] clock phases.	JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

three-phase inverter: A circuit that produces a three-phase ac output from a dc input. JESD14, 11/86

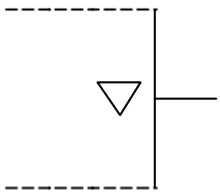
three-state bus: A bus on which each output port can be placed at a logic high level or a logic low level or in a high-impedance state. JESD12-1B, 8/93 JESD99C, 12/12

three-state circuits (internal and output): Cells or macros whose outputs can be placed in a high-impedance state and can also supply low-impedance high and low logic levels. JESD12-4, 4/87

three-state output: A bipolar output both of whose active devices can be caused to be in the off state at the same time, thus presenting a high-impedance state at the output similar to the off state of an open-circuit output. JESD99C, 12/12

NOTE When the active devices are not in their simultaneous off states, the output acts like a totem-pole output.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



threshold crossing: The point at which a logic signal transitions from one logic state to another. JESD65B, 9/03

threshold LET: The minimum linear energy transfer (LET) required to cause a single-event effect (SEE). JESD57, 12/96

threshold level: The concentration level that defines the limit equal to or above which the presence of a substance in a product shall be declared based on the requirements of JIG-101. JIG-101 Ed 2.0, 4/09

through-silicon via (TSV): A conductive via that runs vertically through a silicon chip and electrically connects structures on the top side and the bottom side of the chip. JEP158, 11/09

through-transmission acoustic microscope: An acoustic microscope that transmits ultrasound completely through the sample from a sending transducer to a receiver on the opposite side. J-STD-035, 5/99

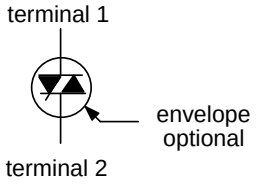
through-transmission mode: See “acoustic data, through-transmission mode”.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

thyristor, bidirectional diode: A two-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the thyristor voltage-current characteristic. JESD77D, 8/12

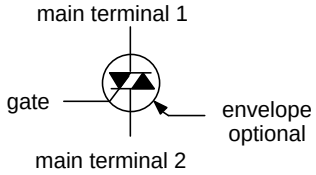
Graphic symbol (ref. IEEE Std 315):



thyristor, bidirectional triode: A three-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal characteristic. JESD77D, 8/12

NOTE Usually the configuration is pnpnp or npnpn.

Graphic symbol (ref. IEEE Std 315):

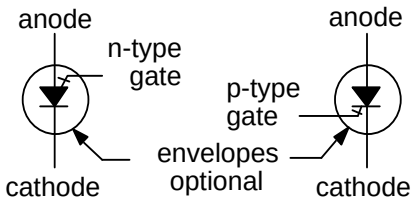


thyristor-diode SPCM: A semiconductor power-control module consisting of thyristors and rectifier diodes, with the control signal(s) supplied from an external source. JESD14, 11/86

thyristor, gate-turn-off, (asymmetrical): A gate-turn-off thyristor whose rated reverse voltage is significantly lower than its rated off-state voltage. JESD77D, 8/12

thyristor, gate-turn-off, (reverse-blocking); GTO thyristor: A reverse-blocking triode thyristor that can be switched from the on state to the off state as well as from the off state to the on state by applying control signals of appropriate polarity to the gate terminal. JESD77D, 8/12

Graphic symbols (ref. IEEE Std 315):



thyristor, gate-turn-off, reverse-conducting: A reverse-conducting triode thyristor that can be switched from the on state to the off state as well as from the off state to the on state by applying control signals of appropriate polarity to the gate terminal. JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

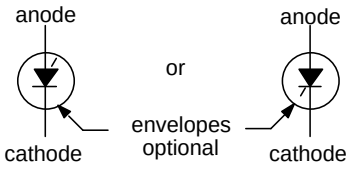
thyristor, gate-turn-off, symmetrical: A gate-turn-off thyristor whose rated reverse voltage and rated off-state voltage are essentially equal. JESD77D, 8/12

thyristor, n-gate: A unidirectional triode thyristor whose gate terminal is connected to the n-region nearest the anode and that is normally switched to the on-state by applying a negative signal to the gate terminal with respect to the anode terminal. JESD77D, 8/12

thyristor, p-gate: A unidirectional triode thyristor whose gate terminal is connected to the p-region nearest the cathode and that is normally switched to the on-state by applying a positive signal to the gate terminal with respect to the cathode terminal. JESD77D, 8/12

thyristor, reverse-blocking diode: A unidirectional diode thyristor that exhibits a blocking state in the reverse direction. JESD77D, 8/12

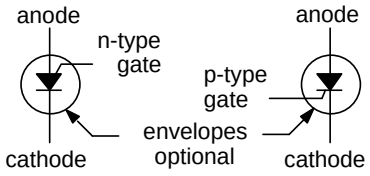
Graphic symbols (ref. IEEE Std 315):



thyristor, reverse-blocking triode: A unidirectional triode thyristor that exhibits a blocking state in the reverse direction. JESD77D, 8/12

NOTE If no ambiguity is likely to occur, the term may be abbreviated to “thyristor”.

Graphic symbols (ref. IEEE Std 315):



thyristor, reverse-blocking triode, asymmetrical: A reverse-blocking triode thyristor whose rated reverse voltage is significantly lower than its rated off-state voltage. JESD77D, 8/12

thyristor, reverse-blocking triode, (symmetrical): A reverse-blocking triode thyristor whose rated reverse voltage and rated off-state voltage are essentially equal. JESD77D, 8/12

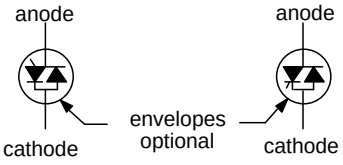
The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

thyristor, reverse-conducting diode: A unidirectional diode thyristor that conducts large currents in the reverse direction at reverse voltages comparable in magnitude to the forward on-state voltage. JESD77D, 8/12

NOTE Thyristors intended for use as surge protective devices and meeting this definition are referred to as forward-conducting rather than reverse-conducting.

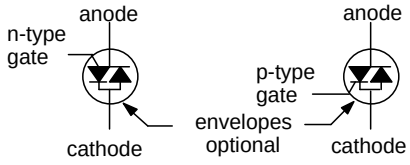
Graphic symbols:



thyristor, reverse-conducting triode: A unidirectional triode thyristor that conducts large currents in the reverse direction at reverse voltages comparable in magnitude to the forward on-state voltage. JESD77D, 8/12

NOTE Thyristors intended for use as surge protective devices and meeting this definition are referred to as forward-conducting rather than reverse-conducting.

Graphic symbols:



thyristor (general)**:** A semiconductor device that is capable, due to internal feedback, of assuming either of two stable states and maintaining the assumed state either with no sustained control current or voltage or at least with considerably less than that necessary to initially establish that state, and that is designed to operate as a switch for the principal or on-state current. JESD77D, 8/12

NOTE 1 A thyristor is a switch that can be switched on either for only one direction of the principal current (a unidirectional thyristor) or for both directions (a bidirectional thyristor).

NOTE 2 The usual configuration is a pnpn configuration to which can be added other elements needed for additional functions.

NOTE 3 The term “thyristor” may be used for any member of the pnpn family (including devices having more than four layers) when such use does not result in ambiguity or misunderstanding. In particular, the abbreviated term “thyristor” is widely used for the reverse-blocking triode thyristor, formerly called “SCR”, “semiconductor controlled rectifier”, or “silicon controlled rectifier”.

thyristor SPCM: A semiconductor power-control module consisting only of thyristors, with the control signal(s) supplied from an external source. JESD14, 11/86

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
thyristor surge protective device (TSPD): A thyristor that is intended to operate as a transient voltage suppressor.	JESD66, 11/99# JESD77D, 8/12
thyristor surge suppressor (TSS): Synonym for "thyristor surge protective device".	JESD66, 11/99# JESD77D, 8/12
thyristor, unidirectional diode: A two-terminal thyristor that can switch only when the anode voltage is positive.	JESD77D, 8/12
thyristor, unidirectional triode: A three-terminal thyristor that can switch only when the anode voltage is positive. NOTE In this definition, a second cathode or anode terminal for connecting to the control circuit is not counted.	JESD77D, 8/12
thyristor voltage (of a bidirectional diode thyristor): The voltage between the two terminals. NOTE The polarity of the thyristor voltage (with regard to terminals 1 and 2) must be specified.	JESD77D, 8/12
tie bar: Additional metal, at the outside ends of the leads, that connects together the individual leads to protect the leads from bending or damage and/or to aid in holding during assembly, plating, or handling operations. NOTE Tie bars are incorporated into the lead frame design and can be manufactured by stamping, etching, or welding methods.	JESD9B, 5/11
tier: Synonym for "stratum".	JEP158, 11/09
time-dependent effect (TDE): A change in a transistor or integrated circuit parameter caused by the time-dependent growth and annealing effects of ionizing-radiation-induced trapped charge and interface states.	JEP133C, 1/10
time-of-flight (in acoustic microscopy) (TOF): (1) In the reflective mode, the time it takes for the acoustic pulse to travel from a single transducer/receiver to the interface of interest and back. (2) In the through-transmission mode, the time it takes for the acoustic pulse to travel from the sending transducer through the sample to the receiving transducer.	J-STD-035, 5/99
time to failure (in a SWEAT) (t_F): The time it takes for the resistance of the test structure to first equal or exceed the failure resistance criterion, R_{FC}, while the structure is under stress from the SWEAT algorithm.	JEP119A, 8/03
time to reach the specified failure criterion (t_{tar}): The time it takes under specific conditions for the value of a particular parameter to reach a specified failure criterion. See also "time to target".	JESD28-1, 9/01#
time to target (t_{tar}): The time it takes under specific conditions for the value of a particular parameter of a device to change by a specified amount or to a specified value.	JESD28-A, 12/01# JESD60A, 9/04 JESD90, 11/04
time-to-whisker-nucleation (TTWN): The incubation time interval before whiskers begin to grow.	JEP122G, 10/11

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
timing library: The timing models of a set of macrocells and/or macro functions.	JESD12-1B, 8/93 JESD99C, 12/12
timing-related input pin: A pin such as clock, crystal oscillator, charge pump circuit, etc., required to place the device under test in a normal operating mode.	JESD78D, 11/11
timing simulation: The process of exercising the functional and timing models of a particular netlist by applying input stimuli to observe the timing responses.	JESD12-1B, 8/93 JESD99C, 12/12
tin and tin alloy surface finish: Tin-based outer surface finish for external component terminations and other exposed metal.	JESD201A, 8/08
tin whisker mitigation practice: The process(es) performed during the manufacture of a component to reduce the propensity for tin whisker growth by minimizing the surface finish internal compressive stress.	JESD201A, 8/08 JP002, 3/06
TMA: See "thermomechanical analysis".	
TMS: See "test mode select".	
TOF: See "time-of-flight".	
tool: A program that performs a function within a design automation system.	JESD12-1B, 8/93 JESD99C, 12/12
tool failure: A failure of stud, fixture, or other mechanical apparatus that prevents the execution of a tensile pull on the die.	JESD22-B109A, 1/09
top-down design: The process of designing a circuit hierarchically starting at the highest level followed by detailed design at a lower level.	JESD12-1B, 8/93 JESD99C, 12/12
topology: The surface layout design of a microcircuit, applied chiefly to the preparation of the masks used in fabrication.	JESD99C, 12/12
top-side die-atach substrate view area: The interface between the encapsulant and the die side of the die attach surrounding the die. (Refer to Type III in Annex A of J-STD-035.)	J-STD-035, 5/99
total charge (in a bucket-brigade device): The total electric charge stored in a potential well or in a discrete region of the device.	JESD99C, 12/12
total error; absolute accuracy error (of a linear digital-to-analog converter) (E_T): The difference (positive or negative) between the actual step value and the nominal step value for any step. NOTE 1 If this error is expressed as a relative value, the term "relative accuracy error" should be used rather than "absolute accuracy error" or "total error". NOTE 2 This error includes all contributions from offset error, gain error, and linearity error.	JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

total error; absolute accuracy error (of a linear analog-to-digital converter) (E_T): The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step. JESD99C, 12/12

NOTE 1 If this error is expressed as a relative value, the term "relative accuracy error" should be used rather than "absolute accuracy error" or "total error".

NOTE 2 This error includes all contributions from offset error, gain error, linearity error, and the inherent quantization error.

total harmonic distortion (THD): The ratio, expressed as a percentage, of the rms voltage of all harmonics present in the output to the total rms voltage of the output, for a pure sine-wave input. JESD99C, 12/12

total ionizing dose (TID) effects: Circuit degradation or failure resulting from radiation-induced charge trapped in insulating layers (usually oxides). JEP133C, 1/10

total phase offset ($t_{(\phi)tot}$): The sum of static phase offset, dynamic phase offset, and phase jitter. JESD65B, 9/03

total power dissipation: The sum of the forward and reverse power dissipations. JESD77D, 8/12
JESD282-B, 4/00

total quality management (TQM): The management of company resources with the exclusive focus on customer satisfaction as the means of achieving sustained financial success. It combines the efforts of all employees to develop, implement, continually assess, and improve the effectiveness of its processes and systems in support of the customers' needs. JEP132, 7/98

total response time (t_{tot}, $t_{tot(r)}$, and $t_{tot(f)}$): The sum of delay time, rise or fall time, and ripple time. (Ref. IEC 747-3.) JESD99C, 12/12

totem-pole output: A bipolar output whose active devices are so controlled that as the resistance of one increases, the resistance of the other decreases so that, according to the relative states of the two active devices, the output voltage can swing between levels approaching the two supply voltages. JESD99C, 12/12

NOTE 1 The term "totem-pole output", as commonly used, does not include three-state outputs.

NOTE 2 No standard qualifying symbol, as part of a graphic symbol, exists to designate the totem-pole output. In ANSI/IEEE Std 91 and IEC 617-12 these outputs are identified by the absence of a qualifying symbol.

TQM: See "total quality management".

transfer acknowledge output (GSF; QSY): On a device having both serial and parallel access ports, the output that, when true, signifies that a transfer of data from the parallel to the serial port, in certain special transfer cycles, has been completed. In devices and modules that have multiple QSFs, the QSFs are numbered beginning with 0. JESD21-C, 1/97

transfer channel: The region of a charge-transfer device within which the charge flow is confined. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

transfer gate: A gate electrode, isolated from the channel by an insulating layer or junction, to which voltage is applied in order to transfer charge. JESD99C, 12/12

transfer inefficiency product (in a charge-transfer device) (nε): The product of the number of transfers (n) and the charge-transfer inefficiency (ε). JESD99C, 12/12

transferred-electron diode: A semiconductor microwave diode that exhibits negative resistance arising from the transferred-electron effect. JESD77D, 8/12

NOTE 1 The transferred-electron effect is the generation of bulk negative differential conductivity in compound semiconductor devices that have multiple energy valleys when the applied electrical field is greater than the critical value at which electrons transfer from (1) a lower energy valley in which they have greater mobility and smaller effective mass to (2) a higher energy valley in which they have smaller mobility and greater effective mass.

NOTE 2 The term "energy valley" refers to a valley in an energy-versus-momentum profile.

transient thermal impedance ($Z_{\theta(t)}$) (formerly $\theta_{(t)}$): See "thermal impedance, (transient)".

transient voltage suppressor (TVS): A semiconductor device that is intended to limit voltage transients by conducting surge currents. JESD77D, 8/12

transistor (general): A semiconductor device, capable of providing power amplification, whose basic functional structure includes the series connection of a supply region, a control region, and a collection region, and whose output is a simple, continuous function of the input. JESD10, 1/76
JESD77D, 8/12

transistor, bipolar: A transistor in which electrical conduction depends on the flow of both majority and minority carriers. JESD99C, 12/12

transistor, collector field-effect: A modified junction field-effect transistor, used as a constant-current source, whose gate is connected to the substrate. JESD99C, 12/12

NOTE The channel is formed from the epitaxial material that in other regions forms the collectors of the bipolar transistors.

transistor-diode SPCM: A semiconductor power-control module consisting of transistors and rectifier diodes, with the control signal(s) supplied from an external source. JESD14, 11/86

transistor, field-effect (FET): A transistor in which the conduction is due entirely to the flow of majority carriers and can be varied by an electric field produced by an auxiliary source. JESD99C, 12/12

transistor, insulated-gate field-effect (IGFET): A field-effect transistor having one or more gate electrodes that are electrically insulated from the channel. JESD99C, 12/12

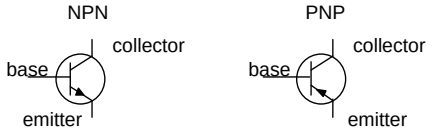
transistor, junction-gate field-effect (JFET): A field-effect transistor having one or more gates that form p-n junctions with the channel. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

transistor, junction, multijunction type: A transistor having a base and two or more junctions. JESD10, 1/76

Graphic symbols for triode transistors (Ref. ANSI Y32.2):



NOTE In the graphic symbols, the envelope is optional if no element is connected to the envelope.

transistor, lateral: A transistor whose emitter-base and collector-base junctions are formed in separate topological areas of a microcircuit and in which the charge carriers flow between these junctions in a plane parallel to the surface. JESD99C, 12/12

transistor, metal-oxide-semiconductor field-effect (MOSFET): An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material. JESD99C, 12/12

transistor SPCM: A semiconductor power-control module consisting only of transistors, with the control signal(s) supplied from an external source. JESD14, 11/86

transistor, substrate pnp: A pnp transistor formed from the base and collector regions of a normal npn bipolar transistor and the substrate. JESD99C, 12/12

transistor, unipolar: A transistor in which the electrical conduction is due entirely to the flow of majority carriers. JESD99C, 12/12

transition frequency; frequency at which small-signal forward current transfer ratio (common-emitter) extrapolates to unity (f_T): The product of the modulus (magnitude) of the common-emitter small-signal short-circuit forward current transfer ratio, h_{fe}, and the frequency of measurement when this frequency is sufficiently high that the modulus (magnitude) of h_{fe} is decreasing with a slope of approximately 6 dB per octave. (Ref. IEEE Std 255.) JESD10, 1/76

transition region, (physical) (within a semiconductor material): The physical region between two homogeneous semiconductor regions that have different electrical properties. JESD77D, 8/12

transition time (t_t): The time interval between two specified levels, one near the beginning and one near the end of the same pulse edge. JESD99C, 12/12

transition time, high-to-low-level; fall time (t_{THL}): The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level. JESD99C, 12/12
JESD100-B, 12/99

transition time, low-to-high-level; rise time (t_{TLH}): The time interval between the specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level. JESD99C, 12/12
JESD100-B, 12/99

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Terms, abbreviations, letter symbols, and definitions **References**

TRAPATT [trapped plasma avalanche transit-time] diode; avalanche diode operating in TRAPATT mode: A semiconductor microwave diode that, when its junction is biased into avalanche, exhibits a negative resistance at frequencies below the transit-time frequency range of the diode due to generation and dissipation of trapped electron-hole plasma resulting from the intimate interaction between the diode and a multiresonant microwave cavity. JESD77D, 8/12

trend: The movement of a process in a consistently increasing or decreasing direction. EIA-557-B, 2/06

TRG(n): See "data-transfer/output-enable input".

triac: An alternative term for "thyristor, bidirectional triode". JESD77D, 8/12

triboelectric charging: The generation of electrostatic charge that results from the separation of two pieces of material in intimate contact, when at least one is an insulator). JESD625B, 1/12

NOTE Substantial static electricity can be generated by contact and separation of two materials or by rubbing two substances together.

trigger duration: The duration of an applied pulse from the trigger source. JESD78D, 11/11

trigger pulse (1) **(general):** A positive or negative current pulse or voltage pulse applied to any terminal or node in an attempt to induce a specific effect. JESD77D, 8/12
JESD99C, 12/12

NOTE A clock signal or other periodic input for the normal functioning of a device is sometimes called a trigger pulse.

(2) **(in latch-up testing):** A positive or negative current pulse or voltage pulse applied to any terminal under test in an attempt to induce latch-up. JESD78D, 11/11

triode field-effect transistor: A field-effect transistor having a gate, a source, and a drain. (Ref. IEC 747-8.) JESD24, 7/85
JESD77D, 8/12

NOTE If no confusion is likely, the term may be abbreviated to "field-effect triode".

TRST: See "test port reset".

true-dose-rate effect: An effect, on a transistor or integrated circuit during low-dose-rate irradiation, that cannot be reproduced with a high-dose-rate irradiation and a subsequent equivalent time anneal. JEP133C, 1/10

NOTE Typically the equivalent time anneal is the difference in time to achieve the same total dose at a high dose rate as at a low dose rate.

true position: The theoretically exact location of a feature established by basic dimensions. JESD95-1, 3/97

truth table: A tabulation relating all output logic states to all necessary or possible combinations of input logic states for sufficient successive time intervals (t_n, t_{n+1}) to completely characterize the static and dynamic functions of the digital integrated circuit, expressed in logic states or appropriate symbols. JESD99C, 12/12

NOTE Contrast with "function table".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

TSOP types I and II packages (TSOP1; TSOP2): Small-outline packages having gull-wing leads and whose thickness is substantially less than that of the standard SOG package. TSOP1 has the leads on the ends or short edges of the package while TSOP2 has the leads on the sides or long edges of the package. The lead pitch is often finer than that commonly used in the standard SOG package. JESD21-C, 1/97

TSP: See "temperature-sensitive parameter".

TSPD: See "thyristor surge protective device".

TSS: See "thyristor surge suppressor".

TSV: See "through-silicon via".

tuning diode: A varactor diode used for rf tuning. JESD77D, 8/12

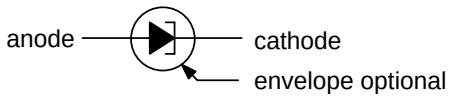
NOTE This includes functions such as automatic frequency control (AFC) and automatic fine tuning (AFT).

tunnel diode: A semiconductor diode in which quantum-mechanical tunneling leads to a region of negative slope in the forward direction of the current-voltage characteristic. JESD77D, 8/12

NOTE 1 The current is typically a single-valued function of voltage.

NOTE 2 In practice, the distinction between tunnel diodes and backward diodes is based on circuit application emphasis of the negative-resistance property (tunnel diode) or the low-level rectification property (backward diode).

Graphic symbol (ref. IEEE Std 315):



turn-off time (t_{off}): The sum of storage time and fall time, i.e., $t_s + t_f$. JESD10, 1/76

turn-on time (t_{on}): The sum of delay time and rise time, i.e., $t_d + t_r$. JESD10, 1/76

TVS: See "transient voltage suppressor".

2-D code label (matrix): A label that contains data in two dimensions as either stack or matrix types. J-STD-609A.01, 2/11

NOTE This was originally published as "2D code label (matrix)".

two-phase charge-coupled device: A charge-coupled device with asymmetrical potential wells that provide a unidirectional flow of charge packets under the control of two sequential clock phases. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

typical use conditions: The normal environmental and/or operating ranges that the application is known to function within. JEP149, 11/04

NOTE….This is a subset of the application use conditions.

U

U: See "upper byte".

UART: See "universal asynchronous receiver transmitter".

UB: See "upper-byte enable".

UBER: See "uncorrectable bit-error rate".

UBER: See "uncorrectable bit error rate; uncorrectable bit error ratio".

UBM: See "under-bump metal" and "under-bump metallurgy".

UJT: See "unijunction transistor".

ultraviolet-erasable programmable read-only memory (UV-EPROM): Synonym for "erasable programmable read-only memory (EPROM)". JESD100-B, 12/99

uncased device: A device with some portion of the die exposed. JESD30E, 8/08

NOTE….Usually the chip has bonding pads, bumps, etc. that may be bonded to pads or lands on a lead-frame, tape, substrate, or printed wiring board.

uncommitted logic array: Synonym for "gate array integrated circuit".

uncorrectable bit-error rate (UBER): A metric for data corruption rate equal to the number of data errors per bit read after applying any specified error-correction method. JESD22-A117B, 3/09

uncorrectable bit error rate; uncorrectable bit error ratio (UBER): A metric for the rate of occurrence of data errors that is the number of data errors divided by the number of bits read. JESD218A, 2/11

under-bump metal (UBM); bump-limiting metal (BLM): The metal layers located between the solder bump or column and the die. JEP156, 3/09
JEP158, 11/09

under-bump metallization (UBM): A patterned, thin-film stack of material that provides 1) an electrical connection from the silicon die to a solder bump; 2) a barrier function to limit unwanted diffusion from the bump to the silicon die; and 3) a mechanical interconnection of the solder bump to the die through adhesion to the die passivation and attachment to a solder bump pad. JEP154, 1/08

under-bump metallurgy (UBM): The metal layers located between the solder bump and the die. JESD22-B109A, 1/09

undercut: The reduction of the cross section of a material caused by etching action spreading beneath the edge of the photoresist or other masking films. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

underfill: The adhesive material applied between the solder bump side of the flip chip die and the substrate. JESD22-B109A, 1/09

underlay: A plated barrier layer between the base metal and the tin finish. JP002, 3/06

underplate: Plated layers between the base metal and the outer surface finish. JESD201A, 8/08

underplating; underplate: Any plating layers between the outermost plating layer and the base metal. JESD9B, 5/11
JESD201A, 8/08#

NOTE In JESD201A, "outermost plating layer" is referred to as "outer surface finish".

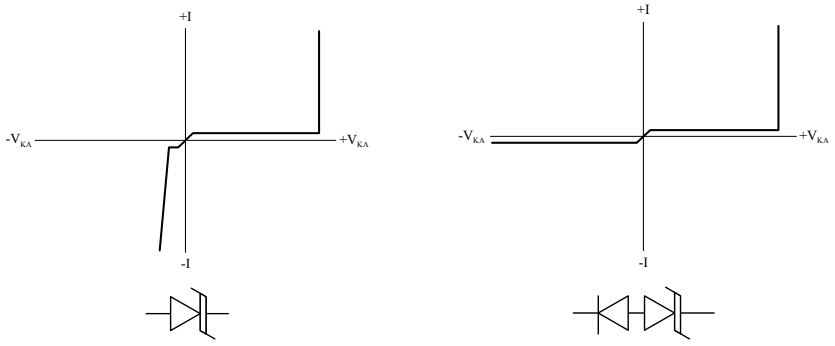
undetectable fault: A functional fault for which no test pattern can be created that will cause the effects of the fault to be observable at an externally accessible node. JESD12-5, 8/88

undetected fault: A functional fault that causes effects that are not observed at an externally accessible node when the circuit is exercised by the existing test pattern. JESD12-5, 8/88

uniaxial strain gage: A strain gage incorporating a single strain gage element, which means it is capable of detecting strain along a single axis only. JESD22-B113A, 9/12

unidirectional ABD: A two-terminal ABD with a voltage-current avalanche breakdown characteristic in one direction and either a forward or a blocking characteristic in the other. JESD77D, 8/12
JESD210, 12/07

NOTE Large transient currents will be clamped for positive cathode-to-anode voltages when driven into the avalanche breakdown region with one or more p-n junctions placed in series or parallel with each junction connected in the same direction. Large transient currents may also be clamped for negative cathode-to-anode voltages at significantly lower voltages with the typical forward-conducting characteristics of a single p-n junction (or of multiple p-n junctions connected in the same direction). The most common type of unidirectional ABD has a forward-conducting characteristic.



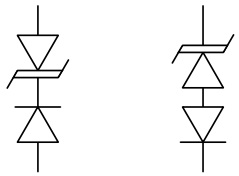
Unidirectional-conducting ABD **Unidirectional-blocking ABD**

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

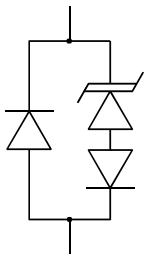
unidirectional-blocking low-capacitance ABD: A two-terminal device that has at least one unidirectional ABD with at least one rectifier p-n junction connected in series in the opposite polarity in order to reduce capacitance. JESD77D, 8/12 JESD210, 12/07

NOTE The unidirectional-blocking low-capacitance ABD is intended to suppress transients in only one direction. The rectifier p-n junction(s) have low capacitance and block in the reverse direction; they are not intended to be operated in their reverse avalanche breakdown regions. The p-n junction that serves as the unidirectional ABD determines which terminal is the anode and which is the cathode; for that determination, the rectifier p-n junction is ignored.



unidirectional-conducting low-capacitance ABD: A two-terminal device comprising a unidirectional-blocking low-capacitance ABD and an anti-parallel diode. JESD77D, 8/12 JESD210, 12/07

NOTE To create a low-capacitance ABD with a forward-conducting, low-voltage characteristic, a low-capacitance diode (such as a rectifier) is placed in anti-parallel to the unidirectional-blocking low-capacitance ABD. This diode must have a reverse blocking voltage greater than the avalanche breakdown voltage of the unidirectional ABD.

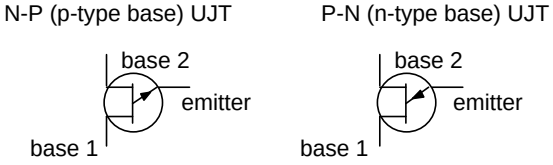


unidirectional thyristor surge protective device: A thyristor surge protective device (TSPD) that can switch in only one quadrant. JESD77D, 8/12

NOTE The two types are forward-conducting TSPDs and reverse-blocking TSPDs.

unijunction transistor (UJT): A three-terminal semiconductor device having one junction and a stable negative-resistance characteristic over a wide temperature range. JESD77D, 8/12

Graphic symbols (ref. IEEE Std 315):



NOTE In the graphic symbols, the envelope is optional if no element is shown connected to the envelope.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

unipolar output: An output that, depending on its design, can either source or sink current, but not both. JESD99C, 12/12

unipolar technology: A technology for producing devices in which electrical conduction is due entirely to the flow of majority carriers. JESD77D, 8/12 JESD99C, 12/12

unit gate size (of a gate array): A physical space occupied by a single gate equivalent, including any area allocated to power connections, signal connections, and isolation requirements. JESD12-1B, 8/93 JESD99C, 12/12

unit load: A measure of load (usually capacitance) equal to that presented by a specified input of a specified primitive. JESD12-1B, 8/93 JESD99C, 12/12

unit symbol: A letter symbol that is used in place of the name of a unit. JESD77D, 8/12 JESD99C, 12/12

NOTE Neither subscripts nor postscripts may be appended to unit symbols as a means of giving information about the special nature of the quantity under consideration. Such information should be conveyed instead by the quantity symbol.

universal asynchronous receiver transmitter (UART): A circuit used in asynchronous data communication applications to provide all the necessary logic to recover data in a serial-in, parallel-out fashion and to transmit data in a parallel-in, serial-out fashion. JESD100-B, 12/99

NOTE This circuit is usually full-duplex (i.e., it can transmit and receive simultaneously) with the option to handle various data word lengths.

universal synchronous/asynchronous receiver transmitter (USART): A circuit used in synchronous/ asynchronous data communication applications to provide all the necessary logic to recover data in a serial-in, parallel-out fashion and to transmit data in a parallel-in, serial-out fashion. JESD100-B, 12/99

NOTE This circuit is usually full-duplex (i.e., it can transmit and receive simultaneously) with the option to handle various data word lengths.

universal synchronous receiver transmitter (USRT): A circuit used in synchronous data communication applications to provide all the necessary logic to recover data in a serial-in, parallel-out fashion and to transmit data in a parallel-in, serial-out fashion. JESD100-B, 12/99

NOTE This circuit is usually full-duplex (i.e., it can transmit and receive simultaneously) with the option to handle various data word lengths.

unprotected ESDS device: An electrostatic-discharge-sensitive device that is not in an electrostatic-discharge-protective package. JESD625B, 1/12

untestable circuit: A circuit that contains logic functions that cannot be tested because of the lack of controllability or observability. JESD12-1B, 8/93 JESD99C, 12/12

upper byte (U): An indicator used in conjunction with a data or control term to signify that the combined term applies to the upper byte of a two-byte data interface device; e.g., UW means write enable, upper-byte. JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

upper-byte enable (on word-wide devices) (UB): An input that, when true, enables the upper byte data input/outputs, terminals DQ8 through DQ15. JESD21-C, 1/97

upper-byte write enable (on word-wide devices) (UW): An input that, when true, causes the data present on the upper byte input/outputs, terminals DQ8 through DQ15, to be written into the addressed cells of the device. JESD21-C, 1/97

usable gates (in a gate array): The typical number of gate equivalents that can be used in a given gate array size. JESD12-1B, 8/93
JESD99C, 12/12

USART: See "universal synchronous/asynchronous receiver transmitter".

use conditions: The environmental factors during manufacturing, shipping, and useful life to which a component is exposed. JESD94A, 7/08

NOTE The useful life consists of the operating, nonoperating, and storage lifetimes.

use condition time (t_U): The time interval equivalent to the ELF test duration, as determined by the product of the acceleration factor and the actual accelerated test time: $A \times t_A$. JEP143C, 7/12
JESD74A, 2/07

used gate (in a gate array): A single gate equivalent that has been interconnected and is employed in the functioning of the circuit. JESD12-1B, 8/93
JESD99C, 12/12

useful life: (1) **(general):** The phase in the life of a device during which the mortality function is relatively constant. JEP122G, 10/11
JEP143C, 7/12

NOTE….As typically used with the bathtub curve, the useful life phase is the bottom of the curve.

(2) **(of an unrepairable unit):** The time interval between the start of use of an unrepairable unit and its statistically expected failure in an application. JEP148A, 12/08

user ID: A programmable space on some devices that allows users to store nonfunctional data of any sort. It is often used to track design revision numbers or other such identifying information. JESD32, 6/96

USRT: See "universal synchronous receiver transmitter".

UV-EPROM: See "ultraviolet-erasable programmable read-only memory".

UW: See "upper-byte write enable".

V

validation: The process of confirming the verification process under use conditions. JEP148A, 12/08

valid time (general)**:** The time interval during which a signal is (or should be) valid. JESD100-B, 12/99

valid time, output data-: The time interval during which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval. JESD100-B, 12/99

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

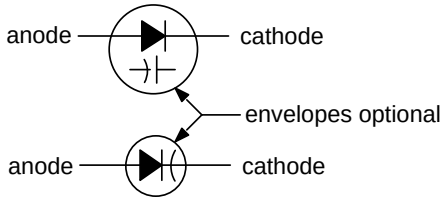
Terms, abbreviations, letter symbols, and definitions **References**

valley point (1) **(of a programmable unijunction transistor characteristic):** The point on the current-voltage characteristic corresponding to the second lowest current at which $dv_{AK}/di_A = 0$ when the gate is biased from a resistive voltage divider. JESD77D, 8/12

(2) **(of a unijunction transistor characteristic):** The point on the emitter current-voltage characteristic corresponding to the second lowest current at which $dv_{EB1}/di_E = 0$. JESD77D, 8/12

varactor diode: A two-terminal semiconductor device in which use is made of the property that its capacitance varies with the applied voltage. JESD77D, 8/12

Graphic symbols (ref. IEEE Std 315):



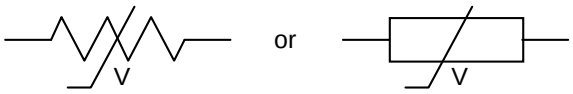
variables data: A measure of a characteristic for which every value within a given interval is possible. EIA-557-B, 2/06
JESD659B, 2/07

variance components analysis: A design-of-experiments (DOE) method of estimating the magnitude and contribution of each investigated source of variability to the total. JEP132, 7/98

variation: The difference among individual outputs of a process. The sources of variation can be grouped into two major classes: common causes and special causes. EIA-557-B, 2/06

varistor: A transient voltage suppressor that is a two-terminal semiconductor device having a nonlinear voltage-current characteristic. JESD77D, 8/12

Graphic symbols (ref. IEEE Std 315):



VCC: See “logic power voltage”.

VCCQ: See “output stage logic power voltage”.

VDD: See “drain power voltage”.

VDDQ: See “output stage drain power voltage”.

VEE: See “emitter power voltage”.

verification: The process of confirming that the specified requirements are fulfilled, excluding reliability requirements. JEP148A, 12/08

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

verify: To interrogate the internal configuration contents of a programmable logic device (PLD) to confirm that it has been correctly programmed by comparing the data in the device to that in an external file containing the desired configuration. Similar to reading except that the contents of the PLD are not transferred to the programming system. JESD32, 6/96

vertical field-effect transistor (VFET): A field-effect transistor in which the current between the drain and source electrodes is primarily normal to the top surface of the die. JESD24, 7/85 JESD77D, 8/12#

NOTE If the device has an MOS structure, the usual abbreviation is "VMOS".

vertical surface-mount package: A surface-mount package that is intended to be mounted perpendicular to the seating plane. JESD30E, 8/08

NOTE….The package may include supporting posts (for insertion through the seating surface) or pedestals (for attachment to the seating surface).

VFET: See "vertical field-effect transistor".

VHH: See "special function enable voltage".

VHSIC: See "integrated circuit, very-high-speed".

via: An electrically conducting path that passes through an insulating material and connects conducting layers in two or more planes. JESD99C, 12/12

via-first: A through-silicon via formed before completion of the silicon device fabrication. JEP158, 11/09

NOTE A via-first may be created before or during front-end-of-line (FEOL) but before back-end-of-line (BEOL) processing. The via is created by etching it from the top side of the wafer and is buried below the subsequent BEOL layers. The process allows for interconnects with a high density. A via-first connects circuits at the global or intermediate IC level.

via-last: A through-silicon via formed after the completion of the silicon device fabrication, specifically after the completion of both front-end-of-line and back-end-of-line layer processes. JEP158, 11/09

NOTE The through-silicon vias connect circuits at the bond-pad level.

via-middle: A through-silicon via formed after FEOL processing and prior to or during the BEOL process. JEP158, 11/09

NOTE A via-middle process is sometimes considered to be part of a via-first process.

video RAM (VRAM): See "multiport DRAM".

virtual junction: The theoretical point or region in a simplified model of the thermal and electrical behavior of a semiconductor device at or in which all the power dissipation within the device is assumed to occur. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

virtual-junction temperature; internal equivalent temperature (T_J; T_{VJ}): (1) A temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behavior of the semiconductor device. JESD77D, 8/12 JESD282-B, 4/00

NOTE The term "virtual-junction temperature" is taken from IEC standards. It is particularly applicable to multijunction semiconductors and is used to denote the temperature of the active semiconductor element when required in specifications and test methods. The term "virtual-junction temperature" is used interchangeably with the term "junction temperature".

(2) The temperature of the virtual junction. JESD99C, 12/12

virtual memory: The control and organization of main storage to create a memory-mapping scheme that augments main storage by transferring in a block of data from mass storage whenever a portion of that block is addressed. JESD100-B, 12/99

NOTE 1 These transfers do not require implementation by the programmer.

NOTE 2 The use of virtual memory causes mass storage to appear as part of main storage.

visible-light-emitting diode (VLED): Deprecated synonym for "light-emitting diode". JESD77D, 8/12

visual index (on a package): A reference mark, chamfer, notch, tab, flat, or similar feature that identifies the number-one terminal position. RS-308-A, 8/81 Rescinded 5/09

VLED: See "visible-light-emitting diode (deprecated)".

VLSI: Very-large-scale integration. JESD99C, 12/12

VMOS: See "vertical field-effect transistor".

void: A hollow or indentation in a surface, typically an absence of intended material such as plating or metallization. JESD9B, 5/11

volatile memory: A memory in which the data content is lost when power is no longer supplied to it. (Ref. IEC 748-2.) JESD100-B, 12/99

voltage, dc or average [base-collector (V_{BC}), base-emitter (V_{BE}), collector-base(V_{CB}), collector-emitter (V_{CE}), emitter-base(V_{EB}), emitter-collector (V_{EC})] (V_{CB}), collector-emitter (V_{CE}), emitter-base(V_{EB}), emitter-collector (V_{EC})]: The dc voltage between the terminal indicated by the first subscript and the reference terminal (stated in terms of the polarity at the terminal indicated by the first subscript). JESD10, 1/76

voltage amplification, common-mode (A_{VC}): The ratio of the change in voltage at the output terminal with respect to ground (or change in voltage between the output terminals) to the change in common-mode input voltage with the differential input voltage held constant. JESD99C, 12/12

voltage amplification, differential (A_{VD}): The ratio of the change in voltage at the output terminal with respect to ground (or change in voltage between the output terminals) to the change in differential input voltage with the common-mode input voltage held constant. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

voltage amplification, single-ended (A_{VS}): The ratio of the change in single-ended output voltage of a differential amplifier to the change in single-ended input voltage. JESD99C, 12/12

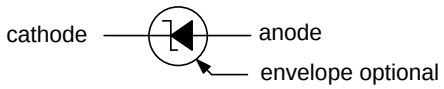
voltage delay time (of a transistor) (t_{dv}): The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the collector voltage waveform falls to 90% of its on-state amplitude, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance. JESD77D, 8/12

voltage fall time (of a transistor) (t_{fv}): The time interval during which the collector (or drain) voltage changes from 90% to 10% of its peak off-state value, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance. JESD24, 7/85
JESD77D, 8/12

voltage gain: Commonly used as a synonym for "voltage amplification". JESD99C, 12/12

voltage-reference diode: A diode that is normally biased to operate in the breakdown region of its voltage-current characteristic and that develops across its terminals a reference voltage of specified accuracy when biased to operate throughout a specified current and temperature range. (Ref. IEC 747-1.) JESD77D, 8/12

Graphic symbol (ref. IEEE Std 315):



voltage regulator: A circuit or portion of a circuit that provides isolation between the load and the supply to be regulated so that the load voltage remains relatively independent of load current or input voltage fluctuations. JESD99C, 12/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

voltage-regulator diode: A semiconductor diode with a single p-n junction (or with multiple p-n junctions, none of which interact) that is normally biased in the breakdown region of its voltage-current characteristic and limits variation in voltage across its terminals over a specified current range. (Ref. JESD211.)

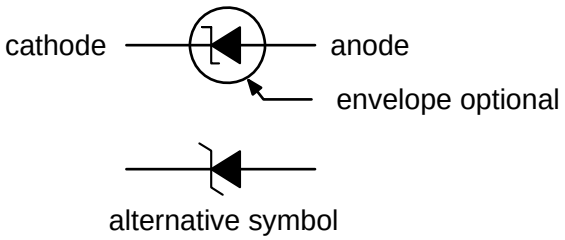
JESD77D, 8/12
JESD211, 12/09

NOTE 1 The breakdown region may be due to either avalanche breakdown or Zener breakdown phenomenon (also often known as tunneling or field-emission breakdown).

NOTE 2 When forward-biased, a voltage-regulator diode has a voltage-current characteristic similar to that of a rectifier diode.

NOTE 3 In general usage, voltage-regulator diodes are often referred to as "Zener diodes", even if their breakdown characteristics are due to avalanche breakdown. A voltage-regulator diode may also be referred to as a "voltage-reference diode**"** when its application is to maintain a reference voltage within a specified accuracy over a specified current and temperature range in the breakdown region of the diode's voltage-current characteristic.

Graphic symbol (Ref. IEEE Std 315):



voltage rise time (of a transistor) (t_{rv}): The time interval during which the collector (or drain) voltage changes from 10% to 90% of its peak on-state value, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance.

JESD24, 7/85
JESD77D, 8/12

voltage turn-off delay time ($t_{d(off)v}$): The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain voltage waveform rises to 10% of its off-state amplitude, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance.

JESD24, 7/85
JESD77D, 8/12

voltage turn-off time ($t_{off(v)}$): The sum of voltage turn-off delay time and voltage rise time, i.e., $t_{off(v)} = t_{d(off)v} + t_{rv}$.

JESD24, 7/85
JESD77D, 8/12

voltage turn-on delay time ($t_{d(on)v}$): The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain voltage waveform falls to 90% of its off-state amplitude, ignoring spikes caused by interaction with other components or parasitics, e.g., freewheeling-diode recovery current and parasitic inductance.

JESD24, 7/85
JESD77D, 8/12

voltage turn-on time ($t_{on(v)}$): The sum of voltage turn-on delay time and voltage fall time, i.e., $t_{d(on)v} = t_{d(on)v} + t_{fv}$.

JESD24, 7/85
JESD77D, 8/12

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

voltage-variable-capacitance diode (VVC or **VVCD):** Synonym for "varactor diode". JESD77D, 8/12

volume resistivity (ρ_v): The dc voltage per unit thickness, applied across two electrodes in contact with a specimen, divided by the current per unit area passing through the system. JESD625B, 1/12

NOTE Volume resistivity is expressed in ohm-centimeters.

VPP: See "programming power voltage".

V_R: See "reverse voltage".

VRAM: See "multiport DRAM".

VREF: See "reference power supply".

VSS: See "ground reference or source power voltage (pin)".

VSSQ: See "output stage source power voltage or output stage ground reference (pin)".

V_{supply} overvoltage test: A latch-up test that supplies overvoltage pulses to the V_{supply} pin under test. JESD78D, 11/11

V_{supply} pin (or pin group): All device under test power supply and external voltage source pins (excluding ground pins), including both positive- and negative-potential pins. JESD78D, 11/11

NOTE 1 Generally, it is permissible to treat equal potential voltage source pins as one V_{supply} pin (or pin group) and connect them to one power supply.

NOTE 2 When forming V_{supply} pins (or pin groups), combining V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low-supply-current pins.

VTC: The temperature coefficient of gate-emitter on-state voltage with respect to junction temperature. JESD24-6, 10/91

VVC: See "voltage-variable-capacitance diode".

VVCD: See "voltage-variable-capacitance diode".

V_Z: See "regulator [Zener] voltage".

V_{ZM}: See "maximum regulator [Zener] voltage".

W

W: See "write enable".

WAF: See "write amplification factor".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

wafer: A slice or flat disk, either of semiconductor material or of such a material deposited on a substrate, in which circuits or devices are simultaneously processed and subsequently separated into chips if there is more than one device. JESD99C, 12/12

wafer backside: The side of the wafer that does not contain fabricated semiconductor circuits or circuit elements. JESD22-B118, 3/11

wafer backside grind: A process of abrading the wafer backside. JESD22-B118, 3/11

NOTE Abrading is usually done with a fine grit to eliminate surface scratches or to create a thinned wafer.

wafer backside metallization: A metal film layer on the wafer backside surface. JESD22-B118, 3/11

wafer-level package: A chip-scale package package whose size is generally equal to the size of the semiconductor device it contains and that is formed by processing on a complete wafer rather than on an individual device. JESD30E, 8/08

NOTE 1 Because of the wafer-level processing, the size of a wafer-level package may be defined by finer dimensions and tighter tolerances than those for a similar non-wafer-level package.

NOTE 2 The package size will change with changes in the size of the die.

wafer lot: A quantity of wafers that are processed together as a batch under a given set of conditions. JESD22-B118, 3/11

wait signal: A signal indicating that the device addressed by the central processing unit has not yet completed its data transfer. (Ref. IEC 824.) JESD100-B, 12/99

water vapor transmission rate (WVTR): A measure of the permeability of plastic film or metallized plastic film material to moisture. J-STD-033C, 2/12

WE: See “write enable”.

wear leveling: Methods employed by the solid-state drive to spread the program-erase cycles across the nonvolatile memory physical locations even when the workload may be unevenly distributed across the logical drive capacity. JESD218A, 2/11

wearout: The phase in the life of a device during which the mortality function is increasing. JEP122G, 10/11
JEP143C, 7/12

NOTE….As typically used with the bathtub curve, the wearout phase follows the useful life of the device.

wedge bond; stitch bond: The adhesion or weld of a thin wire, usually aluminum, to a package bonding surface, usually a plated leadframe post or finger, using an ultrasonic wire bonding process. JESD22-B116A, 8/09

NOTE The wedge bond includes the compressed (ultrasonically bonded) area of the wire and the underlying bonding surface. For bonding to an aluminum alloy die bond pad, there is no wedge bond-bond pad intermetallic because the two materials are of the same composition, but the two materials are recrystallized together by the ultrasonic energy of the welding process.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

weld projection: A delta-shaped (Δ) projection that welds to the package/cover to create a hermetic seal. JESD9B, 5/11

wetting, solder: The formation of a relatively uniform, smooth, unbroken, and adherent film of solder to a basis metal. (Ref. IPC-T-50.) J-STD-002B, 2/03

Wheatstone bridge: A 4-arm bridge forming a diamond, all of whose arms are predominantly resistive, with three resistors of known values in three of the arms and the unknown resistor in the fourth. JEP154, 1/08

NOTE 1 A voltage source, e.g., a battery, is connected across two opposite points of the diamond and a current-detecting instrument (e.g., a galvanometer) is connected across the other two points. The values of one or two of the known resistors are varied until no current flows through the galvanometer. The bridge is then balanced and the value of the unknown resistor can be calculated in terms of the other three.

NOTE 2 A method using the Wheatstone bridge for monitoring resistance of solder bumps in electromigration tests has greater sensitivity to resistance change than other methods. Net resistance changes due to electromigration of only the solder bumps, excluding the Al or Cu traces, can be deduced by this method.

whisker: A spontaneous columnar or cylindrical filament, usually of monocrystalline metal, emanating from the surface of a finish. JEP122G, 10/11
JESD22-A121A, 7/08
JESD201A, 8/08
JP002, 3/06

NOTE 1 Whiskers have the following characteristics:
• they have aspect ratios (length/width) greater than 2;
• they can be kinked, bent, or twisted;
• they usually have a uniform cross-sectional shape;
• they typically consist of a single columnar filament that rarely branches;
• they may have striations along the length of the column and/or rings around the circumference of the column;
• they have lengths of 10 micrometers or greater; features shorter than 10 micrometers may be deemed important for research but are not considered significant in JESD22-A121A.

NOTE 2 Whiskers are not to be confused with dendrites: fern-like growths on the surface of a material, which can be formed as a result of electromigration of an ionic species or produced during solidification.

whisker density: The number of whiskers per unit area on a single lead or coupon area. JESD22-A121A, 7/08

whisker growth: Measurable changes in whisker length and/or whisker density after exposure to a whisker test condition for a certain duration or number of cycles. JESD22-A121A, 7/08
JP002, 3/06

whisker length: The straight line distance from the point of emergence of the whisker to the most distant point on the whisker (i.e., the radius of the smallest sphere containing the whisker with the sphere's center located at the point of emergence). JESD22-A121A, 7/08
JESD201A, 8/08

whisker test coupon: A piece of metal of specified size and shape that is plated or dipped with a tin finish for the purpose of measuring the propensity for whisker formation and growth. JESD22-A121A, 7/08

width (of a data path): The number of data lines used in parallel transmission. JESD100-B, 12/99

NOTE For digital data, width is usually expressed in bits, bytes, or words.

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions	References
window: A hole formed by etching through an oxide or insulating layer on a semiconductor for the purpose of diffusion into or deposition onto a selected area of the semiconductor.	JESD99C, 12/12
WIP: "Work in progress" or "work in process".	JESD22-B101B, 8/09
wire-bond surface: The area where wire(s) may be bonded.	J-STD-020D.1, 3/08
wire-bond trace: Synonym for "bonding trace".	
wire length: The total amount of interconnect of a net (specified in units of either length or capacitance).	JESD12-1B, 8/93 JESD99C, 12/12
word: A character string or a binary element string that it is convenient to consider as an entity. (Adapted from ANSI X3.172.)	JESD100-B, 12/99
NOTE For memories, it is common practice to use the term "word" generically for any number of bits that occupy a single address location.	
word-wide device: A device that has a parallel data interface of 16 bits or more (usually in multiples of 16 bits), possibly with additional bits appended to provide parity or error-detection capability.	JESD21-C, 1/97# JESD100-B, 12/99
working area: The portion of a chamber, used for stress testing, that meets the calibration requirements.	JEP153,1/08
working peak reverse voltage (V_{RWM}): The peak reverse voltage excluding all transient voltages.	JESD77D, 8/12 JESD282-B, 4/00
workload: The detailed sequence of host writes and reads (including data content and timing) applied to the solid-state drive during endurance testing.	JESD218A, 2/11
WP: See "write protect".	
write: To make a permanent or transient recording of data in a storage device or on a data medium. (Ref. ANSI X3.172.)	JESD100-B, 12/99
write amplification factor (WAF): The data written to the nonvolatile memory divided by data written by the host to the solid-state drive.	JESD218A, 2/11
NOTE Write amplification factor will depend on the workload and may vary over the lifetime of the device.	
write disturb: The corruption of data in one location caused by the writing of data at another location.	JESD100-B, 12/99
write enable (WE; W): The input that, when true, causes the data present on the D or the DQ pin(s) to be written into the address cell(s) of the device. For devices that have one WE per byte, the WEs are designated LWE and UWE. For devices that have more than two bytes and one WE per byte, and for all modules that have multiple WEs, the WEs are numbered beginning with 0.	JESD21-C, 1/97

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

write protect (WP): The output signal used to reflect the status of the write-protect switch on the memory card. If the memory card write-protect switch is present, this signal will be asserted by the card when the switch is enabled, and deasserted when the switch is disabled. If the memory card has no write-protect switch, the card will connect this line to ground or V_{CC}, depending on the condition of the card memory. If the card can always be written, the pin will be connected to V_{SS}. If the card is permanently write-protected, the pin will be connected to V_{CC}. JESD21-C, 1/97

write transfer (WT): An operation in which the data to be written is introduced through the serial port and is then transferred internally to the memory array data bus for writing into the cells. At the same time, the "tap pointer" is set. This is a counter that defines the starting point in the serial register into which data is entered. Data is entered serially from this point, with wraparound when the end of the register is reached. The contents of the full serial register are transferred in parallel. In addition to the normal write transfer, numerous other types of special write transfers are defined in JESD 21-C. JESD21-C, 1/97

WT: See "write transfer".

WVTR: See "water vapor transmission rate".

X

x: See "byte [word] identifier".

Y

yield: The ratio of the number of units that pass some inspection criteria to the number submitted. EIA-557-B, 2/06

yield analysis: For existing and modified processes, the determination of product yields and comparison to prior process performance. JEP132, 7/98

Z

Zener diode: A semiconductor diode with a single p-n junction whose breakdown characteristics are due to the Zener effect. (Ref. JESD211.) JESD77D, 8/12

NOTE Although true Zener breakdown occurs below approximately 6 volts, the term "Zener diode" is often used interchangeably with "voltage-regulator diode" and "voltage-reference diode" even for voltages over 6 volts, where the breakdown characteristic is due to avalanche breakdown.

zero-gate-voltage drain current (I_{DSS}): The direct current into the drain terminal when the gate-source voltage is zero. JESD24, 7/85

NOTE This is an on-state current in a depletion-type device, an off-state in an enhancement-type device.

zero-gate-voltage source current (I_{SDS}): The direct current into the source terminal when the gate-drain voltage is zero. JESD24, 7/85

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Terms, abbreviations, letter symbols, and definitions **References**

zero scale (of an analog-to-digital converter [a digital-to-analog converter] with true zero): JESD99C, 12/12
A term used to refer a characteristic to the step whose nominal midstep [step] value equals zero.

NOTE 1 The subscript for the letter symbol of a characteristic at zero scale is "ZS".

NOTE 2 In place of a letter symbol, the abbreviation "ZS" is commonly used.

zero-scale error (of a linear analog-to-digital converter [digital-to-analog converter]) (E_{ZS}): JESD99C, 12/12
The difference between the actual midstep [step] value and the nominal midstep [step] value at specified zero scale.

NOTE Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

zero scale, negative (of an analog-to-digital converter or **digital-to-analog converter with no true zero):** JESD99C, 12/12
A term used to refer a characteristic to the negative step closest to analog zero.

NOTE 1 The subscript for the letter symbol of a characteristic at negative zero scale is "ZS–", e.g., $V_{ZS–}$, $I_{ZS–}$.

NOTE 2 In place of a letter symbol, the abbreviation "ZS–" is commonly used.

zero scale, positive (of an analog-to-digital converter or **digital-to-analog converter with no true zero):** JESD99C, 12/12
A term used to refer a characteristic to the positive step closest to analog zero.

NOTE 1 The subscript for the letter symbol of a characteristic at positive zero scale is "ZS+", e.g., V_{ZS+}, I_{ZS+}.

NOTE 2 In place of a letter symbol, the abbreviation "ZS+" is commonly used.

0-state: The logic state represented by the binary number 0 and usually standing for an inactive or false logic condition. (Ref. ANSI/IEEE Std 91.) JESD99C, 12/12

ZIP/SIMM, ZIP/SIMM module: A multichip memory module in which the body has a single-in-line package (SIP) form but the leads have been formed into a zigzag configuration. JESD21-C, 1/97

ZZ: See "sleep-mode enable".

z_{zk}: See "regulator [Zener] knee impedance".

z_{zt}: See "regulator [Zener] impedance".

Greek

µC: See "microcomputer".

µP: See "microprocessor (integrated circuit)".

The definition in this referenced publication has been reworded in this dictionary for clarity or consistency.

Annex A (informative) List of referenced documents

Document	Title	Date
	EIA Standards (EIA and RS*)	
RS-308-A*	Preparation of Outline Drawings of Solid State Products for JEDEC Type Registration	8/81, Rescinded 5/09
RS-311-A*	Measurement of Transistor NFoise Figure and Effective Input Noise Temperature at MF, HF, and VHF	11/81, Redesignated JESD311A 3/09
RS-323*	Air-Convection-Cooled Life Test Environment for Lead-Mounted Semiconductor Devices	3/66, Reaffirmed 2/72
RS-353*	The Measurement of Transistor Noise Figure at Frequencies Up to 20 kHz By Sinusoidal Signal-Generator Method	4/68, Redesignated JESD353 3/09
RS-371*	The Measurement of Small-Signal VHF-UHF Transistor Short-Circuit Forward Current Transfer Ratio	2/70, Redesignated JESD371 3/09
RS-372*	The Measurement of Small-Signal VHF-UHF Transistor Admittance Parameters	5/70, Redesignated JESD372 3/09
RS-435*	Standard for the Measurement of Small-Signal Transistor Scattering Parameters	4/76, Redesignated JESD435 3/09
EIA-557-B	Statistical Process Control Systems	2/06, Reaffirmed 10/11

* Older EIA standards were identified by the prefix “RS”. While they may still carry that designation on their covers, they are sometimes redesignated (e.g., on the JEDEC Web site) with the prefix “EIA” instead of the prefix “RS”. When reissued, they have been or may be redesignated with the prefix “JESD”.

Annex A (informative) List of referenced documents (cont'd)

Document	Title	Date
	JEDEC Publications (JEP)	
JEP96	Guidelines for Nondestructive Pull Testing of Wire Bonds on Hybrid Devices	3/77, Reaffirmed 3/82, Rescinded 4/00
JEP119A	A Procedure for Executing SWEAT	8/03
JEP121A	Requirements for Microelectronic Screening and Test Optimization	10/06
JEP122G†	Failure Mechanisms and Models for Semiconductor Devices	10/11
JEP123	Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters	10/95
JEP131B†	Potential Failure Mode and Effects Analysis (FMEA)	4/12
JEP132	Process Characterization Guideline	7/98
JEP133C†	Guide for the Production and Acquisition of Radiation-Hardness-Assured Multichip Modules and Hybrid Microcircuits	1/10
JEP134	Guidelines for Preparing Customer-Supplied Background Information Relating to a Semiconductor-Device Failure Analysis	9/98
JEP136	Signature Analysis	7/99
JEP138	User Guidelines for IR Thermal Imaging Determination of Die Temperature	9/99
JEP140	Beaded Thermocouple Temperature Measurement of Semiconductor Packages	6/02
JEP143C†	Solid-State Reliability Assessment and Qualification Methodologies	7/12
JEP146A	Guidelines for Supplier Performance Rating	1/09
JEP148A	Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment	12/08
JEP149	Application Thermal Derating Methodologies	11/04
JEP150	Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid-State Surface-Mount Components	5/05
JEP153	Characterization and Monitoring of Thermal Stress Test Oven Temperatures	1/08
JEP154	Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress	1/08
JEP155A.01†	Recommended ESD Target Levels for HBM/MM Qualification	3/12
JEP156	Chip-Package Interaction Understanding, Identification and Evaluation	3/09
JEP157†	Recommended ESD-CDM Target Levels	10/09
JEP158†	3-D Chip Stack with Through-Silicon Vias (TSVS): Identifying, Evaluating, and Understanding Reliability Interactions	11/09
JEP160†	Long-Term Storage for Electronic Solid-State Wafers, Dice, and Devices	11/11

† This publication was not referenced in previous editions of JESD88 or is a revised edition of a publication that was referenced.

Annex A (informative) List of referenced documents (cont'd)

Document	Title	Date
	JEDEC Standards (JESD)	
JESD4	Definition of External Clearance and Creepage Distances of Discrete Semiconductor Packages for Thyristors and Rectifier Diodes	11/83, Reaffirmed 1/91
JESD7-A	Standard for Description of 54/74HC and 54/74HCT High-Speed CMOS Devices	8/86
JESD9B†	Inspection Criteria for Microelectronic Packages and Covers	5/11
JESD10	Low-Frequency Power Transistors	1/76, Reaffirmed 10/02
JESD12-1B	Terms and Definitions for Gate Arrays and Cell-Based Digital ICs	8/93
JESD12-4	Method of Specification of Performance Parameters for CMOS Semicustom ICs	4/87
JESD13-B	Standard Specification for Description of 'B' Series CMOS Devices	5/80
JESD14	Semiconductor Power Control Modules	11/86, Reaffirmed 6/92
JESD16-A	Assessment of Average Outgoing Quality Levels in Parts per Million (PPM)	4/95, Reaffirmed 9/08
JESD18-A	Standard for Description of Fast CMOS TTL-Compatible Logic	1/93
JESD21-C	Configurations for Solid-State Memories	9/91
JESD22-A105C	Power and Temperature Cycling	1/04, Reaffirmed 1/11
JESD22-A108D†	Temperature, Bias, and Operating Life	11/10
JESD22-A109-A	Hermeticity	7/01
JESD22-A117B	Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test	3/09
JESD22-A121A	Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes	7/08
JESD22-B101B†	External Visual	8/09
JESD22-B103B	Vibration, Variable Frequency	6/02, Reaffirmed 9/10
JESD22-B104C	Mechanical Shock	11/04, Reaffirmed 6/09
JESD22-B108B†	Coplanarity Test for Surface-Mount Semiconductor Devices	9/10
JESD22-B109A	Flip Chip Tensile Pull	1/09
JESD22-B110A	Subassembly Mechanical Shock	11/05
JESD22-B111	Board Level Drop Test Method of Components for Handheld Electronic Products	7/03
JESD22-B112A†	Package Warpage Measurement of Surface-Mount Integrated Circuits at Elevated Temperature	10/09
JESD22-B113A†	Board-Level Cyclic Bend Test Method for Interconnect Reliability Characterization of SMT ICs for Handheld Electronic Products	9/12
JESD22-B114A†	Mark Legibility	5/11
JESD22-B116A	Wire Bond Shear Test Method	8/09

† This publication was not referenced in previous editions of JESD88 or is a revised edition of a publication that was referenced.

Annex A (informative) List of referenced documents (cont'd)

Document	Title	Date
JESD22-B117A	Solder Ball Shear	10/06
JESD22-B118†	Semiconductor Wafer and Die Backside External Visual Inspection	3/11
JESD22-C101E†	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components	12/09
JESD24	Power MOSFETs	7/85
JESD24-1	Method for Measurement of Power Device Turn-Off Switching Loss	9/89
JESD24-2	Gate Charge Test Method	1/91
JESD24-3	Thermal Impedance Measurements for Vertical Power MOSFETs (Delta Source-Drain Voltage Method)	11/90
JESD24-4	Thermal Impedance Measurements for Biploar Transistors (Delta Base-Emitter Voltage Method)	11/90
JESD24-5	Single-Pulse Unclamped Inductive Switching (UIS) Avalanche Test Method	8/90
JESD24-6	Thermal Impedance Measurements for Insulated-Gate Bipolar Transistors	10/91
JESD24-8	Method for Repetitive Inductive-Load Avalanche Switching	8/92
JESD24-9	Short-Circuit Withstand Time Test Method	8/92
JESD24-11	Power MOSFET Equivalent Series Gate Resistance Test Method	8/96
JESD26-A	General Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications	4/90
JESD27	Ceramic Package Specification for Microelectronic Packages	8/93
JESD28-A	Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation at Maximum Substrate Current Under DC Stress	12/01
JESD28-1	N-channel MOSFET Hot Carrier Data Analysis	9/01
JESD30E	Descriptive Designation System for Semiconductor-Device Packages	8/08
JESD31D†	General Requirements for Distributors of Commercial and Military Semiconductor Devices	9/10
JESD31C	General Requirements for Distributors of Commercial and Military Semiconductor Devices	9/03
JESD32	Standard for Chain Description File	6/96
JESD33B	Standard Method for Measuring and Using The Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line	2/04
JESD35-A	Procedure for the Wafer-Level Testing of Thin Dielectrics	4/01
JESD37	Standard for Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method	10/92
JESD41	Reverse Recovery Characteristics of Silicon Diodes	5/95
JESD45	Measurement Method for Thermal Resistance of Bridge Rectifier Assemblies	12/94
JESD46D†	Customer Notification of Product/Process Changes by Solid-State Suppliers	12/11

† This publication was not referenced in previous editions of JESD88 or is a revised edition of a publication that was referenced.

Annex A (informative) List of referenced documents (cont'd)

Document	Title	Date
JESD47I†	Stress-Test-Driven Qualification of Integrated Circuits	7/12
JESD50B.01	Special Requirements for Maverick Product Elimination and Outlier Management	11/08
JESD51-1	Integrated Circuits Thermal Measurement Method — Electrical Test Method (Single Semiconductor Device)	12/95
JESD51-8	Integrated Circuit Thermal Test Method Environmental Conditions — Junction-to-Board	10/99
JESD51-13†	Glossary of Thermal Measurement Terms and Definitions	6/09
JESD51-31	Thermal Test Environment Modifications for Multichip Packages	7/08
JESD51-51†	Implementation of the Electrical Test Method for the Measurement of Real Thermal Resistance and Impedance of Light-Emitting Diodes with Exposed Cooling	4/12
JESD54	Standard for Description of 54/74ABTXXX and 74BCXXX TTL-Compatibility BiCMOS Logic Devices	2/96
JESD55	Standard for Description of Low-Voltage TTL-Compatible BiCMOS Logic Devices	5/96
JESD57	Test Procedures for the Measurements of Single-Event Effects in Semiconductor Devices From Heavy Ion Irradiation	12/96
JESD60A	A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress	9/04
JESD61A.01	Isothermal Electromigration Test Procedure	10/07
JESD64-A	Standard for Description of 2.5-V CMOS Logic Devices with 3.6-V CMOS-Tolerant Inputs and Outputs	10/00
JESD65B	Definition of Skew Specification for Standard Logic Devices	9/03
JESD66	Transient Voltage Suppressor Standard for Thyristor Surge Protective Device Rating Verification and Characteristic Testing	11/99
JESD73	Standard for Description of 5 V Bus Switch Devices with TTL-Compatible Control Inputs	6/99
JESD73-1	Standard for Description of 3.3 V NFET Bus Switch Devices	8/01
JESD73-2	Standard for Description of 3.3 V NFET Bus Switch Devices with Integrated Charge Pumps	8/01
JESD73-3	Standard for Description of 3877: 2.5 V, Single 10-Bit, 2-Port, DDR FET Switch	11/01
JESD73-4	Standard for Description of 3867: 2.5 V, Dual 5-Bit, 2-Port, DDR FET Switch	11/01
JESD74A	Early Life Failure Rate Calculation Procedure for Electronic Components	2/07
JESD77D†	Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices	8/12
JESD78D†	IC Latch-Up Test	11/11
JESD82-2	Description of a 3.3 V, 18-Bit, LVTTL I/O Register for PC133 Registered DIMM Applications	7/01
JESD85	Methods for Calculating Failure Rates in Units of FITs	7/01

† This publication was not referenced in previous editions of JESD88 or is a revised edition of a publication that was referenced.

Annex A (informative) List of referenced documents (cont'd)

Document	Title	Date
JESD86A†	Electrical Parameters Assessment	10/09
JESD89A	Measurement and Reporting of Alpha Particles and Terrestrial Cosmic-Ray-Induced Soft Errors in Semiconductor Devices	10/06
JESD89-1A	System Soft Error Rate (SSER) Test Method	10/07
JESD89-2A	Test Method for Alpha Source Accelerated Soft Error Rate	10/07
JESD89-3A	Test Method for Beam-Accelerated Soft Error Rate	11/07
JESD90	A Procedure for Measuring P-Channel MOSFET Negative-Bias Temperature Instabilities	11/04
JESD91A	Method for Developing Acceleration Models for Electronic Component Failure Mechanisms	8/03
JESD93	Hybrids/MCM	9/05, Reaffirmed 1/09
JESD94A	Application Specific Qualification Using Knowledge Based Test Methodology	7/08
JESD95-1	Design Requirements for Outlines of Solid-State and Related Products	1/97
JESD96	Radio Front End-Baseband (RF-BB) Interface	4/04
JESD99C†	Terms, Definitions, and Letter Symbols for Microelectronic Devices	12/12
JESD100-B	Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits	12/99
JESD100B.01	(Minor revision of JESD100-B)	12/02
JESD201A	Environmental Acceptance Requirements for Tin-Whisker Susceptibility of Tin and Tin-Alloy Surface Finished	8/08
JESD206	FBDIMM: Architecture and Protocol	1/07
JESD210	Avalanche Breakdown Diode (ABD) Transient Voltage Suppressors	12/07
JESD211†	Zener and Voltage Regulator Diode Rating Verification and Characterization Testing	12/09
JESD217†	Test Methods to Characterize Voiding in Pre-SMT Ball Grid Array Packages	9/10
JESD218A†	Solid-State Drive (SSD) Requirements and Endurance Test Method	2/11
JESD229	Wide I/O Single Data Rate (Wide I/O SDR)	12/11
JESD282-B	Silicon Rectifier Diodes	4/00
JESD282B.01	(Minor revision of JESD282-B)	11/02
JESD311A†	Measurement of Transistor Noise Figure at MF, HF, and VHF	11/86
JESD353	The Measurement of Transistor Noise Figure at Frequencies Up to 20 kHz By Sinusoidal Signal-Generator Method	RS-353, 4/68, Redesignated 3/09
JESD371	The Measurement of Small-Signal VHF-UHF Transistor Short-Circuit Forward Current Transfer Ratio	EIA-371, 2/70, Redesignated 3/09
JESD372	The Measurement of Small-Signal VHF-UHF Transistor Admittance Parameters	EIA-372, 5/70, Redesignated 3/09

† This publication was not referenced in previous editions of JESD88 or is a revised edition of a publication that was referenced.

Annex A (informative) List of referenced documents (cont'd)

Document	Title	Date
JESD435	Standard for the Measurement of Small-Signal Transistor Scattering Parameters ..... RS-435, 5/76, Redesignated	3/09
JESD625B†	Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices	1/12
JESD659B	Failure-Mechanism-Driven Reliability Monitoring	2/07
JESD671B†	Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems)	6/12
	Joint Industry Guide, EIA/EICTA/JEDEC/JGPSSI (JIG)	
JIG-101 Ed 2.0	Material Composition Declaration for Electrotechnical Products	4/09
	Joint JEDEC/IPC Standards and Publications (IPC/JEDEC, JP, and J-STD	
IPC/JEDEC -9702	Monotonic Bend Characterization of Board-Level Interconnects	6/04
JP002†	Current Tin Whiskers Theory and Mitigation Practices Guideline	3/06
J-STD-002B	Solderability Tests for Component Leads, Terminations, Lugs, Terminals, and Wires	2/03
J-STD-020D.1†	Moisture/Reflow Sensitivity Classification for Nonhermetic Solid-State Surface-Mount Devices	3/08
J-STD-033C†	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices	2/12
J-STD-035	Acoustic Microscopy for Nonhermetic Encapsulated Electronic Components ..... 5/99, Reaffirmed	9/10
J-STD-609A.01†	Marking and Labeling of Components, PCBs, and PCBAs to Identify Lead (Pb), Lead-Free (Pb-Free), and Other Attributes	2/11
	Joint JEDEC/ESDA Stadards (JS)	
JS-001-2012†	ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Component Level	4/12
	Joint JEDEC/ECA Stadards (JS)	
JS709A†	Defining "Low-Halogen" Passives and Solid-State Devices (Removal of BFR/CFR/PVC)	5/12
	Other publications	

The following references have been used when necessary to supply general definitions used in the solid-state industry for several terms that have been only narrowly defined in JEDEC publications:

IEEE Std 100	IEEE Standard Dictionary of Electrical and Electronics Terms
—	Merriam-Webster's Collegiate Dictionary

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