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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

HI7700/4 Renesas Industrial Realtime Operating System

Configuration Guide

Renesas Microcomputer Development Environment System

Renesas Electronics
www.renesas.com

Rev.1.0 2003.03

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Preface

This guide describes how to configure systems using HI7700/4.

To execute application programs registered as tasks on HI7700/4, the Solution Engine®, the product of Hitachi ULSI Systems Co., Ltd., shall be used as a target board and the HDI of the E10A emulator as a debugger in the initial debug stage. For details about HI7700/4, see the HI7000/4 Series (HI7000/4, HI7700/4, HI7750/4) User's Manual (hereinafter referred to as the HI7000/4 Series User's Manual). To create application programs and link them with HI7700/4, you should use the SuperH™ RISC engine C/C++ compiler package (hereinafter referred to as the SHC/C++ compiler) and the Hitachi Embedded Workshop (HEW), which is an integrated development tool, supplied with the SuperH™ RISC engine C/C++ compiler package.

This guide describes how to change, add and configure programs before executing the start task on multitasking operating system using the above target board, emulator, and compiler.

Related manuals

- HI7000/4 Series (HI7000/4, HI7700/4, HI7750/4) Hitachi Industrial Realtime Operating System User's Manual
- SuperH RISC engine C/C++ Compiler SH-1, SH-2, SH-2E, SH-3, SH3E, SH-4 User's Manual
- SuperH RISC engine C/C++ Compiler Assembler Optimizing Linkage Editor User's Manual
- H Series Linkage Editor, Librarian, and Object Converter User's Manual
- Hitachi Embedded Workshop 2 HEW Debugger User's Manual
- SH7729 Solution Engine™ (MS7729SE01) Overview
- The hardware manual and programming manual of the SuperH microcomputer used

Contents

Section 1 Introduction

1.1 Overview

Follow the procedure below to run application programs on HI7700/4:

1. Create application programs.
2. Use the configurator to register the application programs to HI7700/4.
3. Build the executable file using HEW.
4. Install the application programs to the target board, and download and execute them.

This guide describes the above procedure to run the programs on the target board by using a sample program.

1.2 System Configuration

This guide describes how to create sample programs of tasks and an interrupt handler and how to run the programs on the target board.

Figure 1.1 shows an example of a hardware configuration.

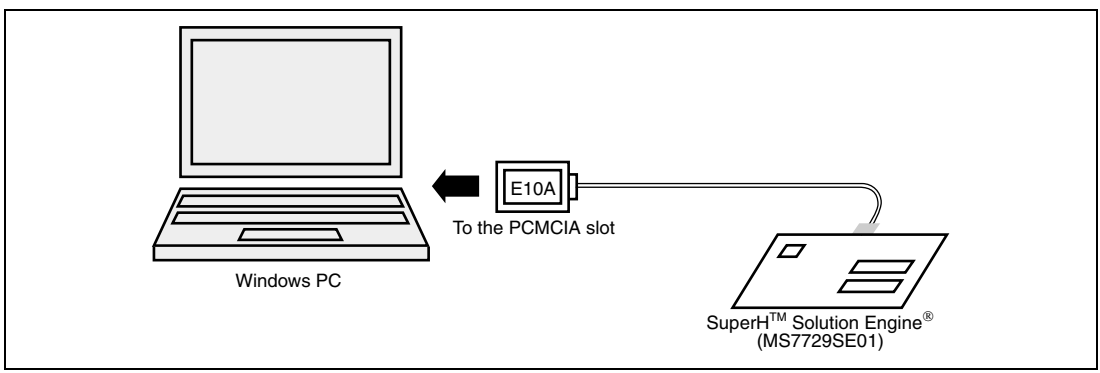


Figure 1.1 Hardware Configuration Example

Table 1.1 lists software configuration.

Table 1.1 Software Configuration

Program	Description	Type	Remarks
CPU initialization routine	Sets the bus controller. Initializes the hardware.	Non-task	
Main task	Initializes the environment. Waits for an event after initialization by setting the wai_flg flag. Cancels the wait status by setting the event flag of the timer interrupt handler and starts the LED task (sta_tsk).	Task	
LED task	Started by the main task to turn the LED on when it is off or turn it off when it is on, and then terminates.	Task	
Timer interrupt handler	Started by the timer interrupt every one second and sets the main task event flag (set_flg).	Non-task	

1.3 Prerequisites

Table 1.2 lists hardware and software required to run the application programs on HI7700/4.

Table 1.2 Required Hardware and Software

Product Name	Product Type	Manufacturer
Windows® personal computer	—	Any manufacturer*[1]
SuperH™ Solution Engine®	MS7729RSE01	Hitachi ULSI Systems Co., Ltd.
E10A emulator	HS7729RKCM01H	Hitachi, Ltd.
SuperH™ RISC engine C/C++ compiler	P0700CAS6-MWR	Hitachi, Ltd. *[2]
HI7700/4	HS0700ITI41SRE	Hitachi, Ltd. *[3]

Notes: 1. Hardware environment: PC/AT compatible machine with 486DX2/66 MHz or more (Pentium® or later recommended)
Operating system: Windows®2000, WindowNT®4.0, Windows®98, Windows®95
CD-ROM drive
PCMCIA card slot
Memory: 32 Mbytes or more (For Windows®2000 and WindowNT®4.0, memory with 64 Mbytes or more is recommended.)
Free space required on the hard disk: 8 Mbytes or more

2. Version. 6.0 AR2 of the compiler shall be used. You may also use the compilers from Hitachi ULSI Systems Co., Ltd. or Hitachi Software Engineering Co., Ltd.
HI7700/4 with evaluation license (object) shall be used. You may also use HI7700/4 with mass-production license.

The HDI of the E10A emulator, SuperH™ RISC engine C/C++ compiler package, and HI7700/4 (for SHCV6) must have been installed in the Windows personal computer beforehand. The SH7729 is a target CPU assumed in this manual.

Figure 1.2 shows the folder structure of HI7700/4 that you have just installed.

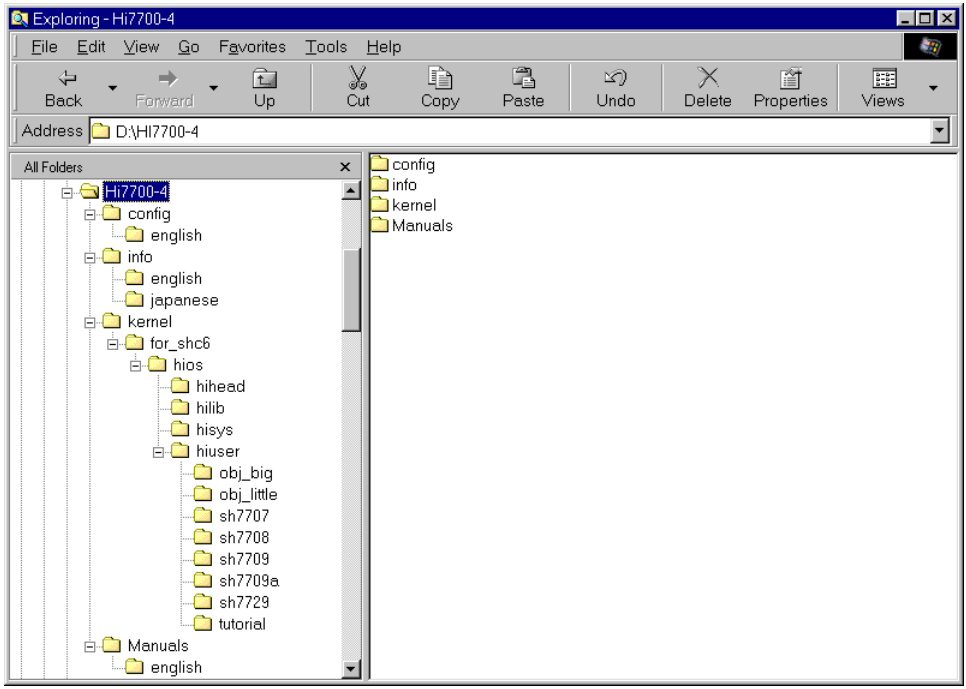


Figure 1.2 Folder Structure of HI7700/4

The install drive is “D” in this guide, but you may use a desired drive for installing HI7700/4. An install folder is represented as the install folder “folder name” in this manual.

Section 2 Creating Application Programs

This section describes how to create application programs that run on HI7700/4. Figure 2.1 shows the relationship among application programs. (The programs in the heavy-outline boxes are created in this guide.)

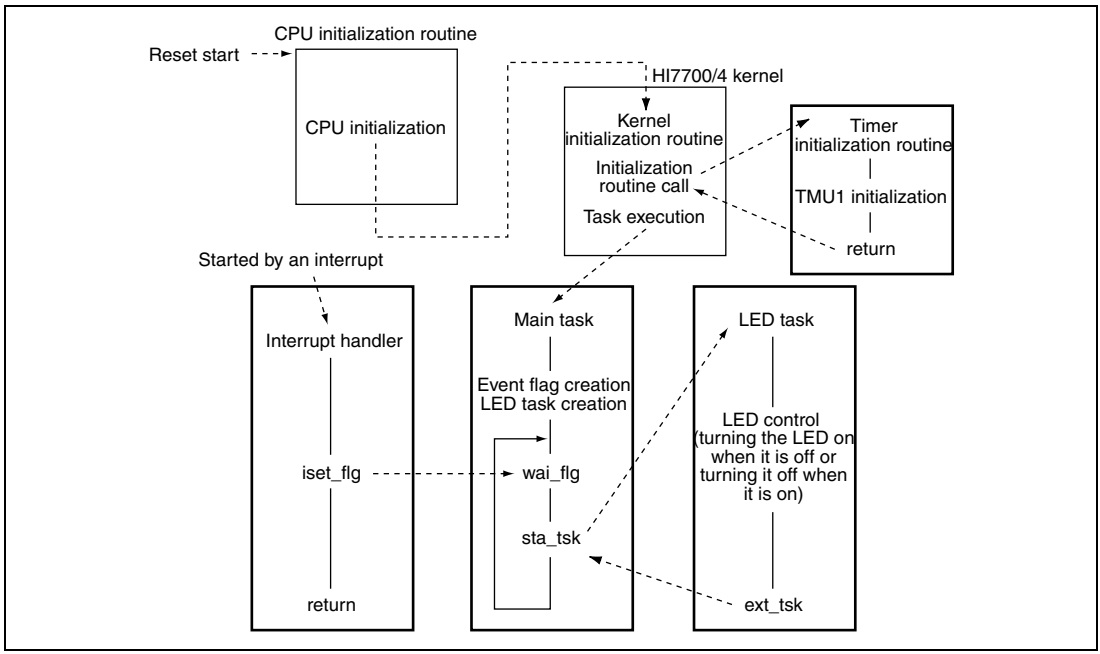


Figure 2.1 Relationship among Application Programs

Figure 2.2 shows the programs to be created in this guide.

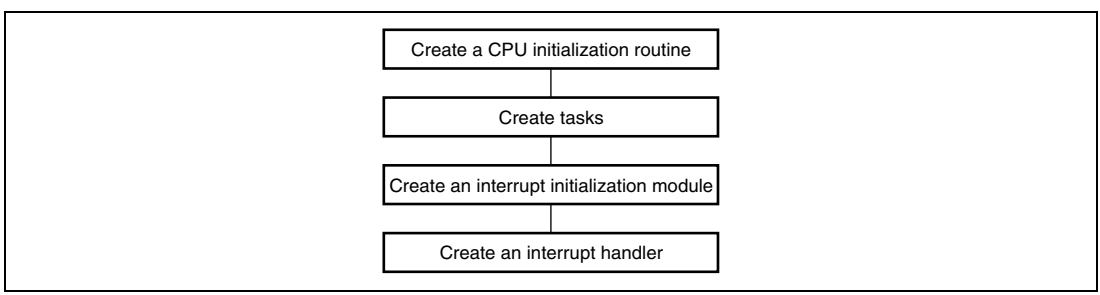


Figure 2.2 Programs to be Created

2.1 Creating CPU Initialization Routine

After the CPU reset, the CPU initialization routine is executed for setting a bus state controller and initializing the hardware.

The ROM monitor supplied with the Solution Engine has already set the bus state controller and initialized the hardware. Thus, this guide omits the description of them.

Figure 2.3 shows the procedure to create the CPU initialization routine.

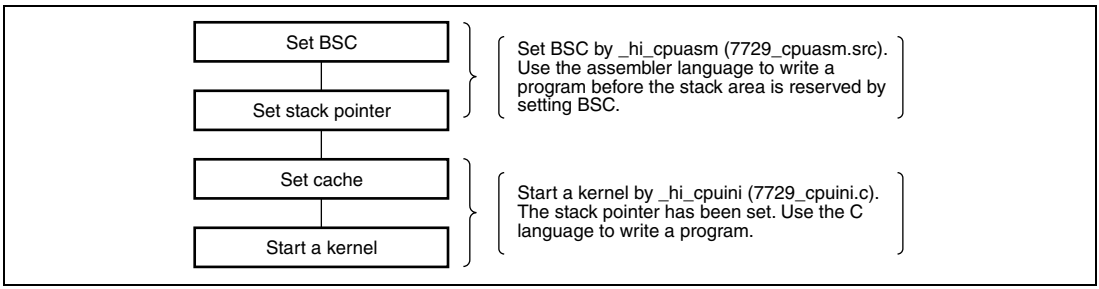


Figure 2.3 Creating a CPU Initialization Routine

In the CPU initialization routine, the stack pointer must be reserved completely before you attempt to execute any program written in the C language. Because the program created by the compiler may locate the stack frame or work area in a stack, you cannot execute it until the stack area is completely reserved.

Figures 2.4 to 2.7 show the parts to be changed in of _hi_cpuasm (7729_cpuasm.src).

```
;*****************************************************************************;
;*              HI7750/4 CPU initialize routine                              ;*;
;*              Copyright (c)  Hitachi, Ltd. 2000.                           ;*;
;*              Licensed Material of Hitachi, Ltd.                           ;*;
;*              HI7750/4(HS0775ITI41SR) V1.0                                 ;*;
;*****************************************************************************;
;
;*****************************************************************************;
;*  FILE      = 7750_cpuasm.src ;                                            ;*;
;*  CPU type  = SH7750                                                       ;*;
;*****************************************************************************;
        .program        _hi_cpuasm
        .heading        "hi_cpuasm : CPU initialize routine"
        .export         _hi_cpuasm
        .import         _hi_cpuini
        .import         __kernel_pon_sp
        .import         __kernel_man_sp
        .section        P_hicpuasm,code,align=4
;
;*****************************************************************************;
;* EXPEVT address, data                                                      ;*;
;*****************************************************************************;
CCN_BASE     .assign  h'ff000020           ; CCN base address
EXPEVT       .assign  h'ff000024-CCN_BASE  ; EXPEVT      address offset
;
PON_CODE     .assign  h'000                ; power-on reset exception code
;
```

Figure 2.4 Parts to be Changed in _hi_cpuasm (7729_cpuasm.src)

```
;*************************************************************************;
;*              BSC address                                              ;*;
;*************************************************************************;
BSC_BASE     .assign  h'ffffff60           ; BSC         base address
BCR1         .assign  h'ffffff60-BSC_BASE  ; BCR1        address offset
BCR2         .assign  h'ffffff62-BSC_BASE  ; BCR2        address offset
WCR1         .assign  h'ffffff64-BSC_BASE  ; WCR1        address offset
WCR2         .assign  h'ffffff66-BSC_BASE  ; WCR2        address offset
MCR          .assign  h'ffffff68-BSC_BASE  ; MCR         address offset
DCR          .assign  h'ffffff6a-BSC_BASE  ; DCR         address offset
PCR          .assign  h'ffffff6c-BSC_BASE  ; PCR         address offset
RTCSR        .assign  h'ffffff6e-BSC_BASE  ; RTCSR       address offset
RTCNT        .assign  h'ffffff70-BSC_BASE  ; RTCNT       address offset
RTCOR        .assign  h'ffffff72-BSC_BASE  ; RTCOR       address offset
RFCR         .assign  h'ffffff74-BSC_BASE  ; RFCR        address offset
BCR3         .assign  h'ffffff7E-BSC_BASE  ; BCR3        address offset
;
MCSCR_REG_BASE .assign  h'ffffff50         ; MCSCR register base address
MCSCR0         .assign  h'ffffff50-MCSCR_REG_BASE ; MCSCR0 address offset
MCSCR1         .assign  h'ffffff52-MCSCR_REG_BASE ; MCSCR1 address offset
MCSCR2         .assign  h'ffffff54-MCSCR_REG_BASE ; MCSCR2 address offset
MCSCR3         .assign  h'ffffff56-MCSCR_REG_BASE ; MCSCR3 address offset
MCSCR4         .assign  h'ffffff58-MCSCR_REG_BASE ; MCSCR4 address offset
MCSCR5         .assign  h'ffffff5a-MCSCR_REG_BASE ; MCSCR5 address offset
MCSCR6         .assign  h'ffffff5c-MCSCR_REG_BASE ; MCSCR6 address offset
MCSCR7         .assign  h'ffffff5e-MCSCR_REG_BASE ; MCSCR7 address offset
;
SDMR_CS2     .assign  h'ffffd000           ; SDMR (CS2)   base address
SDMR_CS3     .assign  h'ffffe000           ; SDMR (CS3)   base address
;
CMF_BIT      .assign  h'0080               ; CMF bit in RTCSR
;
;*************************************************************************;
;*              BSC initial data                                         ;*;
;*************************************************************************;
;*  After reset, you must initialize BSC for memory (stack) access at first.;*;
;*  Please modify these definition in order to your hardware.            ;*;
;*************************************************************************;
BCR1_DATA    .assign  h'0000               ; BCR1        initial data
BCR2_DATA    .assign  h'3ffc               ; BCR2        initial data
WCR1_DATA    .assign  h'3fff               ; WCR1        initial data
WCR2_DATA    .assign  h'ffff               ; WCR2        initial data
MCR_DATA     .assign  h'0000               ; MCR         initial data
DCR_DATA     .assign  h'0000               ; DCR         initial data
PCR_DATA     .assign  h'0000               ; PCR         initial data
RTCSR_DATA   .assign  h'a500 + h'00        ; RTCSR       initial data
RTCNT_DATA   .assign  h'a500 + h'00        ; RTCNT       initial data
RTCOR_DATA   .assign  h'a500 + h'00        ; RTCOR       initial data
RFCR_DATA    .assign  h'a400 + h'000       ; RFCR        initial data
BCR3_DATA    .assign  h'0000               ; BCR3        initial data
;
STP_REFRESH  .assign  h'a500               ; RTCSR initial data (stop count-up)
;
SDMR2_DATA   .assign  h'0230               ; SDMR_CS2    initial data
SDMR3_DATA   .assign  h'0230               ; SDMR_CS3    initial data
;
MCSCR_DATA   .assign  h'0000               ; MCSCR       initial data
;
IDLE_TIME    .assign  h'566                ; loop counter for idle-time
REFRESH_CNT  .assign  h'8                  ; counter for dummy refresh
;
```

Change the BSC value according to the hardware

Figure 2.5 Parts to be Changed in _hi_cpuasm (7729_cpuasm.src)

```
;*************************************************************************;
;*  NAME      = _hi_cpuasm                                                 ;*;
;*  FUNCTION  = CPU initialize routine                                     ;*;
;*************************************************************************;
_hi_cpuasm:
;***** Initialize BSC
;       mov.l   #BSC_BASE,r0            ; Set BCR base address to gbr
;       ldc     r0,gbr
;
;       mov.w   #BCR1_DATA,r0           ; Initialize BCR1
;       mov.w   r0,@ (BCR1,gbr)
;
;       mov.w   #BCR2_DATA,r0           ; Initialize BCR2
;       mov.w   r0,@ (BCR2,gbr)
;
;       mov.w   #WCR1_DATA,r0           ; Initialize WCR1
;       mov.w   r0,@ (WCR1,gbr)
;
;       mov.w   #WCR2_DATA,r0           ; Initialize WCR2
;       mov.w   r0,@ (WCR2,gbr)
;
;       mov.w   #MCR_DATA,r0            ; Initialize MCR
;       mov.w   r0,@ (MCR,gbr)
;
;       mov.w   #DCR_DATA,r0            ; Initialize DCR
;       mov.w   r0,@ (DCR,gbr)
;
;       mov.w   #PCR_DATA,r0            ; Initialize PCR
;       mov.w   r0,@ (PCR,gbr)
;
;       mov.w   #STP_REFRESH,r0         ; Stop refresh
;       mov.w   r0,@ (RTCSR,gbr)
;
;       mov.w   #RTCNT_DATA,r0          ; Initialize RTCNT
;       mov.w   r0,@ (RTCNT,gbr)
;
;       mov.w   #RTCOR_DATA,r0          ; Initialize RTCOR
;       mov.w   r0,@ (RTCOR,gbr)
;
;       mov.w   #RFCR_DATA,r0           ; Initialize RFCR
;       mov.w   r0,@ (RFCR,gbr)
;
;       mov.w   #BCR3_DATA,r0           ; Initialize BCR3
;       mov.w   r0,@ (BCR3,gbr)
;
;       mov.l   #MCSCR_REG_BASE,r0      ; Set MCSCR base address to gbr
;       ldc     r0,gbr
;
;       mov.w   #MCSCR_DATA,r0          ; Set Initialize MCSCR_DATA
;
;       mov.w   r0,@ (MCSCR0,gbr)       ; Initialize MCSCR0
;
;       mov.w   r0,@ (MCSCR1,gbr)       ; Initialize MCSCR1
;
;       mov.w   r0,@ (MCSCR2,gbr)       ; Initialize MCSCR2
;
;       mov.w   r0,@ (MCSCR3,gbr)       ; Initialize MCSCR3
;
;       mov.w   r0,@ (MCSCR4,gbr)       ; Initialize MCSCR4
;
;       mov.w   r0,@ (MCSCR5,gbr)       ; Initialize MCSCR5
;
;       mov.w   r0,@ (MCSCR6,gbr)       ; Initialize MCSCR6
;
;       mov.w   r0,@ (MCSCR7,gbr)       ; Initialize MCSCR7
;
```

Omit the comment to set BSC.

Figure 2.6 Parts to be Changed in _hi_cpuasm (7729_cpuasm.src)

```
;*** Initialize SDRAM
;
;       mov.l   #IDLE_TIME,r0           ; loop for idle-time
;hicpuasm010:
;       add     #-1,r0
;       cmp/eq  #0,r0
;       bf      hicpuasm010
;
;       mov.l   #SDMR_CS2,r0            ; Initialize SDMR (CS2)
;       mov.l   #SDMR2_DATA*4,r2
;       mov.b   r1,@ (r0,r2)            ; write dummy data (r1)
;
;       mov.l   #SDMR_CS3,r0            ; Initialize SDMR (CS3)
;       mov.l   #SDMR3_DATA*4,r2
;       mov.b   r1,@ (r0,r2)            ; write dummy data (r1)
;
;       mov.w   #RTCSR_DATA,r0          ; Initialize RTCSR
;       mov.w   r0,@ (RTCSR,gbr)
;
;       mov.w   #REFRESH_CNT,r2
;hi_cpuasm020:
;       mov.w   @ (RFCR,gbr),r0         ; read RFCR
;       cmp/ge  r2,r0                   ; if end dummy refresh
;       bf      hi_cpuasm020            ; else goto hi_cpuasm020
;
;hi_cpuasm030:
;
;***** Initialize sp and jump to hi_cpuini () written by C-language
        mov.l   #CCN_BASE,r2            ; get CCN base address
        mov.l   #PON_CODE,r3            ; get exception code to power-on
        mov.l   @ (EXPEVT,r2),r0        ; get exception code
        cmp/eq  r3,r0                   ; if exception != power-on
        bf      hi_cpuasm050            ; then hi_cpuasm050
;
        mov.l   #__kernel_pon_sp,r2          ; get stack address
;
hi_cpuasm040:
        mov     r2,r15                  ; set SP
;
        mov.l   #_hi_cpuini,r0          ; get hi_cpuini address
        jmp     @r0                     ; jump to hi_cpuini ()
        nop                             ; never return to this point
;
hi_cpuasm050:
        mov.l   #__kernel_man_sp,r2          ; get stack address
        bra     hi_cpuasm040
        nop
;
                .pool
;
        .end
```

Omit the comment to set BSC

Set stack pointer

Jump to hi_cpuini

Set stack pointer

Figure 2.7 Part to be Changed in _hi_cpuini (7729_cpuini.c)

```
/************************************************************************/
/*              HI7700/4 CPU initialize routine                         */
/*              Copyright  (c)  Hitachi, Ltd. 2001.                      */
/*              Licensed Material of Hitachi, Ltd.                      */
/*              HI7700/4 (HS0770ITI41SR) V1.0A                           */
/************************************************************************/
/************************************************************************/
/*  FILE      = 7729_cpuini.c ;                                         */
/*  CPU type  = SH7729                                                  */
/************************************************************************/
#include    <machine.h>
#include    "itron.h"
#include    "kernel.h"

/************************************************************************/
/*              environment data                                        */
/************************************************************************/
#define IOBASE   0xfffffe80             /* I/O base address    = 0xfffffe80 */
#define CCR       (0xffffffec - IOBASE)  /* CCN CCR           address offset */

#define CACHE_ON  0x00000001            /* CACHE enable  data              */
#define CACHE_OFF 0x00000000            /* CACHE disable data              */

/* extern  void    _INITSCT (void); */   /* section-initialize routine       */

#pragma section _hicpuini
/************************************************************************/
/*  NAME      = hi_cpuini                                               */
/*  FUNCTION  = CPU initialize routine                                  */
/************************************************************************/
#pragma noregsave (hi_cpuini)

void    hi_cpuini (void)
{

/*** Initialize Hardware Environment ***/
    set_gbr ( (VP)IOBASE);              /* set I/O base address to GBR      */
    gbr_write_long (CCR, CACHE_OFF);    gbr_write_long (CCR, CACHE_ON);

/*** Initialize Software Environment ***/

/*  _INITSCT ();    */                  /* Call section-initialize routine  */

    vsta_knl ();                        /* Start kernel                 */
}
```

Enable cache

Start a kernel

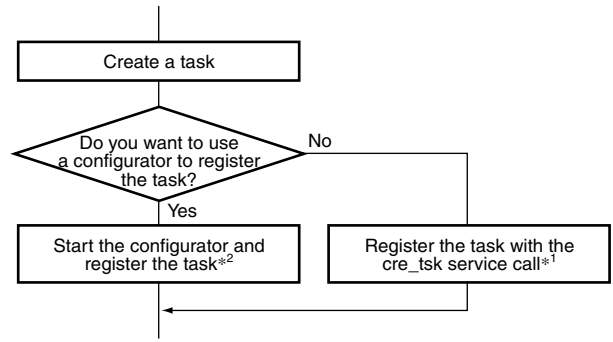
Figure 2.8 Part to be Changed in _hi_cpuini (7729_cpuini.c)

Set the bus state controller and create a hardware initialization routine for the specific hardware.

2.2 Creating Tasks

A task is the main processing of an application program.

Figure 2.9 shows the procedure to create and register a task.



Notes: 1. The cre_tsk service call must be enabled to register the task.
For details, see the HI7000/4 Series User's Manual.
2. This procedure is described in section 3, Configurator.

Figure 2.9 Creating and Registering Task

Create a task by changing the sample (task.c) supplied with HI7700/4. The sample is in the install folder “tutorial”.

In this guide, the main task (MainTask) is registered by the configurator and the LED task by the cre_tsk service call.

2.2.1 Main Task

This section describes how to change MainTask contained in the sample program (task.c) supplied with HI7700/4. Figure 2.10 shows the overview of changes made in MainTask. Starting task7 periodically turns the LED on and off.

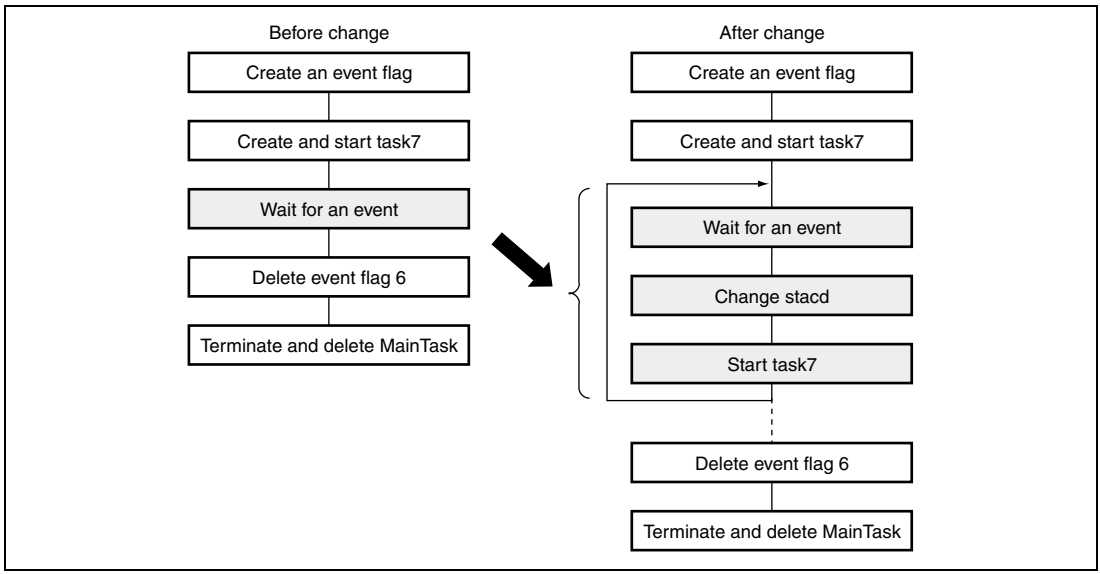


Figure 2.10 Overview of Changes Made in MainTask

Figure 2.11 shows the parts to be changed in MainTask.

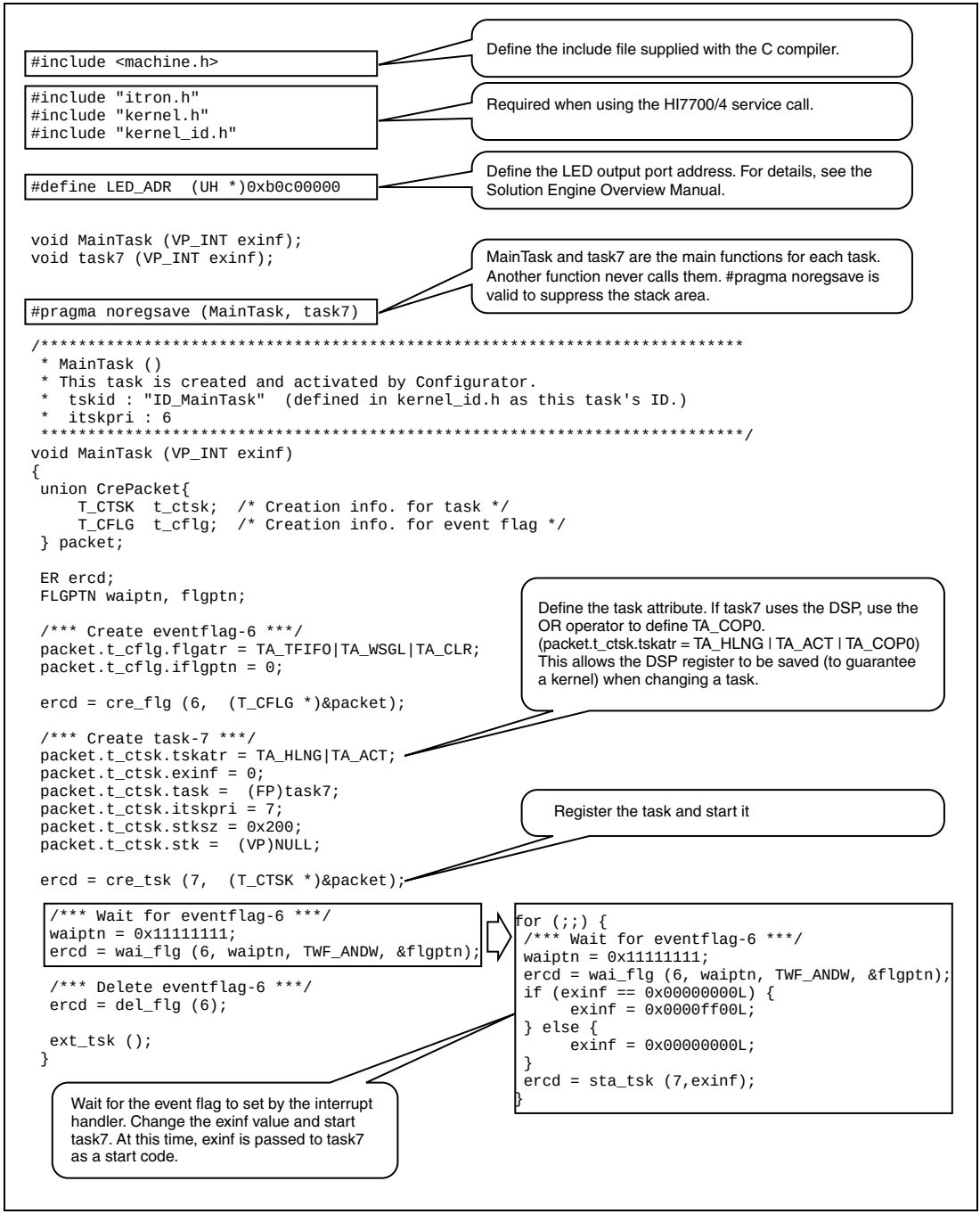


Figure 2.11 Changing MainTask

2.2.2 LED Task

This section describes how to change task7 of the sample program (task.c) supplied with HI7700/4. Figure 2.12 shows the part to be changed in task7.

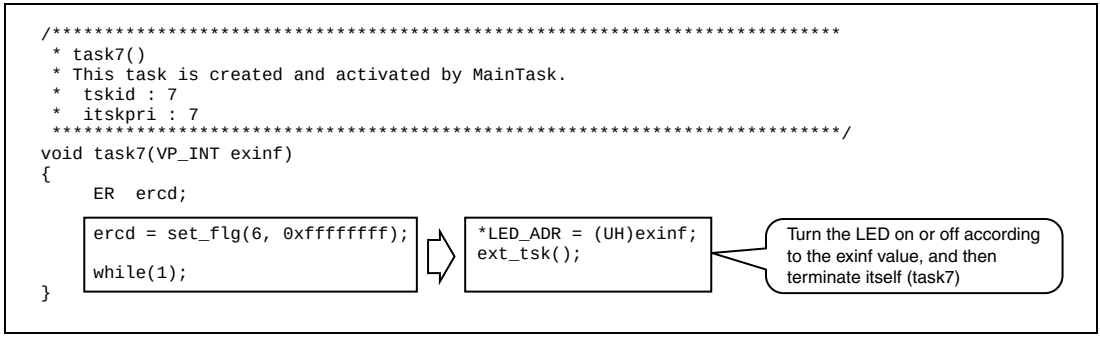


Figure 2.12 Changing task7

2.3 Creating an Interrupt Handler

The interrupt handler is started by an external interrupt that suspends another processing.

Figure 2.13 shows the procedure to create and register the initialization module and the interrupt handler.

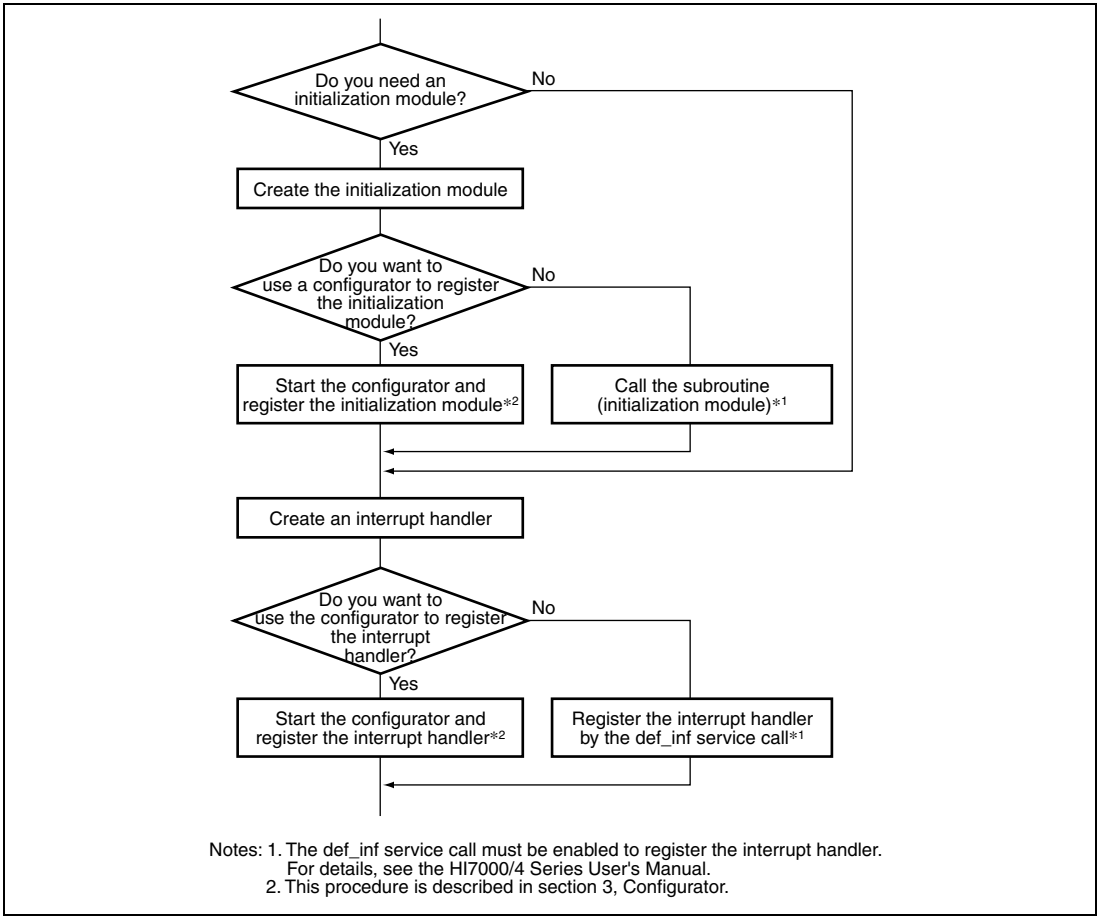


Figure 2.13 Creating and Registering Initialization Module and Interrupt Handler

This guide describes how to use the on-chip TPU1 in the SH7729 to create the interrupt handler and how to use a configurator to register it.

Create the tmu1.c file for the initialization module and the interrupt handler and store the file in the install folder “tutorial”. Note that the interrupts used in this guide has no relation with the timer used for time management by a kernel.

Table 2.1 lists the interrupt conditions.

Table 2.1 Interrupt Conditions

Item	Description	Function	File Name
Initialization module	Required. Use the configurator to register the module.	TMU2_ini	tmu2.c
Interrupt handler	Use the configurator to register the handler.	TMU2_int	tmu2.c
Interrupt cycle	An interrupt occurs every one second.	—	—
Interrupt level	1	—	—

2.3.1 Creating Initialization Module

This section describes how to create an initialization module for the on-chip TPU2 in the SH7729. The initialization module initializes the TPU1 and sets the interrupt cycle and level. Figure 2.14 shows the procedure to create the initialization module.

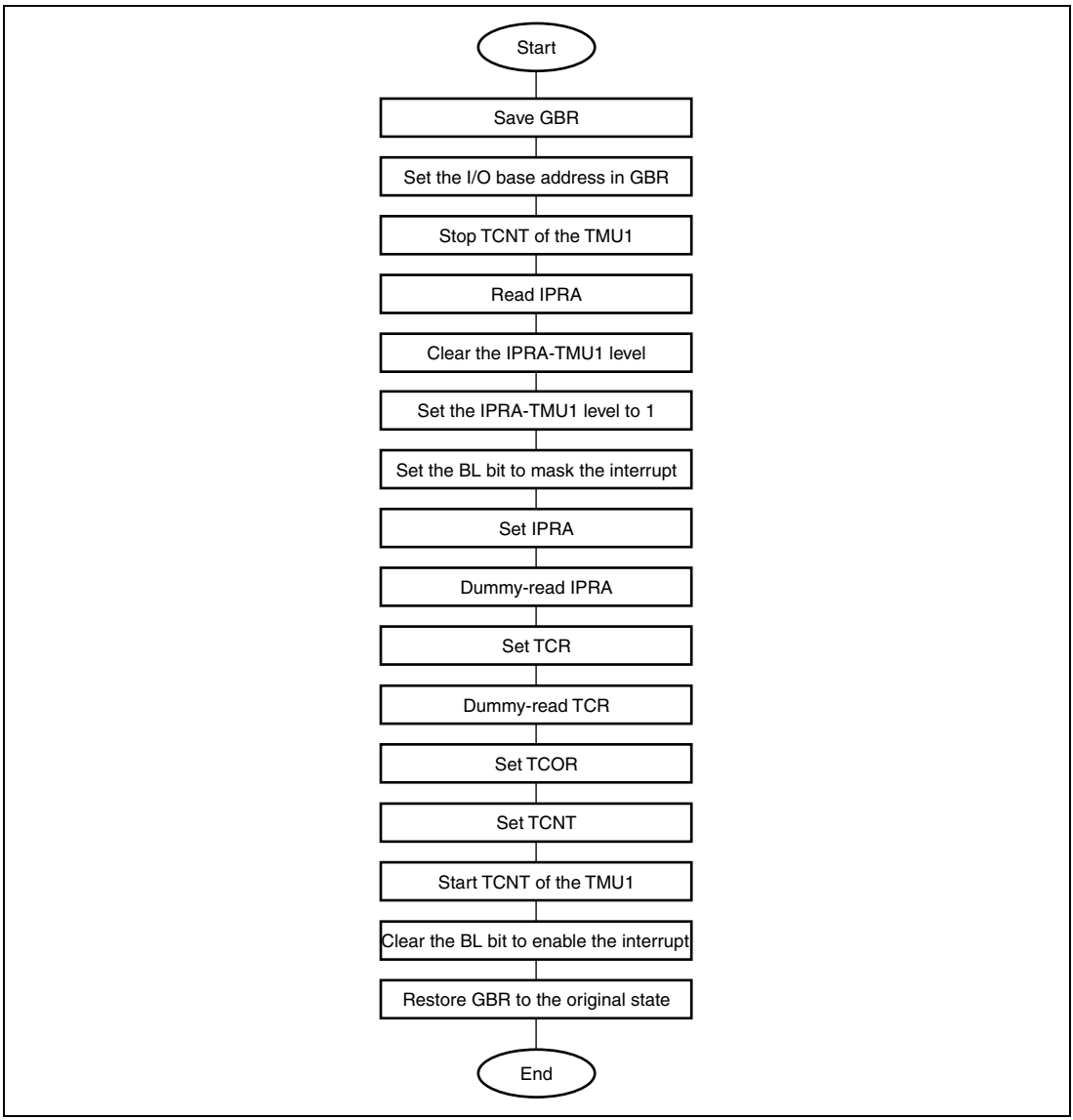


Figure 2.14 Creating Initialization Module

Figure 2.15 show the contents of TMU1_ini (tmu1.c).

```
#include <machine.h>
#include "itron.h"
#include "kernel.h"

#define BL_BIT 0x10000000               /* BL bit pattern                   */

/* Peripheral Clock (CPG set value = H'0102 (CPU:Bus:P = 133:33:33 MHz))    */
#define PCLK            33333400

/* TSTR set value */
#define TCNT1_STA       0x02            /* Start TCNT of the TMU1            */
#define TCNT1_STP       0xfd            /* Stop TCNT of the TMU1             */

/* TCR set value */
/* TCNT operated at a maximum frequency of 2 MHz */
#define DIV             64              /* Division ratio = 64                          */
#define DIV64           0x0002          /* Division ratio = 1/64                        */
#define UNIE            0x0020          /* Interrupt generated by an underflow of the TCR1 */

/* TCNT set value */
#define INTERVAL        1000000         /* 1 second: 1000ms: 1000000us                  */
#define TCNT1_DAT     (UW) (((double)INTERVAL/(((double)1/(double)PCLK)*(double)DIV))-(double)1)
                                        /* (1 second/ ( (1second/33.3334 MHz)*64))-1    */

/* IPRA set value */
#define IPRA_CLR_TPU1   0xf0ff          /* IPR bit8-11 clear data           */
#define TMU1_LVL        1               /* TMU1 interrupt level = 1         */

/* TMU,IPRA I/O address */
#define IOBASE   0xfffffe80             /* I/O base address = 0xfffffe80    */
#define TSTR     (0xfffffe92 - IOBASE)  /* TMU TSTR          address offset */
#define TCOR1    (0xfffffea0 - IOBASE)  /* TMU TCOR (ch1)     address offset */
#define TCNT1    (0xfffffea4 - IOBASE)  /* TMU TCNT (ch1)     address offset */
#define TCR1     (0xfffffea8 - IOBASE)  /* TMU TCR  (ch1)     address offset */
#define IPRA     (0xfffffee2 - IOBASE)  /* IPRA (TMU0:TMU1:TMU2:RTC) address */

/************************************************************************/
/*  NAME      = TMU1_ini                                                */
/*  FUNCTION  = initialize the TMU1                                     */
/************************************************************************/
void TMU1_ini (void)
{
    VP      gbrsave;                    /* GBR save area                    */
    UH      ipra;                       /* IPRA retention area              */

    gbrsave = get_gbr ();               /* GBR save area                    */
    set_gbr ( (VP)IOBASE);              /* Set the I/O base address in GBR  */

    gbr_and_byte (TSTR,TCNT1_STP);      /* Stop TCNT of the TMU1            */
    ipra = gbr_read_word (IPRA);        /* Read IPRA                        */
    ipra &= IPRA_CLR_TPU1;              /* Clear the IPRA-TMU1 level        */
    ipra |= TMU1_LVL << 8;              /* IPRA-TMU1 level = 1              */

    set_cr (BL_BIT | get_cr ());       /* Set the BL bit to mask an interrupt */
    gbr_write_word (IPRA,ipra);         /* Set IPRA                         */
    gbr_read_word (IPRA);               /* Dummy-read IPRA                  */

    gbr_write_word (TCR1,UNIE|DIV64);   /* Set TCR                          */
    gbr_read_word (TCR1);               /* Dummy-read TCR                   */

    gbr_write_long (TCOR1,TCNT1_DAT);   /* Set TCOR                         */
    gbr_write_long (TCNT1,TCNT1_DAT);   /* Set TCNT                         */

    gbr_or_byte (TSTR, TCNT1_STA);      /* Start TCNT of the TMU1           */

    set_cr (~BL_BIT & get_cr ());       /* Clear the BL bit to enable an interrupt  */
    set_gbr (gbrsave);                  /* Restore GBR to the original state        */
}
```

Figure 2.15 Contents of TMU1_ini (tmu1.c)

2.3.2 Creating Interrupt Handler

This section describes how to create an interrupt handler for the on-chip TPU1 in the SH7729R. The interrupt handler clears an interrupt source of the TPU1 and issues an event flag to task7. Figure 2.16 shows the procedure to create the interrupt handler.

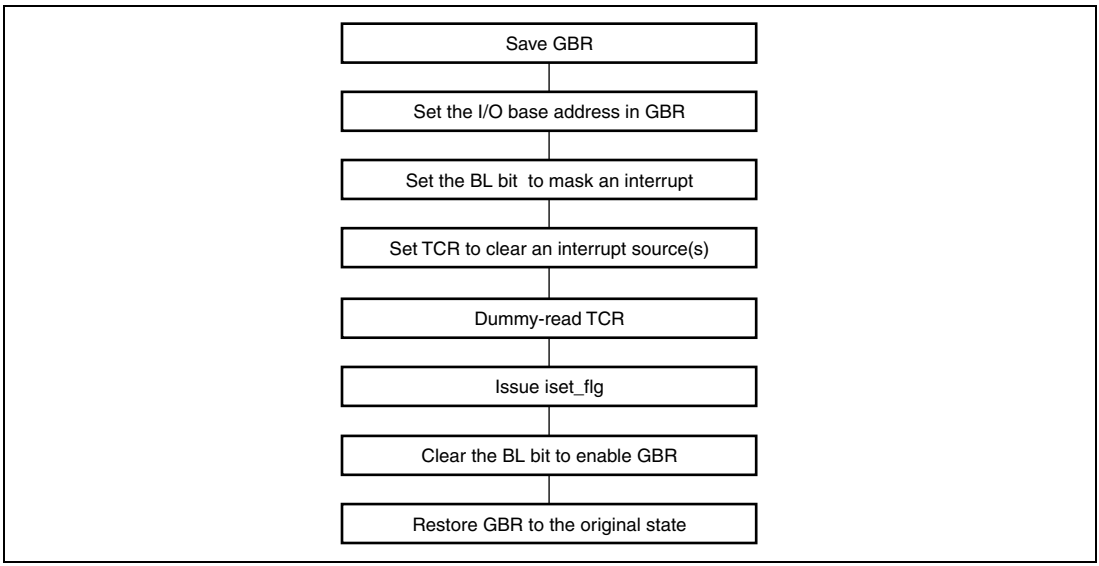


Figure 2.16 Creating Interrupt Handler

Figure 2.17 shows the contents of TMU2_int (tmu1.c).

```
/************************************************************************/
/*  NAME      = TMU1_int                                                */
/*  FUNCTION  = TMU1 Interrupt Handler                                  */
/************************************************************************/
void    TMU1_int (void)
{
    VP      gbrsave;                    /* GBR save area                        */

    gbrsave = get_gbr ();               /* Save GBR                             */
    set_gbr ( (VP)IOBASE);              /* Set the I/O base address in GBR      */
    set_cr (BL_BIT | get_cr ());        /* Set the BL bit to mask an interrupt  */

    gbr_write_word (TCR1,TCNT1_DAT);    /* Clear UNF                            */
    gbr_read_word (TCR1);               /* Dummy-read TCR                       */

    iset_flg (6, 0xffffffff);           /* Set an event flag for task7          */

    set_cr (~BL_BIT & get_cr ());       /* Clear the BL bit to enable an interrupt */
    set_gbr (gbrsave);                  /* Restore GBR to the original state    */
}                                       /* ret_int                              */
```

Figure 2.17 Contents of TPU2_int (tpu2.c)

Section 3 Configuration

Configuration means to register the programs created in section 2 to HI7700/4. HI7700/4 provides a tool that allows easy configuration using GUI and a configurator.

This section describes how to use the configurator to register the application programs.

Figure 3.1 shows the programs to be registered in this guide.

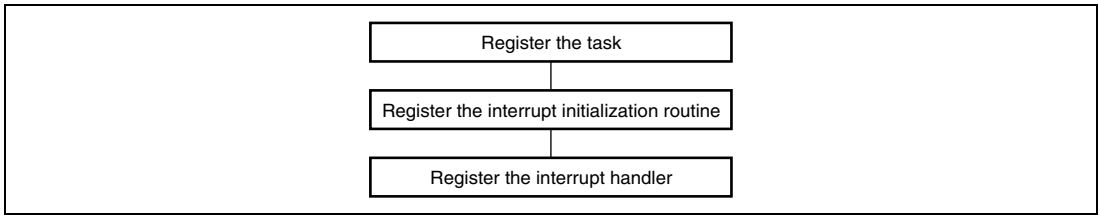


Figure 3.1 Programs to be Registered

The defaults are used for programs other than those above.

For details of each program set by the configurator, see the Configurator Help.

3.1 Starting Configurator

Double-click the configurator set file (7729.hcf) to start the configurator. The 7729.hcf file is in the install folder “sh7729”.

Figure 3.2 shows the Configurator Startup screen.

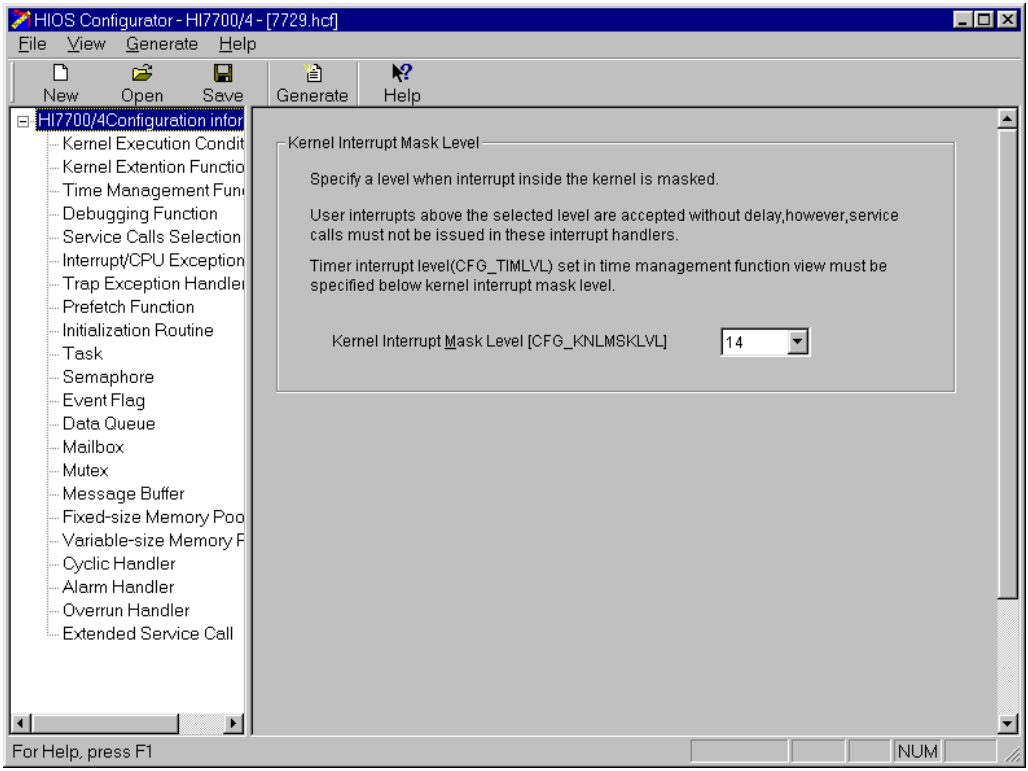


Figure 3.2 Configurator Startup Screen

3.2 Interrupt Mask Level

Table 3.1 lists the interrupt mask levels for the application programs in this guide.

Table 3.1 Interrupt Mask Levels

Type	Mask Level	Remarks
Task	0	
Interrupt handler	1	
Kernel	14	Default

Click kernel operational conditions in the HI7700/4 Configuration Information area on the Configuration Startup screen to view the screen in figure 3.2. In this screen, the mask level for a kernel interrupt can be set. Since the default value (14) is used for the mask level of a kernel interrupt in this guide, you do not need to change the interrupt level.

3.3 Registering Task

Click Task in the HI7700/4 Configuration Information area on the Configuration Startup screen to view the Task Information screen in figure 3.3.

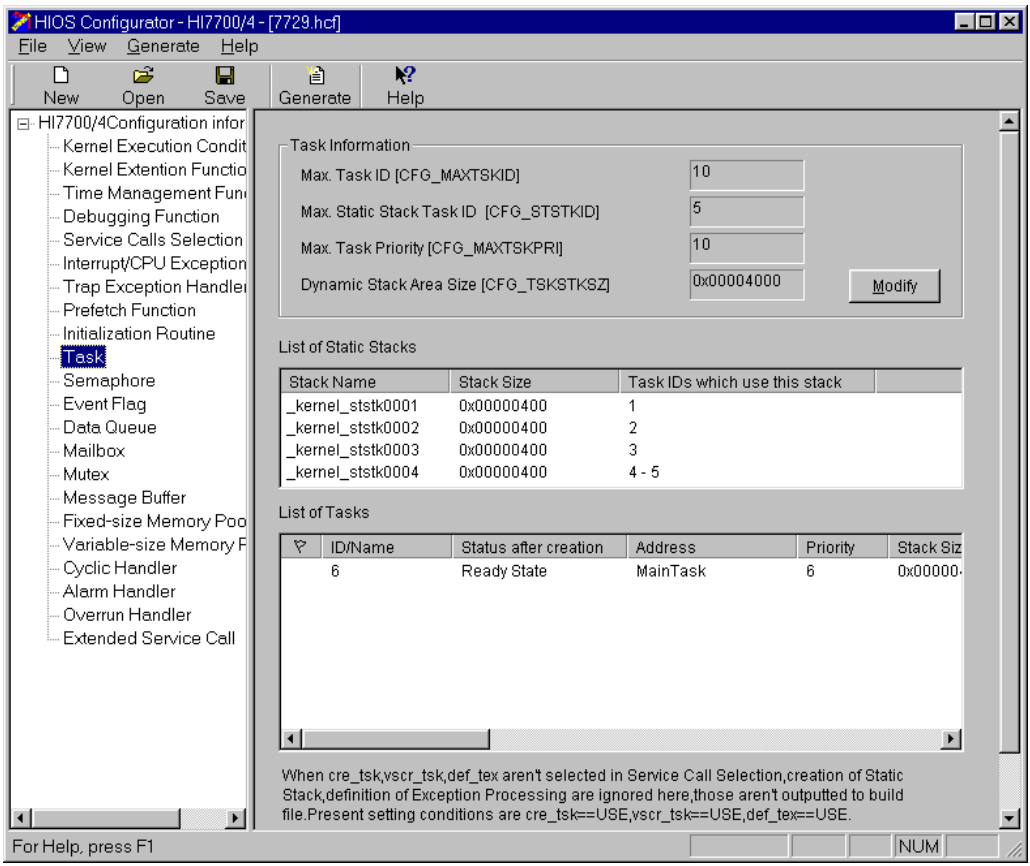


Figure 3.3 Task Information Screen

Click the Change button in the Task Information area in figure 3.3 to view the Modification of Task Information screen in figure 3.4.

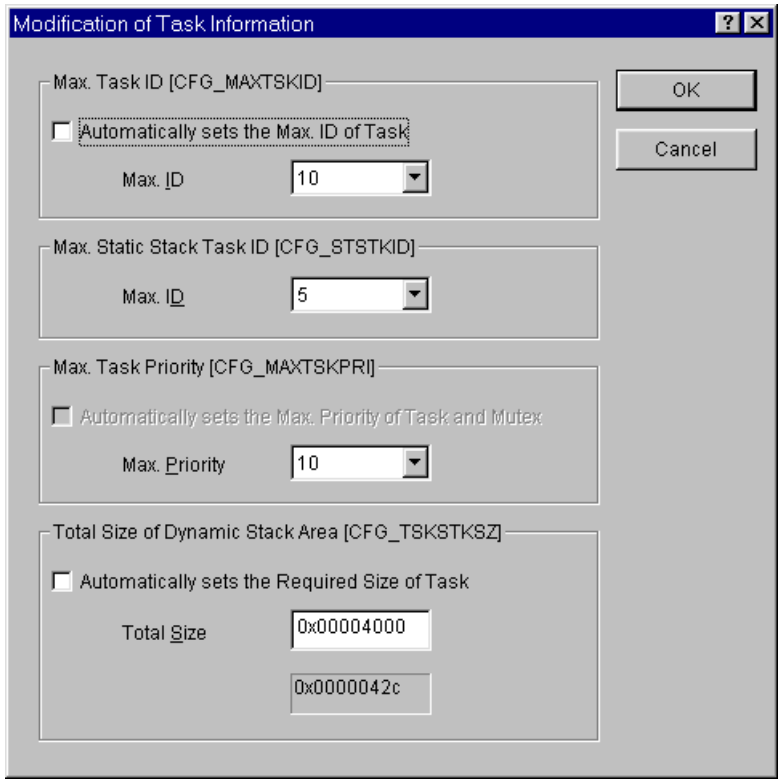


Figure 3.4 Modification of Task Information Screen

On this screen, you can change the maximum task ID, the maximum task ID using static stacks, maximum task priority, and the total size of the dynamic stack area. For details about differences between static stacks and dynamic stacks, see section 2.6.6, Task Stack, in the HI7000/4 Series User's Manual.

For details about how to calculate the task stack size, see Appendix C, Calculation of Work Area Size, in the HI7000/4 Series User's Manual.

In this guide, the defaults are used for registering the task. You do not need to change the task information.

3.4 Registering Interrupt Handler

Click Interrupt and CPU Exception Handler in the HI7700/4 Configuration Information area on the Configuration Startup screen to view the List of Interrupt/CPU/Trap Exception Handlers screen in figure 3.5.

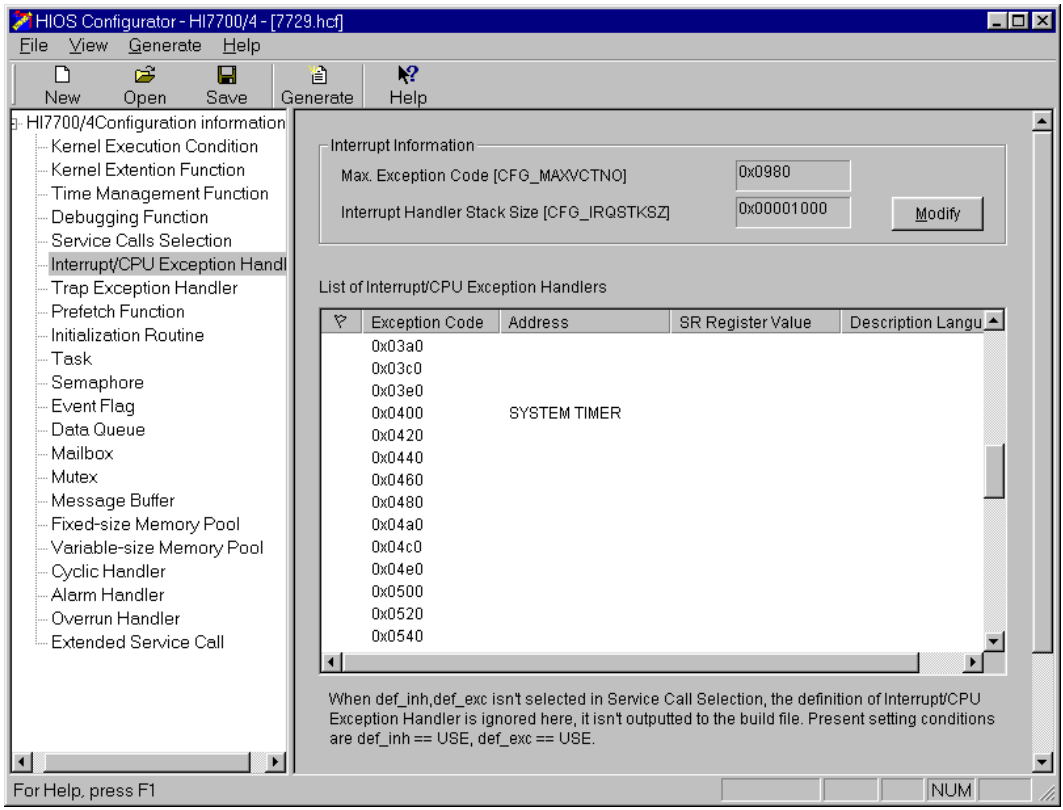


Figure 3.5 List of Interrupt/CPU/Trap Exception Handlers Screen

On-chip TPU1 in the SH7729 is used for an interrupt source in this guide. Use the mouse on the scroll bar on the right of the List of Interrupt/CPU/Trap Exception Handlers to view the exception code around 0x0420. Double click exception code 0x0420 to view the Definition of Interrupt/CPU/Trap Exception Handler screen in figure 3.6.

The exception code, 0x0420, is used for the TMU1 interrupt exception code in this guide. For details of the exception code, see the SH7729R Hardware Manual.

Double click exception code 0x0420 to view the screen shown in figure 3.6.

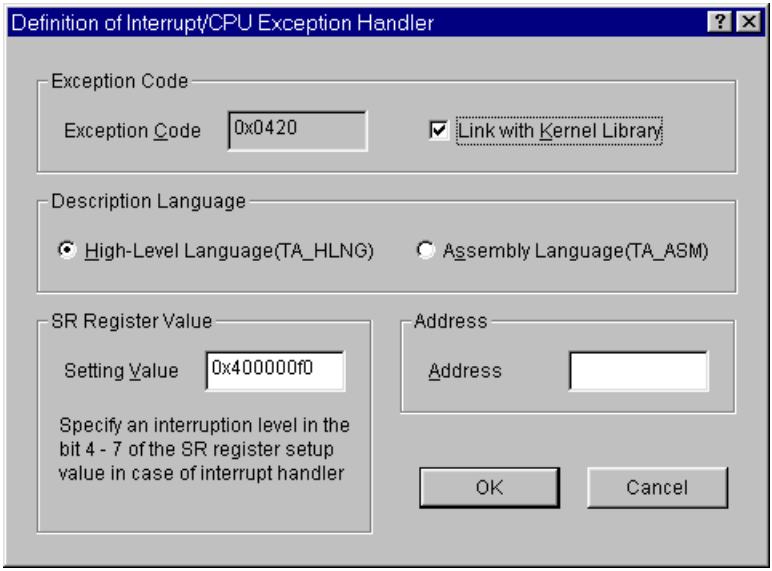


Figure 3.6 List of Interrupt/CPU/Trap Exception Handlers Screen

Set TMU1_int in the Address box. The mask level of the interrupt handler in this guide is 1. So change the SR register setting to 0x4000010 (bits 4 to 7 in SR are the mask bits).

This SR register setting is used as a SR register setting when control is passed to the TMU1_init interrupt handler. The level should be set to higher than hardware interrupt levels. However, if a service call is issued from the interrupt handler, the level must be set to less than the level of a kernel.

Figures 3.7 and 3.8 show the Definition of Interrupt/CPU/Trap Exception Handler screens after you made definitions.

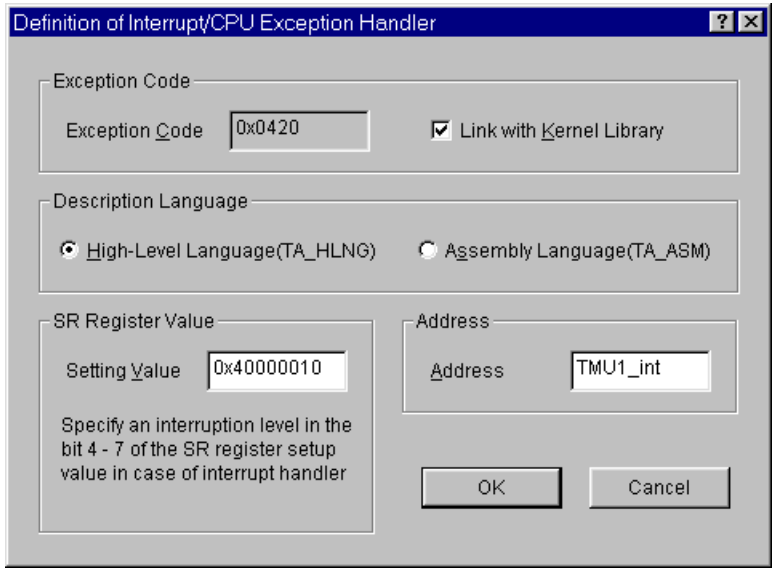


Figure 3.7 Definition of Interrupt/CPU/Trap Exception Handler Screen

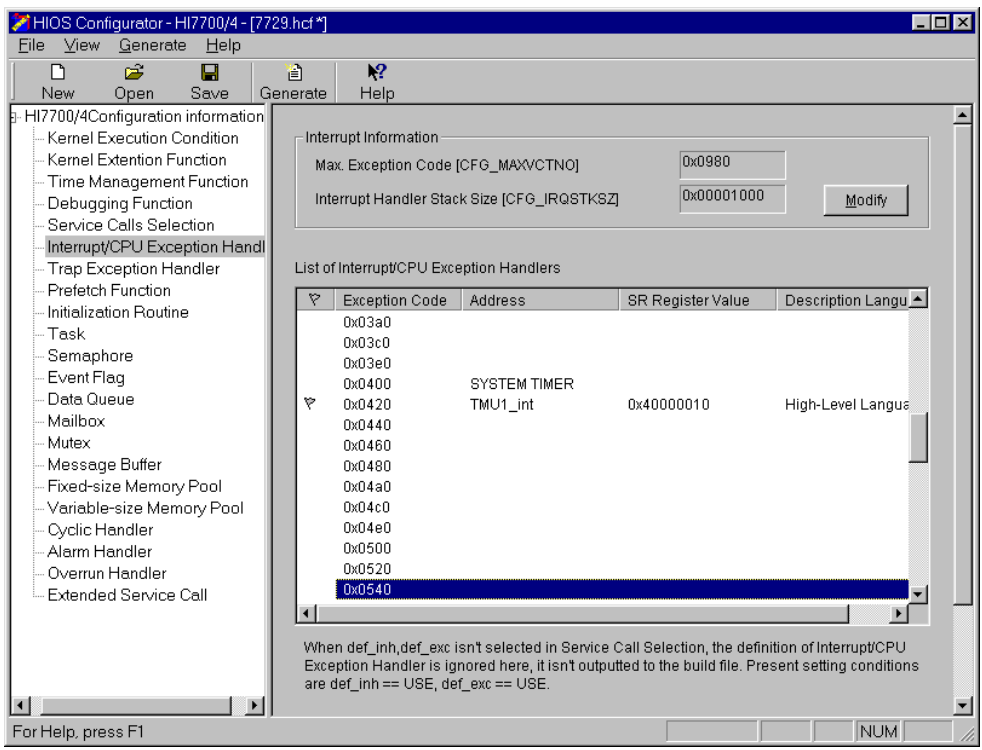


Figure 3.8 Definition of Interrupt/CPU/Trap Exception Handler Screen (after Making Definitions)

For details about how to calculate the handler stack size, see Appendix C, Calculation of Work Area Size, in the HI7000/4 Series User's Manual.

3.5 Registering Initialization Routine

Click Initialization Routine in the HI7700/4 Configuration Information area on the Configurator Startup screen to view the Initialization Routine List screen in figure 3.9.

The initialization routine that is registered on this screen is called immediately after the kernel startup (setup) completes and executed with the kernel mask level (the value set for the kernel operational conditions in the configuration information). This routine differs from the CPU initialization routine that is executed immediately after a reset.

In the initialization routine, the service call of a kernel can be issued.

The issuable service call is the one that can be called from non-task context (system state: N) described in section 3, Service Calls, in the HI7000/4 Series User's Manual.

The initialization routine is used for the following purposes:

1. Interrupt initialization
2. Initialization routine for task setup
3. Event flag, mailbox, or memory pool of which initial setting is to be completed before passing the control to a task or an interrupt handler

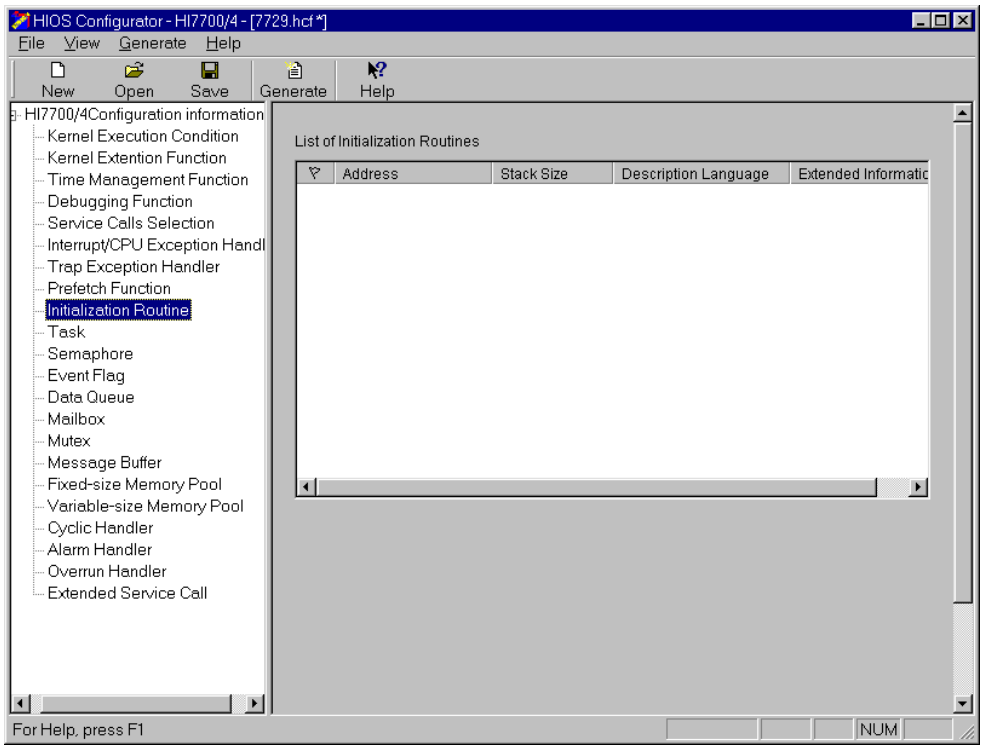


Figure 3.9 List of Initialization Routines Screen

Right click on the blank area of the List of Initialization Routines to view the menu. Then, select Register to view the Registration of Initial Routine screen in figure 3.10.

The following explains how to register the initial routine.

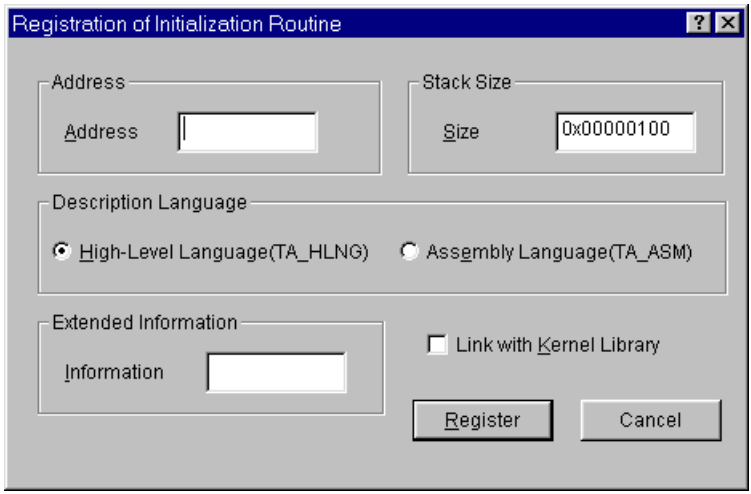


Figure 3.10 Registration of Initialization Routine Screen

Set TMU1_ini in the Address box and click the Register button, and then the Close button. Use the expression below to obtain the stack size.

- TMU1_ini stack frame size: 8 bytes
- Required size for the initialization routine: 184 + 24 bytes

  Total: 216 bytes

For details about how to calculate the stack size, see Appendix C, Calculation of Work Area Size, in the HI7000/4 Series User's Manual. Use the default since the calculated stack size is smaller than it.

Figure 3.11 shows the Registration of Initialization Routine screen after registration. Figure 3.12 shows the List of Initialization Routines screen after registration.

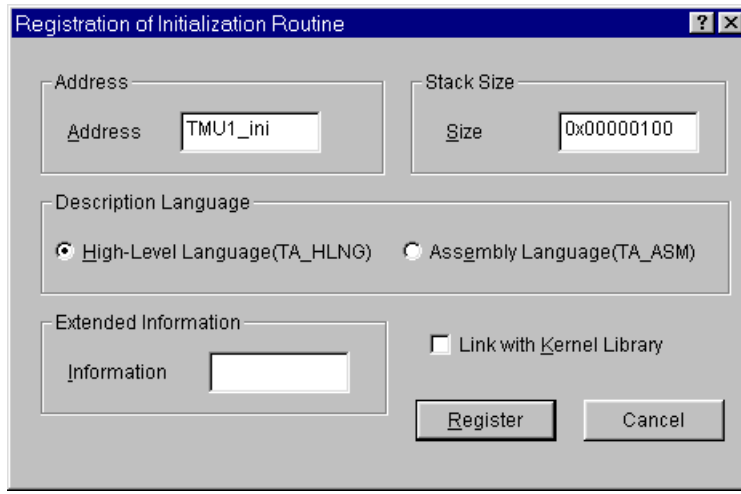


Figure 3.11 Registration of Initialization Routine Screen (after Registration)

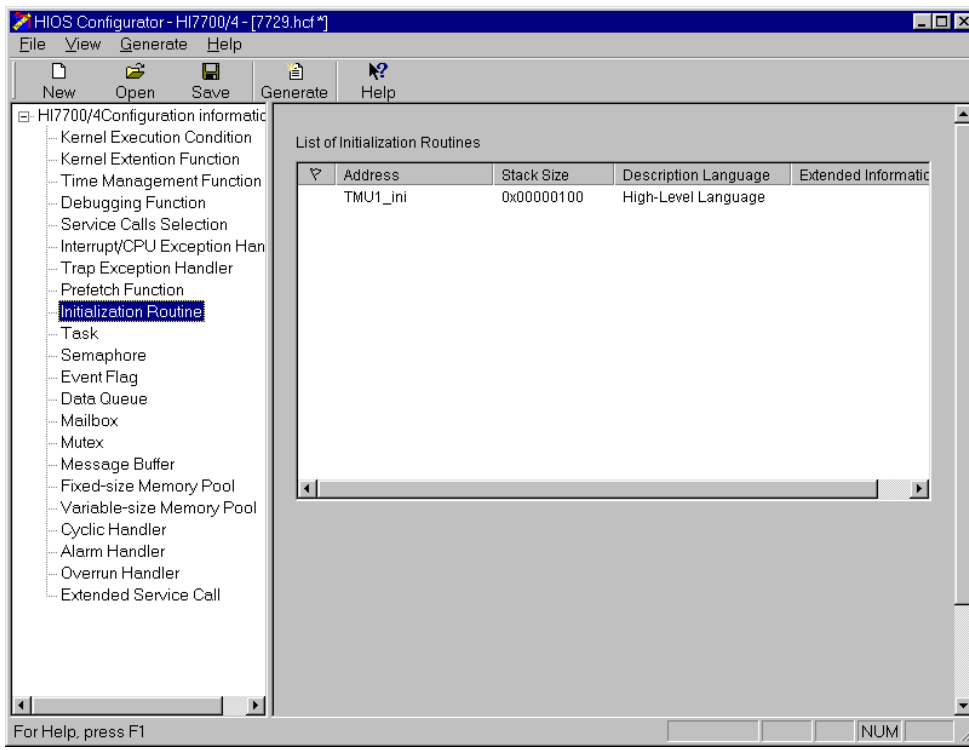


Figure 3.12 List of Initialization Routines Screen (after Registration)

3.6 Registering Event Flag Information

Click Event Flag in the HI7700/4 Configuration Information area on the Configuration Startup screen to view the Event Flag Information screen in figure 3.13.

Click the Change button in the Event Flag Information area to change the maximum event flag ID. Right click on the blank area of the Event Flag List and select Create to view the Creation of Event Flag screen in figure 3.14. For initial creation of an event flag, set the information about the event flag on this screen.

The application implemented in this guide dynamically creates one event flag in the task. Use the default event flag information.

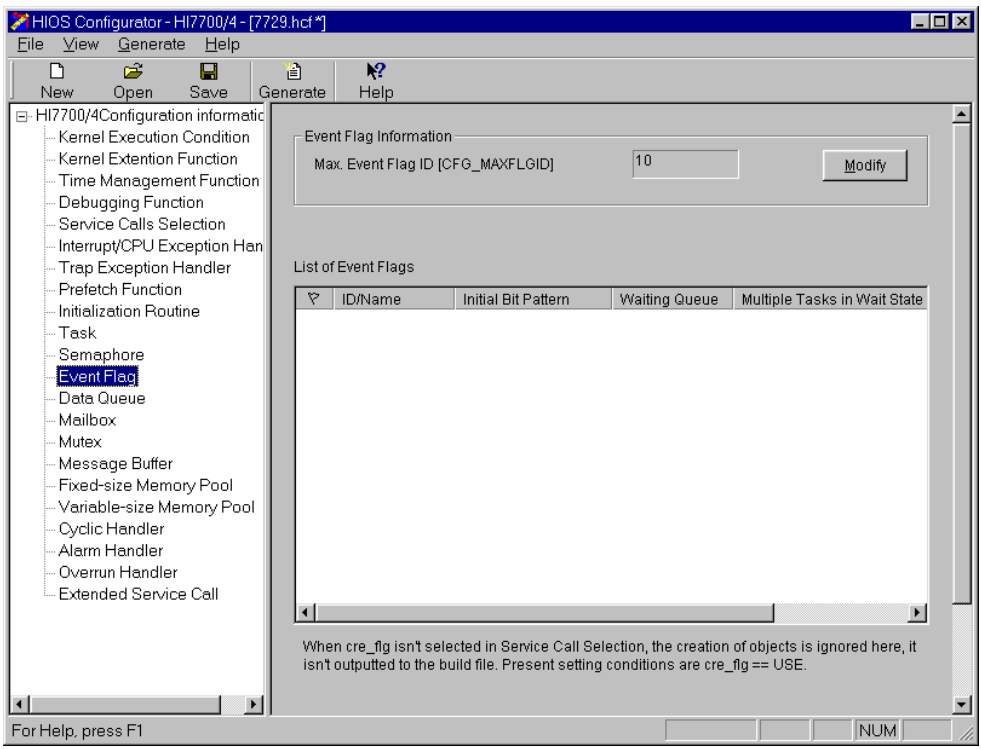


Figure 3.13 Event Flag Information Screen

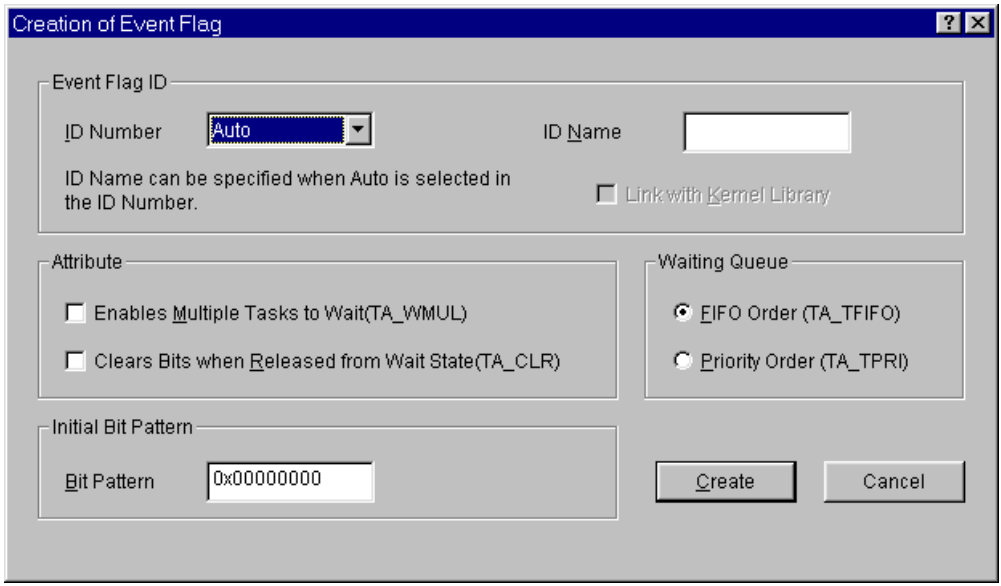


Figure 3.14 Creation of Event Flag Screen

3.7 Creating Configuration Files

Click the Create button on the Configurator Startup screen to create the configuration files required for configuring HI7700/4. For details about the configuration files, see section 5.1.2, Configurator Output File, in the HI7000/4 Series User's manual.

Now, the definition and registration by the configurator are complete. To close 7729.hcf, choose Overwrite or Save As from the File menu to save all the information.

3.8 Building the Executable File by HEW

Compile and link the files created by the configurator using HEW supplied with SHC/C++ compiler to create the executable file to be downloaded. This section describes how to build the executable file by HEW.

There are two methods to configure HI7700/4. Table 3.2 lists the type of links.

Table 3.2 Type of Links

Type	Description
Whole linkage	Links the kernel and all configuration files into a single load module (called a whole load module).
Separate linkage	Links the kernel code portion (called a kernel load module) and the kernel data portion (called a kernel environment load module) into separate load modules. Application files can be included in a kernel load module, a kernel environment load module, or in an independent application load module.

For details, see section 5, Configuration, in the HI7000/4 Series User's Manual.

This guide describes how to use the whole link method to configure the program in big endian format.

3.8.1 Starting HEW

Double click hios.hws in the install folder “hios” to start HEW to build HI7700/4. Figure 3.15 shows the HEW Startup screen.

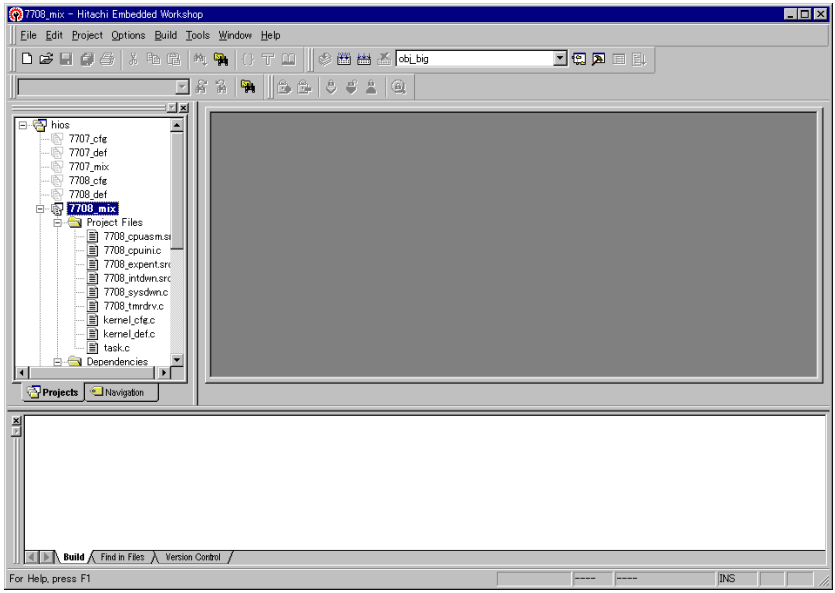


Figure 3.15 HEW Startup Screen

The standard project file hios.hws contains three sub-projects to configure the program for the target CPU. Table 3.3 lists the type of project files.

Table 3.3 Project Files

7729_mix	Project file for creating the whole load module for the whole link method
7729_cfg	Project file for creating the kernel load module for the separate link method
7729_def	Project file for creating the kernel environment load module for the separate link method

Select the project file 7729_mix for creating the whole load module.

Figure 3.16 shows the Set Current Project screen.

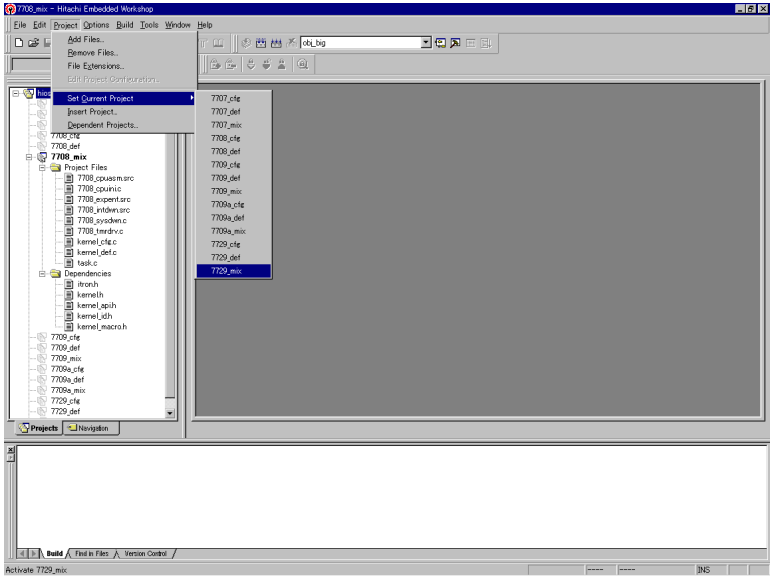


Figure 3.16 Set Current Project Screen

3.8.2 Defining Configuration File

Define each application program created in section 2 as a project file. Use the default project file configuration and define only the timer driver to implement the sample program operation in this guide.

On the Current Project Set screen, select Add Files... from the Project menu to add tmu1.c as a project file. Figures 3.17 and 3.18 show the screen for adding a file.

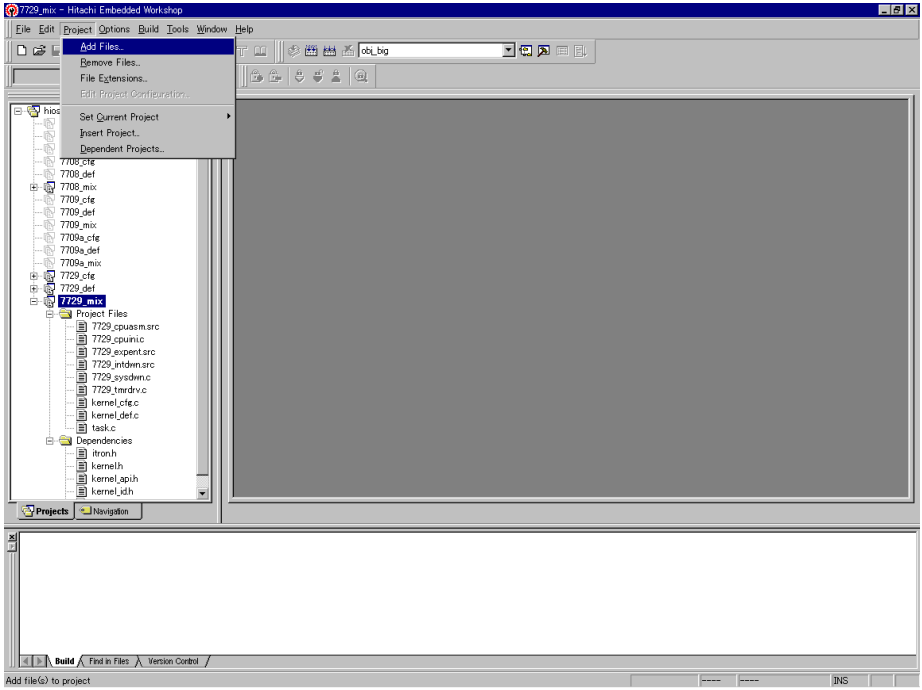


Figure 3.17 Adding a File

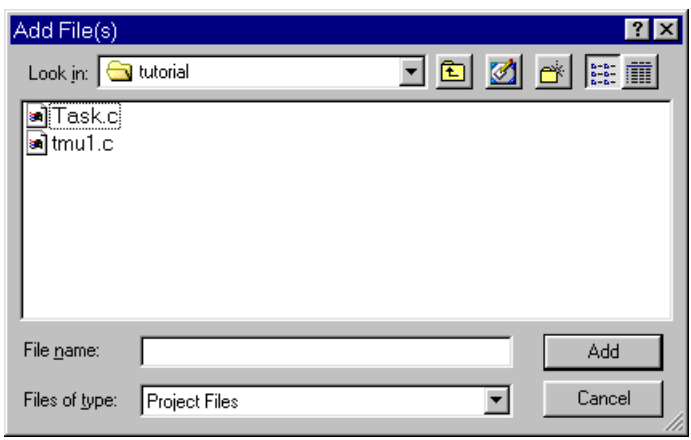


Figure 3.18 Adding a File

Now, defining the configuration files completes.

3.8.3 Changing a Linkage Address

Change the linkage addresses to run the programs on the Solution Engine address map.

The Solution Engine is supplied with 32-Mbyte SDRAM from 0x0C00000 to 0x0FFFFFFF. In this guide, 16 Mbytes from 0x0C00000 to 0x0CFFFFFF are used.

Select OptLinker from the Options menu to view the OptLinker Options screen (figure 3.19).

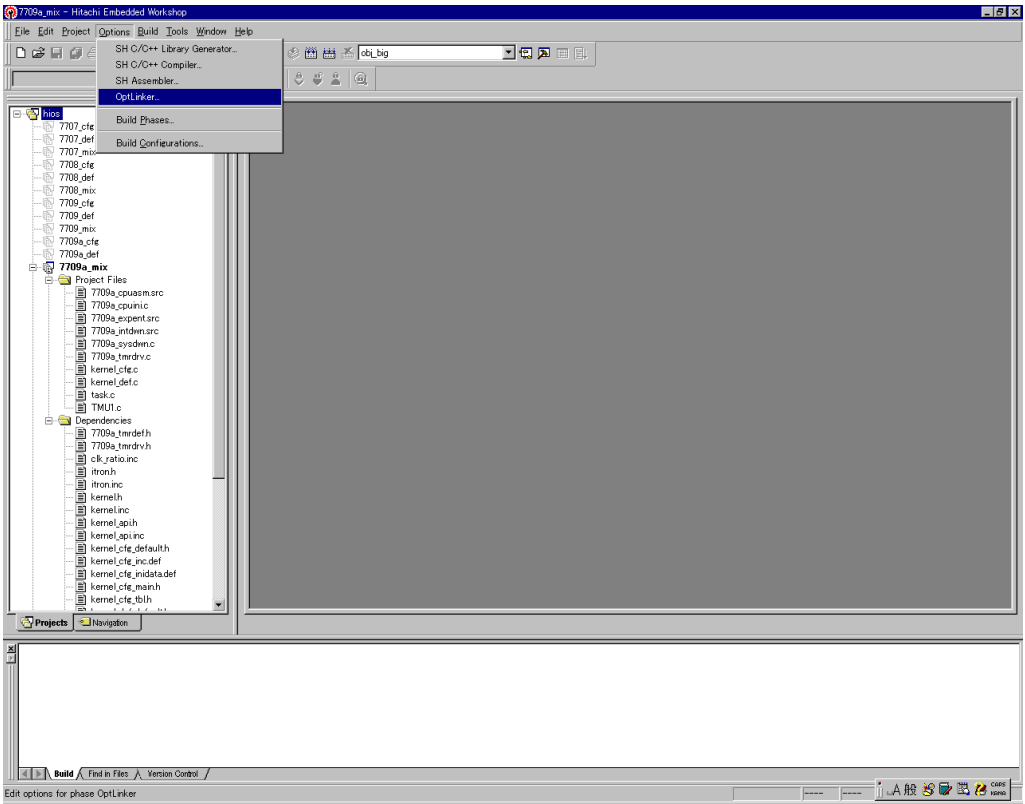


Figure 3.19 Selecting OptLinker

- Changing a kernel stack pointer

Double click _kernel_pon_sp and _kernel_man_sp in the Input tab and set the value so that the values point to the end address of the RAM mounted on each hardware + 1 (0xAD000000 in P2 space) as shown in figures 3.20 to 3.22.

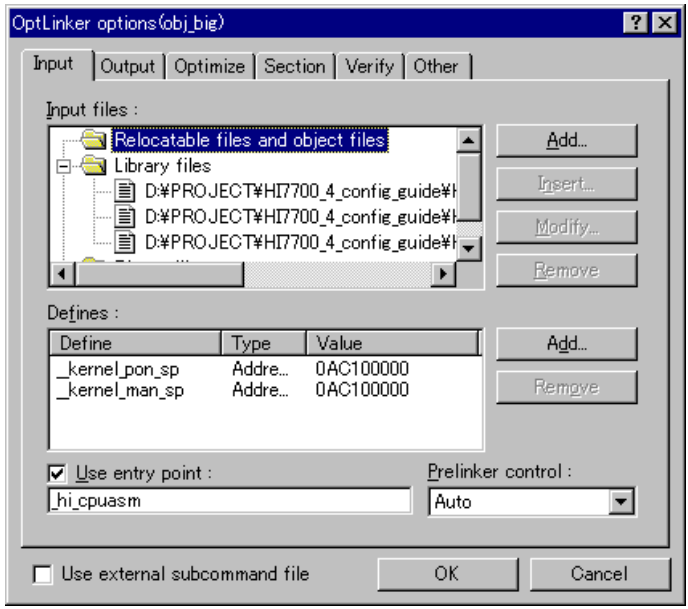


Figure 3.20 OptLinker options Screen

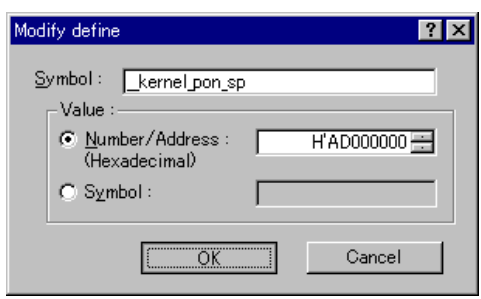


Figure 3.21 OptLinker options Screen (_kernel_pon_sp)

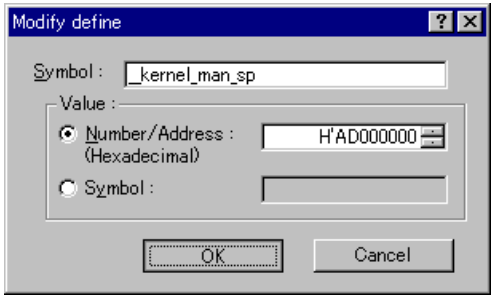


Figure 3.22 OptLinker options Screen (_kernel_man_sp)

- Changing a section address

Click the Section tab to view the Define Section screen (figure 3.23).

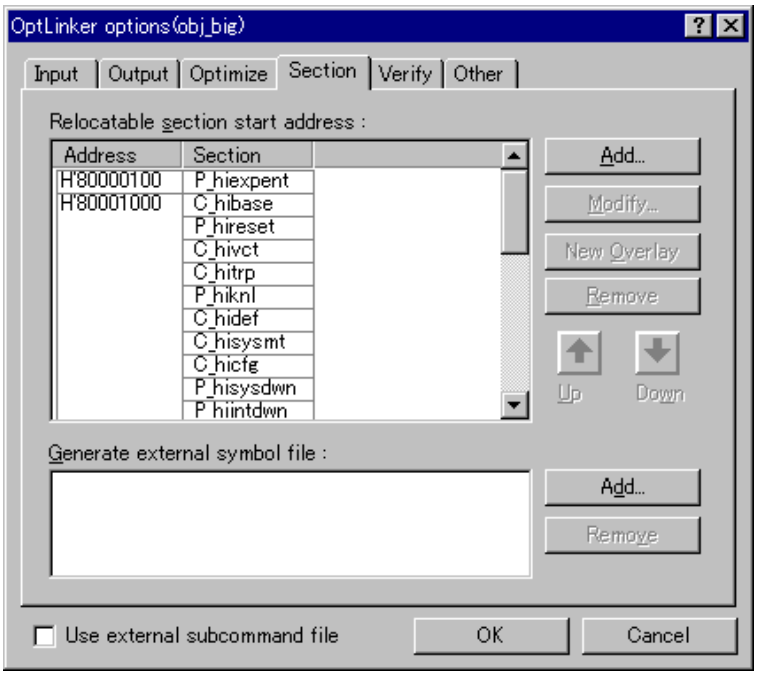


Figure 3.23 Define Section Screen

Click Address for each section to enable the Modify... button. Change the section addresses as listed in table 3.4.

Table 3.4 Section Addresses

Section Name	Before Change	After Change	Section Name	Before Change	After Change
P_hiexpent	80000100	8C000100	B_hiwrk	8C000000	8C010000
C_hibase	80001000	8C001000	B_himpl		
P_hireset			B_hidystk		
C_hivct			B_histstk		
C_hitrp			B_hiirqstk		
P_hiknl			B_hitrcbuf		
C_hidef			B_hitrceml		
C_hisysmt			B		
C_hicfg			R		
P_hisysdwn			P_hicpuasm	A0000000	AC000000
P_hiintdwn			P_hicpuini		
P_hitmrdrv					
P					
C					
D					

3.8.4 Build

Execute HEW to build an executable file that can be downloaded to the Solution Engine by the E10A emulator. Select Build from the Build menu. Figure 3.24 shows the screen for selecting Build.

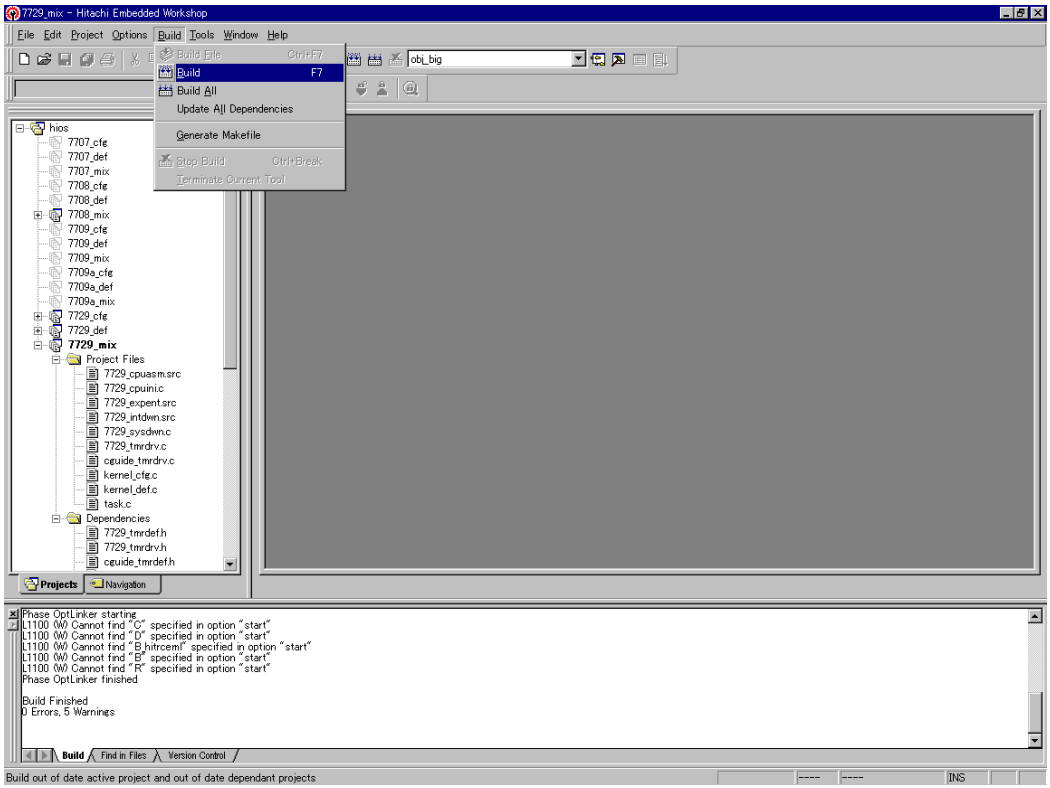


Figure 3.24 Selecting Build

The executable file is created by selecting Build. The result of compilation and linkage is shown at the bottom of the window. If a compile error occurs, correct the applicable source and build the file again. The executable file (with the file extension .abs) is created in the install folder “obj_big”.

Now you can download the file to the Solution Engine by the E10A emulator and execute it. For details about how to download and execute the file, see section 4, Downloading and Executing Application Programs.

3.9 Disabling Parameter Check Function

When debugging the application programs completes and they are ready to be installed into the product, you can disable the parameter check function. This check function is an unnecessary routine performed in the beginning of the service call, in the HI series operating system.

You can use the configurator to disable the parameter check function. Figure 3.25 shows the screen for disabling the parameter check function.

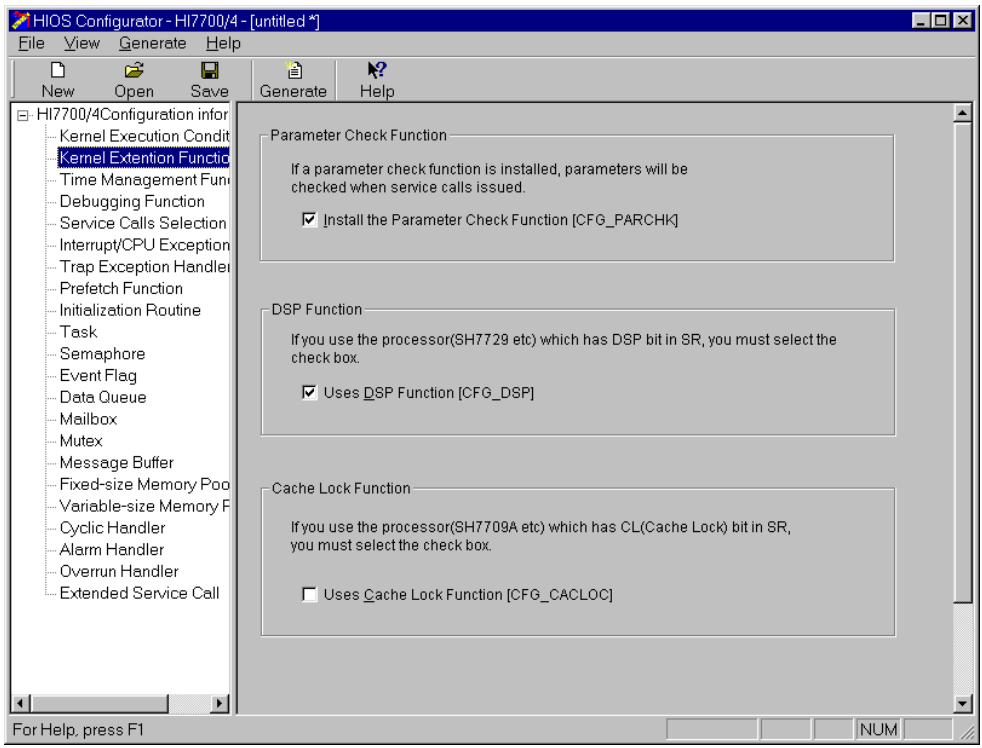


Figure 3.25 Disabling Parameter Check Function

Click Kernel Extended Function on the Configurator Startup screen to view the screen in figure 3.25. Uncheck the Install the Parameter Check Function checkbox and create and build the configuration files. The executable file with the parameter check function disabled is created.

Section 4 Downloading and Executing Application Programs

This section describes how to use the E10A to download the executable file created in section 3, Configuration, and run it on the Solution Engine.

4.1 Initializing Solution Engine

The ROM monitor supplied with the Solution Engine initializes the CPU. In this guide, this monitor is used for the CPU initialization. (When using another board, you must use a specific CPU initialization routine. For details of CPU initialization, see section 2.1, Creating CPU Initialization Routine.)

Configure the system as shown in figure1.1 in section 1, Overview. Start the host computer, turn the Solution Engine on, select HDI for E10A SH7729 from the Windows Start menu to start the HDI. Figure 4.1 shows the HDI Startup screen.

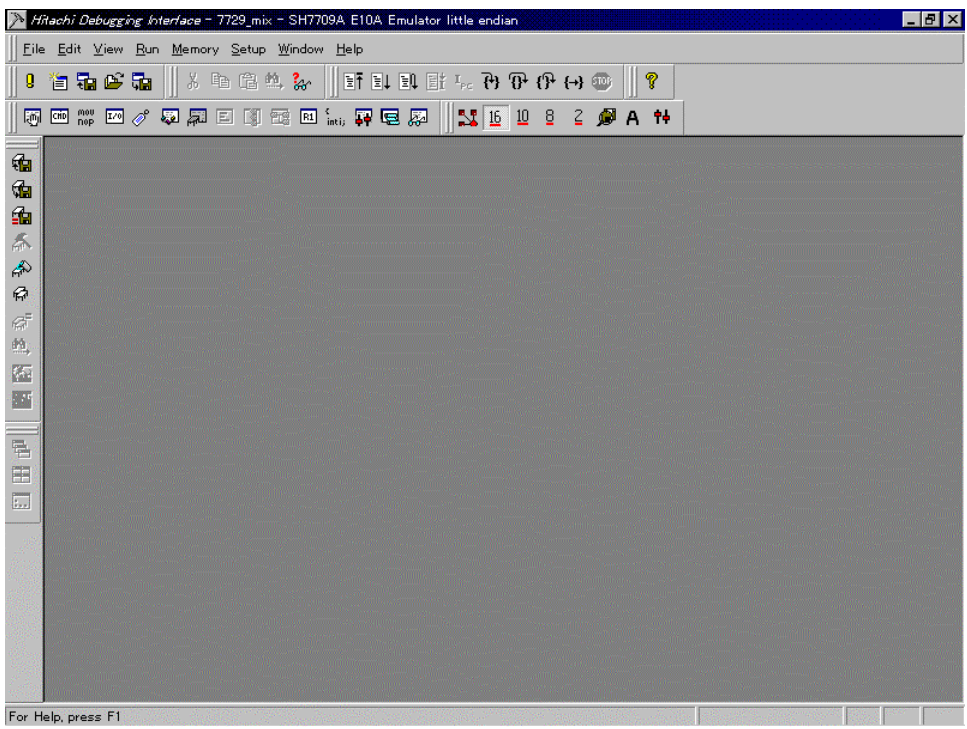


Figure 4.1 HDI Startup Screen

Then, choose Go from the Run menu (figure 4.2).

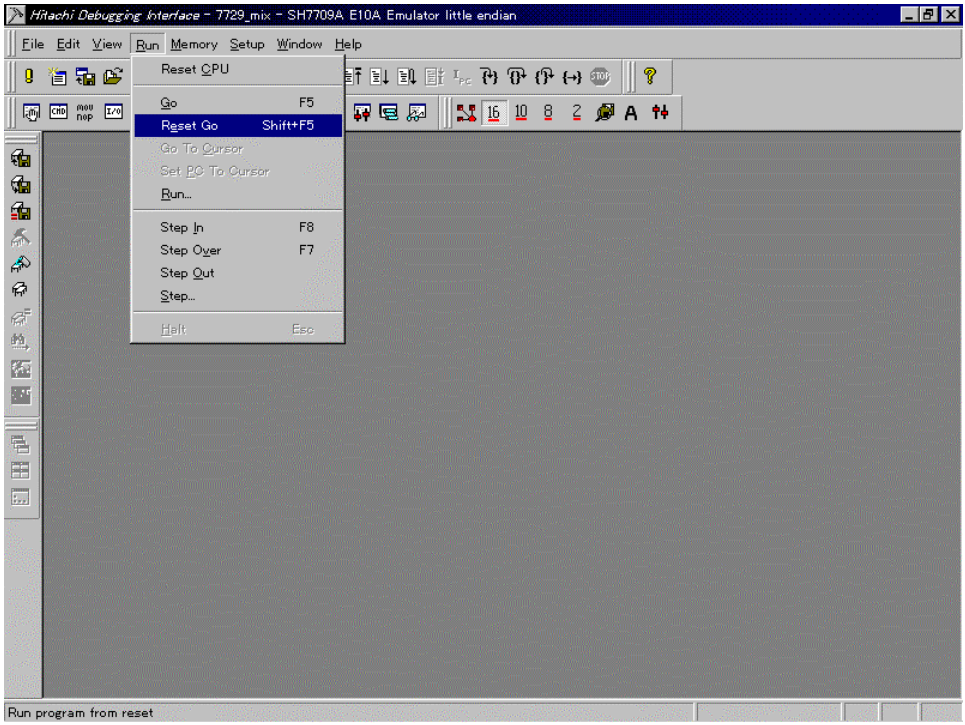


Figure 4.2 Reset Go menu

After one or two seconds, click the STOP button (red) on the menu bar. Now, initializing the Solution Engine completes and this allows reading from or writing to the SDRAM supplied with the Solution Engine.

4.2 Downloading Application Program

Download the executable file created in section 3, Configuration, to the E10A.

Figure 4.3 shows the screen for downloading the executable file.

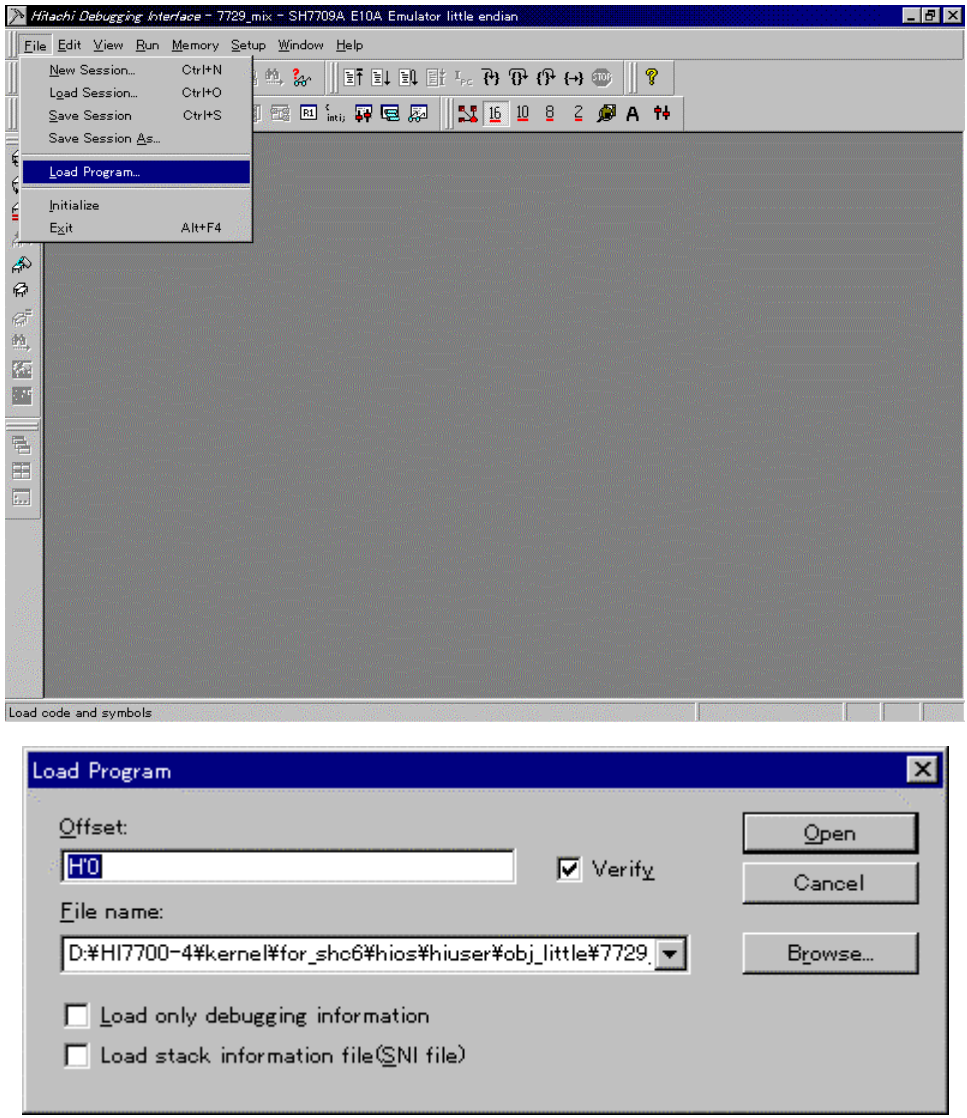


Figure 4.3 Downloading Executable File

Select Load Program... from the File menu on the HDI Startup screen. On the Load Program screen in figure 4.3, enter the name of the executable file to download in the File Name box and

click the Open button to download it. The executable file is 7729_mix.abs in the install folder “obj_big”.

After downloading succeeds, the Complete Download screen in figure 4.4 appears.

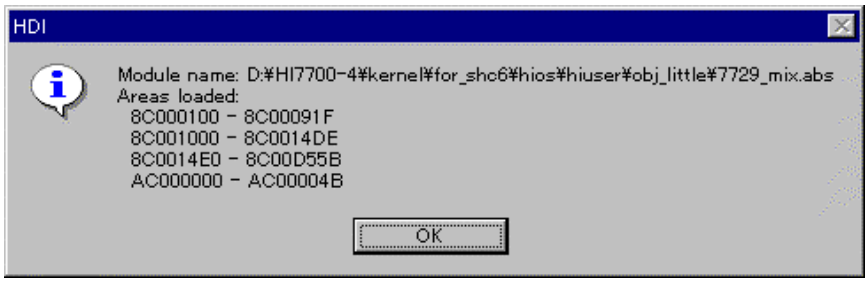


Figure 4.4 Complete Download Screen

Click the OK button on the Complete Download screen.

4.3 Executing Application Program

To execute the program, choose Registers from the View menu on the HDI Startup screen to view the register information (figure 4.5).

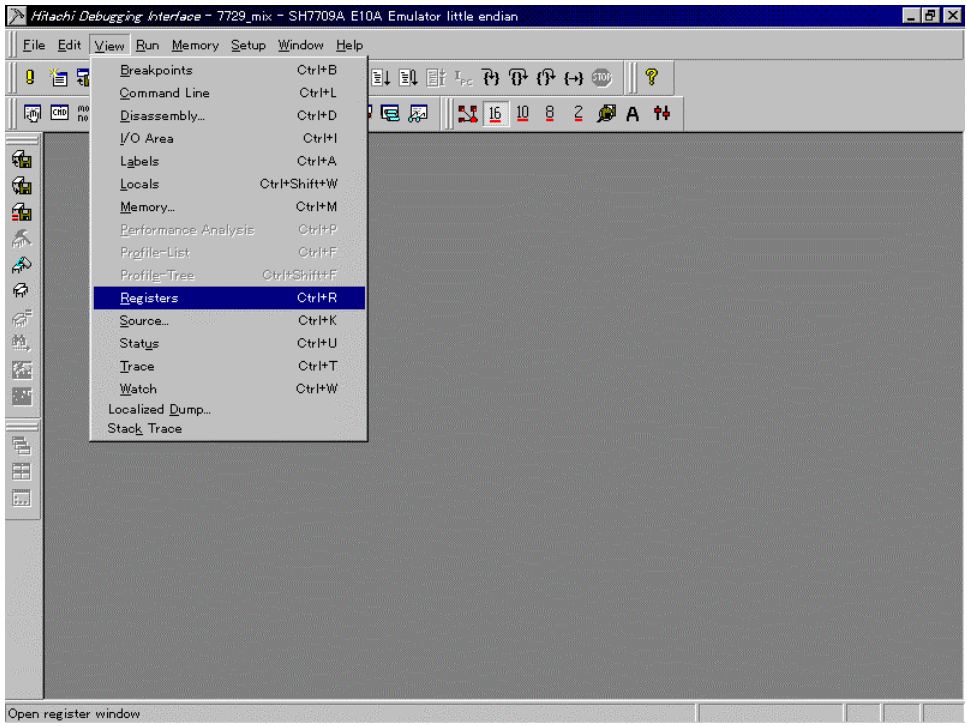


Figure 4.5 Register Information

Then, change the PC value. Double click the PC value on the Register Information screen to view the Change PC Value screen (figure 4.6).

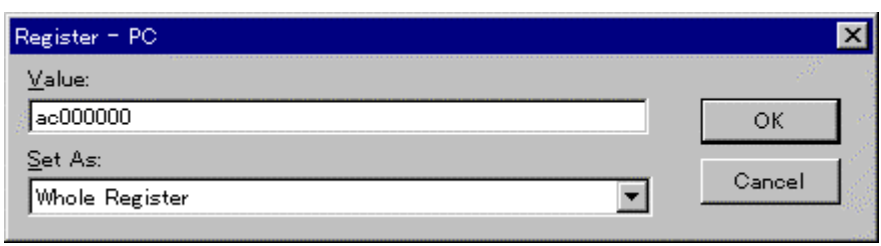


Figure 4.6 Change PC Value Screen

Change the PC value to AC000000 as shown in figure 4.6 and click the OK button. This value is the start address of the CPU initialization routine.

Now, you can execute the program. Select Go from the Run menu to execute the program (figure 4.7).

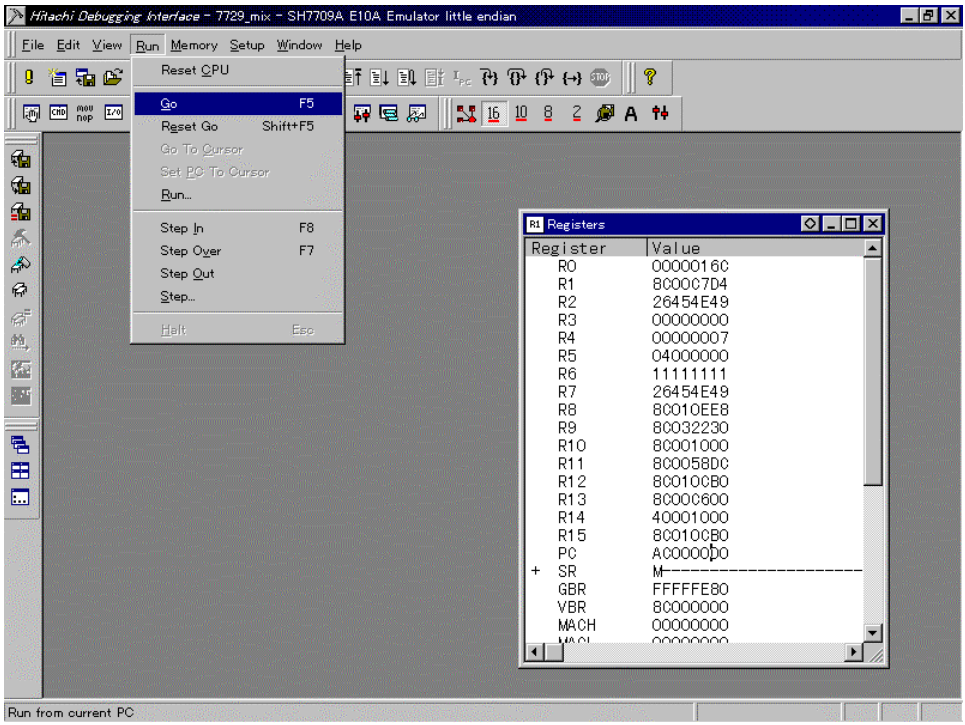


Figure 4.7 Execute Program Screen

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