IDT71V656xx and IDT71V658xx Device Errata 256K x 36 and 512K x 18 3.3V Synchronous ZBT™ SRAMs

Notes

Supplemental Information

This Device Errata reflects Z versions of silicon involving IDT71V656xx and IDT71V658xx, 9M ZBT family devices and supplements information found in the documentation for these devices. Silicon revisions can be identified as follows:

Z is revision 1.0

Revision History

July 28, 2000: First version of device errata for Revision 1.0 silicon

Descriptions and Workarounds

Item #1: - JTAG Functionality and Associated Pins

Issue: The JTAG circuitry does not function on the current version of silicon. The goal of JTAG in these memory devices is to provide the ability to perform boundary scan. The goal of boundary scan is to have the ability at board level to test and ensure that all pins of the device are properly connected.

All items referent to this function have been removed from the datasheet. These include:

The inoperative TMS, TDI, TDO and TCK functions on the following pins and respective packages:

- *Pins 38, 39, 42, and 43 on 100 pin thin quad plastic flatpack (TQFP)*
- *Pins U2, U3, U4, and U5 on 119 ball grid array (BGA)*
- *Pins P5, R5, P7, and R7 on 165 fine pitch ball grid array (fBGA)*

Workaround: These JTAG pins are currently not bonded to the die. Without harm to the function of these memory devices, the JTAG pins can be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).

Fix: - The JTAG circuitry will be functional on the next revision of silicon, scheduled for release in Quarter 02, 2002.

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