79RC64574/RC64575 Document Errata

Notes

Supplemental Information

This Document Errata reflects all changes made to the October 1999 version of the *IDT79RC64574/RC64575 User Reference Manual,* Version 1.0 and the data sheet for this device.

Revision History

November 30, 1999: First version of documentation errata for this device.

March 1, 2000: Added Item #2.

March 16, 2000: Added Item #3.

April 13, 2000: Added Item #4.

Errata Items

Item #1 - Changes to Figure 12.4 on page 12-3.

Issue: Figure 12.4 on page 12-3 of the manual includes two "R" labels in the PLL Circuit which could be interpreted as a requirement to include two resistors. No resistors are required in this circuit.

Item #2 - Change to Imp field in PRId register.

Issue: The value in the Imp field of the PRId register on page 5-7 of the manual is incorrectly given as 0x23. The correct value is 0x15.

Item #3 - Change to bulleted list on page 12-8.

Issue: The bulleted list directly above Table 12.2 incorrectly states that bits 15 to 255 are reserved bits. However, bits 15 to 26 are used in initialization of the CPU. Bits 27 to 256 are reserved bits.

Item #4 - Change to Config Register (16) section on page 5-7.

Issue: The third sentence in the first paragraph should read as follows: Other configuration options are read/write (as indicated by Config register bits 2:0) and controlled by software; on Reset, this field is undefined.

Add the following descriptions for BE and IC to Table 5.7.

Field	Description
BE	Big Endian Mode 0 → Little Endian 1 → Big Endian
IC	Primary I-cache size (I-cache size = 2^{12+IC} bytes). In the RC64574/64575 processor, this is set to 32Kbytes (DE=3).

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