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Errata Notification

EN #: SMEN-01-03 Errata Revision #: 00

Issue Date: July 23, 2001 Effective Date: July 23, 2001

Product Affected: 70V659, 70V658, 70V657, 70V631 and 70V639

ERRATA DETAILS: **ATTACHMENT** ☐ Yes ■ No

■ Data Sheet Errata — $\overline{BUSY}$ Timing Parameters t_{BDA}, t_{BAC}, t_{BDC} and t_{BDD} not correct on Datasheets

☐ Device Manual Errata

☐ Application Notes Errata

☐ Other (Please Specify)

Changed $\overline{BUSY}$ Timing Parameters t_{BDA}, t_{BAC}, t_{BDC} and t_{BDD} to match t_{BAA} ($\overline{BUSY}$ Access Time from Address Match) of each Speed Grade. (See $\overline{BUSY}$ AC Electrical Characteristics Table)

Symbol	Parameter	Min.	Max.	Units
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	--	10, 12, 15	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	--	10, 12, 15	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	--	10, 12, 15	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data	--	10, 12, 15	ns

IDT Web Site Location: http://www.idt.com/products/pages/Multi-Ports.html

CUSTOMER NOTIFICATION:

As a result of Errata listed above, IDT has decided to notify you through this Errata Notification.
We recommend you to review this notification in details prior to the use of affected product in your application.
Please use acknowledgement below or E-Mail to request additional information.

If you have any questions, please feel free to contact your local IDT distributor or sales representative.

Customer: _____ E-Mail Address: _____

Name/Date: _____ Phone #: _____

Title: _____ Fax # : _____

CUSTOMER COMMENTS: _____