NEC

Data Sheet

V850ES/FK3

32-bit Single-Chip Microcontroller

Hardware

μPD70F3383(A) **μPD70F3384(A)** **μPD70F3385(A)**
μPD70F3383(A1) **μPD70F3384(A1)** **μPD70F3385(A1)**
μPD70F3383(A2) **μPD70F3384(A2)** **μPD70F3385(A2)**

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Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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1. Pin Group Information

1.1 Device package information

The V850ES/Fx3 device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
μPD70F3370A μPD70F3371	64	FE3
μPD70F3372 μPD70F3373	80	FF3
μPD70F3374 μPD70F3375 μPD70F3376A μPD70F3377A	100	FG3
μPD70F3378 μPD70F3379 μPD70F3380 μPD70F3381 μPD70F3382	144	FJ3
μPD70F3383 μPD70F3384 μPD70F3385	176	FK3

This document describes the specification for the V850ES/FK3.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915 (FJ3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915, P156-157 (FK3)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912 (FJ3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912, P150-155 (FK3)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3)

2D: (SHMT3)
- PDL0-7 (FE3)
- PDL0-11 (FF3)

1.4 Pin Groups 3x: Pins supplied by BVDD

3A: (CMOS)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FG3)
- PCD0-3, PCM0-5, PCS0-7, PCT0-7 (FJ3) + (FK3)

3D: (SHMT3)
- PDL0-13 (FG3)
- PDL0-15 (FJ3) + (FK3)

1.5 Pin Groups 4: Pins supplied by AVREF0

4: (CMOS)
- P70-79 (FE3)
- P70-711 (FF3)
- P70-715 (FG3)
- P70-715, P120-127 (FJ3) + (FK3)

1.6 Pin Groups 5: Pins supplied by AVREF1

- P20-P215 (FK3) (CMOS)

1.7 Pin Groups 6: Pins supplied by EVDD

- RESET (SHMT2)
- IC, FLMD0

1.8 Pin Groups 7: Pins supplied by VRO

- X1, X2, XT1, XT2

2. Electrical Specifications of (A)-Grade

This product has to be used only under the conditions of VDD = VDD1 = EVDD = BVDD. Operation is not ensured at the time of using this product except this condition.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	VDD	VDD = VDD1 = EVDD = BVDD,		-0.5 to +6.5	V
	VDD1	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	EVDD	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	BVDD	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	AVREF0			-0.5 to +6.5	V
	AVREF1			-0.5 to +6.5	V
	VSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	VSS1	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	EVSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	BVSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS11		-0.5 to +0.5	V
	AVSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS11		-0.5 to +0.5	V
	AVSS1	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
Input voltage	VI1	Pin Group 1x, 6		-0.5 to EVDD+0.5 Note1	V
	VI2	Pin Group 3x		-0.5 to BVDD+0.5 Note1	V
	VI3	Pin Group 7		-0.5 to VRO+0.5 Note1	V
Analog input voltage	VIAN	Pin Group 4		-0.5 to AVREF0+0.5 Note1	V
		Pin Group 5		-0.5 to AVREF1+0.5 Note1	V
High level output current	IOH	Pin Group 1x	1 pin	-4	mA
			Total	-50	mA
		Pin Group 3x	1 pin	-4	mA
			Total	-50	mA
		Pin Group 4	1 pin	-4	mA
			Total	-20 Note2	mA
		Pin Group 5	1 pin	-4	mA
			Total	-20 Note2	mA
Low level output current	IOL	Pin Group 1x	1 pin	4	mA
			Total	50	mA
		Pin Group 3x	1 pin	4	mA
			Total	50	mA
		Pin Group 4	1 pin	4	mA
			Total	20 Note2	mA
		Pin Group 5	1 pin	4	mA
			Total	20 Note2	mA
Operating ambient temperature	Ta	Normal operating mode		-40 to +85	°C
		Flash programming mode		-40 to +85	
Storage temperature	Tstg			-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 / IAREF1 current.

2.2 Capacities

(Ta = 25°C, VDD = VDD1 = EVDD = BVDD = AVREF0 = AVREF1 = VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input/output capacitance	CIO	f=1MHz, Not measured pins is 0V.			10	pF

2.3 Operating condition

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, C = 4.7uF))

Internal System clock frequency (f_{VBCLK})	Supply voltage (VDD)	Operating Condition

$4.0 \le f_{xx} \le 48$MHz Note1	4.0V≤VDD≤5.5V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • $f_{XP1} \le 32$MHz
		  • $f_{XP2} \le 32$MHz
		• AC characteristics:
		  • Refer to chapter '2.7 AC Characteristics' for details.

	3.5V≤VDD≤4.0V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • $f_{XP1} \le 20$MHz
		  • $f_{XP2} \le 20$MHz
		• AC characteristics:
		  • Refer to chapter '2.7 AC Characteristics' for details.

	3.3V≤VDD<3.5V Note2	Only operation of following function is assured: • CPU • Flash (include programming) • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI

	3.5V≤AVREF0<5.5V	• A/D Converter
		  • Refer to chapter '2.8 A/D Converter' for details.
		  • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0)

	3.5V≤AVREF1<5.5V	• A/D Converter
		  • Refer to chapter '2.8 A/D Converter' for details.
		  • stop ADC for AVREF1 < 4.0V (ADA1CE bit =0)

32kHz≤f_{XT}≤35kHz (Crystal)	3.3V≤VDD<5.5V Note2	-
12.5kHz≤f_{XT}≤27.5kHz Note3 (RC)		
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note2	-

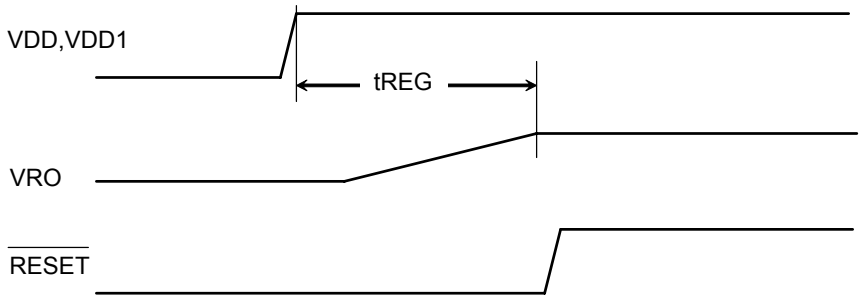
Notes: 1. For using SSCG please refer to '2.5.5 SSCG Characteristics' for details
2. VDD = VDD1 = EVDD = BVDD
3. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.4 Voltage Regulator Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	VDD		3.5		5.5	V
	VDD1	Limited function see '2.3 Operating condition'	3.3			V
Output voltage	VRO			2.5		V
Output voltage stabilization time	t_{REG} Note	After VDD=VDD1 reaches voltage range min. 3.3V To connect C=4.7uF on REGC terminal and C=4.7uF on REGC1 terminal			1	ms

Note: In case of non-POC device, be sure to start VDD in the state of $\overline{\text{RESET}}$=VSS=0V. For POC devices there is no need to control external $\overline{\text{RESET}}$ terminal. For decives with POC function the internal $\overline{\text{RESET}}$ signal will automatically controlled until VRO is stable.



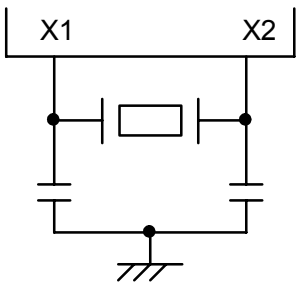
2.5 Clock Generator Circuit

2.5.1 Main System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, C = 4.7uF)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal / Ceramic resonator	Refer to figure below	Oscillator frequency (fx) Note1		4		16	MHz
		Oscillation stabilization time Note2	After STOP mode	64 Note4	Note3		µs
			After IDLE2 mode	54 Note4	Note3		µs

Notes: 1. Indicates only oscillation circuit characteristics. Refer to '2.7 AC Characteristics' for CPU operation clock.
2. Time required to stabilize oscillation after VDD reaches oscillator voltage range MIN. 3.3V
3. Depends on the setting of the oscillation stabilization time select register (OSTS)
4. Minimum time required to stabilize flash. Time has to be secured by setting the oscillation stabilization time select register (OSTS)



2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

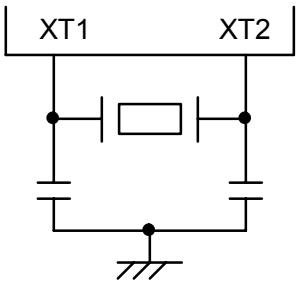
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Refer to Figure 1	Oscillator frequency (fxt)Note1		32	32.768	35	kHz
		Oscillation stabilization time Note2				10	s
RC resonator	Refer to Figure 2	Oscillator frequencyNote1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	μs

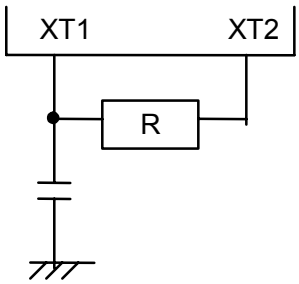
Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided 2 internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 =0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_{RL}	240kHz Internal-OSC	204	240	276	kHz
	f_{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation stabilization time		240kHz Internal-OSC		10	36	μs
		8MHz Internal-OSC	51	92	256	μs

2.5.4 PLL Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note1	3		6	MHz
Output frequency	fxx		12		48	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

2.5.5 SSCG Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	f_{XX}		12		48	MHz
Lock time	t_{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector SFC1[6:4]	Percent modulation		Maximum average operating frequency		Unit
	TYP	MAX		≥384KB product	
000B	± 0.5%	± 2.0%		47.0	MHz
001B	± 1.0%	± 2.5%		46.8	
010B	± 2.0%	± 4.0%		46.1	
011B	± 3.0%	± 6.0%		45.1	
100B	± 4.0%	± 8.0%		44.2	
101B	± 5.0%	± 10.0%		43.2	

2.6 DC Characteristics

2.6.1 Input/Output Level

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Sym-bol	Conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH1	Pin Group 1B		0.7·EVDD		EVDD	V
	VIH2	Pin Group 1D		0.8·EVDD		EVDD	V
		Pin Group 3D		0.8·BVDD		BVDD	V
	VIH3	Pin Group 3A		0.7·BVDD		BVDD	V
	VIH4	Pin Group 4		0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
	VIH6	Pin Group 5		0.7·AVREF1		AVREF1	V
Low level input voltage	VIL1	Pin Group 1B		EVSS		0.3·EVDD	V
	VIL2	Pin Group 1D		EVSS		0.4·EVDD	V
		Pin Group 3D		BVSS		0.4·BVDD	V
	VIL3	Pin Group 3A		BVSS		0.3·BVDD	V
	VIL4	Pin Group 4		AVSS		0.3·AVREF0	V
	VIL5	Pin Group 6		EVSS		0.2·EVDD	V
	VIL6	Pin Group 5		AVSS1		0.3·AVREF1	V
Input hysteresis	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
	VHYS2	Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
		Pin Group 3D	Center point at 0.6 x BVDD Note3		0.192 x BVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High level output voltage Note2	VOH1	Pin Group 1x	IOH=-1.0mA	EVDD-1.0		EVDD	V
			IOH=-100uA	EVDD-0.5		EVDD	V
	VOH2	Pin Group 3x	IOH=-1.0mA	BVDD-1.0		BVDD	
			IOH=-100uA	BVDD-0.5		BVDD	V
	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
			IOH=-100uA	AVREF0-0.5		AVREF0	V
	VOH4	Pin Group 5	IOH=-1.0mA	AVREF1-1.0		AVREF1	V
			IOH=-100uA	AVREF1-0.5		AVREF1	V
Low level output voltage Note2	VOL1	Pin Group 1x	IOL=1.0mA	0		0.4	V
		P914, 915	IOL=3.0mA				
	VOL2	Pin Group 3x	IOL=1.0mA	0		0.4	V
	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
	VOL4	Pin Group 5	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	VI=0V		10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI=VDD		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)

2. Total IOH/IOL max is 20mA/-20mA each power supply line (EVDD,BVDD,AVREF0 and AVREF1).
AVREF0/AVREF1 IOH/IOL current is excluding ADC current IAREF0/IAREF1.

3. Typical value. Not tested and guaranteed

2.6.2 PIN leakage current

(Ta =-40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V,VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Symbol	Conditions	MIN.		TYP.	MAX.	Unit
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.2	uA
			Other pins Note1			0.5	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.2	
			Other pins Note1			-0.5	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.2	
			Other pins			0.5	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.2	
			Other pins			-0.5	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current : 2.0uA
Low level input leakage current : -2.0uA

2.6.3 Power supply current (A-grade)

2.6.3.1 µPD70F3383 / µPD70F3384 / µPD70F3385

(a) Absolute values

(Ta = -40 to +85°C,
VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V Note1)

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	35	47	mA
					f_{xx}=32MHz f_X=16MHz	52	68	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	17	24	mA
					f_{xx}=16MHz f_X=16MHz	29	38	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	63	81	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	28		mA
					f_{xx}=32MHz f_X=16MHz	41		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	15		mA
					f_{xx}=16MHz f_X=16MHz	23		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	54		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	24	34	mA
					f_{xx}=32MHz f_X=16MHz	36	51	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	10	16	mA
					f_{xx}=16MHz f_X=16MHz	18	26	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	40	54	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	16		mA
					f_{xx}=32MHz f_X=16MHz	24		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	8		mA
					f_{xx}=16MHz f_X=16MHz	12		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	30		mA

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	2.6	3.3	mA
				f_{xx}=12MHz f_x=12MHz	4.1	5.3	mA
				f_{xx}=16MHz f_x=16MHz	4.9	6.5	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		3.0	3.9	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4		mA
				f_{xx}=12MHz f_x=12MHz	1.8		mA
				f_{xx}=16MHz f_x=16MHz	2.0		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.3		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	0.7	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.0	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.2	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.5	mA
SUB operating mode Note5	IDD5	Crystal resonator (fxt = 32,768kHz)			90	400	μA
		RC resonator (fxt=20kHz) Note6			90	400	μA
		240 kHz Internal-OSC (SubOSC stopped)			330	1310	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	μA
		RC resonator (fxt=20kHz) Note6			40	220	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	100	μA
			240kHz Internal-OSC working		15.5	115	μA
		POC work	240kHz Internal-OSC stop		10.5	105	μA
			240kHz Internal-OSC working		18.5	120	μA

(b) Calculation formulas

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V) Note1)

Mode	Symbol	Condition			TYP. Note9	MAX. Note9	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{XX} PRSI option: 0	PLL: ON 12MHz≤f_{XX}≤32MHz	1.39·f_{XX}+7.5	1.67·f_{XX}+14.0	mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	1.44·f_{XX}+5.5	1.73·f_{XX}+10.6	mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 12MHz≤f_{XX}≤48MHz	1.17·f_{XX}+6.9	1.41·f_{XX}+13.3	mA
		All peripherals stopped	Peripheral: ff_{XX-} PRSI option: 0	PLL: ON 12MHz≤f_{XX}≤32MHz	1.06·f_{XX}+7.2		mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	1.00·f_{XX}+7.0		mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 12MHz≤f_{XX}≤48MHz	0.96·f_{XX}+7.8		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: ff_{XX-} PRSI option: 0	PLL: ON 16MHz≤f_{XX}≤32MHz	1.00·f_{XX}+4.0	1.40*f_{XX}+6.4	mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	0.94·f_{XX}+2.7	1.27*f_{XX}+5.4	mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 16MHz≤f_{XX}≤48MHz	0.75·f_{XX}+4.0	0.94*f_{XX}+9.0	mA
		All peripherals stopped	Peripheral: f_{XX} PRSI option: 0	PLL: ON 16MHz≤f_{XX}≤32MHz	0.65·f_{XX}+3.4		mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	0.59·f_{XX}+2.8		mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 16MHz≤f_{XX}≤48MHz	0.54·f_{XX}+4.4		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{XX}≤16MHz Note7	0.211·f_{XX}+1.54	0.295·f_{XX}+ 1.80	mA
		All peripherals stopped			0.054·f_{XX}+1.15		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{XX}≤16MHz Note7			0.037·f_{XX}+0.21	0.049·f_{XX}+ 0.43	mA

Notes: 1. VDD, VDD1, EVDD and BVDD total current. (Ports are stopped).
AVREF0 and AVREF1 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

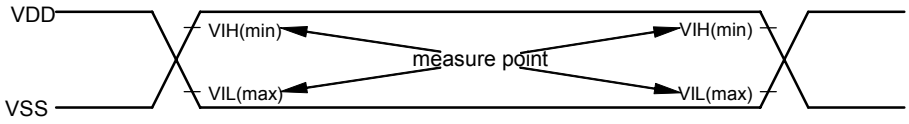
2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or EEPROM emulation mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 14-(0.33*fxx/2+0.1)*2 [mA]
  + In case of PLL ON: 14-(0.18*fxx/2+3.0)*2 [mA]
- EEPROM emulation mode:
  + 7-(0.18*fxx/4+3.0) [mA]

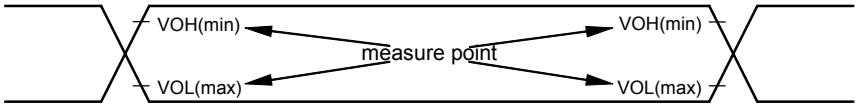
3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{XX} are tested in the outgoing device inspection.

2.7 AC Characteristics

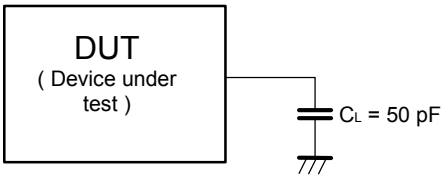
AC test Input measurement points (VDD, AVREF0,AVREF1, EVDD, BVDD)



AC test output measurement points



Load conditions



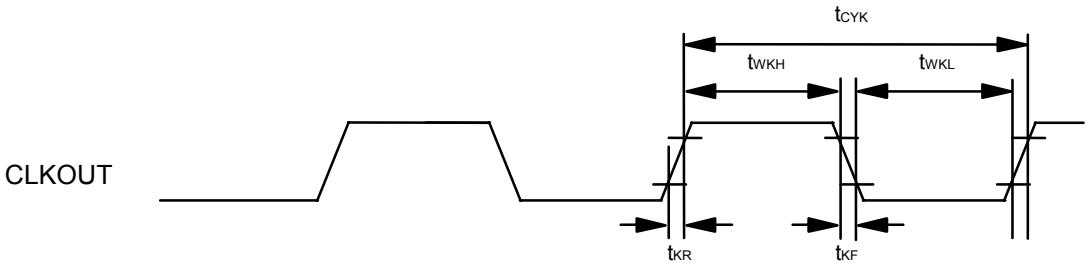
Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

2.7.1 CLKOUT Output Timing

(Ta =-40 to +85°C,
VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	tCYK	VDD = VDD1 = EVDD = BVDD = 4.0V ~ 5.5V	31.25ns	80μs	
		VDD = VDD1 = EVDD = BVDD = 3.5V ~ 5.5V	50ns		
High level width	tWKH	VDD = VDD1 = EVDD = BVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = VDD1 = EVDD = BVDD = 3.5V ~ 5.5V	tCYK/2-15		
Low level width	tWKL	VDD = VDD1 = EVDD = BVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = VDD1 = EVDD = BVDD = 3.5V ~ 5.5V	tCYK/2-15		
Rise time	tKR	VDD = VDD1 = EVDD = BVDD = 4.0V ~ 5.5V		13	ns
		VDD = VDD1 = EVDD = BVDD = 3.5V ~ 5.5V		15	
Fall time	tKF	VDD = VDD1 = EVDD = BVDD = 4.0V ~ 5.5V		13	ns
		VDD = VDD1 = EVDD = BVDD = 3.5V ~ 5.5V		15	

CLKOUT output timing



2.7.2 Bus Timing (Multiplexed bus mode)

(a) CLKOUT asynchronous: In multiplexed bus mode

(Ta = -40 to +85°C,
3.5V ≤ VDD = VDD1 = EVDD = BVDD < 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	tSAST	<14>		$(0.5+t_{ASW})$T-20		ns
Address hold time (from ASTB↓)	tHSTA	<15>		$(0.5+t_{AHW})$T-15		ns
Delay time from _RD↓ to address float	tFRDA	<16>			16	ns
Data Input setup time from address	tSAID	<17>			$(2+n+t_{ASW}+t_{AHW})$T-40	ns
Data Input setup time from _RD↓	tSRDID	<18>			(1+n)T-34	ns
Delay time from ASTB↓ to _RD↓, _WRm↓	tDSTRDWR	<19>		$(0.5+t_{AHW})$T-15		ns
Data Input hold time (from _RD↑)	tHRDID	<20>		0		ns
Address output time from _RD↑	tDRDA	<21>		$(1+i+t_{AHW})$T-15		ns
Delay time from _RD↑, _WRm↑ to ASTB↑	tDRDWRST	<22>		0.5T-15		ns
Delay time from _RD↑ to ASTB↓	tDRDST	<23>		$(1.5+i+t_{AHW})$T-15		ns
_RD, _WRn low level width	tWRDWRL	<24>		(1+n)T-20		ns
ASTB high level width	tWSTH	<25>		$(1+i+t_{ASW})$T-15		ns
Data output time from _WRm↓	tDWROD	<26>			15	ns
Data output setup time (to _WRm↑)	tSODWR	<27>		(1+n)T-25		ns
Data output hold time (from _WRm↑)	tHWROD	<28>		T-15		ns
_WAIT setup time (to address)	tSAWT1	<29>	n≥1		$(1.5+t_{ASW+}t_{AHW})$T-45	ns
	tSAWT2	<30>			$(1.5+n+t_{ASW+}t_{AHW})$T-45	ns
_WAIT hold time (from address)	tHAWT1	<31>	n≥1	$(0.5+n+t_{ASW+}t_{AHW})$T		ns
	tHAWT2	<32>		$(1.5+n+t_{ASW+}t_{AHW})$T		ns
_WAIT setup time (to ASTB↓)	tSSTWT1	<33>	n≥1		$(1+t_{AHW})$T-35	ns
	tSSTWT2	<34>			$(1+n+t_{AHW})$T-35	ns
_WAIT hold time (from ASTB↓)	tHSTWT1	<35>	n≥1	$(n+t_{AHW})$T		ns
	tHSTWT2	<36>		$(1+n+t_{AHW})$T		ns
_HLDRQ high level width	tWHQH	<37>		T+10		ns
_HLDAK low level width	tWHAL	<38>		T-20		ns
Delay time from _HLDAK↑ to bus output	tDHAC	<40>		-3		ns
Delay time from _HLDRQ↓ to _HLDAK↓	tDHQHA1	<41>			(2n+7.5)T+25	ns
Delay time from _HLDRQ↑ to _HLDAK↑	tDHQHA2	<42>		0.5T	1.5T+35	ns

(b) CLKOUT synchronous: In multiplexed bus mode

(Ta = -40 to +85°C,
3.5V ≤ VDD = VDD1 = EVDD = BVDD < 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	tDKA	<43>		0	24	ns
Delay time from CLKOUT↑ to address float	tFKA	<44>		0	24	ns
Delay time from CLKOUT↓ to ASTB	tDKST	<45>		-7	18	ns
Delay time fromCLKOUT↑ to _RD, _WRm	tDKRDWR	<46>		-2	18	ns
Data Input setup time (from CLKOUT↑)	tSIDK	<47>		20		ns
Data Input hold time (from CLKOUT↑)	tHKID	<48>		5		ns
Data output delay time (from CLKOUT↑)	tDKOD	<49>			27	ns
_WAIT setup time (to CLKOUT↓)	tSWTK	<50>		30		ns
_WAIT hold time (from CLKOUT↓)	tHKWT	<51>		5		ns
HLDRQ setup time (to CLKOUT↓)	tSHQK	<52>		30		ns
_HLDRQ hold time (from CLKOUT↓)	tHKHQ	<53>		5		ns
Delay time from CLKOUT↑ to _HLDAK	tDKHA	<54>			24	ns
Delay time from CLKOUT↑ to address float	tDKF	<55>			25	ns

Remarks: 1. T=1/fcpu (fcpu: CPU operation clock frequency)

2. n: Number of wait clocks Inserted In the bus cycle.
The sampling timing changes when a programmable wait is Inserted.

3. i: Number of Idle states Inserted after the read cycle (0 or 1).

4. The values In the above specifications are values for when clocks with a 1: 1 duty ratio are Input from X1

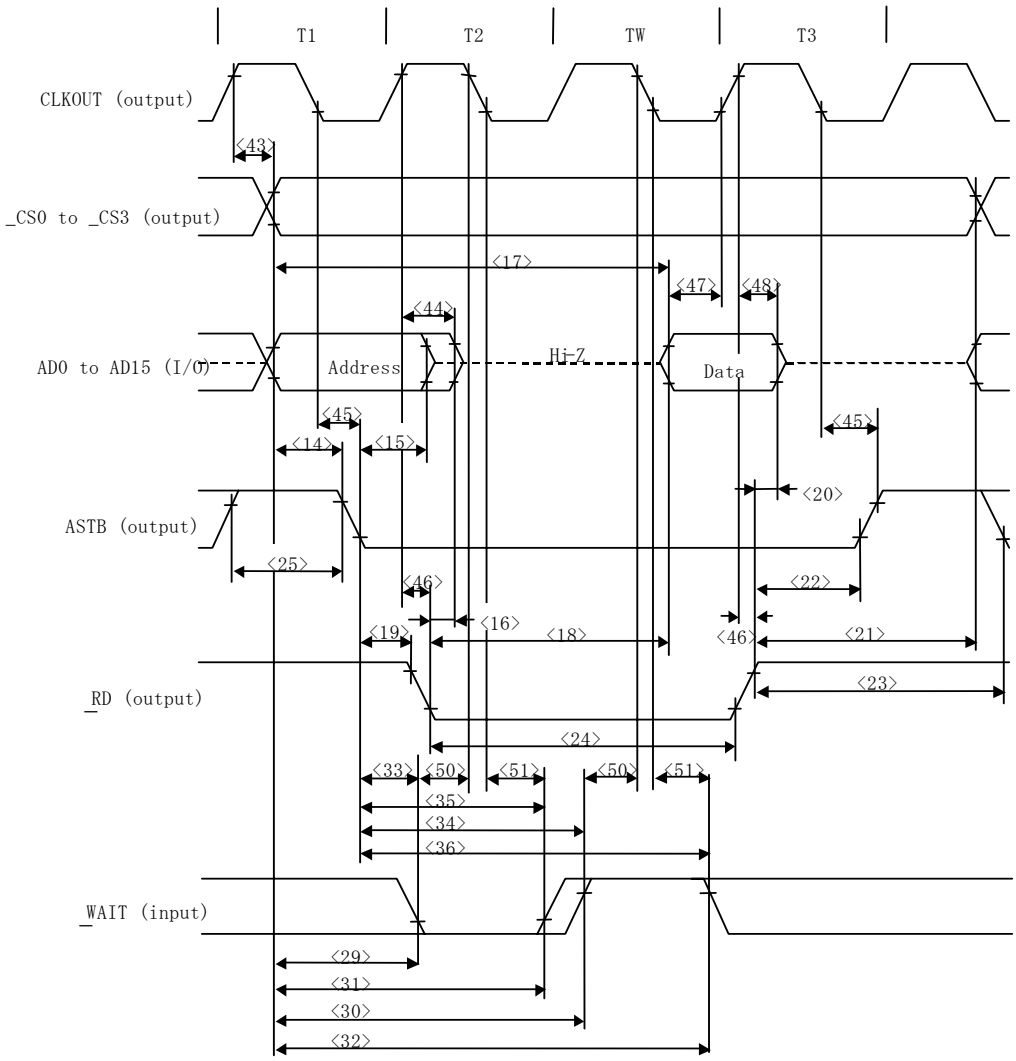
5. m=0,1

6. t_{ASW}=Number of address setup wait clocks (0 or 1)
t_{AHW}=Number of address hold wait clocks (0 or 1)

7. When the operation frequency is high, it is not possible to access by no wait bus cycle. Please insert wait clock (data wait (n)) / address setup wait (tASW) / address hold wait (tAHW)).
Example: Set the following in accordance to the CPU operating clock frequency (k=0 to 3).

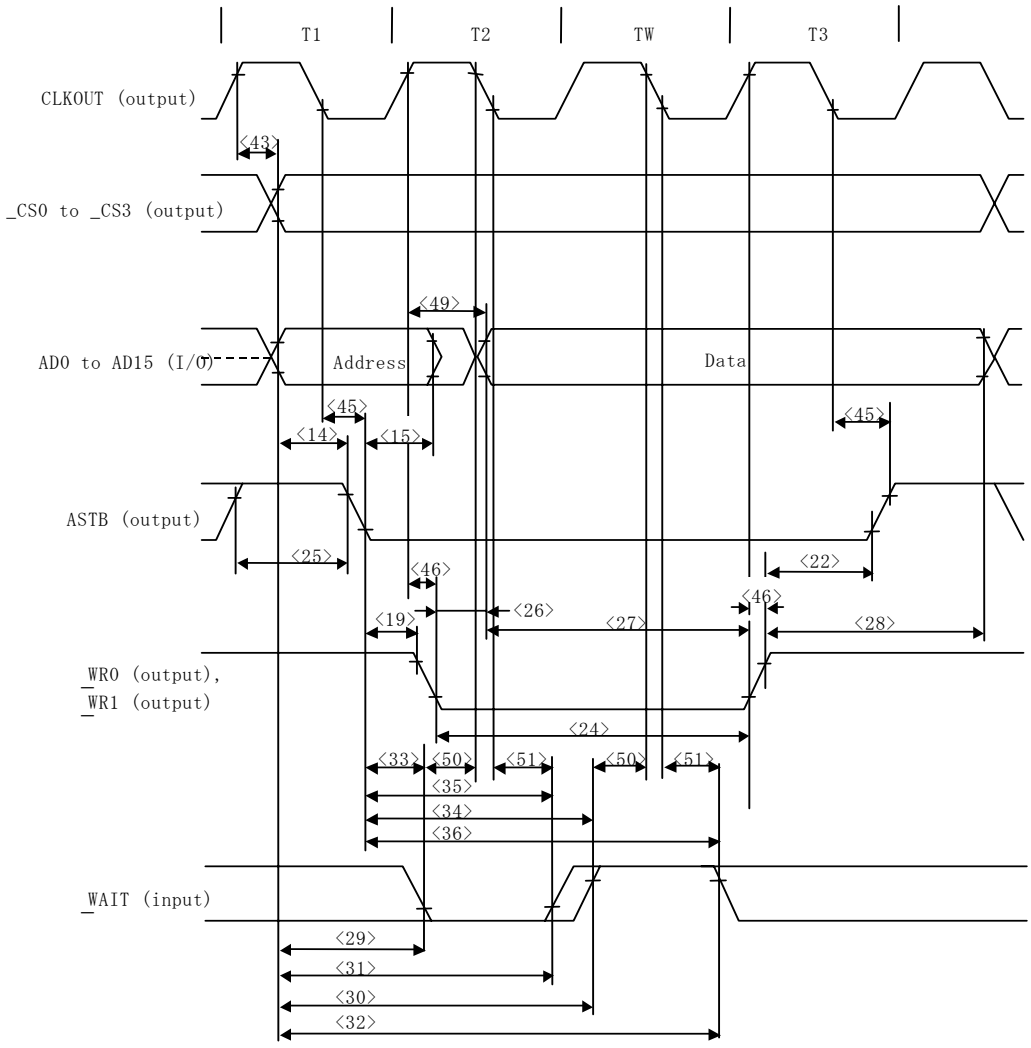
- 30ns≤1/fcpu<40ns: Set address setup wait (AWC.ASWk bit=1).
- 20.8ns≤1/fcpu<30ns: Set address setup wait (AWC.ASWk bit=1) and address hold wait (AWC.AHWk bit=1).
- 20.8ns≤1/fcpu≤25ns: Set a data wait (minimum 1 wait)

Read Cycle (CLKOUT Synchronous/ Asynchronous, 1 Wait): In Multiplexed Bus Mode



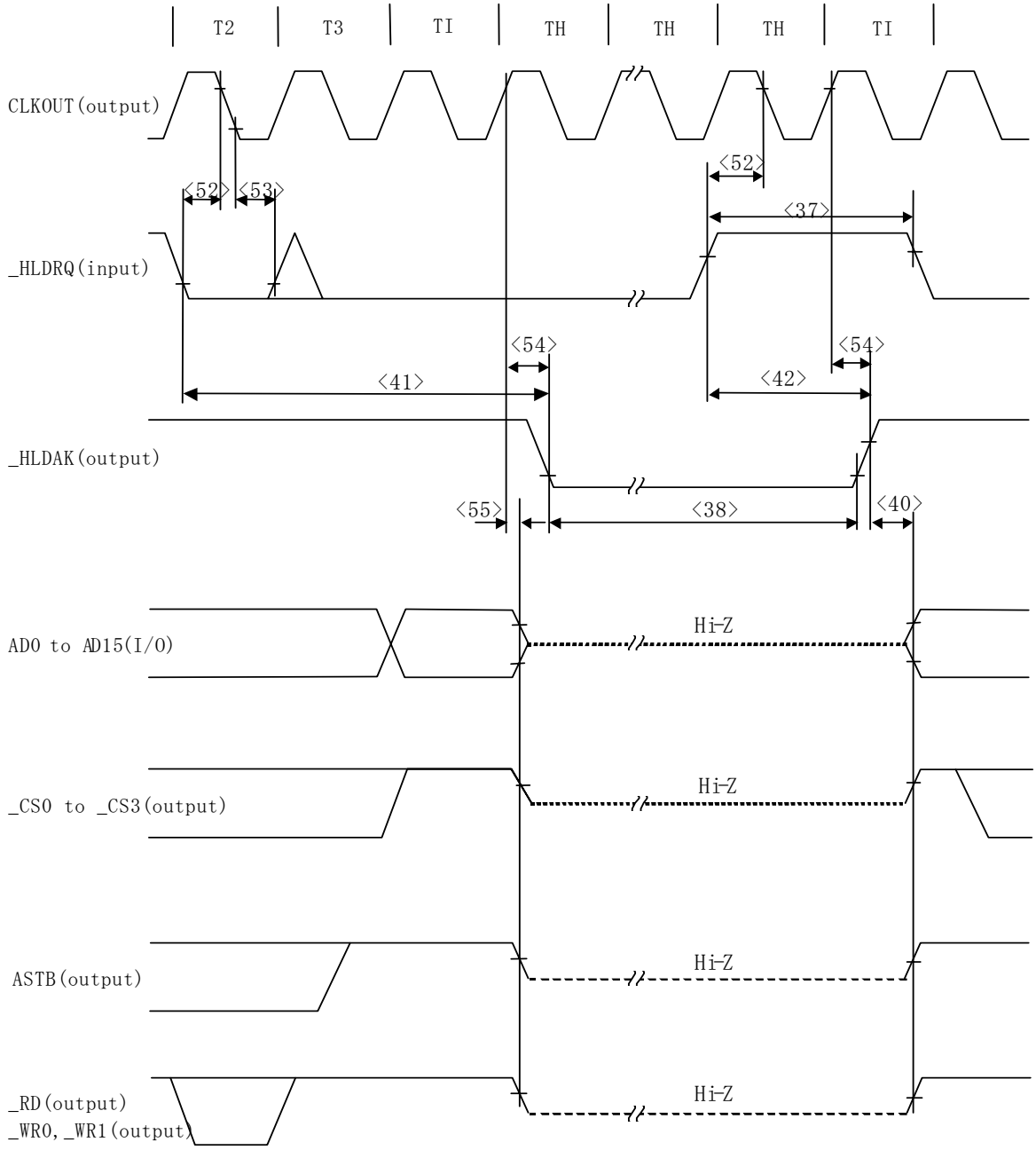
Remark: _WR0 and _WR1 are high level.

Write Cycle (CLKOUT Synchronous/ Asynchronous, 1 Wait): In Multiplexed Bus Mode



Remark: _RD Is high level.

Bus Hold: In Multiplexed Bus Mode



2.7.3 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-14	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-14	250			ns
		digital filter ,n=3	Note2			ns
ADTRG1 input high level width	tWADH	analog filter	250			ns
ADTRG1 input low level width	tWADL	analog filter	250			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG, ADTRG1 and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Key Return Timing

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 Timer Timing

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1] TIAA50-51,60-61,70-71 [Note1] TIAB00-03,10-13,20-23 [Note1]		250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1] TIAA50-51,60-61,70-71 [Note1] TIAB00-03,10-13,20-23 [Note1]		250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1] TIAA50-51,60-61,70-71 [Note1] TIAB00-03,10-13,20-23 [Note1]	4.0V≤VDD≤5.5V			16	MHz
			3.5V≤VDD<4.0V			10	

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn and TIABn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.6 CSI Timing

(a) Master mode

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

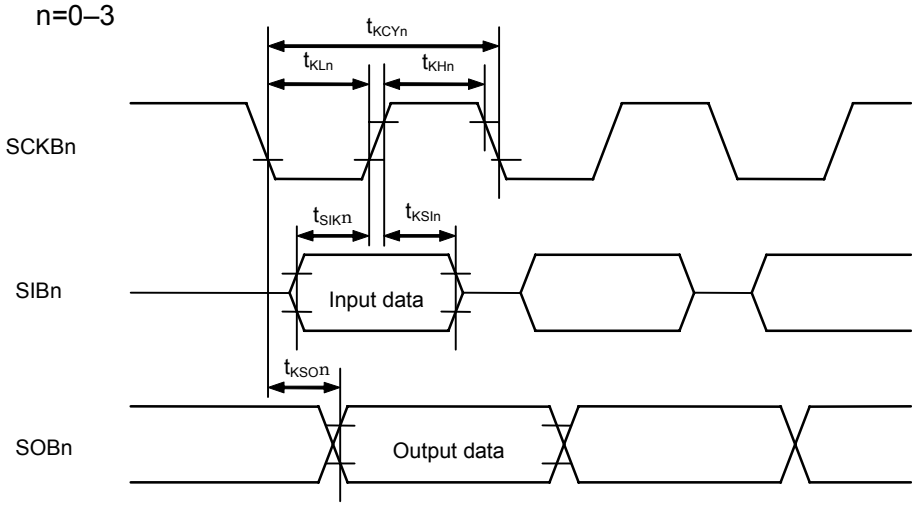
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–3



2.7.7 UART Timing

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

2.7.8 IIC Timing

Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter		Symbol	Normal mode		High-speed mode		Unit
			min.	max.	min.	max.	
SCL00 clock frequency		fCLK	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		tBUF	4.7		1.3		us
Hold time[Note1]		tHD:STA	4.0		0.6		us
SCL00 clock low-level width		tLOW	4.7		1.3		us
SCL00 clock high-level width		tHIGH	4.0		0.6		us
Setup time for start/restart conditions		tSU:STA	4.7		0.6		us
Data hold time	CBUS compatible master	tHD:DAT	5.0				us
	IIC mode		0[Note2]		0[Note2]	0.9[Note3]	us
Data setup time		tSU:DAT	250		100[Note4]		ns
SDA00 and SCL00 signal rise time		tR		1000	20+0.1Cb	300	ns
SDA00 and SCL00 signal fall time		tF		300	20+0.1Cb	300	ns
Stop condition setup time		tSU:STO	4.0		0.6		us
Pilse width with spike supporessed by input filter		tSP			0	50	ns
Capacitance load of each bus line		Cb		400		400	pF

Notes: 1. At the start condition, the first clock pulse Is generated after the hold time

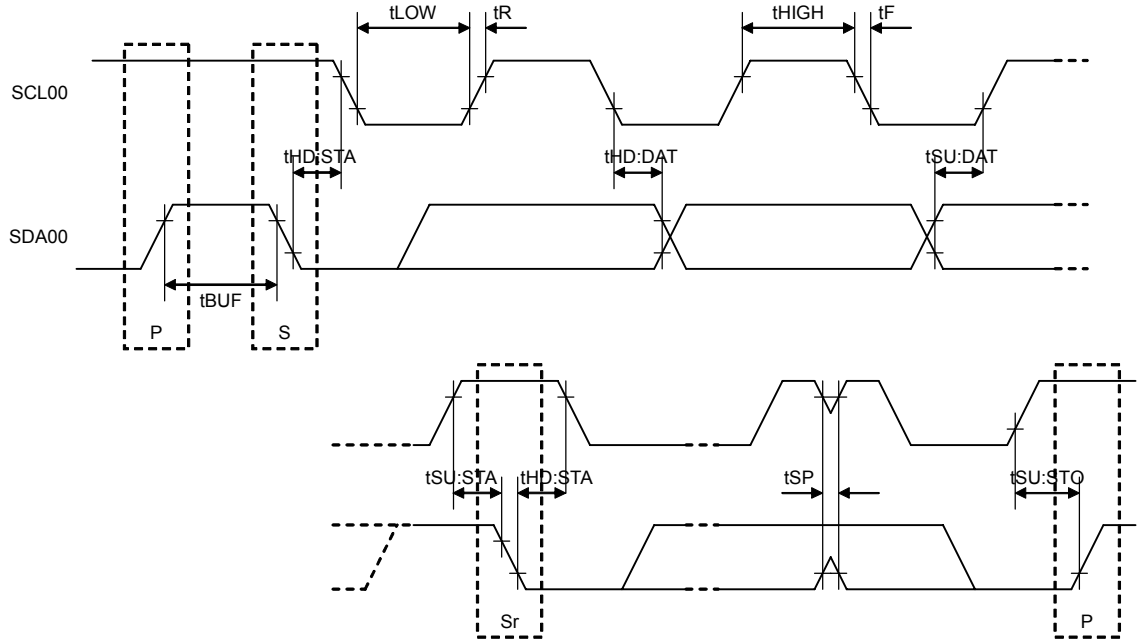
2. The system requires a minimum of 300ns hold time Internally for the SDA signal (at VIH-min. of SCL00 signal)
In order to occupy the undefined area at the falling edge of SCL00.

3. If the system does not extend the SCL00 signal low hold time (tlow), only the maximum data hold time (tHD:DAT) needs to be satisfied.

4. The high-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the high-speed-mode IIC bus so that It meets the following conditions.
- If the system does not extend the SCL00 signal's low state hold time:
SU:DAT?250ns
- If the system extends the SCL00 signal's low state hold time:
Transmit the following data bit to the SDA00 line prior to releasing the SCL00 line (tRmax.+tSU:DAT=1000+250=1250ns: Normal mode IIC bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

IIC bus interface timing

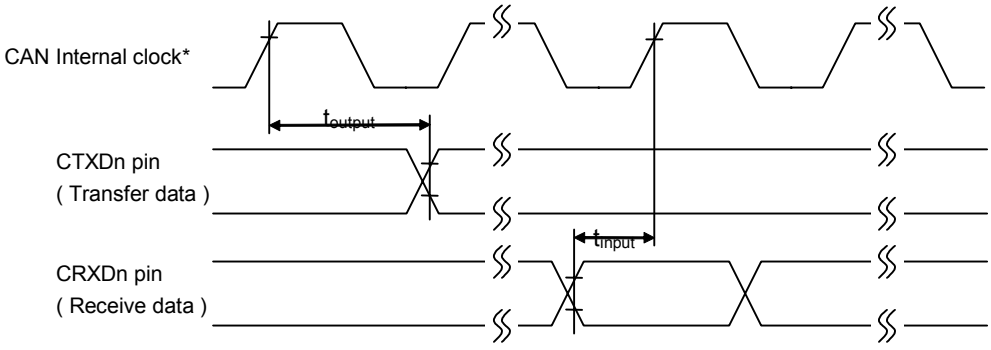


Remark: P: Stop condition
S: Start condition
Sr: Restart condition

2.7.9 CAN Timing

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time					100	ns



Internal delay time (tNODE)= Internal Transfer Delay(t_{output}) + Internal Receive Delay(t_{input})

*) CAN Internal clock (f_{CAN}) :CAN baud rate clock

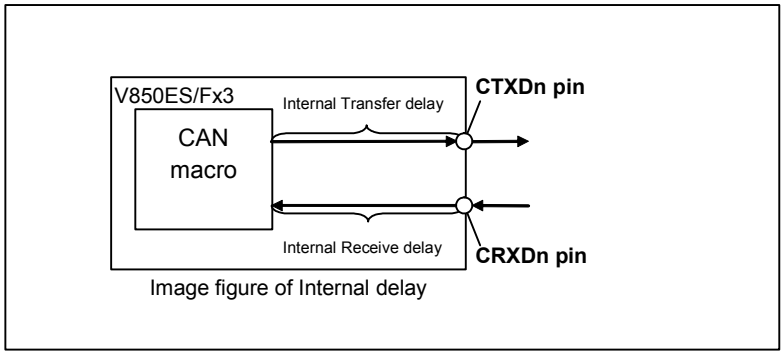


Image figure of Internal delay

2.8 A/D Converter

(a) AD0

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note1]		4.0V≤AVREF0<5.5V		±0.15	±0.3	%FSR
Conversion time	tCONV		3.10		16	μs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2			μs
Recovery time for power down mode	tDPU		1			μs
Zero-scale error[Note1]	ZSE				±0.3	%FSR
Full-scale error[Note1]	FSE				±0.3	%FSR
Integral non-liniearity error[Note2]	INL				±2.5	LSB
Differential non-liniearity error[Note2]	DNL				±1.5	LSB
Analog input voltage	VIAN		AVSS		AVREF0	V
Analog input equivalent circuit capacitance [Note3,4]	CINA				6.19	pF
Analog input equivalent circuit resistance [Note3]	RINA				2.55	kΩ
AVREF0 current	IAREF0	A/D operating		4	7	mA
		A/D operation stop		1	10	uA
Conversion rusult when using Diagnostic function		AVREF0 conversion	3FC		3FF	HEX
		AVSS conversion	000		003	HEX

(b) AD1

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V,VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note1]		4.0V≤AVREF1<5.5V		±0.15	±0.3	%FSR
Conversion time	tCONV		3.10		16	μs
Stabilization time	tSTA	After ADA1PS bit = 0 -> 1	2			μs
Recovery time for power down mode	tDPU		1			μs
Zero-scale error[Note1]	ZSE				±0.3	%FSR
Full-scale error[Note1]	FSE				±0.3	%FSR
Integral non-liniearity error[Note2]	INL				±2.5	LSB
Differential non-liniearity error[Note2]	DNL				±1.5	LSB
Analog input voltage	VIAN		AVSS		AVREF1	V
Analog input equivalent circuit capacitance [Note3,4]	CINA				5.51	pF
Analog input equivalent circuit resistance [Note3]	RINA				2.30	kΩ
AVREF1 current	IAREF1	A/D operating		4	7	mA
		A/D operation stop		1	10	uA
Conversion rusult when using Diagnostic function		AVREF1 conversion	3FC		3FF	HEX
		AVSS1 conversion	000		003	HEX

Notes: 1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.

2. Excluding quantization error (±1/2 LSB)

3. Not tested in production.

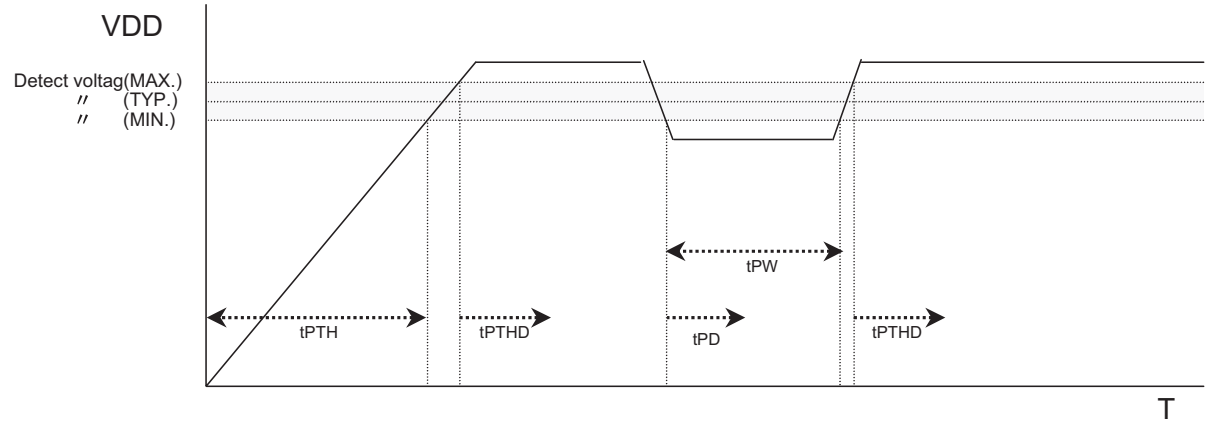
4. Does not include input/output capacitance CIO

2.9 POC

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VPOC0		3.3	3.5	3.7	V
Supply voltage rise time	tPTH	From VDD=0V to VDD=3.3V	0.002			ms
Response time1 Note1	tPTHD	In case of power on. After VDD reaches 3.7V.			2.0	ms
Response time2 Note2	tPD	In case of power off. After VDD drop 3.3V.		0.2	1.0	ms
VDD minimum width	tPW		0.2			ms

Notes: 1. From detect voltage to release reset signal
2. From detect voltage to occurrence of reset signal



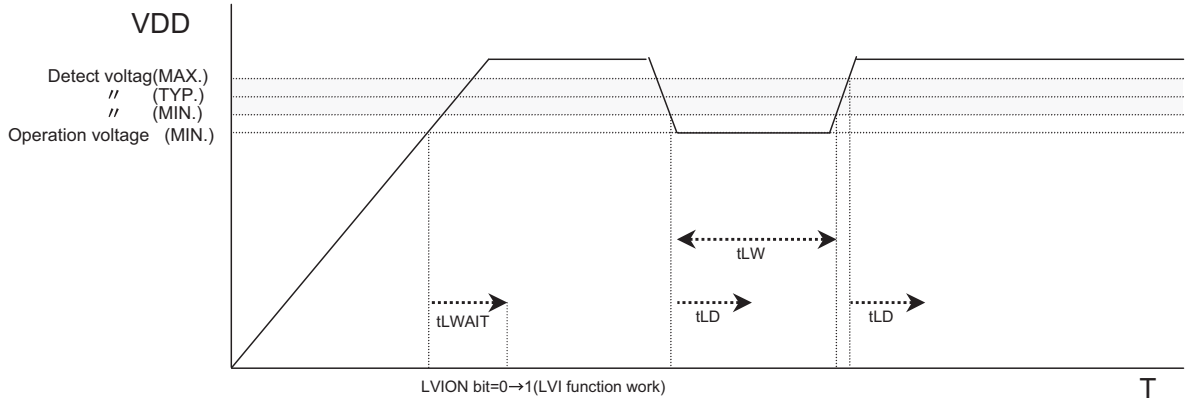
Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3 User's Manual.

2.10 LVI

(Ta = -40 to +85°C,
VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V,
VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VLVI0		3.8	4.0	4.2	V
	VLVI1		3.5	3.7	3.9	V
Response time Note1	tLD	After VDD reaches VLVI0/1(max). After VDD drop VLVI0/1(min).		0.2	2.0	ms
VDD minimum width	tLW		0.2			ms
Reference voltage stabilization wait time Note2	tLWAIT	After VDD reaches 3.3V. After LVION bit (LVIM.bit7) = 0->1		0.1	0.2	ms

Notes: 1. From detect voltage to occurrence interrupt/reset signal
2. If POC functionality is available, the wait time is not needed.

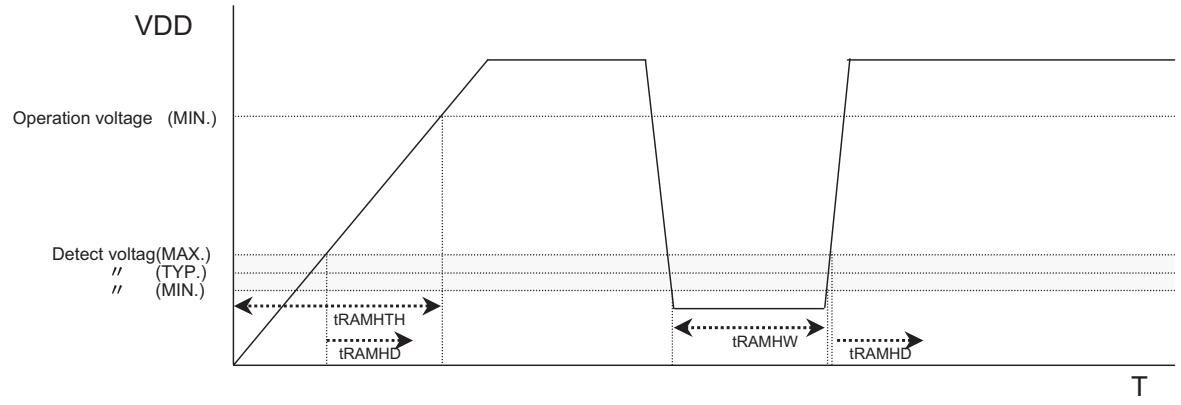


2.11 RAM Retention Flag

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 1.9V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VRAMH		1.9	2.0	2.1	V
Supply voltage rise time	tRAMHTH	From VDD=0V to VDD=3.3V	0.002		1800	ms
Response time Note1	tRAMHD	After VDD reaches 2.1V.		0.2	2.0	ms
VDD minimum width	tRAMHW		0.2			ms

Notes: 1. From detect voltage to set RAMFbit (RAMS.bit0)

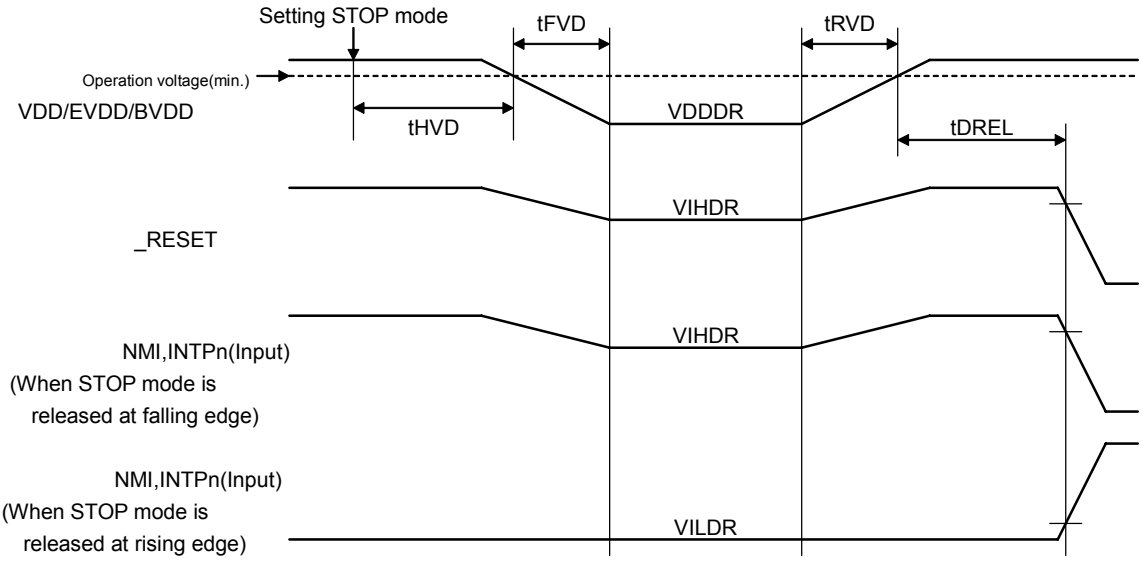


2.12 Data Retention Characteristics

(Ta = -40 to +85°C, VDD = VDD1 = EVDD = BVDD = 1.9V to 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	VDDDR	STOP mode (All function is stopped)	1.9		5.5	V
Data retention power supply current	IDDDR	VDDDR=2.0V(All function is stopped)		6.5	70	μA
Supply voltage rise time	tRVD		1			μs
Supply voltage fall time	tFVD		1			μs
Supply voltage hold time	tHVD	After STOP mode	0			ms
STOP release signal input time	tDREL	After VDD reaches operating voltage range MIN. 3.3V	0			ms
Data retention high-level input voltage	VIHDR	All input port	0.9VDDDR		VDDDR	V
Data retention low-level input voltage	VILDR	All input port	0		0.1VDDDR	V

Remark: When STOP mode is entered/released operation voltage range must be controlled.



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = VDD1 = EVDD = BVDD, AVREF0 = 3.5 to 5.5V, AVREF1 = 3.5 to 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	fCPU		4		48	MHz
Supply voltage	VDD		3.3		5.5	V
Number of rewrites	CWRT1	Code Flash	1000			count
		Data Flash				
	CWRT2		10000			
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V
Programming temperature	tPRG		-40		+85	°C
Data retention		Code Flash			15[Note1]	year
		Data Flash				
					5[Note2]	

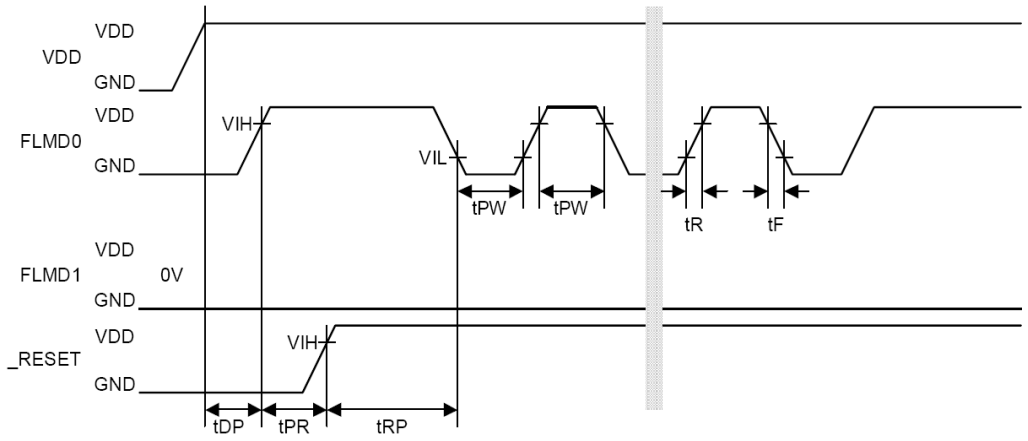
Notes: 1. Under the condition of CWRT1
2. Under the condition of CWRT2

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

(VDD = VDD1 = EVDD = BVDD, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	tDP		1			ms
$\overline{\text{RESET}}$ release (from FLMD0)	tPR		2			ms
FLMD0 pulse input start (from raise edge of _RESET)	tRP		800			μs
FLMD0 high level width / low level width	tPW		10		100	μs
FLMD0 raise time	tR				50	ns
FLMD0 fall time	tF				50	ns



3. Electrical Specifications of (A1)-Grade

This product has to be used only under the conditions of VDD = VDD1 = EVDD = BVDD. Operation is not ensured at the time of using this product except this condition.

3.1 Absolute Maximum Ratings

AbsAbsolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	VDD	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	VDD1	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	EVDD	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	BVDD	VDD = VDD1 = EVDD = BVDD		-0.5 to +6.5	V
	AVREF0			-0.5 to +6.5	V
	AVREF1			-0.5 to +6.5	V
	VSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	VSS1	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	EVSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	BVSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	AVSS	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
	AVSS1	VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1		-0.5 to +0.5	V
Input voltage	VI1	Pin Group 1x, 6		-0.5 to EVDD+0.5 Note1	V
	VI2	Pin Group 3x		-0.5 to BVDD+0.5 Note1	V
	VI3	Pin Group 7		-0.5 to VRO+0.5 Note1	V
Analog input voltage	VIAN	Pin Group 4		-0.5 to AVREF0+0.5 Note1	V
		Pin Group 5		-0.5 to AVREF1+0.5 Note1	V
High level output current	IOH	Pin Group 1x	1 pin	-4	mA
			Total	-20	mA
		Pin Group 3x	1 pin	-4	mA
			Total	-20	mA
		Pin Group 4	1 pin	-4	mA
			Total	-10 Note2	mA
		Pin Group 5	1 pin	-4	mA
			Total	-10 Note2	mA
Low level output current	IOL	Pin Group 1x	1 pin	4	mA
			Total	20	mA
		Pin Group 3x	1 pin	4	mA
			Total	20	mA
		Pin Group 4	1 pin	4	mA
			Total	10 Note2	mA
		Pin Group 5	1 pin	4	mA
			Total	10 Note2	mA
Operating ambient temperature	Ta	Normal operating mode		-40 to +110	°C
		Flash programming mode		-40 to +110	
Storage temperature	Tstg			-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 / IAREF1 current.

3.2 Capacities

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.3 Operating condition

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.4 Voltage Regulator Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.5 Clock Generator Circuit

3.5.1 Main System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +110°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

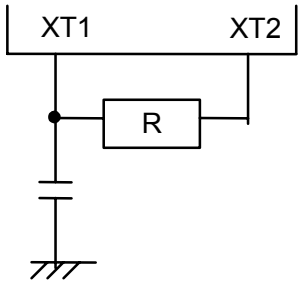
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequency Note1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	μs

Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided by 2 internally. In case of RC Oscillator, internal system clock frequency(fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.



3.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.5.4 PLL Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.5.5 SSCG Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.6 DC Characteristics

3.6.1 Input/Output Level

(Ta = -40 to +110°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Sym-bol	Conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH1	Pin Group 1B		0.7·EVDD		EVDD	V
	VIH2	Pin Group 1D		0.8·EVDD		EVDD	V
		Pin Group 3D		0.8·BVDD		BVDD	V
	VIH3	Pin Group 3A		0.7·BVDD		BVDD	V
	VIH4	Pin Group 4		0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
	VIH6	Pin Group 5		0.7·AVREF1		AVREF1	V
Low level input voltage	VIL1	Pin Group 1B		EVSS		0.3·EVDD	V
	VIL2	Pin Group 1D		EVSS		0.4·EVDD	V
		Pin Group 3D		BVSS		0.4·BVDD	V
	VIL3	Pin Group 3A		BVSS		0.3·BVDD	V
	VIL4	Pin Group 4		AVSS		0.3·AVREF0	V
	VIL5	Pin Group 6		EVSS		0.2·EVDD	V
	VIL6	Pin Group 5		AVSS1		0.3·AVREF1	V
Input hysteresis	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
	VHYS2	Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
		Pin Group 3D	Center point at 0.6 x BVDD Note3		0.192 x BVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High level output voltage Note2	VOH1	Pin Group 1x	IOH=-1.0mA	EVDD-1.0		EVDD	V
			IOH=-100uA	EVDD-0.5		EVDD	V
	VOH2	Pin Group 3x	IOH=-1.0mA	BVDD-1.0		BVDD	
			IOH=-100uA	BVDD-0.5		BVDD	V
	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
			IOH=-100uA	AVREF0-0.5		AVREF0	V
	VOH4	Pin Group 5	IOH=-1.0mA	AVREF1-1.0		AVREF1	V
			IOH=-100uA	AVREF1-0.5		AVREF1	V
Low level output voltage Note2	VOL1	Pin Group 1x	IOL=1.0mA	0		0.4	V
		P914, 915	IOL=3.0mA				
	VOL2	Pin Group 3x	IOL=1.0mA	0		0.4	V
	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
	VOL4	Pin Group 5	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	VI=0V		10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI=VDD		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)

2. Total IOH/IOL max is 20mA/-20mA for the power supply lines EVDD and BVDD.
Total IOH/IOL max is 10mA/-10mA for the power supply line AVREF0 and AVREF1.
AVREF0/AVREF1 IOH/IOL current is excluding ADC current IAREF0/IAREF1.

3. Typical value. Not tested and guaranteed

3.6.2 PIN leakage current

(Ta = -40 to +110°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Symbol	Conditions	MIN.		TYP.	MAX.	Unit
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.4	uA
			Other pins Note1			0.8	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.4	
			Other pins Note1			-0.8	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.4	
			Other pins			0.8	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.4	
			Other pins			-0.8	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current : 4.0uA
Low level input leakage current : -4.0uA

3.6.3 Power supply current (A1-grade)

3.6.3.1 µPD70F3383 / µPD70F3384 / µPD70F3385

(a) Absolute values

(Ta = -40 to +110°C,
VDD =VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V Note1)

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	35	47	mA
					f_{xx}=32MHz f_X=16MHz	52	68	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	17	24	mA
					f_{xx}=16MHz f_X=16MHz	29	38	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	63	81	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	28		mA
					f_{xx}=32MHz f_X=16MHz	41		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	15		mA
					f_{xx}=16MHz f_X=16MHz	23		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	54		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	24	34	mA
					f_{xx}=32MHz f_X=16MHz	36	51	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	10	16	mA
					f_{xx}=16MHz f_X=16MHz	18	26	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	40	54	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	16		mA
					f_{xx}=32MHz f_X=16MHz	24		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	8		mA
					f_{xx}=16MHz f_X=16MHz	12		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_X=12MHz	30		mA

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	2.6	3.6	mA
				f_{xx}=12MHz f_X=12MHz	4.1	5.6	mA
				f_{xx}=16MHz f_X=16MHz	4.9	6.8	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		3.0	4.2	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	1.4		mA
				f_{xx}=12MHz f_X=12MHz	1.8		mA
				f_{xx}=16MHz f_X=16MHz	2.0		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.3		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_X=5MHz	0.4	0.9	mA
				f_{xx}=12MHz f_X=12MHz	0.7	1.2	mA
				f_{xx}=16MHz f_X=16MHz	0.8	1.4	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.7	mA
SUB operating mode Note5	IDD5	RC resonator (fxt=20kHz) Note6			80	600	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1200	μA
SubIDLE mode Note3,5	IDD6	RC resonator (fxt=20kHz) Note6			40	420	μA
		240kHz Internal-OSC (SubOSC stopped)			25	380	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	280	μA
			240kHz Internal-OSC working		15.5	295	μA
		POC work	240kHz Internal-OSC stop		10.5	285	μA
			240kHz Internal-OSC working		18.5	300	μA

(b) Calculation formulas

(Ta = -40 to +110°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V) Note1)

Mode	Symbol	Condition			TYP. Note9	MAX. Note3	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{XX} PRSI option: 0	PLL: ON 12MHz≤f_{XX}≤32MHz	1.39·f_{XX}+7.5	1.67·f_{XX}+14.0	mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	1.44·f_{XX}+5.5	1.73·f_{XX}+10.6	mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 12MHz≤f_{XX}≤48MHz	1.17·f_{XX}+6.9	1.41·f_{XX}+13.3	mA
		All peripherals stopped	Peripheral: ff_{XX}- PRSI option: 0	PLL: ON 12MHz≤f_{XX}≤32MHz	1.06·f_{XX}+7.2		mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	1.00·f_{XX}+7.0		mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 12MHz≤f_{XX}≤48MHz	0.96·f_{XX}+7.8		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: ff_{XX}- PRSI option: 0	PLL: ON 16MHz≤f_{XX}≤32MHz	1.00·f_{XX}+4.0	1.40*f_{XX}+6.4	mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	0.94·f_{XX}+2.7	1.27*f_{XX}+5.4	mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 16MHz≤f_{XX}≤48MHz	0.75·f_{XX}+4.0	0.94*f_{XX}+9.0	mA
		All peripherals stopped	Peripheral: f_{XX} PRSI option: 0	PLL: ON 16MHz≤f_{XX}≤32MHz	0.65·f_{XX}+3.4		mA
				PLL: OFF 4MHz≤f_{XX}≤16MHz	0.59·f_{XX}+2.8		mA
			Peripheral: f_{XX}/2 PRSI option: 1	PLL: ON 16MHz≤f_{XX}≤48MHz	0.54·f_{XX}+4.4		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{XX}≤16MHz Note7	0.211·f_{XX}+1.54	0.295·f_{XX}+ 2.10	mA
		All peripherals stopped			0.054·f_{XX}+1.15		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{XX}≤16MHz Note7			0.037·f_{XX}+0.21	0.049·f_{XX}+ 0.63	mA

Notes: 1. VDD, VDD1, EVDD and BVDD total current. (Ports are stopped).
AVREF0 and AVREF1 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

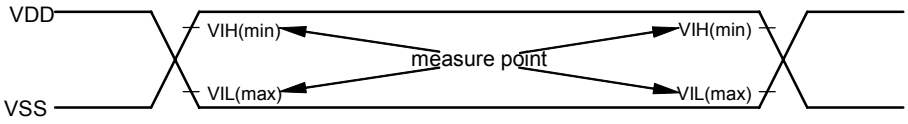
2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or EEPROM emulation mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 14-(0.33*fxx/2+0.1)*2 [mA]
  + In case of PLL ON: 14-(0.18*fxx/2+3.0)*2 [mA]
- EEPROM emulation mode:
  + 7-(0.18*fxx/4+3.0) [mA]

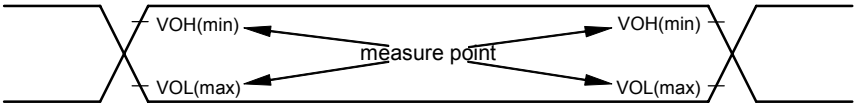
3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{XX} are tested in the outgoing device inspection.

3.7 AC Characteristics

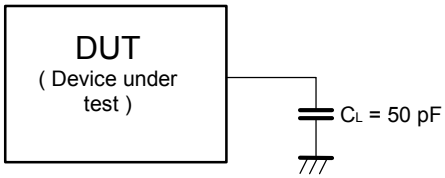
AC test Input measurement points (VDD, AVREF0, AVREF1, EVDD, BVDD)



AC test output measurement points



Load conditions



Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

3.7.1 CLKOUT Output Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.2 Bus Timing (Multiplexed bus mode)

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.3 RESET, Interrupt, ADTRG Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.4 Key Return Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.5 Timer Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.6 CSI Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.7 UART Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.8 IIC Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.7.9 CAN Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.8 A/D Converter

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.9 POC

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.10 LVI

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.11 RAM Retention Flag

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.12 Data Retention Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

3.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = VDD1 = EVDD = BVDD, AVREF0 = 3.5 to 5.5V, AVREF1 = 3.5 to 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	fCPU		4		48	MHz
Supply voltage	VDD		3.3		5.5	V
Number of rewrites	CWRT1	Code Flash	1000			count
		Data Flash				
	CWRT2		10000			
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V
Programming temperature	tPRG		-40		+110	°C
Data retention		Code Flash			15[Note1]	year
		Data Flash				
					5[Note2]	

Notes: 1. Under the condition of CWRT1
2. Under the condition of CWRT2

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +110°C.

4. Electrical Specifications of (A2)-Grade

This product has to be used only under the conditions of VDD = VDD1 = EVDD = BVDD. Operation is not ensured at the time of using this product except this condition.

4.1 Absolute Maximum Ratings

Specification is identical to that from (A1)-Grade except

- Operating ambient temperature Ta = -40 to +125°C
- Note2: AVREF0/AVREF1 IOH/IOL current is including ADC max. current IAREF0/IAREF1.

4.2 Capacities

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.3 Operating condition

(Ta = -40 to +125°C, VDD = VDD1 = EVDD = BVDD, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, C = 4.7uF)

Internal System clock frequency (f_{VBCLK})	Supply voltage (VDD)	Operating Condition

4.0≤f_{xx}≤32MHz Note1	4.0V≤VDD≤5.5V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • $f_{XP1} \leq f_{xx}$
		  • $f_{XP2} \leq f_{xx}$
		• AC characteristics:
		  • Refer to chapter '4.7 AC Characteristics' for details.

	3.5V≤VDD≤4.0V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • $f_{XP1} \leq$ 20MHz
		  • $f_{XP2} \leq$ 20MHz
		• AC characteristics:
		  • Refer to chapter '4.7 AC Characteristics' for details.

	3.3V≤VDD<3.5V Note2	Only operation of following function is assured: • CPU • Flash (include programming) • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI

	3.5V≤AVREF0<5.5V	• A/D Converter
		  • Refer to chapter '4.8 A/D Converter' for details.
		  • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0)

	3.5V≤AVREF1<5.5V	• A/D Converter
		  • Refer to chapter '4.8 A/D Converter' for details.
		  • stop ADC for AVREF1 < 4.0V (ADA1CE bit =0)

12.5kHz≤f_{XT}≤27.5kHz Note3(RC)	3.3V≤VDD<5.5V Note2	-
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note2	-

Notes: 1. For using SSCG please refer to '4.5.5 SSCG Characteristics' for details
2. VDD = VDD1 = EVDD = BVDD
3. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

4.4 Voltage Regulator Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.5 Clock Generator Circuit

4.5.1 Main System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.5.2 Sub System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A1)-Grade except Ta = -40 to +125°C.

4.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.5.4 PLL Characteristics

(Ta = -40 to +125°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note	3		6	MHz
Output frequency	fxx		12		32	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

4.5.5 SSCG Characteristics

(Ta = -40 to +125°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	f_{XX}		12		32	MHz
Lock time	t_{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector SFC1[6:4]	Percent modulation		Maximum average operating frequency		Unit
	TYP	MAX		≥384KB product	
000B	± 0.5%	± 2.0%		31.4	MHz
001B	± 1.0%	± 2.5%		31.2	
010B	± 2.0%	± 4.0%		30.7	
011B	± 3.0%	± 6.0%		30.1	
100B	± 4.0%	± 8.0%		29.4	
101B	± 5.0%	± 10.0%		28.8	

4.6 DC Characteristics

4.6.1 Input/Output Level

Specification is identical to that from (A1)-Grade except

- Ta = -40 to +125°C.
- **Note 2:**Total IOH/IOL max is 20mA/-20mA for the power supply lines EVDD and BVDD.
  Total IOH/IOL max is 3mA/-3mA for the power supply line AVREF0 and AVREF1.
  AVREF0/AVREF1 IOH/IOL current is excluding ADC current IAREF0/IAREF1.
  If ADC0/ADC1 is not used total IOH/IOL max is 10mA/-10mA for the power supply line AVREF0 and AVREF1.

4.6.2 PIN leakage current

(Ta = -40 to +125°C, VDD = VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V)

Parameter	Symbol	Conditions	MIN.		TYP.	MAX.	Unit
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.5	uA
			Other pins Note1			1.0	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.5	
			Other pins Note1			-1.0	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.5	
			Other pins			1.0	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.5	
			Other pins			-1.0	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current: 5.0uA
Low level input leakage current: -5.0uA

4.6.3 Power supply current (A2-grade)

4.6.3.1 µPD70F3383 / µPD70F3384 / µPD70F3385

(a) Absolute values

(Ta = -40 to +125°C,
VDD =VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V Note1)

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	35	47	mA
					f_{xx}=32MHz f_x=16MHz	52	68	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	17	24	mA
					f_{xx}=16MHz f_x=16MHz	29	38	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	28		mA
					f_{xx}=32MHz f_x=16MHz	41		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	15		mA
					f_{xx}=16MHz f_x=16MHz	23		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	24	34	mA
					f_{xx}=32MHz f_x=16MHz	36	51	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	10	16	mA
					f_{xx}=16MHz f_x=16MHz	18	26	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	16		mA
					f_{xx}=32MHz f_x=16MHz	24		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	8		mA
					f_{xx}=16MHz f_x=16MHz	12		mA

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	2.6	3.9	mA
				f_{xx}=12MHz f_X=12MHz	4.1	5.9	mA
				f_{xx}=16MHz f_X=16MHz	4.9	7.1	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		3.0	4.5	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	1.4		mA
				f_{xx}=12MHz f_X=12MHz	1.8		mA
				f_{xx}=16MHz f_X=16MHz	2.0		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.3		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_X=5MHz	0.4	1.1	mA
				f_{xx}=12MHz f_X=12MHz	0.7	1.5	mA
				f_{xx}=16MHz f_X=16MHz	0.8	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	1.0	mA
SUB operating mode Note5	IDD5	RC resonator (fxt=20kHz) Note6			80	850	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1760	μA
SubIDLE mode Note3,5	IDD6	RC resonator (fxt=20kHz) Note6			40	670	μA
		240kHz Internal-OSC (SubOSC stopped)			25	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	550	μA
			240kHz Internal-OSC working		15.5	565	μA
		POC work	240kHz Internal-OSC stop		10.5	555	μA
			240kHz Internal-OSC working		18.5	570	μA

(b) Calculation formulas

(Ta = -40 to +125°C, VDD =VDD1 = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V) Note1)

Mode	Symbol	Condition			TYP. Note9	MAX. Note3	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	1.39·f_{xx}+7.5	1.67·f_{xx}+14.0	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	1.44·f_{xx}+5.5	1.73·f_{xx}+10.6	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	1.17·f_{xx}+6.9	1.41·f_{xx}+13.3	mA
		All peripherals stopped	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	1.06·f_{xx}+7.2		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	1.00·f_{xx}+7.0		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.96·f_{xx}+7.8		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	1.00·f_{xx}+4.0	1.40*f_{xx}+6.4	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.94·f_{xx}+2.7	1.27*f_{xx}+5.4	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.75·f_{xx}+4.0	0.94*f_{xx}+9.0	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.65·f_{xx}+3.4		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.59·f_{xx}+2.8		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.54·f_{xx}+4.4		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	0.211·f_{xx}+1.54	0.295·f_{xx}+ 2.40	mA
		All peripherals stopped			0.054·f_{xx}+1.15		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz Note7			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.88	mA

Notes: 1. VDD, VDD1, EVDD and BVDD total current. (Ports are stopped).
AVREF0 and AVREF1 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

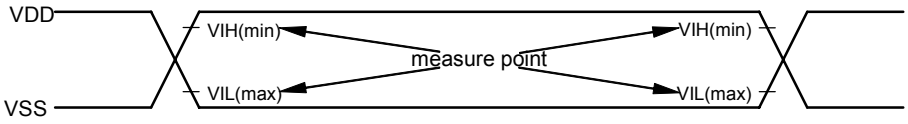
2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or EEPROM emulation mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 14-(0.33*fxx/2+0.1)*2 [mA]
  + In case of PLL ON: 14-(0.18*fxx/2+3.0)*2 [mA]
- EEPROM emulation mode:
  + 7-(0.18*fxx/4+3.0) [mA]

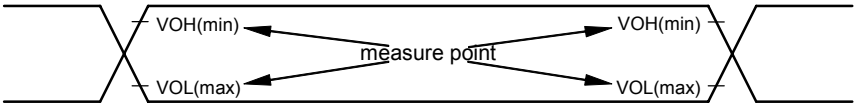
3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

4.7 AC Characteristics

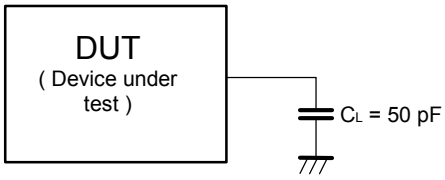
AC test Input measurement points (VDD, AVREF0, AVREF1, EVDD, BVDD)



AC test output measurement points



Load conditions



Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

4.7.1 CLKOUT Output Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.2 Bus Timing (Multiplexed bus mode)

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.3 RESET, Interrupt, ADTRG Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.4 Key Return Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.5 Timer Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.6 CSI Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.7 UART Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.8 IIC Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.7.9 CAN Timing

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.8 A/D Converter

(a) AD0

(Ta = -40 to +125°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note1]		4.0V≤AVREF0<5.5V		±0.15	±0.35	%FSR
Conversion time	tCONV		3.10		16	μs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2			μs
Recovery time for power down mode	tDPU		1			μs
Zero-scale error[Note1]	ZSE				±0.35	%FSR
Full-scale error[Note1]	FSE				±0.35	%FSR
Integral non-liniearity error[Note2]	INL				±2.5	LSB
Differential non-liniearity error[Note2]	DNL				±1.5	LSB
Analog input voltage	VIAN		AVSS		AVREF0	V
Analog input equivalent circuit capacitance [Note3,4]	CINA				6.19	pF
Analog input equivalent circuit resistance [Note3]	RINA				2.55	kΩ
AVREF0 current	IAREF0	A/D operating		4	7	mA
		A/D operation stop		1	10	uA
Conversion rusult when using Diagnostic function		AVREF0 conversion	3FC		3FF	HEX
		AVSS conversion	000		003	HEX

(b) AD1

(Ta = -40 to +125°C, VDD = VDD1 = EVDD = BVDD = 3.5V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, 4.0 ≤ AVREF1 ≤ 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1 = 0V, CL = 50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note1]		4.0V≤AVREF1<5.5V		±0.15	±0.35	%FSR
Conversion time	tCONV		3.10		16	μs
Stabilization time	tSTA	After ADA1PS bit = 0 -> 1	2			μs
Recovery time for power down mode	tDPU		1			μs
Zero-scale error[Note1]	ZSE				±0.35	%FSR
Full-scale error[Note1]	FSE				±0.35	%FSR
Integral non-liniearity error[Note2]	INL				±2.5	LSB
Differential non-liniearity error[Note2]	DNL				±1.5	LSB
Analog input voltage	VIAN		AVSS		AVREF1	V
Analog input equivalent circuit capacitance [Note3,4]	CINA				5.51	pF
Analog input equivalent circuit resistance [Note3]	RINA				2.30	kΩ
AVREF1 current	IAREF1	A/D operating		4	7	mA
		A/D operation stop		1	10	uA
Conversion rusult when using Diagnostic function		AVREF1 conversion	3FC		3FF	HEX
		AVSS1 conversion	000		003	HEX

Notes: 1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.

2. Excluding quantization error (±1/2 LSB)

3. Not tested in production.

4. Does not include input/output capacitance CIO

4.9 POC

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.10 LVI

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.11 RAM Retention Flag

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.12 Data Retention Characteristics

Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

4.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = VDD1 = EVDD = BVDD, AVREF0 = 3.5 to 5.5V, AVREF1 = 3.5 to 5.5V, VSS = VSS1 = EVSS = BVSS = AVSS = AVSS1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	fCPU		4		32	MHz
Supply voltage	VDD		3.3		5.5	V
Number of rewrites	CWRT1	Code Flash	1000			count
		Data Flash				
	CWRT2		10000			
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V
Programming temperature	tPRG		-40		+125	°C
Data retention		Code Flash			15[Note1]	year
		Data Flash				
					5[Note2]	

Notes: 1. Under the condition of CWRT1
2. Under the condition of CWRT2

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

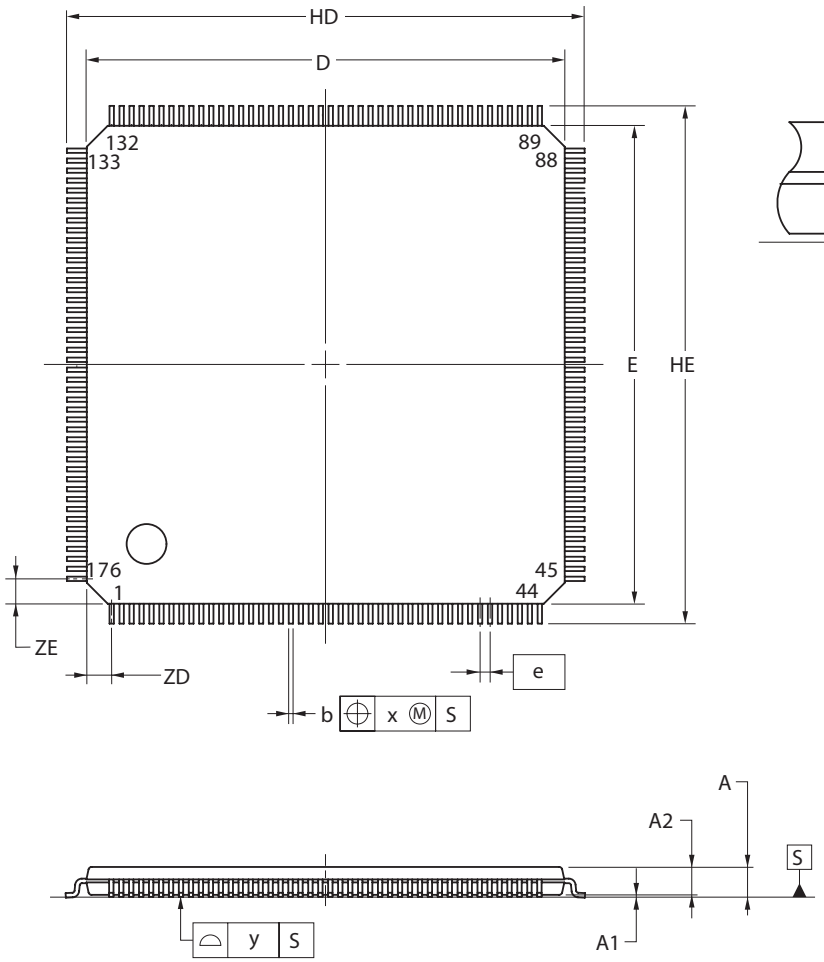
(b) Serial Writing Operation Characteristics

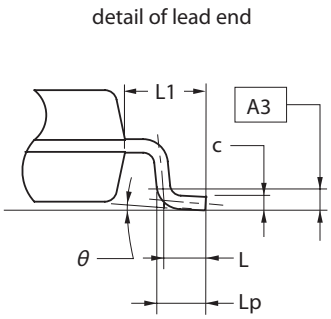
Specification is identical to that from (A)-Grade except Ta = -40 to +125°C.

5. Package

5.1 Package Dimension

176-PIN PLASTIC LQFP (FINE PITCH) (24x24)





(UNIT:mm)

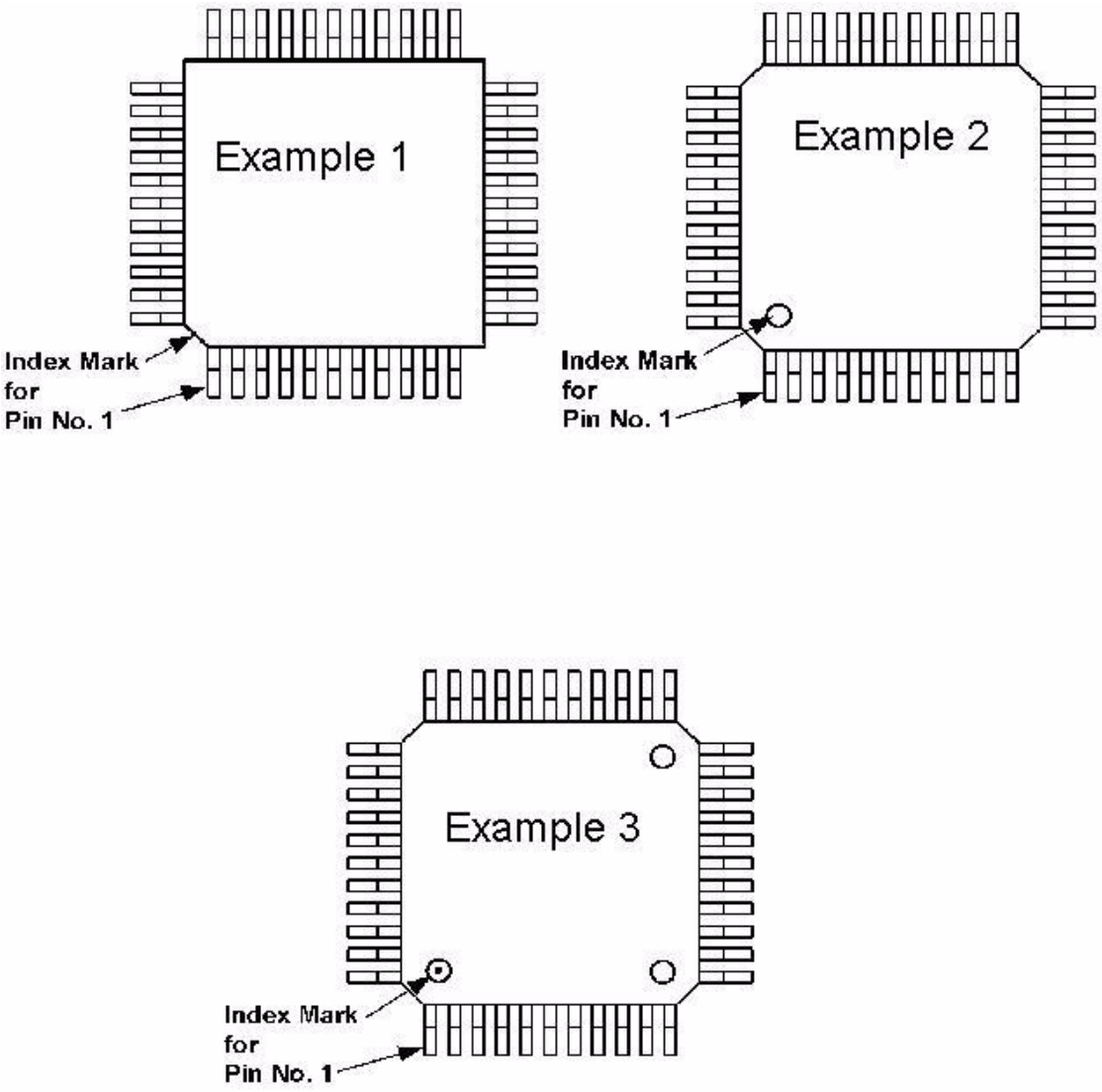
ITEM	DIMENSIONS
D	24.00 ±0.20
E	24.00 ±0.20
HD	26.00 ±0.20
HE	26.00 ±0.20
A	1.60 MAX.
A1	0.10 ±0.05
A2	1.40 ±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P176GM-50-GAR

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

5.2 Product Marking

5.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

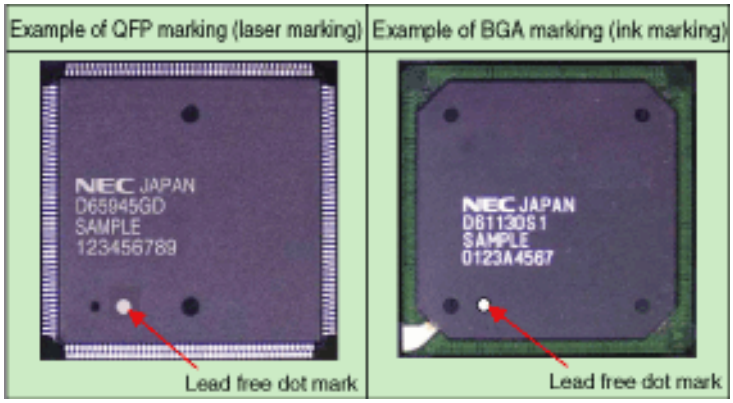
Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 5.2.2 "Identification of Lead-Free Products" on page 63.

5.2.2 Identification of Lead-Free Products

Lead-Free products are marked with a dot "•". The marking methods are the paint or the laser (It doesn't sink in). The shape of lead-free marks is a circle.
Example:



6. Change History

The following revision list shows all major changes of the different datasheet versions.

Version	Chapter	Comment
V1.0		Initial release
V1.1	2.13 3.13	Removed ’Target Specification’ for (A)- and (A1)-Grade Devices in the Flash Programming specifications.
		Changed specification of ’Number of rewrites’ from MAX. to MIN.
	2.8 4.8	Removed Caution (described in User’s Manual)
V1.2		Changed document status from ’Preliminary Datasheet’ to ’Datasheet’.
	4.13	Removed ’Target Specification’ for (A2)-Grade Devices in the Flash Programming specifications.

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Clarity	☐	☐	☐	☐
Technical Accuracy	☐	☐	☐	☐
Organization	☐	☐	☐	☐

[MEMO]