Data Sheet

32

V850E/DG3

32-bit Single-Chip Microcontroller

μPD70F3416
μPD70F3417

Renesas Electronics
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R01DS0109ED0200, Rev. 2.00
Jun 8, 2011

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   – The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at power-on

   The state of the product is undefined at the moment when power is supplied.

   – The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited.

   – The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   – When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   – The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Table of Contents

Chapter 1 Overview

The V850E/DG3 is a product in Renesas V850 family of single-chip microcontrollers designed for Automotive applications.

1.1 General

The V850E/DG3 single-chip microcontroller, is a member of Renesas V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.

The V850E/DG3 provides an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI), Timers and measurement inputs (A/D converter), with dedicated CAN network support. Control and driver for 6 stepper motors are included.

The device offers power-saving modes to manage the power consumption effectively under varying conditions.

Thus equipped, the V850E/DG3 is ideally suited for automotive applications, like dashboard or body. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

This specification covers the following devices of the family:

Family Code	Product Code	Package	Internal Flash	Internal RAM
DG3	µPD70F3417GC(A)-UEU	LQFP 14 x 14mm	256 kbyte	12 kbytes
	uPD70F3416GC(A)-UEU		128 kbyte	6 kbytes

The following table gives a more detailed overview of the different derivates and their major features.

Series name		**V850E/DG3**	
Product Code		**µPD70F3417(A)**	**µPD70F3416(A)**
Technology		MF2 (Flash)	MF2 (Flash)
Internal memory	Flash	256kB	128kB
	ROM	None	None
	RAM	12kB	6kB
Operating Clock	Main (internal)	24MHz[a] max.	
	Ring-OSC	240kHz typ.	
	Subclock	32kHz typ.	
I/O ports		72	
Input ports		8	
A/D converter		8 ch	
Timers	TMZ	6 ch	
	TMP	1 ch	
	TMG	2 ch	
	TM0	1 ch	
	WDT	provided	
	Watch	provided	
	Watch calibration	provided	
Serial interfaces	AFCAN	1 ch (with 32 message buffers)	
	UARTA	2 ch (with LIN support)	
Serial interfaces	CSIB	2 ch	
	IIC	1 ch	
Interrupts	External	4	
	Internal	52	
	NMI	2	
Other functions	ROM-correction	6 ch	
	POC	provided	
	Clock supervision	2 ch	
	Sound generator	1 ch	
	Stepper motor C/D	4 ch	
	LCD C/D	40 x 4	
	Auxilliary frequency output	provided	
Operating voltage		3.2V to 5.5V for core functions, ADC and StepperMotor C/D, 3.0V to 5.5V for all other I/O Full operation in range from 3.5V to 5.5V due to POC function (*8.2 on page 57*)	
Package		100-pin LQFP	

a) Operated with spread spectrum PLL

Chapter 2 Pinout Information

2.1 Pin Configuration µPD70F3417(A), µPD70F3416(A)

- µPD70F3417(A)GC
- µPD70F3416(A)GC

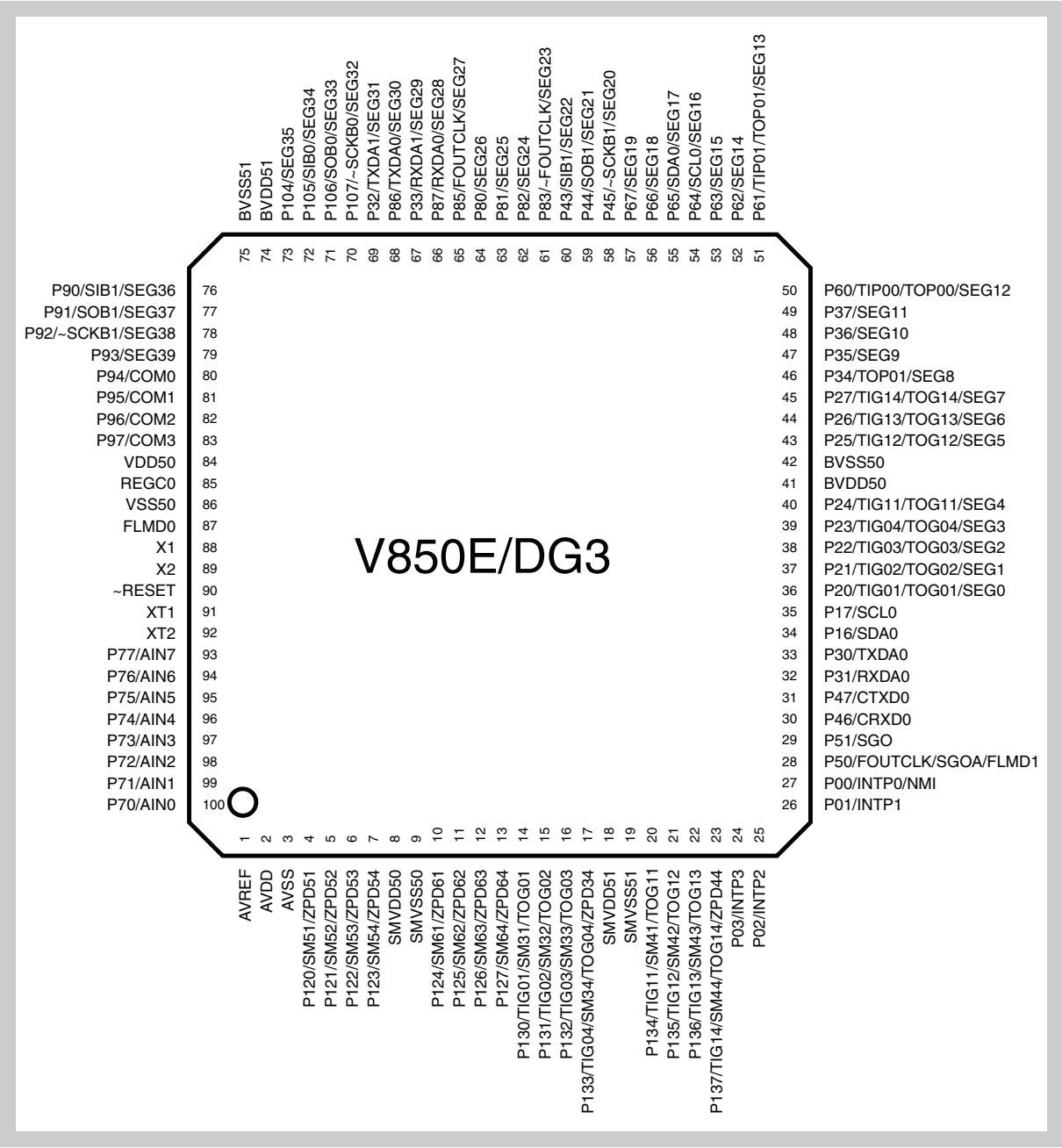


Figure 2-1 Pin Configuration µPD70F3417(A), µPD70F3416(A)

2.2 Pin Group information

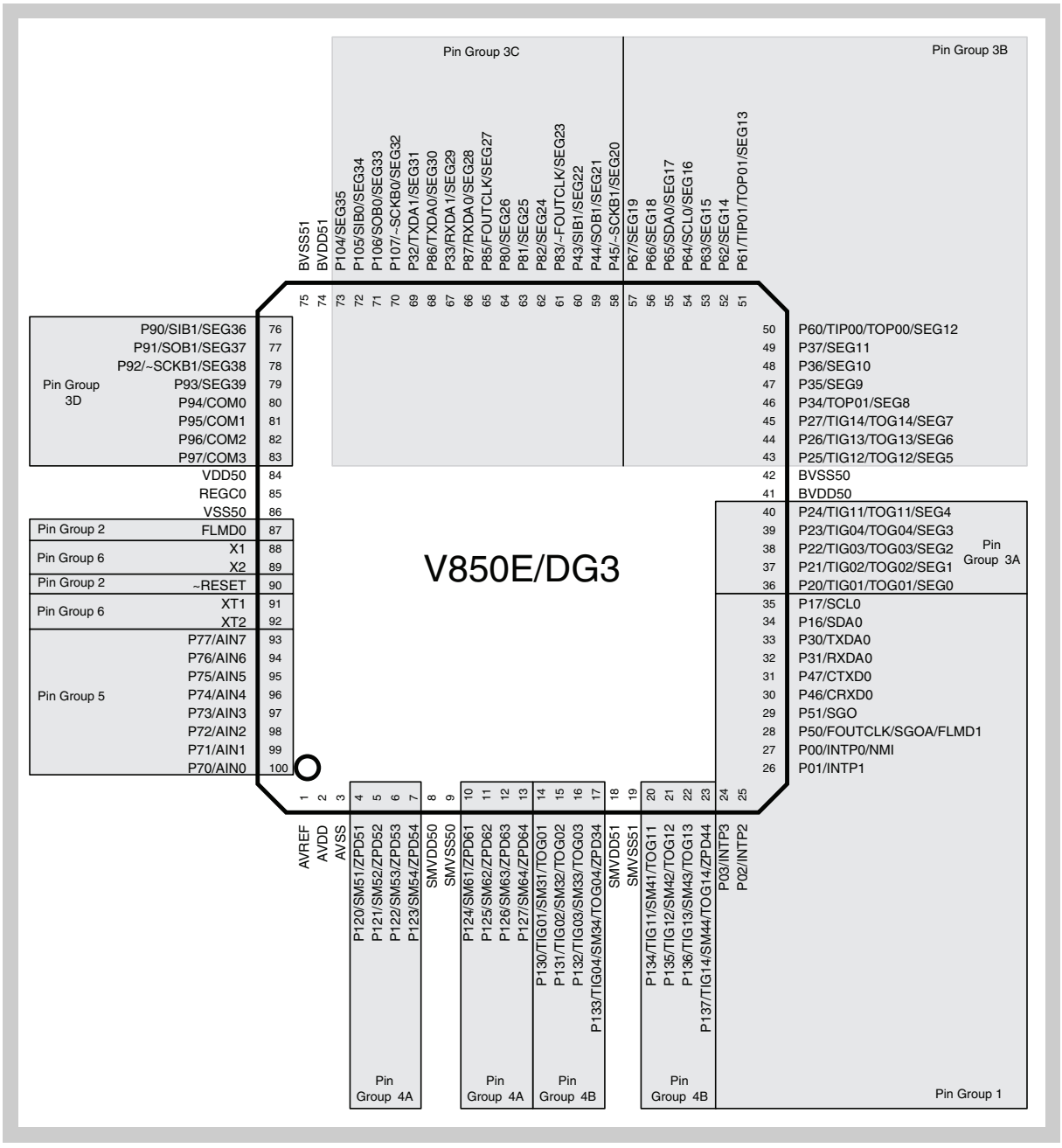


Figure 2-2 Pin Group Information µPD70F3417(A), µPD70F3416(A)

- Pin Groups 1x: GPIO pins supplied by BV_{DD5}
  1: P00-P03, P16-P17, P30-P31, P46-P47, P50-P51
- Pin Group 2: Pins supplied by V_{DD50}
  2: ($\overline{\text{RESET}}$, FLMD0)
- Pin Group 3x: GPIO and LCD controller supplied by BV_{DD5}
  3A: P20-P24
  3B: P20-P27, P34-P37, P60-P67
  3C: P32, P43-P45, P80-P83, P85-P87, P104-P107
  3D: P90-P97
- Pin Group 4x: Stepper Motor outputs supplied by SMV_{DD5}
  4A: P120-P127
  4B: P130-P137
- Pin Group 5: ADC Inputs supplied by AV_{DD}
  5: P70-P77
- Pin Group 6: Oscillator function supplied internally
  6: X1, X2, XT1, XT2
- Pin Group 7: Pins used for ZPD (if supported). This group is a subset of Group 4.
  7: P120-P127, P133, P137

Chapter 3 Absolute Maximum Ratings

Condition 1: T_A = -40 ... +85°C,

Operation Modes: RUN, HALT, IDLE

Power dissipation: < 0.61W

Duration: 15000 hours

V_{SS5} = 0V

Condition 2: T_A = -40 ... +85°C,

Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation

Power dissipation: < 0.5W

Duration: 15 years

V_{SS5} = 0V

Table 3-1 Absolute maximum ratings voltages

Parameter		Symbol	Test Conditions	Ratings [a]	Unit
Supply voltage		V_{DD5}		-0.5 ~ +6.5	V
		AV_{DD}		-0.5 ~ +6.5	V
		AV_{REF}		-0.5 ~ +6.5	V
		BV_{DD5}		-0.5 ~ +6.5	V
		SMV_{DD5}		-0.5 ~ +6.5	V
		AV_{SS}		-0.5 ~ +0.5	V
		BV_{SS5}		-0.5 ~ +0.5	V
		SMV_{SS5}		-0.5 ~ +0.5	V
Input voltage	Group 1	V_{I1}	$V_{I1} < BV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 2	V_{I2}	$V_{I2} < V_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 4	V_{I4}	$V_{I4} < SMV_{DD5} + 0.5$ V	-0.5 ~ + 6.5	V
	Group 5, AVREF	V_{IA}	$V_{IA} < AV_{DD} + 0.5$ V	-0.5 ~ + 6.5	V
Special [b]	X1, X2, XT1, XT2, REGC0	V_{IS}		-0.5 ~ + 3.6	V
Output voltage		V_O		-0.5 ~ +6.5	V
Operating temperature (ambient)		T_{OPR}		-40 ~ +85	°C
Storage temperature		T_{STGB}		-40 ~ +150	°C

a) Currents are average current over the given life time. Transient currents are not relevant as long as the average of transient is below the given value.

b) These pins are for special use only and should not be used for other connections than specified. Pins operate with the internal generated core voltage.

Note See “Pinout Information” on page 9. for pin to group association.

- V_{DD5} is the supply voltage for the internal voltage regulators applied to pin V_{DD50}.
- V_{SS5} is the ground for the internal logic applied to pin V_{SS50}.
- A_{VDD} is the supply for analog part of the A/D converter.
- A_{VSS} is the ground for the analog part of the A/D converter.
- BV_{DD5} is the supply voltage for the I/O buffers applied to pins BV_{DD5x}.
- BV_{SS5} is the ground for the I/O buffers applied to pins BV_{SS5x}.
- SMV_{DD5} is the supply voltage for the I/O buffers of the stepper motor drivers applied to pins SMV_{DD5x}.
- SMV_{SS5} is the ground for the I/O buffers of the stepper motor drivers applied to pins SMV_{SS5x}.

Table 3-2 Absolute maximum ratings currents

Parameter		Symbol	Test Conditions	Ratings average [a]	Ratings peak [b]	Unit
Output current low	1 pin	I_{OL1}	Groups 1, 3A, 3B, 3C, 3D	30	50	mA
	All pins	I_{OLA1}	Group 1	50	100	mA
	All pins	I_{OLA3A}	Group 3A	50	100	mA
	All pins	I_{OLA3B}	Group 3B	50	100	mA
	All pins	$I_{OLA13AB}$	Sum of groups 1, 3A, 3B	100	200	mA
	All pins	I_{OLA3C}	Group 3C	50	100	mA
	All pins	I_{OLA3D}	Group 3D	50	100	mA
	All pins	I_{OLA3CD}	Sum of Groups 3C, 3D	100	200	mA
	1 pin	I_{OL4}	Group 4A	45	55	mA
	All pins	I_{OLA4A}		200	270	mA
	1 pin	I_{OL4}	Group 4B	45	55	mA
	All pins	I_{OLA4B}		200	270	mA
Output current high	1 pin	I_{OH1}	Groups 1, 3A, 3B, 3C, 3D	-30	-50	mA
	All pins	I_{OHA1}	Group 1	-50	-100	mA
	All pins	I_{OHA3A}	Group 3A	-50	-100	mA
	All pins	I_{OHA3B}	Group 3B	-50	-100	mA
	All pins	I_{OHA13B}	Sum of Groups 1, 3A, 3B	-100	-200	mA
	All pins	I_{OHA3C}	Group 3C	-50	-100	mA
	All pins	I_{OHA3D}	Group 3D	-50	-100	mA
	All pins	I_{OH3CD}	Sum of Groups 3C, 3D	-100	-200	mA
	1 pin	I_{OH4A}	Group 4A	-45	-55	mA
	All pins	I_{OHA4A}		-200	-270	mA
Output current high	1 pin	I_{OH4}	Group 4B	-45	-55	mA
	All pins	I_{OHA4B}		-200	-270	mA

a) Currents are averaged current over the given life time. Transient currents are not relevant as long as the average of transient is below the given value.

b) The peak current sets the limit for short term current flows.

3.1 Conditions for Extended Operating Temperature Range: T_A = -40 ~ 105°C

Caution

1. For any device's operation within the extended operating temperature range (T_A = -40 ... +105°C), the device's total power consumption must be reduced. The following tables of this chapter describe additional device conditions securing the requested decrease of the device's power consumption.
2. In case any device may operate within the extended operating temperature range (T_A = -40 ... +105°C) all of the below mentioned conditions must never be exceeded at any time.
3. All of the below mentioned device conditions must be applied in addition to any other parameter that is described within this document

Condition 1: T_A = -40 ... +105°C,

Operation Modes: RUN, HALT, IDLE

Power dissipation: < 0.52W

Duration: 15000 hours

V_{SS5} = 0V

Condition 2: T_A = -40 ... +105°C,

Operation Modes: WATCH, Sub-WATCH, STOP, Sub-Clock CPU Operation

Power dissipation: < 0.5W

Duration: 15 years

V_{SS5} = 0V

Table 3-3 Absolute maximum ratings currents 105°C

Parameter		Symbol	Test Conditions		Ratings average	Unit
Output current low	All pins	I_{OLA}	Sum of Groups 1, 3, 5	f_{sys} = 16MHz	100	mA
Output current high		I_{OHA}			-100	mA
Number of active stepper motor driver					4	

Chapter 4 General Characteristics

4.1 Requirements for external power supply connections

The user has to ensure a low resistive connection of

- all VSS pins on the PCB. This specification denotes this as:
  $V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0$ V
  in the further text.
- the V_{DD50} pin.
- all BV_{DD5x} pins.
- all SMV_{DD5x} pins.

4.2 Capacitance connected to REGC0

The Device requires to connect a capacitor with the following parameters to the pin REGC0. The pin REGC0 must not be connected externally.

Table 4-1 External Capacitance Requirement

Parameter	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Capacitance	C_{REG}		3.3	4.7	10	µF
ESR of capacitance	C_{ESR}	F0 = 100kHz			0.6	Ω

4.3 Main Oscillator Characteristics

Conditions

T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note

1. Refer to *"Power On Clear" on page 57* for further functional restriction.
2. A ceramic or crystal resonator has to be connected to the main clock input pins as shown in *Figure 4-1*.
3. External clock supply is not possible in user mode due to oscillator circuit limitation.

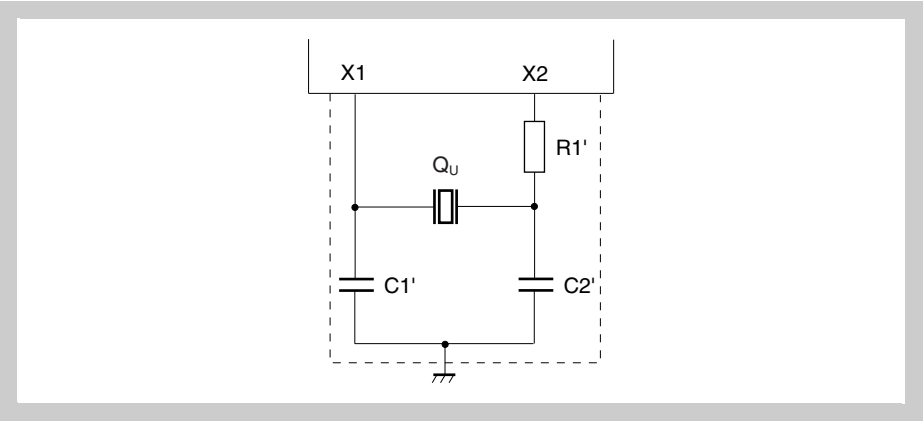


Figure 4-1 Recommended Main Oscillator Circuit

Note Values of C_1, C_2 and R depend on the used crystal or resonator and must be specified in cooperation with crystal/resonator manufacturer.

Caution

1. External clock input is prohibited.
2. When using the main system clock oscillator, wire as shown in above figure. This will avoid an adverse effect from wiring capacitance.
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with other signal lines.
   - Do not route this circuit close to a signal line with high fluctuating current flow.
   - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
   - Do not ground the capacitor to a ground pattern with high current flow.
   - Do not fetch signals from the oscillator.

Table 4-2 Main Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			16 [a]	ms
X1, X2 Oscillator Frequency	f_{OSC}		3.6	4.0	4.4	MHz

a) T_{OST} depends on the external crystal. Shorter timing might be found by evaluation.

Remark This value is valid for crystal operation only.

Table 4-3 Main Oscillator Characteristics - Crystal Type NDK LN-G8-1404

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			10[a]	ms
X1, X2 Oscillator Frequency	f_{OSC}		3.6	4.0	4.4	MHz

a) The given oscillation stabilization time is valid exclusively in case the below mentioned crystal-type from the manufacturer NDK is used for the main-oscillator operation. Beside the application of this specific crystal type, the PCB-design and capacitance configuration must ensure proper operation of the crystal enbling a load capacitance of about CL=12 pF. This parameter has to be verified by a dedicated crystal-evaluation based on the final PCB.

NDK Spec. No.: LN-G8-1404
Holder: AT-51GW
Frequency: 4.000 MHz

4.4 Sub-Oscillator Characteristics

Conditions T_A = -40 ~ +85°C,

BV_{DD5} = 3.0 V ~ 5.5 V,

AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,

V_{DD5} = 3.2 V ~ 5.5 V, (see *"Power On Clear" on page 57* for further functional restriction),

$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note
1. Refer to *"Power On Clear" on page 57* for further functional restriction.
2. A crystal resonator has to be connected to the sub clock input pins as shown in *Figure 4-2*.
3. External clock supply is not possible in user mode due to oscillator circuit limitation.

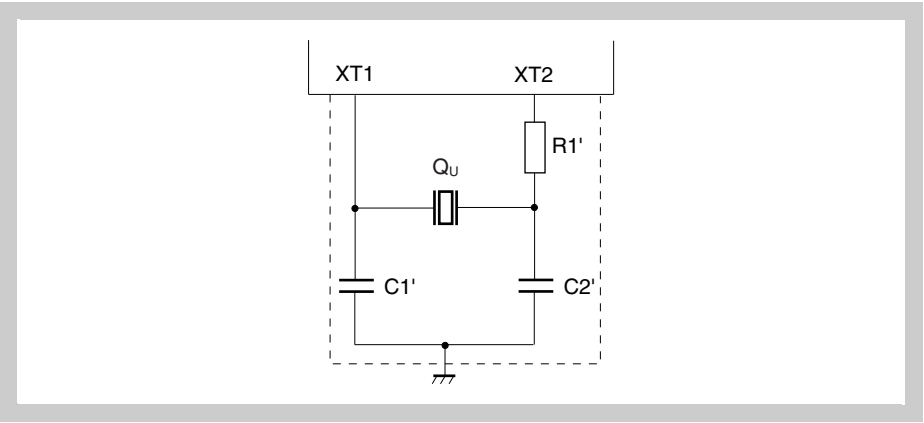


Figure 4-2 Recommended Sub Oscillator Circuit

Note Values of C_{S1}, C_{S2} and R_S depend on the used crystal and must be specified in cooperation with crystal manufacturer.

Caution
1. External clock input is prohibited.
2. When using the main system clock oscillator, wire as shown in above figure. This will avoid an adverse effect from wiring capacitance.
   - Keep the wiring length as short as possible.
   - Do not cross the wiring with other signal lines.
   - Do not route this circuit close to a signal line with high fluctuating current flow.
   - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
   - Do not ground the capacitor to a ground pattern with high current flow.
   - Do not fetch signals from the oscillator.

Table 4-4 Sub Oscillator Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ	Max	Unit
XT1,XT2 Oscillator Frequency	f_{SOSC}		32	32.768	35	KHz
Sub oscillator stabilization time	T_{SOST}				5 [a]	s

a) T_{SOST} depends on the external crystal. Shorter timing might be found by evaluation.

Remark These values are valid for crystal operation only.

4.5 Peripheral PLL Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 4-5 Peripheral PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL Startup Time	T_{PST}	OSC MODE			1.2	ms
PLL Output period jitter [a]	T_{PJ}	Peak to peak			1	ns
PLL Long term jitter [a]	T_{LJ}	Time = 20µs			2	ns

a) Not tested in production. Specified by design.

4.6 Spread Spectrum PLL Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 4-6 Spread Spectrum PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SSCG Startup Time	T_{SSCGST}	OSC MODE			1.2	ms
SSCG Frequency modulation range [a]	DITHER	OSC MODE, dither setting 3%	0		±4.2	%
		OSC MODE, dither setting 5%			±6.8	%
SSCG center frequency during dithering [a]	f_{DITHER}			1.0 * $f_{nominal}$		
SSCG modulation frequency [a]	f_{Mod}	SCFMC1-0 = [b] 01 10 11		 40 50 60		kHz

a) Not tested in production. Specified by design.
b) The typical modulation frequency can be selected by register SCFMC.

4.7 Ring Oscillator Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 4-7 Ring Oscillator Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ	Max	Unit
Ring Oscillator Frequency	f_{RING}		200	240	300	KHz
Ring oscillator Stabilization Time [a]	T_{ROST}				20	µs

a) Not tested in production. Specified by design.

4.8 I/O Capacitances

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 4-8 I/O Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Input/output capacitance, all I/O pins except group 4	C_{IO}				15	pF
Input/output capacitance Group 4	C_{IO4}				30	pF

Chapter 5 Operation Conditions

5.1 CPU Clock

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 5-1 CPU Clock Frequencies

Clock Mode	Prescale	Operation Mode	Device	CPU Operation Clock Frequency [MHz]
OSC mode	n/a	all modes	all	4
OSC mode, PLL x8	1/2			16
OSC mode, SSCG x12	1/6			8
OSC mode, SSCG x16	1/4			16
OSC mode, SSCG x 12	1/2			24
OSC mode, Ring OSC	n/a			0.2
OSC mode, Sub OSC	n/a			0.032

5.2 Peripheral Clock

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 5-2 Peripheral Clock Frequencies

Clock	Clock Source	Max	Unit
PCLK0 - 1	Main OSC	4	MHz
	Main OSC, PLL x 8	16, 8	MHz
PCLK2 - 15	Main OSC	4, 2, ... , 1/2048	MHz

Table 5-2 Peripheral Clock Frequencies (Continued)

Clock	Clock Source	Max	Unit
IICLK	Main OSC	4	MHz
	Main OSC, PLL x8	32[a]	MHz
	Main OSC, SSCG		
SPCLK0 - 1	Main OSC	4	MHz
	Main OSC, PLL x8	16, 8[b]	MHz
	Main OSC, SSCG		
SPCLK2 - 15	Main OSC	4, 2 ... 1/2048	MHz
	Main OSC, SSCG		
FOUT (CLKOUT)	Main OSC, PLL x8	32	MHz
	Main OSC, SSCG	32[c]	MHz
	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
LCDCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WTCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WDTCLK	Main OSC	4	MHz
	Ring OSC	0.2	MHz
	Sub OSC	0.032	MHz
WCTCLK	Main OSC	4	MHz
	PCLK1	see PCLK1	MHz
TMCCLK	Main OSC	4	MHz
	PCLK1	see PCLK1	MHz

a) needs to be ensured by proper configuration of the IICLK divider.
b) needs to be ensured by proper configuration of the SPCLK divider.
c) needs to be ensured by proper configuration of the FOUT (CLKOUT) divider.

Chapter 6 DC Characteristics

6.1 General DC Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-1 General DC Characteristics

Parameter	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input leakage	1	I_{LI1}	0 <= V_I <= BV_{DD5}	-1		+1	µA
	2	I_{LI2}	0 <= V_I <= V_{DD50}	-1		+1	µA
	3	I_{LI3}	0 <= V_I <= V_{DD50}	-1		+1	µA
	4	I_{LIS}	0 <= V_I <= SMV_{DD5}	-10		+10	µA
	5	I_{LIA}	0 <= V_I <= AV_{DD}	-0.2		+0.2	µA

6.2 Injected Current Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-2 Injected Current Characteristics

Parameter	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Injected current per pin [a]	All, except 5	I_{INJ}		-2		+2	mA
Injected current per pin [a]	5	I_{INJ}	[b]	-2		+2	mA

a) The injected current will not be tested during production. Value will be verified by evaluation. The total current per pin group (injected plus operating) has to be in the limits of the absolute maximum ratings for output currents (values for output current low and output current high). The operation voltage must stay in the limits of the operating conditions. The user has to make sure that the injected current does not pull the supplied voltage outside of the operating conditions.

b) The accuracy of the ADC specified in this document is only valid when the sum of all currents of pin group 5 is in the range of -14mA and +14mA.

6.3 Pin Group 1

Pin Group 1x: Pins supplied by BV_{DD5}
P00-P03, P16-P17, P30-P31, P46-P47, P50-P51

(1) Normal Voltage Operation

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 4.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-3 Pin Group 1 - Normal Voltage Operation

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	1	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2		V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	1	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2		V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	1	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2		V_{IL2}		0		0.5 BV_{DD5}	V
	CMOS1	1	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2		V_{IL4}		0		0.5 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	1	V_{HY1}		150			mV
	Schmitt2		V_{HY2}		150			mV
Output voltage high	Limit1	1	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
	Limit2		V_{OH}	I_{OH} = -5.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2		V_{OL}	I_{OL} = 5.0 mA			0.45	V
Maximum output short circuit current high	Limit1	1	I_{OHM1}	V_{OH} = 0 V	-2		-12	mA
	Limit2		I_{OHM2}		-5		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	2		12	mA
	Limit2		I_{OLM2}		5		30	mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

(2) Low Voltage Operation

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 4.0 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-4 Pin Group 1 - Low Voltage Operation

Parameter	Pin mode [a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	1	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2		V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	1	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2		V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	1	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2		V_{IL2}		0		0.35 BV_{DD5}	V
	CMOS1	1	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2		V_{IL4}		0		0.5 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	1	V_{HY1}		100			mV
	Schmitt2		V_{HY2}		100			mV
Output voltage high	Limit1	1	V_{OH}	I_{OH} = -1.0 mA	BV_{DD5} - 0.45			V
	Limit2	1	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	1	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2	1	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	1	I_{OHM1}	V_{OH} = 0 V	-1			mA
	Limit2		I_{OHM2}		-2			mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	1			mA
	Limit2		I_{OLM2}		2			mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

6.4 Pin group 2: $\overline{\text{RESET}}$ and FLMD0

Pin Group 2: Pins supplied by V_{DD50}
2: ($\overline{\text{RESET}}$, FLMD0)

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-5 Pin Group 2 - Normal Voltage Operation

Parameter	Pin mode	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	2	V_{IH1}		0.7 V_{DD50}		V_{DD50}	V
Input voltage low	Schmitt1	2	V_{IL1}		0		0.3 V_{DD50}	V

6.5 Pin Group 3: GPIO and LCD Controller

Pin Group 3: GPIO and LCD Controller supplied by BV_{DD5}
3A: P20-P24
3B: P20-P27, P34-P37, P60-P67
3C: P32, P43-P45, P80-P83, P85-P87, P104-P107
3D: P90-P97

Caution Do not operate buffers of pin group 3 in current limit state, when the LCD function is used. Failing to do so may lead to a decreased accuracy of the LCD waveforms.

(1) Normal Voltage Operation

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 4.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-6 Pin Group 3 - Normal Voltage Operation

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	3	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2		V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	3	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2		V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	3	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2		V_{IL2}		0		0.5 BV_{DD5}	V
	CMOS1	3	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2		V_{IL4}		0		0.5 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	3	V_{HY1}		150			mV
	Schmitt2		V_{HY2}		150			mV
Output voltage high	Limit1	3	V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
	Limit2		V_{OH}	I_{OH} = -5.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	3	V_{OL}	I_{OL} = 2.0 mA			0.45	V
	Limit2		V_{OL}	I_{OL} = 5.0 mA			0.45	V

Table 6-6 Pin Group 3 - Normal Voltage Operation

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Maximum output short circuit current high	Limit1	3	I_{OHM1}	V_{OH} = 0 V	-2		-12	mA
	Limit2		I_{OHM2}		-5		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	2		12	mA
	Limit2		I_{OLM2}		5		30	mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

(2) Low Voltage Operation

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 4.0 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-7 Pin Group 3 - Low Voltage Operation

Parameter	Pin mode[a]	Pin Group	Symbol	Test Conditions	Min.	Typ	Max.	Unit
Input voltage high	Schmitt1	3	V_{IH1}		0.7 BV_{DD5}		BV_{DD5}	V
	Schmitt2		V_{IH2}		0.8 BV_{DD5}		BV_{DD5}	V
	CMOS1	3	V_{IH3}		0.7 BV_{DD5}		BV_{DD5}	V
	CMOS2		V_{IH4}		0.8 BV_{DD5}		BV_{DD5}	V
Input voltage low	Schmitt1	3	V_{IL1}		0		0.3 BV_{DD5}	V
	Schmitt2		V_{IL2}		0		0.35 BV_{DD5}	V
	CMOS1	3	V_{IL3}		0		0.3 BV_{DD5}	V
	CMOS2		V_{IL4}		0		0.5 BV_{DD5}	V
Input hysteresis [b]	Schmitt1	3	V_{HY1}		100			mV
	Schmitt2		V_{HY2}		100			mV
Output voltage high	Limit1	3	V_{OH}	I_{OH} = -1.0 mA	BV_{DD5} - 0.45			V
	Limit2		V_{OH}	I_{OH} = -2.0 mA	BV_{DD5} - 0.45			V
Output voltage low	Limit1	3	V_{OL}	I_{OL} = 1.0 mA			0.45	V
	Limit2		V_{OL}	I_{OL} = 2.0 mA			0.45	V
Maximum output short circuit current high	Limit1	3	I_{OHM1}	V_{OH} = 0 V	-1		-12	mA
	Limit2		I_{OHM2}		-2		-30	mA
Maximum output short circuit current low	Limit1		I_{OLM1}	V_{OL} = BV_{DD5}	1		12	mA
	Limit2		I_{OLM2}		2		30	mA

a) CMOS1, CMOS2, Schmitt1 and Schmitt2 denote the non-schmitt and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
Limit1 and Limit2 denote the two output characteristics with current limit functionality of the device pins. The characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design

6.6 ADC Input

This chapter describes the digital functions available at the pins supplied by AVDD.

Pin Group 5: Pins supplied by AV_{DD5}
P70 .. P77

(1) Normal Voltage Operating

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-8 Pin Group 5 - Normal Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 AV_{DD5}		AV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 AV_{DD5}		AV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 AV_{DD5}	V
	Schmitt2	V_{IL2}		0		0.5 AV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{HI2}		150			mV

a) Schmitt1 denotes the schmitt trigger input characteristics of the device pins.
b) Not tested in production. Specified by design.

(2) Low Voltage Operation

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 4.0 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-9 Pin Group 5 - Low Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 AV_{DD5}		AV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 AV_{DD5}		AV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 AV_{DD5}	V
	Schmitt2	V_{IL2}				0.35 AV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{HI2}		150			mV

a) Schmitt1 denotes the schmitt trigger input characteristics of the device pins.
b) Not tested in production. Specified by design.

6.7 LCD Common and Segment Lines

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 4.5 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-10 DC Characteristics LCD Common and Segment Lines

Parameter	Symbol	TestConditions	Min.	Typ	Max	Unit
LCD Segment Output Voltage (unloaded)	V_{ODS}	IO = ±1µA	V_{LCDn} - 0.2	V_{LCDn}[a]	V_{LCDn} + 0.2	V
LCD Common Output Voltage (unloaded)	V_{ODC}	IO = ±1µA	V_{LCDn} - 0.2	V_{LCDn}	V_{LCDn} + 0.2	V
LCD split voltage[b]	V_{LC0}	IO = ±1.5 mA	V_{LCD0} - 0.1	V_{LCD0}	V_{LCD0} + 0.1	V
	V_{LC1}	IO = ±1.0 mA	V_{LCD1} - 0.1	V_{LCD1}	V_{LCD1} + 0.1	V
	V_{LC2}	IO = ±1.0 mA	V_{LCD2} - 0.1	V_{LCD2}	V_{LCD2} + 0.1	V
	V_{LC3}	IO = ±1.5 mA	V_{LCD3} - 0.1	V_{LCD3}	V_{LCD3} + 0.1	V
LCD Series resistance[c]	R_{LCDS}	Segment lines, V_{LCDn} to pin			1.8	kΩ
	R_{LCDC}	Common lines, V_{LCDn} to pin			1.8	kΩ
LCD operation current	IDD_{LCD}	f_{frame}=244Hz, All segment and common lines set to LCD mode and open			200	µA

a) VLCDn (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.
b) The split voltage is an internal design value. Direct measurement is not possible.
c) The Series resistance is an internal design value. Direct measurement is not possible.

Note The power supply configuration is restricted, when the LCD is used. The LCD voltages are generated centrally.

VLCDn	Voltage
VLCD0	BV_{DD5}
VLCD1	2/3 x BV_{DD5}
VLCD2	1/3 x BV_{DD5}
VLCD3	0 x $BV_{DD5} = BV_{SS5}$

6.8 Stepper Motor Driver IO

Pin Group 4: Stepper Motor outputs supplied by SMV_{DD5}
4A: P120-P127
4B: P130-P137

(1) Normal Voltage Operation

(a) Input Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 4.0 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-11 DC Characteristics Stepper Motor Driver Input - Normal Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 SMV_{DD5}		SMV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 SMV_{DD5}		SMV_{DD5}	
	CMOS1	V_{IH3}		0.7 SMV_{DD5}		SMV_{DD5}	V
	CMOS2	V_{IH4}		0.8 SMV_{DD5}		SMV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 SMV_{DD5}	V
	Schmitt2	V_{IL2}		0		0.5 SMV_{DD5}	
	CMOS1	V_{IL3}		0		0.3 SMV_{DD5}	V
	CMOS2	V_{IL4}				0.5 SMV_{DD5}	
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		150			mV
	Schmitt2	V_{HI2}		150			mV

a) CMOS1 and Schmitt1 denote the non-schmitt trigger and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.
b) Not tested in production. Specified by design.

(b) Output Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 4.75 V ~ 5.25 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-12 DC Characteristics Stepper Motor Driver Output - Normal Voltage Operation

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High		V_{OH}	I_{OH} = -40 mA, T_A= -40°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
		V_{OH}	I_{OH} = -30 mA, T_A= +25°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
		V_{OH}	I_{OH} = -27 mA, T_A= +85°C	SMV_{DD5} - 0.5		SMV_{DD5}	V
Output Voltage Low		V_{OL}	I_{OL} = 40 mA, T_A= -40°C	0		0.5	V
		V_{OL}	I_{OL} = 30 mA, T_A= +25°C	0		0.5	V
		V_{OL}	I_{OL} = 27 mA, T_A= +85°C	0		0.5	V
Output voltage deviation [a]		V_{DEV}		0		50	mV
Output Slew rate [b]		t_{RF}	10% - 90%	12	25	70	ns
Peak Cross Current[c]		I_{CROSS}				50	mA
Output Pulse width[d]		t_{MO}		125			ns
Output Pulse length deviation[e]		t_{SMDEV}		-10	+5	+45	ns

a) Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (| V_{OHx} - V_{OHy} | , | V_{OLx} - V_{OLy} |) @ $I_{OHx} = I_{OHy}$, $I_{OLx}=I_{OLy}$.
x and y denote any combination of two pins of the following pin groups: (P120-123, P124-P127, P130-P133, P134-P137)

b) The slew rate is not tested, but derived from simulation.

c) The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transistion time t_{RF}. It flows in addition to the output current. The cross current is not tested, but derived from simulation.

d) The output buffer can not generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested, but derived from simulation.

e) The slew rate control function causes a deviation of output pulse time compared to the ideal selected output pulse setting. This value is not tested, but derived from simulation.

Caution The stepper output drivers have no current limitation and are not protected against short circuit.

(2) Low Voltage Operation

(a) Input Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4.0 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-13 DC Characteristics Stepper Motor Driver Input - Low Voltage Operation

Parameter	Pin mode [a]	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage High	Schmitt1	V_{IH1}		0.7 SMV_{DD5}		SMV_{DD5}	V
	Schmitt2	V_{IH2}		0.8 SMV_{DD5}		SMV_{DD5}	V
	CMOS1	V_{IH3}		0.7 SMV_{DD5}		SMV_{DD5}	V
	CMOS2	V_{IH4}		0.8 SMV_{DD5}		SMV_{DD5}	V
Input Voltage Low	Schmitt1	V_{IL1}		0		0.3 SMV_{DD5}	V
	Schmitt2	V_{IL2}				0.35 SMV_{DD5}	V
	CMOS1	V_{IL3}		0		0.3 SMV_{DD5}	V
	CMOS2	V_{IL4}				0.5 SMV_{DD5}	V
Input Voltage Hysteresis [b]	Schmitt1	V_{HI1}		100			mV
	Schmitt2	V_{HI2}		100			mV

a) CMOS1 and Schmitt1 denote the non-schmitt trigger and the two schmitt trigger input characteristics of the device pins. This characteristic can be selected bitwise by software.

b) Not tested in production. Specified by design.

(b) Output Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 4.75 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-14 DC Characteristics Stepper Motor Driver Output - Low Voltage Operation

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High		V_{OH}	I_{OH} = -5 mA,	SMV_{DD5} - 0.5		SMV_{DD5}	V
Output Voltage Low		V_{OL}	I_{OL} = +5 mA,	0		0.5	V

6.9 Current Limit Function of I/O buffers

The output buffers of the pin groups 1 incorporate a current limiting function. This function limits the output current of the buffer to a certain value during output signal switching.

The limit is disabled when the buffer output voltage is near to its target voltage, thus providing full drivability. During full drivability the current may reach values given in absolute maximum ratings for a single pin.

The user can select different limit ranges by software (see Functional Target Specification for details).

The limit function is independent from the operation mode of the device.

A permanent short circuit of outputs is not permitted.

The stepper motor driver outputs do not support a current limiting function.

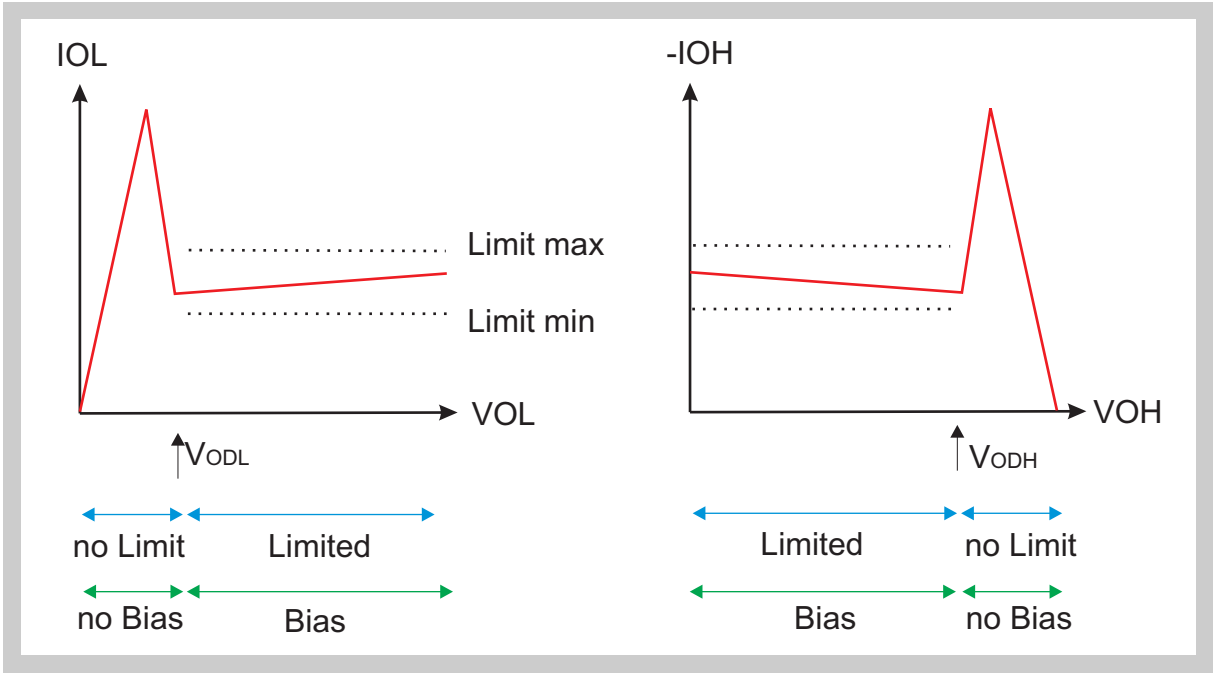


Figure 6-1 Current Limit Function Principle

Note The current limit function of the I/O buffers needs additional bias current to control the output stage. The additional bias current depend on the status of each buffer. Each buffer with either high or low output and in the stage of current limiting will draw this bias current.

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, (
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 6-15 DC Characteristics of Current Limiting Function [a]

Parameter	Pin mode	Symbol	Test Conditions	Min	Typ	Max	Unit
Limit disable threshold voltage for V_{OH}		V_{ODH}		VDDx[b] - 1.6		VDDx - 1.1	V
Limit disable threshold voltage for V_{OL}		V_{ODL}		1.1		1.6	V
Supply Current per buffer for current limitation [c]	Limit1	I_{DDCL1}				0.8	mA
	Limit2	I_{DDCL2}				1.7	mA

a) These values are not tested. They are given based on design simulation
b) VDDx denotes the corresponding voltage supply of the pin.
c) This current need not be considered during absolute maximum current calculation.

Note The function of the current limiting operation is sensitive against inductive loads under a certain condition:

- The load of the pin is below the selected current limit and the device could reach a sufficient output voltage. The device changed to full drivability.
- The external circuitry sinks/sources more and more current.
- The current creates an increasing voltage drop in the output stage of the device.
- The increasing voltage drop enables the current limiting function.
- The enabling of the current limit together with an external inductance may lead to an oscillation of the output between the limited and unlimited state. The external inductance creates voltage peaks that change the state of the output buffers current limiting function.
- Recommendation: keep external inductance small (keep external wiring short).

6.10 Supply Current

Table 6-16 DC Characteristics Supply Current µPD70F3417(A), µPD70F3416(A)[a]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_{DD13}	Operating (f_{CPU} = 24 MHz; SSCG,PLL: on)		40	55	mA
	I_{DD13}	Operating (f_{CPU} = 16 MHz; SSCG,PLL: on)		29	40	mA
	I_{DD13}	Operating (f_{CPU} = 8 MHz; SSCG,PLL: on)		18	25	mA
	I_{DD14}	Operating (f_{CPU} = 4 MHz; SSCG,PLL: off)		11	15	mA
	I_{DD15}	Operating (f_{CPU} = 32 kHz; SSCG,PLL: off)		0.5	0.8	mA
	I_{DD16}	Operating (f_{CPU} = RingOSC = 300 kHz; SSCG,PLL: off)		3.5	5.0	mA
	I_{DD21}	HALT Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		16	24	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 16 MHz; SSCG,PLL: on)		3.2	4.8	mA
	I_{DD5}	STOP		10	190	µA
	I_{DD6}	WATCH		150	350	µA
	I_{DD6A}	WATCH Monitored		165	390	µA
	I_{DD7}	SUB WATCH		50	200	µA
	I_{DD7A}	SUB WATCH Monitored		65	215	µA
	I_{DD7B}	SUB WATCH on RingOSC		65	215	µA

a) These values are target values without current consumption due to external circuitry at the IO-pins.

The low current modes (STOP, WATCH, SUB WATCH) are tested under the following conditions:

- Operation modes setting as described in table below.
- All functional pins with output possibility are set to output with alternating high and low output levels.
- Testequipment is disconnected from output pins.
- IDD is the total sum of currents to the device supply pins V_{DD5}, BV_{DD5}, SMV_{DD5}, AV_{DD}
- Device drives its own leakage currents by its output stages.
- The leakage current is included in the given IDD values.

Unit	Watch	Watch monitored	Sub Watch	Sub Watch on RingOSC	Sub Watch monitored	STOP
Main-oscillator	running	running	stopped	stopped	stopped	stopped
Sub-oscillator	stopped (XT1 clamped)	stopped (XT1 clamped)	running	stopped (XT1 clamped)	running	stopped
Ring-oscillator	stopped	running	stopped	running	running	stopped
SSCG	stopped	stopped	stopped	stopped	stopped	stopped
PLL	stopped	stopped	stopped	stopped	stopped	stopped
CPU system	stopped	stopped	stopped	stopped	stopped	stopped
IICCLK	stopped	stopped	stopped	stopped	stopped	stopped
PCLK0, PCLK1	stopped	stopped	stopped	stopped	stopped	stopped
PCLK2…PCLK15	stopped	stopped	stopped	stopped	stopped	stopped
SPCLK0, SPCLK1	stopped	stopped	stopped	stopped	stopped	stopped
SPCLK2…SPCLK15	stopped	stopped	stopped	stopped	stopped	stopped
FOUT	stopped	stopped	stopped	stopped	stopped	stopped
WTCLK	running	running	running	running	running	stopped
WDTCLK	stopped	stopped	stopped	stopped	stopped	stopped
TM0CLK	stopped	stopped	stopped	stopped	stopped	stopped
LCD	disabled	disabled	disabled	disabled	disabled	disabled
ADC	disabled	disabled	disabled	disabled	disabled	disabled
Regulator[a]	Standby	Standby	Standby	Standby	Standby	Standby

a) Regulator in standby: STBCTL = 0x03

Chapter 7 AC Characteristics

7.1 AC Test Input/Output Waveform

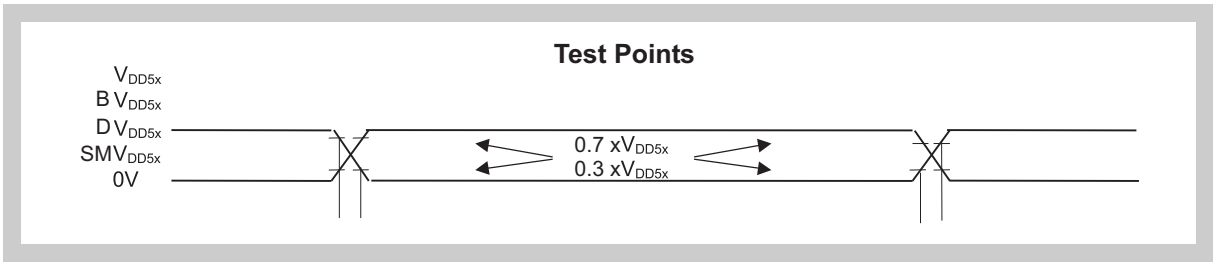


Figure 7-1 AC Test Input/Output Waveform

7.2 AC Test Load Condition

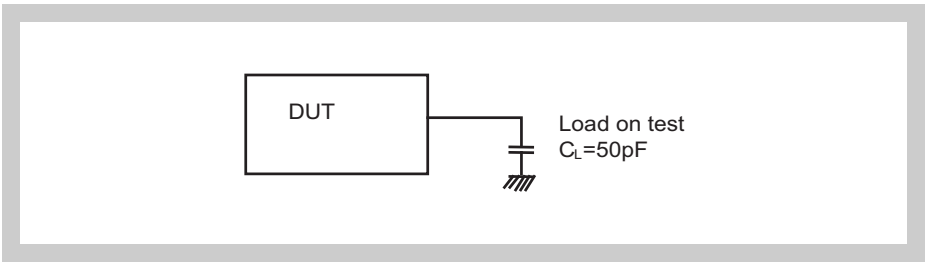


Figure 7-2 AC Test Load Condition

7.3 Reset

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 7-1 Reset AC Characteristics

Parameter	Symbol	Test Conditions	MIN.		MAX.	Unit
$\overline{\text{RESET}}$ high-level width [a]	t_{WRSH}		500			ns
$\overline{\text{RESET}}$ low-level width [b]	t_{WRSL}		500			ns
$\overline{\text{RESET}}$ Pulse rejection [c]	t_{WRRJ}		50			ns

a) This signal high time is needed to ensure that the internal RESET release operation starts.
b) This signal low time is needed to ensure that the internal RESET is activated.
c) The RESET input incorporates an analog filter. Pulses shorter than this minimum will be ignored. Not tested in production.

Note Reset pulses shorter than the given value may not be recognized by the device, they do not cause undefined states of the device.

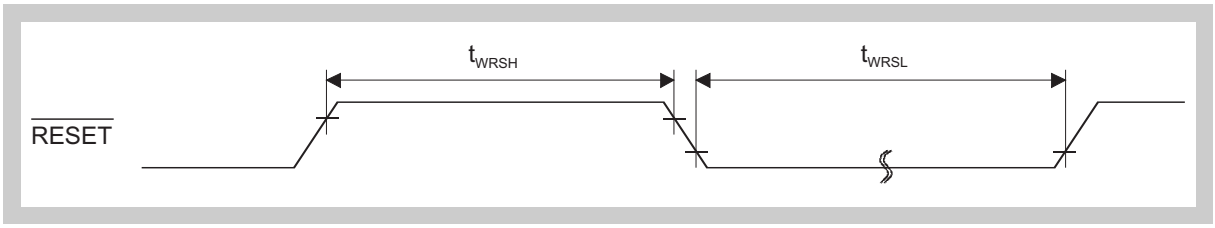


Figure 7-3 Reset Timing

7.4 Interrupt Timing

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 7-2 Interrupt AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NMI high-level width [a]	t_{NIH}		360			ns
NMI low-level width [a]	t_{NIL}		360			ns
NMI pulse rejection [b]	t_{NIRJ}		50		360	ns
INTPn[c] high-level width [a]	t_{ITH}		360			ns
INTPn[c] low-level width [a]	t_{ITL}		360			ns
INTPn[c] pulse rejection [b]	t_{ITRJ}		50		360	ns

a) Pulses longer than this value will pass the input filter.
b) Pulses shorter than this value do not pass the input filters. Not tested in production.
c) n = 7…0

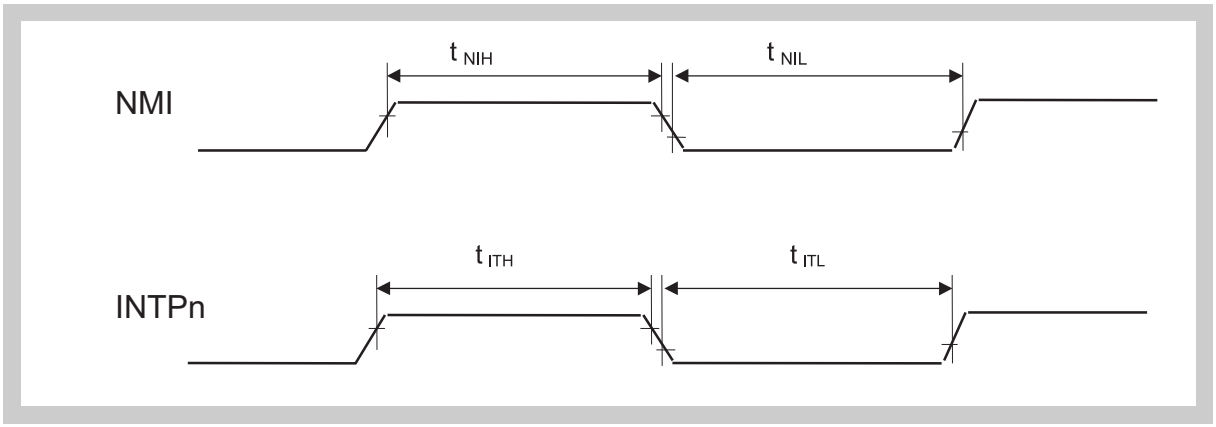


Figure 7-4 Interrupt Timing

Note Interrupt timing is generated by analog delay elements. Delay characteristics have a wide range in production.

7.5 Peripheral Function Characteristics

The following conditions are valid for all peripheral function characteristics unless otherwise noted.

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

7.5.1 Timer P

Table 7-3 Timer P AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TIPmn[a] high-level width	t_{TIPHD}	Digital filter	45 +3/f_{PCLK0}[b]			ns
	t_{TIPHNB}	No digital filter, react on both edge	45 +2/f_{PCLK0}			ns
	t_{TIPHNS}	No digital filter, react on single edge	45 +1/f_{PCLK0}			ns
TIPmn [a] low-level width	t_{TIPL}	Digital filter	45 +3/f_{PCLK0}			ns
	t_{TIPLNB}	No digital filter, react on both edge	45 +2/f_{PCLK0}			ns
	t_{TIPLNS}	No digital filter, react on single edge	45 +1/f_{PCLK0}			ns

a) m = 0, n = 1…0
b) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

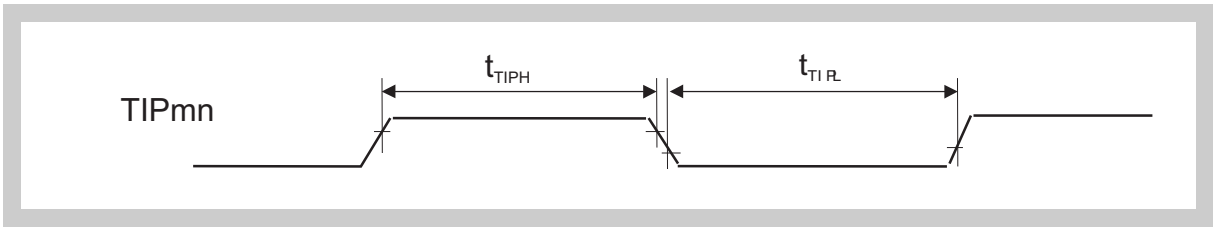


Figure 7-5 Timer P Input Timing

7.5.2 Timer G

Table 7-4 Timer G Input Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TIGmn[a] high-level width	t_{TIGH1}	Digital filter, f_{PCLK0}[b] = f_{CCLK}[c]	45 + 3/f_{PCLK0}			ns
	t_{TIGH2}	Digital filter, $f_{PCLK0} > f_{CCLK}$	45 + 2/f_{CCLK}			ns
	t_{TIGH0}	No digital filter	45 + 2/f_{CCLK}			ns
TIGmn[a] low-level width	t_{TIGL1}	Digital filter, $f_{PCLK0} = f_{CCLK}$	45 + 3/f_{PCLK0}			ns
	t_{TIGL2}	Digital filter, $f_{PCLK0} > f_{CCLK}$	45 + 2/f_{CCLK}			ns
	t_{TIGL0}	No digital filter	45 + 2/f_{CCLK}			ns

a) m = 0…1: n = 1…4; m = 2: n = 0...5
b) f_{SPCLK0} is the clock frequency of the digital filter connected to the input pin.
c) f_{CCLK} is the count clock frequency of the Timer G.

7.5.3 UARTA

Table 7-5 UARTA AC Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Unit
Transfer rate	T_{UARTA}		0.3	1000	Kbps

7.5.4 CAN

Table 7-6 CAN AC Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	f_{CAN}[a] ≥ 8 MHz		1	Mbps

a) f_{CAN} is the CAN macro clock frequency. For CAN clock selection refer to functional specification of the CAN.

7.5.5 CSI B (High Voltage Operation)

Conditions As specified at start of chapter *7.5 on page 46*.

(1) CSIB Master Mode

(a) With Digital Filter

Table 7-7 CSIB Master Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{SCKBn}$ high level width	t_{KH1}		$0.5\ t_{KCY1}$ - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		$0.5\ t_{KCY1}$ - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		$50 + 4/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		$-31 - 4/f_{PCLK0}$		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			6	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-8 CSIB Master Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		125		ns
$\overline{SCKBn}$ high level width	t_{KH1}		$0.5\ t_{KCY1}$ - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		$0.5\ t_{KCY1}$ - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		50		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-31		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			6	ns

Note n = 0…1

(2) CSIB Slave Mode

(a) With Digital Filter

Table 7-9 CSIB Slave Mode AC Characteristics with Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		$4/f_{PCLK0}$ - 5		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		$4/f_{PCLK0}$ - 5		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		$15 + 2/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		$5 + 2/f_{PCLK0}$		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			$45 + 3/f_{PCLK0}$	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-10 CSIB Slave Mode AC Characteristics without Digital Filter

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{\text{SCKBn}}$ cycle time	t_{KCY1}		125		ns
$\overline{\text{SCKBn}}$ high level width	t_{KH1}		50		ns
$\overline{\text{SCKBn}}$ low level width	t_{KL1}		50		ns
SIBn setup time (to $\overline{\text{SCKBn}}$)	t_{SIK1}		15		ns
SIBn hold time (from $\overline{\text{SCKBn}}$)	t_{KSI1}		5		ns
Delay time from $\overline{\text{SCKBn}}$ to SOBn	t_{KSO1}			45	ns

Note n = 0…1

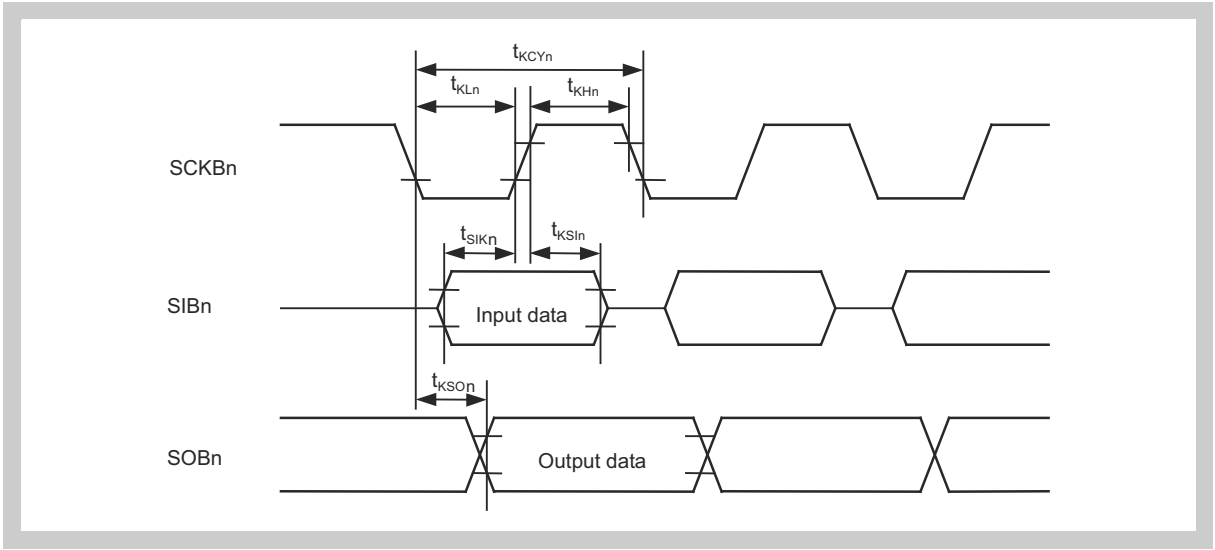


Figure 7-6 CSI Master/Slave Mode Timing

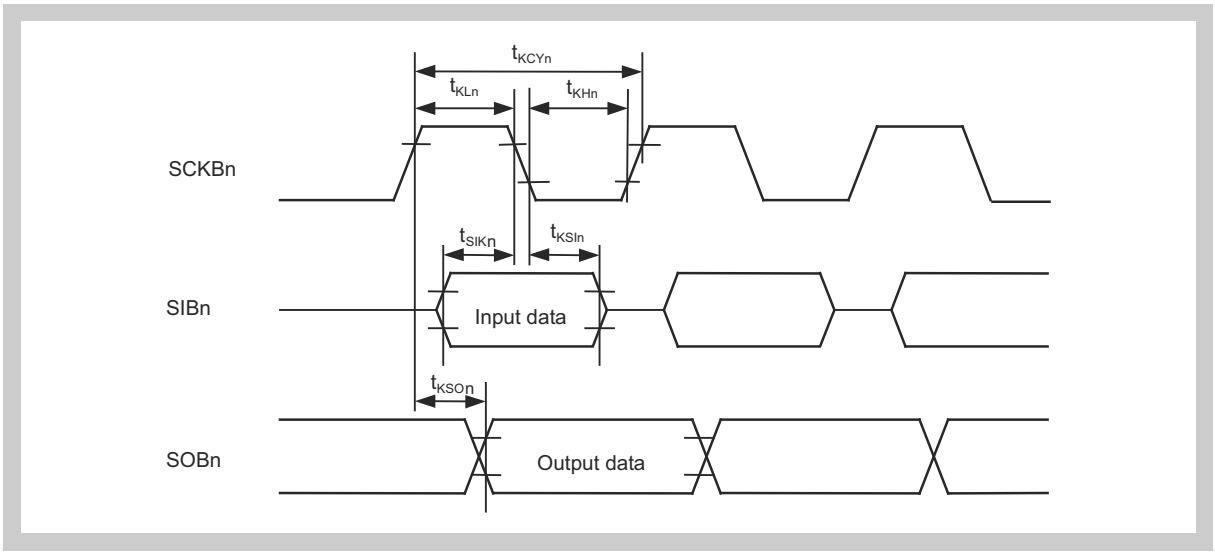


Figure 7-7 CSI Master/Slave Mode Timing Inverted Clock

7.5.6 CSIB (Low Voltage Operation)

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 4.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V, ‘
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *“Power On Clear“ on page 57* for further functional restriction.

(1) CSIB Master Mode - Low Voltage Operation

(a) With Digital Filter

Table 7-11 CSIB Master Mode AC Characteristics with Digital Filter - Low Voltage Operation

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		93 + $4/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-49 - $4/f_{PCLK0}$		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			45	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-12 CSIB Master Mode AC Characteristics without Digital Filter - Low Voltage Operation

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		125		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 80		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 80		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		93		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		-49		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			45	ns

Note n = 0…1

(2) CSIB Slave Mode - Low Voltage Operation

(a) With Digital Filter

Table 7-13 CSIB Slave Mode AC Characteristics with Digital Filter - Low Voltage Operation

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		$8/f_{PCLK0}$		ns
$\overline{SCKBn}$ high level width	t_{KH1}		$4/f_{PCLK0}$ - 5		ns
$\overline{SCKBn}$ low level width	t_{KL1}		$4/f_{PCLK0}$ - 5		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		$15 + 2/f_{PCLK0}$ [a]		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		$5 + 2/f_{PCLK0}$		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			$100 + 3/f_{PCLK0}$	ns

a) f_{PCLK0} is the clock frequency of the digital filter connected to the input pin.

(b) Without Digital Filter

Table 7-14 CSIB Slave Mode AC Characteristics without Digital Filter - Low Voltage Operation

Parameter	Symbol	Test Conditions	Min	Max	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		125		ns
$\overline{SCKBn}$ high level width	t_{KH1}		50		ns
$\overline{SCKBn}$ low level width	t_{KL1}		50		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		15		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		5		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			100	ns

Note n = 0…1

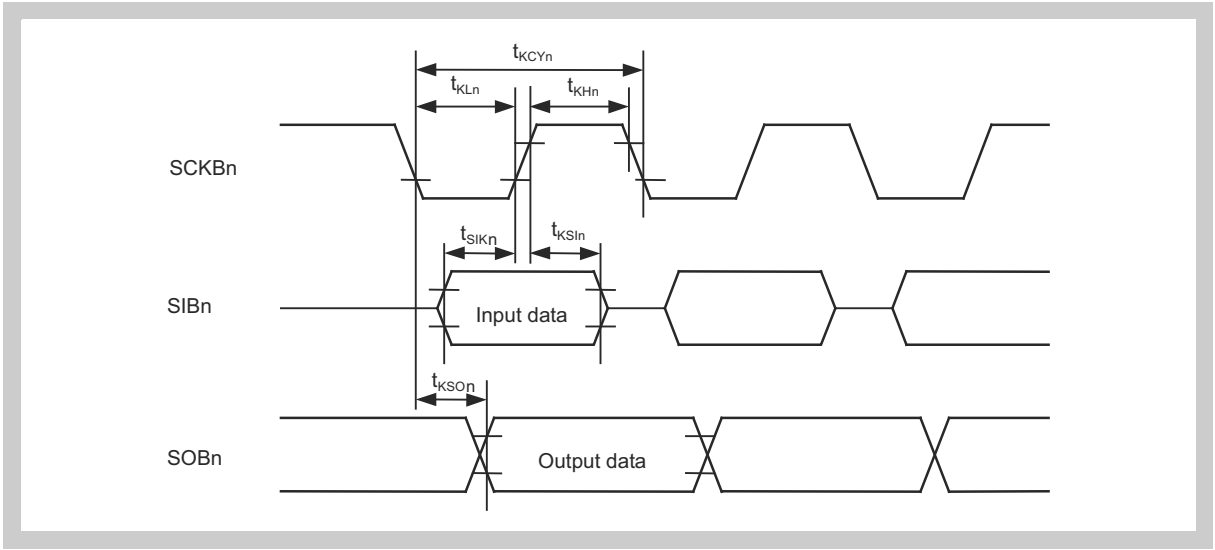


Figure 7-8 CSI Master/Slave Mode Timing - Low Voltage Operation

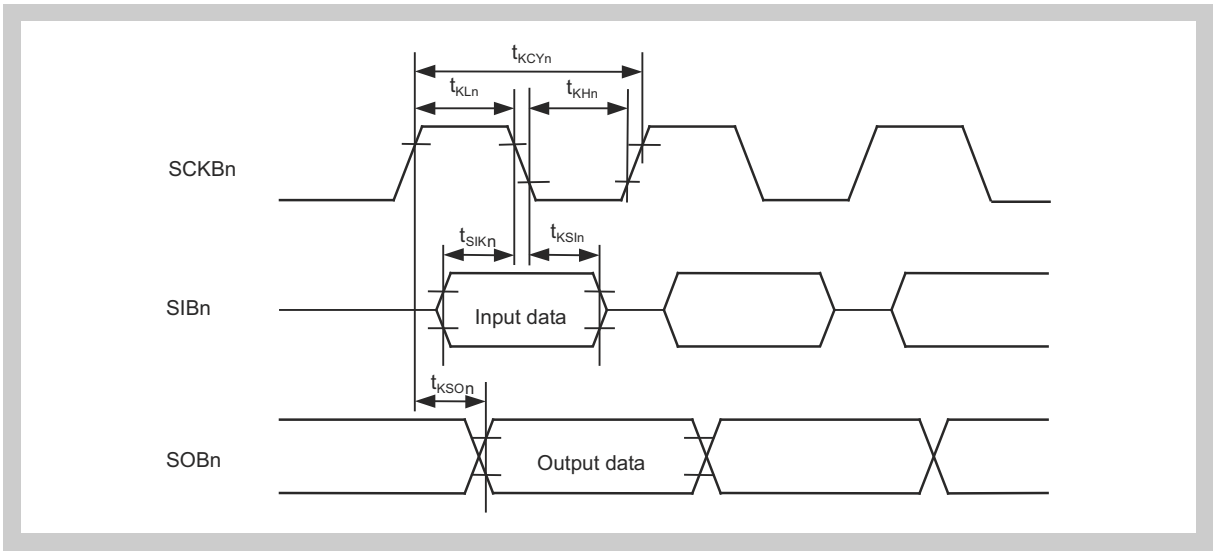


Figure 7-9 CSI Master/Slave Mode Timing Inverted Clock - Low Voltage Operation

7.5.7 I²C

Table 7-15: I²C AC Characteristics

Parameter		Symbol	Normal Mode		Fast-speed Mode		Unit
			min	max	min	max	
SCL0 clock frequency		f_{CLK}	0	100	0	381	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7	—	1.3	—	µs
Hold time[a]		$t_{HD:STA}$	4.0	—	0.6	—	µs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	µs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	µs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	µs
	I²C mode		0[b]	3.45 [c]	0[Note b]	0.9[c]	µs
Data setup time		$t_{SU:DAT}$	250	—	100[d]	—	ns
STOP condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	µs
Noise suppression [e]		t_{SP}				t_{IICLK}[f]	ns
Capacitive load of each bus line		C_b	—	400	—	400	pF

a) At the start condition, the first clock pulse is generated after the hold time

b) The system requires a minimum of 300ns hold time Internally for the SDA signal (at V_{IHmin} of SCL0 signal) in order to occupy the undefined area at the falling edge of SCL0.

c) If the system does not extend the SCL0 signal low hold time (t_{low}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

d) The fast-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the fast-speed-mode IIC bus so that It meets the following conditions:
- If the system does not extend the SCL0n signal's low state hold time: tSU:DAT>/=250ns
- If the system extends the SCL0n signal's low state hold time:
Transmit the following data bit to the SDA0 line prior to releasing the SCL0 line
(t_{Rmax}.+$t_{SU:DAT}$=1000+250=1250ns: Normal mode IIC bus specification).

e) Noise suppression is only available in Fast-speed mode.

f) t_{IICLK} is the period of the IICLK supplied by the clock controller.

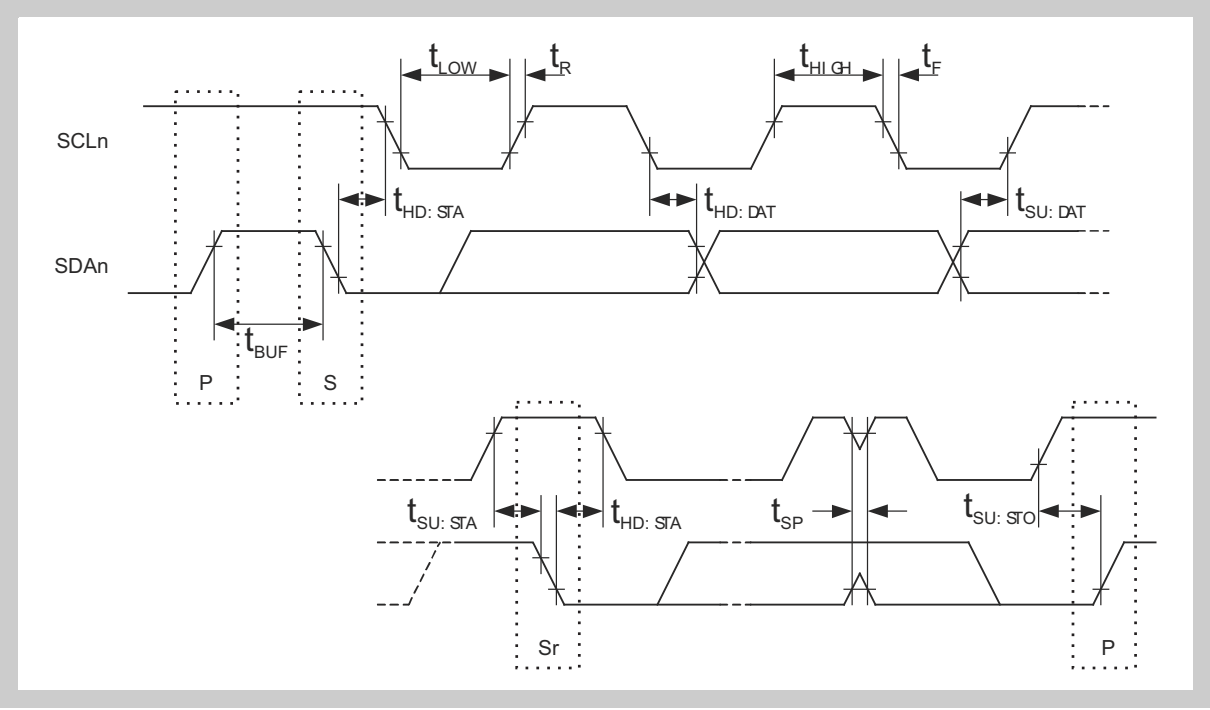


Figure 7-10 I^2C Timing

Remarks

1. P: Stop condition
2. S: Start condition
3. Sr: Restart condition
4. Rise and Fall time depend on the actual load of the signal and the selected output current limit. For a capacitive load the time can be roughly calculated from:
   ($t_R = V_{OH} / I_{OH} * C_L$),
   ($t_F = V_{OH} / I_{OL} * C_L$)

Chapter 8 Analog Functions

8.1 A/D Converter

8 channel input P70 - P77

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 8-1 A/D Converter Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution	-			10		Bit
Reference voltage	AVREF		AV_{SS}		AV_{DD}	V
Overall error [a]	-	$AV_{SS} \le AIN \le AV_{REF}$, $4.5V \le (AV_{REF} = AV_{DD}) \le 5.5V$			+/- 3.5	LSB
	-	$AV_{SS} \le AIN \le AV_{REF}$, $3.5V = AV_{REF}$, $4.0V \le AV_{DD} \le 5.5V$			+/- 10	LSB
Additional error due to disturbance by digital read of P70..P77 [b]	DRERR				1	LSB
Conversion time [c]	T_{CONV}		3.88		15.50	µs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Analogue supply current	I_{AVDD}				10	mA
Analog input equivalent circuit resistanceb)	R_{INA}		0.3		2.55	kΩ
Analog input equivalent circuit capacitanceb)	C_{INA}		4.0		8.0	pF
Analogue supply current	I_{AVDD}				10	mA
Reference voltage supply current [d]	I_{AVREF}				250	µA

a) Quantization error of ±0.5 LSB is not included
b) This value is not tested during production.
c) T_{CONV} depends on register setting
d) The reference current is mainly a transient current that is influenced by the conversion time. The given value is the maximum value. Value is not tested during production.

8.2 Power On Clear

Conditions T_A = -40 ~ +85°C,
V_{DD5} = 0 ~ 5.5 V,
V_{SS} = 0 V

Table 8-2 Power On Clear Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold Voltage	V_{IP}		3.2	3.35	3.5	V
Detection time [a]	T_{DETP}	V_{DD5} slope > 25mV/µs			2	µs

a) Not tested in production.

Note
1. The POC ensures that the devices stops operation (RESET condition) when the device is outside the operation voltage range, under the condition that the supply voltage slope on V_{DD5} is ≤ 25mV/µs.
2. Full device operation is only available, when the supply voltage is above the maximum threshold voltage. The device may stop operation due to reset condition generated by POC, if the supply voltage dropps below the given max threshold voltage.

Chapter 9 Memory Characteristics

9.1 Basic Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 3.2 V ~ 5.5 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 9-1 Memory Operation Characteristics

Parameter	Symbol	Device	Min	Typ	Max	Unit
Operation Frequency	f_{CPU}	µPD70F3416(A) µPD70F3417(A)	0.032		24	MHz

Note The above maximum operation frequency specification lists the center frequency of the SSCG. The maximum dithering range of the SSCG is assured for this center frequency.

9.2 Flash Memory Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 4.5 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 9-2 Flash Memory Programming Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Number of Rewrites	C_{WRT}					1000	times
Data retention	t_{RET}			15			years
Blank Check Time[a]	t_{IVBL4k}	One memoy block (4k)	f_{CPU} = 24 MHz		520	630	µs
	$t_{IVBL128k}$	32 memory blocks (128k)			9.12	10.94	ms
Erase Time	t_{IERT4k}	One memoy block (4k)			26.18	523.6	ms
	$t_{IERT128k}$	32 memory blocks (128k)			34.87	697.40	ms
Write Time	t_{IWRT4k}	Write two words[b]			300	900	µs
	$t_{IWRT128k}$	One memoy block (4k) @ 256 bytes			42.79	354.24	ms
Erase/Write Current [c]	I_{DDFL}				1	3	mA
Programming Temperature	t_{PRG}			-40		+65	°C
		maximum power dissipation 0.6W [d]		-40		+85	°C

a) Blank check of one memory block (4 kB).
b) Write of 2 words. The corresponding library call is configured for 2 word per call.
c) Additional current that is only needed during erase or write of flash.
d) The power dissipation may be reduced by disabling some functionality or reducing the CPU operation speed.

9.3 Special Conditions for End-of-Line Programming

Conditions T_A = +15 ~ +40°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 4.8 V ~ 5.15 V,
V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS} = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 9-3 Flash Memory End-of-Line Programming Characteristics (PG-FP4: CSI)

Parameter	Symbol	Device	Test Conditions	Min	Typ	Max	Unit
Blank Check	t_{IVBL}	µPD70F3417	W/E cycles ≤ 5, f_{CPU} = 24MHz		20	40	ms
		µPD70F3416			12	20	ms
Erase Time [a]	t_{IWRT}	µPD70F3417			0.1	0.3	s
		µPD70F3416			0.1	0.3	s
Write Time [b]	t_{IERT}	µPD70F3417			10	18	s
		µPD70F3416			6	10	s
Verify Time	t_{IVRT}	µPD70F3417			8	10	s
		µPD70F3416			4	5	s

a) Erase of all flash-memory blocks (0 .. 63)
b) Write of complete flash area.

Note All parameters were determined at: SIO @ 2.5MHz (max. comm. speed).

Table 9-4 Flash Memory End-of-Line Programming Characteristics (PG-FP4: UART)

Parameter	Symbol	Device	Test Conditions	Min	Typ	Max	Unit
Blank Check	t_{IVBL}	µPD70F3417	W/E cycles ≤ 5, f_{CPU} = 24MHz		20	40	ms
		µPD70F3416			12	20	ms
Erase Time [a]	t_{IWRT}	µPD70F3417			0.1	0.3	s
		µPD70F3416			0.1	0.3	s
Write Time [b]	t_{IERT}	µPD70F3417			21	30	s
		µPD70F3416			11	16	s
Verify Time	t_{IVRT}	µPD70F3417			20	25	s
		µPD70F3416			10	12	s

a) Erase of all flash-memory blocks (0 .. 63)
b) Write of complete flash area.

Note All parameters were determined at: UART @ 153600baud.

Table 9-5 Flash Memory End-of-Line Programming Characteristics (Flash-Selfprogramming)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Blank Check One memory block (4k)	t_{IVBL4k}	W/E cycles ≤ 5, f_{CPU} = 24MHz		0.52	0.63	ms
Blank Check 32 memory blocks (128k)	$t_{IVBL128k}$			9.12	10.94	ms
Erase Time One memory block (4k)	t_{IERT4k}			26.18	104.72	ms
Erase Time 32 memory blocks (128k)	$t_{IERT128k}$			34.87	139.48	ms
Write Time Write two words [a]	t_{IWRT}			0.30	0.43	ms
Write Time: One memory block (4k) @ 256 Bytes [b]	t_{IWRT4k}			42.79	112.00	ms
Verify Time: One memory block (4k)	t_{IVRT4k}			17.13	20.55	ms
Verify Time: 32 memory blocks (128k)	$t_{IVRT128k}$			541.20	649.44	ms

a) The corresponding library call is configured for 2 words per call.
b) The corresponding library call uses a 256 Bytes (64 words) source buffer.

9.4 Serial Write Operation Characteristics

Conditions T_A = -40 ~ +85°C,
BV_{DD5} = 3.0 V ~ 5.5 V,
AV_{DD} = 3.2 V ~ 5.5 V, SMV_{DD5} = 3.2 V ~ 5.5 V,
V_{DD5} = 4.5 V ~ 5.5 V,
$V_{SS5} = BV_{SS5} = SMV_{SS5} = AV_{SS}$ = 0 V

Note Refer to *"Power On Clear" on page 57* for further functional restriction.

Table 9-6 Flash Memory AC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
FLMD0 setup time to rising edge of $\overline{\text{RESET}}$	t_{MDSET}		2			ms
Count start time from rising edge of $\overline{\text{RESET}}$ to FLMD0	t_{RFCF}		0.8			ms
Count execution time	t_{COUNT}		20			ms
FLMD0 counter High/Low level width	t_{CH},t_{CL}		10		100	µs
FLMD0 counter rise/fall time	t_R,t_F				50	ns

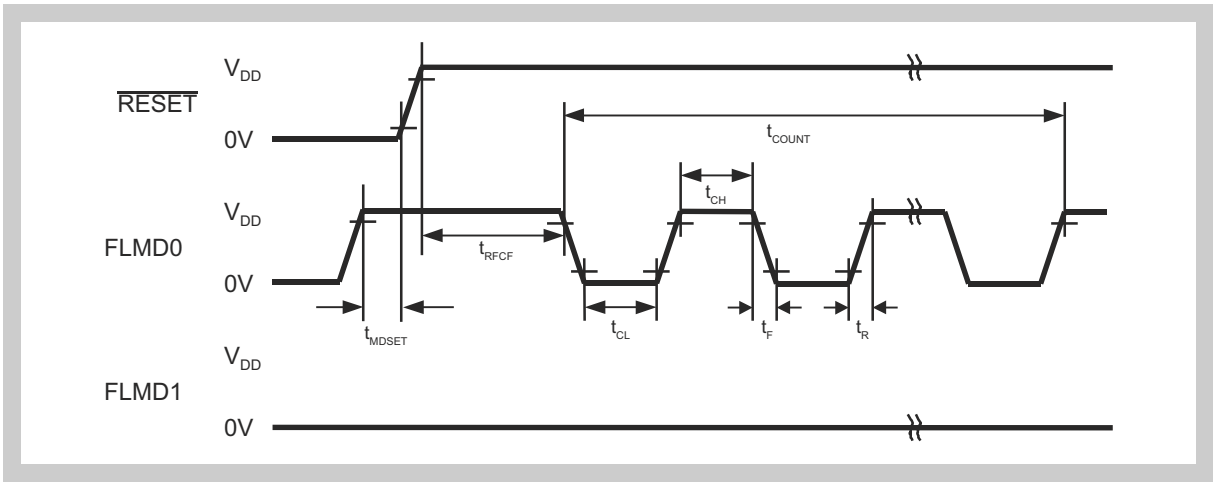
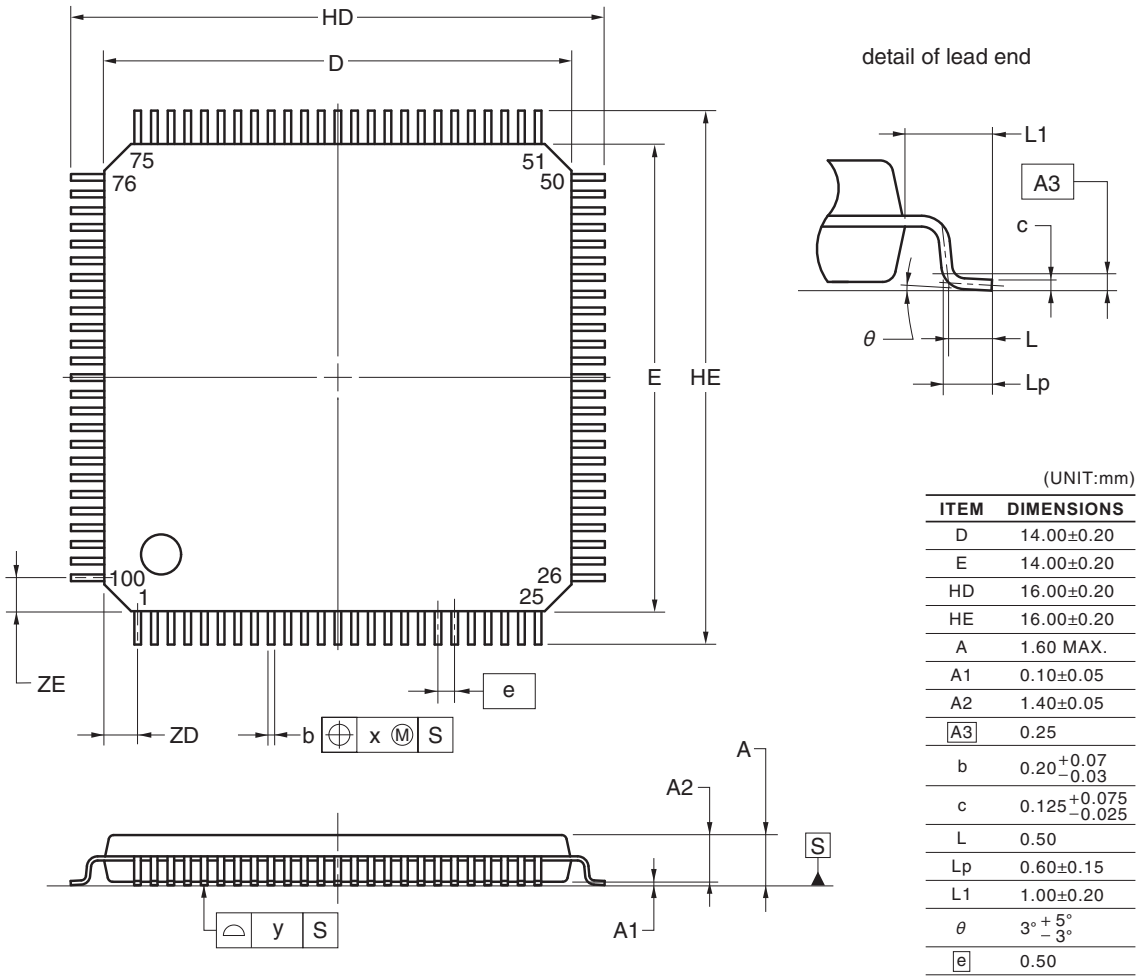


Figure 9-1 Flash Memory Timing

Note FLMD1 is a shared pin function.

Chapter 10 Package

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

P100GC-50-UEU-1

Figure 10-1 Package Drawing µPD70F3417(A)GC, µPD70F3416(A)GC

Copper lead frame with NiPdAu plating.

Appendix A Revision History

Item	Date published	Document No.	Comment
1	Dec 19 , 2006	EASE-DS-0004-1V0	First release of this document
2	Oct 2, 2008	U19509EE1V0DS00	Update of whole document, added conditions for extended operating temperature range, added injected current characteristics, added low voltage operation for CSIB, added supply current of flash devices, updated flash memory programming characteristics, added package drawing, added device µPD70F3416.
3	Jan 20, 2010	U19509EE1V1DS00	- µPD70F3416(A) was µPD70F3416 - µPD70F3417(A) was µPD70F3417
			- Added TM0 in Table 1-1
			- Added Table 4-3 - Main OSC Characteristics example for NDK LN-G8-1404
			- Added “Main OSC, PLLx8” and “Main OSC, SSCG” in table 5-2 for FOUT
			- Corrected values for “$\overline{\text{SCKBn}}$ high level width” and “$\overline{\text{SCKBn}}$ low level width” in table 7-9 (CSIB Slave Mode AC Characteristics with Digital Filter)
			- Corrected prefix of min. “SIBn hold time (from $\overline{\text{SCKBn}}$)” in table 7-11 (CSIB Master Mode AC Characteristics with Digital Filter - Low Voltage Operation)
			- Corrected Package code to “GC” (whole document)
4	Jun 8, 2011	R01DS0109ED0200	- Update the whole document to new Renesas format.
			- AC Characteristics of Flash Memory changed to more relaxed values (t_{MDSET}, t_{COUNT})

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