# µPC813

## High Slew Rate, Low Offset Voltage J-FET Input Operational Amplifier

R03DS0149EJ0100
Rev.1.00
2019.06.13

## DESCRIPTION

µPC813 is a high-speed version of µPC811. The J-FET input operational amplifier features a high-speed PNP transistor in the output stage for stable operation at a high slew rate of 25V/us with a gain of 1 (full feedback)

The resistor-trimming method proven in other Renesas High-Precision Op-Amp and High-Precision reference voltage is incorporate in this Op-Amp input stage, thus producing an excellent low offset voltage characteristics that has surpasses conventional general purpose op-amp in spite of being JFET input.

Under the same series, µPC814, 4094 with the same circuit configuration are also available.

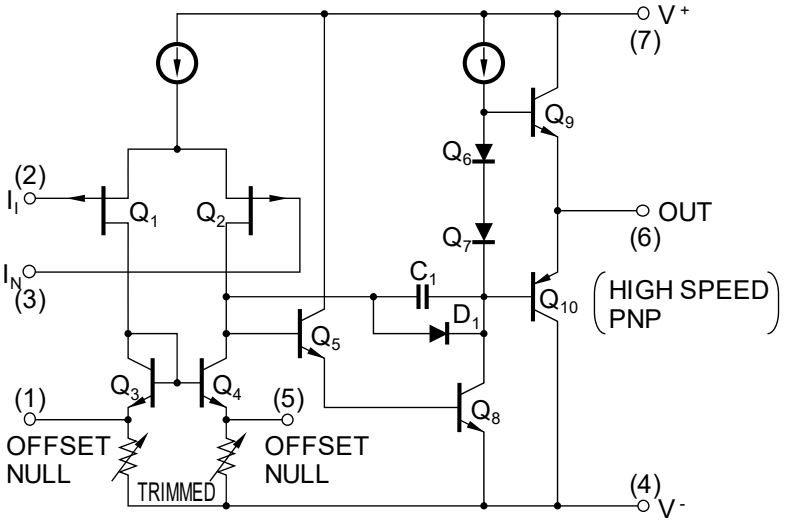
## FEATURES

- Input Offset Voltage ±1 mV (TYP.) (±2.5 mV MAX.)
- $V_{IO}$ Temperature Drift ±7 µV/°C (TYP.)
- Input Bias Current 50 pA (TYP.)
- Slew Rate 25 V/µs (TYP.)
- Unity Gain Frequency 6 MHz (TYP.)
- Input Equivalent Noise Voltage Density 19 nV/$\sqrt{Hz}$ (TYP.) (f = 1 kHz)
- Stable operation against capacitive load (Capacitive Load at 220 pF, $A_V$ = +1 )
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Single Op-Amp terminal connection (pin compatible)

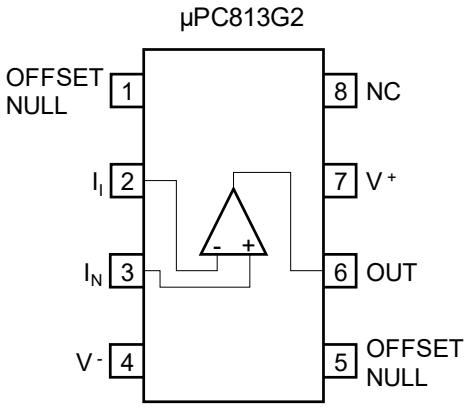
## ORDERING INFORMATION

| Ordering Name | Package |
|---|---|
| µPC813G2-A | 8-pin plastic SOP ( 225 mil) |

## EQUIVALENT CIRCUIT




## PIN CONFIGURATION (Top View)




Note NC : No Connection

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C)

| PARAMETER | SYMBOL | μPC813G2 | UNIT |
|---|---|---|---|
| Supply Voltage Note1 | $V^+ - V^-$ | -0.3 ~ +36 | V |
| Differential Input Voltage | $V_{ID}$ | ±30 | V |
| Input Voltage Note2 | $V_I$ | $V^-$ -0.3 ~ $V^+$ +0.3 | V |
| Output Applied Voltage Note 3 | $V_O$ | $V^-$ -0.3 ~ $V^+$ +0.3 | V |
| Total Power Dissipation Note 4 | $P_T$ | 440 | mW |
| Output Short Circuit Duration Note 5 | | Indefinite | s |
| Operating Ambient Temperature | $T_A$ | -40 ~ +85 | °C |
| Storage Temperature | $T_{stg}$ | -55 ~ +125 | °C |

【Note】 1. Note that reverse connections of the power supply may damage the ICs.

2. The input terminal must be apply within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operates within the electrical characteristics range of input common-mode voltage.

3. The output terminal must be apply within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operates within the electrical characteristics range of maximum output voltage.

4. This is the value at $T_A \leqq$ +25 °C. De-rate value at -4.4 mW/°C when $T_A >$ 25 °C

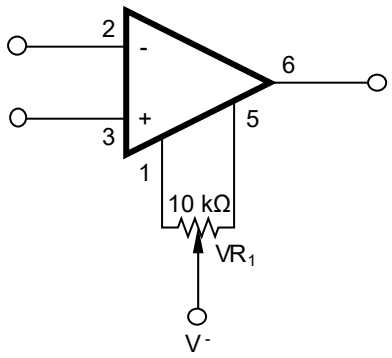
5. Please use the total loss and the de-rating value from Note 4.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Power Supply Voltage | $V^{\pm}$ | ±5 | | ±16 | V |
| Load Current | $I_O$ | | | ±10 | mA |
| Load Capacitance (When $A_V$ = +1) | $C_L$ | | | 220 Note 6 | pF |

【Note】 6. This is the value when the feedback resistor ($R_f$) = 0 Ω. The higher the $R_f$ value, the more likely it is to oscillate due to the influence of the input capacitance. So connect a capacitor of about 100 pF in parallel with $R_f$

### OFFSET ADJUSTMENT METHOD




**Note** OFFSET NULL pin should be open or connected to $V^-$ via a resistor as shown above. Any connection other than $V^-$ may cause malfunction, characteristics degradation or damage

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C, $V^{\pm}$ = ±15 V)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | | ±1 | ±2.5 | mV | $R_S$ ≦ 50 Ω |
| Input Offset Current Note 7 | $I_{IO}$ | | ±25 | ±100 | pA | |
| Input Bias Current Note 7 | $I_B$ | | 50 | 200 | pA | |
| Large Signal Voltage Gain | $A_V$ | 25000 | 200000 | | | $R_L$ ≧ 2 kΩ, $V_O$ = ±10 V |
| Circuit Current | $I_{CC}$ | | 2.5 | 3.4 | mA | $I_O$ = 0 A |
| Common Mode Rejection Ratio | CMR | 70 | 100 | | dB | |
| Supply Voltage Rejection Ratio | SVR | 70 | 100 | | dB | |
| Output Voltage Swing | $V_{om}$ | ±12 | +14.0<br>-13.3 | | V | $R_L$ ≧ 10 kΩ |
| Output Voltage Swing | $V_{om}$ | ±10 | +13.5<br>-12.8 | | V | $R_L$ ≧ 2 kΩ |
| Common Mode Input Voltage Range | $V_{ICM}$ | ±11 | +14<br>-12 | | V | |
| Slew Rate | SR | | 25 | | V/μs | $A_V$ = 1 |
| Unity Gain Frequency | $f_{unity}$ | | 6 | | MHz | |
| Input Equivalent Noise Voltage Density | $e_n$ | | 19 | | nV/$\sqrt{Hz}$ | $R_S$ = 100 Ω, f = 1 kHz |
| Input Offset Voltage | $V_{IO}$ | | | ±5 | mV | $R_S$ ≦ 50 Ω, $T_A$ = -20 ~ +70 °C |
| Average $V_{IO}$ Temperature Drift | $\Delta V_{IO}/\Delta T$ | | ±7 | | μV/°C | $T_A$ = -20 ~ +70 °C |
| Input Offset Current Note 7 | $I_{IO}$ | | | ±2 | nA | $T_A$ = -20 ~ +70 °C |
| Input Bias Current Note 7 | $I_B$ | | | 7 | nA | $T_A$ = -20 ~ +70 °C |

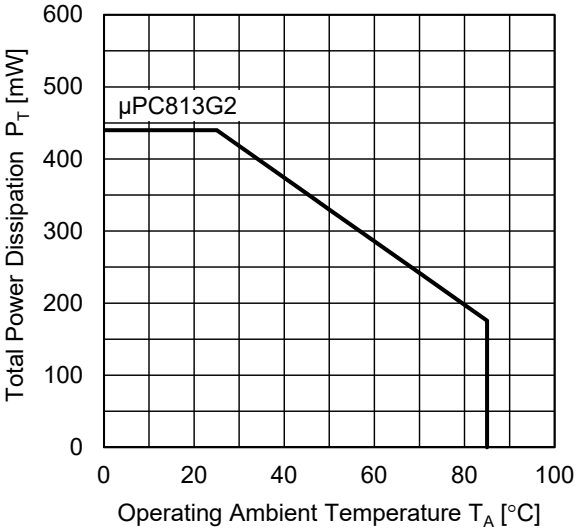
【Note】7. The direction of the input bias current is the same direction that flows into the IC because the first stage is composed of Pch J-FET. When $T_J$ = 25 °C or higher, it increases exponentially with increase in temperature (please see $I_B$ - $T_A$ characteristics). During measurement, please kindly take care of $T_J \fallingdotseq T_A$

**Caution**

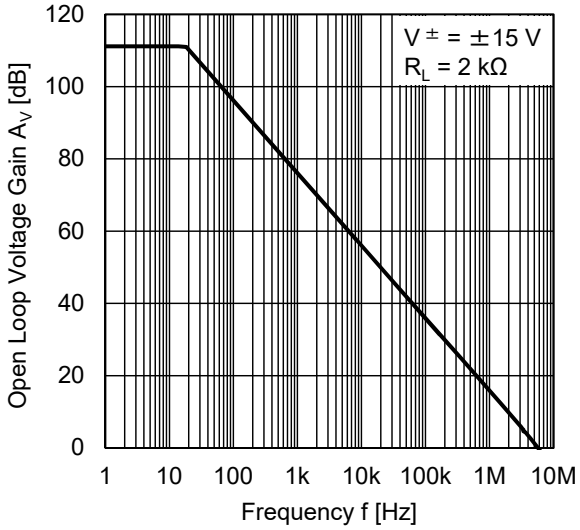
Since μPC813 has high input impedance characteristics, please be careful of insulation between the terminals on the board

## ELECTRICAL CHARACTERISTICS CURVE ($T_A$ = 25 °C, TYP.)

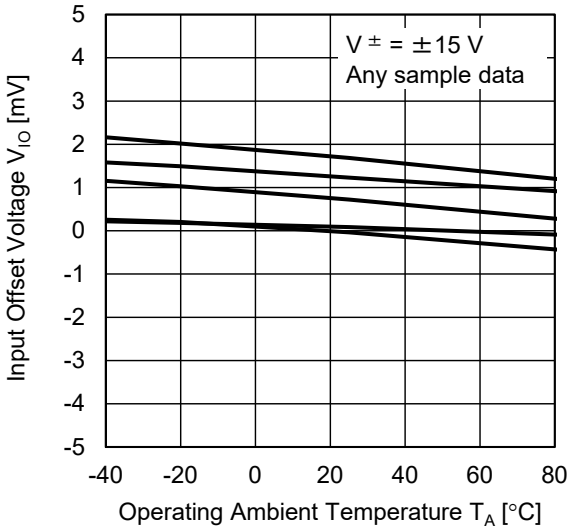
$P_T$ vs. $T_A$ (Absolute maximum rating)



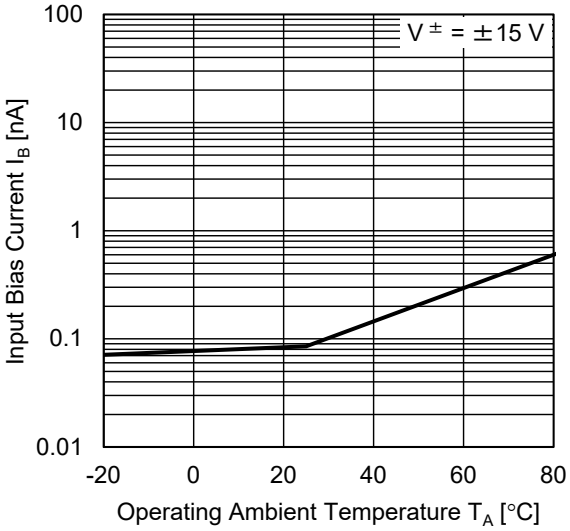

$A_V$ vs. f



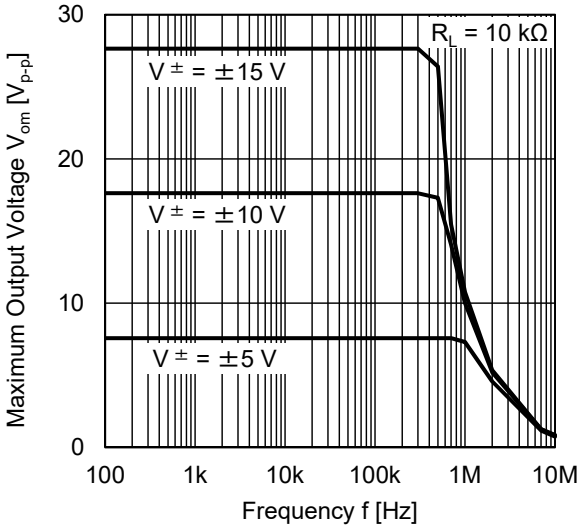

$V_{IO}$ vs. $T_A$



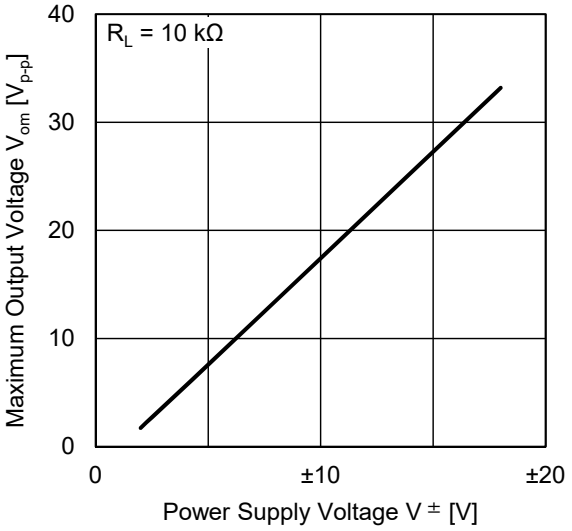

$I_B$ -vs.$T_A$



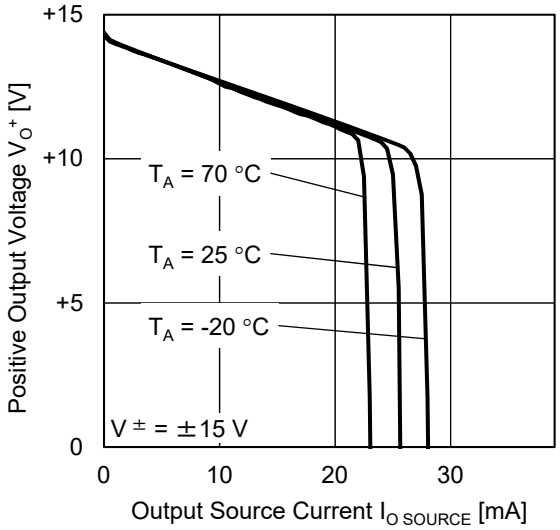

$V_{om}$ vs. f



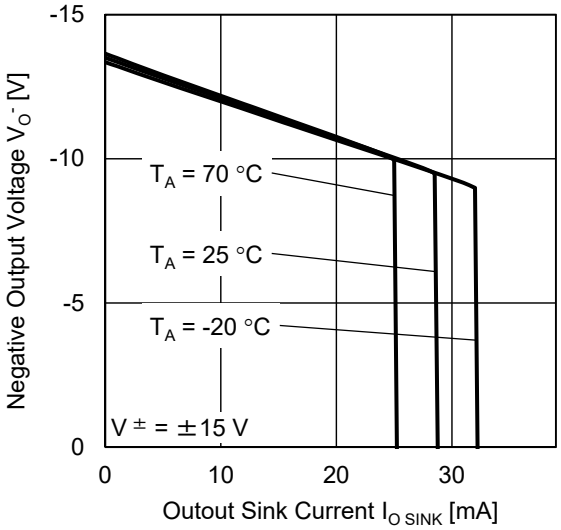

$V_{om}$ vs. $V^{\pm}$



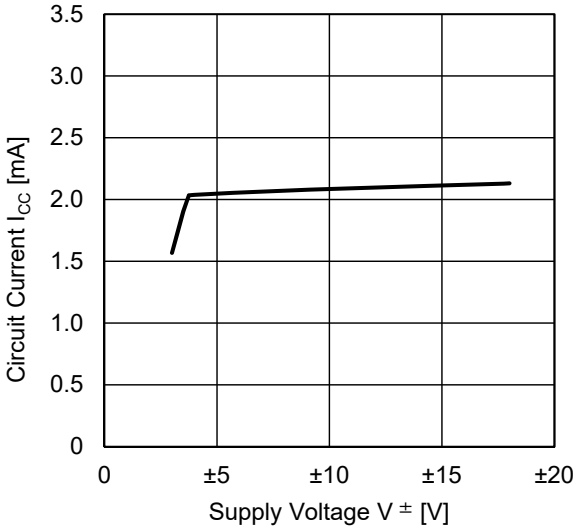
$V_O^+$ vs. $I_{O\ SOURCE}$



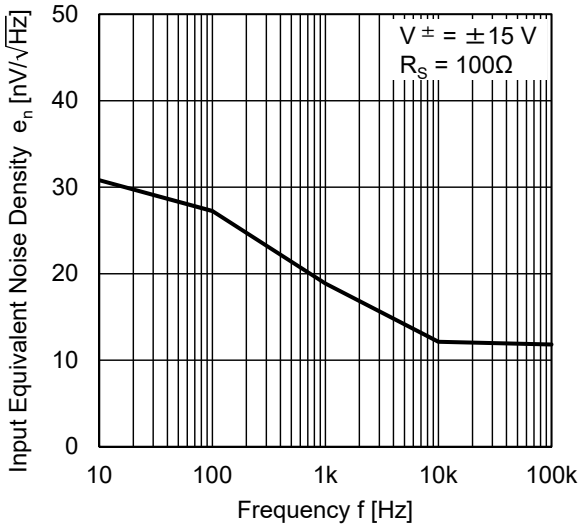

$V_O^-$ vs. $I_{O\ SINK}$



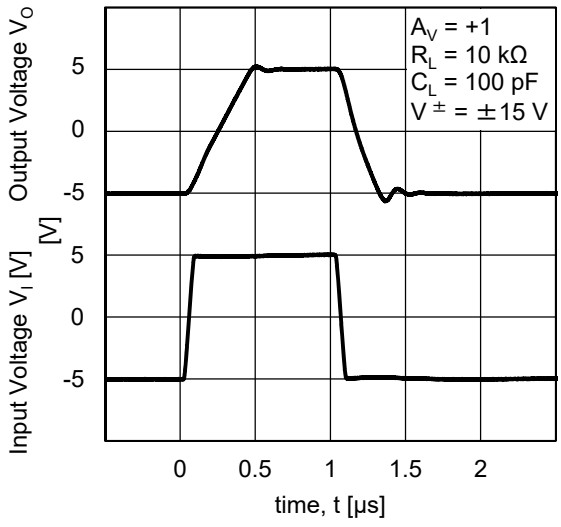

$I_{CC}$ vs. V ±




$e_n$ vs. f




Pulse Response Characteristics



## USE WITH PRECAUTIONS

- **Power Supply (Dual Power Supply / Single Power Supply)**
  The op amp operates when a predetermine voltage is applied between $V^+$ - $V^-$. Therefore, while it operates from a single power supply ($V^-$ = GND), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- **Ratings of input/output pin voltage**
  When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than $V^-$, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**
  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

  $V_{ICM}$ (TYP.) : $V^-$ +3 ~ $V^+$ -1 [V] ($T_A$ = 25 °C)

  During designing, do include some margin by considering characteristics variation, temperature characteristics etc.

- **Maximum Output Voltage**
  The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

  $V_{om}{}^+$ (TYP.) : $V^+$ -1 [V] ($T_A$ = 25 °C), $V_{om}{}^-$ (TYP.) : $V^-$ +1.7 [V] ($T_A$ = 25° C)

  During designing, do include some margin by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om+}$ − $V_{om-}$) will become narrow when the output current increases.

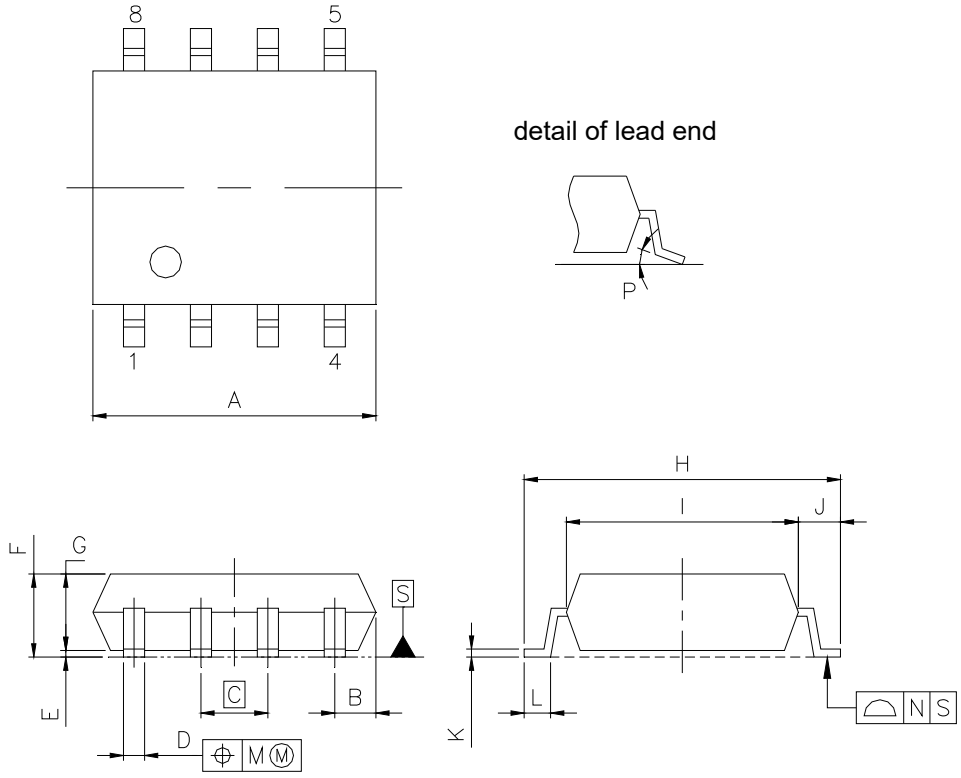
- **Handling of ICs**
  When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

## PACKAGE DRAWINGS

8-PIN PLASTIC SOP

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.) [g] |
|---|---|---|---|
| P-SOP8-0225-1.27 | PRSP0008DL-A | S8GM-50-225B | 0.08 |

Unit : mm




**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 5.2 +0.17 -0.20 |
| B | 0.78 MAX |
| C | 1.27 (T.P) |
| D | 0.42 +0.08 -0.07 |
| E | 0.1 ±0.1 |
| F | 1.59 ±0.21 |
| G | 1.49 |
| H | 6.5 ±0.3 |
| I | 4.4 ±0.15 |
| J | 1.1 ±0.2 |
| K | 0.17 +0.08 -0.07 |
| L | 0.6 ±0.2 |
| M | 0.12 |
| N | 0.10 |
| P | 3° +7° -3° |

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6. 使用瑞萨电子产品时，请参阅最新产品信息（数据表、使用说明书、应用指南、可靠性手册中的“半导体元件处理和使用一般注意事项”等），并确保使用条件在瑞萨电子指定的最大额定值、电源工作电压范围、散热特性、安装条件等范围内使用。对于在上述指定范围之外使用瑞萨电子产品而产生的任何故障、失效或事故，瑞萨电子概不承担任何责任。
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8. 关于环境保护方面的详细内容，例如每种瑞萨电子产品的环境兼容性等，请与瑞萨电子的营业部门联系。用户负责仔细并充分查阅对管制物质的使用或含量进行管理的所有适用法律法规（包括但不限于《欧盟RoHS指令》），并在使用瑞萨电子产品时遵守所有适用法律法规。对于因用户未遵守相应法律法规而导致的损害或损失，瑞萨电子概不承担任何责任。
9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将瑞萨电子产品或技术用于(1)与大规模杀伤性武器（例如核武器、化学武器、生物武器或运送此等武器的导弹，包括无人机(UAV)）的开发、设计、制造、使用、存储等相关的任何目的；(2)与常规武器的开发、设计、制造或使用相关的任何目的；(3)扰乱国际和平与安全的任何其他目的，并且不可向任何第三方销售、出口、租赁、转让、或让与瑞萨电子产品或技术，无论直接或间接知悉或者有理由知悉该第三方或任何其他方将从事上述活动。用户必须遵守对各方或交易行使司法管辖权的任意国家/地区政府所公布和管理的任何适用出口管制法律法规。
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（注1） 瑞萨电子：在本文档中指瑞萨电子株式会社及其控股子公司。
（注2） 瑞萨电子产品：指瑞萨电子开发或生产的任何产品。

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