TP65H300G4LSGBE

650V SuperGaN® GaN FET in PQFN 8 × 8 Industry Standard Package (source tab)

Description

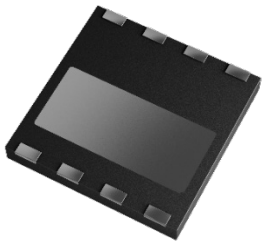
The TP65H300G4LSGBE 650V, 240mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance while enabling reduced system size and cost.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

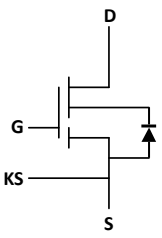
Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly used gate drivers

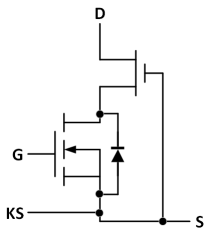
Product/Schematic Diagrams



TP65H300G4LSGBE PQFN 8 × 8 IP



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Robust design, defined by:
  - Transient over-voltage capability
  - Operation with E-mode Gate drivers without need for Zener protection
- Reduced crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	312
Q_{OSS} (nC) typical	19
Q_G (nC) typical	12.7

1. Dynamic $R_{DS(on)}$; see Figure 17 and Figure 18.

© 2025 Renesas Electronics

Contents

1. Pin Information 3
1.1 Pin Assignments 3
1.2 Pin Descriptions 3
2. Specifications 4
2.1 Absolute Maximum Ratings 4
2.2 Thermal Specifications 4
2.3 Electrical Specifications – Forward Device 5
2.4 Electrical Specifications – Reverse Device 6
3. Typical Performance Graphs 7
4. Test Circuits and Waveforms 9
5. Package Outline Drawings 10
6. Related Information 11
7. Ordering Information 11
8. Revision History 11

Figures

Figure 1. Pin Assignments – Bottom View 3
Figure 2. Typical Output Characteristics, T_J = 25°C Parameter: V_{GS} 7
Figure 3. Typical Output Characteristics, T_J = 150°C Parameter: V_{GS} 7
Figure 4. Typical Transfer Characteristics V_{DS} = 10V, parameter: T_J 7
Figure 5. Normalized On-resistance I_D = 5A, V_{GS} = 6V 7
Figure 6. Typical Capacitance V_{GS} = 0V, f = 1MHz 7
Figure 7. Typical C_{OSS} Stored Energy 7
Figure 8. Typical Q_{OSS} 8
Figure 9. Typical Gate Charge 8
Figure 10. Power Dissipation 8
Figure 11. Current Derating 8
Figure 12. Forward Characteristics of Rev. Diode 8
Figure 13. Transient Thermal Resistance 8
Figure 14. Safe Operating Area T_C = 25°C 9
Figure 15. Switching Time Test Circuit 9
Figure 16. Switching Time Waveform 9
Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit 9
Figure 18. Dynamic $R_{DS(on)eff}$ Waveform 9
Figure 19. 8 × 8 PQFN IP Package Outline Drawing 10

1. Pin Information

1.1 Pin Assignments

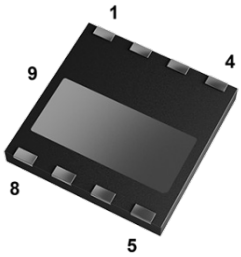


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4	D	Drain.
5, 6	S	Source.
7	KS	Kelvin source.
8	G	Gate.
9	S	Source.

2. Specifications

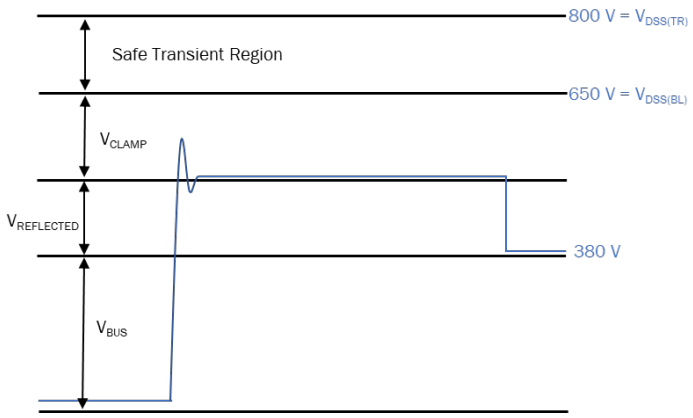
2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	-	650	V
$V_{DSS(TR)\ ,\ non\text{-}repetitive}$	Transient drain to source voltage, non-repetitive [1]	-	800	
$V_{DSS(TR)\ ,\ repetitive}$	Transient drain to source voltage, repetitive [2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at T_C = 25°C	-	31.5	W
I_D	Continuous drain current at T_C = 25°C	-	8	A
	Continuous drain current at T_C = 100°C	-	5	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	-	30	A
T_J	Junction operation temperature	-55	+150	°C
T_S	Storage temperature	-55	+150	°C
T_{SOLD}	Reflow soldering temperature [3]	-	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. Off-state, spike duration < 5µs.
3. Reflow MSL3.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	4	°C/W
$R_{\Theta JA}$	Junction-to-ambient [1]	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm^2 copper area and 70µm thickness).

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.5mA	1.2	1.6	2	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-5.8	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 6V, I_D = 5A, T_J = 25°C	-	240	312	mΩ
		V_{GS} = 6V, I_D = 5A, T_J = 150°C	-	492	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	1.2	12	µA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	8	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	1225	-	pF
C_{OSS}	Output capacitance		-	16.7	-	
C_{RSS}	Reverse transfer capacitance		-	3.4	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	23.7	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	48	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 6V, I_D = 5A	-	12.7	-	nC
Q_{GS}	Gate-source charge		-	3	-	
Q_{GD}	Gate-drain charge		-	4.6	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	19	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 6V, I_D = 5A, R_{G_on} = 15Ω, R_{G_off} = 5Ω, Z_{FB} = 120Ω at 100MHz (see Figure 15)	-	33	-	ns
t_R	Rise time		-	5.6	-	
$t_{D(off)}$	Turn-off delay		-	68	-	
t_F	Fall time		-	10	-	

1. Dynamic $R_{DS(on)}$ 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	5	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 2.5A	-	1.3	-	V
		V_{GS} = 0V, I_S = 5A	-	1.9	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

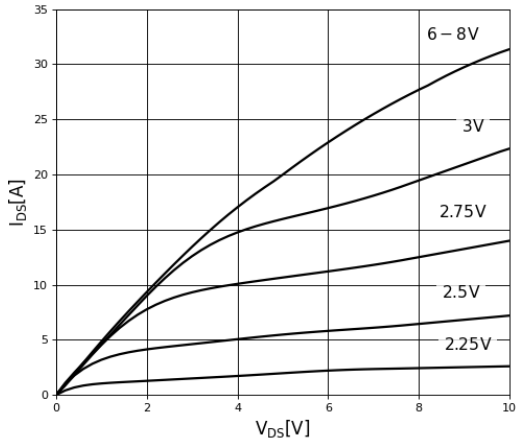


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

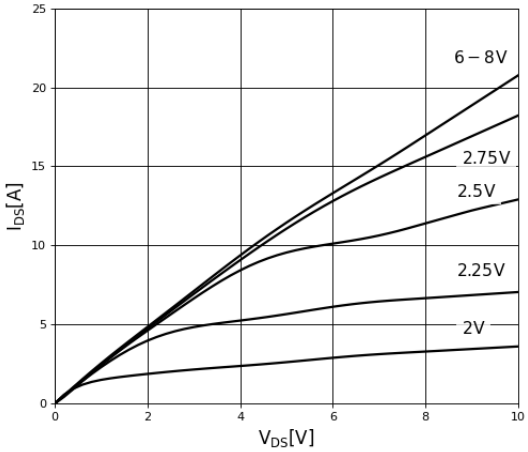


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

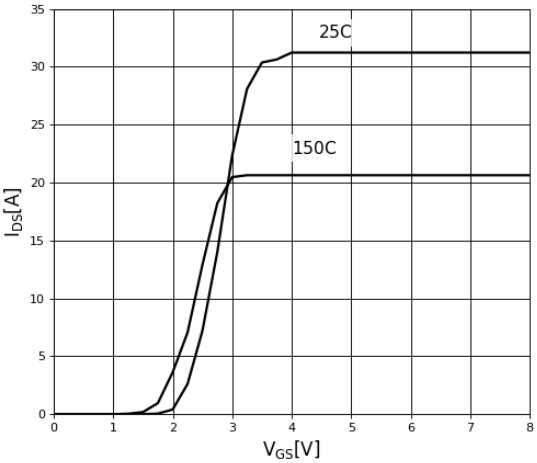


Figure 4. Typical Transfer Characteristics

V_{DS} = 10V, parameter: T_J

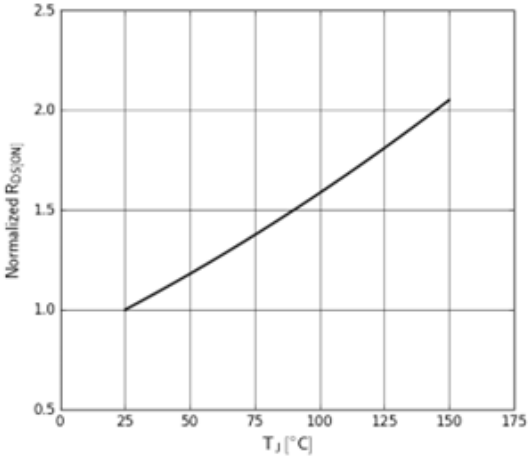


Figure 5. Normalized On-resistance

I_D = 5A, V_{GS} = 6V

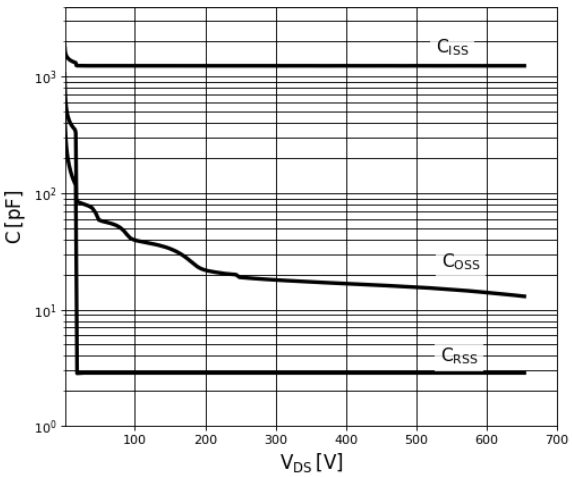


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 1MHz

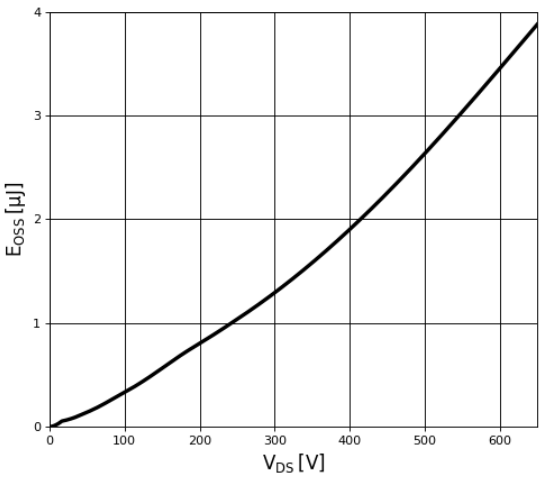


Figure 7. Typical C_{OSS} Stored Energy

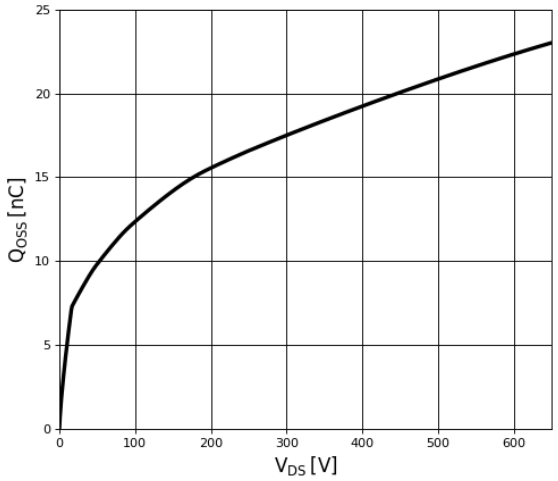


Figure 8. Typical Q_{OSS}

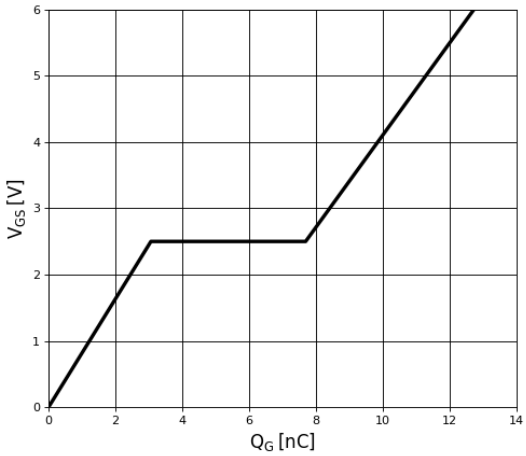


Figure 9. Typical Gate Charge

I_{DS} = 5A, V_{DS} = 400V

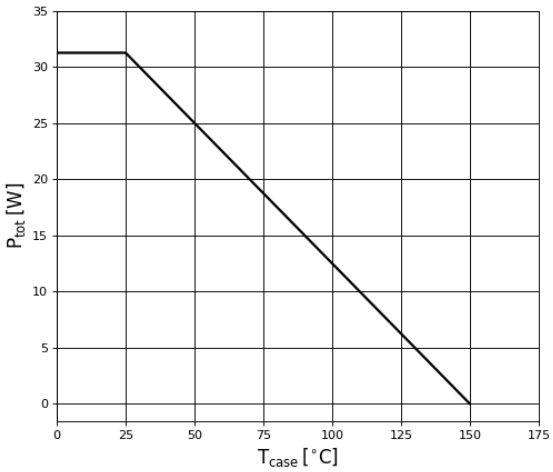


Figure 10. Power Dissipation

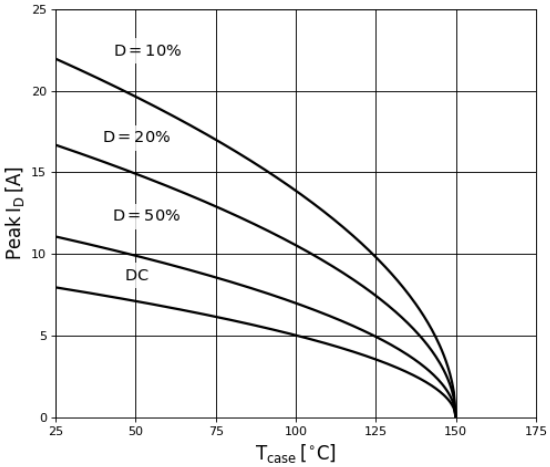


Figure 11. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 6V

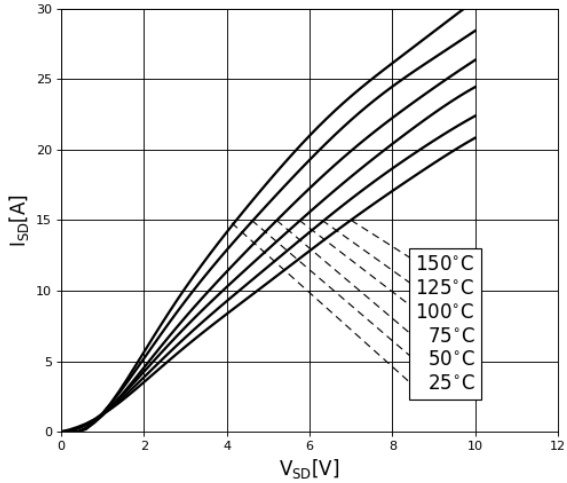


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

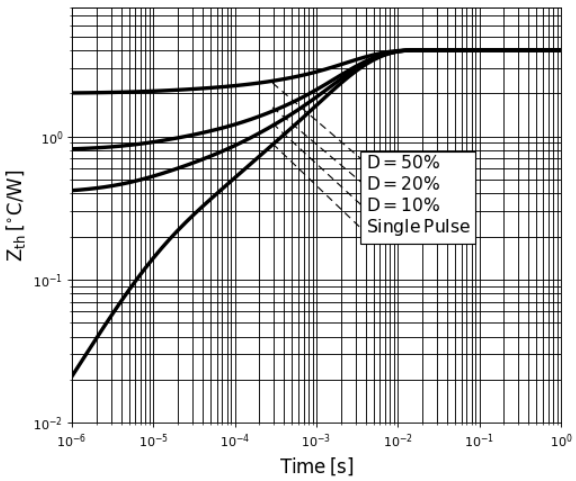


Figure 13. Transient Thermal Resistance

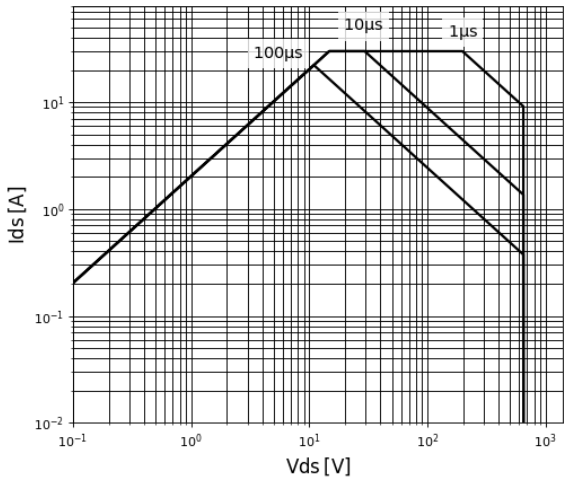


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

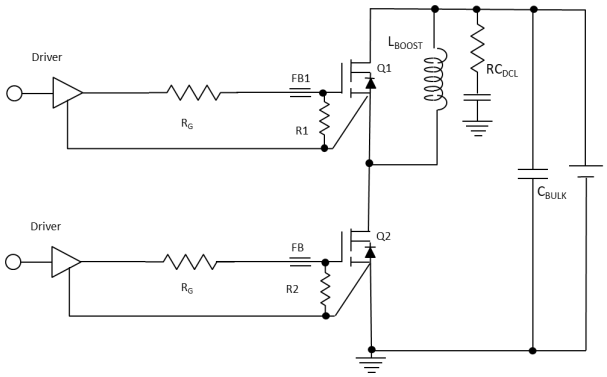


Figure 15. Switching Time Test Circuit

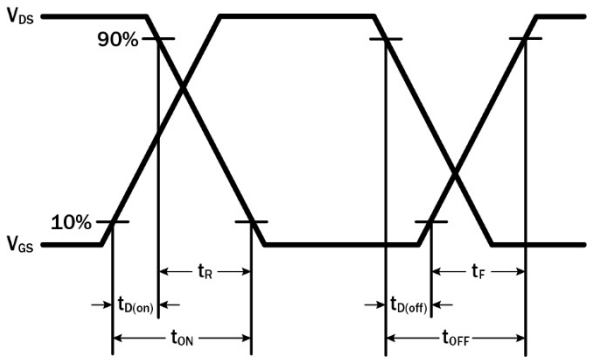


Figure 16. Switching Time Waveform

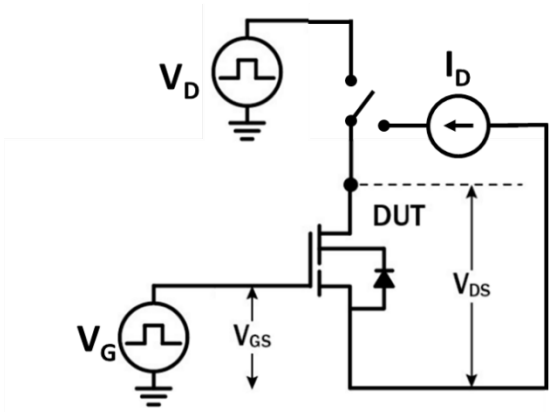


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

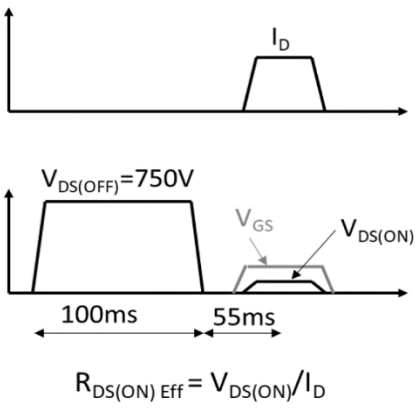
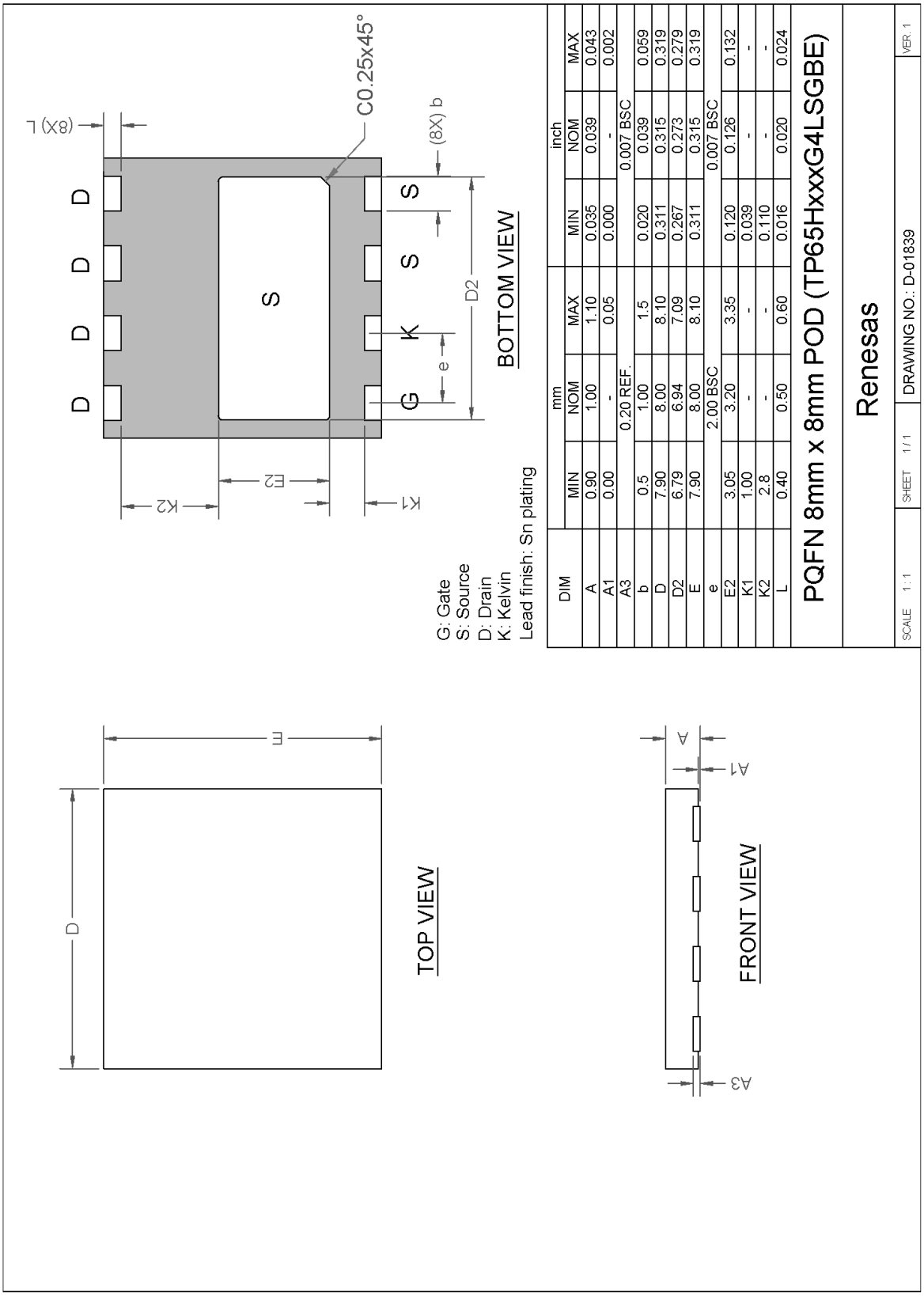


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 REF.			0.007 BSC	
b	0.5	1.00	1.5	0.020	0.039	0.059
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.79	6.94	7.09	0.267	0.273	0.279
E	7.90	8.00	8.10	0.311	0.315	0.319
e		2.00 BSC			0.007 BSC	
E2	3.05	3.20	3.35	0.120	0.126	0.132
K1	1.00	-	-	0.039	-	-
K2	2.8	-	-	0.110	-	-
L	0.40	0.50	0.60	0.016	0.020	0.024

Figure 19. 8 × 8 PQFN IP Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H300G4LSGBE-TR [1]	8 × 8 PQFN IP	Source

1. “-TR” suffix refers to tape and reel.

8. Revision History

Revision	Date	Description
2.00	Nov 21, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Apr 9, 2025	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2025 Renesas Electronics Corporation. All rights reserved.