SLG46620-A

Auto AEC-Q100 Qualified GreenPAK Programmable Mixed-signal Matrix

General Description

The SLG46620-A provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins and the macrocells of the SLG46620-A. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- 8-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC)
- ADC 3-bit Programmable Gain Amplifier (PGA)
- Two Digital-to-Analog Converters (DAC)
- Six Analog Comparators (ACMP)
- Two Voltage References (Vref)
- Twenty Five Combinatorial Look Up Tables (LUTs)
  - Eight 2-bit LUTs
  - Sixteen 3-bit LUTs
  - One 4-bit LUT
- One Combination Function Marcocells
  - Pattern Generator or 4-bit LUT
- Three Digital Comparators/Pulse Width Modulators (DCMPs /PWMs) w/ Selectable Deadband
- Ten Counters/Delays (CNT/DLY)
  - Two 14-bit Delay/Counter
  - One 14-bit Delay/Counter (Wake-Sleep Control)
  - One 14-bit Delay/Counter/Finite State Machine
  - Five 8-bit Delay/Counter
  - One 8-bit Delay/Counter/Finite State Machine
- Twelve D Flip-Flops/Latches
- Two Pipe Delays – 16 stage/ 2 output
- Two Programmable Delays w/ Edge Detection
- Three Internal Oscillators
  - Low-Frequency
  - Ring
  - RC 25 kHz and 2 MHz
- Power-On Reset (POR)
- Two Bandgaps
- Slave SPI
- Read Back Protection (Read Lock)
- Power Supply
  - 1.8 V (±5 %) to 3.3 V (±10 %)
- Ambient Operating Temperature Range: -40 °C to 105 °C
- RoHS Compliant / Halogen-Free
- Available Package
  - 20-pin TSSOP: 6.5 mm x 6.4 mm x 1.2 mm, 0.65 mm pitch
- AEC-Q100 (T_A = -40 °C to 105 °C) Qualified

Applications

- Infotainment
- Navigation
- Advanced Driver Assistance Systems (ADAS)
- Automotive Display Clusters
- Body Electronics

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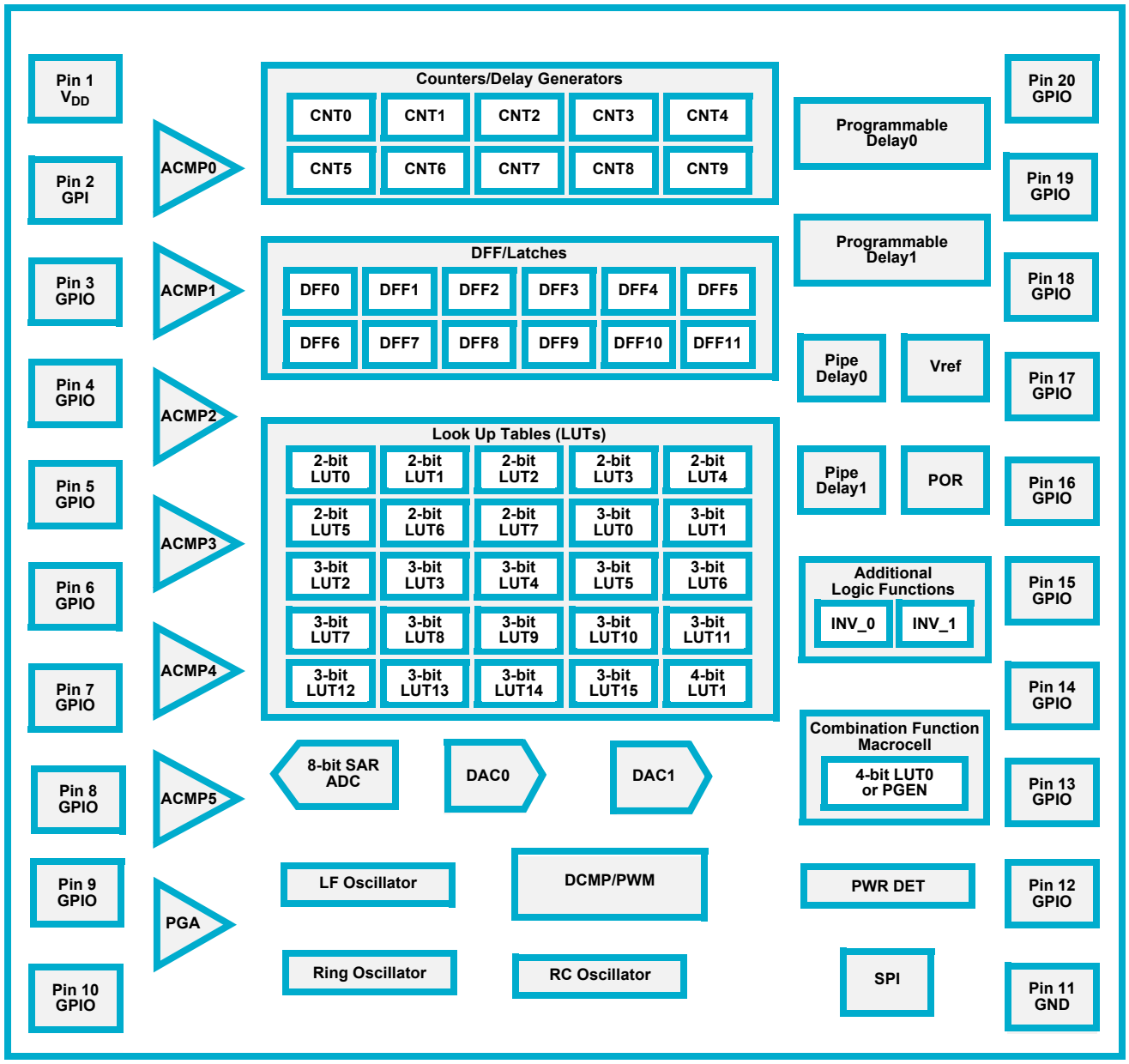
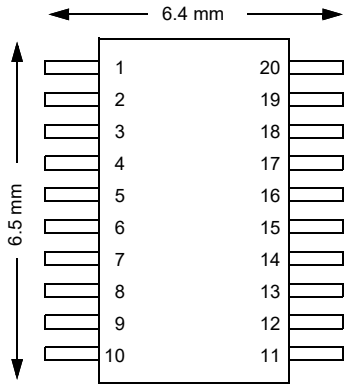
1 Block Diagram



2 Pinout

2.1 PIN CONFIGURATION - TSSOP-20



TSSOP-20
(Top View)

Table 1: Functional Pin Description

Pin #	Pin Type	Function
1	VDD	Power Supply
2	GPI	General Purpose Input External Reset ADC CLK
3	GPIO	General Purpose IO with OE ACMP4(+)
4	GPIO	General Purpose IO ACMP5(+)
5	GPIO	General Purpose IO with OE ACMP5 (-)
6	GPIO	General Purpose IO ACMP0(+) / ACMP1(+) / ACMP2(+) / ACMP3(+) / ACMP4(+)
7	GPIO	General Purpose IO with OE ACMP0(-) / ACMP1(-) / PGA_OUT
8	GPIO	General Purpose IO PGA(+)
9	GPIO	General Purpose IO with OE PGA(-)
10	GPIO	General Purpose IO with OE ACMP0(-) / ACMP1(-) / ACMP2(-) / ACMP3(-) / ACMP4(-) Super Drive IO
11	GND	Ground
12	GPIO	General Purpose IO ACMP1(+) Super Drive IO
13	GPIO	General Purpose IO with OE ACMP2(+) / ACMP3(+)
14	GPIO	General Purpose IO with OE ACMP2(-)

Table 1: Functional Pin Description (Continued)

Pin #	Pin Type	Function
15	GPIO	General Purpose IO ACMP3(+) / ACMP4(+)
16	GPIO	General Purpose IO with OE
17	GPIO	General Purpose IO
18	GPIO	General Purpose IO with OE Vref OUT 1
19	GPIO	General Purpose IO with OE Vref OUT 0
20	GPIO	General Purpose IO

Table 2: Pin Type Definitions

Pin Type	Description
V_{DD}	Power Supply
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
GND	Ground

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
PGA Input voltage **(Note 1)**	Single-ended	--	1.98/G	V
	Differential	--	(1.98 - 0.55)/G	V
	Pseudo-differential	--	(1.98 - 0.18)/G	V
Maximum Average or DC Current Through V_{DD} Pin (Per chip side, **(Note 2)**)	T_J = 85 °C	--	45	mA
	T_J = 110 °C	--	21	mA
Maximum Average or DC Current Through GND Pin (Per chip side, **(Note 2)**)	T_J = 85 °C	--	69	mA
	T_J = 110 °C	--	33	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	10	mA
	Push-Pull 2x	--	14	
	Push-Pull 4x	--	28	
	OD 1x	--	14	
	OD 2x	--	27	
	OD 4x	--	46	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitive Level		1		

Note 1 IN+ relative to GND in Single-ended mode, IN+ and IN- relative to each other in Differential and Pseudo-differential modes.
Note 2 The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model), corner pins	750	--	V
ESD Protection (Charged Device Model), other pins	500	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		1.71	3.6	V
Operating Temperature		-40	105	°C

Table 5: Recommended Operating Conditions (Continued)

Parameter	Condition	Min	Max	Unit
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.71	3.3	3.6	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 3)**	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input **(Note 3)**	1.25	--	V_{DD}+ 0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 3)**	GND-0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input **(Note 3)**	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger, V_{DD} = 1.71 V	0.174	0.342	0.530	V
		Logic Input with Schmitt Trigger, V_{DD} = 1.8 V	0.181	0.346	0.530	V
		Logic Input with Schmitt Trigger, V_{DD} = 1.89 V	0.187	0.346	0.530	V
		Logic Input with Schmitt Trigger, V_{DD} = 3 V	0.253	0.405	0.630	V
		Logic Input with Schmitt Trigger, V_{DD} = 3.3 V	0.266	0.421	0.643	V
		Logic Input with Schmitt Trigger, V_{DD} = 3.6 V	0.271	0.432	0.681	V
V_{OH}	HIGH-Level Output Voltage	PMOS OD, 1x Drive, I_{OH} = 0.1 mA, V_{DD} = 1.71 V	1.677	1.697	--	V
		PMOS OD, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3 V	2.678	2.773	--	V
		PMOS OD, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.011	3.092	--	V

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage	PMOS OD, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.337	3.408	--	V
		PMOS OD, 2x Drive, I_{OH} = 0.1 mA, V_{DD} = 1.71 V	1.69	1.704	--	V
		PMOS OD, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3 V	2.843	2.887	--	V
		PMOS OD, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.156	3.196	--	V
		PMOS OD, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.467	3.503	--	V
		PMOS OD, 4x Drive, I_{OH} = 0.1 mA, V_{DD} = 1.71 V	1.702	1.707	--	V
		PMOS OD, 4x Drive, I_{OH} = 3 mA, V_{DD} = 3 V	2.918	2.941	--	V
		PMOS OD, 4x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.225	3.245	--	V
		PMOS OD, 4x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.53	3.549	--	V
		Push-Pull, 1x Drive, I_{OH} = 0.1 mA, V_{DD} = 1.71 V	1.677	1.703	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3 V	2.675	2.772	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.009	3.091	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.336	3.408	--	V
		Push-Pull, 2x Drive, I_{OH} = 0.1 mA, V_{DD} = 1.71 V	1.69	1.704	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3 V	2.842	2.886	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.156	3.196	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.466	3.503	--	V
		Push-Pull, 4x Drive, I_{OH} = 0.1 mA, V_{DD} = 1.71 V	1.702	1.707	--	V

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 4x Drive, I_{OH} = 3 mA, V_{DD} = 3 V	2.918	2.941	--	V
		Push-Pull, 4x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.225	3.246	--	V
		Push-Pull, 4x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.53	3.549	--	V
V_{OL}	LOW-Level Output Voltage	NMOS OD, 1x Drive, I_{OL} = 0.1 mA, V_{DD} = 1.71 V	--	0.003	0.007	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3 V	--	0.064	0.094	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.06	0.088	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	0.056	0.083	V
		NMOS OD, 2x Drive, I_{OL} = 0.1 mA, V_{DD} = 1.71 V	--	0.002	0.004	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3 V	--	0.035	0.051	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.033	0.048	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	0.031	0.046	V
		NMOS OD, 4x Drive, I_{OL} = 0.1 mA, V_{DD} = 1.71 V	--	0.001	0.002	V
		NMOS OD, 4x Drive, I_{OL} = 3 mA, V_{DD} = 3 V	--	0.018	0.026	V
		NMOS OD, 4x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.017	0.025	V
		NMOS OD, 4x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	0.016	0.024	V
		Push-Pull, 1x Drive, I_{OL} = 0.1 mA, V_{DD} = 1.71 V	--	0.008	0.017	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3 V	--	0.153	0.232	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.144	0.216	V

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	0.133	0.201	V
		Push-Pull, 2x Drive, I_{OL} = 0.1 mA, V_{DD} = 1.71 V	--	0.004	0.009	V
		Push-Pull, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3 V	--	0.079	0.117	V
		Push-Pull, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.074	0.109	V
		Push-Pull, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	0.069	0.103	V
		Push-Pull, 4x Drive, I_{OL} = 0.1 mA, V_{DD} = 1.71 V	--	0.002	0.004	V
		Push-Pull, 4x Drive, I_{OL} = 3 mA, V_{DD} = 3 V	--	0.04	0.057	V
		Push-Pull, 4x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.037	0.053	V
		Push-Pull, 4x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	0.035	0.050	V
I_{OH}	HIGH-Level Output Pulse Current **(Note 1)**	PMOS OD, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 1.71 V	0.888	1.327	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V	5.014	6.862	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	7.602	10.292	--	mA
		PMOS OD, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	10.22	13.661	--	mA
		PMOS OD, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 1.71 V	1.784	2.602	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V	9.758	13.325	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	14.765	19.961	--	mA
		PMOS OD, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	19.786	26.453	--	mA

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Pulse Current **(Note 1)**	PMOS OD, 4x Drive, $V_{OH} = V_{DD} - 0.2$ V_{DD} = 1.71 V	3.467	4.940	--	mA
		PMOS OD, 4x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V	18.41	24.709	--	mA
		PMOS OD, 4x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	27.793	36.972	--	mA
		PMOS OD, 4x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	37.08	48.908	--	mA
		Push-Pull, 1x Drive, $V_{OH} = V_{DD} - 0.2$ V_{DD} = 1.71 V	0.886	1.328	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V	4.988	6.850	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	7.57	10.274	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	10.186	13.642	--	mA
		Push-Pull, 2x Drive, $V_{OH} = V_{DD} - 0.2$ V_{DD} = 1.71 V	1.772	2.602	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V	9.73	13.308	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	14.727	19.934	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	19.742	26.407	--	mA
		Push-Pull, 4x Drive, $V_{OH} = V_{DD} - 0.2$ V_{DD} = 1.71 V	3.474	4.967	--	mA
		Push-Pull, 4x Drive, V_{OH} = 2.4 V, V_{DD} = 3 V	18.371	24.763	--	mA
		Push-Pull, 4x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	27.716	37.017	--	mA
		Push-Pull, 4x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	36.955	48.951	--	mA

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Pulse Current **(Note 1)**	NMOS OD, 1x Drive, V_{OL} = 0.15 V V_{DD} = 1.71 V	2.605	3.747	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3 V	11.731	17.144	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V	12.68	18.499	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V	13.405	20.055	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V V_{DD} = 1.71 V	4.973	7.184	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3 V	21.614	32.171	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V	23.323	34.195	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V	24.348	37.261	--	mA
		NMOS OD, 4x Drive, V_{OL} = 0.15 V V_{DD} = 1.71 V	10.026	14.124	--	mA
		NMOS OD, 4x Drive, V_{OL} = 0.4 V V_{DD} = 3 V	43.796	62.595	--	mA
		NMOS OD, 4x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V	45.48	65.776	--	mA
		NMOS OD, 4x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V	49.417	72.104	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V V_{DD} = 1.71 V	1.053	1.521	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3 V	4.903	7.109	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V	5.266	7.734	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V	5.67	8.393	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V V_{DD} = 1.71 V	2.091	3.020	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3 V	9.54	13.867	--	mA

Table 6: EC at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Pulse Current **(Note 1)**	Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V	10.285	15.013	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V	10.928	16.260	--	mA
		Push-Pull, 4x Drive, V_{OL} = 0.15 V V_{DD} = 1.71 V	4.213	6.012	--	mA
		Push-Pull, 4x Drive, V_{OL} = 0.4 V V_{DD} = 3 V	19.57	27.791	--	mA
		Push-Pull, 4x Drive, V_{OL} = 0.4 V V_{DD} = 3.3 V	20.916	29.449	--	mA
		Push-Pull, 4x Drive, V_{OL} = 0.4 V V_{DD} = 3.6 V	22.726	32.030	--	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time **(Note 2)** From V_{DD} rising past PON_{THR}	T_{ramp} = 3 ms **(Note 4)**	--	1.448	3.229	ms
		T_{ramp} = 10 ms **(Note 4)**	--	1.567	7.458	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	0.921	1.464	1.700	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.836	1.107	1.390	V
R_{PUP}	Pull-up Resistance	1 M Pull-up	--	1	--	MΩ
		1 M Pull-up (PINs 17, 18, 19)	--	1	--	MΩ
		100 k Pull-up	--	100	--	kΩ
		10 k Pull-up	--	10	--	kΩ
R_{PDWN}	Pull-down Resistance	1 M Pull-down	--	1	--	MΩ
		100 k Pull-down	--	100	--	kΩ
		10 k Pull-down	--	10	--	kΩ
C_{IN}	Input Capacitance		--	2.49	2.97	pF

Note 1 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2 V_{DD} ramp rising speed must be less than 0.6 V/µs after Power-on. Violating this specification may cause chip to restart.
Note 3 No hysteresis.
Note 4 T_{ramp} - linear voltage ramp duration 0 V to V_{DD} on PIN1 relative to GND.

Table 7: Input Leakage Current at T_A = -40 °C to 105 °C, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{LKG} (Absolute Value)	ACMP Input Leakage	V_{IN-} = 0 V, V_{DD} = 1.71 V Ext.Vref/2	--	0.32	6.49	nA
		V_{IN-} = 0 V, V_{DD} = 1.71 V Ext.Vref	--	0.09	7.76	nA
		V_{IN+} = 0 V, V_{DD} = 1.71 V Buffer Disable, Gain = 0.25, 0.33, 0.5	--	1.30	5.90	nA
		V_{IN+} = 0 V, V_{DD} = 1.71 V Buffer Disable, Gain = 1	--	0.009	1.69	nA
		V_{IN+} = 0 V, V_{DD} = 1.71 V Buffer Enable	--	0.005	0.81	nA
		V_{IN-} = 1.2 V, V_{DD} = 1.71 V Ext.Vref	--	0.05	12.61	nA
		V_{IN-} = 1.2 V, V_{DD} = 1.71 V Ext.Vref/2	--	1198	1489	nA
		V_{IN+} = V_{DD}, V_{DD} = 1.71 V Buffer Enable	--	0.003	5.16	nA
		V_{IN+} = V_{DD}, V_{DD} = 1.71 V Buffer Disable, Gain = 0.25, 0.33, 0.5	--	1649	2078	nA
		V_{IN+} = V_{DD}, V_{DD} = 1.71 V Buffer Disable, Gain = 1	--	0.006	7.84	nA
		V_{IN-} = 0 V, V_{DD} = 3.3 V ± 10 % Ext.Vref/2	--	0.31	7.10	nA
		V_{IN-} = 0 V, V_{DD} = 3.3 V ± 10 % Ext.Vref	--	0.1	8.19	nA
		V_{IN+} = 0 V, V_{DD} = 3.3 V ± 10 % Buffer Disable, Gain = 0.25, 0.33, 0.5	--	1.36	6.78	nA
		V_{IN+} = 0 V, V_{DD} = 3.3 V ± 10 % Buffer Disable, Gain = 1	--	0.018	1.99	nA
		V_{IN+} = 0 V, V_{DD} = 3.3 V ± 10 % Buffer Enable	--	0.005	0.95	nA
		V_{IN-} = 1.2 V, V_{DD} = 3.3 V ± 10 % Ext.Vref	--	0.048	12.39	nA
		V_{IN-} = 1.2 V, V_{DD} = 3.3 V ± 10 % Ext.Vref/2	--	1200	1493	nA
		V_{IN+} = V_{DD}, V_{DD} = 3.3 V ± 10 % Buffer Enable	--	0.007	10.06	nA
		V_{IN+} = V_{DD}, V_{DD} = 3.3 V ± 10 % Buffer Disable, Gain = 0.25, 0.33, 0.5	--	3483	4389	nA
		V_{IN+} = V_{DD}, V_{DD} = 3.3 V ± 10 % Buffer Disable, Gain = 1	--	0.016	14.35	nA
	PGA Input Leakage ADC Mode = DI, PD, SE	V_{IN} = 0 V, V_{DD} = 1.71 V	--	0.005	1	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V	--	0.008	4.75	nA
		V_{IN} = 0 V, V_{DD} = 3.3 V ± 10 %	--	0.004	0.84	nA
		V_{IN} = V_{DD}, V_{DD} = 3.3 V ± 10 %	--	0.004	3.92	nA

Table 7: Input Leakage Current at T_A = -40 °C to 105 °C, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{LKG} (Absolute Value)	Logic Input without Schmitt Trigger (Floating) Leakage	V_{IN} = 0 V, V_{DD} = 1.71 V to 3.6 V	--	0.003	1.09	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V to 3.6 V	--	0.007	5.46	nA
	Logic Input without Schmitt Trigger (Floating) Leakage (pin 17, 18, 19)	V_{IN} = 0 V, V_{DD} = 1.71 V to 3.6 V	--	0.004	2.94	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V to 3.6 V	--	2.56	445.77	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	V_{IN} = 0 V, V_{DD} = 1.71 V to 3.6 V	--	0.003	1.06	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V to 3.6 V	--	0.007	5.43	nA
	Logic Input with Schmitt Trigger (Floating) Leakage (pin 17, 18, 19)	V_{IN} = 0 V, V_{DD} = 1.71 V to 3.6 V	--	0.004	2.90	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V to 3.6 V	--	2.56	442.87	nA
	Low-Level Logic Input (Floating) Leakage	V_{IN} = 0 V, V_{DD} = 1.71 V to 3.6 V	--	0.003	1.04	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V to 3.6 V	--	0.007	5.39	nA
	Low-Level Logic Input (Floating) Leakage (pin 17, 18, 19)	V_{IN} = 0 V, V_{DD} = 1.71 V to 3.6 V	--	0.004	2.85	nA
		V_{IN} = V_{DD}, V_{DD} = 1.71 V to 3.6 V	--	2.57	439.75	nA

Table 8: Typical Current Consumption Estimated for Each Macrocell at T_A = -40 °C to 105 °C

Condition	V_{DD} = 1.71 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V	Unit
Quiescent current	0.29	0.39	0.4	µA
BG Force On, Output Delay = 550 µs	35.56	29.24	29.89	µA
Charge Pump Mode - Any	0.29	0.38	0.40	µA
LF OSC Force PWR On; Matrix PWR Down Dis; Pre-Divider = 1	0.47	0.52	0.53	µA
LF OSC Force PWR On; Matrix PWR Down Dis; Pre-Divider = 16	0.46	0.49	0.49	µA
RC OSC (25 kHz) Force PWR On; Matrix PWR Down Dis; Pre-Divider = 1; Second Divider = 1	4.52	5.19	5.31	µA
RC OSC (25 kHz) Force PWR On; Matrix PWR Down Dis; Pre-Divider = 8; Second Divider = 1	4.30	4.73	4.80	µA
RC OSC (2 MHz) Force PWR On; Matrix PWR Down Dis; Pre-Divider = 1; Second Divider = 1	34.18	59.68	64.61	µA
RC OSC (2 MHz) Force PWR On; Matrix PWR Down Dis; Pre-Divider = 8; Second Divider = 1	16.92	23.22	24.43	µA
RING OSC Force PWR On; Matrix PWR Down Dis; Pre-Divider = 1; Second Divider = 1	80.11	112.34	120.23	µA
RING OSC Force PWR On; Matrix PWR Down Dis; Pre-Divider = 16; Second Divider = 1	57.28	62.06	64.75	µA
Internal Vref	77.63	77.3	77.95	µA
DAC0 Force On	47.86	41.90	42.56	µA
DAC0+DAC1 Force On	97.63	94	94.67	µA
PGA Force On; Gain = 0.5; ADC SE; Ext_OUT Dis	100	98.13	99.04	µA
PGA Force On; Gain = 1; ADC SE; Ext_OUT Dis/En	67.84	62.44	63.06	µA
PGA Force On; Gain = 2; ADC SE; Ext_OUT Dis	100.58	98.51	99.41	µA

Table 8: Typical Current Consumption Estimated for Each Macrocell at T_A = -40 °C to 105 °C (Continued)

Condition	V_{DD} = 1.71 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V	Unit
PGA Force On; Gain = 4; ADC SE; Ext_OUT Dis	101.15	98.88	99.69	µA
PGA Force On; Gain = 8; ADC SE; Ext_OUT Dis	101.87	99.59	100.47	µA
ACMP0; Hyst Disable or Hyst = 25 mV; IN PIN6; Buff Bandwidth = 1 kHz; Gain = 1; Vref = 1 V	46.09	40.10	40.75	µA
ACMP0; Hyst Disable; IN Buffered PIN6; BUF Bandwidth = 1 kHz; Gain = 0.25, 0.33, 0.5; Vref = 1 V	47.68	45.07	45.99	µA
ACMP0; Hyst Disable; IN Buffered PIN6; BUF Bandwidth = 1 kHz; Gain = 1; Vref = 1 V	51.19	45.83	46.53	µA
ACMP0; Hyst Disable; IN Buffered PIN6; BUF Bandwidth = 5 kHz; Gain = 1; Vref = 1 V	56.49	51.63	52.34	µA
ACMP0; Hyst Disable; IN Buffered PIN6; BUF Bandwidth = 20 kHz; Gain = 1; Vref = 1 V	68.11	64.36	65.15	µA
ACMP0; Hyst Disable; IN Buffered PIN6; BUF Bandwidth = 50 kHz; Gain = 1; Vref = 1 V	89.69	88.07	89.07	µA
ACMP0; Hyst Disable; IN V_{DD}; BUF Bandwidth = 1 kHz; Gain = 1; Vref = 1 V	42.72	41.95	42.61	µA
ACMP0; Hyst Disable; IN PIN6; BUF Bandwidth = 1 kHz; 100uA En; Gain = 1; Vref = 1 V	80.52	76.08	76.83	µA
ACMP0,1,2,3,4,5; Hyst Disable; IN PIN6,12,13,15,3,4; BUF Bandwidth = 1 kHz; Gain = 1; Vref = 1 V	70.90	65.73	66.36	µA
ACMP0 WS En; Force Sleep Low; CNT Data = 10	4.69	4.19	4.26	µA
ADC PD; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1; WS En; Force Sleep Low; CNT Data = 10	35.23	37.45	37.56	µA
ADC PD; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1	368.32	387.98	389.54	µA
ADC DI; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1	379.01	400.05	401.65	µA
ADC DI; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1; WS En; Force Sleep Low; CNT Data = 10	36.28	38.58	38.75	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider - Any	168.86	168.06	168.84	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1; WS En; Force Sleep Low; CNT Data = 10	16.57	16.64	16.75	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (2 MHz); CLK Divider = 1	204.74	239.56	247.46	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (2 MHz); CLK Divider = 16	198.20	223.08	228.91	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RC OSC (2 MHz); CLK Divider = 1; WS En; Force Sleep Low; CNT Data = 10	18.96	21.86	22.52	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RING OSC; CLK Divider = 1	273.88	425.84	499.10	µA
ADC SE; Vref = 1.2 V; Analog Force En; CLK Source: RING OSC; CLK Divider = 16	246.19	332.03	349.54	µA

Table 8: Typical Current Consumption Estimated for Each Macrocell at T_A = -40 °C to 105 °C (Continued)

Condition	V_{DD} = 1.71 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V	Unit
ADC SE; Vref = PWR Div(0.25xV_{DD}); Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1	162.09	165.18	166.51	µA
ADC SE; Vref = PWR Div(0.25xV_{DD}); Analog Force En; CLK Source: RC OSC (25 kHz); CLK Divider = 1; WS En; Force Sleep Low; CNT Data = 10	15.87	16.37	16.53	µA

3.5 TIMING CHARACTERISTICS

Table 9: Typical Delay Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 1.71 V		V_{DD} = 3.3 V		V_{DD} = 3.6V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Both Matrix 2-bit LUT	19	17	6	6	6	5	ns
tpd	Delay	Both Matrix 3-bit LUT	21	18	7	6	6	6	ns
tpd	Delay	Matrix 0 4-bit LUT	28	26	9	9	9	8	ns
tpd	Delay	Matrix 1 4-bit LUT	23	19	8	7	7	6	ns
tpd	Delay	Both Matrix DFF Q	27	25	9	10	8	9	ns
tpd	Delay	Both Matrix DFF nQ	27	23	10	10	9	9	ns
tpd	Delay	Both Matrix DFF nSET Q	33	--	11	--	10	--	ns
tpd	Delay	Both Matrix DFF nSET nQ	--	30	--	11	--	10	ns
tpd	Delay	Both Matrix DFF nRST Q	--	28	--	10	--	9	ns
tpd	Delay	Both Matrix DFF nRST nQ	31	--	10	--	9	--	ns
tpd	Delay	Matrix 0 Digital Input to 1x 3-State (Hi-Z to 0)	--	42	--	16	--	15	ns
tpd	Delay	Matrix 0 Digital Input to 1x 3-State (Hi-Z to 1)	47	--	17	--	16	--	ns
tpd	Delay	Matrix 1 Digital Input to 1x 3-State (Hi-Z to 0)	--	36	--	14	--	13	ns
tpd	Delay	Matrix 1 Digital Input to 1x 3-State (Hi-Z to 1)	41	--	15	--	14	--	ns
tpd	Delay	Matrix 0 Digital Input to PP 1x	44	42	16	17	15	16	ns
tpd	Delay	Matrix 1 Digital Input to PP 1x	36	34	13	14	12	13	ns
tpd	Delay	Matrix 0 Digital Input to NMOS 1x	--	40	--	16	--	15	ns
tpd	Delay	Matrix 1 Digital Input to NMOS 1x	--	32	--	12	--	11	ns
tpd	Delay	Matrix 0 Digital Input to PP 2x 3-State (Hi-Z to 0)	--	41	--	16	--	14	ns
tpd	Delay	Matrix 0 Digital Input to PP 2x 3-State (Hi-Z to 1)	45	--	17	--	16	--	ns
tpd	Delay	Matrix 1 Digital Input to PP 2x 3-State (Hi-Z to 0)	--	35	--	13	--	12	ns
tpd	Delay	Matrix 1 Digital Input to PP 2x 3-State (Hi-Z to 1)	39	--	15	--	14	--	ns
tpd	Delay	Matrix 0 Digital Input to PP 2x	42	41	16	16	15	15	ns

Table 9: Typical Delay Estimated for Each Macrocell at T_A = 25 °C (Continued)

Parameter	Description	Note	V_{DD} = 1.71 V		V_{DD} = 3.3 V		V_{DD} = 3.6V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Matrix 1 Digital Input to PP 2x	34	32	13	13	12	12	ns
tpd	Delay	Matrix 0 Digital Input to NMOS 2x	--	39	--	15	--	14	ns
tpd	Delay	Matrix 1 Digital Input to NMOS 2x	--	31	--	12	--	11	ns
tpd	Delay	Matrix 0 Digital Input to PP 1x With Schmitt Trigger	44	43	17	18	16	17	ns
tpd	Delay	Matrix 1 Digital Input to PP 1x With Schmitt Trigger	38	35	14	15	13	14	ns
tpd	Delay	Matrix 0 Digital Input Low Voltage	51	564	18	187	17	168	ns
tpd	Delay	Matrix 1 Digital Input Low Voltage	41	392	15	134	14	121	ns
tpd	Delay	Both Matrix INV	19	16	6	7	5	6	ns
tpd	Delay	Both Matrix LATCH Q	25	24	9	9	8	8	ns
tpd	Delay	Both Matrix LATCH nQ	27	22	8	9	7	8	ns
tpd	Delay	Both Matrix LATCH nSET Q	30	--	10	--	9	--	ns
tpd	Delay	Both Matrix LATCH nSET nQ	--	26	--	10	--	9	ns
tpd	Delay	Both Matrix LATCH nRST Q	--	30	--	11	--	10	ns
tpd	Delay	Both Matrix LATCH nRST nQ	33	--	11	--	10	--	ns
tpd	Delay	Matrix Ports P0 - P9	15	13	5	4	4	4	ns
tpd	Delay	Matrix Ports P10 - P19	22	20	8	7	7	7	ns
tpd	Delay	PGEN CLK	31	32	12	12	11	11	ns
tpd	Delay	PGEN Hi-Z to 0	--	33	--	13	--	12	ns
tpd	Delay	PGEN Hi-Z to 1	37	--	13	--	11	--	ns
tpd	Delay	Both Matrix Pipe Delay CLK Q	37	35	13	14	12	13	ns
tpd	Delay	Both Matrix Pipe Delay CLK nQ	--	40	--	16	--	15	ns
tpd	Delay	Both Matrix Pipe Delay CLK nRST Q	--	38	--	15	--	14	ns
tpd	Delay	Both Matrix Pipe Delay CLK nRST nQ	45	--	16	--	15	--	ns

Table 10: Programmable Delay Expected Delays and Widths (Typical) at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 1.71 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V	Unit
time 1	Pulse Width, 1 cell	Mode: (any) edge detector, Output mode: Non-delayed	401	160	148	ns
time 1	Pulse Width, 2 cell	Mode: (any) edge detector, Output mode: Non-delayed	798	316	292	ns
time 1	Pulse Width, 3 cell	Mode: (any) edge detector, Output mode: Non-delayed	1196	473	437	ns
time 1	Pulse Width, 4 cell	Mode: (any) edge detector, Output mode: Non-delayed	1592	630	582	ns
tpd	Delay, 1 cell	Mode: (any) edge detector, Output mode: Non-delayed	37	13	12	ns
tpd	Delay, 2 cell	Mode: (any) edge detector, Output mode: Non-delayed	37	13	12	ns
tpd	Delay, 3 cell	Mode: (any) edge detector, Output mode: Non-delayed	37	13	12	ns

Table 10: Programmable Delay Expected Delays and Widths (Typical) at T_A = 25 °C (Continued)

Parameter	Description	Note	V_{DD} = 1.71 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V	Unit
tpd	Delay, 4 cell	Mode: (any) edge detector, Output mode: Non-delayed	37	13	12	ns
time 1	Pulse Width, 1 cell	Mode: (any) edge detector, Output mode: Delayed	393	157	145	ns
time 1	Pulse Width, 2 cell	Mode: (any) edge detector, Output mode: Delayed	790	312	288	ns
time 1	Pulse Width, 3 cell	Mode: (any) edge detector, Output mode: Delayed	1179	466	430	ns
time 1	Pulse Width, 4 cell	Mode: (any) edge detector, Output mode: Delayed	1578	621	573	ns
time 2	Delay, 1 cell	Mode: (any) edge detector, Output mode: Delayed	226	78	71	ns
time 2	Delay, 2 cell	Mode: (any) edge detector, Output mode: Delayed	407	143	128	ns
time 2	Delay, 3 cell	Mode: (any) edge detector, Output mode: Delayed	591	207	186	ns
time 2	Delay, 4 cell	Mode: (any) edge detector, Output mode: Delayed	772	271	244	ns
time 2 + time 1	Delay, 1 cell	Mode: Both edge delay	438	172	158	ns
time 2 + time 1	Delay, 2 cell	Mode: Both edge delay	835	328	303	ns
time 2 + time 1	Delay, 3 cell	Mode: Both edge delay	1233	485	447	ns
time 2 + time 1	Delay, 4 cell	Mode: Both edge delay	1631	641	592	ns

Note See Timing Diagram in section 17.1.

3.6 OSCILLATOR CHARACTERISTICS

See section 19 Clocking.

Table 11: Oscillators Frequency Limits

OSC	Power Supply Range (V_{DD}), V	Ambient Temperature Range					
		25 °C			-40 °C to 105 °C		
		Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
LF OSC (1.73 kHz)	1.71 V to 3.6 V	1.449	2.092	-16.2 +20.9	1.364	2.133	-21.2 +23.3
	1.8 V ± 5 %	1.450	2.087	-16.2 +20.6	1.364	2.132	-21.2 +23.2
	3.3 V ± 10 %	1.457	2.092	-15.8 +20.9	1.373	2.133	-20.6 +23.3
	3.3 V ± 10 % over lifetime at 105 °C **(Note 2)**	1.457	2.161	-15.8 +24.9	1.373	2.202	-20.6 +27.3
	2.3 V to 3.6 V	1.454	2.092	-16 +20.9	1.371	2.133	-20.8 +23.3
	2.3 V to 3.6 V over lifetime at 105 °C **(Note 2)**	1.454	2.161	-16 +24.9	1.371	2.202	-20.8 +27.3
RC OSC (25 kHz)	1.71 V to 3.6 V	22.888	31.065	-8.4 +24.3	22.527	38.073	-9.9 52.3 **(Note 1)**
	1.8 V ± 5 %	23.343	26.946	-6.6 +7.8	20.176	37.500	-19.3 50 **(Note 1)**
	3.3 V ± 10 %	24.741	25.344	-1 +1.4	23.490	26.450	-6 +5.8
	3.3 V ± 10 % over lifetime at 105 °C **(Note 2)**	24.741	26.544	-1 +6.2	23.490	27.650	-6 +10.6
	2.3 V to 3.6 V	24.432	26.066	-2.3 +4.3	23.353	27.063	-6.6 +8.3
	2.3 V to 3.6 V over lifetime at 105 °C **(Note 2)**	24.433	27.266	-2.3 +9.1	23.353	28.263	-6.6 +13.1

Table 11: Oscillators Frequency Limits (Continued)

OSC	Power Supply Range (V_{DD}), V	Ambient Temperature Range					
		25 °C			-40 °C to 105 °C		
		Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
RC OSC (2 MHz)	1.71 V to 3.6 V	1726.1	2110.3	-13.7 +5.5	1676	2179.1	-16.2 +9
	1.8 V ± 5 %	1942.4	2133	-2.9 +6.7	1869.8	2197.4	-6.5 +9.9
	3.3 V ± 10 %	1967.8	2039.9	-1.6 +2	1842.4	2121.8	-7.9 +6.1
	3.3 V ± 10 % over lifetime at 105 °C **(Note 2)**	1967.8	2119.9	-1.6 +6	1842.4	2201.8	-7.9 +10.1
	2.3 V to 3.6 V	1908.3	2095.6	-4.6 +4.8	1842.4	2158	-7.9 +7.9
	2.3 V to 3.6 V over lifetime at 105 °C **(Note 2)**	1908.3	2175.6	-4.6 +8.8	1842.4	2238	-7.9 +11.9
Ring OSC (27 MHz)	1.71 V to 3.6 V	21787.1	30437.8	-19.3 +12.7	20418	30437.8	-24.4 +12.7
	1.8 V ± 5 %	21920	30424.3	-18.8 +12.7	20579.6	30424.3	-23.8 +12.7
	3.3 V ± 10 %	23687.7	30224	-12.3 +11.9	22551.8	30224	-16.5 +11.9
	3.3 V ± 10 % over lifetime at 105 °C **(Note 2)**	23687.7	31304	-12.3 +15.9	22551.8	31304	-16.5 +15.9
	2.3 V to 3.6 V	23679.8	30224.7	-12.3 +11.9	22548.5	30224.7	-16.5 +11.9
	2.3 V to 3.6 V over lifetime at 105 °C **(Note 2)**	23679.8	31304.7	-12.3 +15.9	22548.5	31304.7	-16.5 +15.9

Note 1 Based on characterization data and is not guaranteed. Due to the large frequency error of this device at 1.8 V, the SLG46620-A is not recommended for applications requiring accurate frequency at V_{DD} below 2.2 V. This maximum frequency value is documented only to provide designers guidance on the part's expected performance at these conditions.

Note 2 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

3.6.1 OSC Power-On Delay

Table 12: Oscillators Power-On Delay

Power Supply Range (V_{DD}), V	LF OSC (1.73 kHz)		RC OSC (2 MHz)		RC OSC (25 kHz)		Ring OSC (27MHz), Bandgap enable		Ring OSC (27MHz), Bandgap disable	
	Typical Value, µs	Max. Value, µs	Typical Value, ns	Max. Value, ns	Typical Value, µs	Max. Value, µs	Typical Value, µs	Max. Value, µs	Typical Value, µs	Max. Value, µs
1.71	575.10	722.19	886.5	1335.33	41.55	45.16	0.134	0.283	48.84	328.52
3	566.94	709.98	695.5	900.10	40.56	43.36	0.089	0.151	3.09	4.41
3.3	564.91	706.96	677.5	849.62	40.51	43.11	0.087	0.156	2.31	3.19
3.6	562.19	706.39	662	810.79	40.46	43.19	0.083	0.150	1.83	2.48

Note 1 Typical values are given for T_A = 25 °C, maximum values are given for T_A = -40 °C to 105 °C.
Note 2 RC OSC Power Setting: "Auto Power-On", RC OSC Clock to Matrix Input: “Enable”.

3.7 ACMP CHARACTERISTICS

Table 13: ACMP Specifications at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Voltage Offset	Vhys = 0 mV, Gain =1, Vref = 1200 mV	T_A = 25 °C	-8.09	--	20.71	mV
				-11.77	--	20.71	mV
		Vhys = 0 mV, Gain =1, Vref = 100 mV	T_A = 25 °C	-9.34	--	5.96	mV
				-9.35	--	6.36	mV
V_{BUF_offset}	ACMP Buffer Input Voltage Offset	Vhys = 0 mV, Gain =1, Vref = 100 mV	T_A = 25 °C	-17.43	--	13.39	mV
				-23.30	--	19.34	mV
		Vhys = 0 mV, Gain =1, Vref = 600 mV	T_A = 25 °C	-17.59	--	13.15	mV
				-23.76	--	19.71	mV
		Vhys = 0 mV, Gain =1, Vref = 1200 mV	T_A = 25 °C	-39.29	--	20.62	mV
				-74.22	--	36.09	mV
t_{start}	ACMP Startup Time	ACMP Power-On delay, Minimal required wake time for the “Wake and Sleep function”	Force BG on - Disable, Output Delay - 100 µs, V_{DD} = 1.71 V	--	89.1	696.2	µs
			Force BG on - Disable, Output Delay - 100 µs, V_{DD} ≥ 3 V	--	84.2	732.6	µs
			Force BG on - Disable, Output Delay - 550 µs, V_{DD} = 1.71 V	--	421.7	3381.8	µs
			Force BG on - Disable, Output delay - 550 µs, V_{DD} ≥ 3 V	--	418.6	3349.8	µs
			Force BG on - Enable, ACMP0,1, 2, 3, 4, Vref = 50 mV to 600 mV, V_{DD} = 1.71 V	--	290.7	401.1	ns

Table 13: ACMP Specifications at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted (Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
t_{start}	ACMP Startup Time	ACMP Power-On delay, Minimal required wake time for the “Wake and Sleep function”	Force BG on - Enable, ACMP0,1, 2, 3, 4, Vref = 50 mV to 600 mV, $V_{DD} \geq 3$ V	--	194.9	280	ns
			Force BG on - Enable, ACMP0,1, 2, 3, 4, Vref = 1200 mV, V_{DD} = 1.71 V	--	469.1	1040.4	ns
			Force BG on - Enable, ACMP0,1, 2, 3, 4, Vref = 1200 mV, $V_{DD} \geq 3$ V	--	221.3	289.1	ns
			Force BG on - Enable, ACM5, Vref = 50 mV to 600 mV, V_{DD} = 1.71 V	--	405.6	514.7	ns
			Force BG on - Enable, ACMP5, Vref = 50 mV to 600 mV, $V_{DD} \geq 3$ V	--	291.4	389.2	ns
			Force BG on - Enable, ACMP5, Vref = 1200 mV, V_{DD} = 1.71 V	--	718.6	1653.6	ns
			Force BG on - Enable, ACMP5, Vref = 1200 mV, $V_{DD} \geq 3$ V	--	335.7	449.4	ns
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV V_{IL} = Vref - V_{HYS}/2 V_{IH} = Vref + V_{HYS}/2	T_A = 25 °C	10.59	--	36.5	mV
		V_{HYS} = 50 mV V_{IL} = Vref - V_{HYS} V_{IH} = Vref	T_A = 25 °C	45.57	--	59.75	mV
		V_{HYS} = 200 mV V_{IL} = Vref - V_{HYS} V_{IH} = Vin	T_A = 25 °C	193.38	--	210.47	mV
		V_{HYS} = 25 mV V_{IL} = Vref - V_{HYS}/2 V_{IH} = Vref + V_{HYS}/2		3.35	--	37.75	mV
		V_{HYS} = 50 mV V_{IL} = Vref - V_{HYS} V_{IH} = Vref		45.45	--	64	mV
		V_{HYS} = 200 mV V_{IL} = Vref - V_{HYS} V_{IH} = Vin		193.06	--	214.68	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ

Table 13: ACMP Specifications at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted (Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
G	Gain error (including threshold and internal Vref error), T_A = -40 °C to 105 °C	G = 1	Vref = 50 mV to 1200 mV	--	1	--	
		G = 0.5, V_{DD} = 1.71 V	Vref = 100 mV	-1.98	--	2.65	%
			Vref = 600 mV	-1.14	--	1.10	%
		G = 0.5, V_{DD} = 3.3 V ±10 %	Vref = 100 mV	-2.39	--	2.69	%
			Vref = 600 mV	-0.91	--	1.24	%
			Vref = 1200 mV	-0.72	--	0.92	%
		G = 0.33, V_{DD} = 1.71 V	Vref = 100 mV	-1.01	--	3.82	%
		G = 0.33, V_{DD} = 3.3 V ±10 %	Vref = 100 mV	-1.28	--	3.92	%
			Vref = 600 mV	-0.37	--	2.56	%
		G = 0.25, V_{DD} = 1.71 V	Vref = 100 mV	-2.06	--	3.11	%
		G = 0.25, V_{DD} = 3.3 V ±10 %	Vref = 100 mV	-2.32	--	3.08	%
			Vref = 600 mV	-1.03	--	1.47	%

3.8 VREF OUT CHARACTERISTICS

Table 14: Vref OUT Specifications at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
Vref OUT Error	Vref OUT through PINs 18 or 19	Vref = 100 mV	T_A = 25 °C	-10.47	--	12.72	%
				-13.92	--	11.97	%
		Vref = 600 mV	T_A = 25 °C	-1.64	--	2.26	%
				-2.35	--	2.70	%
		Vref = 1000 mV	T_A = 25 °C	-0.89	--	1.55	%
				-1.51	--	1.85	%
		Vref = 1200 mV **(Note 1)**	T_A = 25 °C	-0.85	--	1.24	%
				-1.49	--	1.48	%
Note 1 V_{DD} > 2.0 V.							

Table 15: Delay Estimated for Each ACMP at T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note		Typ		Max		Unit
				Rising	Falling	Rising	Falling	
PROP	Propagation Delay, Response Time for ACMP 0 V_{IN+} Source - Buffered PIN	Overdrive = 10 mV	V_{DD} = 1.71 V	0.98	1.17	3.72	4.49	µs
			V_{DD} = 3.3 V	0.82	0.72	1.62	1.49	µs
			V_{DD} = 3.6 V	0.83	0.75	1.67	1.56	µs
		Overdrive = 100 mV	V_{DD} = 1.71 V	0.53	0.61	3.19	3.13	µs
			V_{DD} = 3.3 V	0.36	0.37	0.69	0.78	µs
			V_{DD} = 3.6 V	0.35	0.36	0.67	0.76	µs
	Propagation Delay, Response Time for ACMP 0 to 4 V_{IN+} Source - PIN	Overdrive = 10 mV	V_{DD} = 1.71 V	1.12	1.19	2.92	2.75	µs
			V_{DD} = 3.3 V	0.90	0.94	2.30	2.00	µs
			V_{DD} = 3.6 V	0.91	0.95	2.12	2.07	µs
		Overdrive = 100 mV	V_{DD} = 1.71 V	0.35	0.27	0.73	0.42	µs
			V_{DD} = 3.3 V	0.25	0.23	0.42	0.36	µs
			V_{DD} = 3.6 V	0.25	0.23	0.45	0.41	µs
	Propagation Delay, Response Time for ACMP 5 V_{IN+} Source - PIN	Overdrive = 10 mV	V_{DD} = 1.71 V	3.27	3.28	4.66	4.62	µs
			V_{DD} = 3.3 V	3.09	3.07	4.21	4.41	µs
			V_{DD} = 3.6 V	3.08	3.07	4.24	4.42	µs
		Overdrive = 100 mV	V_{DD} = 1.71 V	0.99	0.79	1.65	1.08	µs
			V_{DD} = 3.3 V	0.76	0.71	1.07	1.00	µs
			V_{DD} = 3.6 V	0.76	0.71	1.07	1.01	µs

3.9 ADC CHARACTERISTICS INCLUDING PGA

Note: PGA input voltage should not exceed values given in Table 3.

Table 16: Single-Ended ADC Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Max	Unit
Vinp	Input Voltage Range (bit 0 to bit 255), relative to GND	G = 0.5	V_{DD} = 2.5 to 3.6 V	60	2060	mV
		G = 1		30	1030	mV
		G = 2		20	520	mV
		G = 4		15	265	mV
		G = 8		12	137	mV
ZE	Offset Zero Error **(Note 2)**	G = 0.5	T_A = 25 °C, V_{DD} = 3.3 V to 3.6 V	-3.8	+3.8	LSB
		G = 1	T_A = 25 °C	-4.9	+4.9	LSB
		G = 2		-4.3	+4.3	LSB
		G = 4		-3.3	+3.3	LSB
		G = 8		-3.7	+3.7	LSB
		G = 0.5	V_{DD} = 3.3 to 3.6 V	-5.0	+5.0	LSB
		G = 1		-6.4	+6.4	LSB
		G = 2		-6.3	+6.3	LSB
		G = 4		-8.5	+8.5	LSB
		G = 8		-14.3	+14.3	LSB
GE	Gain Error	G = 0.5	T_A = 25 °C, V_{DD} = 3.3 V to 3.6 V	-5.1	+5.1	LSB
		G = 1	T_A = 25 °C	-5.8	+5.8	LSB
		G = 2		-4.7	+4.7	LSB
		G = 4		-4.5	+4.5	LSB
		G = 8		-3.9	+3.9	LSB
		G = 0.5	V_{DD} = 3.3 to 3.6 V	-6.4	+6.4	LSB
		G = 1		-6.8	+6.8	LSB
		G = 2		-6.3	+6.3	LSB
		G = 4		-5.9	+5.9	LSB
		G = 8		-6.5	+6.5	LSB
INL	Integral Non-Linearity Error	G = 1	T_A = 25 °C	-2.3	+2.3	LSB
				-6.2	+6.2	LSB
DNL	Differential Non-Linearity	G = 1	T_A = 25 °C	-1.0	+1.0	LSB
				-2.1	+2.1	LSB

Note 1 To ensure linear operation, absolute input voltage on each pin should not exceed V_{DD} - 0.5.
Note 2 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

Table 17: Differential ADC Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Max	Unit
V_{ind}	Input Voltage Range (bit 0 to bit 255), Differential	G = 1		-500	500	mV
		G = 2		-250	250	mV
		G = 4		-125	125	mV
		G = 8		-62.5	62.5	mV
		G = 16		-31.25	31.25	mV
V_{cm}	Typical Input Common Voltage **(Note 2)**	G = 1, 2, 4, 8, 16	V_{DD} = 1.8 V ±5 %	400	550	mV
			V_{DD} = 3.3 V ±10 %	400	950	mV
ZE	Offset Zero Error **(Note 4)**	G = 1	T_A = 25 °C	-3.9	+3.9	LSB
		G = 2		-3.6	+3.6	LSB
		G = 4		-3.7	+3.7	LSB
		G = 8		-4.2	+4.2	LSB
		G = 16		-6.8	+6.8	LSB
		G = 1		-6.3	+6.3	LSB
		G = 2		-6.3	+6.3	LSB
		G = 4		-8.1	+8.1	LSB
		G = 8		-10.3	+10.3	LSB
		G = 16		-18.3	+18.3	LSB
GE	Gain Error	G = 1	T_A = 25 °C	-5.3	+5.3	LSB
		G = 2		-5.1	+5.1	LSB
		G = 4		-4,0	+4.0	LSB
		G = 8		-3.6	+3.6	LSB
		G = 16		-5.8	+5.8	LSB
		G = 1		-6.4	+6.4	LSB
		G = 2		-6.2	+6.2	LSB
		G = 4		-6.7	+6.7	LSB
		G = 8		-5.2	+5.2	LSB
		G = 16		-7.5	+7.5	LSB
INL	Integral Non-Linearity Error	G = 1	T_A = 25 °C	-2.4	+2.4	LSB
				-5.5	+5.5	LSB
		G = 2	T_A = 25 °C	-2.4	+2.4	LSB
				-5.3	+5.3	LSB
		G = 4	T_A = 25 °C	-2.5	+2.5	LSB
				-5.5	+5.5	LSB
		G = 8	T_A = 25 °C	-2.4	+2.4	LSB
				-5.6	+5.6	LSB
		G = 16	T_A = 25 °C	-3.3	+3.3	LSB
				-5.6	+5.6	LSB

Table 17: Differential ADC Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Unless Otherwise Noted (Continued)

Parameter	Description	Note	Conditions	Min	Max	Unit
DNL	Differential Non-Linearity	G = 1	T_A = 25 °C	-1.3	+1.3	LSB
				-1.3	+1.3	LSB
		G = 2	T_A = 25 °C	-1.2	+1.2	LSB
				-1.2	+1.2	LSB
		G = 4	T_A = 25 °C	-1.0	+1.0	LSB
				-1.2	+1.2	LSB
		G = 8	T_A = 25 °C	-1,0	+1.0	LSB
				-1.1	+1.1	LSB
		G = 16	T_A = 25 °C	-1.3	+1.3	LSB
				-1.3	+1.3	LSB

Note 1 V_{cm} = 500 mV.
Note 2 V_{cm} range is given for stable CMRR > 34 dB.
Note 3 To ensure linear operation, absolute input voltage on each pin should not exceed V_{DD} - 0.5.
Note 4 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

Table 18: Pseudo-Differential ADC Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Max	Unit
V_{ind}	Input Voltage Range (bit 0 to bit 255), Differential	G = 1		0	980	mV
		G = 2		0	490	mV
V_{inn}	Typical Negative input voltage range	G = 1, 2	V_{DD} = 1.8 V ±5 %	500	500	mV
			V_{DD} = 3.3 V ±10 %	500	1250	mV
ZE	Offset Zero Error (Note 4)	G = 1	T_A = 25 °C, V_{DD} = 3.3 to 3.6 V	-3.1	+3.1	LSB
		G = 2	T_A = 25 °C	-2.7	+2.7	LSB
		G = 1	V_{DD} = 3.3 to 3.6 V	-5.3	+5.3	LSB
		G = 2		-6.5	+6.5	LSB
GE	Gain Error	G = 1	T_A = 25 °C, V_{DD} = 3.3 to 3.6 V	-3.5	+3.5	LSB
		G = 2	T_A = 25 °C	-5.0	+5.0	LSB
		G = 1	V_{DD} = 3.3 to 3.6 V	-6.2	+6.2	LSB
		G = 2		-6.8	+6.8	LSB
INL	Integral Non-Linearity Error	G = 1	T_A = 25 °C, V_{DD} = 3.3 to 3.6 V	-2.2	+2.2	LSB
			V_{DD} = 3.3 to 3.6 V	-3.2	+3.2	LSB
		G = 2	T_A = 25 °C	-2.6	+2.6	LSB
				-3.2	+3.2	LSB
DNL	Differential Non-Linearity	G = 1	T_A = 25 °C, V_{DD} = 3.3 to 3.6 V	-1.1	+1.1	LSB
			V_{DD} = 3.3 to 3.6 V	-1.1	+1.1	LSB
		G = 2	T_A = 25 °C	-1.1	+1.1	LSB
				-1.1	+1.1	LSB

Table 18: Pseudo-Differential ADC Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Max	Unit
Note 1 V_{cm} = 500 mV. **Note 2** V_{inn} is given for convenience instead of V_{cm}. **Note 3** To ensure linear operation, absolute input voltage on each pin should not exceed V_{DD}-0.5. **Note 4** Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.						

3.10 PGA SPECIFICATIONS

Note 1: PGA input voltage should not exceed values given in section 3.1.

Table 19: Single-Ended PGA Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{os}	Offset Voltage (RTI **(Note 1)**) **(Note 3)**	G = 0.5	T_A = 25 °C, V_{DD} = 3.3 V to 3.6 V	-24.65	1.15	+27.61	mV
		G = 1	T_A = 25 °C	-9.59	0.95	+13.52	mV
		G = 2	T_A = 25 °C	-14.76	-0.80	+12.45	mV
		G = 4	T_A = 25 °C	-13.74	-1.02	+10.38	mV
		G = 8	T_A = 25 °C	-13.47	-1.31	+10.48	mV
		G = 0.5	V_{DD} = 3.3 V to 3.6 V	-34.49	1.20	+33.34	mV
		G = 1		-12.83	0.91	+15.37	mV
		G = 2		-20.13	0.77	+14.77	mV
		G = 4		-18.42	1.04	+11.53	mV
		G = 8		-18.57	1.23	+12.25	mV
ΔG	Gain Error	G = 0.5	V_{DD} = 3.3 V to 3.6 V	-0.8	0.2	1.1	%
		G = 1		-0.2	0	0.1	%
		G = 2		-1.5	-0.3	1.0	%
		G = 4		-2.3	-0.6	0.9	%
		G = 8		-4.0	-1.3	0.8	%
Vsw	Output Voltage Swing			--	50 to 1380	--	mV
V_{OUT_LIN}	Linear Output Voltage Range **(Note 2)**	G = 0.5	V_{DD} 3.3 V to 3.6 V	56.65	--	1257	mV
		G = 1		80.10	--	1155	mV
		G = 2		97.83	--	1159	mV
		G = 4		108.5	--	1156	mV
		G = 8		144.1	--	1143	mV

Note 1 RTI - referred to input.
Note 2 Gain Error < 10 %.
Note 3 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

Table 20: Differential PGA Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{os}	Offset Voltage (RTO, **(Note 2)**)	All gains	V_{id} = 0	--	550	--	mV
ΔVos	Offset Voltage Error (RTO) **(Note 4)**	G = 1	T_A = 25 °C	-3.07	0.86	+5.64	mV
		G = 2	T_A = 25 °C	-4.01	0.80	+5.96	mV
		G = 4	T_A = 25 °C	-5.84	0.57	+8.10	mV
		G = 8	T_A = 25 °C	-9.83	0.28	+12.05	mV
		G = 16	T_A = 25 °C	-21.57	-0.26	+23.96	mV
		G = 1		-15.07	0.14	+12.38	mV
		G = 2		-16.99	0.18	+14.37	mV
		G = 4		-23.44	0.18	+20.45	mV
		G = 8		-38.27	0.13	+35.20	mV
		G = 16		-70.14	-0.06	+70.15	mV
ΔG	Gain Error	G = 1		-1.4	-0.2	0.9	%
		G = 2		-2.0	-0.5	0.9	%
		G = 4		-2.5	-0.9	0.6	%
		G = 8		-3.9	-1.5	0.4	%
		G = 16		-4.3	-1.8	0.6	%
CMRR	Common-Mode Rejection Rate	G = 1		--	57	--	dB
		G = 2		--	57	--	dB
		G = 4		--	56	--	dB
		G = 8		--	55	--	dB
		G = 16		--	51	--	dB
ICMR	Input Common Mode Range	All gains		See Figure 22			
Vsw	Output Voltage Swing			--	50 to 1380	--	mV
V_{OUT_LIN}	Linear Output Voltage Range **(Note 3)**	G = 1		101.5	--	1262	mV
		G = 2		102.8	--	1262	mV
		G = 4		109.8	--	1266	mV
		G = 8		156.6	--	1327	mV
		G = 16		156.6	--	1327	mV

Note 1 ADC - Power-On, Vcm = 500 mV.
Note 2 RTO - referred to output.
Note 3 Gain Error < 10 %.
Note 4 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

Table 21: Pseudo-Differential PGA Operation, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{os}	Offset Voltage (RTO) **(Note 2)**	All gains	V_{id} = 0	--	180	--	mV
ΔVos	Offset Voltage Error (RTO) **(Note 4)**	G = 1	T_A = 25 °C	-2.53	0.68	+5.43	mV
		G = 2	T_A = 25 °C	-3.78	0.64	+7.19	mV
		G = 1		-12.75	0.50	+13.70	mV
		G = 2		-16.04	0.43	+17.09	mV
ΔG	Gain Error	G = 1		-3.0	-0.3	1.1	%
		G = 2		-2.2	-0.5	0.9	%
CMRR	Common-Mode Rejection Rate	G = 1		--	56	--	dB
		G = 2		--	57	--	dB
Vinn	Negative Input Voltage Range	All gains		See Figure 23 and Figure 24			
Vsw	Output Voltage Swing			--	50 to 1380	--	mV
V_{OUT_LIN}	Linear Output Voltage Range **(Note 3)**	G = 1		83.75	--	1252	mV
		G = 2		96.38	--	1155	mV

Note 1 ADC - Power-On, Vinn = 500 mV.
Note 2 RTO - Referred to output.
Note 3 Gain Error < 10 %.
Note 4 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

Table 22: Differential/Pseudo-Differential PGA Mode, T_A = -40 °C to 105 °C, V_{DD} = 1.71 V to 3.6 V, Typical Values are at T_A = 25 °C, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{os}	Offset Voltage (RTI **(Note 2)**)	All gains	T_A = 25 °C, V_{DD} = 3.3 V	--	±1.9	--	mV
ΔG	Gain Error	G = 1		--	-0.2	--	%
		G = 2		--	-0.5	--	%
		G = 4		--	-0.9	--	%
		G = 8		--	-1.5	--	%
		G = 16		--	-1.8	--	%

Note 1 ADC - Power-down, Vcm = 500 mV.
Note 2 RTI - referred to input.
Note 3 When ADC is powered down, PGA operation in Differential or Pseudo-Differential mode is not recommended. Parameters in Table 22 are for reference only.

4 User Programmability

The SLG46620-A is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

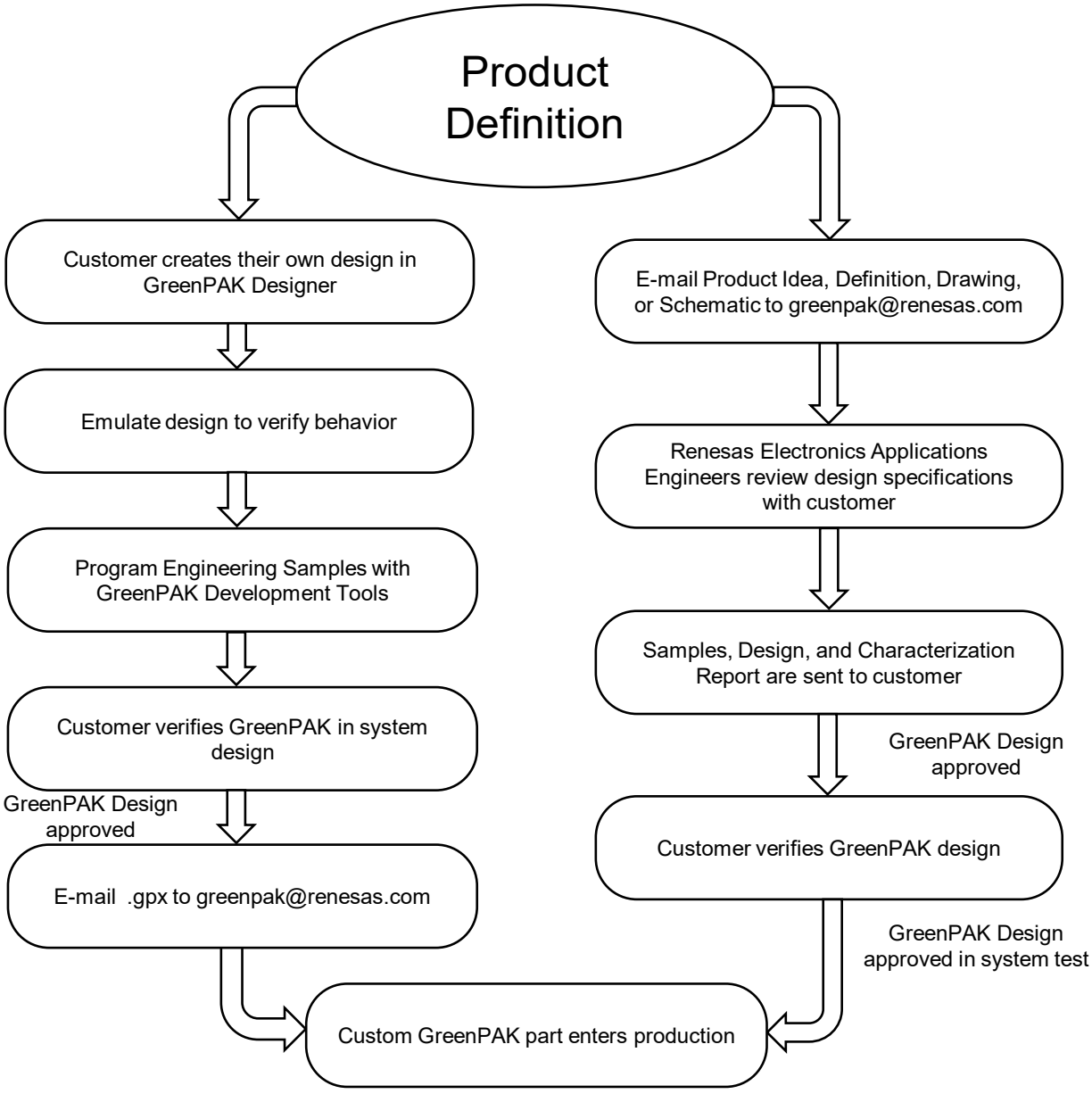


Figure 1: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG46620-A has a total of 18 multi-function IO pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM). Refer to section 2 for normal mode pin definitions

Of the 18 user defined IO pins on the SLG46620-A, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin or external reset.

5.1 INPUT MODES

Each IO pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input. Pins 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 14, 15, 16 and 17 can also be configured to serve as analog inputs to the on-chip comparators. Pins 18 and 19 can also be configured as analog reference voltage outputs.

5.2 OUTPUT MODES

Pins 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 14, 15, 16, 17, 18, 19, and 20 can all be configured as digital output pins.

5.3 PULL-UP/DOWN RESISTORS

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of all IO pins, the internal resistors can be configured as either Pull-up or Pull-downs.

5.4 GPI STRUCTURE

5.4.1 GPI Structure (for Pin 2)

Input Mode [1:0]
00: Digital IN without Schmitt Trigger, WOSMT_EN = 1, OE = 0
01: Digital IN with Schmitt Trigger, SMT_EN = 1, OE = 0
10: Low Voltage Digital IN mode, LV_EN = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user.
Note 2: OE is Matrix output, Digital IN is Matrix input.

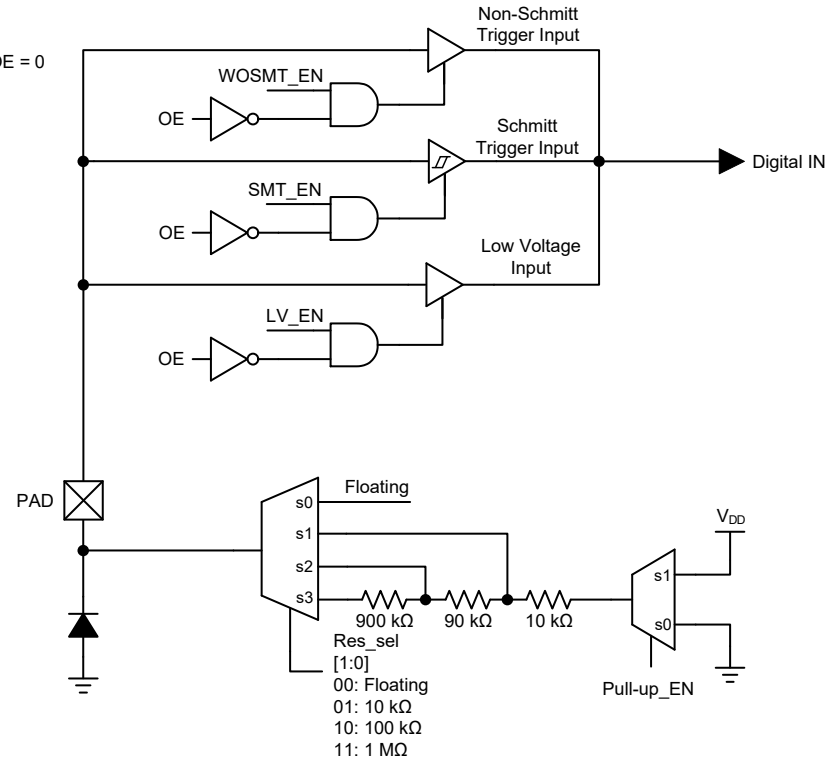


Figure 2: PIN 2 GPI Structure Diagram

5.5 MATRIX OE IO STRUCTURE

5.5.1 Matrix OE IO Structure (for Pins 3, 5, 7, 9, 13, 14, 16, 18, 19)

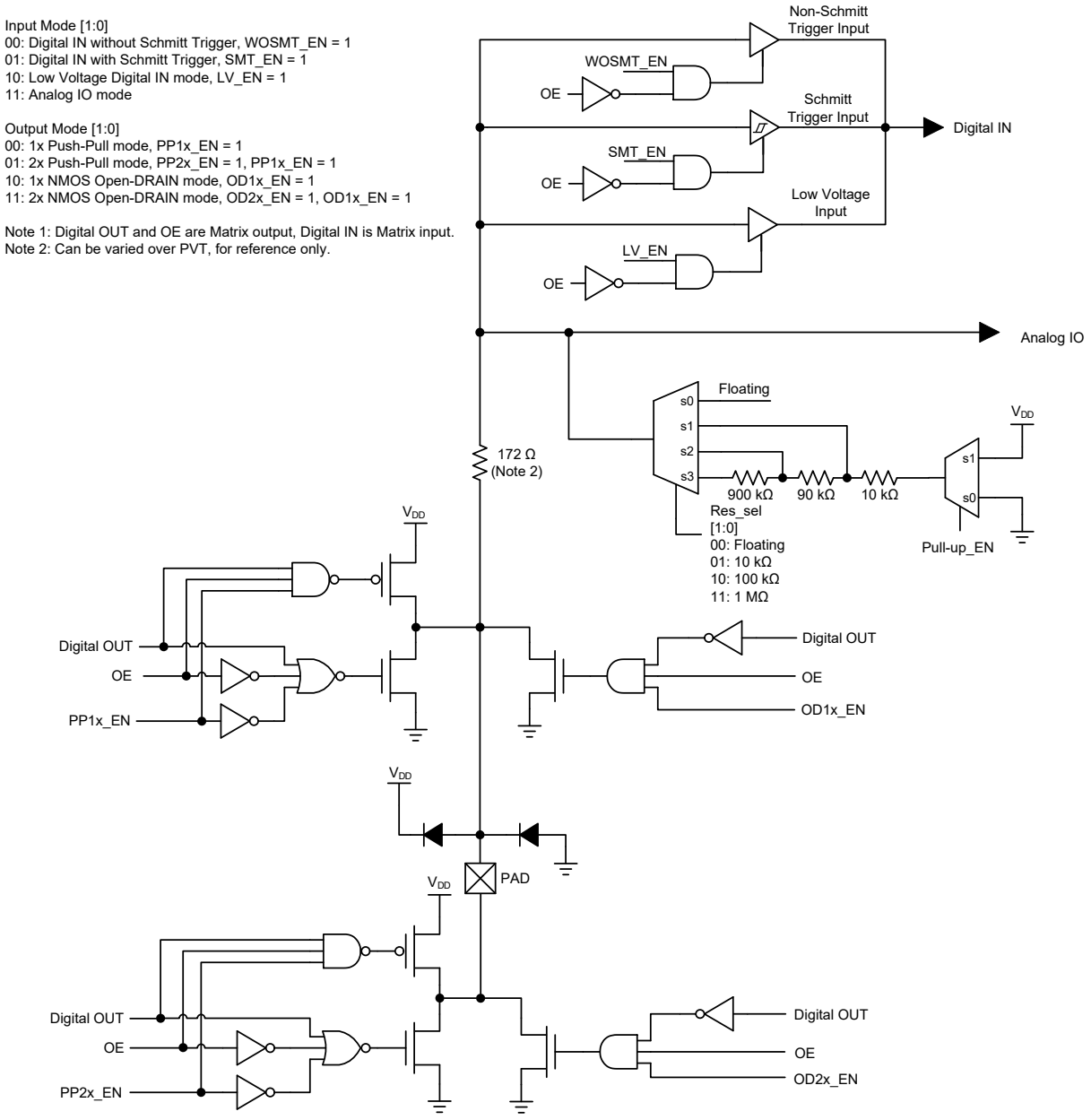


Figure 3: Matrix OE IO Structure Diagram

5.5.2 Matrix OE 4x Drive Structure (for Pin 10)

Input Mode [1:0]
00: Digital IN without Schmitt Trigger, WOSMT_EN = 1
01: Digital IN with Schmitt Trigger, SMT_EN = 1
10: Low Voltage Digital IN mode, LV_EN = 1
11: Analog IO mode

Output Mode [1:0]
00: 1x Push-Pull mode, PP1x_EN = 1
01: 2x Push-Pull mode, PP2x_EN = 1, PP1x_EN = 1
10: 1x NMOS Open-DRAIN mode, OD1x_EN = 1, ODn_EN = 1
11: 2x NMOS Open-DRAIN mode, OD2x_EN = 1, OD1x_en = 1, ODn_EN = 1

Note 1: Digital OUT and OE are Matrix output, Digital IN is Matrix input.
Note 2: Can be varied over PVT, for reference only.

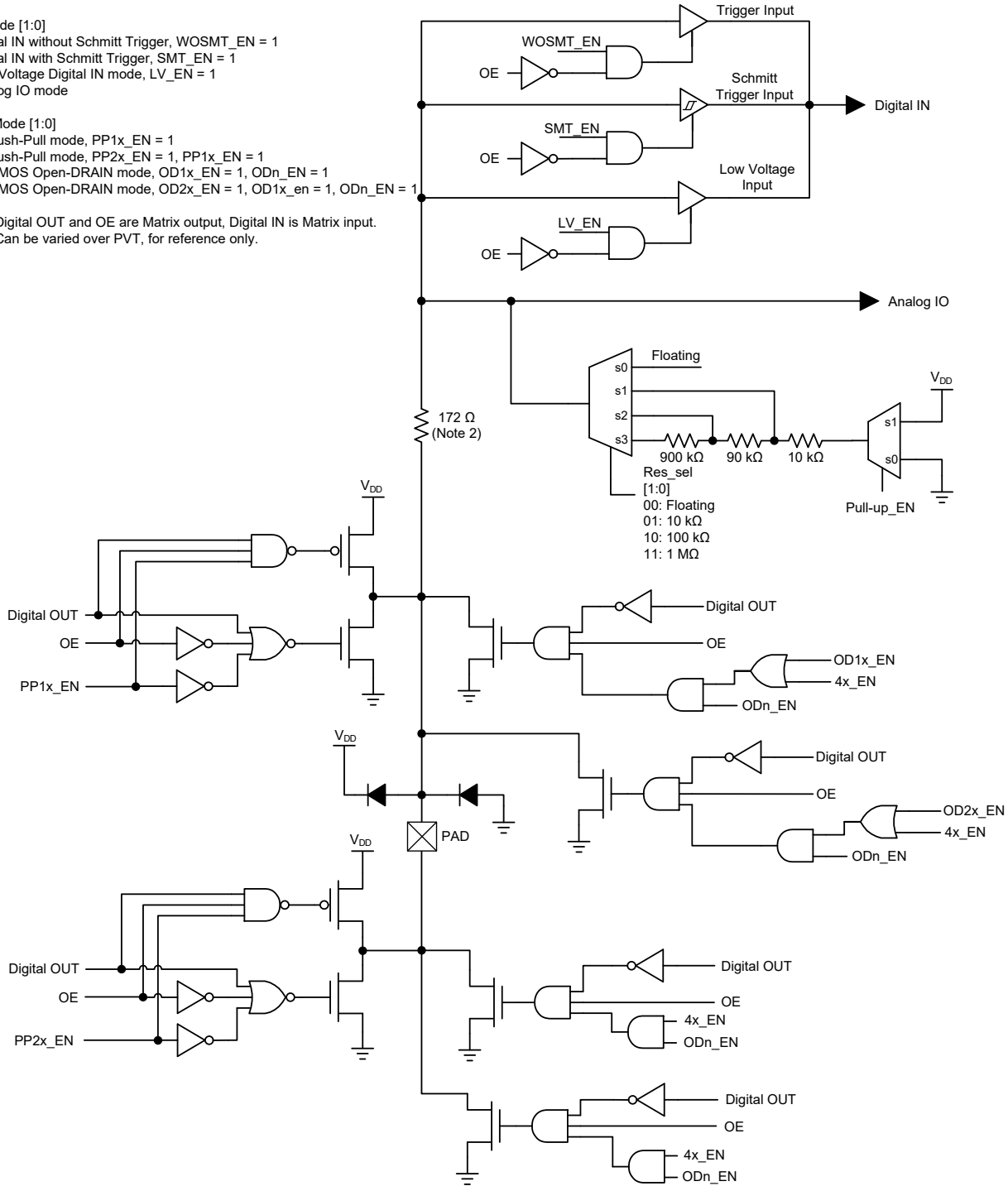


Figure 4: Matrix OE IO 4x Drive Structure Diagram

5.6 REGISTER OE IO STRUCTURE

5.6.1 Register OE IO Structure (for Pins 4, 6, 8, 15, 17, 20)

Mode [2:0]
000: Digital IN without Schmitt Trigger, WOSMT_EN = 1, OE = 0
001: Digital IN with Schmitt Trigger, SMT_EN = 1, OE = 0
010: Low Voltage Digital IN mode, LV_EN = 1, OE = 0
011: Analog IO mode
100: Push-Pull mode, PP_EN = 1, OE = 1
101: NMOS Open-DRAIN mode, ODn_EN = 1, OE = 1
110: PMOS Open-DRAIN mode, ODp_EN = 1, OE = 1
111: Analog IO and NMOS Open-DRAIN mode, ODn_EN = 1 and AIO_EN = 1

Note 1: OE cannot be selected by user.
Note 2: Can be varied over PVT, for reference only.
Note 3: Digital OUT and OE are Matrix output, Digital IN is Matrix input.

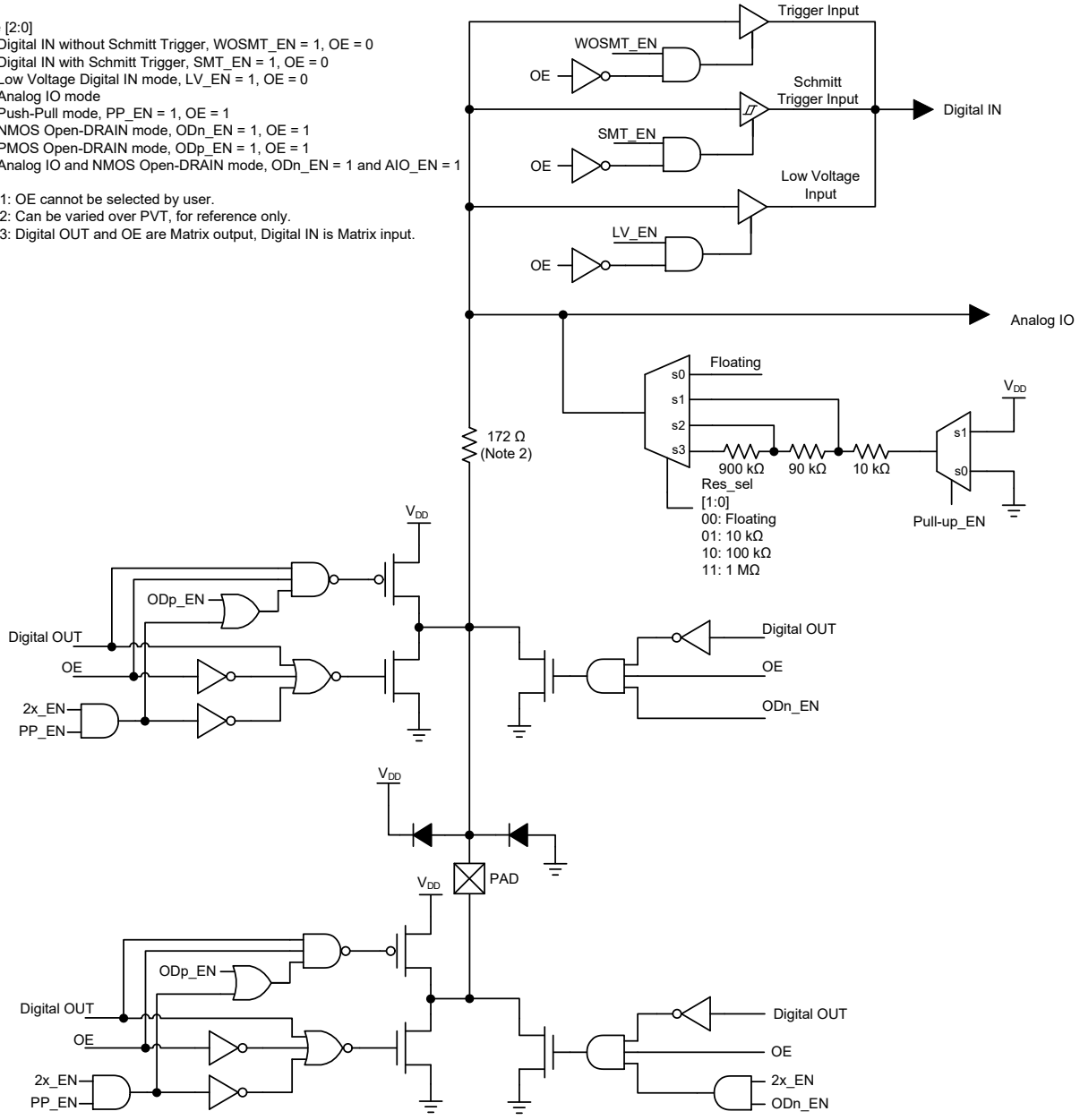


Figure 5: Register IO Structure Diagram

5.6.2 Register OE 4x Drive Structure (for Pin 12)

Mode [2:0]
000: Digital IN without Schmitt Trigger, WOSMT_EN = 1, OE = 0
001: Digital IN with Schmitt Trigger, SMT_EN = 1, OE = 0
010: Low Voltage Digital IN mode, LV_EN = 1, OE = 0
011: Analog IO mode
100: Push-Pull mode, PP_EN = 1, OE = 1
101: NMOS Open-DRAIN mode, ODn_EN = 1, OE = 1
110: PMOS Open-DRAIN mode, ODp_EN = 1, OE = 1
111: Analog IO and NMOS Open-DRAIN mode, odn_EN = 1 and AIO_EN = 1

Note 1: OE cannot be selected by user.
Note 2: Digital OUT and OE are Matrix output, Digital IN is Matrix input.
Note 3: Can be varied over PVT, for reference only.

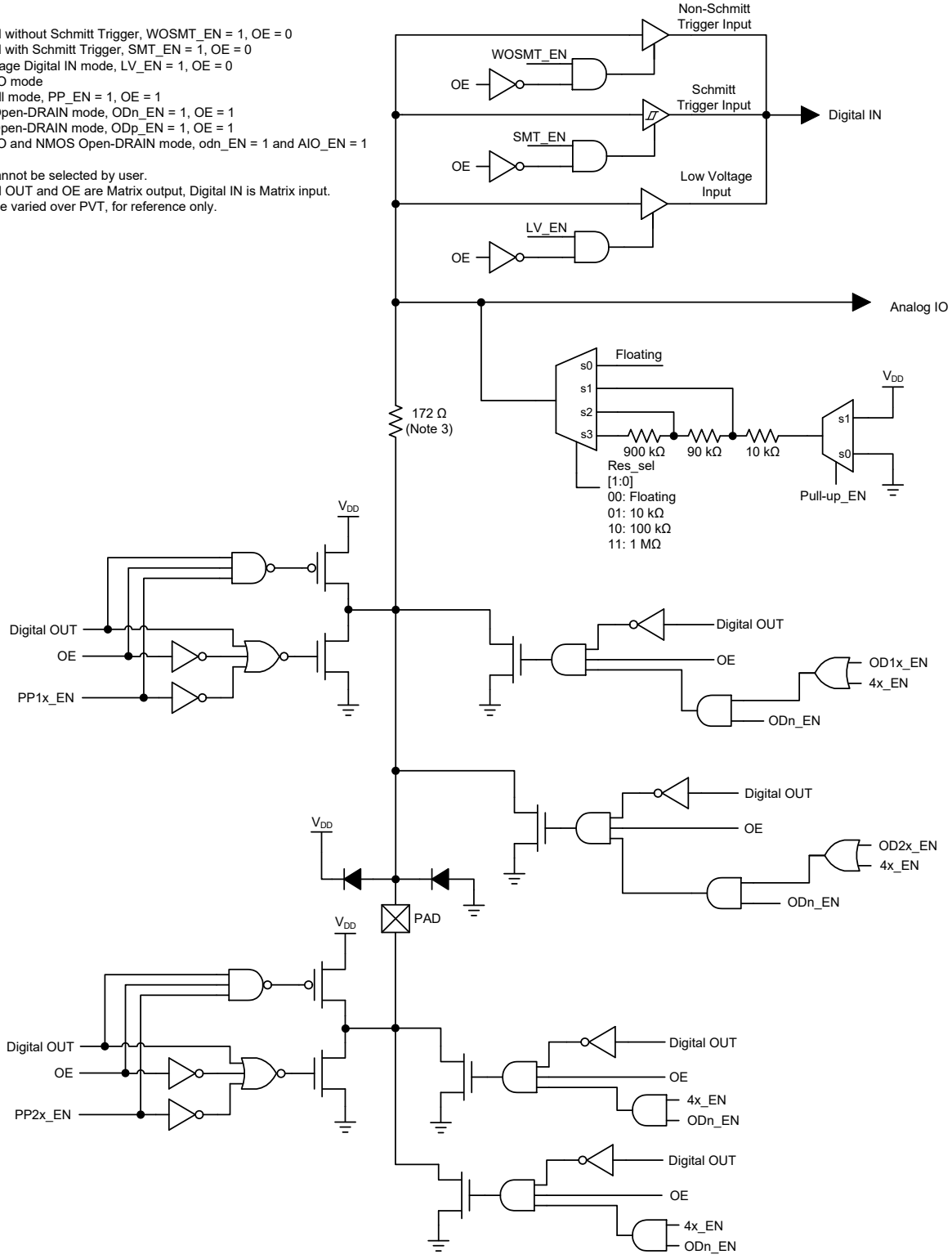


Figure 6: Register OE 4x Drive Structure Diagram

5.7 IO TYPICAL PERFORMANCE

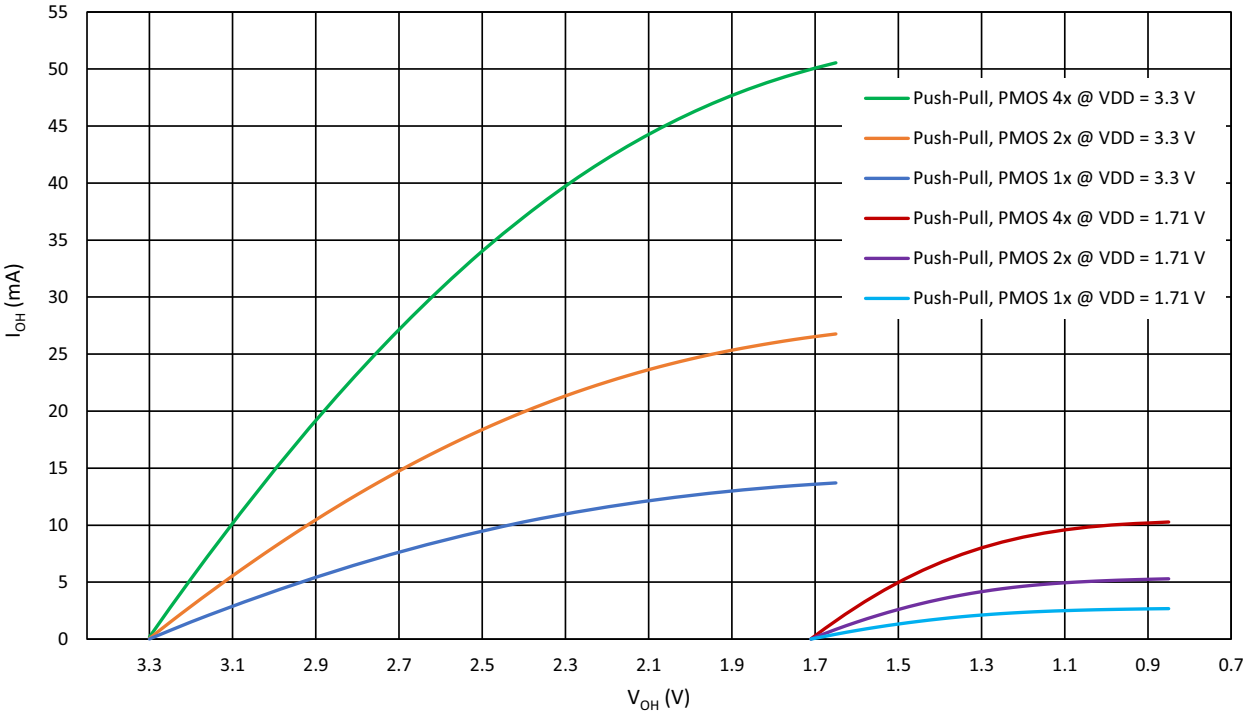


Figure 7: Typical High Level Output Current vs. High Level Output Voltage at T_A = 25 °C

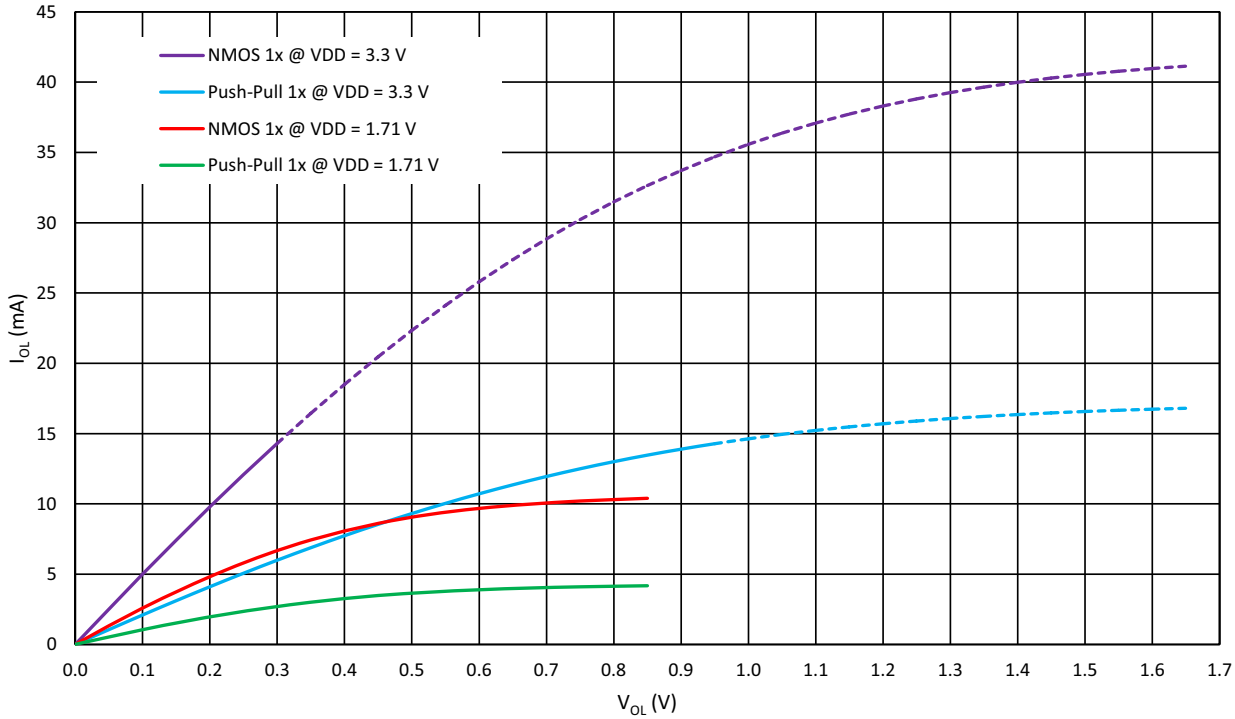


Figure 8: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C

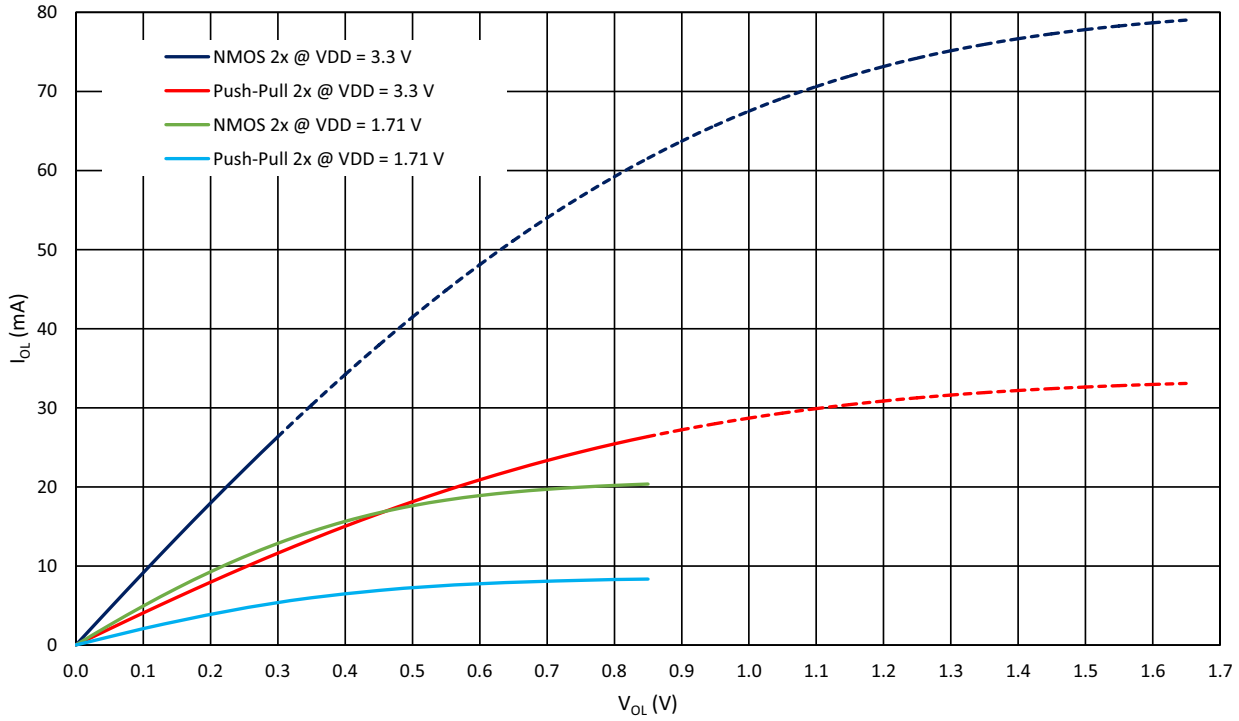


Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C

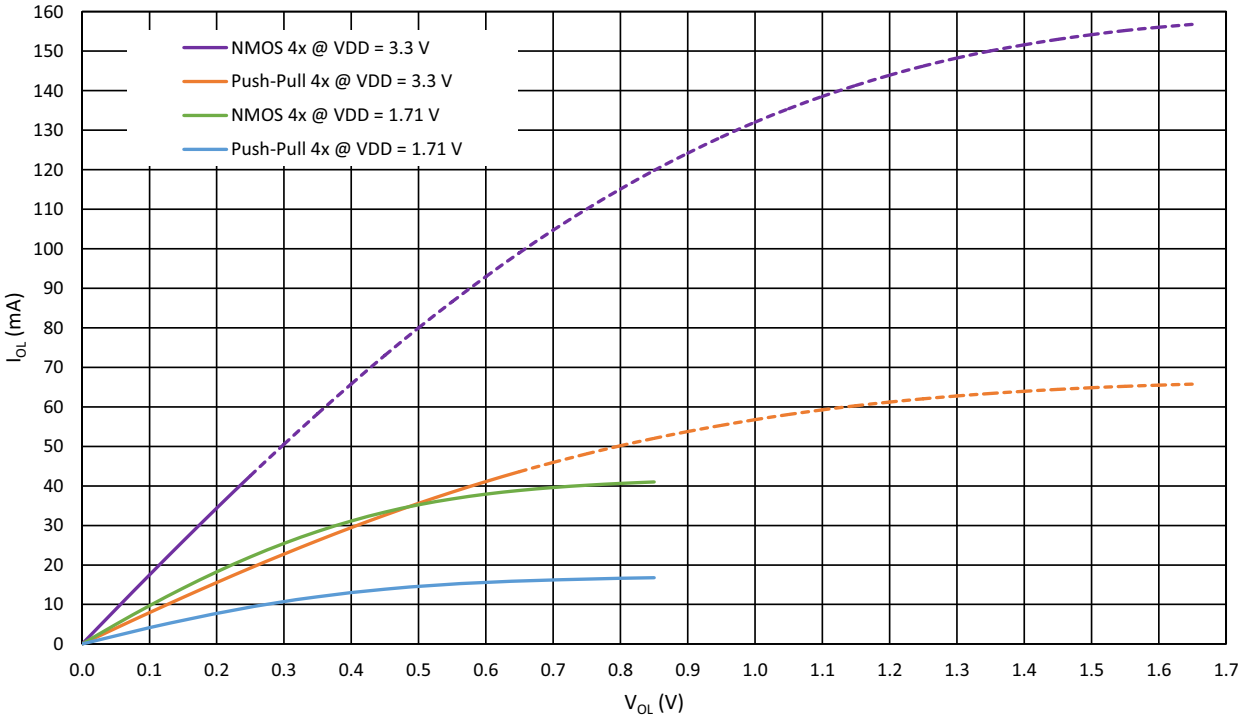


Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 4x Drive at T_A = 25 °C

6 Connection Matrix

The SLG46620-A has two Connection Matrices, which are used to create the internal routing for internal digital signals inside the device, once it is programmed. The registers are programmed from the one-time NVM cells during Test Mode Operation. All of the connection points for each logic cell within the SLG46620-A have a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the SLG46620-A are programmed, a fully custom circuit will be created.

Each Connection Matrix within the device has 64 inputs and 95 outputs. Each of the 64 inputs to each Connection Matrix is hard-wired to the digital output of a particular source macrocell, including I/O pins, LUTs, ADC, analog comparators, other digital macrocells and V_{DD} and VSS. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines. All macrocells associated with a particular matrix has both its inputs and outputs connected to that matrix. To make connections to macrocells associated with the other matrix, the user can select the Matrix Cross Connection lines (see Figure 11).

Each matrix has 10 dedicated output connections for connecting to the other matrix, known as the “Cross Connection “outputs. When using these cross connections, any macrocell can be connected to any other macrocell in the device by first going through the other matrix. As there is fixed number of the Matrix Cross Connections, it is important when making connections of the outputs of macrocells to the inputs of other macrocells that this is done within the same matrix whenever possible. This will leave the Matrix Cross Connection lines free for digital connections to resources associated with the other matrix.

For a complete list of the SLG46620-A’s register table, see section 23.

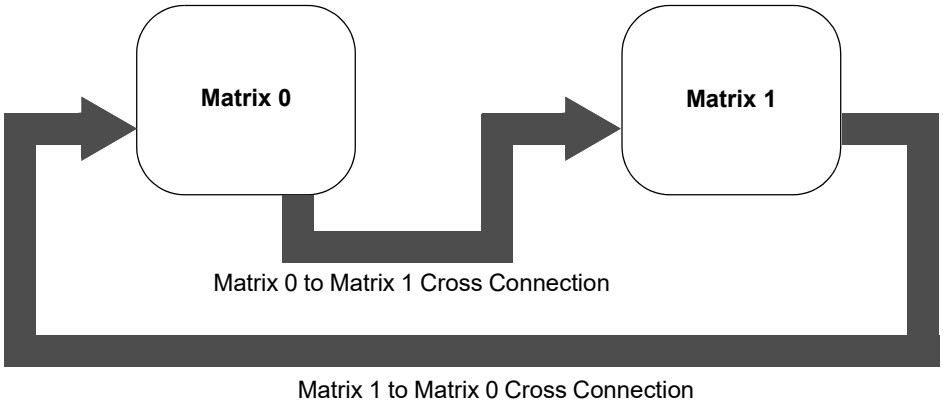
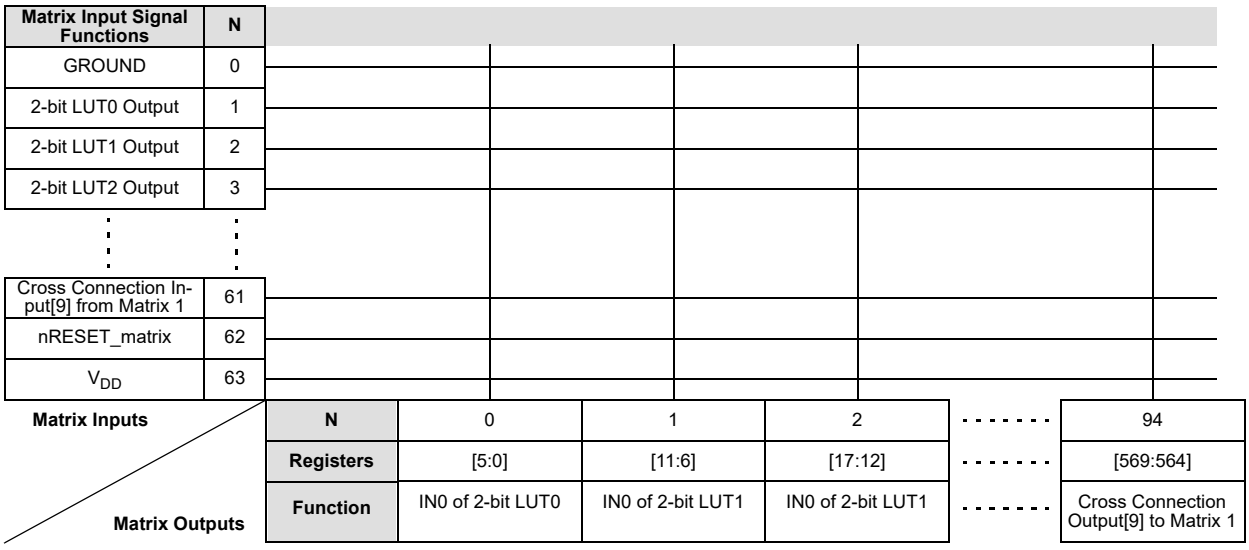


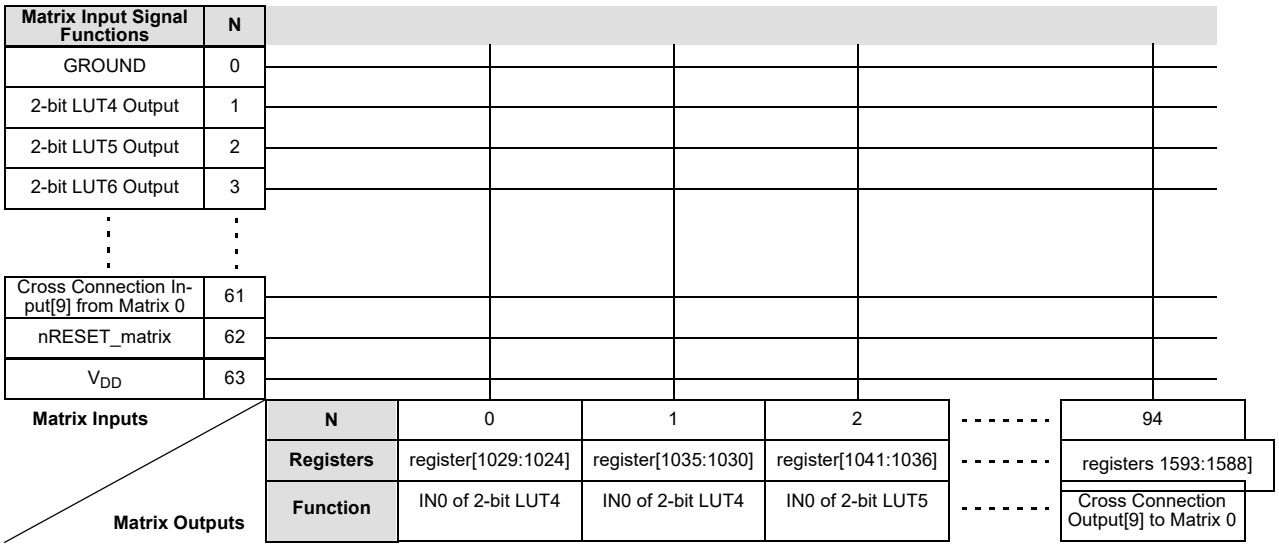
Figure 11: Matrix Cross Connection Block Diagram



Matrix Input Signal Functions	N
GROUND	0
2-bit LUT0 Output	1
2-bit LUT1 Output	2
2-bit LUT2 Output	3
⋮	⋮
Cross Connection Input[9] from Matrix 1	61
nRESET_matrix	62
V_{DD}	63

Matrix Inputs / Matrix Outputs	N	0	1	2	⋯	94
	Registers	[5:0]	[11:6]	[17:12]	⋯	[569:564]
	Function	IN0 of 2-bit LUT0	IN0 of 2-bit LUT1	IN0 of 2-bit LUT1	⋯	Cross Connection Output[9] to Matrix 1

Figure 12: Connection Matrix 0



Matrix Input Signal Functions	N
GROUND	0
2-bit LUT4 Output	1
2-bit LUT5 Output	2
2-bit LUT6 Output	3
⋮	⋮
Cross Connection Input[9] from Matrix 0	61
nRESET_matrix	62
V_{DD}	63

Matrix Inputs / Matrix Outputs	N	0	1	2	⋯	94
	Registers	register[1029:1024]	register[1035:1030]	register[1041:1036]	⋯	registers 1593:1588]
	Function	IN0 of 2-bit LUT4	IN0 of 2-bit LUT4	IN0 of 2-bit LUT5	⋯	Cross Connection Output[9] to Matrix 0

Figure 13: Connection Matrix 1

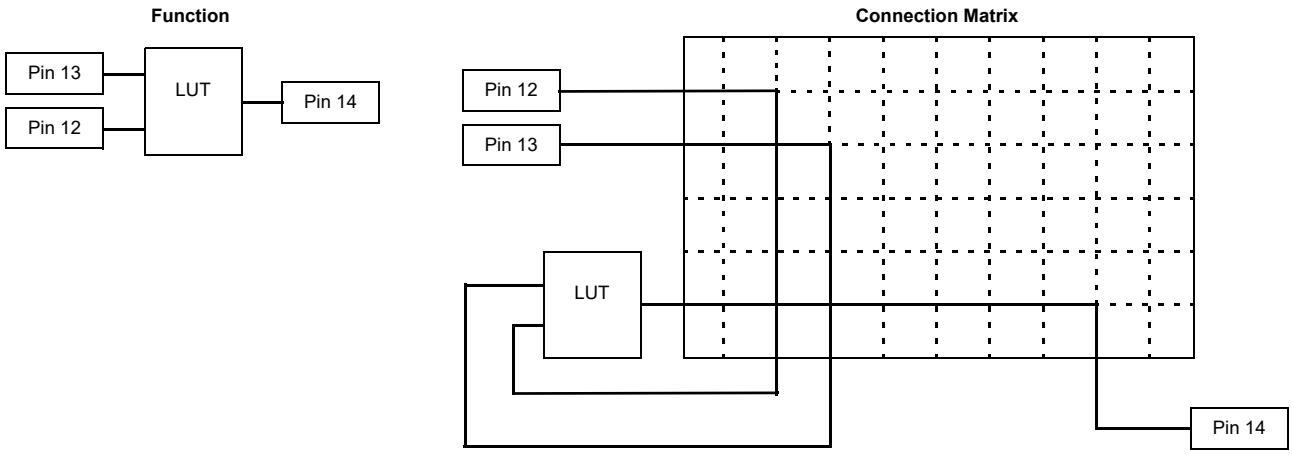


Figure 14: Connection Matrix Example

6.1 MATRIX INPUT 0 TABLE

Table 23: Matrix 0 Input Table

N	Matrix 0 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GROUND	0	0	0	0	0	0
1	2-bit LUT0 Output	0	0	0	0	0	1
2	2-bit LUT1 Output	0	0	0	0	1	0
3	2-bit LUT2 Output	0	0	0	0	1	1
4	2-bit LUT3 Output	0	0	0	1	0	0
5	3-bit LUT0 Output	0	0	0	1	0	1
6	3-bit LUT1 Output	0	0	0	1	1	0
7	3-bit LUT2 Output	0	0	0	1	1	1
8	3-bit LUT3 Output	0	0	1	0	0	0
9	3-bit LUT4 Output	0	0	1	0	0	1
10	3-bit LUT5 Output	0	0	1	0	1	0
11	3-bit LUT6 Output	0	0	1	0	1	1
12	3-bit LUT7 Output	0	0	1	1	0	0
13	4-bit LUT0/PGEN Output	0	0	1	1	0	1
14	DFF0/LATCH0 Output	0	0	1	1	1	0
15	DFF1/LATCH1 Output	0	0	1	1	1	1
16	DFF2/LATCH2 Output	0	1	0	0	0	0
17	DFF3/LATCH3 Output	0	1	0	0	0	1
18	DFF4/LATCH4 Output	0	1	0	0	1	0
19	DFF5/LATCH5 Output	0	1	0	0	1	1
20	Pipe Delay 0 Out0	0	1	0	1	0	0
21	Pipe Delay 0 Out1	0	1	0	1	0	1
22	Edge Detect Programmable Delay 0 Output	0	1	0	1	1	0
23	Inverter 0 Output	0	1	0	1	1	1
24	Pin2 Digital Output	0	1	1	0	0	0
25	Pin3 Digital Output	0	1	1	0	0	1
26	Pin4 Digital Output	0	1	1	0	1	0
27	Pin5 Digital Output	0	1	1	0	1	1
28	Pin6 Digital Output	0	1	1	1	0	0
29	Pin7 Digital Output	0	1	1	1	0	1
30	Pin8 Digital Output	0	1	1	1	1	0
31	Pin9 Digital Output	0	1	1	1	1	1
32	Pin10 Digital Output	1	0	0	0	0	0
33	ACMP0 Output	1	0	0	0	0	1
34	ACMP4 Output	1	0	0	0	1	0
35	ACMP5 Output	1	0	0	0	1	1
36	DLY0/CNT0 Output	1	0	0	1	0	0
37	DLY2/CNT2 Output	1	0	0	1	0	1

Table 23: Matrix 0 Input Table (Continued)

N	Matrix 0 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	DLY5/CNT5 Output	1	0	0	1	1	0
39	DLY6/CNT6 Output	1	0	0	1	1	1
40	DLY9/CNT9 Output	1	0	1	0	0	0
41	Sig_BG_OK	1	0	1	0	0	1
42	Power Detector Output	1	0	1	0	1	0
43	ADC interrupt	1	0	1	0	1	1
44	SPI interrupt	1	0	1	1	0	0
45	GROUND	1	0	1	1	0	1
46	GROUND	1	0	1	1	1	0
47	GROUND	1	0	1	1	1	1
48	Ring Oscillator Output	1	1	0	0	0	0
49	RC Oscillator Output	1	1	0	0	0	1
50	Low Frequency Oscillator Output	1	1	0	0	1	0
51	GROUND	1	1	0	0	1	1
52	Cross Connection Input from Matrix 1 [0]	1	1	0	1	0	0
53	Cross Connection Input from Matrix 1 [1]	1	1	0	1	0	1
54	Cross Connection Input from Matrix 1 [2]	1	1	0	1	1	0
55	Cross Connection Input from Matrix 1 [3]	1	1	0	1	1	1
56	Cross Connection Input from Matrix 1 [4]	1	1	1	0	0	0
57	Cross Connection Input from Matrix 1 [5]	1	1	1	0	0	1
58	Cross Connection Input from Matrix 1 [6]	1	1	1	0	1	0
59	Cross Connection Input from Matrix 1 [7]	1	1	1	0	1	1
60	Cross Connection Input from Matrix 1 [8]	1	1	1	1	0	0
61	Cross Connection Input from Matrix 1 [9]	1	1	1	1	0	1
62	nReset_Matrix	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 MATRIX 0 OUTPUT TABLE

Table 24: Matrix 0 Output Table

Register Bit Address	Matrix 0 Output Signal Function	Matrix Output Number
[5:0]	Matrix 0 OUT: In0 of 2-bit LUT0	0
[11:6]	Matrix 0 OUT: In1 of 2-bit LUT0	1
[17:12]	Matrix 0 OUT: In0 of 2-bit LUT1	2
[23:18]	Matrix 0 OUT: In1 of 2-bit LUT1	3
[29:24]	Matrix 0 OUT: In0 of 2-bit LUT2	4
[35:30]	Matrix 0 OUT: In1 of 2-bit LUT2	5
[41:36]	Matrix 0 OUT: In0 of 2-bit LUT3	6
[47:42]	Matrix 0 OUT: In1 of 2-bit LUT3	7
[53:48]	Matrix 0 OUT: In0 of 3-bit LUT0	8
[59:54]	Matrix 0 OUT: In1 of 3-bit LUT0	9
[65:60]	Matrix 0 OUT: In2 of 3-bit LUT0	10
[71:66]	Matrix 0 OUT: In0 of 3-bit LUT1	11
[77:72]	Matrix 0 OUT: In1 of 3-bit LUT1	12
[83:78]	Matrix 0 OUT: In2 of 3-bit LUT1	13
[89:84]	Matrix 0 OUT: In0 of 3-bit LUT2	14
[95:90]	Matrix 0 OUT: In1 of 3-bit LUT2	15
[101:96]	Matrix 0 OUT: In2 of 3-bit LUT2	16
[107:102]	Matrix 0 OUT: In0 of 3-bit LUT3	17
[113:108]	Matrix 0 OUT: In1 of 3-bit LUT3	18
[119:114]	Matrix 0 OUT: In2 of 3-bit LUT3	19
[125:120]	Matrix 0 OUT: In0 of 3-bit LUT4	20
[131:126]	Matrix 0 OUT: In1 of 3-bit LUT4	21
[137:132]	Matrix 0 OUT: In2 of 3-bit LUT4	22
[143:138]	Matrix 0 OUT: In0 of 3-bit LUT5	23
[149:144]	Matrix 0 OUT: In1 of 3-bit LUT5	24
[155:150]	Matrix 0 OUT: In2 of 3-bit LUT5	25
[161:156]	Matrix 0 OUT: In0 of 3-bit LUT6	26
[167:162]	Matrix 0 OUT: In1 of 3-bit LUT6	27
[173:168]	Matrix 0 OUT: In2 of 3-bit LUT6	28
[179:174]	Matrix 0 OUT: In0 of 3-bit LUT7	29
[185:180]	Matrix 0 OUT: In1 of 3-bit LUT7	30
[191:186]	Matrix 0 OUT: In2 of 3-bit LUT7	31
[197:192]	Matrix 0 OUT: In0 of 4-bit LUT0	32
[203:198]	Matrix 0 OUT: In1 of 4-bit LUT0	33
[209:204]	Matrix 0 OUT: In2 of 4-bit LUT0 or PGEN CLK	34
[215:210]	Matrix 0 OUT: In3 of 4-bit LUT0 or PGEN nRST	35
[221:216]	Matrix 0 OUT: nSET or nRST of DFF0/Latch0	36
[227:222]	Matrix 0 OUT: Data of DFF0/Latch0	37

Table 24: Matrix 0 Output Table (Continued)

Register Bit Address	Matrix 0 Output Signal Function	Matrix Output Number
[233:228]	Matrix 0 OUT: Clock of DFF0/Latch0	38
[239:234]	Matrix 0 OUT: nSET or nRST of DFF1/Latch1	39
[245:240]	Matrix 0 OUT: Data of DFF1/Latch1	40
[251:246]	Matrix 0 OUT: Clock of DFF1/Latch1	41
[257:252]	Matrix 0 OUT: nSET or nRST of DFF2/LatcOUTh2	42
[263:258]	Matrix 0 OUT: Data of DFF2/Latch2	43
[269:264]	Matrix 0 OUT: Clock of DFF2/Latch2	44
[275:270]	Matrix 0 OUT: Data of DFF3/Latch3	45
[281:276]	Matrix 0 OUT: Clock of DFF3/Latch3	46
[287:282]	Matrix 0 OUT: Data of DFF4/Latch4	47
[293:288]	Matrix 0 OUT: Clock of DFF4/Latch4	48
[299:294]	Matrix 0 OUT: Data of DFF5/Latch5	49
[305:300]	Matrix 0 OUT: Clock of DFF5/Latch5	50
[311:306]	Matrix 0 OUT: Clock of Pipe Delay 0	51
[317:312]	Matrix 0 OUT: Input Data of Pipe Delay 0	52
[323:318]	Matrix 0 OUT: Reset of Pipe Delay 0	53
[329:324]	Matrix 0 OUT: Input of Edge Detector and Programmable Delay 0	54
[335:330]	Matrix 0 OUT: Input of Inverter 0	55
[341:336]	Matrix 0 OUT: Digital Output of Pin3	56
[347:342]	Matrix 0 OUT: OE of Pin3	57
[353:348]	Matrix 0 OUT: Digital Output of Pin4	58
[359:354]	Matrix 0 OUT: Digital Output of Pin5	59
[365:360]	Matrix 0 OUT: OE of Pin5	60
[371:366]	Matrix 0 OUT: Digital Output of Pin6	61
[377:372]	Matrix 0 OUT: Digital Output of Pin7	62
[383:378]	Matrix 0 OUT: OE of Pin7	63
[389:384]	Matrix 0 OUT: Digital Output of Pin8	64
[395:390]	Matrix 0 OUT: Digital Output of Pin9	65
[401:396]	Matrix 0 OUT: OE of Pin9	66
[407:402]	Matrix 0 OUT: Digital Output of Pin10	67
[413:408]	Matrix 0 OUT: OE of Pin10	68
[419:414]	Matrix 0 OUT: PDB (Power-down) for ACMP0	69
[425:420]	Matrix 0 OUT: PDB (Power-down) for ACMP4	70
[431:426]	Matrix 0 OUT: PDB (Power-down) for ACMP5	71
[437:432]	Matrix 0 OUT: CNT0/CNT2/CNT9/ External Clock(CLK_Matrix0)	72
[443:438]	Matrix 0 OUT: CNT5/CNT6 External Clock (CLK_Matrix1)	73
[449:444]	Matrix 0 OUT: Input of DLY/CNT0	74
[455:450]	Matrix 0 OUT: Input of DLY/CNT2	75
[461:456]	Matrix 0 OUT: Keep of DLY/CNT2	76

Table 24: Matrix 0 Output Table (Continued)

Register Bit Address	Matrix 0 Output Signal Function	Matrix Output Number
[467:462]	Matrix 0 OUT: Up of DLY/CNT2	77
[473:468]	Matrix 0 OUT: Input of DLY/CNT5	78
[479:474]	Matrix 0 OUT: Input of DLY/CNT6	79
[485:480]	Matrix 0 OUT: Input of DLY/CNT9	80
[491:486]	Matrix 0 OUT: ADC Power-down	81
[497:492]	Matrix 0 OUT: CSB of SPI	82
[503:498]	Matrix 0 OUT: SCLK of SPI	83
[509:504]	Matrix 0 OUT: Oscillator Power-down	84
[515:510]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [0]	85
[521:516]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [1]	86
[527:522]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [2]	87
[533:528]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [3]	88
[539:534]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [4]	89
[545:540]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [5]	90
[551:546]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [6]	91
[557:552]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [7]	92
[563:558]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [8]	93
[569:564]	Matrix 0 OUT: Cross Connection Output to Matrix 1 [9]	94

6.3 MATRIX INPUT 1 TABLE

Table 25: Matrix 1 Input Table

N	Matrix 1 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GROUND	0	0	0	0	0	0
1	2-bit LUT4 Output	0	0	0	0	0	1
2	2-bit LUT5 Output	0	0	0	0	1	0
3	2-bit LUT6 Output	0	0	0	0	1	1
4	2-bit LUT7 Output	0	0	0	1	0	0
5	3-bit LUT8 Output	0	0	0	1	0	1
6	3-bit LUT9 Output	0	0	0	1	1	0
7	3-bit LUT10 Output	0	0	0	1	1	1
8	3-bit LUT11 Output	0	0	1	0	0	0
9	3-bit LUT12 Output	0	0	1	0	0	1
10	3-bit LUT13 Output	0	0	1	0	1	0
11	3-bit LUT14 Output	0	0	1	0	1	1
12	3-bit LUT15 Output	0	0	1	1	0	0
13	4-bit LUT1 Output	0	0	1	1	0	1
14	DFF6/LATCH6 Output	0	0	1	1	1	0
15	DFF7/LATCH7 Output	0	0	1	1	1	1
16	DFF8/LATCH8 Output	0	1	0	0	0	0
17	DFF9/LATCH9 Output	0	1	0	0	0	1
18	DFF10/LATCH10 Output	0	1	0	0	1	0
19	DFF11/LATCH11 Output	0	1	0	0	1	1
20	Pipe Delay 1 Out0	0	1	0	1	0	0
21	Pipe Delay 1 Out1	0	1	0	1	0	1
22	Edge Detect Programmable Delay 1 Output	0	1	0	1	1	0
23	Inverter 1 Output	0	1	0	1	1	1
24	Pin12 Digital Output	0	1	1	0	0	0
25	Pin13 Digital Output	0	1	1	0	0	1
26	Pin14 Digital Output	0	1	1	0	1	0
27	Pin15 Digital Output	0	1	1	0	1	1
28	Pin16 Digital Output	0	1	1	1	0	0
29	Pin17 Digital Output	0	1	1	1	0	1
30	Pin18 Digital Output	0	1	1	1	1	0
31	Pin19 Digital Output	0	1	1	1	1	1
32	Pin20 Digital Output	1	0	0	0	0	0
33	ACMP1 Output	1	0	0	0	0	1
34	ACMP2 Output	1	0	0	0	1	0
35	ACMP3 Output	1	0	0	0	1	1
36	DLY1/CNT1 Output	1	0	0	1	0	0
37	DLY3/CNT3 Output	1	0	0	1	0	1

Table 25: Matrix 1 Input Table (Continued)

N	Matrix 1 Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	DLY4/CNT4 Output	1	0	0	1	1	0
39	DLY7/CNT7 Output	1	0	0	1	1	1
40	DLY8/CNT8 Output	1	0	1	0	0	0
41	Sig_BG_OK	1	0	1	0	0	1
42	PWM0_DCMP0_Out_negative	1	0	1	0	1	0
43	PWM0_DCMP0_Out_positive	1	0	1	0	1	1
44	PWM1_DCMP1_Out_negative/SPI_Out[0]	1	0	1	1	0	0
45	PWM1_DCMP1_Out_positive/SPI_Out[1]	1	0	1	1	0	1
46	PWM2_DCMP2_Out_negative/SPI_Out[2]	1	0	1	1	1	0
47	PWM2_DCMP2_Out_positive/SPI_Out[3]	1	0	1	1	1	1
48	Ring Oscillator Output/SPI_Out[4]	1	1	0	0	0	0
49	RC Oscillator Output/SPI_Out[5]	1	1	0	0	0	1
50	Low Frequency Oscillator Output/SPI_Out[6]	1	1	0	0	1	0
51	GROUND/SPI_Out[7]	1	1	0	0	1	1
52	Cross Connection Input from Matrix 0 [0]	1	1	0	1	0	0
53	Cross Connection Input from Matrix 0 [1]	1	1	0	1	0	1
54	Cross Connection Input from Matrix 0 [2]	1	1	0	1	1	0
55	Cross Connection Input from Matrix 0 [3]	1	1	0	1	1	1
56	Cross Connection Input from Matrix 0 [4]	1	1	1	0	0	0
57	Cross Connection Input from Matrix 0 [5]	1	1	1	0	0	1
58	Cross Connection Input from Matrix 0 [6]	1	1	1	0	1	0
59	Cross Connection Input from Matrix 0 [7]	1	1	1	0	1	1
60	Cross Connection Input from Matrix 0 [8]	1	1	1	1	0	0
61	Cross Connection Input from Matrix 0 [9]	1	1	1	1	0	1
62	nRESET_Matrix	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.4 MATRIX 1 OUTPUT TABLE

Table 26: Matrix 1 Output Table

Register Bit Address	Matrix 1 Output Signal Function	Matrix Output Number
[1029:1024]	Matrix 1 OUT: In0 of 2-bit LUT4	0
[1035:1030]	Matrix 1 OUT: In1 of 2-bit LUT4	1
[1041:1036]	Matrix 1 OUT: In0 of 2-bit LUT5	2
[1047:1042]	Matrix 1 OUT: In1 of 2-bit LUT5	3
[1053:1048]	Matrix 1 OUT: In0 of 2-bit LUT6	4
[1059:1054]	Matrix 1 OUT: In1 of 2-bit LUT6	5
[1065:1060]	Matrix 1 OUT: In0 of 2-bit LUT7	6
[1071:1066]	Matrix 1 OUT: In1 of 2-bit LUT7	7
[1077:1072]	Matrix 1 OUT: In0 of 3-bit LUT8	8
[1083:1078]	Matrix 1 OUT: In1 of 3-bit LUT8	9
[1089:1084]	Matrix 1 OUT: In2 of 3-bit LUT8	10
[1095:1090]	Matrix 1 OUT: In0 of 3-bit LUT9	11
[1101:1096]	Matrix 1 OUT: In1 of 3-bit LUT9	12
[1107:1102]	Matrix 1 OUT: In2 of 3-bit LUT9	13
[1113:1108]	Matrix 1 OUT: In0 of 3-bit LUT10	14
[1119:1114]	Matrix 1 OUT: In1 of 3-bit LUT10	15
[1125:1120]	Matrix 1 OUT: In2 of 3-bit LUT10	16
[1131:1126]	Matrix 1 OUT: In0 of 3-bit LUT11	17
[1137:1132]	Matrix 1 OUT: In1 of 3-bit LUT11	18
[1143:1138]	Matrix 1 OUT: In2 of 3-bit LUT11	19
[1149:1144]	Matrix 1 OUT: In0 of 3-bit LUT12	20
[1155:1150]	Matrix 1 OUT: In1 of 3-bit LUT12	21
[1161:1156]	Matrix 1 OUT: In2 of 3-bit LUT12	22
[1167:1162]	Matrix 1 OUT: In0 of 3-bit LUT13	23
[1173:1168]	Matrix 1 OUT: In1 of 3-bit LUT13	24
[1179:1174]	Matrix 1 OUT: In2 of 3-bit LUT13	25
[1185:1180]	Matrix 1 OUT: In0 of 3-bit LUT14	26
[1191:1186]	Matrix 1 OUT: In1 of 3-bit LUT14	27
[1197:1192]	Matrix 1 OUT: In2 of 3-bit LUT14	28
[1203:1198]	Matrix 1 OUT: In0 of 3-bit LUT15	29
[1209:1204]	Matrix 1 OUT: In1 of 3-bit LUT15	30
[1215:1210]	Matrix 1 OUT: In2 of 3-bit LUT15	31
[1221:1216]	Matrix 1 OUT: In0 of 4-bit LUT1	32
[1227:1222]	Matrix 1 OUT: In1 of 4-bit LUT1	33
[1233:1228]	Matrix 1 OUT: In2 of 4-bit LUT1	34
[1239:1234]	Matrix 1 OUT: In3 of 4-bit LUT1	35
[1245:1240]	Matrix 1 OUT: nSET or nRST of DFF6/Latch6	36
[1251:1246]	Matrix 1 OUT: Data of DFF6/Latch6	37

Table 26: Matrix 1 Output Table (Continued)

Register Bit Address	Matrix 1 Output Signal Function	Matrix Output Number
[1257:1252]	Matrix 1 OUT: Clock of DFF6/Latch6	38
[1263:1258]	Matrix 1 OUT: nSET or nRST of DFF7/Latch7	39
[1269:1264]	Matrix 1 OUT: Data of DFF7/Latch7	40
[1275:1270]	Matrix 1 OUT: Clock of DFF7/Latch7	41
[1281:1276]	Matrix 1 OUT: nSET or nRST of DFF8/Latch8	42
[1287:1282]	Matrix 1 OUT: Data of DFF8/Latch8	43
[1293:1288]	Matrix 1 OUT: Clock of DFF8/Latch8	44
[1299:1294]	Matrix 1 OUT: Data of DFF9/Latch9	45
[1305:1300]	Matrix 1 OUT: Clock of DFF9/Latch9	46
[1311:1306]	Matrix 1 OUT: Data of DFF10/Latch10	47
[1317:1312]	Matrix 1 OUT: Clock of DFF10/Latch10	48
[1323:1318]	Matrix 1 OUT: Data of DFF11/Latch11	49
[1329:1324]	Matrix 1 OUT: Clock of DFF11/Latch11	50
[1335:1330]	Matrix 1 OUT: Clock of Pipe Delay 1	51
[1341:1336]	Matrix 1 OUT: Input Data of Pipe Delay 1	52
[1347:1342]	Matrix 1 OUT: Reset of Pipe Delay 1	53
[1353:1348]	Matrix 1 OUT: Input of Edge Detector and Programmable Delay 1	54
[1359:1354]	Matrix 1 OUT: Input of Inverter 1	55
[1365:1360]	Matrix 1 OUT: Digital Output of PIN 12	56
[1371:1366]	Matrix 1 OUT: Digital Output of PIN 13	57
[1377:1372]	Matrix 1 OUT: OE of PIN 13	58
[1383:1378]	Matrix 1 OUT: Digital Output of PIN 14	59
[1389:1384]	Matrix 1 OUT: OE of PIN 14	60
[1395:1390]	Matrix 1 OUT: Digital Output of PIN 15	61
[1401:1396]	Matrix 1 OUT: Digital Output of PIN 16	62
[1407:1402]	Matrix 1 OUT: OE of PIN 16	63
[1413:1408]	Matrix 1 OUT: Digital Output of PIN 17	64
[1419:1414]	Matrix 1 OUT: Digital Output of PIN 18	65
[1425:1420]	Matrix 1 OUT: OE of PIN 18	66
[1431:1426]	Matrix 1 OUT: Digital Output of PIN 19	67
[1437:1432]	Matrix 1 OUT: OE of PIN 19	68
[1443:1438]	Matrix 1 OUT: Digital Output of PIN 20	69
[1449:1444]	Matrix 1 OUT: PDB (Power-down) for ACMP1	70
[1455:1450]	Matrix 1 OUT: PDB (Power-down) for ACMP2	71
[1461:1456]	Matrix 1 OUT: PDB (Power-down) for ACMP3	72
[1467:1462]	Matrix 1 OUT: CNT7/CNT8/PWM/ADC External Clock (CLK_Matrix2)	73
[1473:1468]	Matrix 1 OUT: CNT1/CNT3/CNT4 External Clock (CLK_Matrix3)	74
[1479:1474]	Matrix 1 OUT: Input of DLY/CNT1	75
[1485:1480]	Matrix 1 OUT: Input of DLY/CNT3	76

Table 26: Matrix 1 Output Table (Continued)

Register Bit Address	Matrix 1 Output Signal Function	Matrix Output Number
[1491:1486]	Matrix 1 OUT: Input of DLY/CNT4	77
[1497:1492]	Matrix 1 OUT: Keep of DLY/CNT4	78
[1503:1498]	Matrix 1 OUT: Up of DLY/CNT4	79
[1509:1504]	Matrix 1 OUT: Input of DLY/CNT7	80
[1515:1510]	Matrix 1 OUT: Input of DLY/CNT8	81
[1521:1516]	Matrix 1 OUT: PWM Power-down	82
[1527:1522]	Matrix 1 OUT: PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 0	83
[1533:1528]	Matrix 1 OUT: PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 1	84
[1539:1534]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [0]	85
[1545:1540]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [1]	86
[1551:1546]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [2]	87
[1557:1552]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [3]	88
[1563:1558]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [4]	89
[1569:1564]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [5]	90
[1575:1570]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [6]	91
[1581:1576]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [7]	92
[1587:1582]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [8]	93
[1593:1588]	Matrix 1 OUT: Cross Connection Output to Matrix 0 [9]	94
[1599:1594]	Reserved	

7 8-bit SAR ADC Analog-to-Digital Converter

The Analog to Digital Converter (ADC) in the SLG46620-A is an 8-bit Successive Approximation Register Analog to Digital Converter (SAR ADC) which operates at a sampling speed of 100 kHz. The ADC's DNL < ± 0.5 LSB and INL < ± 3.4 LSB and has a ADC Vref accuracy of ± 50 mV. The ADC consists of two parts: PGA which provides signal amplification and conditioning and SAR ADC which handles analog to digital conversion. PGA can be used as amplifier when ADC is disabled. Please see section 7.3.2 PGA Output for more details. User controlled inputs and outputs of the ADC are listed below:

Inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input MUX Control Signal (PIN 16, V_{DD})
- IN+: Single-Ended Mode Input (PIN8 or PIN9) and Differential Mode Positive Input (PIN8)
- IN-: Differential Mode Negative Input (PIN 9 or DAC0)
- Vref: ADC Voltage Reference Input (ADC Vref, V_{DD}/4, none)
- CLK or CLK/16: ADC Clock Input (Ring OSC, Ext. CLK2 (Matrix1_OUT73), RC OSC, SPI SCLK)
- Wake/Sleep

Outputs:

- PGA_Out: Output of the PGA to PIN7
- PGA_Out: Output of the PGA to ACMP1
- SER DATA: ADC serial output (SPI)
- PAR DATA: 8-bit ADC parallel data to either the SPI, PWM, or DCMP
- INT_ OUT: ADC Interrupt Output (Matrix0_OUT43)

7.1 ADC FUNCTIONAL DIAGRAM

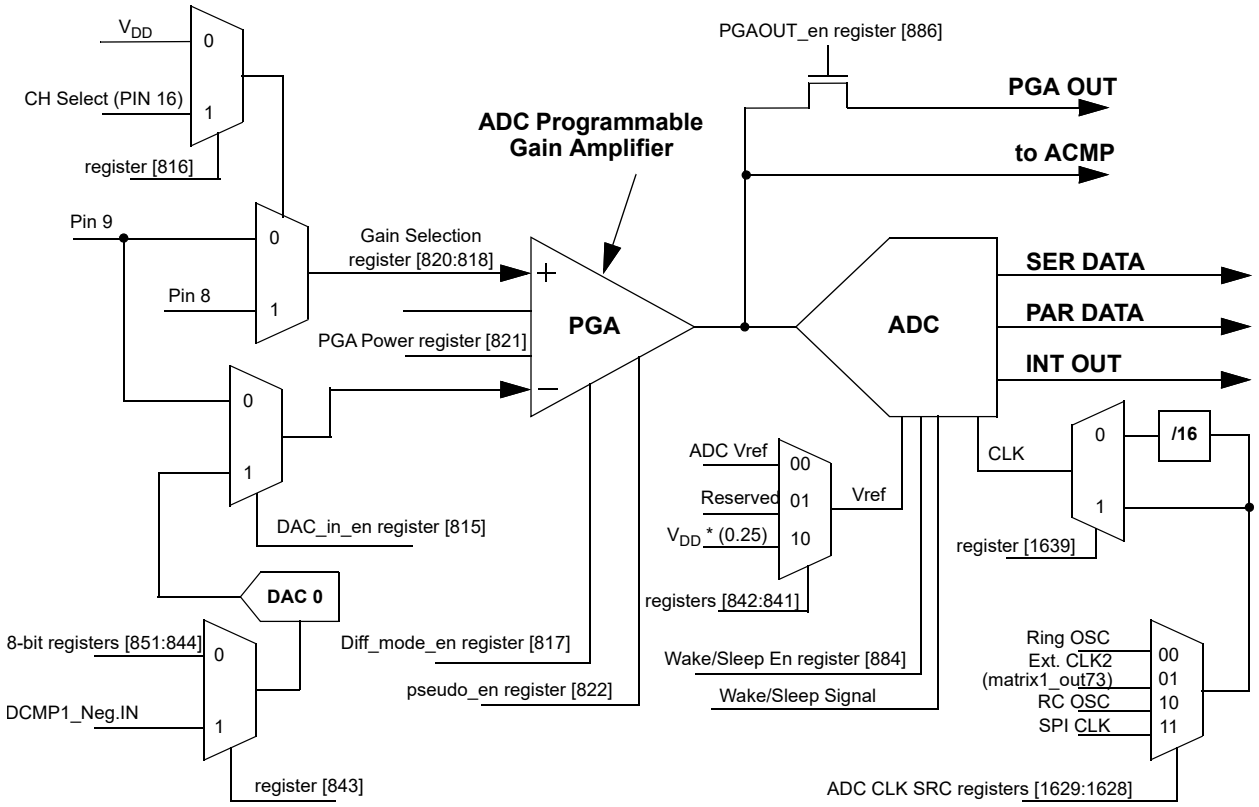


Figure 15: ADC Functional Diagram

7.2 ADC OPERATION MODES

The ADC has three operating modes:

- Single-Ended ADC operation using IN+ from PIN 8 or 9, when *ADC_sel* (register [817]) is “0”
- Differential ADC operation using IN+ from PIN 8 and IN- from PIN 9, when *ADC_sel* (register [817]) is “1”
- Pseudo-Differential ADC operation using IN+ from PIN 8 and IN- from PIN 9, when *ADC_sel* (register [817]) and *ADC_pseudodiff_en* (register [822]) bits are both set to “1”.

7.3 ADC 3-BIT PROGRAMMABLE GAIN AMPLIFIER

The front end of the ADC is a PGA with 3 bits for setting gain. The PGA buffers the ADC in all cases. The PGA gain is set by the ADC_gain_control (registers [820:818]). See ADC Register Settings Table.

Available gain settings depending on PGA mode selected (when used as ADC front-end):

- Single-ended: 0.5x, 1x, 2x, 4x, 8x
- Differential: 1x, 2x, 4x, 8x, 16x
- Pseudo-Differential: 1x, 2x

PGA inputs:

- CH SELECTOR: Single-Ended Mode ADC Selection and Analog Input MUX Control Signal (PIN16, V_{DD})
- IN+: Single-Ended Mode Input (PIN8 or PIN9) and Differential Mode Positive Input (PIN8)
- IN-: Differential Mode Negative Input (PIN9 or DAC0)

PGA output is connected directly to ADC input. Also, it is possible to connect PIN7 to PGA output (register [886]), when ADC is not in use only. The output of PGA has an offset when used as ADC front-end. Please see section 7.3.2 for more details.

7.3.1 PGA 2-Channel Selection

When *ADC_channel_sel* (register [816]) is set to “1”, the PGA of the ADC will sample either PIN 8 or PIN 9 on the IN+ input, where the selection is controlled by PIN 16.

- When PIN 16 is set to “0”, the ADC will sample PIN 9
- When PIN 16 is set to “1”, the ADC will sample PIN 8

When *ADC_channel_sel* (register [816]) is set to “0”, the PGA of the ADC will sample PIN 8 on the IN+ input.

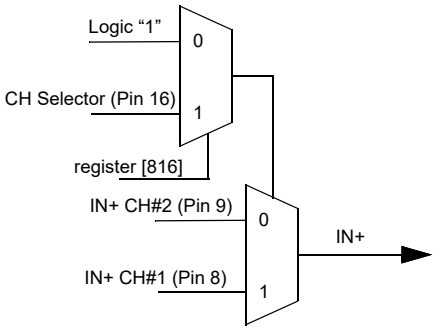


Figure 16: ADC 2-Channel Selection

7.3.2 PGA Output

PGA can be used either in standalone mode or as ADC font-end / ACMP input buffer.

In PGA standalone mode (ADC in POWER-DOWN mode) PGA output is always referenced to GND. When ADC is powered on, it powers also the PGA output reference macrocell, so that the output voltage is referenced to one of predefined output offset voltages Vos(RTO) which can be found in PGA specifications. This offset is required for correct ADC operation and it does not affect output code calculation.

PGA output reference (when ADC is on):

- Single-ended mode: Vos(RTO) = GND
- Differential mode: Vos(RTO) = 550 mV
- Pseudo-Differential mode: Vos(RTO) = 180 mV

Note that the reference voltage macrocell is controlled by ADC, therefore if ADC is in POWER-DOWN mode, the reference macrocell is OFF and PGA output is referenced to GND. In this case both Differential and Pseudo-Differential modes provide the same output. Typical PGA specifications in Differential/Pseudo-Differential mode with ADC in POWER-DOWN state are given in specifications section for information only.

Note 1: PGA operation in Differential/Pseudo-Differential mode with ADC in POWER-DOWN state is not recommended to use.
Note 2: Toggling ADC POWER-DOWN mode will also toggle the PGA output reference macrocell, that will influence the ACMP input voltage.

PGA has a few output connection possibilities: to ACMP1 and/or ADC, and to external output on PIN7. Connection to external output is possible only when ADC is powered down.

PGA output connection options:

- Single-Ended mode:
  - ADC
  - ACMP

- External output
- Differential mode:
  - ADC
  - ACMP **(Note 2)**
  - External output (Operation in this mode is not recommended)
- Pseudo-Differential mode:
  - ADC
  - ACMP **(Note 2)**
  - External output (Operation in this mode is not recommended)

7.3.3 PGA Power-On Signal

Whenever ADC is enabled, PGA is powered on automatically. However, it is possible to use PGA separately. In this case, Power-On function must be enabled, register [821] = 1.

Note 1 In ADC Wake/Sleep dynamic ON/OFF mode, must be set to 0

7.3.4 PGA Typical Performance

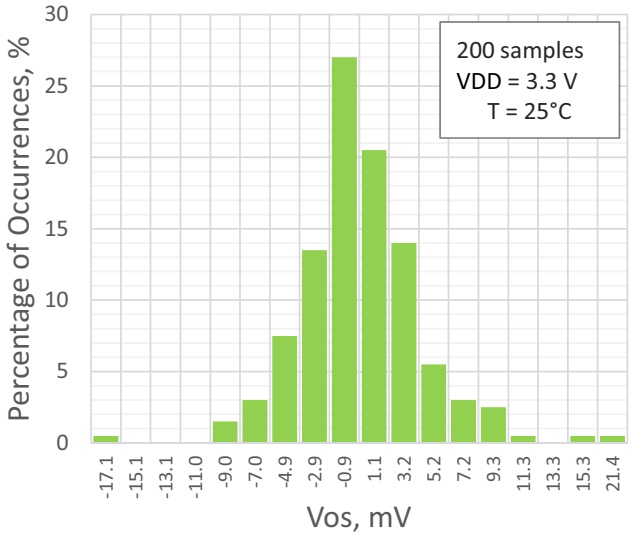


Figure 17: PGA Input Offset Distribution, Single-Ended Mode, G = 0.5

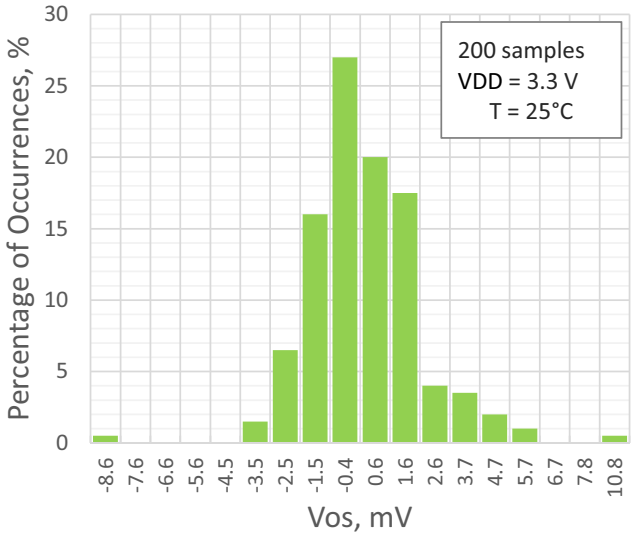


Figure 18: PGA Input Offset Distribution, Single-Ended Mode, G = 1

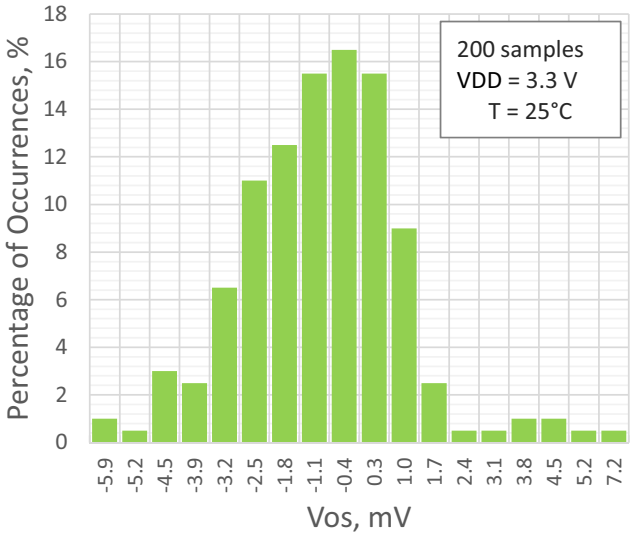


Figure 19: PGA Input Offset Distribution, Single-Ended Mode, G = 2

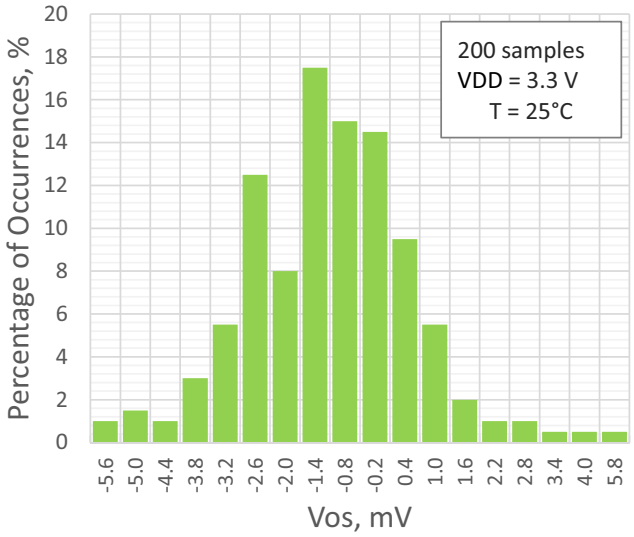


Figure 20: PGA Input Offset Distribution, Single-Ended Mode, G = 4

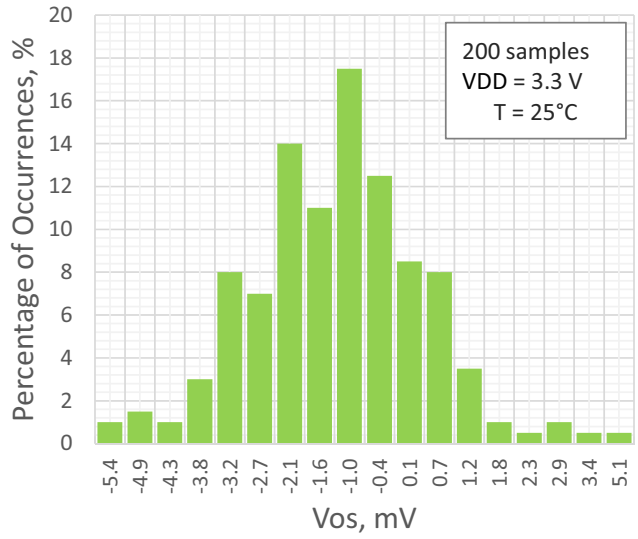


Figure 21: PGA Input Offset Distribution, Single-Ended Mode, G = 8

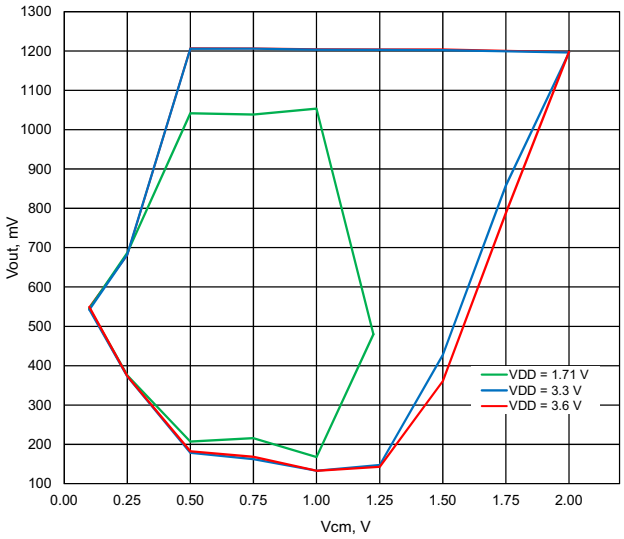


Figure 22: Typical Input Common Mode Voltage Range vs. Linear Output Voltage Range, Differential Mode, All Gains

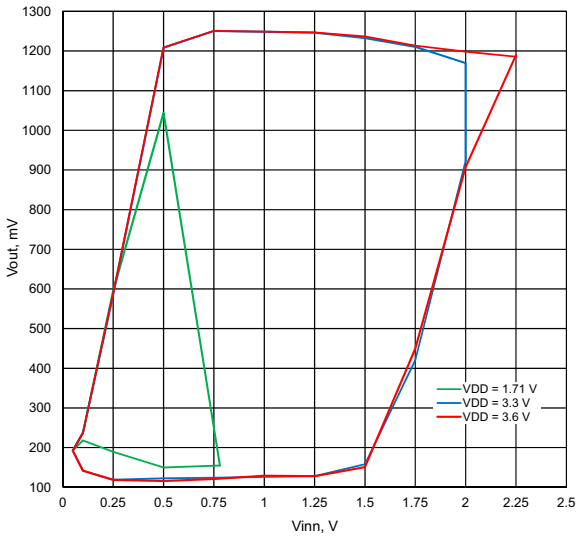


Figure 23: Typical Negative Input Voltage Range vs. Linear Output Voltage, Pseudo-Differential Mode, G = 1

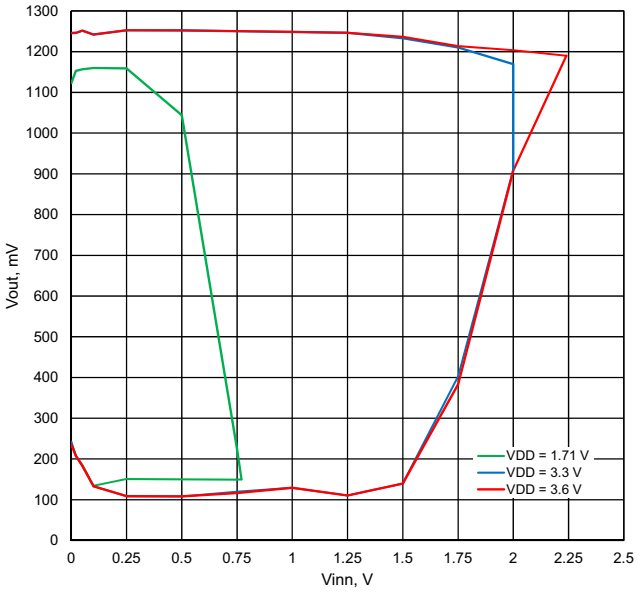


Figure 24: Typical Negative Input Voltage Range vs. Linear Output Voltage, Pseudo-Differential Mode, G = 2

7.4 ADC INPUT VOLTAGE DEFINITION

The ADC's input voltage (V_{IN_ADC}) is calculated based on either the single-ended or differential operation modes the logic cell is set to. In single-ended mode V_{IN_ADC} is the positive input voltage multiplied by the gain of the PGA. While in differential mode the V_{IN_ADC} is the difference between the positive and negative input voltages multiplied by the gain of the PGA plus one half of the reference voltage.

$$V_{OUT(PGA)} = V_{IN(ADC)} = G \cdot (V_{inp} + V_{os(RTI)}) \text{ - for SE mode}$$

$$V_{OUT(PGA)} = V_{IN(ADC)} = G \cdot V_{ind} + V_{os(RTO)} \text{ - for DI and PD mode}$$

V_{os} - PGA offset voltage. RTI and RTO denotes referred to input and referred to output V_{os}.

$$V_{os(RTI)} = \frac{V_{os(RTO)}}{G}$$

G - PGA nominal gain

V_{ind} - PGA input voltage (differential):

$$V_{ind} = V_{inp} - V_{inn}$$

$$V_{inp} = V_{cm} + \frac{V_{ind}}{2}$$

$$V_{inn} = V_{cm} - \frac{V_{ind}}{2}$$

V_{inn} and V_{inp} - absolute voltage at negative and positive PGA input correspondingly

V_{cm} - common mode PGA voltage:

$$V_{cm} = \frac{V_{inn} + V_{inp}}{2}$$

Note: In Pseudo-Differential mode V_{cm} is replaced by V_{inn} voltage for convenience

ADC code for PGA differential input voltage V_{ind} can be calculated as follows:

- Single-ended mode:

$$V_{ind} = V_{inp}$$

$$ADC_{code} = \frac{255}{V_{inp[max]} - V_{inp[min]}} (V_{inp} - V_{inp[min]})$$

Vinp[min] and Vinp[max] - positive input voltage for bit0 and bit255 correspondingly (can be found in ADC specifications)

- Differential and Pseudo-Differential mode:

$$ADC_{code} = \frac{255}{V_{ind[max]} - V_{ind[min]}} (Vind - Vind[min])$$

$V_{ind[min]}$ and $V_{ind[max]}$ - differential input voltage for bit0 and bit255 correspondingly (can be found in ADC specifications)

Least significant bit size (LSB) calculates as follows:

$$LSB = \frac{FS}{255}$$

where FS is full-scale range:

$$FS = V_{ind[max]} - V_{ind[min]}$$

7.5 ADC REFERENCE VOLTAGE

The ADC's reference voltage (Vref) is controlled by ADC_Vref_sel (registers [842:841]). The two reference voltage inputs are chosen from the following:

- ADC Vref from Internal Source (ADC Vref = 1.2 V)
- Power Divider of (0.25) * V_{DD}

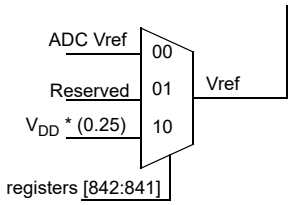


Figure 25: ADC Reference Voltage

7.6 ADC POWER-DOWN SELECT MODE

The ADC's power-down source is selected by Matrix0_Out81 registers [491:486]. A value of "1" will drive the ADC and the PGA to power-down mode. The SLG46620-A also has a slow/fast power-on mode feature controlled by register [885]. When register [885] = 0, the ADC is in slow power-on mode and the entire analog macrocell is controlled by *connection matrix output0 81*. When register [885] = 1, ADC is in fast power-on mode, where only the ADC will be controlled by *connection matrix output0 81* and the analog macrocell will remain on. With this feature, the first ADC power-on (with the rest of the analog macrocell) will be approximately 500 µs; the next power cycle the ADC power-on (ADC only) time is < 5 µs.

7.7 ADC CLOCK SOURCE

The ADC clock source comes from either the internal RC Oscillator, Matrix1_Out73, Ring Oscillator, or SPI CLK. The ADC requires 16 clock cycles to sample the analog voltage and output the sampled data.

Note: Sampling rate should not exceed approximately 100 kbps.

The selection is made from the *ADC_clk_sel* signal via registers [1629:1628] where:

- 00: Ring Oscillator
- 01: Matrix1_Out 73
- 10: RC Oscillator
- 11: SPI CLK

Note: It is not recommended to design in high frequency signals (input our output) on pins adjacent to the following pins: Pin7, Pin8, Pin9 as this may affect ADC performance.

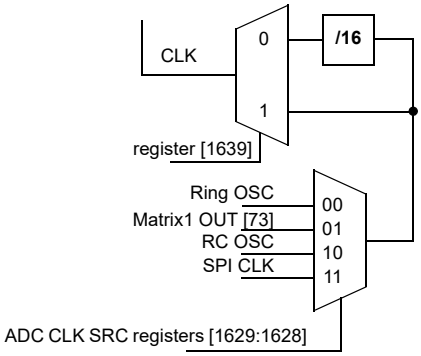


Figure 26: ADC Clock Source

7.8 ADC OUTPUTS

The ADC's output can be shifted out through the SPI logic cell. Both SER DATA and PAR DATA produce an 8-bit data string over 16 clock cycles. See Figure 27.

7.8.1 ADC Serial Output

The 8-bit serial data can be output from the SLG46620-A device on PIN 10. The individual 8 serial data bits can be read into an external device within the larger system design.

To initialize the *SER DATA* the ADC needs a Power-down signal, which can be configured through the connection matrix. After 6 ADC_CLK cycles the ADC will start to output the 8-Bit Serial Data. This PD signal needs to be held for at least 16 ADC_CLK cycles. The ADC_CLK is determined by either the RC OSC, RingOSC OSC, Matrix1_Out73, or SPI CLK.OSC

7.8.2 ADC Parallel Output

The 16-bit parallel data can be output from the ADC logic cell to either the DCMP/PWM or FSM logic cells within the SLG46620-A device.

To initialize the *PAR DATA* the ADC needs a Power-down signal, which can be configured through the connection matrix. After ten ADC_CLK cycles the ADC will start to output the 16-Bit Parallel Data. This PD signal needs to be held for at least 32 ADC_CLK cycles. The ADC_CLK is determined by either the RC OSC, Ring OSC, Matrix1_Out73, or SPI CLK.

7.9 ADC INTERRUPT OUTPUT TIMING DIAGRAM

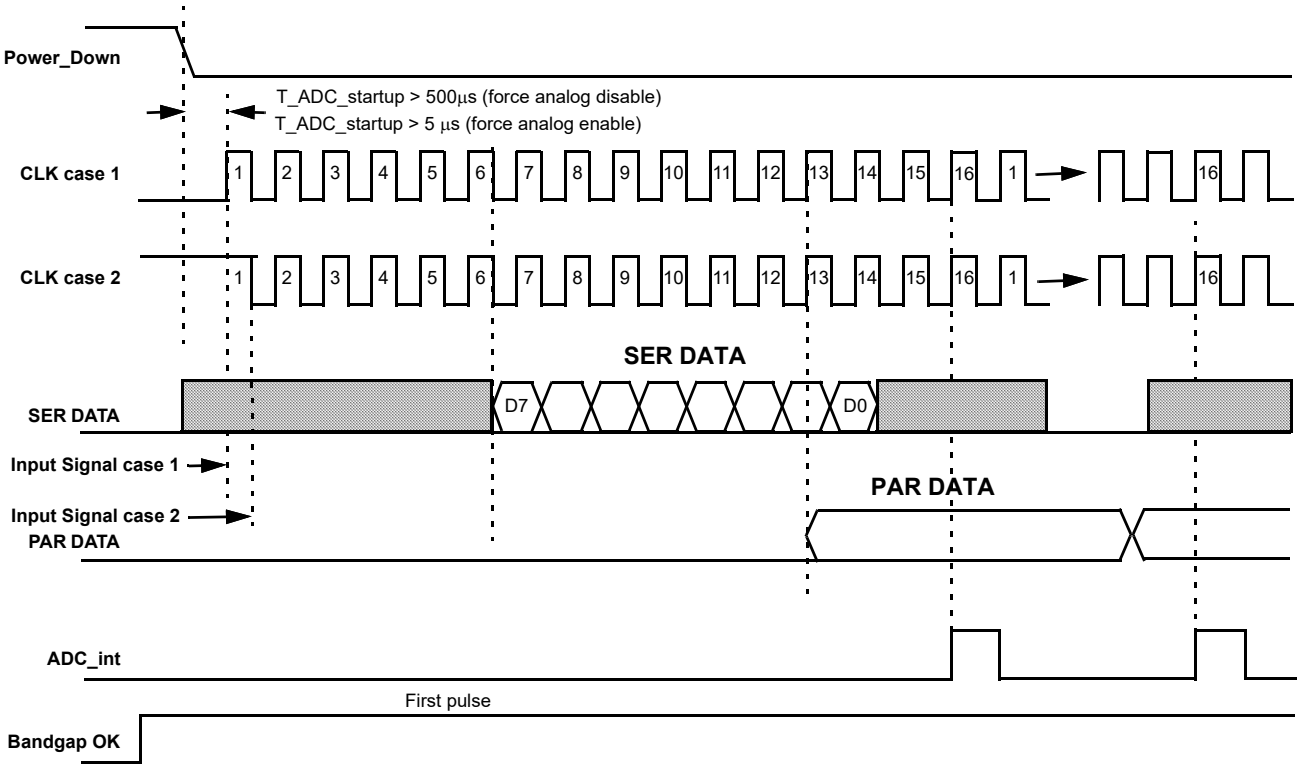


Figure 27: ADC Interrupt Output Timing Diagram

8 8-bit Digital-to-Analog Converter

There are two Digital-to-Analog Converters (DACs) in the SLG46620-A (DAC0 and DAC1), they are 8-bit Digital to Analog Converters which operate at a maximum sampling speed of 100 kbps. The DAC's DNL is less than 1 LSB and INL is less than 1LSB. DAC output to PIN resistance is 1 kΩ. Load resistance is recommended to be no less than 10 kΩ; load capacitance is recommended to be no more than 100 pF.

User controlled inputs and outputs of the DAC are listed below:

DAC0 Inputs:

- Registers
- CNT9_Q[7:0]
- 8LSBs SPI
- FSM0[7:0]

DAC0 Outputs:

- PIN19
- PGA negative input (00: 0 V; FF: 1 V)
- ACMP0 negative input
- ACMP1 negative input
- ACMP2 negative input
- ACMP3 negative input
- ACMP4 negative input
- ACMP5 negative input

DAC1 Inputs:

- Registers
- CNT9_Q[7:0]
- 8LSBs SPI
- FSM0[7:0]

DAC1 Outputs:

- PIN18
- ACMP0 negative input
- ACMP1 negative input
- ACMP2 negative input
- ACMP3 negative input
- ACMP4 negative input
- ACMP5 negative input

If a DAC output is connected to one of SLG46620-A's external pins (Pin19 for DAC0 and Pin18 for DAC1), it is necessary to enable those external pins as analog input/output. Register [840]: 0 - DAC0 power-off, 1 - DAC0 power-on. Register [834]: 0 - DAC1 power-off, 1 - DAC1 power-on.

DAC0 output range: 0 V…1 V
DAC1 output range: 50 mV…1.05 V

Please note that DAC1 is shared with ADC macrocell. Therefore it is impossible to use DAC1, when ADC is used. Also to activate DAC1, DAC0 must be enabled (register [840] = 1 and register [834] = 1). In addition, DAC0 is used as a part of pseudo-differential mode of PGA macrocell. Therefore DAC0 is not available when PGA is in pseudo-differential mode.

8.1 DAC0 FUNCTIONAL DIAGRAM

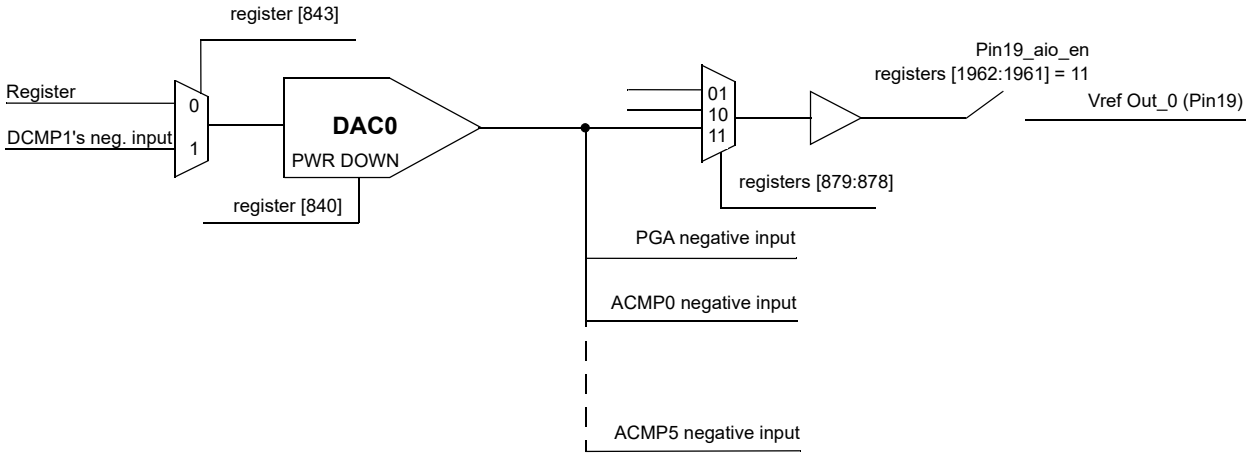


Figure 28: DAC0 Functional Diagram

8.2 DAC1 FUNCTIONAL DIAGRAM

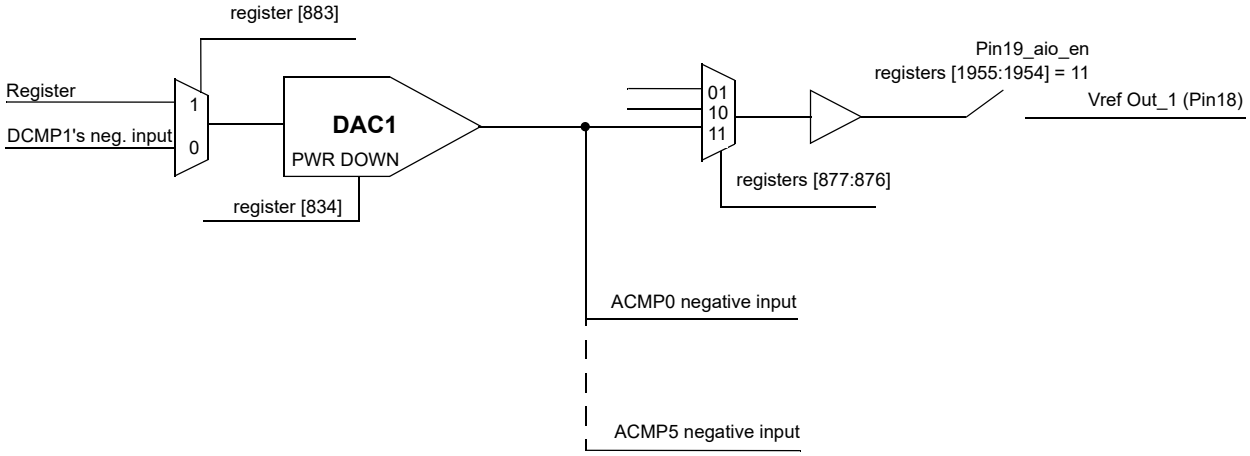


Figure 29: DAC1 Functional Diagram

8.3 DAC TYPICAL PERFORMANCE

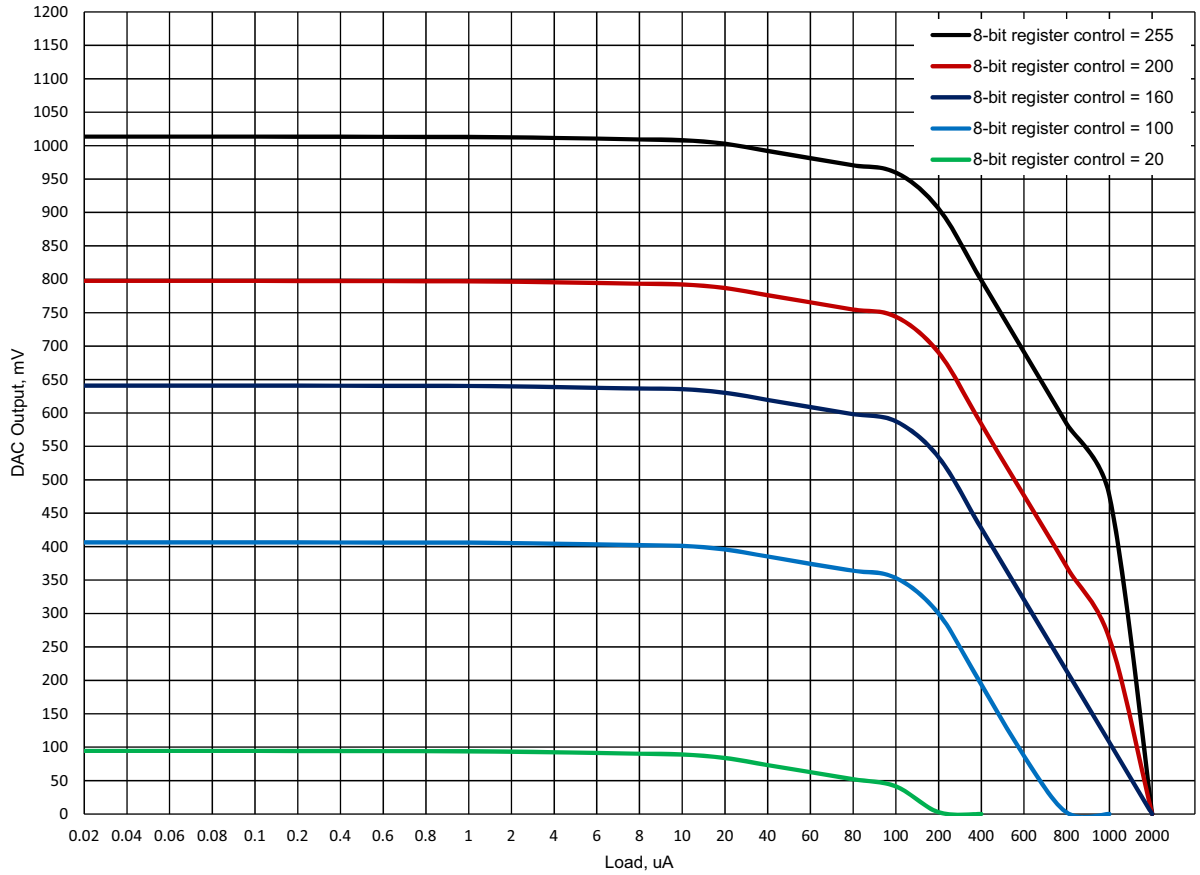


Figure 30: DAC Typical Load Regulation, T_A = 25 °C, V_{DD} = 3.3 V

9 Combinatorial Logic

Combinatorial logic is supported via twenty five Lookup Tables (LUTs) within the SLG46620-A. There are eight 2-bit LUTs, sixteen 3-bit LUTs, and one 4-bit LUT. The device also includes one Combination Function Macrocell that can be used as a 4-bit LUT. For more details, please see section 10.

Inputs/Outputs for the twenty five LUTs are configured from one of the connection matrices with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-BIT LUT

The eight 2-bit LUTs each take in two input signals from one of the two connection matrices and produce a single output, which goes back into the same connection matrix that the inputs came from. The output state of each 2-bit LUT is defined by four register bits, the output state is based on the appropriate bit selected by the value of the two inputs to the LUT.

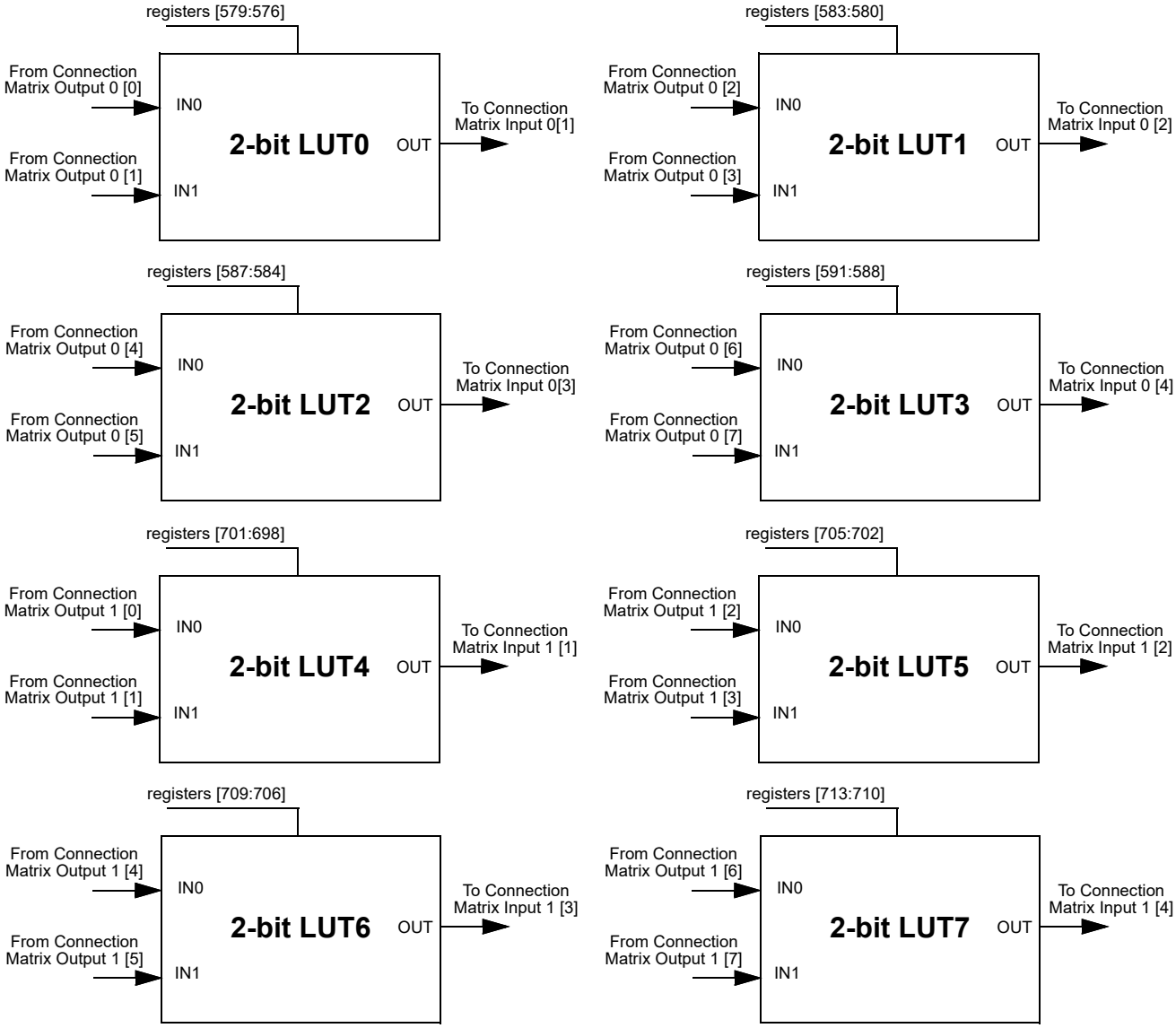


Figure 31: 2-bit LUTs

Table 27: 2-bit LUT0 Truth Table

IN1	IN0	OUT
0	0	register [576]
0	1	register [577]
1	0	register [578]
1	1	register [579]

Table 28: 2-bit LUT1 Truth Table

IN1	IN0	OUT
0	0	register [580]
0	1	register [581]
1	0	register [582]
1	1	register [583]

Table 29: 2-bit LUT2 Truth Table

IN1	IN0	OUT
0	0	register [584]
0	1	register [585]
1	0	register [586]
1	1	register [587]

Table 30: 2-bit LUT3 Truth Table

IN1	IN0	OUT
0	0	register [588]
0	1	register [589]
1	0	register [590]
1	1	register [591]

Table 31: 2-bit LUT4 Truth Table

IN1	IN0	OUT
0	0	register [698]
0	1	register [699]
1	0	register [700]
1	1	register [701]

Table 32: 2-bit LUT5 Truth Table

IN1	IN0	OUT
0	0	register [702]
0	1	register [703]
1	0	register [704]
1	1	register [705]

Table 33: 2-bit LUT6 Truth Table

IN1	IN0	OUT
0	0	register [706]
0	1	register [707]
1	0	register [708]
1	1	register [709]

Table 34: 2-bit LUT7 Truth Table

IN1	IN0	OUT
0	0	register [710]
0	1	register [711]
1	0	register [712]
1	1	register [713]

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [579:576]

2-Bit LUT1 is defined by registers [583:580]

2-Bit LUT2 is defined by registers [587:584]

2-Bit LUT3 is defined by registers [591:588]

2-Bit LUT4 is defined by registers [701:698]

2-Bit LUT5 is defined by registers [705:702]

2-Bit LUT6 is defined by registers [709:706]

2-Bit LUT7 is defined by registers [713:710]

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 35: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-BIT LUT

The sixteen 3-bit LUTs each take in three input signals from one of the two connection matrices and produce a single output, which goes back into the same connection matrix that the inputs came from. The output state of each 3-bit LUT is defined by eight register bits, the output state is based on the appropriate bit selected by the value of the three inputs to the LUT.

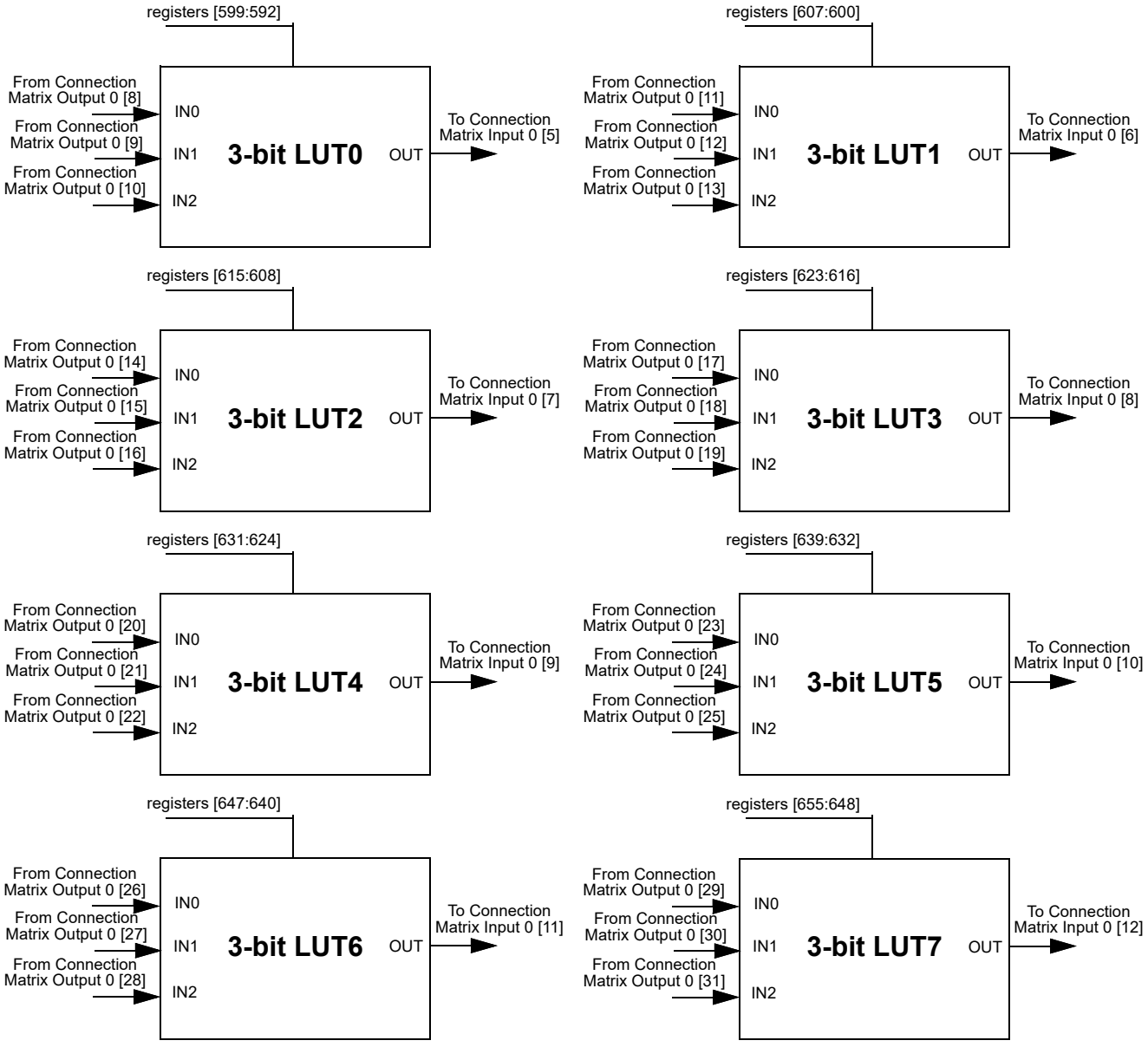


Figure 32: 3-bit LUTs

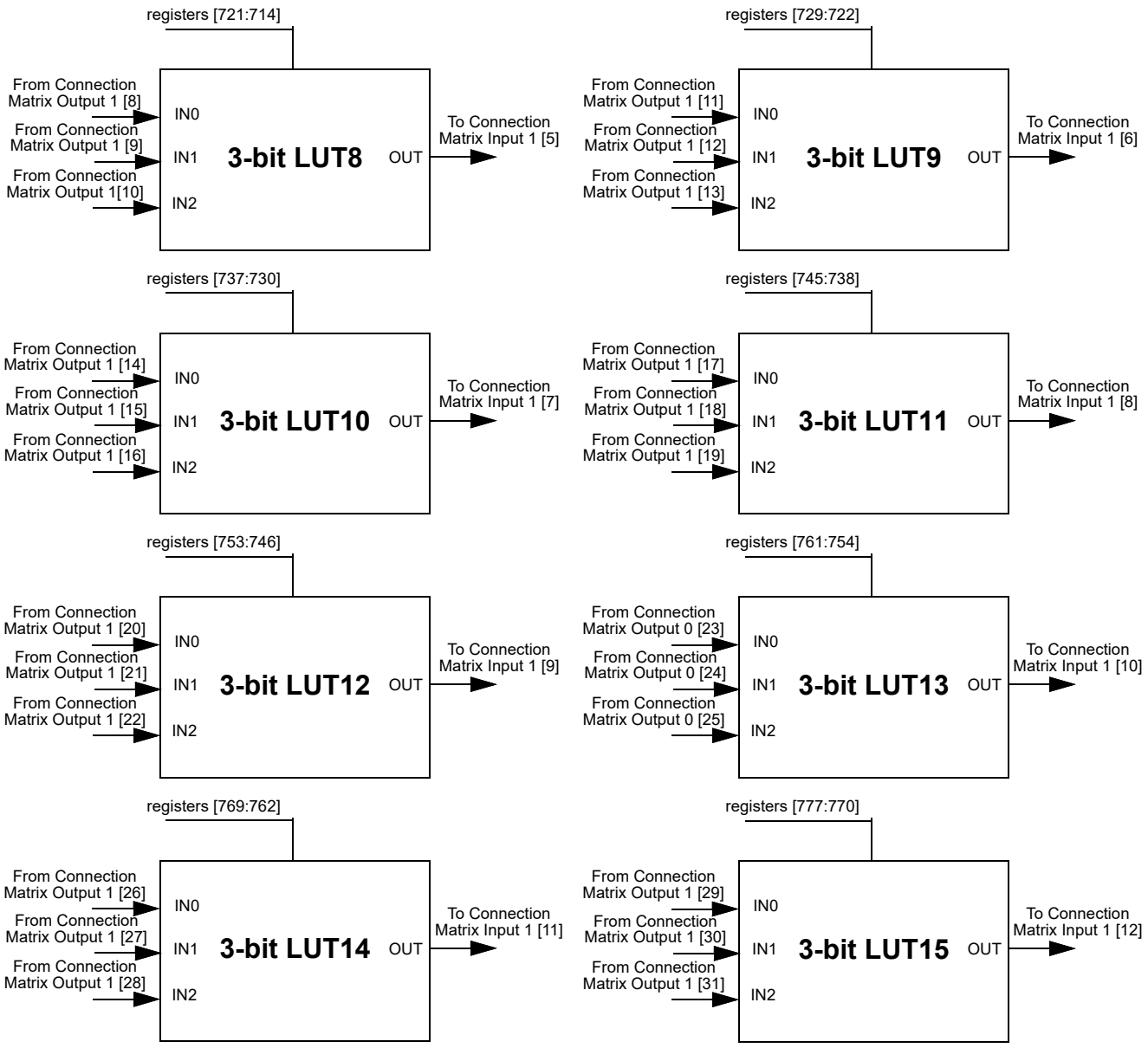


Figure 33: 3-bit LUTs

Table 36: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [592]
0	0	1	register [593]
0	1	0	register [594]
0	1	1	register [595]
1	0	0	register [596]
1	0	1	register [597]
1	1	0	register [598]
1	1	1	register [599]

Table 37: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [600]
0	0	1	register [601]
0	1	0	register [602]
0	1	1	register [603]
1	0	0	register [604]
1	0	1	register [605]
1	1	0	register [606]
1	1	1	register [607]

Table 38: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [608]
0	0	1	register [609]
0	1	0	register [610]
0	1	1	register [611]
1	0	0	register [612]
1	0	1	register [613]
1	1	0	register [614]
1	1	1	register [615]

Table 39: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [616]
0	0	1	register [617]
0	1	0	register [618]
0	1	1	register [619]
1	0	0	register [620]
1	0	1	register [621]
1	1	0	register [622]
1	1	1	register [623]

Table 40: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [624]
0	0	1	register [625]
0	1	0	register [626]
0	1	1	register [627]
1	0	0	register [628]
1	0	1	register [629]
1	1	0	register [630]
1	1	1	register [631]

Table 41: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [632]
0	0	1	register [633]
0	1	0	register [634]
0	1	1	register [635]
1	0	0	register [636]
1	0	1	register [637]
1	1	0	register [638]
1	1	1	register [639]

Table 42: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [640]
0	0	1	register [641]
0	1	0	register [642]
0	1	1	register [643]
1	0	0	register [644]
1	0	1	register [645]
1	1	0	register [646]
1	1	1	register [647]

Table 43: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [648]
0	0	1	register [649]
0	1	0	register [650]
0	1	1	register [651]
1	0	0	register [652]
1	0	1	register [653]
1	1	0	register [654]
1	1	1	register [655]

Table 44: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <714>
0	0	1	register [715]
0	1	0	register [716]
0	1	1	register [717]
1	0	0	register [718]
1	0	1	register [719]
1	1	0	register [720]
1	1	1	register [721]

Table 45: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [722]
0	0	1	register [723]
0	1	0	register [724]
0	1	1	register [725]
1	0	0	register [726]
1	0	1	register [727]
1	1	0	register [728]
1	1	1	register [729]

Table 46: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [730]
0	0	1	register [731]
0	1	0	register [732]
0	1	1	register [733]
1	0	0	register [734]
1	0	1	register [735]
1	1	0	register [736]
1	1	1	register [737]

Table 47: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [738]
0	0	1	register [739]
0	1	0	register [740]
0	1	1	register [741]
1	0	0	register [742]
1	0	1	register [743]
1	1	0	register [744]
1	1	1	register [745]

Table 48: 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [746]
0	0	1	register [747]
0	1	0	register [748]
0	1	1	register [749]
1	0	0	register [750]
1	0	1	register [751]
1	1	0	register [752]
1	1	1	register [753]

Table 49: 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [754]
0	0	1	register [755]
0	1	0	register [756]
0	1	1	register [757]
1	0	0	register [758]
1	0	1	register [759]
1	1	0	register [760]
1	1	1	register [761]

Table 50: 3-bit LUT14 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [762]
0	0	1	register [763]
0	1	0	register [764]
0	1	1	register [765]
1	0	0	register [766]
1	0	1	register [767]
1	1	0	register [768]
1	1	1	register [769]

Table 51: 3-bit LUT15 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [770]
0	0	1	register [771]
0	1	0	register [772]
0	1	1	register [773]
1	0	0	register [774]
1	0	1	register [775]
1	1	0	register [776]
1	1	1	register [777]

Each 3-bit LUT uses an 8-bit register signal to define their output functions:

3-Bit LUT0 is defined by registers [599:592]

3-Bit LUT1 is defined by registers [607:600]

3-Bit LUT2 is defined by registers [615:608]

3-Bit LUT3 is defined by registers [623:616]

3-Bit LUT4 is defined by registers [631:624]

3-Bit LUT5 is defined by registers [639:632]

3-Bit LUT6 is defined by registers [647:640]

3-Bit LUT7 is defined by registers [655 648]

3-Bit LUT8 is defined by registers [721:714]

3-Bit LUT9 is defined by registers [729:722]

3-Bit LUT10 is defined by registers [737:730]

3-Bit LUT11 is defined by registers [745:738]

3-Bit LUT12 is defined by registers [753:746]

3-Bit LUT13 is defined by registers [761:754]

3-Bit LUT14 is defined by registers [769:762]

3-Bit LUT15 is defined by registers [777:770]

The Table 52 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 3-bit LUT logic cells.

Table 52: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

9.3 4-BIT LUT

The one 4-bit LUT (4-bit LUT1) takes in four input signals from connection matrix 1 and produces a single output, which goes back into connection matrix 1. The output state of the 4-bit LUT is defined by sixteen register bits, the output state is based on the appropriate bit selected by the value of the four inputs to the LUT.

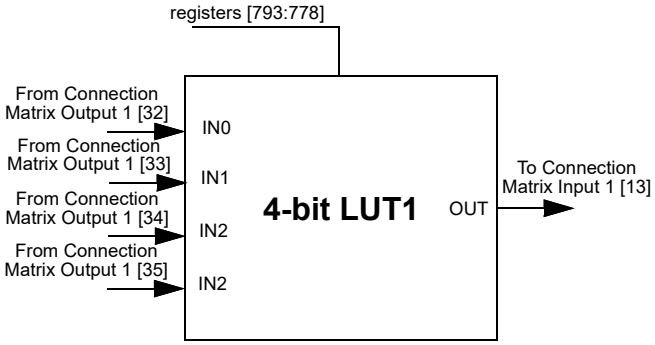


Figure 34: 4-bit LUT1

The device also includes one Combination Function Macrocell that can be used as a 4-bit LUT. For more details, please see section 10.

Table 53: 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	register [778]
0	0	0	1	register [779]
0	0	1	0	register [780]
0	0	1	1	register [781]
0	1	0	0	register [782]
0	1	0	1	register [783]
0	1	1	0	register [784]
0	1	1	1	register [785]
1	0	0	0	register [786]
1	0	0	1	register [787]
1	0	1	0	register [788]
1	0	1	1	register [789]
1	1	0	0	register [790]
1	1	0	1	register [791]
1	1	1	0	register [792]
1	1	1	1	register [793]

Each 4-bit LUT uses an 16-bit register signal to define their output functions:

4-Bit LUT1 is defined by registers [793:778]

The Table 54 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

Table 54: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

10 Combination Function Macrocells

The SLG46620-A has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Function Generator (PGEN).

When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix 0 and produce a single output, which goes back into the connection matrix 0. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Function Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats. See Figure 36.

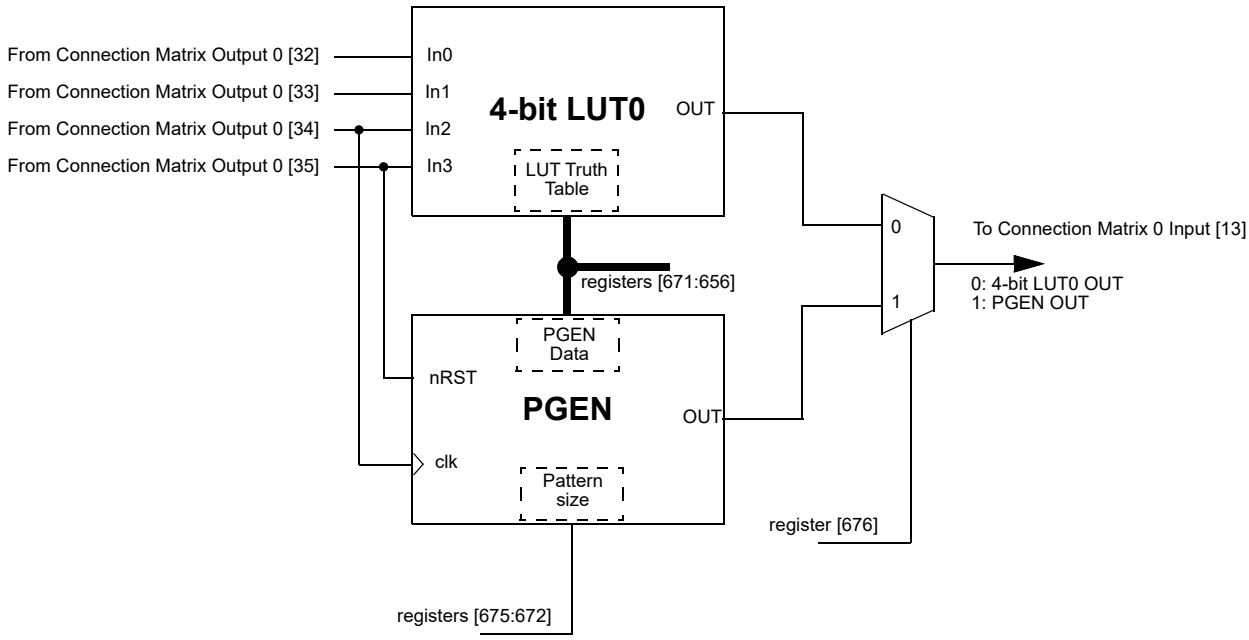


Figure 35: 4-bit LUT0 or PGEN

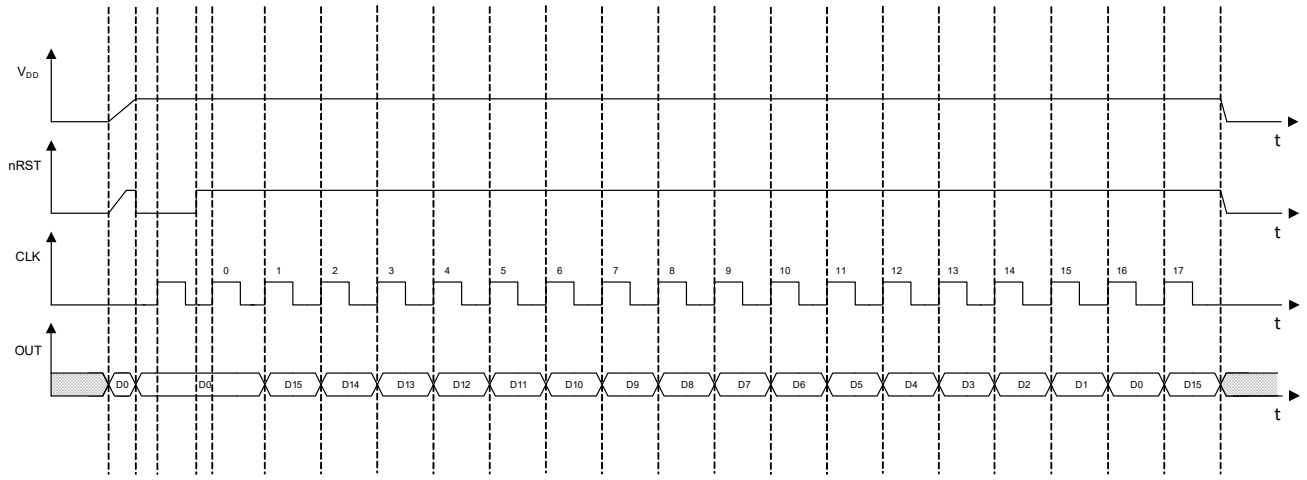


Figure 36: PGEN Timing Diagram

When this macrocell is used to implement LUT function, the 4-bit LUT uses a 16-bit register signal to define its output function:

4-Bit LUT0 is defined by registers [671:656]

Table 55: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT
0	0	0	0	register [656]
0	0	0	1	register [657]
0	0	1	0	register [658]
0	0	1	1	register [659]
0	1	0	0	register [660]
0	1	0	1	register [661]
0	1	1	0	register [662]
0	1	1	1	register [663]
1	0	0	0	register [664]
1	0	0	1	register [665]
1	0	1	0	register [666]
1	0	1	1	register [667]
1	1	0	0	register [668]
1	1	0	1	register [669]
1	1	1	0	register [670]
1	1	1	1	register [671]

11 Analog Comparators

There are six Analog Comparator (ACMP) macrocells in the SLG46620-A. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

PWR UP = 1 → ACMP is powered up.

PWR UP = 0 → ACMP is powered down.

During ACMP power up, its output will remain low, and then becomes valid 2.08 ms (max) after ACMP power up signal goes high, see Figure 37. If V_{DD} is greater or equal to 2.7 V, it is possible to decrease turn-on time by setting the BG ok delay to 100 µs, see Figure 38. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the V_{DD} signal.

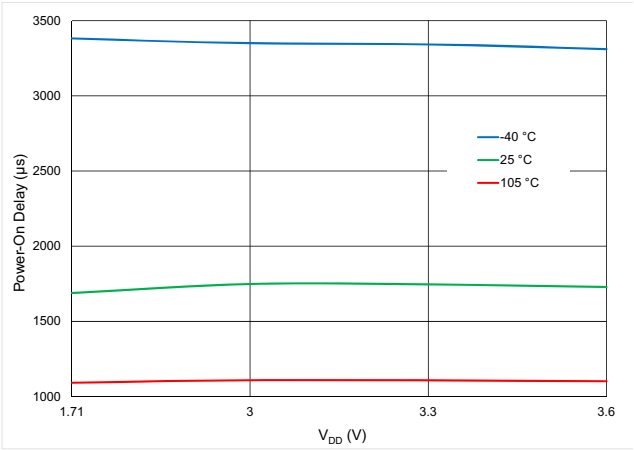


Figure 37: Maximum Power-On Delay vs. V_{DD}, BG = 550 µs, Regulator and Charge Pump set to automatic ON/OFF

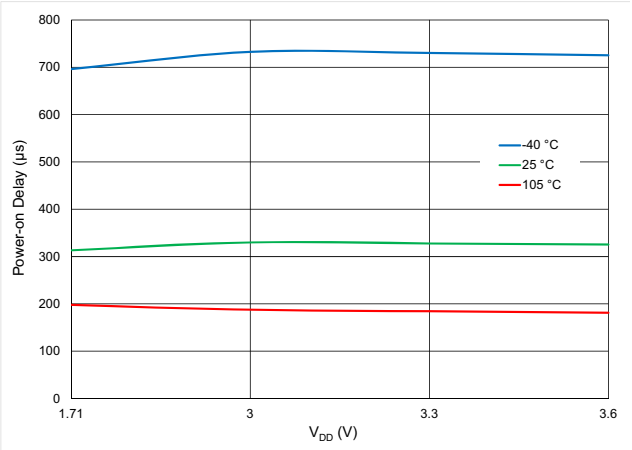


Figure 38: Maximum Power-On Delay vs. V_{DD}, BG = 100 µs, Regulator and Charge Pump set to automatic ON/OFF

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 kΩ (typ.) resistors, see Table 56. For gain divider accuracy refer to Table 57. IN- voltage range: 0 - 1.2 V. Can use Vref selection V_{DD}/4 and V_{DD}/3 to maintain this input range.

Input bias current < 1 nA (typ).

Table 56: Gain Divider Input Resistance (typical)

Gain	x1	x0.5	x0.33	x0.25
Input Resistance	100 GΩ	1 MΩ	0.75 MΩ	1 MΩ

Table 57: Gain Divider typical Accuracy at T_A = -40 °C to 105 °C, V_{DD} = 3.3 V

Gain	x0.5	x0.33	x0.25
Accuracy	±0.50 %	±0.33 %	±0.25 %

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external

voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within threshold window (between Vref and Vref - hysteresis). Please note: for the 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref – hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the Bandgap internal circuit as well. An analog voltage will appear on Vref even when the Force Bandgap option is set as Disabled.

For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer (except ACMP5). However, this will add an offset.

Note 1 When V_{DD} ≤ 2.0 V voltage reference should not exceed 1000 mV.
Note 2 For electrical specification refer to section 3.7.

11.1 ACMP MASTER ARCHITECTURE

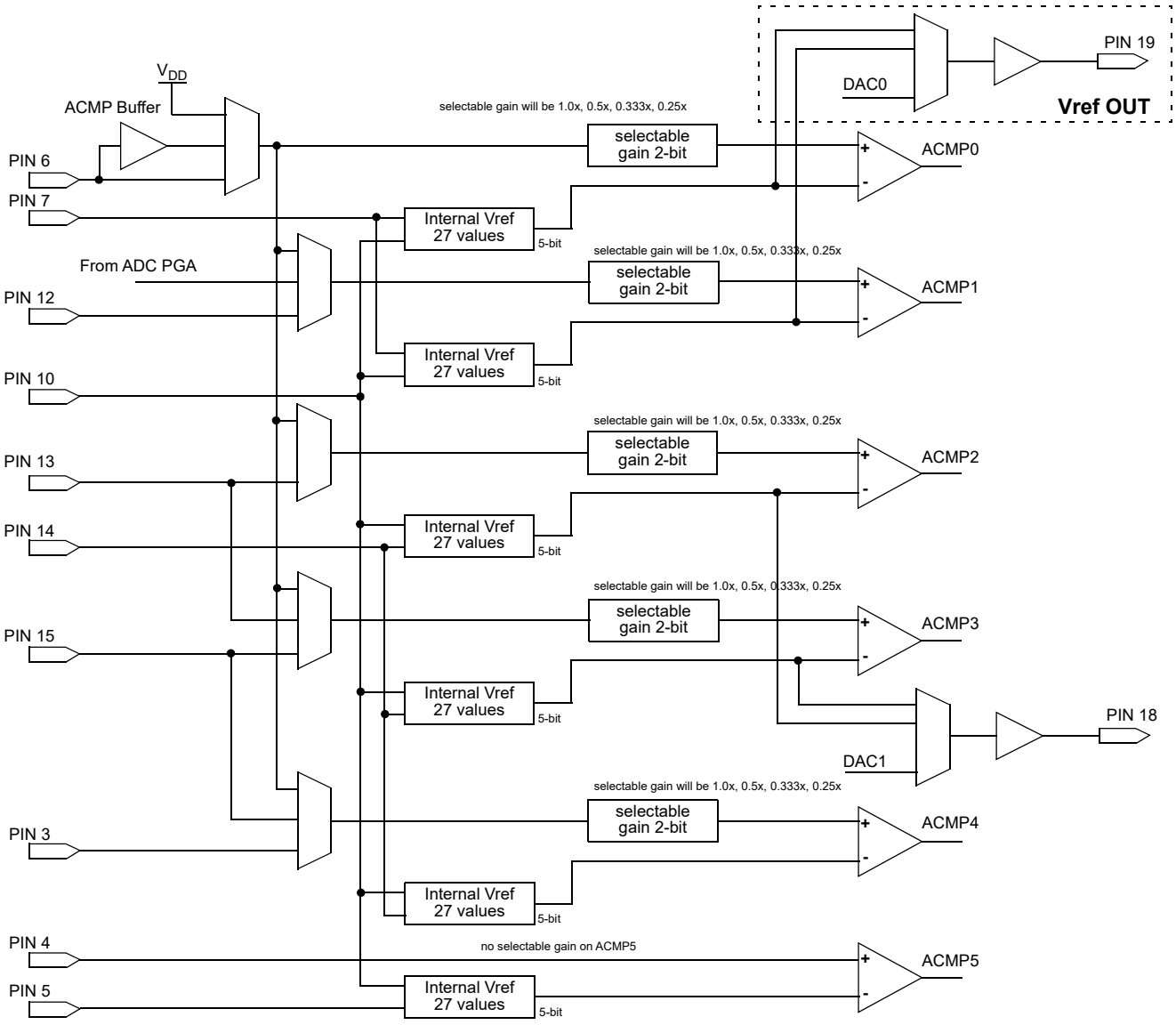


Figure 39: ACMP Master Architecture Diagram

11.2 ACMP0 BLOCK DIAGRAM

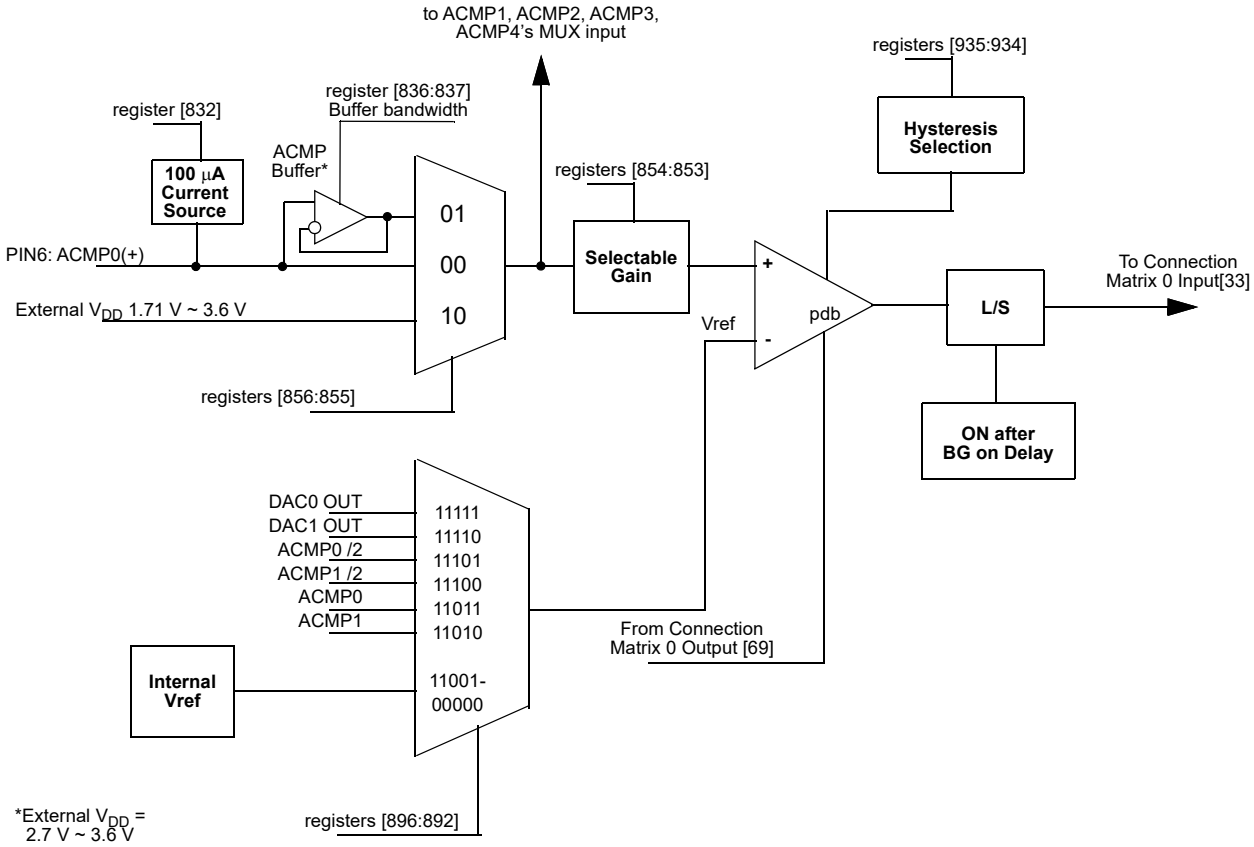


Figure 40: ACMP0 Block Diagram

11.3 ACMP1 BLOCK DIAGRAM

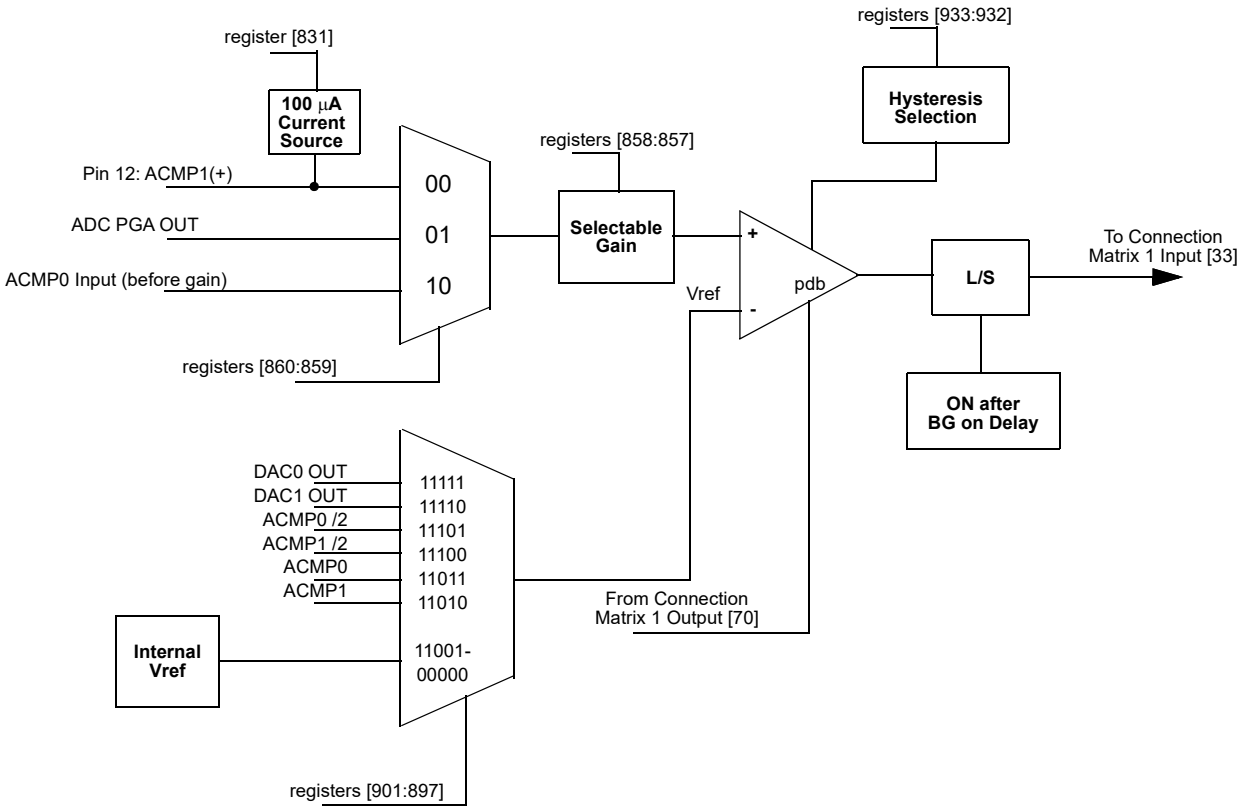


Figure 41: ACMP1 Block Diagram

11.4 ACMP2 BLOCK DIAGRAM

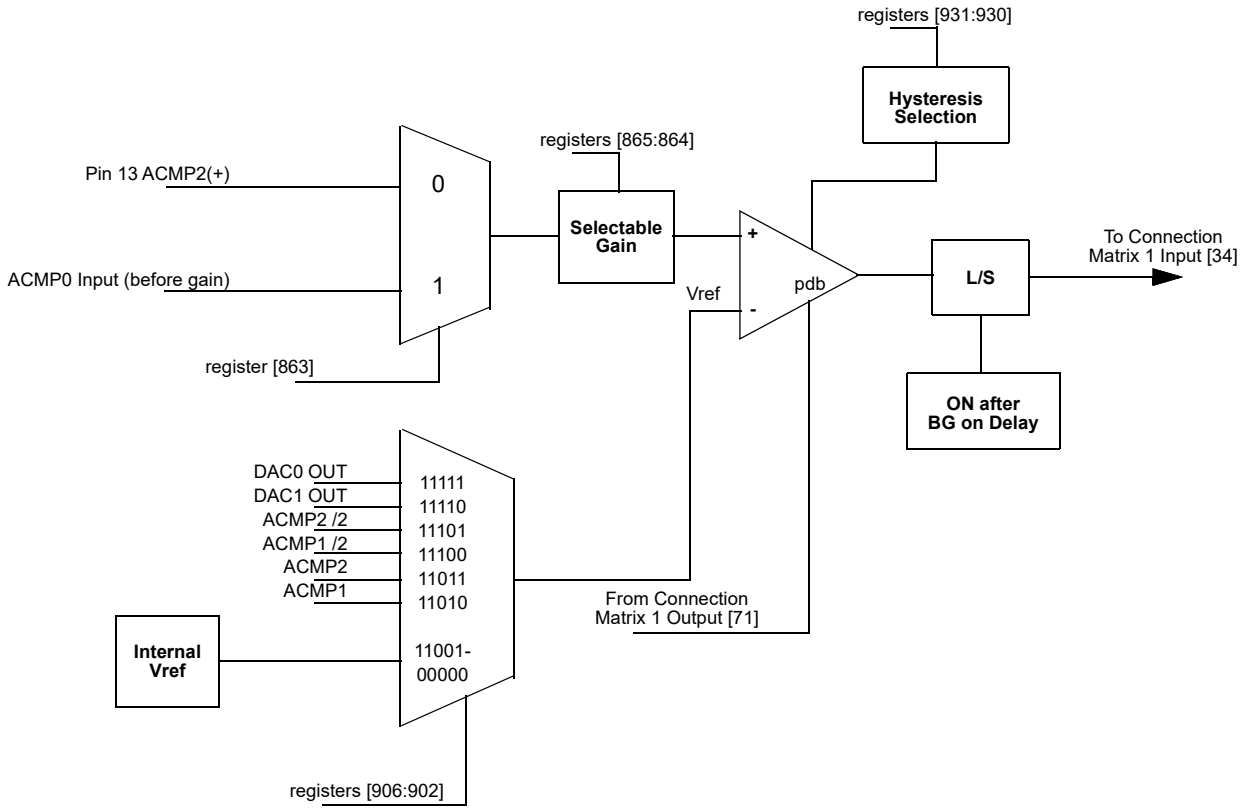


Figure 42: ACMP2 Block Diagram

11.5 ACMP3 BLOCK DIAGRAM

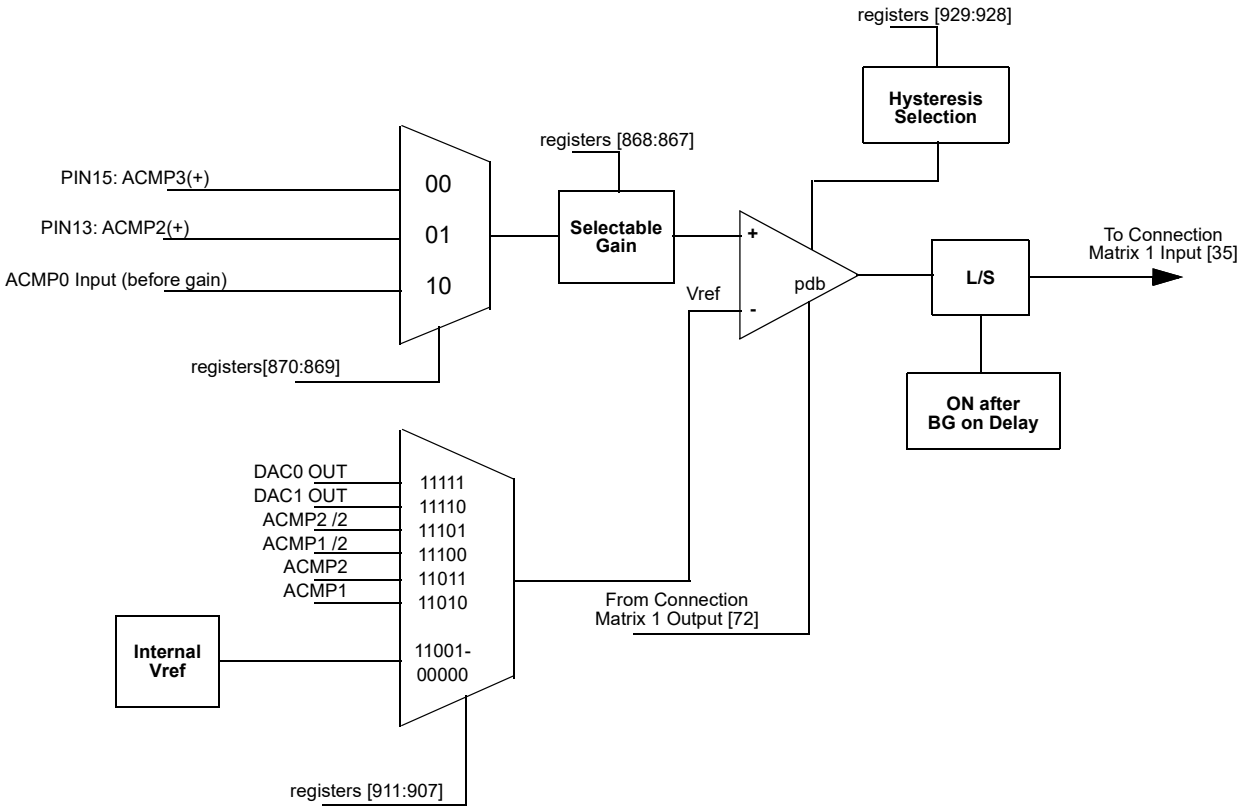


Figure 43: ACMP3 Block Diagram

11.6 ACMP4 BLOCK DIAGRAM

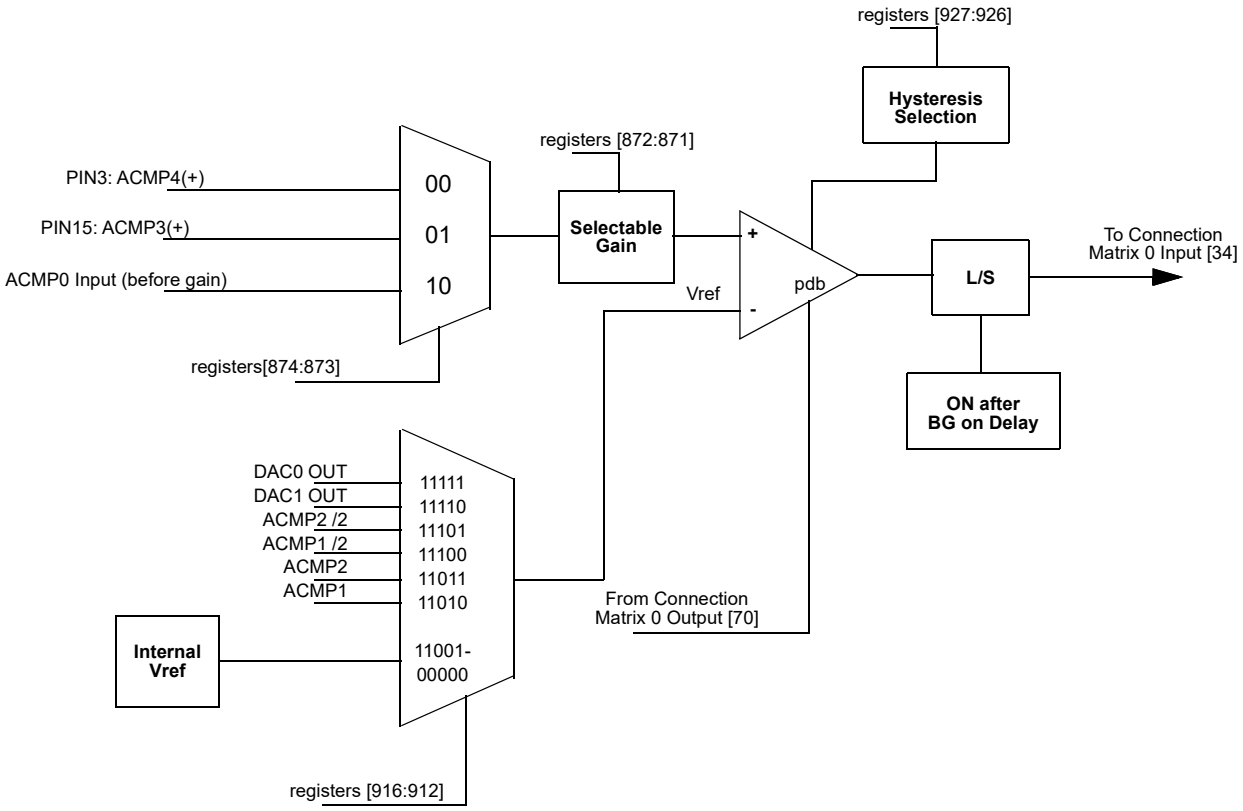


Figure 44: ACMP4 Block Diagram

11.7 ACMP5 BLOCK DIAGRAM

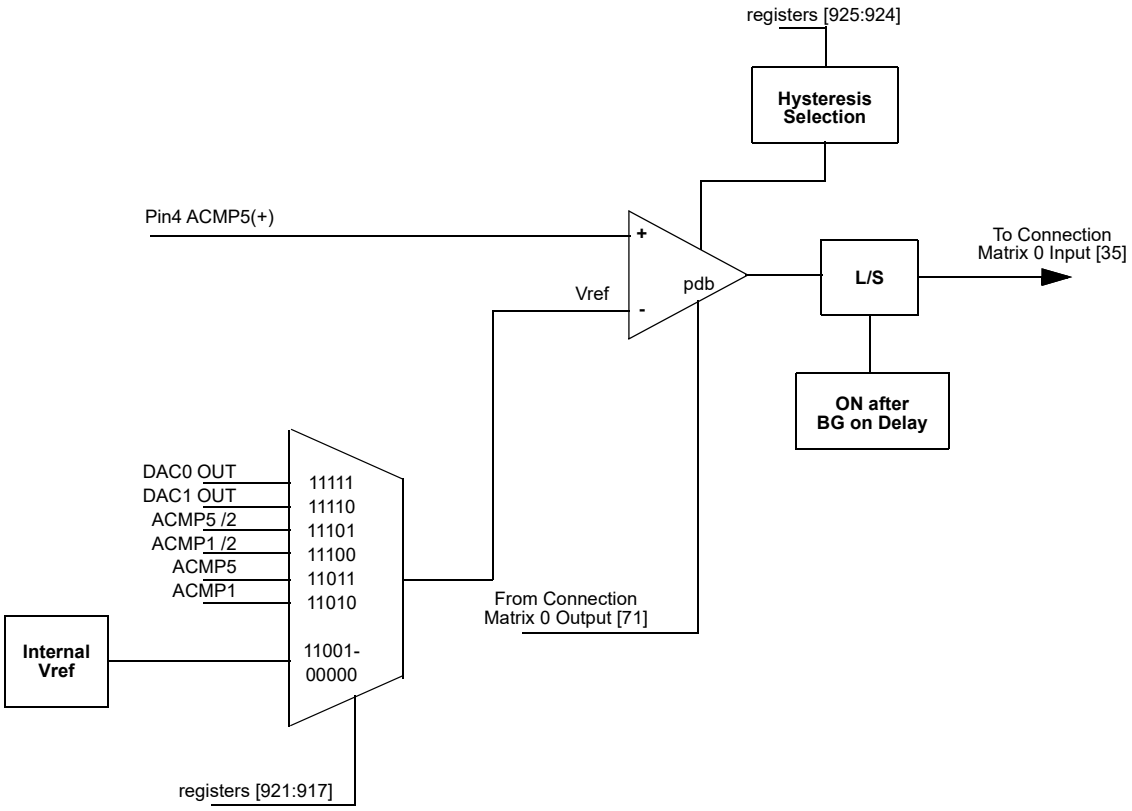


Figure 45: ACMP5 Block Diagram

11.8 ACMP TYPICAL PERFORMANCE

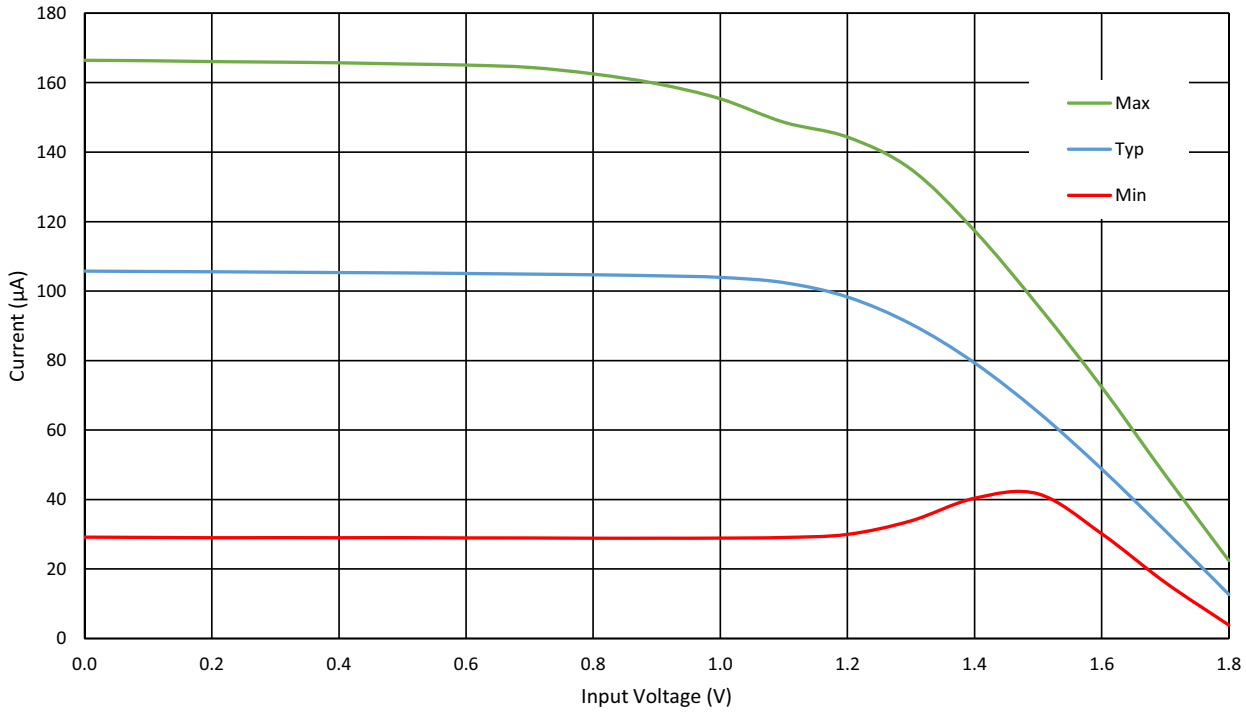


Figure 46: ACMP Input Current Source vs. Input Voltage at T_A = -40 °C to 105 °C, V_{DD} = 3.3 V

12 Digital Storage Elements

There are twelve D Flip-Flop/Latches (DFF/LATCH) logic cells within the SLG46620-A available for design. The source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/LATCH macrocells have user selection for initial state. The macrocells DFF0, DFF1, DFF2, DFF6, DFF7, and DFF8 have an additional input from the matrix that can serve as a nSet or nRST function to the macrocell.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

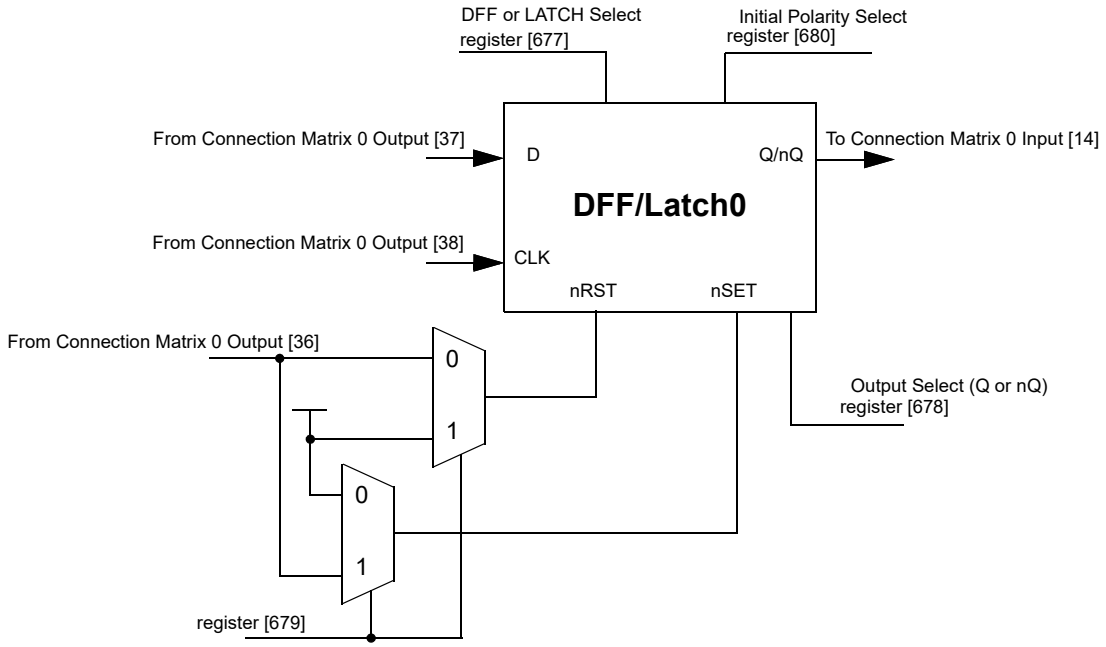


Figure 47: DFF/Latch0

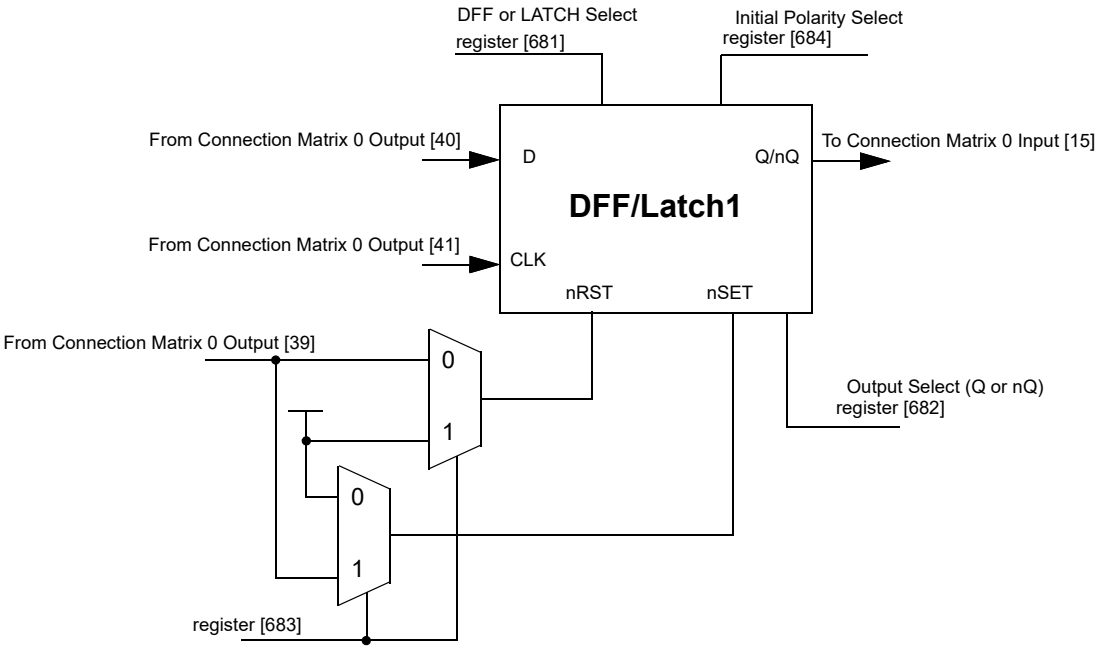


Figure 48: DFF/Latch1

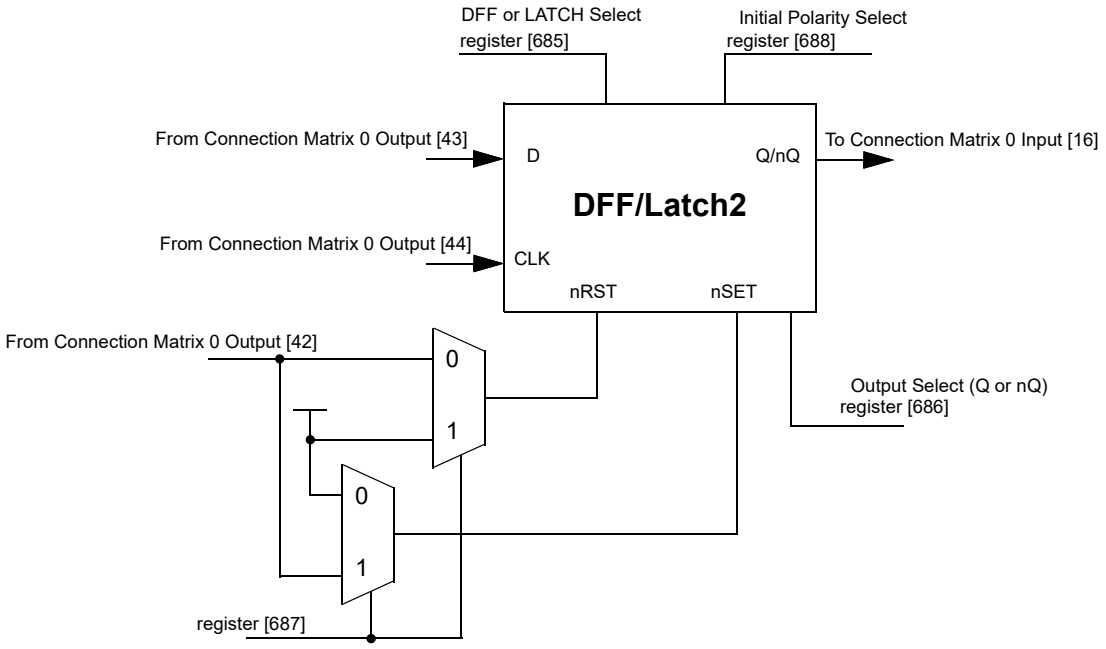


Figure 49: DFF/Latch2

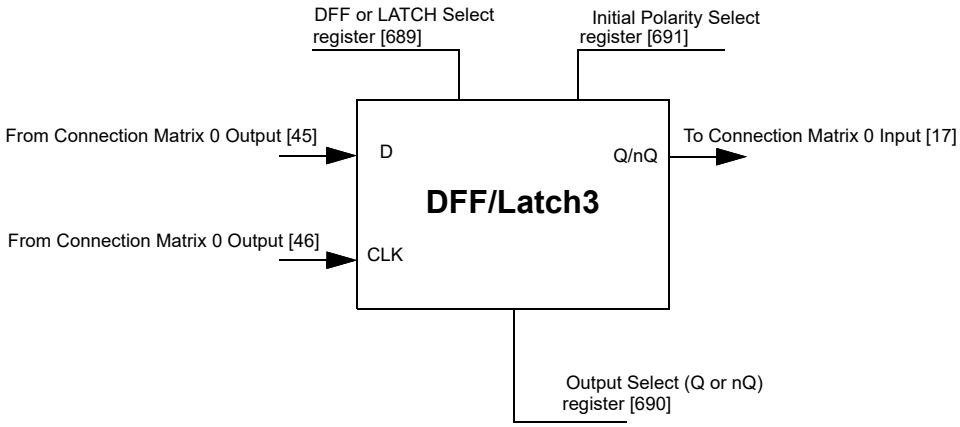


Figure 50: DFF/Latch3

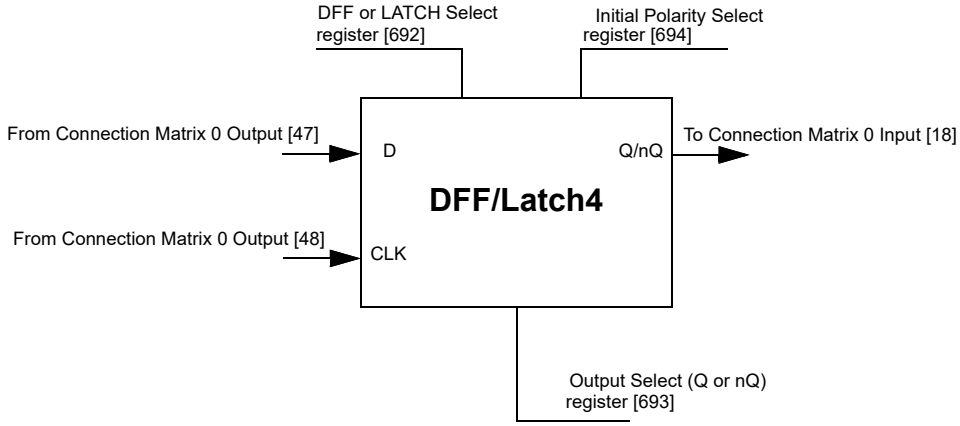


Figure 51: DFF/Latch4

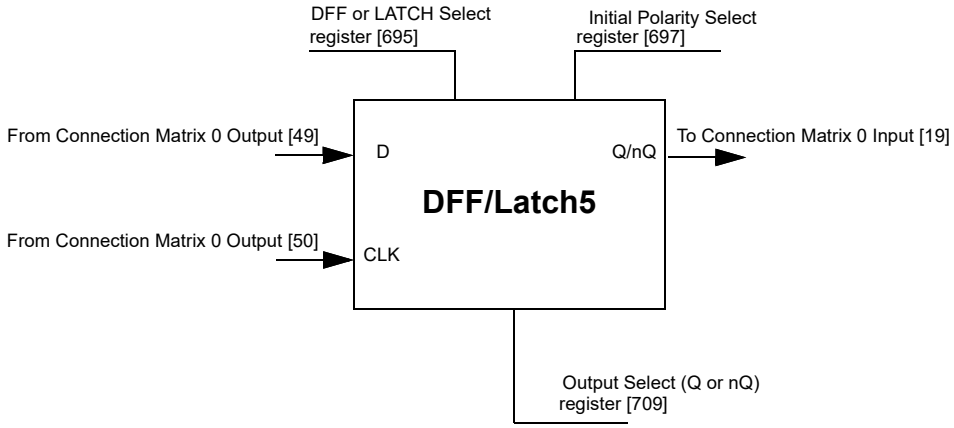


Figure 52: DFF/Latch5

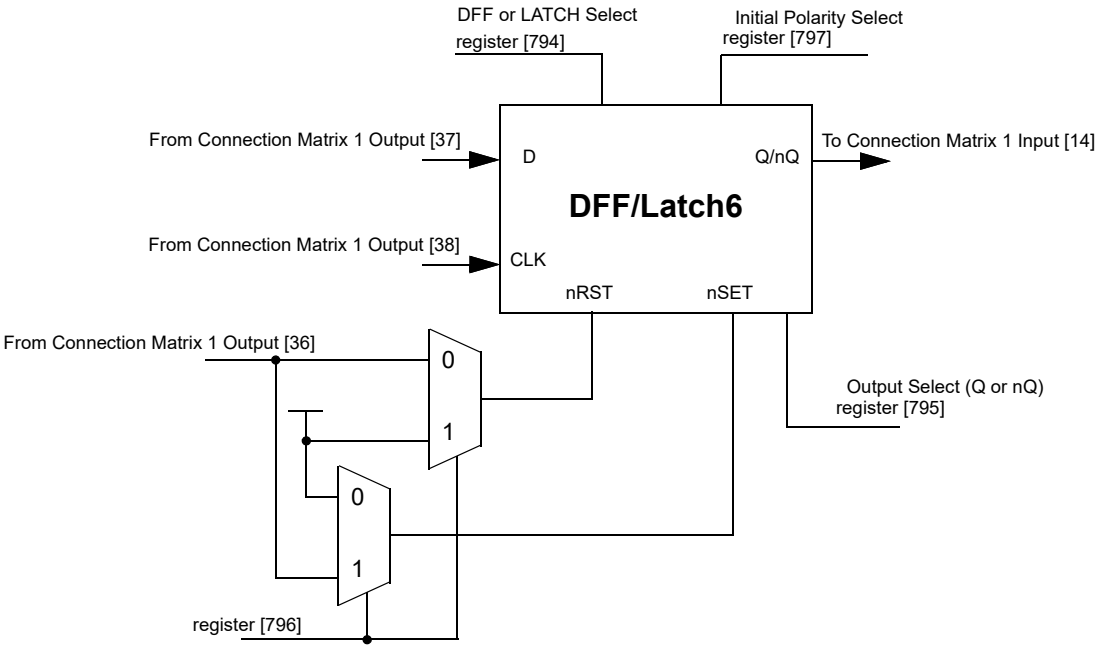


Figure 53: DFF/Latch6

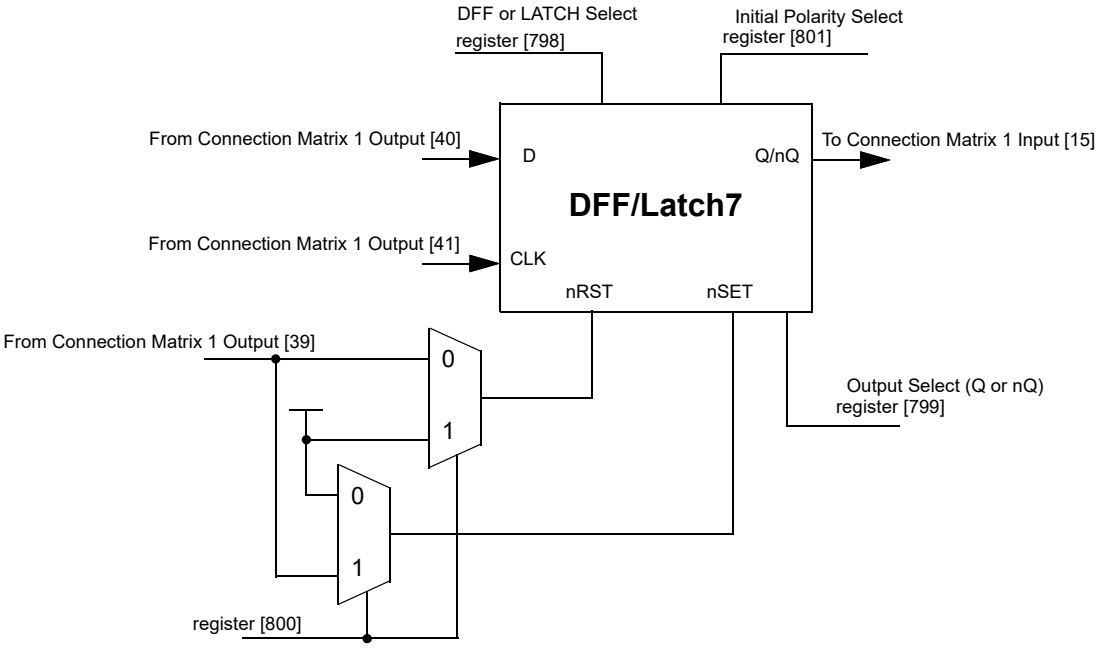


Figure 54: DFF/Latch7

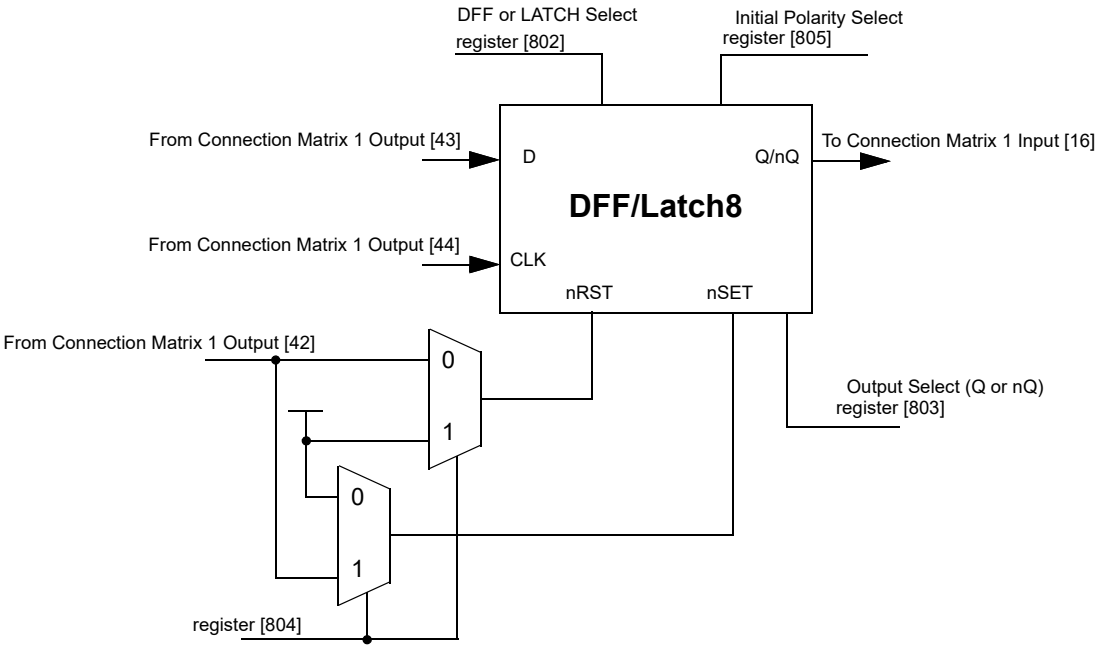


Figure 55: DFF/Latch8

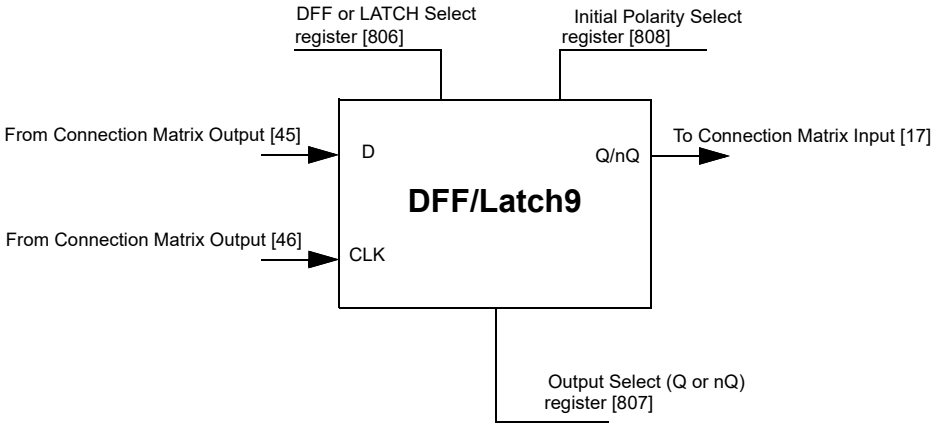


Figure 56: DFF/Latch9

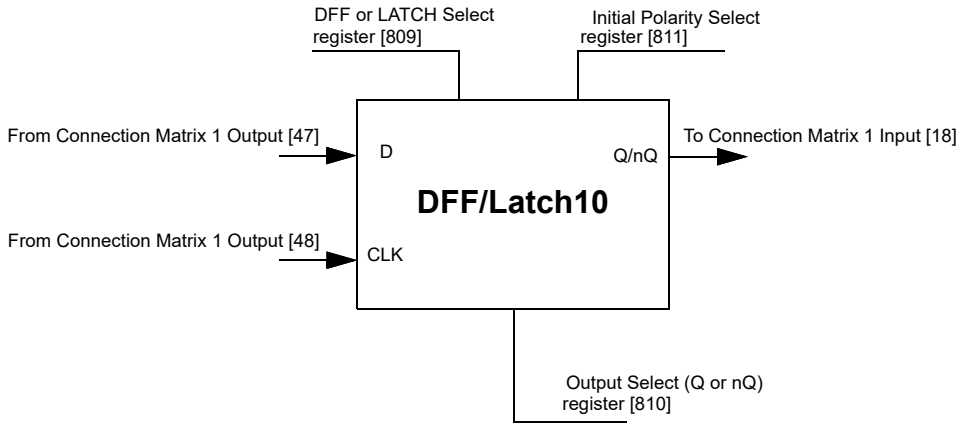


Figure 57: DFF/Latch10

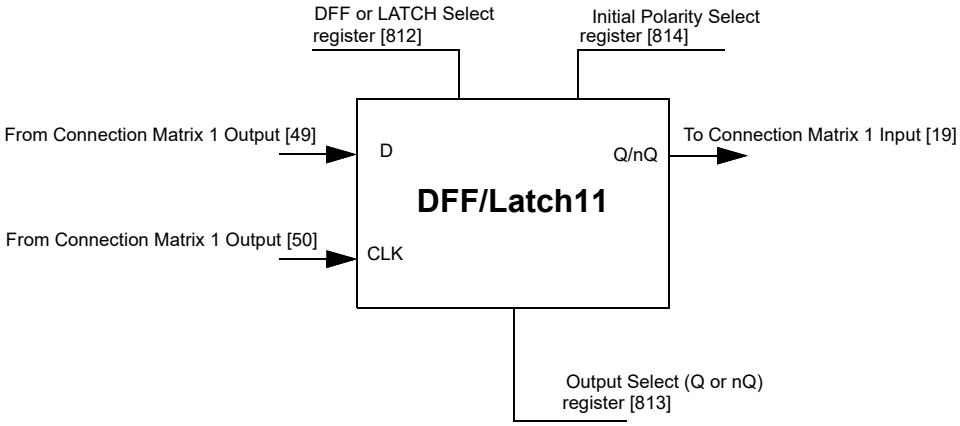


Figure 58: DFF/Latch11

12.1 INITIAL POLARITY OPERATIONS

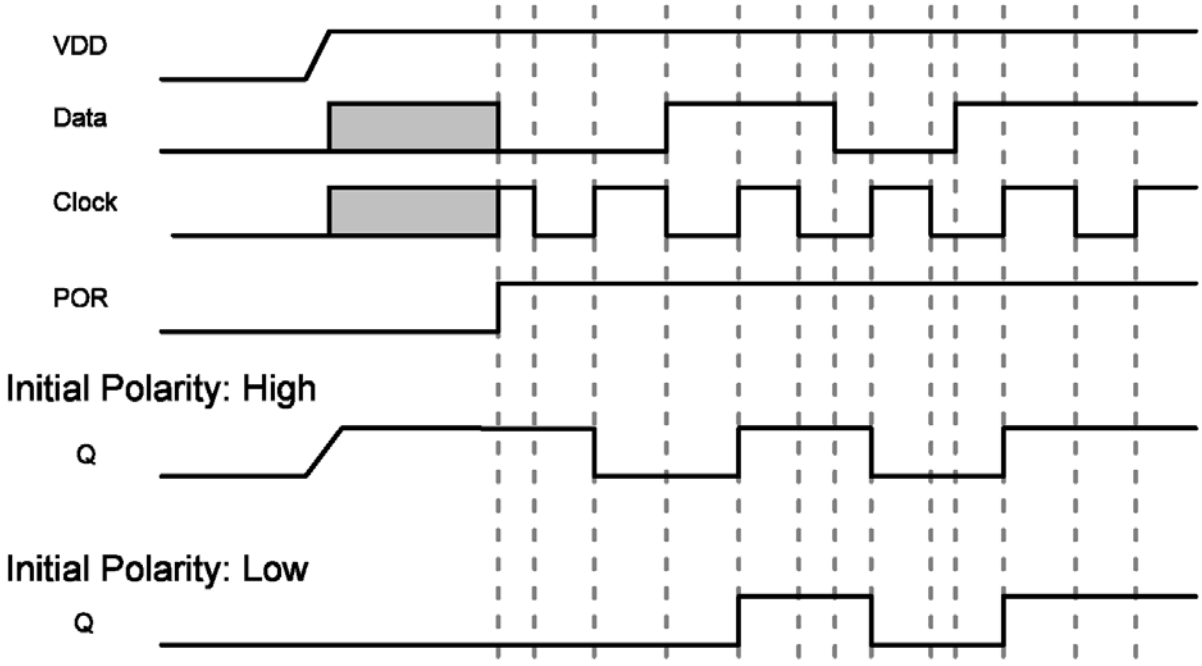


Figure 59: DFF Polarity Operations

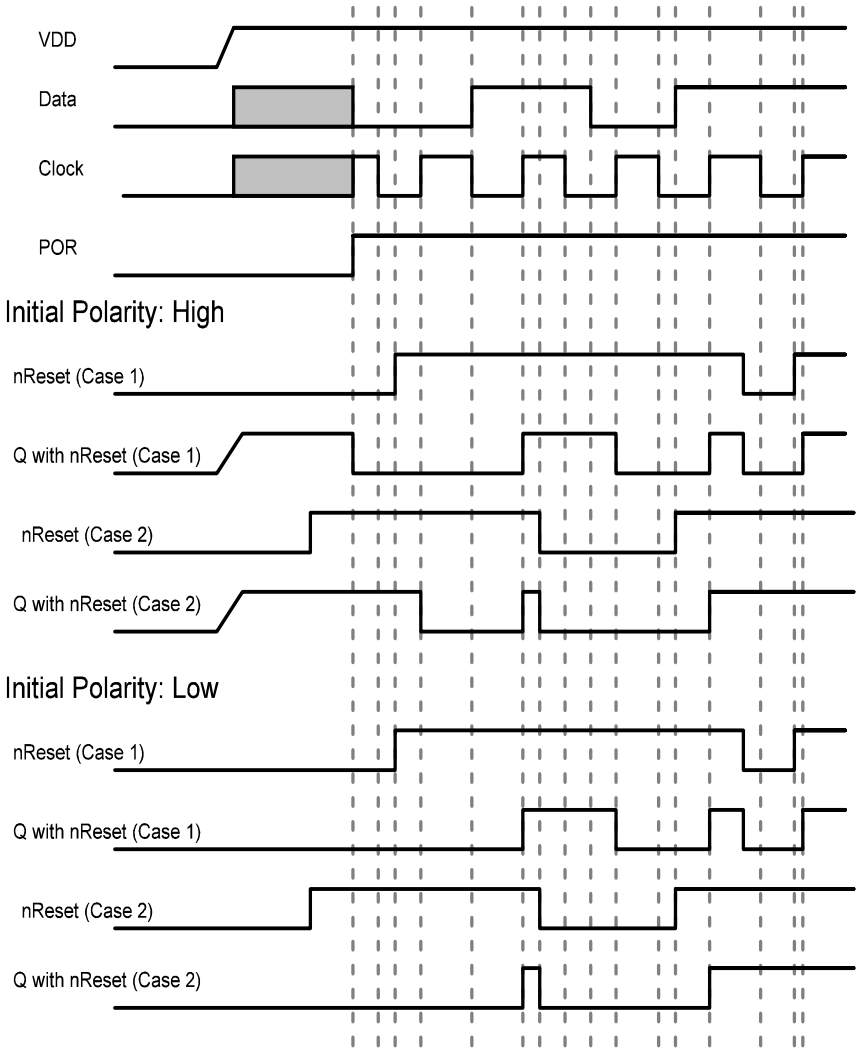


Figure 60: DFF Polarity Operations with nRST

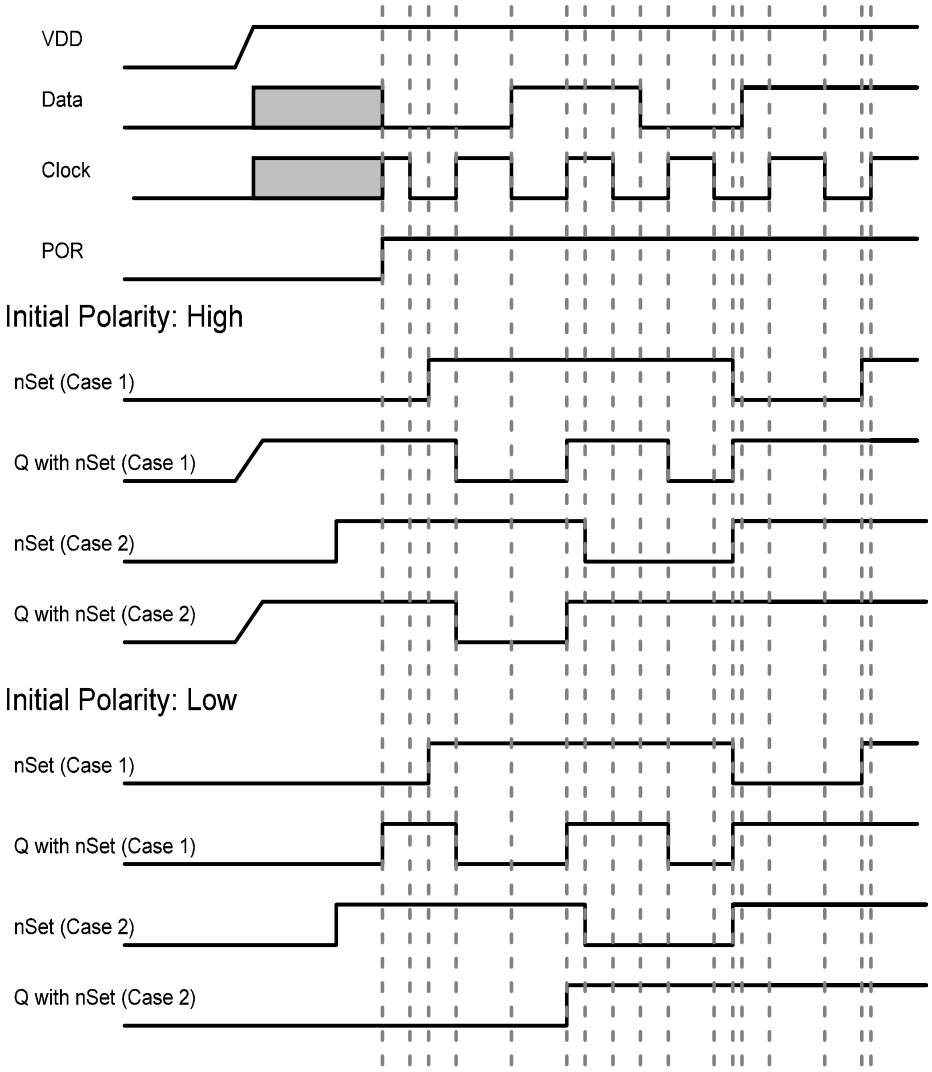


Figure 61: DFF Polarity Operations with nSet

13 Counters/Delay Generators

There are ten configurable counters/delay (CNT/DLY) generators in the SLG46620-A. Four of these counters/delay generators (CNT/DLY 0, 1, 2 and 3) are 14-bit, and six of the counters/delay generators (CNT/DLY 4, 5, 6, 7, 8 and 9) are 8-bit. Each macrocell has a dedicated matrix input connection, some of the macrocells have additional matrix connections to support optional functions, as listed below. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits.

The delay time and counter output equation is as follows:

Delay time = ((counter data + 1) + variable) / Clock
*Variable = (0 or 1) * period*
Counter period = (counter data + 1) / Clock

Note: Variable can be negative, since OSC can operate while Delay input changes. In this case it might be possible that we will not see first period, if OSC rising edge appears immediately after input change.

Counter/delay macrocells (0, 2, 5, 6, 9) are connected to Matrix 0 with both inputs and outputs, counter/delay macrocells (1, 3, 4 7, 8) are connected to Matrix 1 with both inputs and outputs.

Four of the counter/delay generator macrocells (CNT/DLY 0,1,2,3) have an optional Edge Detector function.

Two of the counter/delay generator macrocells (CNT/DLY 2,4) have an optional Finite State Machine (FSM) function.These two macrocells each have two additional matrix inputs for Up and Keep to support FSM functionality.

Two of the counter/delay generator macrocells (CNT/DLY 8,9) have an optional PWM Ramp function.

One of the counter/delay generator macrocells (CNT/DLY 0) can optionally serve as a Wake/Sleep Counter.

Please see Table 58 for a summary of all optional functions:

Table 58: Counter/Delay Macrocell Functions Summary

Macrocell	Bit-Width	Counter	Delay	Finite State Machine (FSM)	PWM Ramp	Edge Detector	Wake/Sleep Counter
CNT/DLY0	14-bit	X	X			X	X
CNT/DLY1	14-bit	X	X			X	
CNT/DLY2	14-bit	X	X	X		X	
CNT/DLY3	14-bit	X	X			X	
CNT/DLY4	8-bit	X	X	X			
CNT/DLY5	8-bit	X	X				
CNT/DLY6	8-bit	X	X				
CNT/DLY7	8-bit	X	X				
CNT/DLY8	8-bit	X	X		X		
CNT/DLY9	8-bit	X	X		X		

Note: Counters initialize with counter data after POR.

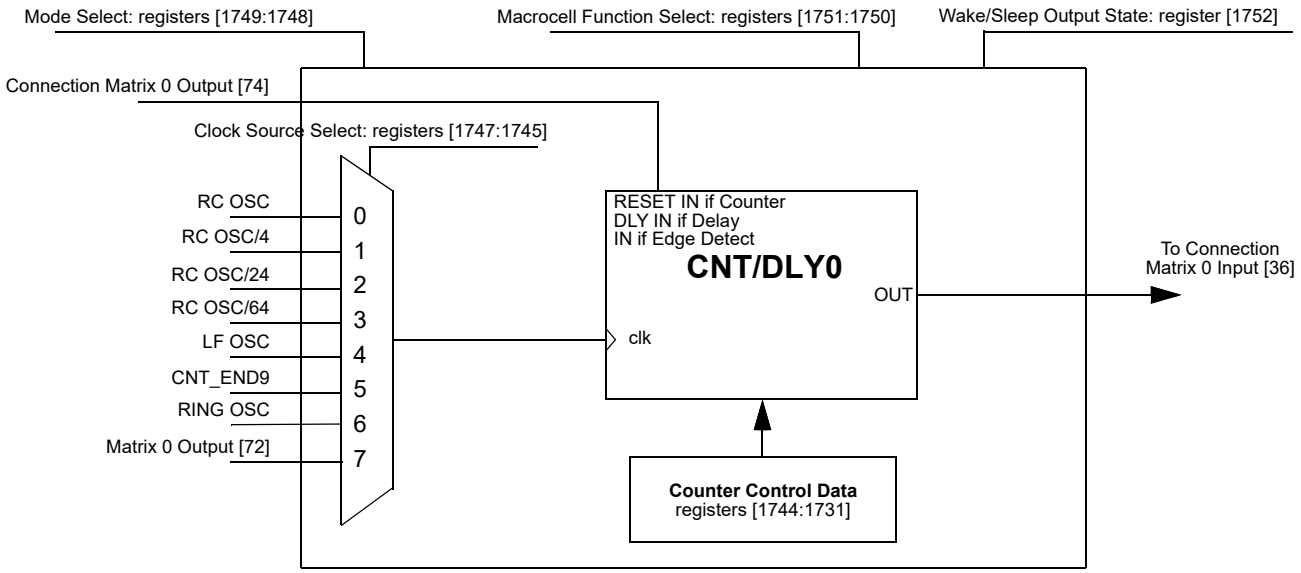


Figure 62: CNT/DLY0

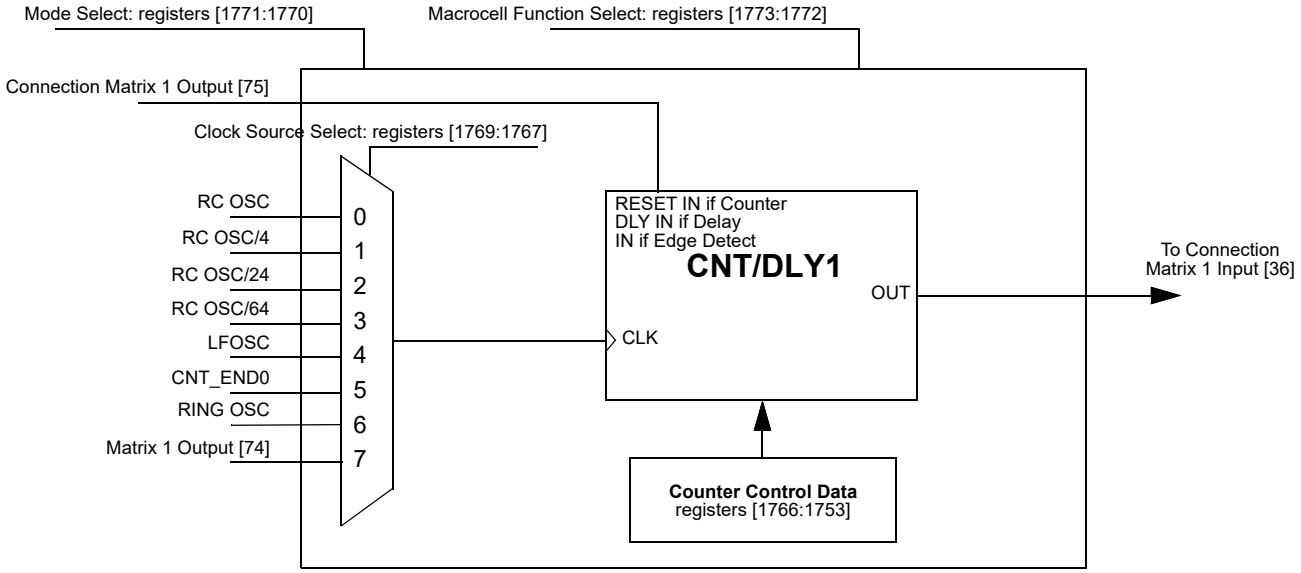


Figure 63: CNT/DLY1

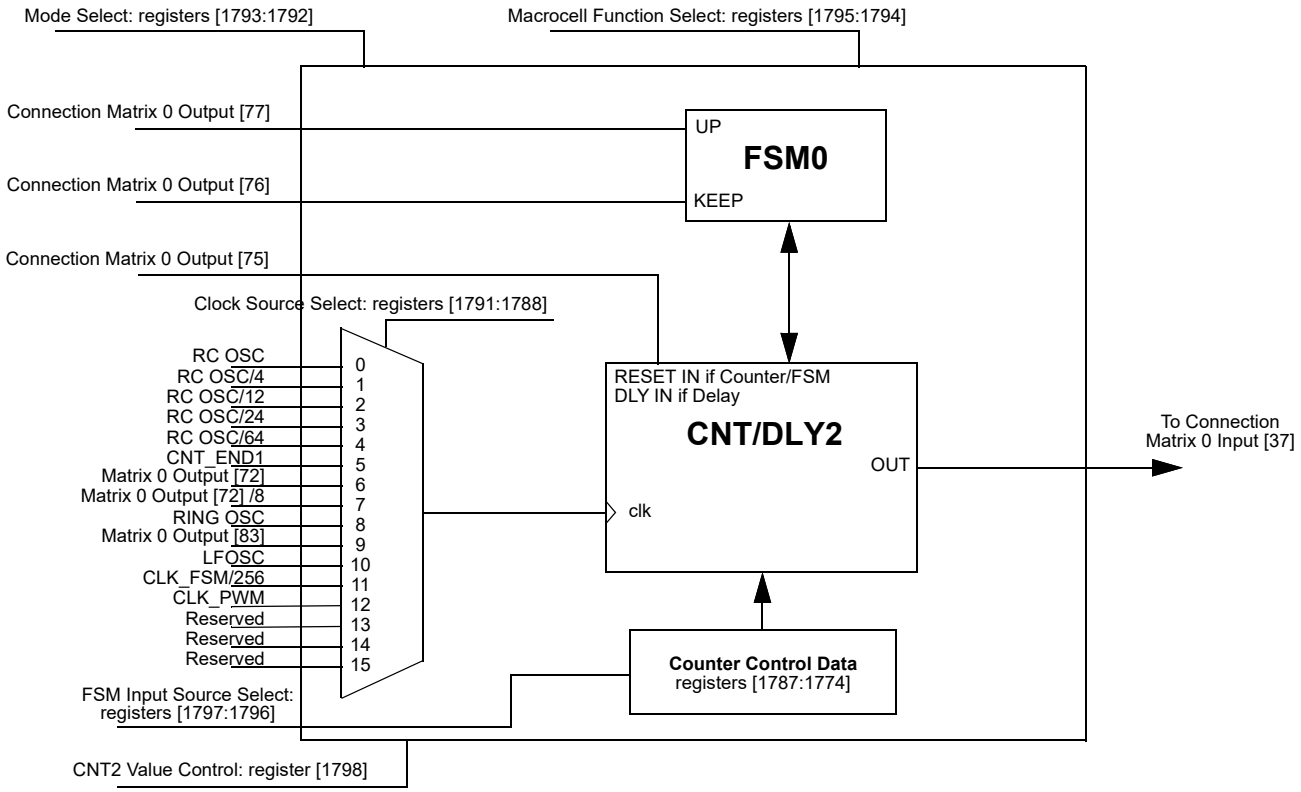


Figure 64: CNT/DLY2/FSM0

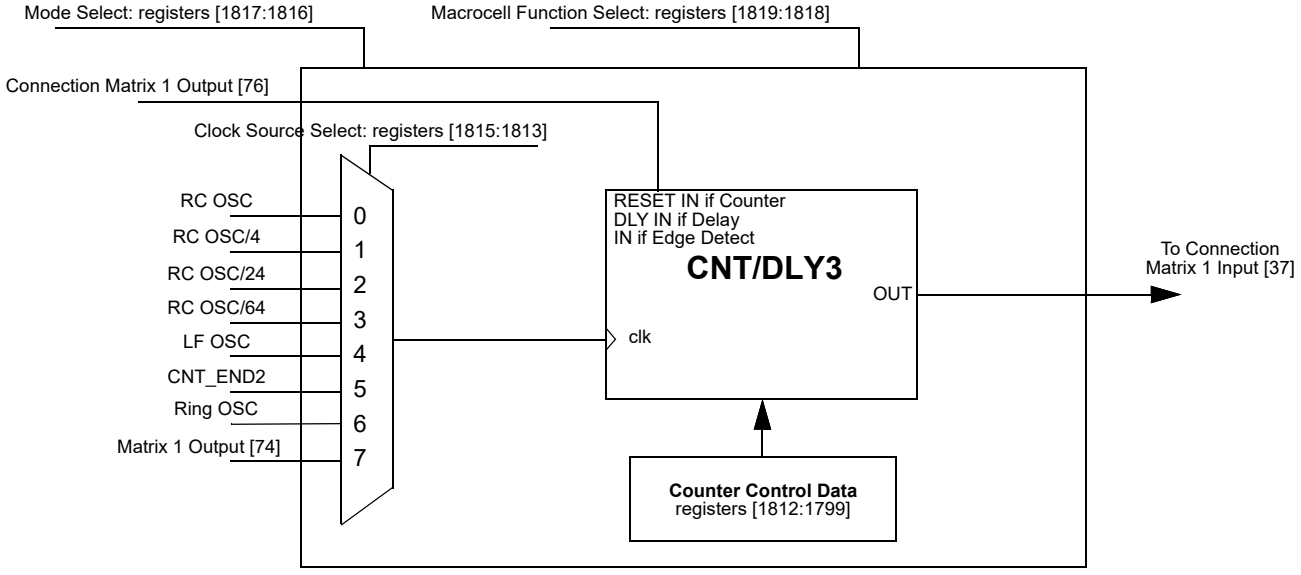


Figure 65: CNT/DLY3

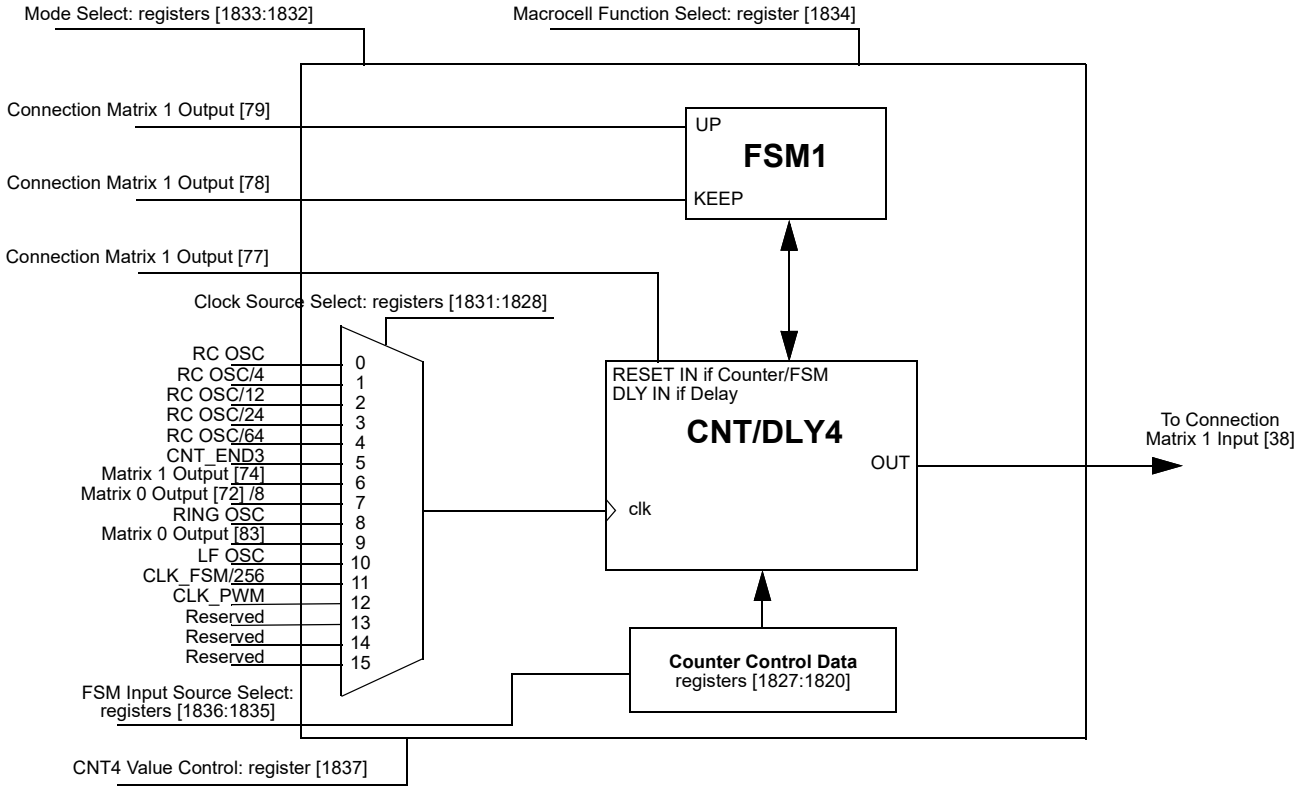


Figure 66: CNT/DLY4/FSM1

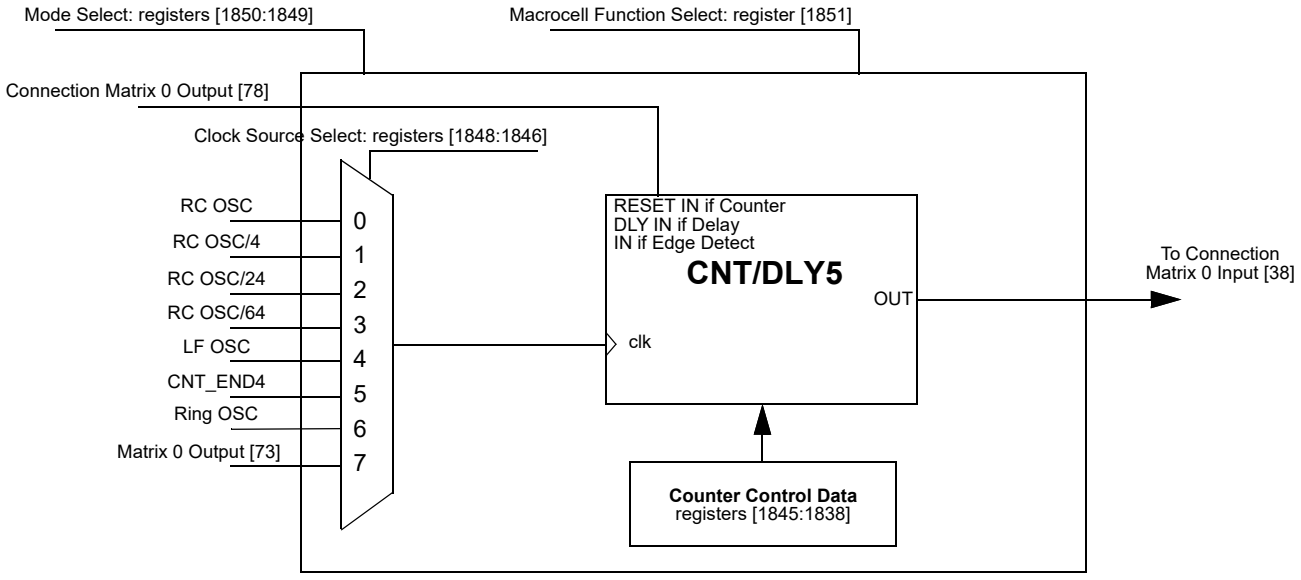


Figure 67: CNT/DLY5

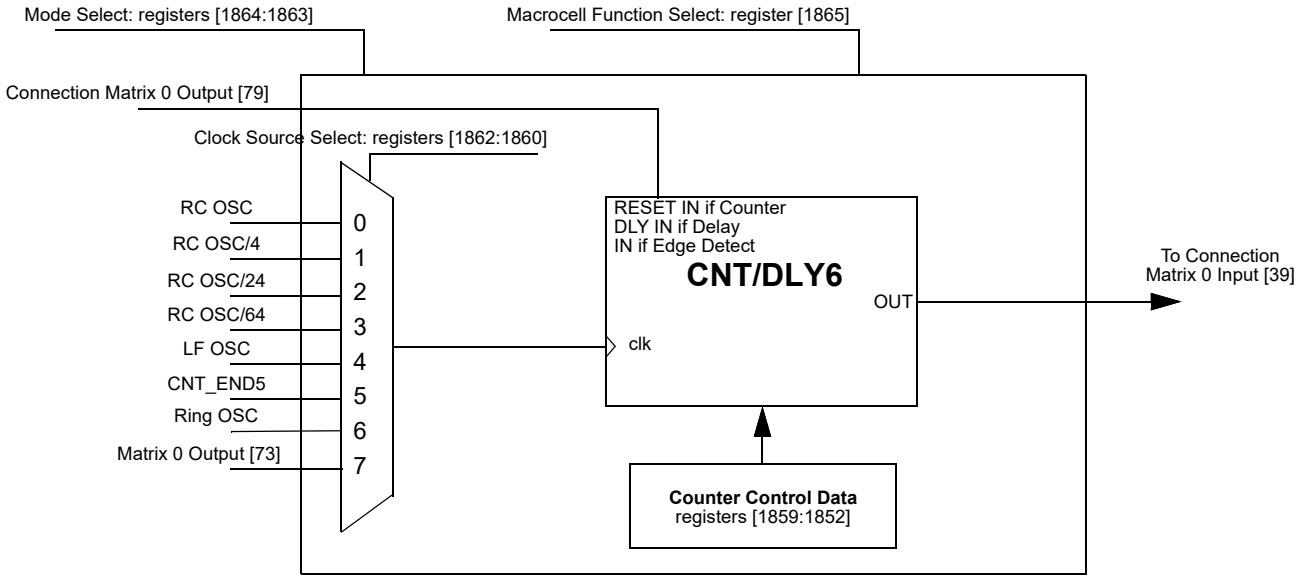


Figure 68: CNT/DLY6

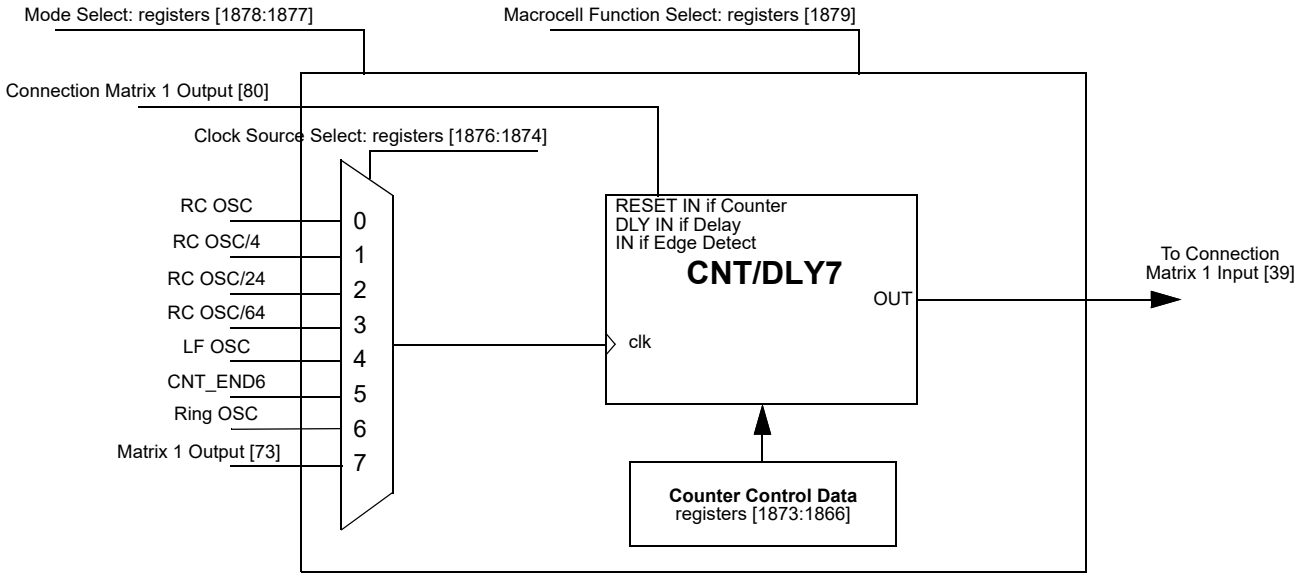


Figure 69: CNT/DLY7

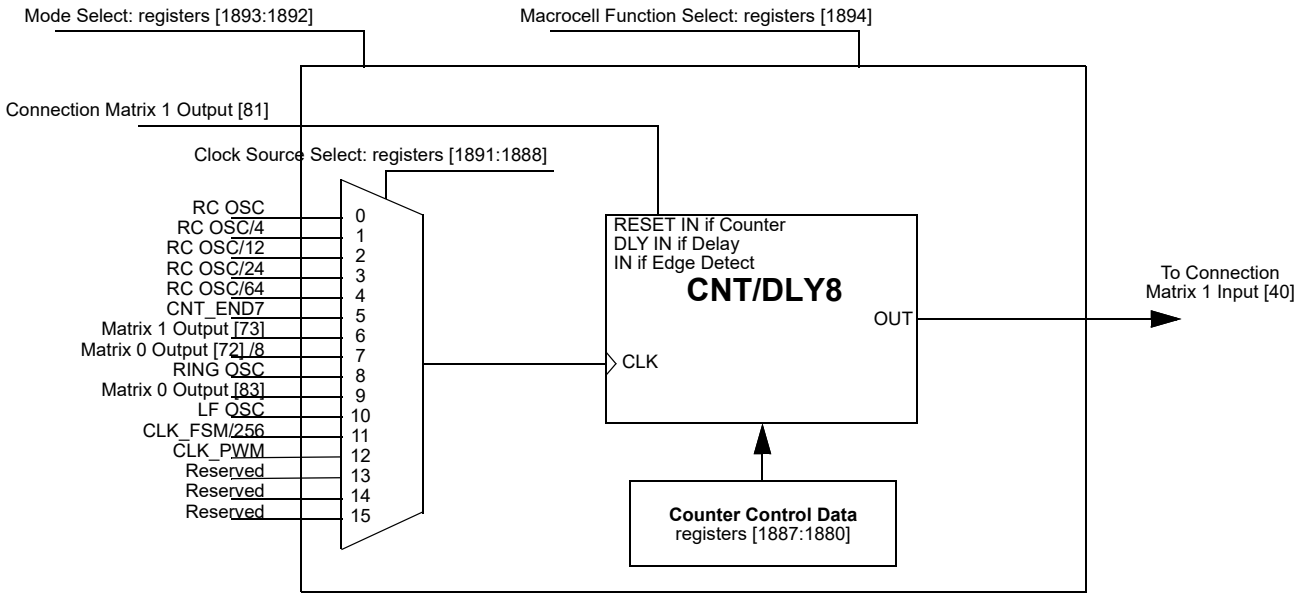


Figure 70: CNT/DLY8/PWM_RAMP

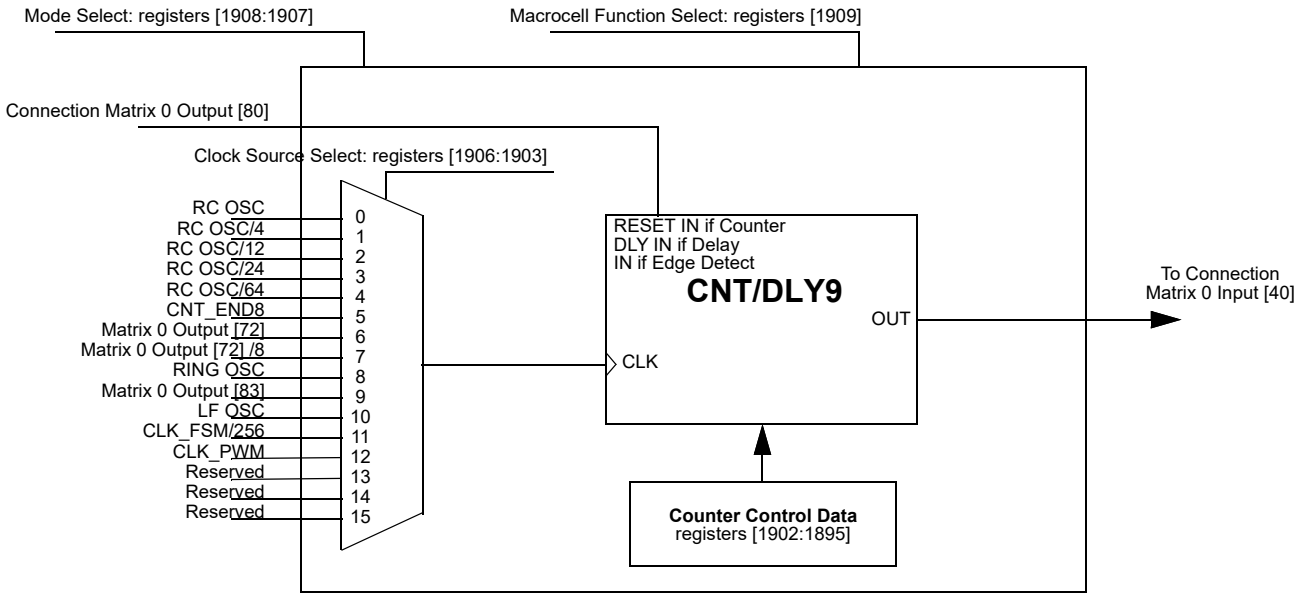


Figure 71: CNT/DLY9/PWM_RAMP

13.1 CNT/DLY TIMING DIAGRAMS

13.1.1 Delay Mode (Counter Data: 3) CNT/DLY0...CNT/DLY9

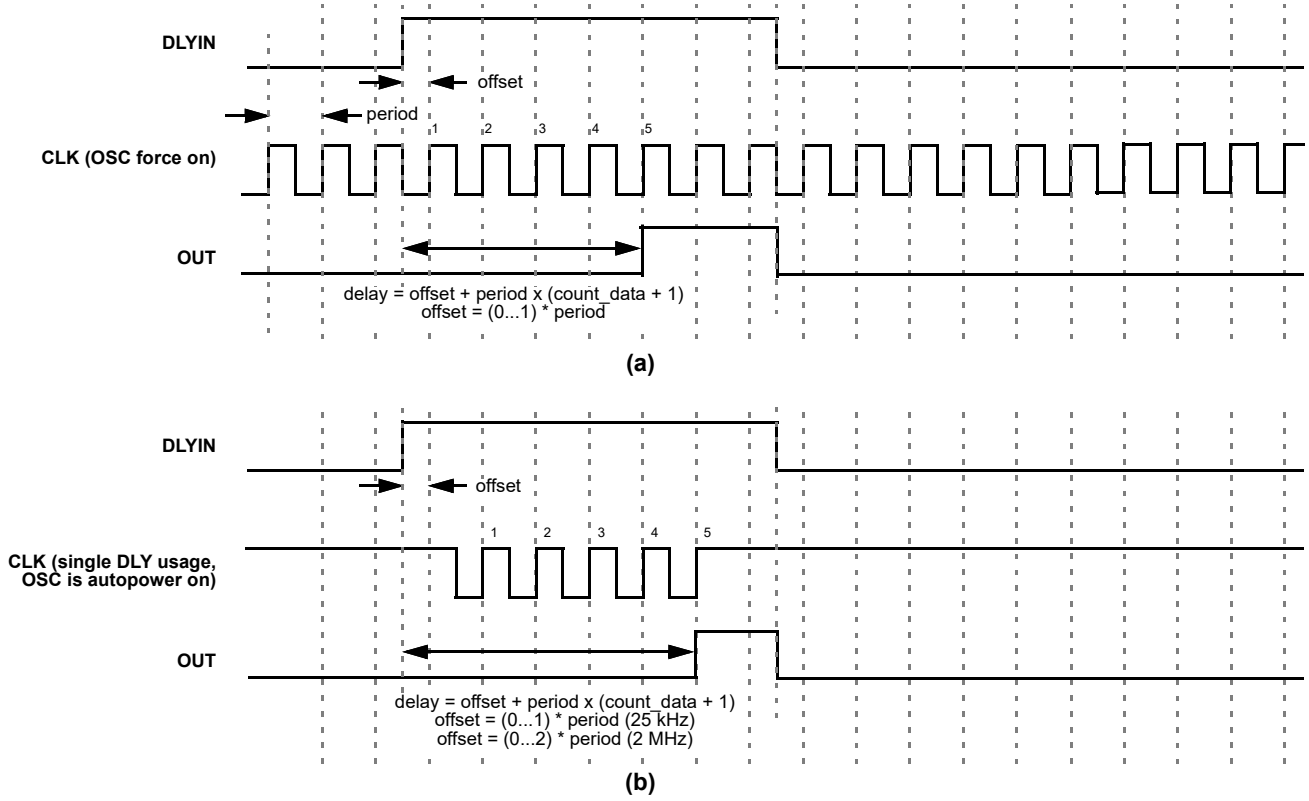


Figure 72: Timing (Rising Edge) for Count Data = 3: (a) Oscillator is in Force Power On Mode or an External Oscillator is Used, (b) Oscillator is in Auto Power On Mode

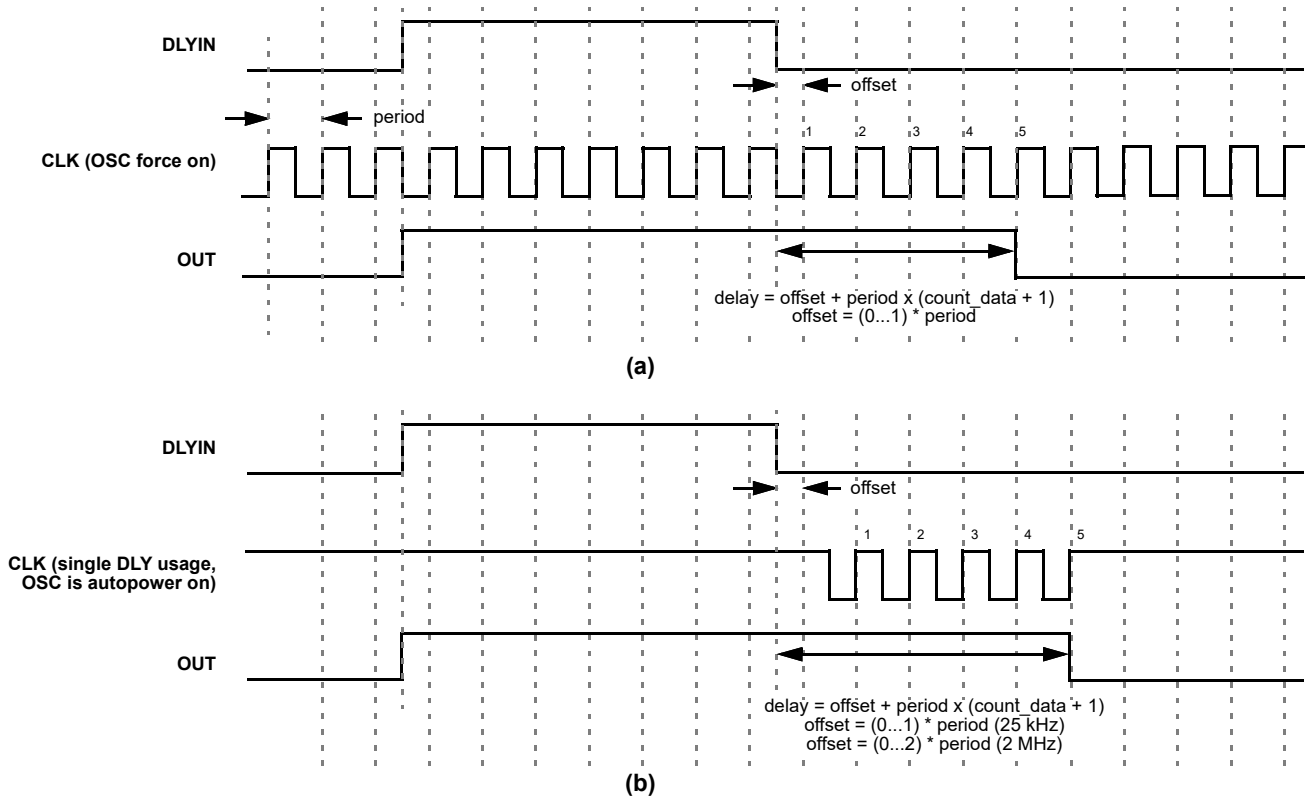


Figure 73: Timing (Falling Edge) for Count Data = 3: (a) Oscillator is in Force Power On Mode or an External Oscillator is Used, (b) Oscillator is in Auto Power On Mode

13.1.2 Counter Mode (Counter Data: 3) CNT/DLY0...CNT/DLY9

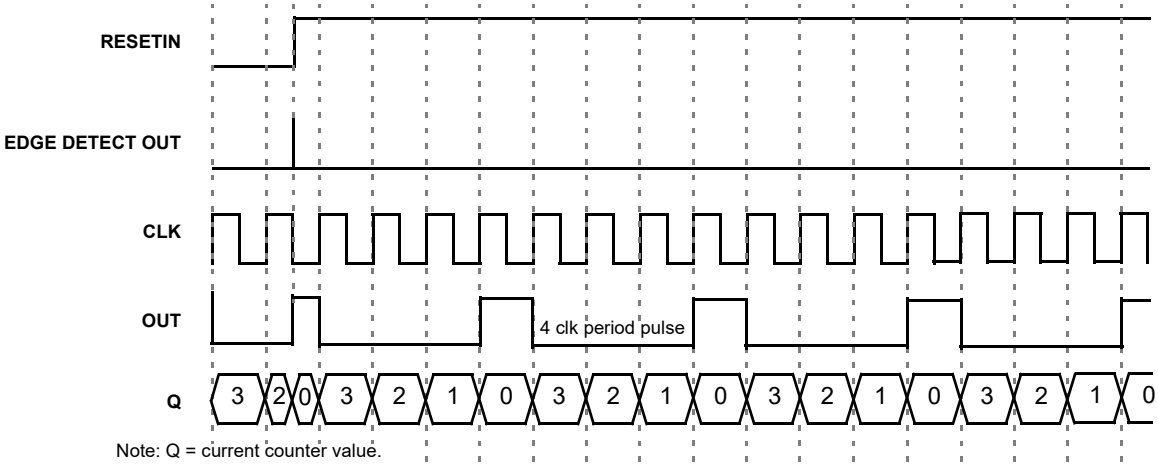


Figure 74: Timing (Reset Rising Edge Mode, Oscillator is Forced on) for Count Data = 3

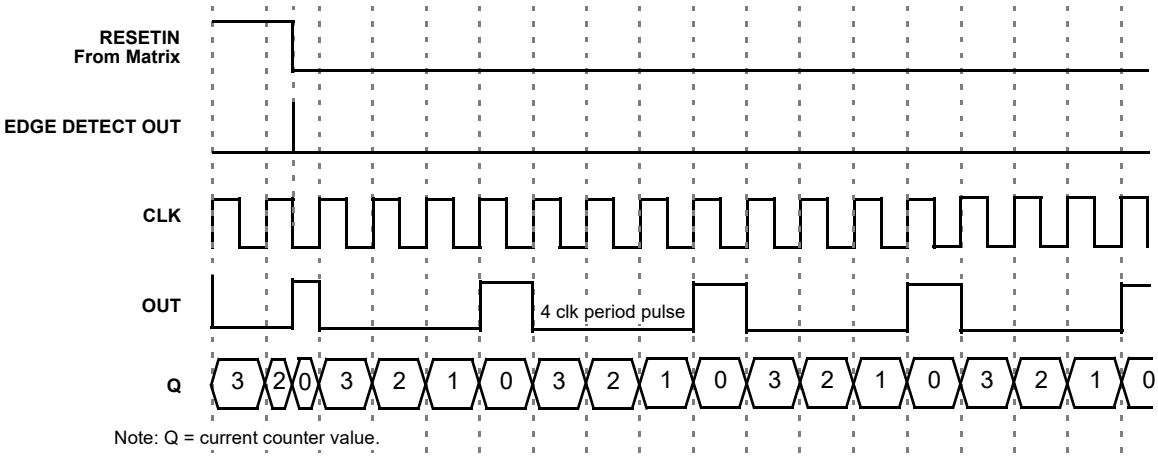


Figure 75: Timing (Reset Falling Edge Mode, Oscillator is Forced on) for Count Data = 3

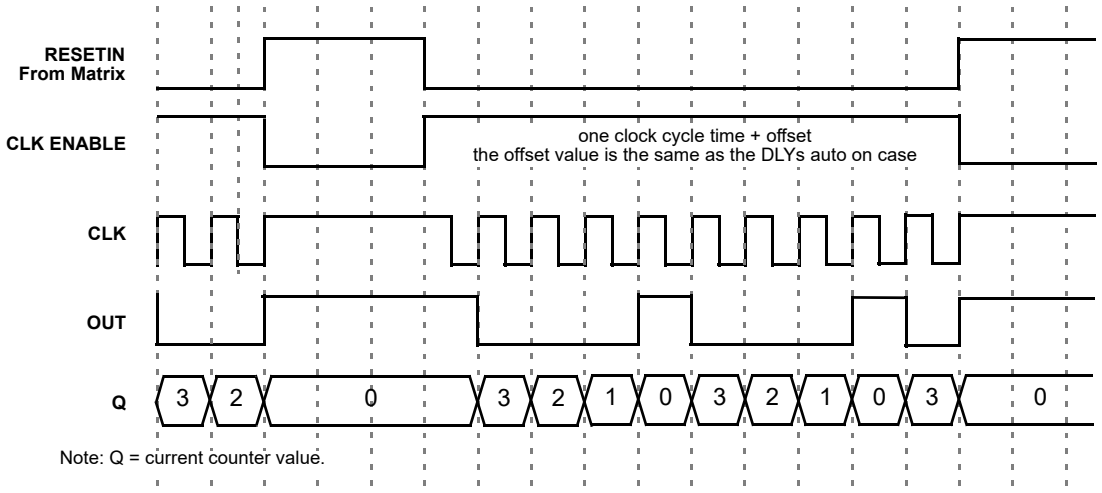


Figure 76: Timing (Reset High Level Mode, Oscillator is Autopowered on (Controlled by Reset)) for Count Data = 3

13.1.3 CNT/FSM Mode CNT/DLY2, CNT/DLY4

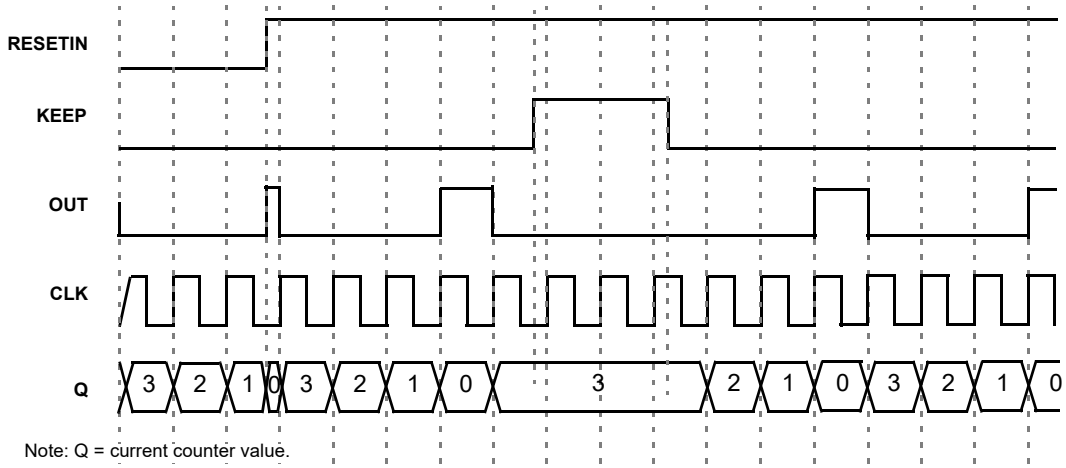


Figure 77: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

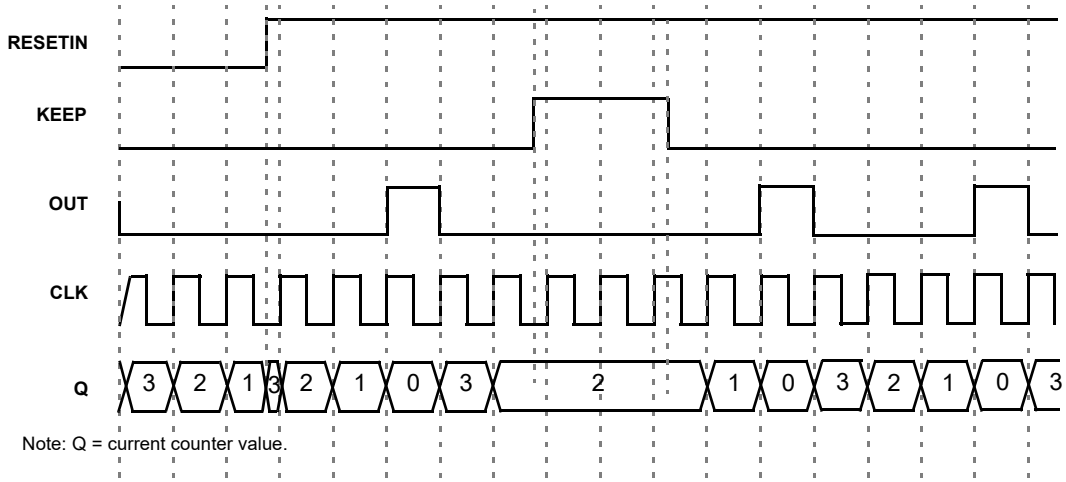


Figure 78: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced on, UP = 0) for Counter Data = 3

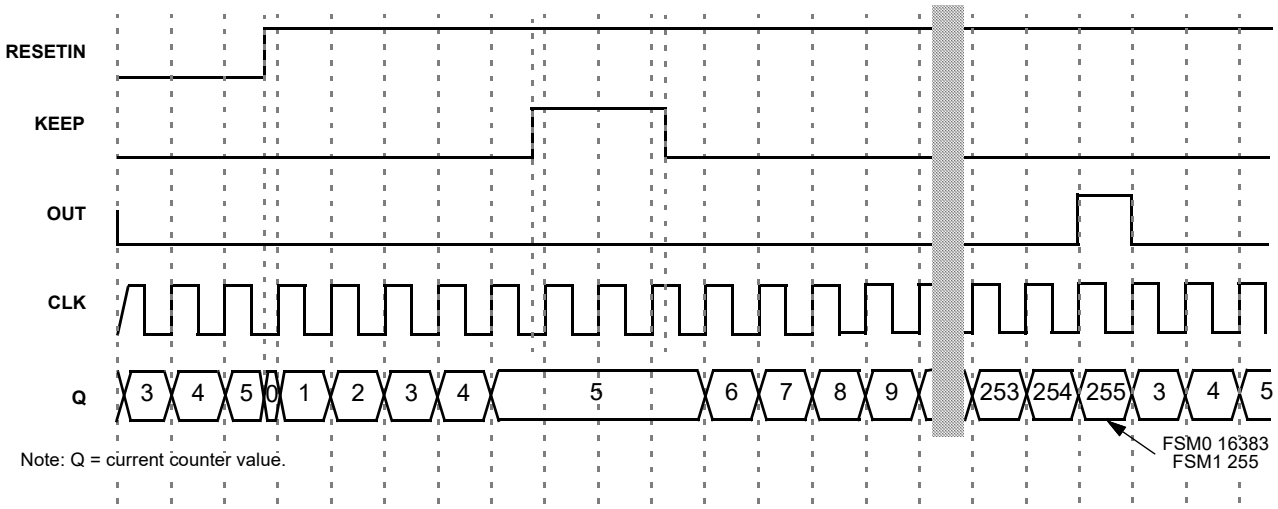


Figure 79: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced on, UP = 1) for Counter Data = 3

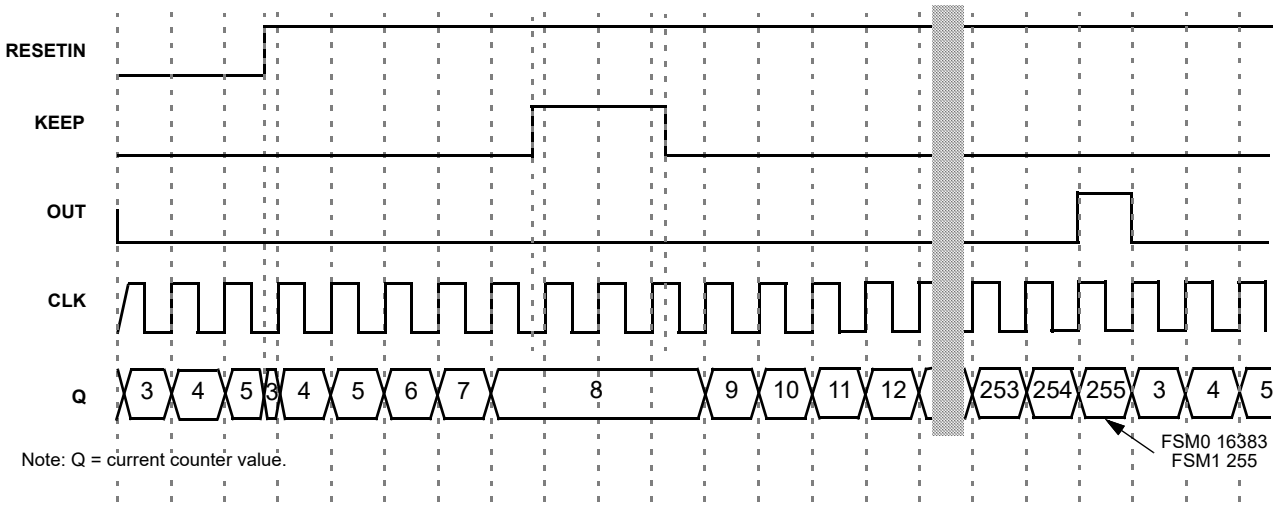


Figure 80: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced on, UP = 1) for Counter Data = 3

14 Digital Comparator/Pulse Width Modulator

The SLG46620-A has three 8-bit digital comparator (DCMP)/ pulse width modulator (PWM) logic macrocells. Each of these three logic macrocells can be either a digital comparator (DCMP) or a pulse width modulator (PWM) independently of how the other two logic macrocells are defined.

Both the DCMP and PWM logic can operate at up to a frequency of 10 MHz. The input power for the three logic macrocells is controlled independently by register [1678] for DCMP0/PWM0, register [1698] for DCMP1/PWM1 and register [1718] for DCMP2/PWM2.

PWM power-down control is configured by register [1677] which is also shared with the ADC and OSC.

14.1 DCMP INPUT MODES

All three DCMP logic macrocells have a positive (IN+) and a negative (IN-) input. The signal (through the IN+ input) takes the value from a 4:1 MUX selection between the following signals:

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the SPI logic cell output (SPI[15:8] for DCMP0 and DCMP2 or SPI[7:0] for DCMP1)
- 8-bit signal from the FSM (FSM0[7:0] for DCMP0 or FSM1[7:0] for DCMP1 and DCMP2)
- 8-bit user defined signal value.

The signal (through the IN- input) takes the value from a 4:1 MUX selection between the following signals:

- 8-bit signal from the CNT (CNT9'Q [7:0] for DCMP1 or CNT8'Q [7:0] for DCMP0 and DCMP2)
- 8-bit signal from the SPI logic cell output (SPI[7:0] for DCMP0 and DCMP2 or SPI[15:8] for DCMP1)
- 8-bit signal from the FSM (FSM1' Q [7:0] for DCMP0 or FSM0'Q[7:0] for DCMP1 and DCMP2)
- 8-bit user defined signal value.

14.2 DCMP OUTPUT MODES

The two 8-bit parallel data inputs from IN+ and IN- are compared within the DCMP logic macrocells to produce the output (OUT+) and an *Equal* signal (EQ).

There are two cases for the OUT+ signal controlled by register [1714], register [1694], register [1673].

If these registers = 0, then

- if *inp* > *inn, OUT*+ = 1, EQ = 0
- if *inp* < *inn*, *OUT*+ = 0, EQ = 0
- if *inp* = *inn, OUT*+ = 0, EQ = 1

If these registers = 1, then

- if *inp* > *inn, OUT*+ = 1, EQ = 0
- if *inp* < *inn, OUT*+ = 0, EQ = 0
- if *inp* = *inn, OUT*+ = 1, EQ = 1

Both the OUT+ and EQ signals are triggered by the rising or falling edge (controlled by register [1676], register [1697] and register[1717]) of the CLK OSC signal (clock source is defined by registers [1629:1628]) and result of comparison can be read in the next clock pulse, see Figure 81, where register [1714], register [1694], register [1673] are equal 0.

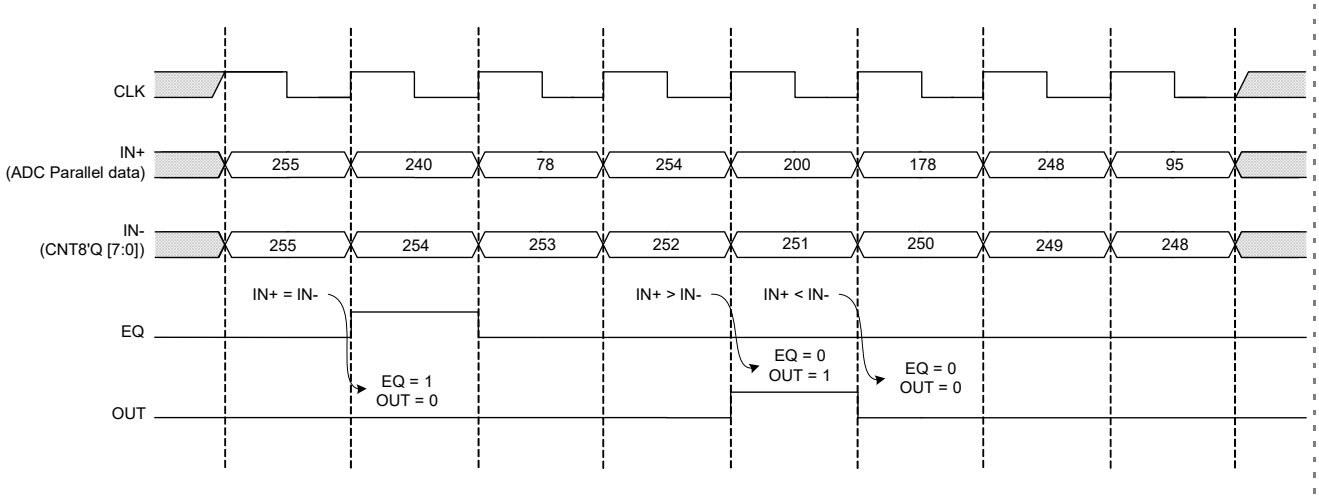


Figure 81: DCMP Timing Diagram

14.3 PWM INPUT MODES

IN+ for the PWM is an 8-bit data string that can be selected from one of four sources;

- 8-bit signal from the ADC Parallel Output
- 8-bit signal from the SPI logic cell output (SPI[15:8] for DCMP0 and DCMP1 or SPI[7:0] for DCMP2)
- 8-bit signal from the FSM0[7:0]
- 8-bit user defined signal value

IN-'s 8-bit data string for all PWMs is sourced from an 8-bit signal from CNT/DLY1.

14.4 PWM OUTPUT MODES

The output (*OUT+*) duty cycle can be set to either count down to 0 % or count up to 100 % and each PWM is independently controlled by the value of register [1673] (PWM0), register [1694] (PWM1), and register [1714] (PWM2). When both inputs are equal the output signal (*EQ*) will go high. The outputs (*OUT-* and *OUT+*) are non-overlapping.

When registers [1673/1694/1714] = "0"

- PWM output duty cycle ranges from 0 % to 99.61 % and is determined by: Output Duty Cycle = IN+/256
- (IN+ = 0: output duty cycle = 0/256 = 0 %; IN+ = 255: output duty cycle = 255/256 = 99.61 %)
- Output signals are triggered by the rising or falling edge of the *CLK OSC* signal (defined by bit registers [1676], [1697], [1717]).

When registers [1673/1694/1714] = "1"

- PWM output duty cycle ranges from 0.39 % to 100 % and is determined by Output Duty Cycle = (IN+ + 1)/256
- 8(IN+ = 0: output duty cycle = 1/256 = 0.39 %; IN+ = 255: output duty cycle = 256/256 = 100 %)
- Output signals are triggered by the rising or falling edge of the *CLK OSC* signal (defined by bit registers [1676], [1697], [1717]).

When IN+ = IN- then EQ = "1".

14.5 DCMP0/PWM0 FUNCTIONAL DIAGRAM

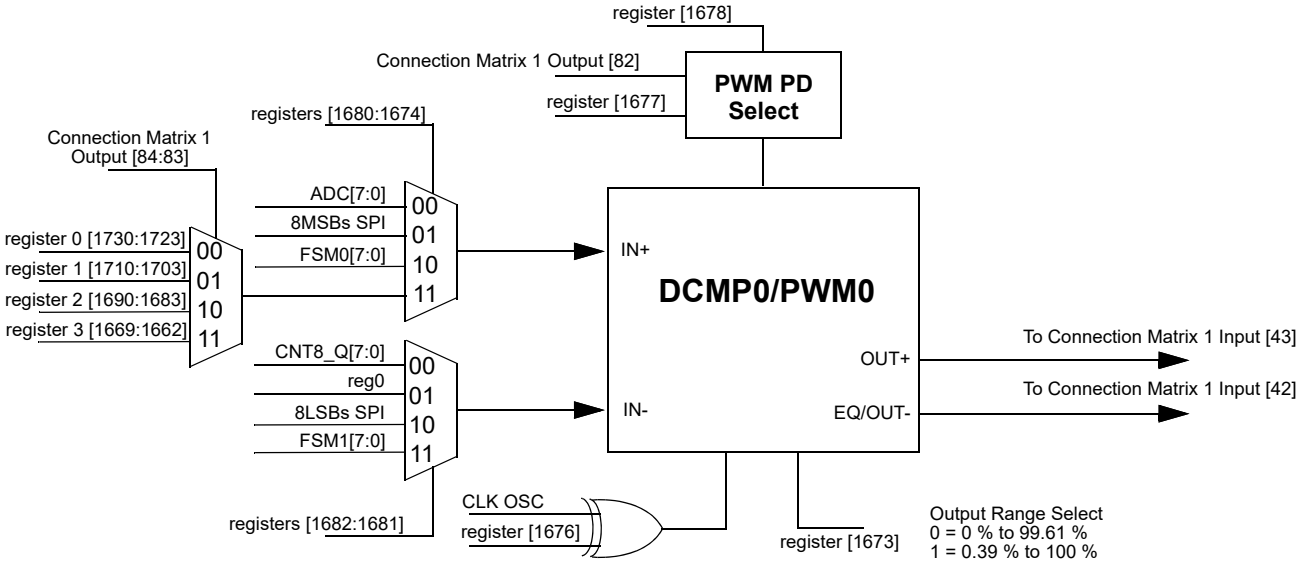


Figure 82: DCMP0/PWM0 Functional Diagram

14.6 DCMP1/PWM1 FUNCTIONAL DIAGRAM

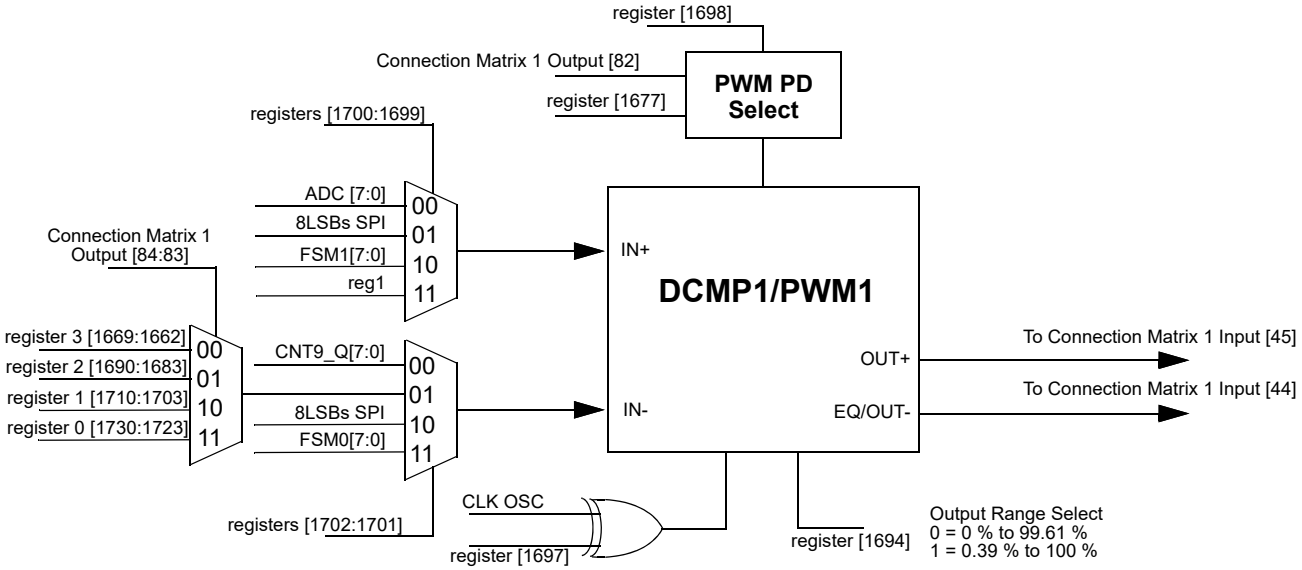


Figure 83: DCMP1/PWM1 Functional Diagram

14.7 DCMP2/PWM2 FUNCTIONAL DIAGRAM

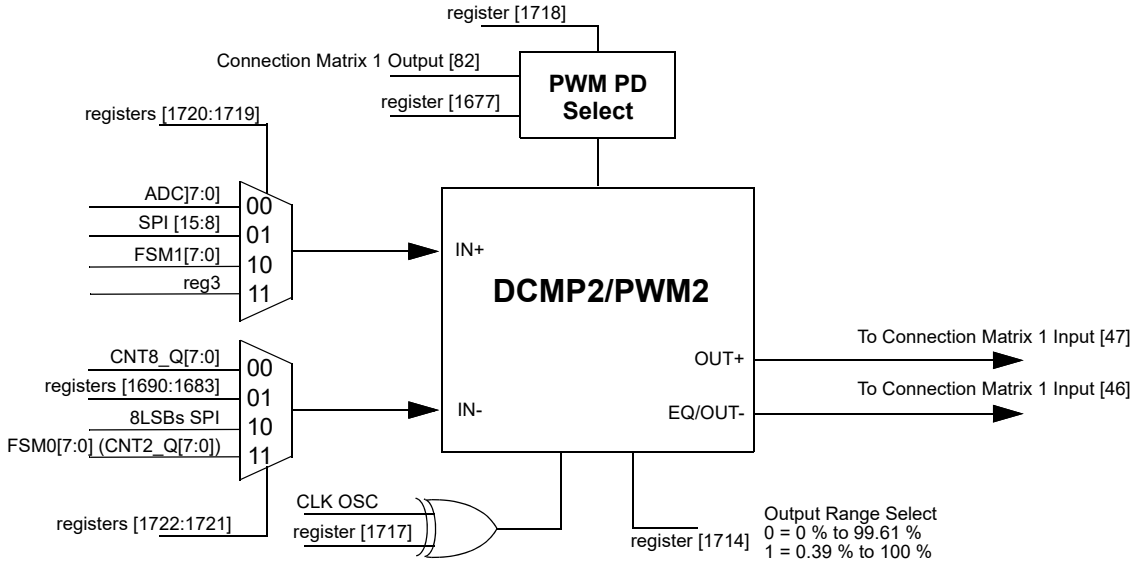


Figure 84: DCMP2/PWM2 Functional Diagram

14.8 PWM DEAD BAND CONTROL

The dead band interval can be controlled with NVM bits from PWM0 registers [1722:1720], from PWM1 registers [1693:1691], from PWM2 registers [1713:1711]. The typical dead band time starts at 8 ns and can go to 64 ns, increasing by 8 ns intervals.

For the Delay dead band control, the dead time control range is:

$$T_D = (PWM\ Register\ bits + 1) \times 8\ ns$$

14.9 PWM DEAD BAND CONTROL TIMING DIAGRAM

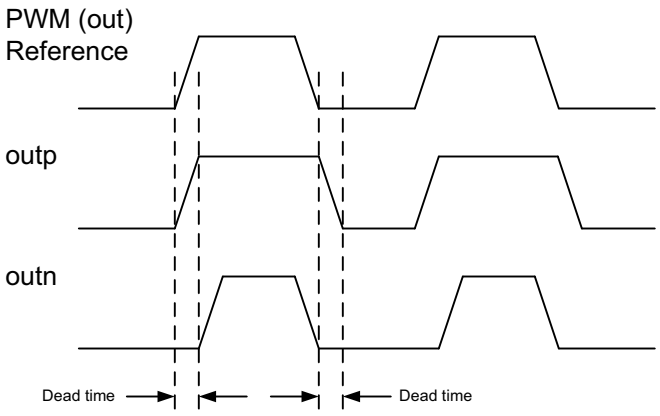


Figure 85: PWM Dead Band Control Timing Diagram

14.10 DCMP/PWM POWER-DOWN CONTROL

The power-down source for the DCMP/PWM logic cells is selected by registers [1521:1516]. The DCMP/PWM logic cells can then be turned on or off individually with the appropriate register. The power-down control of each logic cell is managed by the following register settings:

- When register [1678] = “0” DCMP0/PWM0 is powered down, when “1” logic cell is ON
- When register [1698] = “0” DCMP1/PWM1 is powered down, when “1” logic cell is ON
- When register [1718] = “0” DCMP2/PWM2 is powered down, when “1” logic cell is ON

14.11 DCMP/PWM CLOCK INVERT CONTROL

The three DCMP/PWM logic cells can invert the *CLK OSC* input signal during the compare or PWM function. Register [1676], register [1697] and register [1717] is used to control the three logic cells clock inversion for PWM0, PWM1, and PWM2 respectively.

15 Slave SPI - Serial to Parallel/Parallel to Serial Converter

The Slave (Peripheral) SPI data can be communicated between the SLG46620-A and the larger system design through either the serial to parallel or parallel to serial interface. The SPI has two 8-bit registers (2 bytes) that are used for data transfer. The external clock signal and the nCSB (Enable Control Signal) comes from the Connection Matrix OUT.

For serial to parallel operation (S2P), the serial data in (MOSI) comes from PIN 10 of the SLG46620-A. The S2P will produce a 16-bit parallel data output (S2P[15:0]) where the MSB [15:8] can be used by the PWM/DCMP0_IN+, PWM/DCMP1_IN-, PWM/DCMP2_IN+ and FSM1 logic cells, while the LSB [7:0] can be used by the PWM/DCMP0_IN-, PWM/DCMP1_IN+, PWM/DCMP2_IN- and FSM0 logic cells.

In parallel to serial mode (P2S) there is an additional configuration of the length of converted code - 8-bit and 16-bit. With 8-bit configuration the parallel data from FSM0 or ADC can be converted to serial data. PIN 10 is used to output this 8-bit serial data OUT (MISO) signal. With 16 bit configuration the parallel data from FSM0 and FSM1 can be converted into a serial code. 8 LSB bits of FSM1 data will be sent to PAR_IN[7:0] and 8-bits of FSM0 will be sent to PAR_IN[15:8]. Same as in 8-bit mode 16 bit serial data will be output to PIN 10.

15.1 SPI FUNCTIONAL DIAGRAM

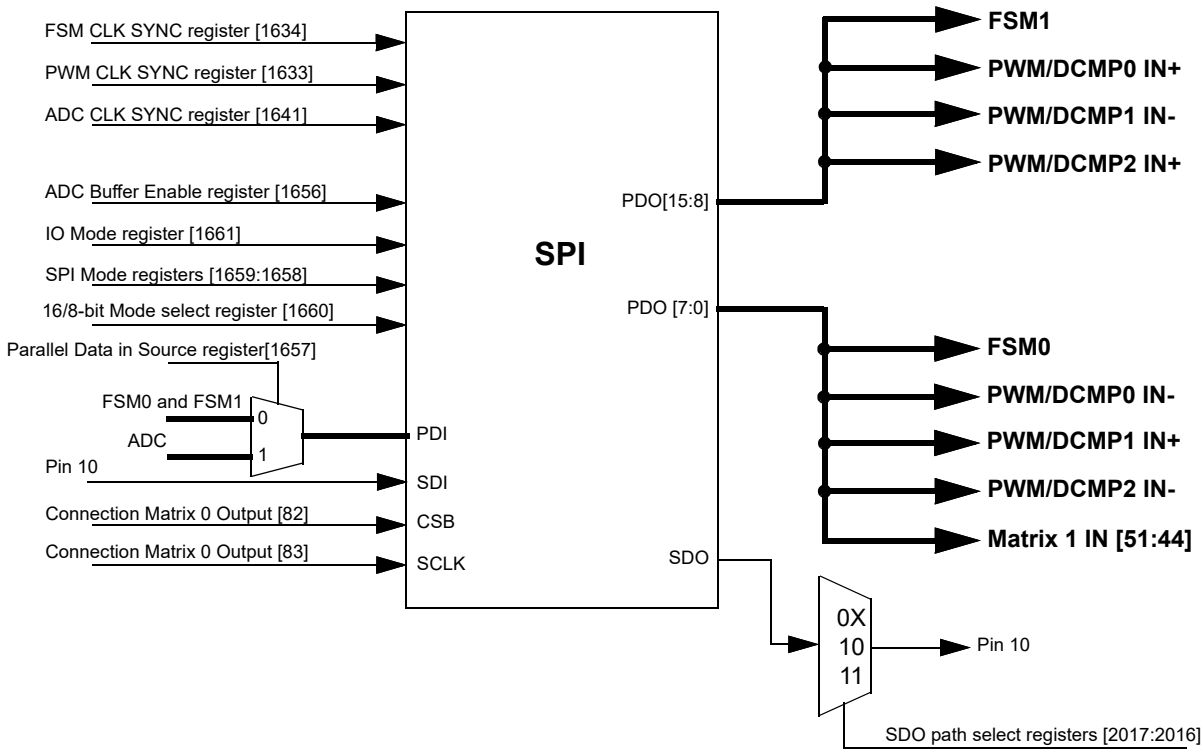


Figure 86: SPI Functional Diagram

15.2 CLOCK POLARITY AND PHASE

In addition to setting the clock frequency, it is possible to configure the clock polarity and phase with respect to the data. This is configured by the CPOL and CPHA respectively.

Figure 87 shows the SPI timing diagram when CPHA = 0; in this mode data can only be transmitted from serial to parallel, not from parallel to serial. Figure 88 shows the SPI timing diagram when CPHA = 1; in this mode data can be transmitted both from serial to parallel and from parallel to serial.

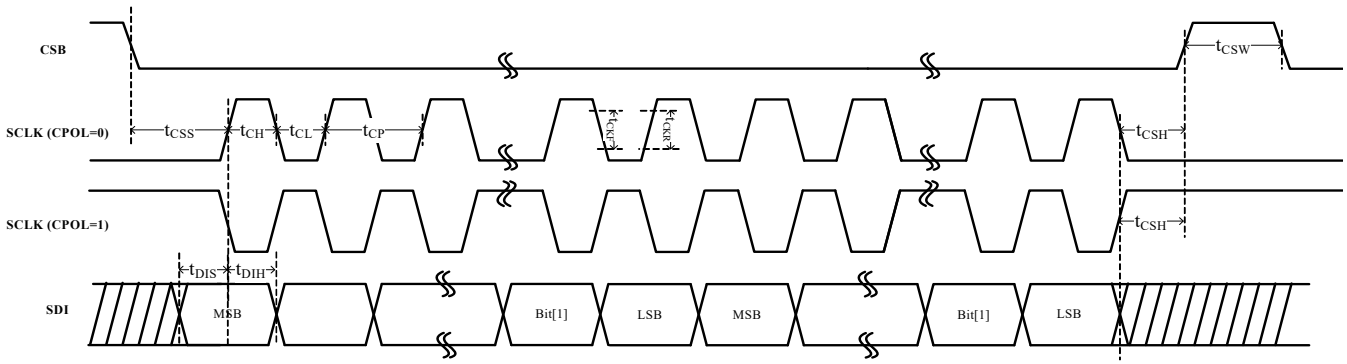


Figure 87: Timing Diagram showing Clock Polarity and Phase, CPHA = 0

Table 59: CPHA = 0 Timing Characteristics

Description	Parameter	Min	Max	Units
SCLK period	t_{CP}	500	--	ns
SCLK pulse width high	t_{CH}	250	--	ns
SCLK pulse width low	t_{CL}	250	--	ns
CSB fall to SCLK first edge setup	t_{CSS}	250	--	ns
SCLK last edge to CSB rise hold	t_{CSH}	250	--	ns
CSB pulse width high	t_{CSW}	500	--	ns
SCLK to SDI hold	t_{DIH}	100	--	ns
SCLK to SDI setup	t_{DIS}	50	--	ns
SCLK rise/fall time	t_{CKR}	--	20	ns

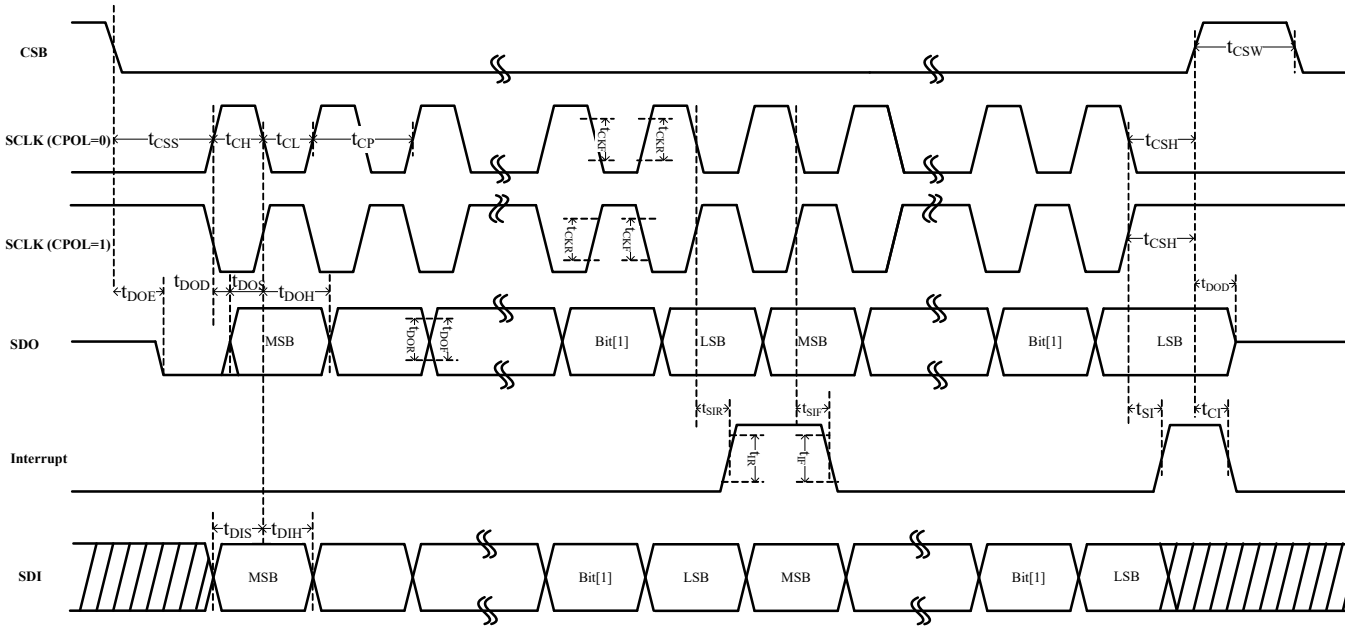


Figure 88: Timing Diagram showing Clock Polarity and Phase, CPHA = 1

Table 60: CPHA = 1 Timing Characteristics

Description	Parameter	Min	Max	Units
SCLK period	t_{CP}	500	--	ns
SCLK pulse width high	t_{CH}	250	--	ns
SCLK pulse width low	t_{CL}	250	--	ns
CSB fall to SCLK first edge setup	t_{CSS}	250	--	ns
SCLK last edge to CSB rise hold	t_{CSH}	250	--	ns
SCLK to SDO hold	t_{DOH}	100	--	ns
SCLK to SDO setup	t_{DOS}	100	--	ns
SCLK to SDO delay	t_{DOD}	--	150 **(Note 1)**	ns
CSB rise to SDO disable	t_{DOD}	5	150 **(Note 1)**	ns
CSB fall to SDO enable	t_{DOE}	5	150 **(Note 1)**	ns
CSB pulse width high	t_{CSW}	500	--	ns
LSB' SCLK fall to Interrupt high	t_{SIR}	5	150 **(Note 1)**	ns
MSB' SCLK fall to Interrupt low	t_{CIF}	5	150 **(Note 1)**	ns
SCLK to Interrupt high	t_{SI}	5	150 **(Note 1)**	ns
CSB rise to Interrupt low	t_{CI}	5	150 **(Note 1)**	ns
SCLK to SDI hold	t_{DIH}	100	--	ns
SCLK to SDI setup	t_{DIS}	50	--	ns
SCLK rise/fall time	t_{CKR}/t_{CKF}	--	20	ns
SDO rise/fall time	t_{DOR}/t_{DOF}	--	20*	ns

Table 60: CPHA = 1 Timing Characteristics (Continued)

Description	Parameter	Min	Max	Units
Interrupt rise/fall time	t_{IR}/t_{IF}	--	20*	ns
Note 1 The data is based on 50 pF loading on the output PIN, and the output drive strength is 2x option.				

- At CPOL = 0 the base value of the clock is zero
  - For CPHA = 0, data are captured on the clock's rising edge (LOW→HIGH transition) and data is propagated on a falling edge (HIGH→LOW clock transition)
  - For CPHA = 1, data are captured on the clock's falling edge and data is propagated on a rising edge
- At CPOL = 1 the base value of the clock is one (inversion of CPOL = 0)
  - For CPHA = 0, data are captured on clock's falling edge and data is propagated on a rising edge
  - For CPHA = 1, data are captured on clock's rising edge and data is propagated on a falling edge

That is, CPHA = 0 means sample on the leading (first) clock edge, while CPHA = 1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. Note that with CPHA = 0, the data must be stable for a half cycle before the first clock cycle.

The MOSI and MISO signals are usually stable (at their reception points) for the half cycle until the next clock transition. SPI master and slave devices may well sample data at different points in that half cycle.

This adds more flexibility to the communication channel between the master and slave.

15.3 SPI CLOCK SYNCHRONIZATION

When the parallel data is going to be loaded into the buffer in SPI, the SPI will generate the "sync" signal, it will be gating the ADC/PWM CLOCK or FSM CLOCK/256 to stop the running ADC, PWM, FSM or CNTs to avoid mis-catch data due to the asynchronization of SCLK and the internal clocks, see Figure 79.

Note: The internal clock and SPI clock must satisfy the: 2TCLK_INT<1/2TSCK.

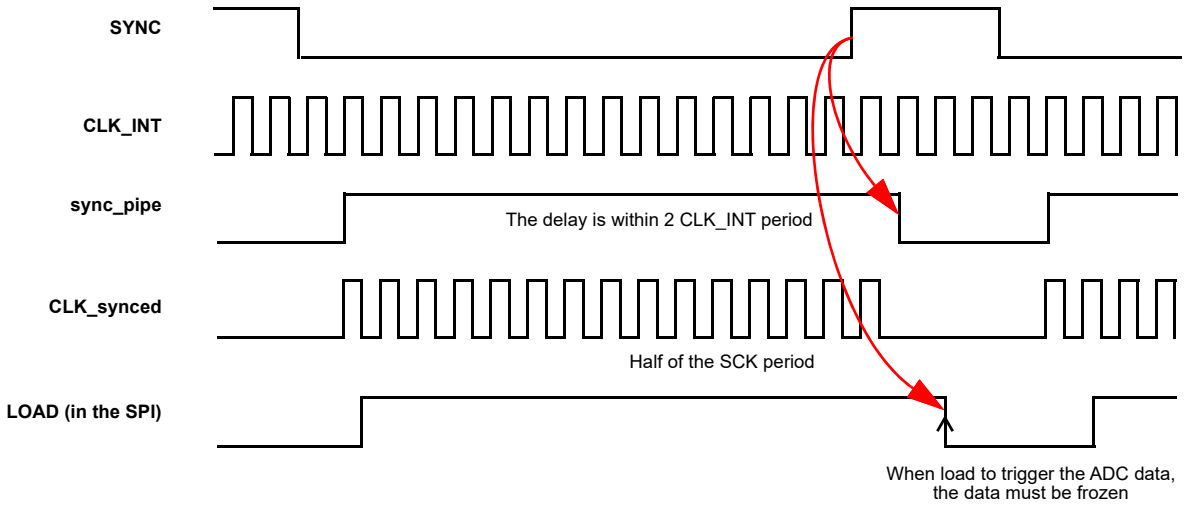


Figure 89: Timing Diagram showing SPI Clock synchronization

15.4 SPI DATA BUFFER FUNCTION

SPI data buffer can be used to have DCMP compare two different ADC timing data. The ADC buffer is shared with the DFFs that are in the SPI macrocell. When the SPI is set to ADC buffer mode (register [1656] = 1), the DFF 's data inputs of SPI's parallel outputs are from ADC and the DFF's clock source comes from matrix0_output83 which can be programmed by user. The DFF's output (SPI[7:0]) is the ADC data's buffered output which can be sent to DCMP/PWMs or FSM (CNT)s.

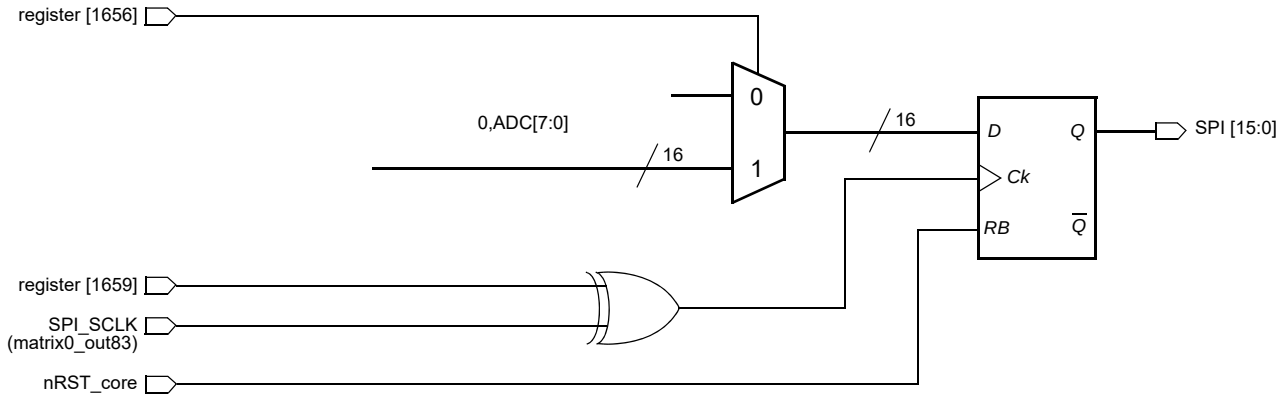


Figure 90: The SPI used as ADC data buffer diagram

16 Pipe Delay

The SLG46620-A has two 16-stages DFF Pipe Delay (PD) Macrocells.

Each Pipe Delay has three input signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide two delay options which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input MUX that is controlled by register bits. The 4-input MUX is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46620-A design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or any Oscillator within the SLG46620-A). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

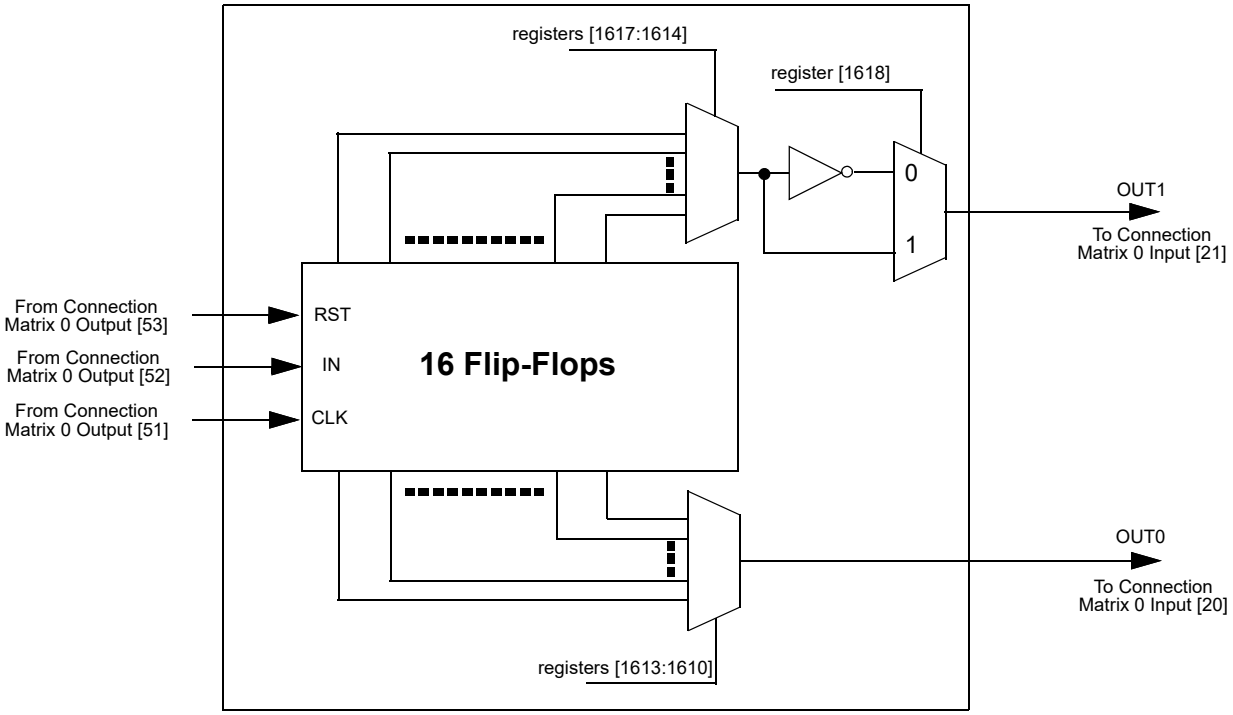


Figure 91: Pipe Delay 0

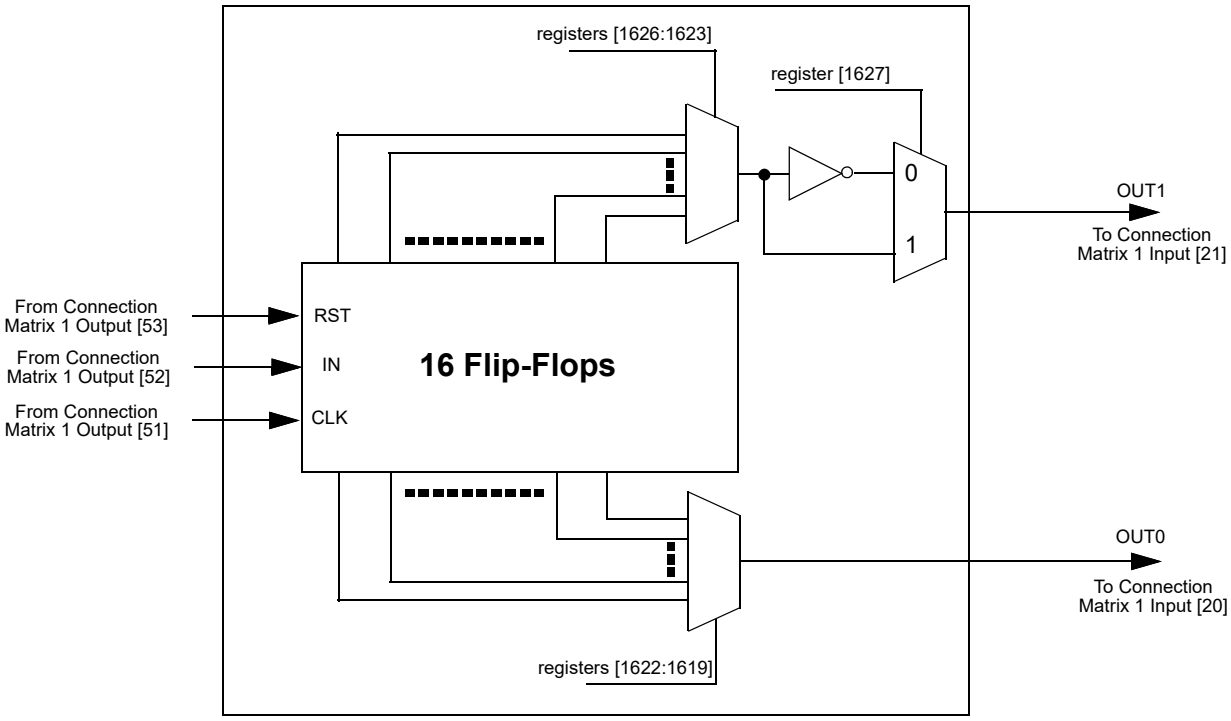


Figure 92: Pipe Delay 1

17 Programmable Delay/Edge Detector

The SLG46620-A has two programmable time delay logic cells available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cells can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. Three of these patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. Note that, delayed edge detection function is not available for both edge delay pattern. See the timing diagrams below for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

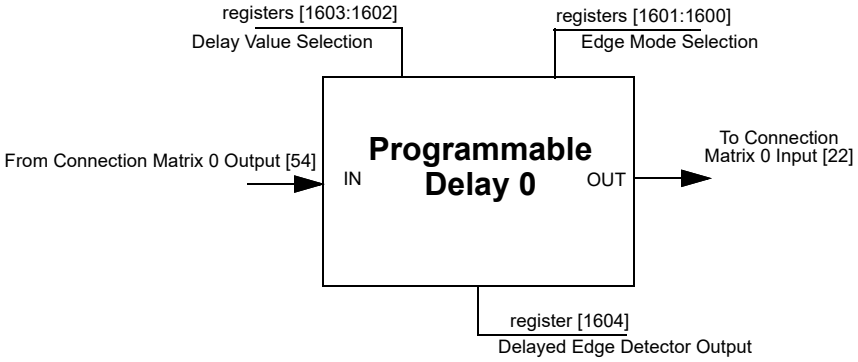


Figure 93: Programmable Delay

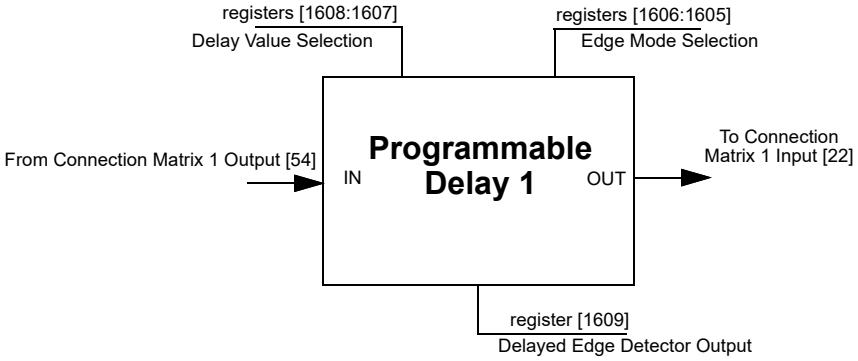
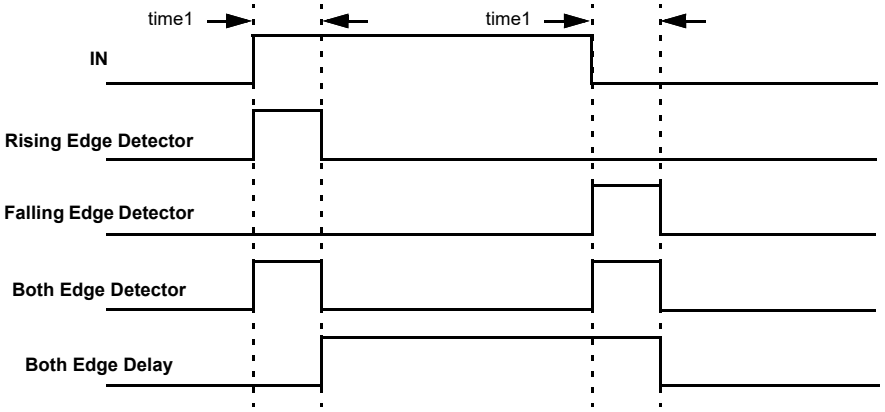


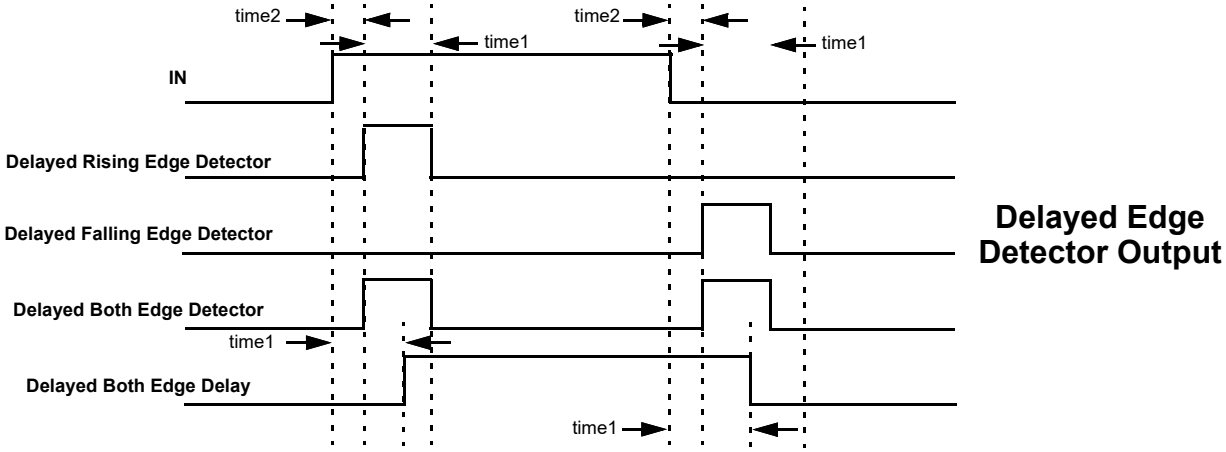
Figure 94: Programmable Delay

17.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT



time1 can be set by register value, see Table 10

Figure 95: Edge Detector Output



time1 can be set by register value (150 ns, 300 ns, 450 ns, 600 ns)
time2 is a fixed value at ~200 ns

Figure 96: Delayed Edge Detector Output

17.2 PROGRAMMABLE DELAY TIMING DIAGRAM - GLITCH FILTERING FOR EDGE DETECTOR OUTPUT

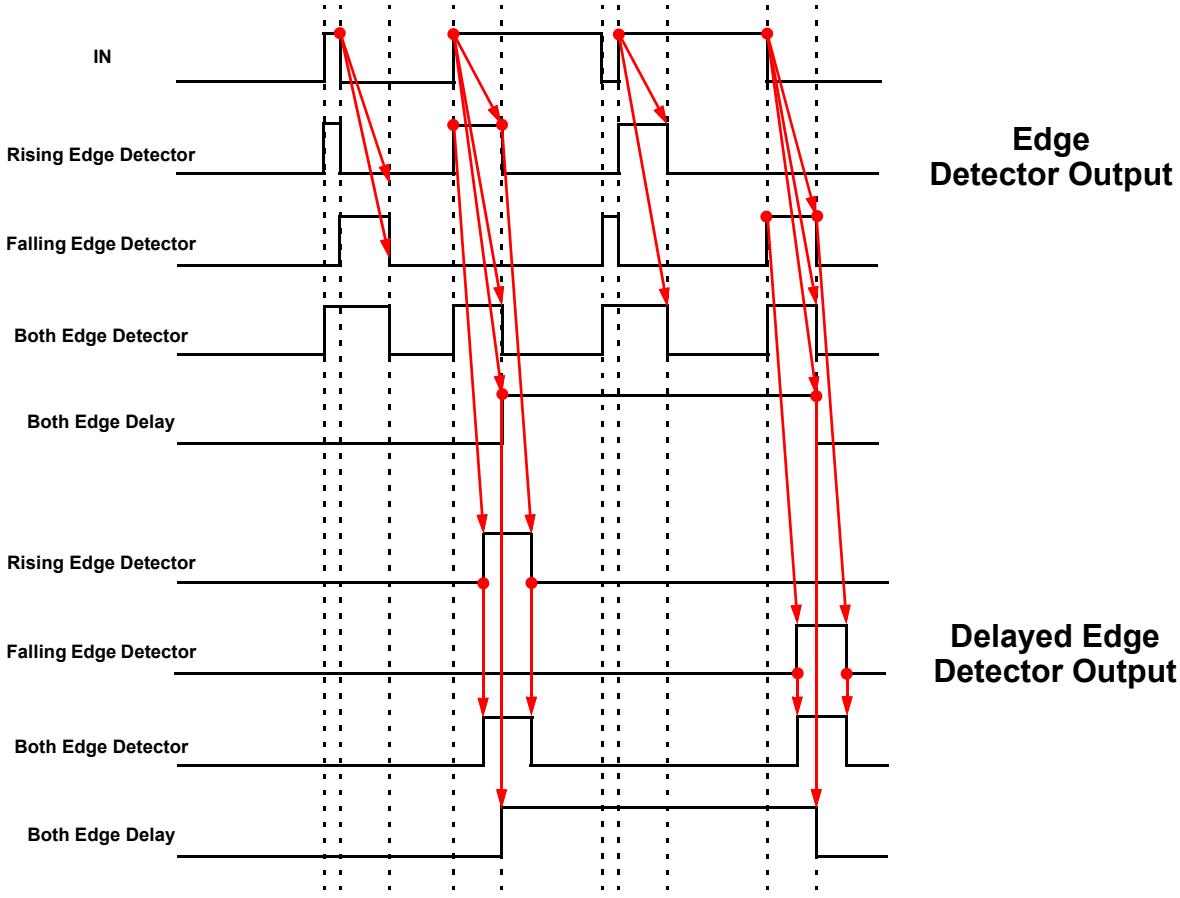


Figure 97: Glitch Filtering for Edge Detector Output

18 Voltage Reference

18.1 VOLTAGE REFERENCE OVERVIEW

The SLG46620-A has a Voltage Reference Macrocell to provide references to the six analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from pins 5, 7,10 and 14. The macrocell also has the option to output reference voltages on pins 18 and 19. See table below for the available selections for each analog comparator. Also see Figure 98 below, which shows the reference output structure.

18.2 VREF SELECTION TABLE

Table 61: Vref Selection Table

registers acmpxref_sel [4:0]	ACMP0_Vref	ACMP1_Vref	ACMP2_Vref	ACMP3_Vref	ACMP4_Vref	ACMP5_Vref
11111	DAC0_OUT	DAC0_OUT	DAC0_OUT	DAC0_OUT	DAC0_OUT	DAC0_OUT
11110	DAC1_OUT	DAC1_OUT	DAC1_OUT	DAC1_OUT	DAC1_OUT	DAC1_OUT
11101	Vref_ext_acmp0 / 2	Vref_ext_acmp0 / 2	Vref_ext_acmp2 / 2	Vref_ext_acmp2 / 2	Vref_ext_acmp2 / 2	Vref_ext_acmp5 / 2
11100	Vref_ext_acmp1 / 2	Vref_ext_acmp1 / 2	Vref_ext_acmp1 / 2	Vref_ext_acmp1 / 2	Vref_ext_acmp1 / 2	Vref_ext_acmp1 / 2
11011	Vref_ext_acmp0	Vref_ext_acmp0	Vref_ext_acmp2	Vref_ext_acmp2	Vref_ext_acmp2	Vref_ext_acmp5
11010	Vref_ext_acmp1	Vref_ext_acmp1	Vref_ext_acmp1	Vref_ext_acmp1	Vref_ext_acmp1	Vref_ext_acmp1
11001	V_{DD}/4	V_{DD}/4	V_{DD}/4	V_{DD}/4	V_{DD}/4	V_{DD}/4
11000	V_{DD}/3	V_{DD}/3	V_{DD}/3	V_{DD}/3	V_{DD}/3	V_{DD}/3
10111	1.20	1.20	1.20	1.20	1.20	1.20
10110	1.15	1.15	1.15	1.15	1.15	1.15
10101	1.10	1.10	1.10	1.10	1.10	1.10
10100	1.05	1.05	1.05	1.05	1.05	1.05
10011	1.00	1.00	1.00	1.00	1.00	1.00
10010	0.95	0.95	0.95	0.95	0.95	0.95
10001	0.90	0.90	0.90	0.90	0.90	0.90
10000	0.85	0.85	0.85	0.85	0.85	0.85
01111	0.80	0.80	0.80	0.80	0.80	0.80
01110	0.75	0.75	0.75	0.75	0.75	0.75
01101	0.70	0.70	0.70	0.70	0.70	0.70
01100	0.65	0.65	0.65	0.65	0.65	0.65
01011	0.60	0.60	0.60	0.60	0.60	0.60
01010	0.55	0.55	0.55	0.55	0.55	0.55
01001	0.50	0.50	0.50	0.50	0.50	0.50
01000	0.45	0.45	0.45	0.45	0.45	0.45
00111	0.40	0.40	0.40	0.40	0.40	0.40
00110	0.35	0.35	0.35	0.35	0.35	0.35
00101	0.30	0.30	0.30	0.30	0.30	0.30
00100	0.25	0.25	0.25	0.25	0.25	0.25
00011	0.20	0.20	0.20	0.20	0.20	0.20
00010	0.15	0.15	0.15	0.15	0.15	0.15

Table 61: Vref Selection Table (Continued)

registers acmpxref_sel [4:0]	ACMP0_Vref	ACMP1_Vref	ACMP2_Vref	ACMP3_Vref	ACMP4_Vref	ACMP5_Vref
00001	0.10	0.10	0.10	0.10	0.10	0.10
00000	0.05	0.05	0.05	0.05	0.05	0.05

Table 62: Vref Range

V_{DD}	Practical Vref Range	Note
2.0 V - 3.6 V	50 mV ~ 1.2 V	
1.7 V - 2.0 V	50 mV ~ 1.0 V	Do not operate above 1.0 V

18.3 VREF BLOCK DIAGRAM

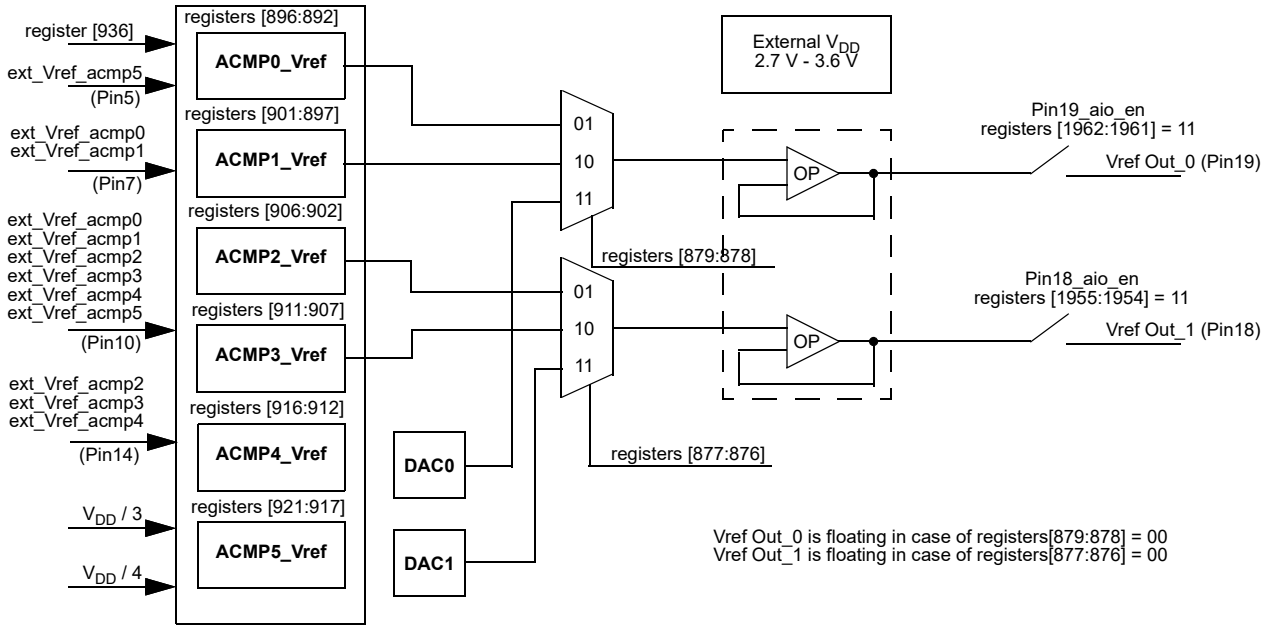


Figure 98: Voltage Reference Block Diagram

18.4 VREF OUT TYPICAL PERFORMANCE

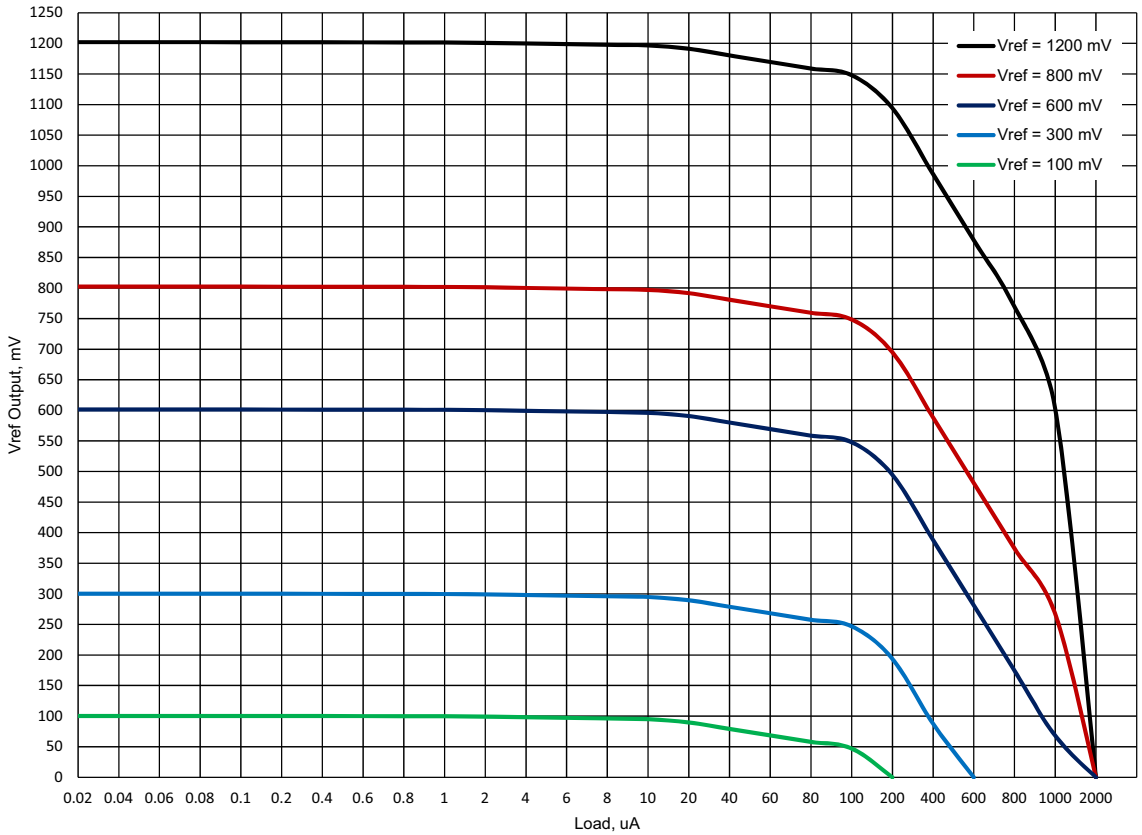


Figure 99: Typical Load Regulation, T_A = 25 °C, V_{DD} = 3.3 V

19 Clocking

19.1 OSCILLATORS GENERAL DESCRIPTION

The SLG46620-A has three internal RC oscillators (25 kHz or 2 MHz, user selectable), as well as one Low-Frequency oscillator (1.73 kHz) and one Ring oscillator (27 MHz).

There are two divider stages for the RC and Ring oscillators, one divider stage for the Low-Frequency oscillator, that gives the user flexibility for introducing clock signals to connection matrix 0 and 1, as well as various other Macrocells. The pre-divider (first stage) for RC Oscillator allows the selection of /1, /2, /4 or /8, for LF OSC - /1, /2, /4 or /16 and for Ring OSC - /1, /4, /8 or /16 to divide down frequency from the fundamental. The second stage divider (does not apply for LF OSC) has an input of frequency from the pre-divider, and outputs one of eight different frequencies on Connection Matrix Input lines [49] and [48]. The output of LF OSC Pre-divider goes directly on Connection Matrix Input line [50]. Please see Figure 87, for more details on the SLG46620-A clock scheme.

The Matrix Power-down function allows to switch on/off the oscillators using an external pin (register [1648] for 25 kHz / 2 MHz OSC, register [1652] for LF OSC and register [1638] for Ring OSC):

- **Enable [1]**. If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off.
- **Disable [0]**. Turns off the Matrix Power-down function.

The PWR CONTROL signal has the highest priority.

The user can select two OSC POWER MODEs (register [1649] for 25 kHz / 2 MHz OSC, register [1653] for LF OSC and register [1640] for Ring OSC):

- **If FORCE POWER-ON [1]** is selected, the OSC will run when the SLG46620-A is powered on.
- **If AUTO POWER-ON [0]** is selected, the OSC will run only when any macrocell that uses OSC is powered on.

OSC can be turned on by:

- Register control (force power-on)
- Delay mode, when delay requires OSC
- ADC
- PWM/DCMP

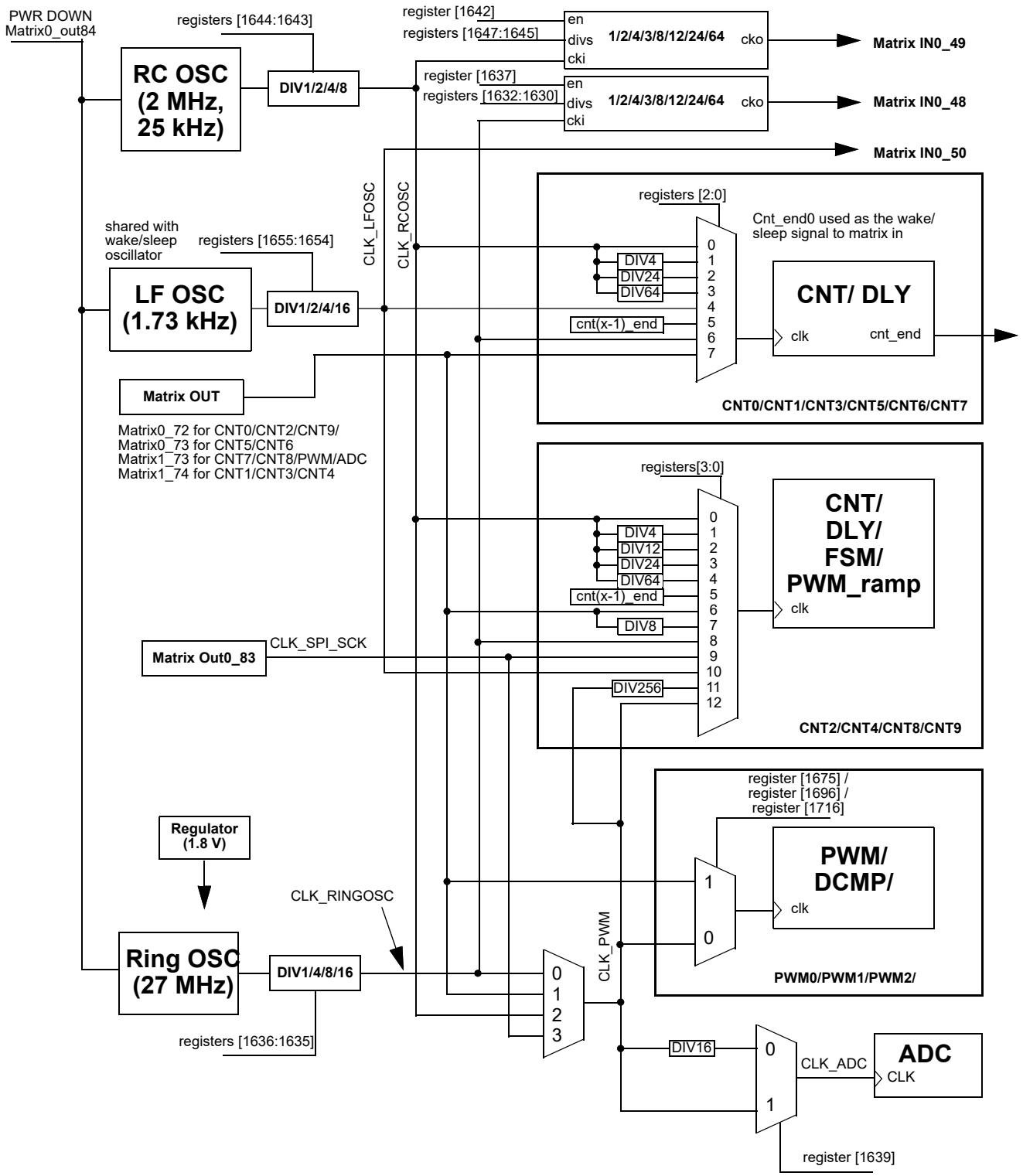


Figure 100: Oscillator Block Diagram

19.2 OSCILLATORS POWER-ON DELAY

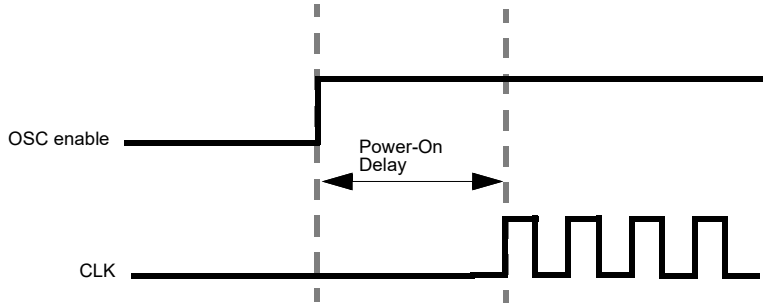


Figure 101: Oscillator Startup Diagram

Note 1 OSC power mode: “Auto Power-On”.

Note 2 “OSC Enable” signal appears when any macrocell that uses OSC is powered on.

Note 3 Calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

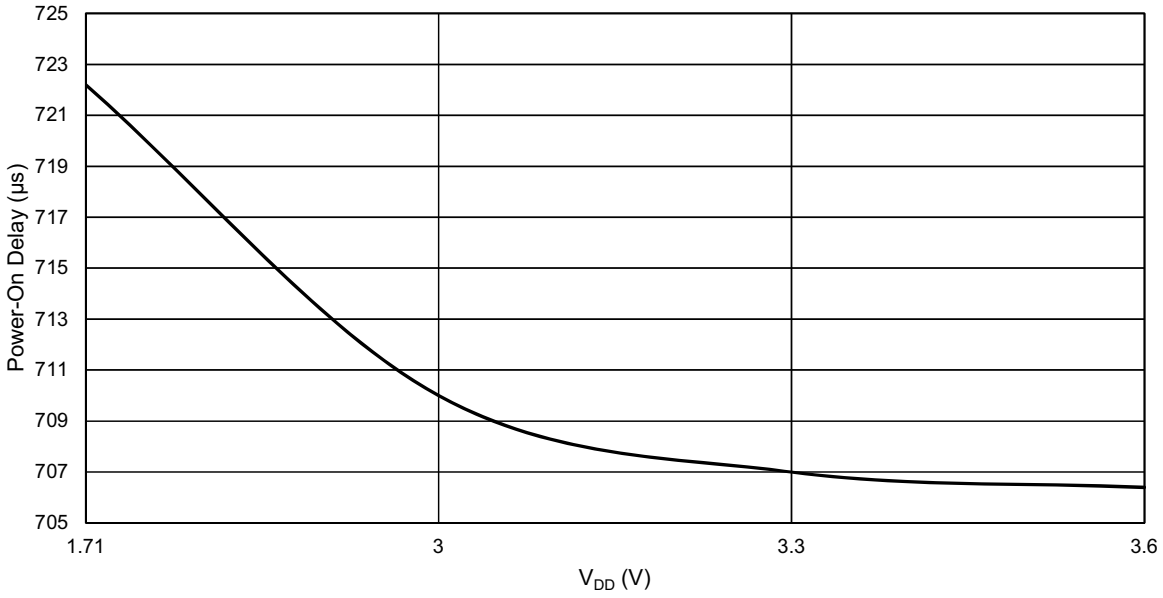


Figure 102: LF Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC = 1.73 kHz

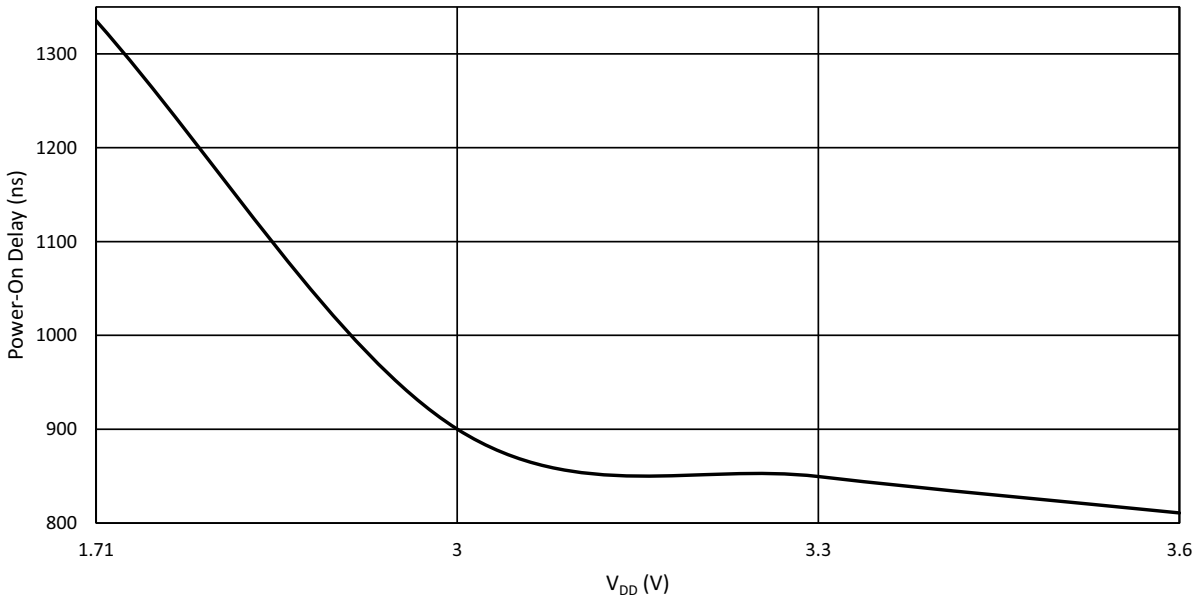


Figure 103: RC Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, RC OSC = 2 MHz

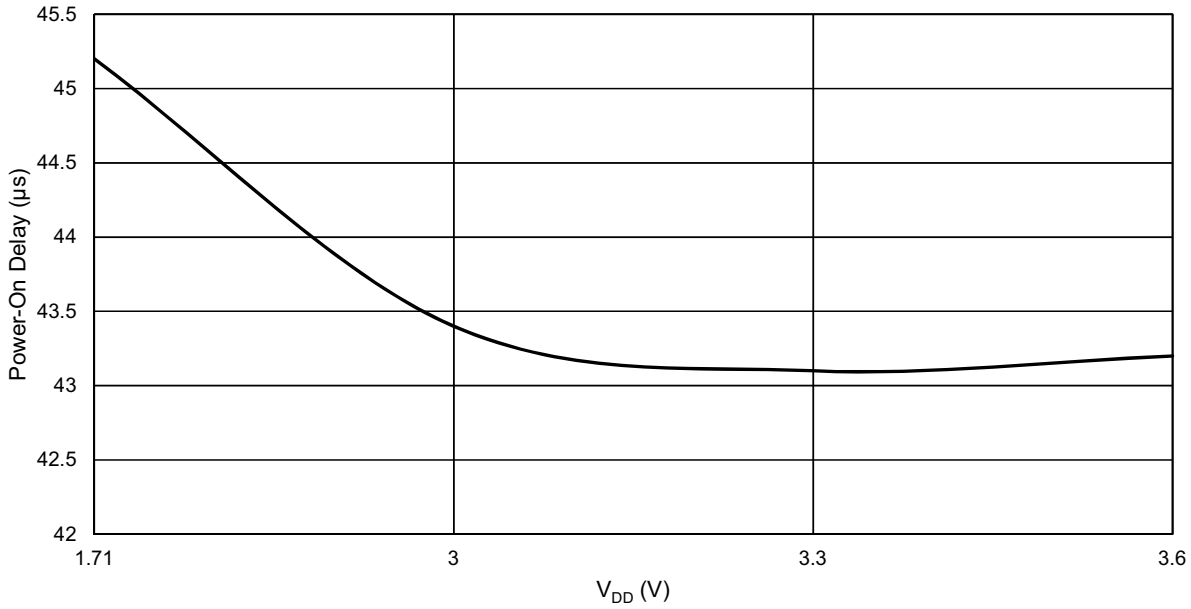


Figure 104: RC Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, RC OSC = 25 kHz

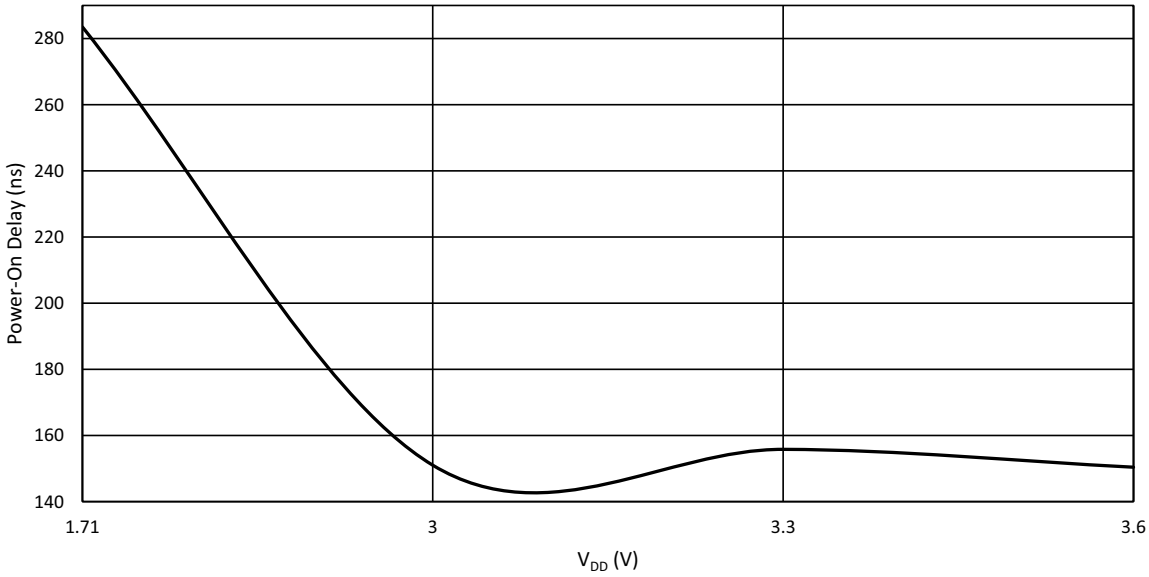


Figure 105: Ring Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC = 27 MHz

19.3 OSCILLATORS ACCURACY

Note calculations based on HTOL drift data obtained through AEC-Q100 stress tests.

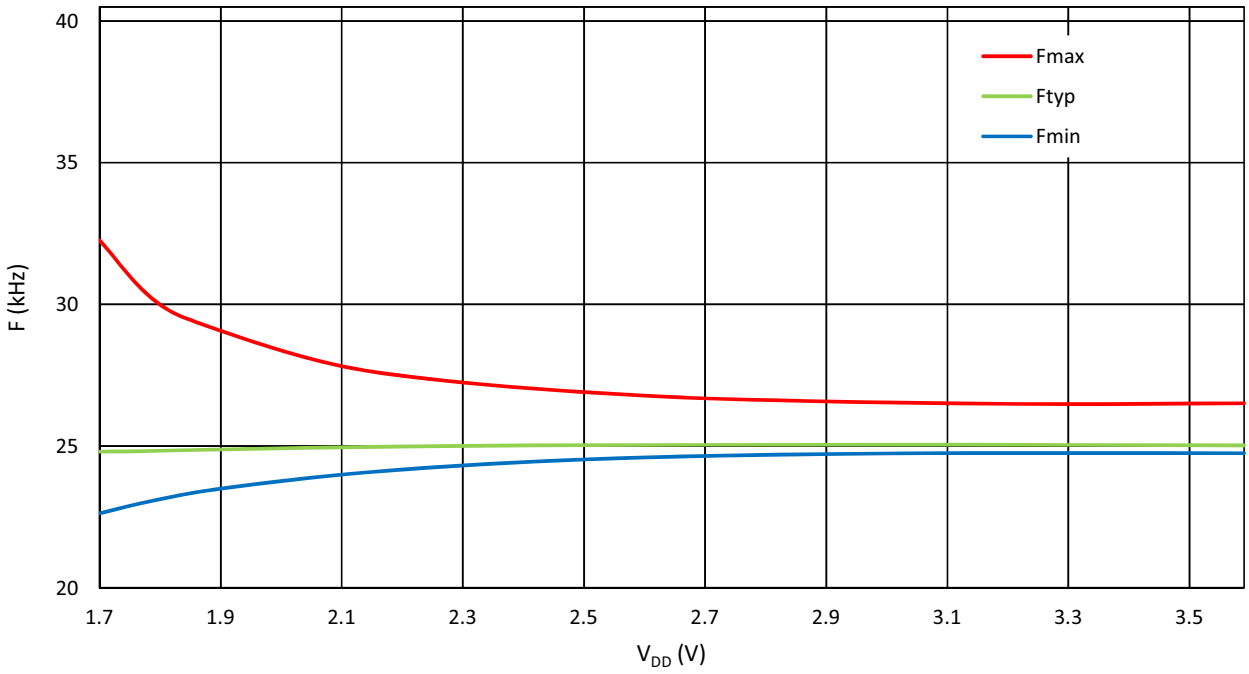


Figure 106: RC Oscillator Frequency vs. V_{DD}, RC OSC = 25 kHz, T_A = 25 °C

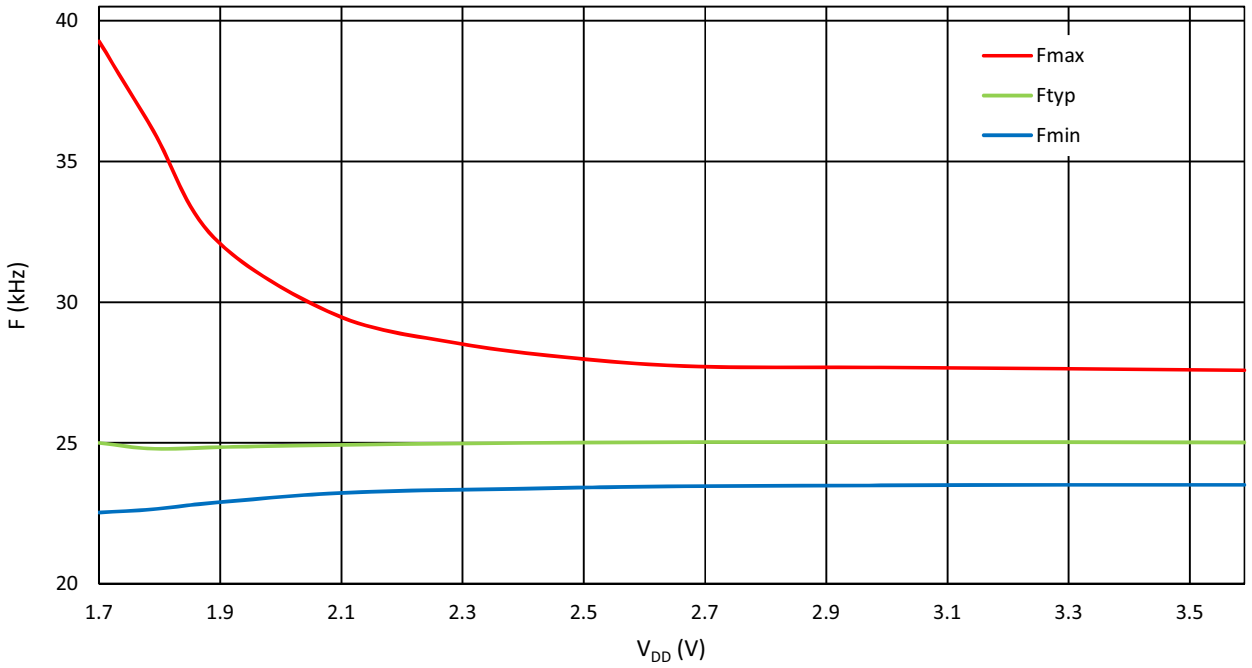


Figure 107: RC Oscillator Frequency vs. V_{DD}, RC OSC = 25 kHz, T_A = -40 °C to 105 °C

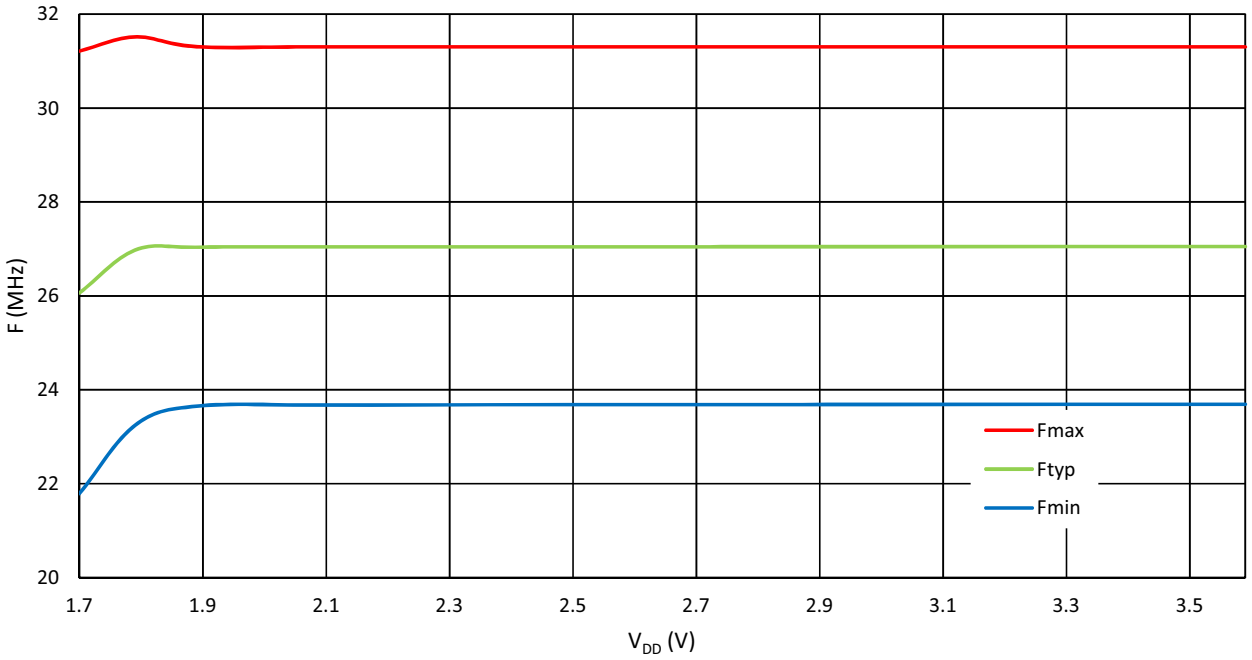


Figure 108: Ring Oscillator Frequency vs. V_{DD}, OSC = 27 MHz, T_A = 25 °C

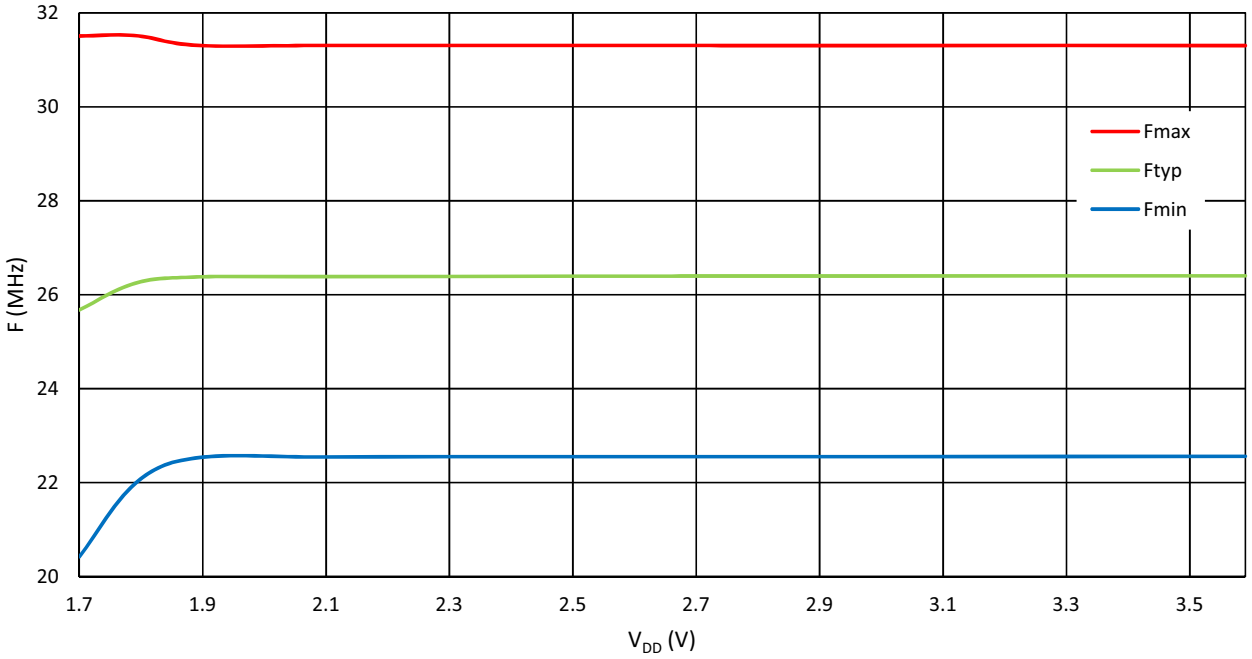


Figure 109: Ring Oscillator Frequency vs. V_{DD}, OSC = 27 MHz, T_A = -40 °C to 105 °C

20 Power-On Reset

The SLG46620-A has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

20.1 GENERAL OPERATION

The SLG46620-A is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1) is less than Power-Off Threshold (see in section 3.4), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46620-A, the voltage applied on the V_{DD} should be higher than the Power_ON threshold **(Note 1)**. The full operational V_{DD} range for the SLG46620-A is 1.71 V – 3.6 V (1.8 V ±5 % - 3.3 V±10 %). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46620-A will have a typical period of time to go through all the steps in the sequence (see Figure 96 and Figure 97), and will be ready and completely operational after the POR sequence is complete.

Note 1: The Power_ON threshold is defined in section 3.4.
Note 2: V_{DD} ramp rising speed must be less than 0.6 V/µs after power-on. Violating this specification may cause chip to restart.

To power-down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

20.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 110.

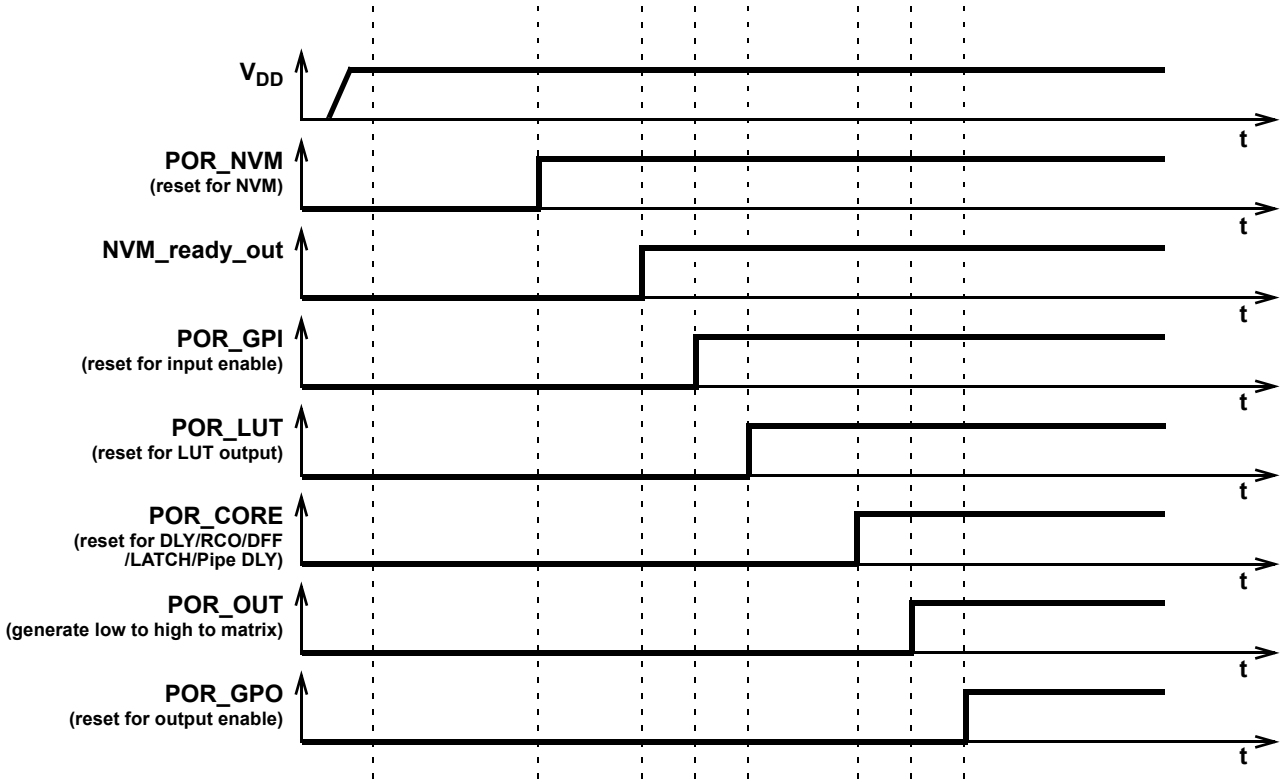


Figure 110: POR sequence

As can be seen from Figure 110 after the V_{DD} has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature and even will vary from chip to chip (process influence).

20.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46620-A operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 111 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

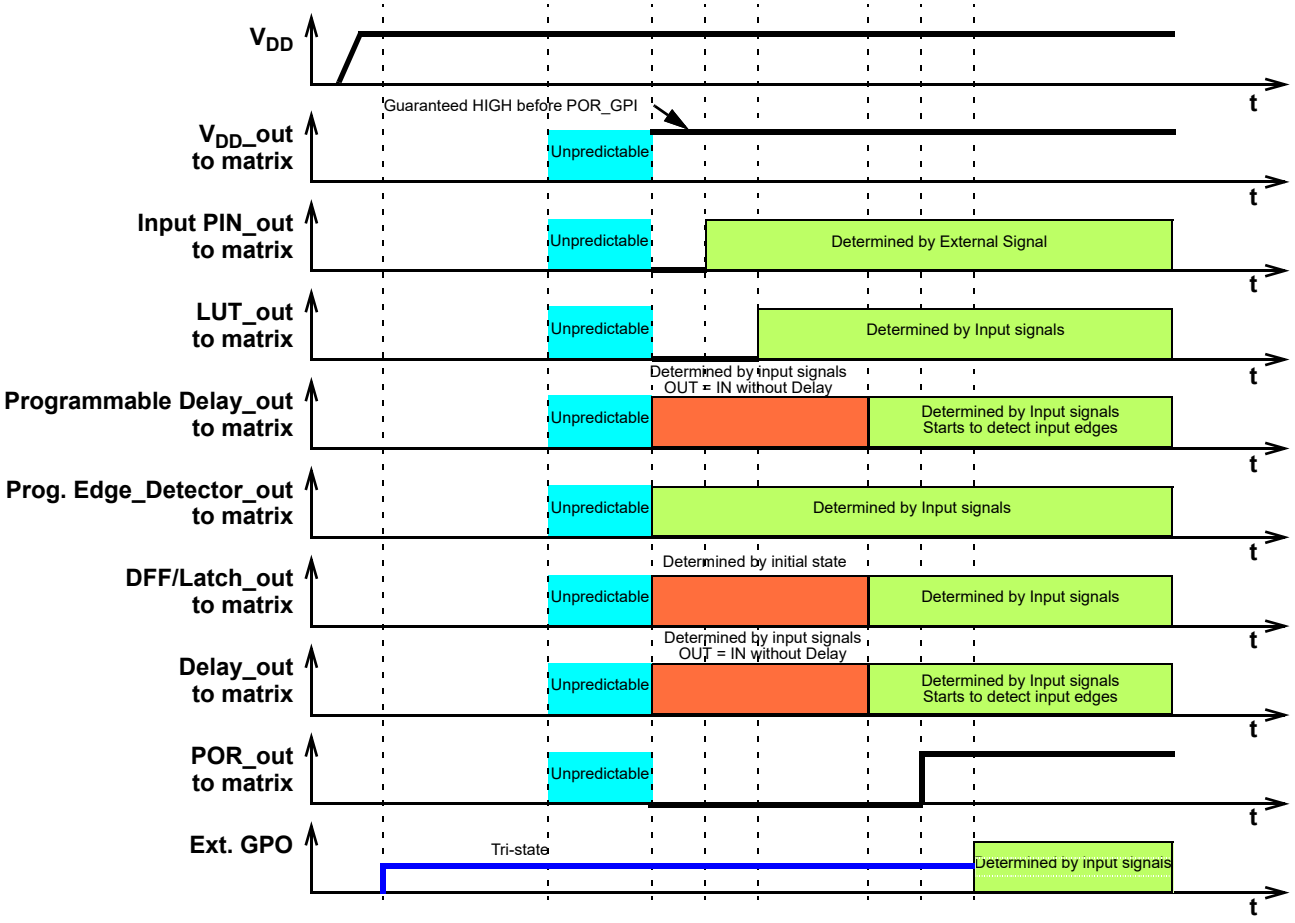


Figure 111: Internal Macrocell States during POR sequence

20.4 INITIALIZATION

All internal macrocells by default have initial low level. Starting from indicated powerup time of 0.92 V - 1.70 V, macrocells in SLG46620-A are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. So if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

20.5 POWER-DOWN

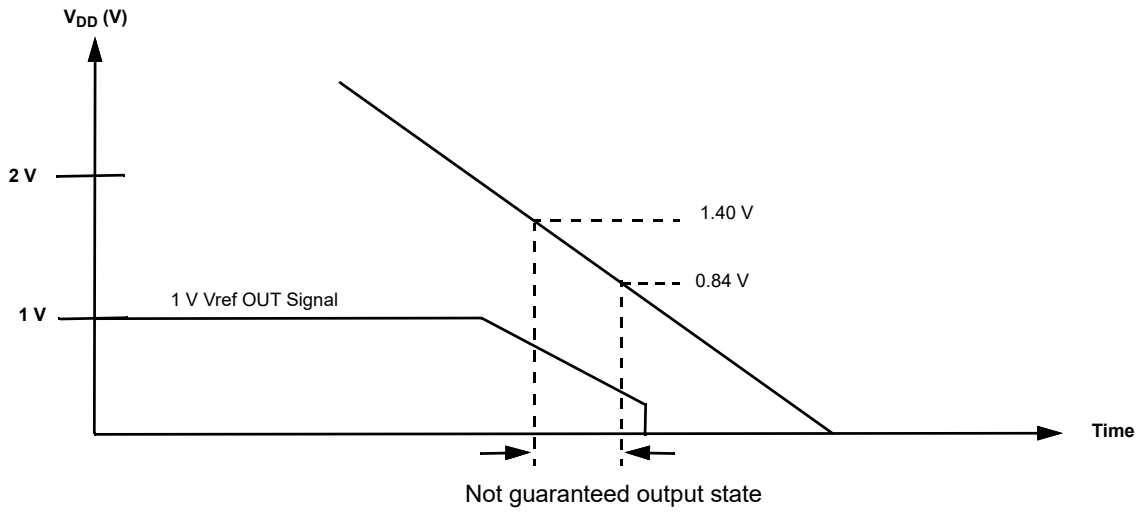


Figure 112: Power-Down

During powerdown, macrocells in SLG46620-A are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

20.6 EXTERNAL RESET

The SLG46620-A has an optional External Reset function on Pin2. It allows to reset the chip while powered on.

Pin2 must be configured as Digital Input registers [942:941] and function Reset must be enabled also, register [2020]: 0 - disabled, 1 - enabled. Unlike POR, External Reset affects only GPI, LUTs, DLY, RC OSC, DFFs, Latchs, Pipe Delay, Matrix and GPO. While NVM remains its previous state, see Figure 113 to Figure 115.

Note: External Reset affects Pipe Delay only if its nRST is connected to POR.

Note that during External Reset the output pin's status will depend on the OE control circuits and current consumption is determined by the design.

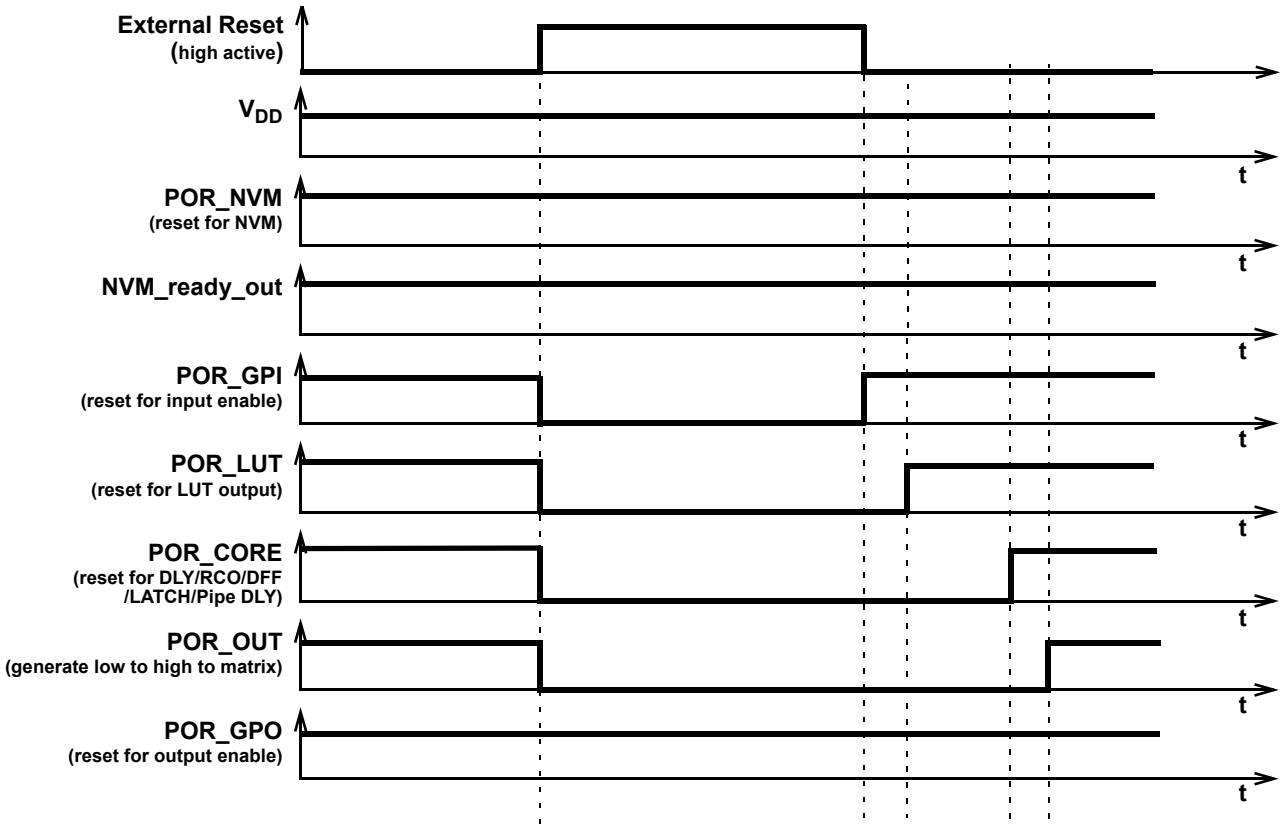


Figure 113: External Reset Sequence (High Active)

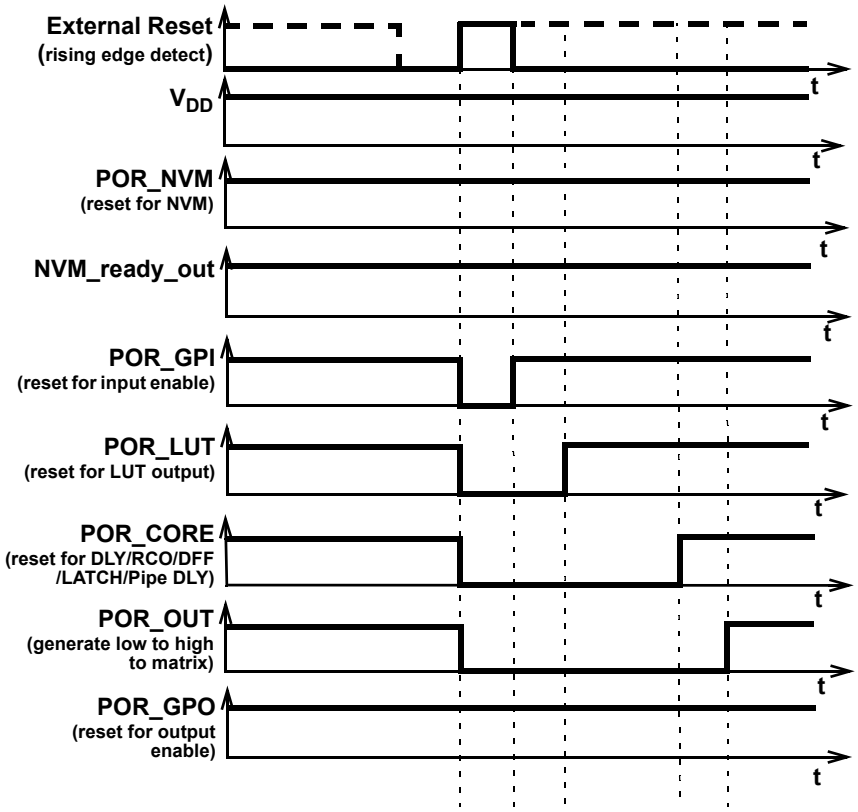


Figure 114: External Reset Sequence (Rising Edge Detect)

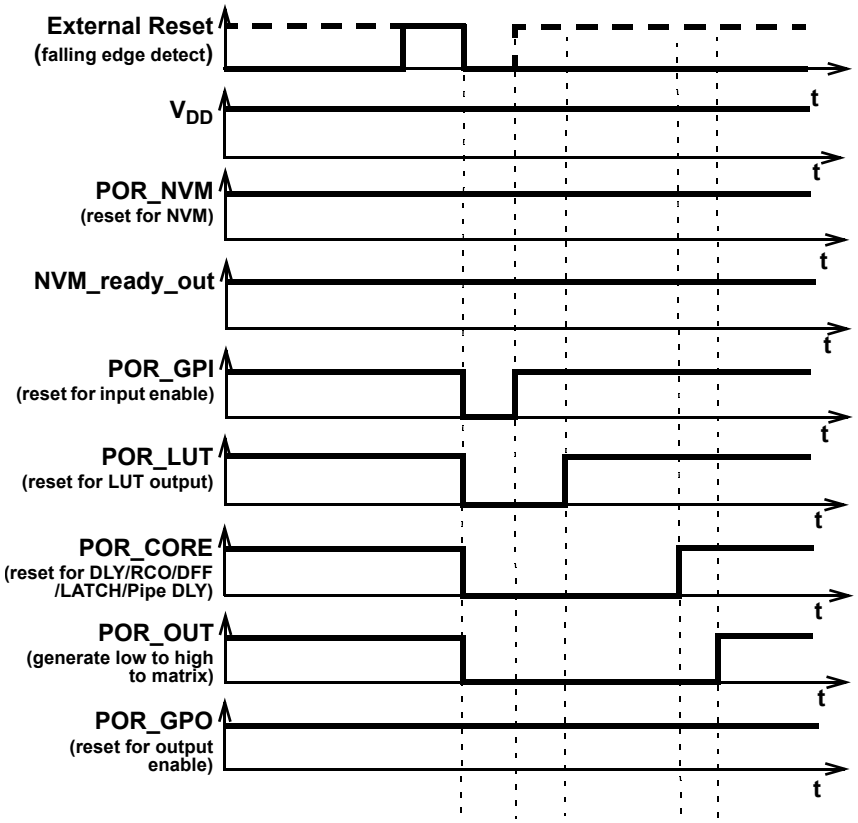


Figure 115: External Reset Sequence (Falling Edge Detect)

21 Power Detector

The Power Detect (PWR DET) is used to monitor the state of the internal Charge Pump regulator. The macrocell only has one output (OUT). The PWR DET output is HIGH when V_{DD} < 2.7V and LOW when V_{DD} > 2.7V. In order to use the macrocell register[2010] must be set to 0.

22 Additional Logic Functions

The SLG46620-A has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two inverters which can switch the polarity of any Connection Matrix signal.

22.1 INV_0 GATE

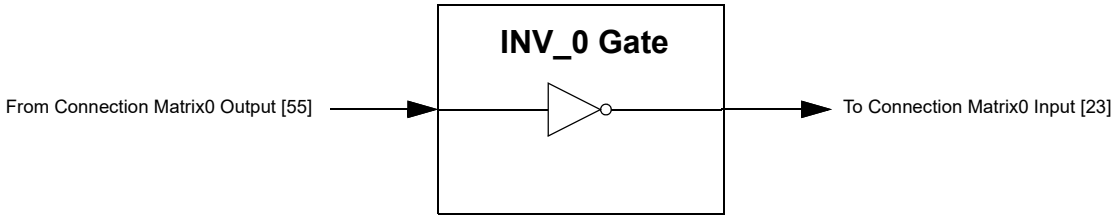


Figure 116: INV_0 Gate

22.2 INV_1 GATE

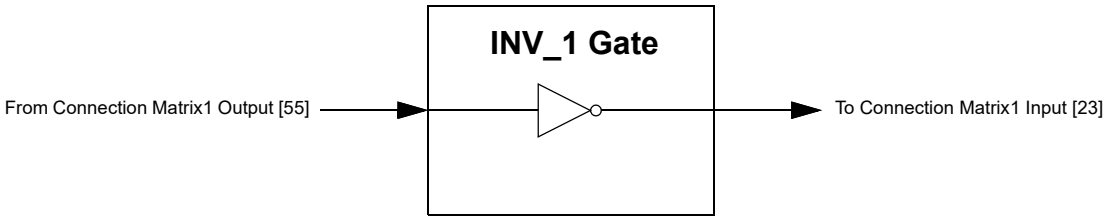


Figure 117: INV_1 Gate

23 Register Definitions

23.1 REGISTER MAP

Table 63: Register Map

Register Bit Address	Signal Function	Register Bit Definition
5:0	Matrix 0 OUT: In0 of 2-bit LUT0	
11:6	Matrix 0 OUT: In1 of 2-bit LUT0	
17:12	Matrix 0 OUT: In0 of 2-bit LUT1	
23:18	Matrix 0 OUT: In1 of 2-bit LUT1	
29:24	Matrix 0 OUT: In0 of 2-bit LUT2	
35:30	Matrix 0 OUT: In1 of 2-bit LUT2	
41:36	Matrix 0 OUT: In0 of 2-bit LUT3	
47:42	Matrix 0 OUT: In1 of 2-bit LUT3	
53:48	Matrix 0 OUT: In0 of 3-bit LUT0	
59:54	Matrix 0 OUT: In1 of 3-bit LUT0	
65:60	Matrix 0 OUT: In2 of 3-bit LUT0	
71:66	Matrix 0 OUT: In0 of 3-bit LUT1	
77:72	Matrix 0 OUT: In1 of 3-bit LUT1	
83:78	Matrix 0 OUT: In2 of 3-bit LUT1	
89:84	Matrix 0 OUT: In0 of 3-bit LUT2	
95:90	Matrix 0 OUT: In1 of 3-bit LUT2	
101:96	Matrix 0 OUT: In2 of 3-bit LUT2	
107:102	Matrix 0 OUT: In0 of 3-bit LUT3	
113:108	Matrix 0 OUT: In1 of 3-bit LUT3	
119:114	Matrix 0 OUT: In2 of 3-bit LUT3	
125:120	Matrix 0 OUT: In0 of 3-bit LUT4	
131:126	Matrix 0 OUT: In1 of 3-bit LUT4	
137:132	Matrix 0 OUT: In2 of 3-bit LUT4	
143:138	Matrix 0 OUT: In0 of 3-bit LUT5	
149:144	Matrix 0 OUT: In1 of 3-bit LUT5	
155:150	Matrix 0 OUT: In2 of 3-bit LUT5	
161:156	Matrix 0 OUT: In0 of 3-bit LUT6	
167:162	Matrix 0 OUT: In1 of 3-bit LUT6	
173:168	Matrix 0 OUT: In2 of 3-bit LUT6	
179:174	Matrix 0 OUT: In0 of 3-bit LUT7	
185:180	Matrix 0 OUT: In1 of 3-bit LUT7	
191:186	Matrix 0 OUT: In2 of 3-bit LUT7	
197:192	Matrix 0 OUT: In0 of 4-bit LUT0	
203:198	Matrix 0 OUT: In1 of 4-bit LUT0	
209:204	Matrix 0 OUT: In2 of 4-bit LUT0 or PGEN CLK	
215:210	Matrix 0 OUT: In3 of 4-bit LUT0 or PGEN nRST	
221:216	Matrix 0 OUT: nSET or nRST of DFF0/Latch0	
227:222	Matrix 0 OUT: Data of DFF0/Latch0	
233:228	Matrix 0 OUT: Clock of DFF0/Latch0	
239:234	Matrix 0 OUT: nSET or nRST of DFF1/Latch1	

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
245:240	Matrix 0 OUT: Data of DFF1/Latch1	
251:246	Matrix 0 OUT: Clock of DFF1/Latch1	
257:252	Matrix 0 OUT: nSET or nRST of DFF2/Latch2	
263:258	Matrix 0 OUT: Data of DFF2/Latch2	
269:264	Matrix 0 OUT: Clock of DFF2/Latch2	
275:270	Matrix 0 OUT: Data of DFF3/Latch3	
281:276	Matrix 0 OUT: Clock of DFF3/Latch3	
287:282	Matrix 0 OUT: Data of DFF4/Latch4	
293:288	Matrix 0 OUT: Clock of DFF4/Latch4	
299:294	Matrix 0 OUT: Data of DFF5/Latch5	
305:300	Matrix 0 OUT: Clock of DFF5/Latch5	
311:306	Matrix 0 OUT: Clock of Pipe Delay 0	
317:312	Matrix 0 OUT: Input Data of Pipe Delay 0	
323:318	Matrix 0 OUT: Reset of Pipe Delay 0	
329:324	Matrix 0 OUT: Input of Edge Detector and Programmable Delay 0	
335:330	Matrix 0 OUT: Input of Inverter 0	
341:336	Matrix 0 OUT: Digital Output of PIN 3	
347:342	Matrix 0 OUT: OE of PIN 3	
353:348	Matrix 0 OUT: Digital Output of PIN 4	
359:354	Matrix 0 OUT: Digital Output of PIN 5	
365:360	Matrix 0 OUT: OE of PIN 5	
371:366	Matrix 0 OUT: Digital Output of PIN 6	
377:372	Matrix 0 OUT: Digital Output of PIN 7	
383:378	Matrix 0 OUT: OE of PIN 7	
389:384	Matrix 0 OUT: Digital Output of PIN 8	
395:390	Matrix 0 OUT: Digital Output of PIN 9	
401:396	Matrix 0 OUT: OE of PIN 9	
407:402	Matrix 0 OUT: Digital Output of PIN 10	
413:408	Matrix 0 OUT: OE of PIN 10	
419:414	Matrix 0 OUT: PDB (Power-down) for ACMP0	
425:420	Matrix 0 OUT: PDB (Power-down) for ACMP4	
431:426	Matrix 0 OUT: PDB (Power-down) for ACMP5	
437:432	Matrix 0 OUT: CNT0/CNT2/CNT9/ External Clock(CLK_Matrix0)	
443:438	Matrix 0 OUT: CNT5/CNT6 External Clock(CLK_Matrix1)	
449:444	Matrix 0 OUT: Input of DLY/CNT0	
455:450	Matrix 0 OUT: Input of DLY/CNT2	
461:456	Matrix 0 OUT: Keep of DLY/CNT2	
467:462	Matrix 0 OUT: Up of DLY/CNT2	
473:468	Matrix 0 OUT: Input of DLY/CNT5	
479:474	Matrix 0 OUT: Input of DLY/CNT6	

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
485:480	Matrix 0 OUT: Input of DLY/CNT9	
491:486	Matrix 0 OUT: ADC Power-down	
497:492	Matrix 0 OUT: CSB of SPI	
503:498	Matrix 0 OUT: SCLK of SPI	
509:504	Matrix 0 OUT: Oscillator Power-down	
515:510	Matrix 0 OUT: Cross Connection Output to Matrix 1 [0]	
521:516	Matrix 0 OUT: Cross Connection Output to Matrix 1 [1]	
527:522	Matrix 0 OUT: Cross Connection Output to Matrix 1 [2]	
533:528	Matrix 0 OUT: Cross Connection Output to Matrix 1 [3]	
539:534	Matrix 0 OUT: Cross Connection Output to Matrix 1 [4]	
545:540	Matrix 0 OUT: Cross Connection Output to Matrix 1 [5]	
551:546	Matrix 0 OUT: Cross Connection Output to Matrix 1 [6]	
557:552	Matrix 0 OUT: Cross Connection Output to Matrix 1 [7]	
563:558	Matrix 0 OUT: Cross Connection Output to Matrix 1 [8]	
569:564	Matrix 0 OUT: Cross Connection Output to Matrix 1 [9]	
575:570	Reserved	
LUT Data		
579:576	2-bit LUT0 Data	Data
583:580	2-bit LUT1 Data	Data
587:584	2-bit LUT2 Data	Data
591:588	2-bit LUT3 Data	Data
599:592	3-bit LUT0 Data	Data
607:600	3-bit LUT1 Data	Data
615:608	3-bit LUT2 Data	Data
623:616	3-bit LUT3 Data	Data
631:624	3-bit LUT4 Data	Data
639:632	3-bit LUT5 Data	Data
647:640	3-bit LUT6 Data	Data
655:648	3-bit LUT7 Data	Data
4-bit LUT0 and PGEN		
671:656	4-bit LUT0 & PGEN Data	Data
675:672	4-bit counter Data in PGEN	Data
676	PGEN Enable Signal	0: 4-bit LUT Function 1: PGEN Function
DFF/LATCH 0		
677	Mode Select	0: DFF Function 1: LATCH Function
678	Output Parity Control	0: Q Output 1: nQ Output
679	nSET or nRST Selection	0: Reset State by Matrix 1: Set State by Matrix
680	Initial State During POR	0: Initial State is 0 1: Initial State is 1

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
DFF/LATCH 1		
681	Mode Select	0: DFF Function 1: LATCH Function
682	Output Parity Control	0: Q Output 1: nQ Output
683	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
684	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 2		
685	Mode Select	0: DFF Function 1: LATCH Function
686	Output Parity Control	0: Q Output 1: nQ Output
687	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
688	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 3		
689	Mode Select	0: DFF Function 1: LATCH Function
690	Output Parity Control	0: Q Output 1: nQ Output
691	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 4		
692	Mode Select	0: DFF Function 1: LATCH Function
693	Output Parity Control	0: Q Output 1: nQ Output
694	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 5		
695	Mode Select	0: DFF Function 1: LATCH Function
696	Output Parity Control	0: Q Output 1: nQ Output
697	Initial State During POR	0: Initial State is 0 1: Initial State is 1
LUT Data		
701:698	2-bit LUT4 Data	Data
705:702	2-bit LUT5 Data	Data
709:706	2-bit LUT6 Data	Data
713:710	2-bit LUT7 Data	Data
721:714	3-bit LUT8 Data	Data
729:722	3-bit LUT9 Data	Data

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
737:730	3-bit LUT10 Data	Data
745:738	3-bit LUT11 Data	Data
753:746	3-bit LUT12 Data	Data
761:754	3-bit LUT13 Data	Data
769:762	3-bit LUT14 Data	Data
777:770	3-bit LUT15 Data	Data
793:778	4-bit LUT1 Data	Data
DFF/LATCH 6		
794	Mode Select	0: DFF Function 1: LATCH Function
795	Output Parity Control	0: Q Output 1: nQ Output
796	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
797	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 7		
798	Mode Select	0: DFF Function 1: LATCH Function
799	Output Parity Control	0: Q Output 1: nQ Output
800	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
801	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 8		
802	Mode Select	0: DFF Function 1: LATCH Function
803	Output Parity Control	0: Q Output 1: nQ Output
804	Set or Reset Selection	0: Reset State by Matrix 1: Set State by Matrix
805	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 9		
806	Mode Select	0: DFF Function 1: LATCH Function
807	Output Parity Control	0: Q Output 1: nQ Output
808	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 10		
809	Mode Select	0: DFF Function 1: LATCH Function
810	Output Parity Control	0: Q Output 1: nQ Output

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
811	Initial State During POR	0: Initial State is 0 1: Initial State is 1
DFF/LATCH 11		
812	Mode Select	0: DFF Function 1: LATCH Function
813	Output Parity Control	0: Q Output 1: nQ Output
814	Initial State During POR	0: Initial State is 0 1: Initial State is 1
ADC and ACMP Control		
815	ADC Native Input From Internal DAC0	0: Disable 1: Enable
816	Multichannel Input MUX Enable (State by PIN 16)	0: Disable (PIN 16 can not Control) 1: Enable
817	ADC Input Mode Control	0: Single-Ended Input 1: Differential Input
820:818	ADC PGA Gain Selection	000: Reserved 001: 0.5x (For single-ended operation only) 010: 1x 011: 2x 100: 4x (For single-ended and differential operation) 101: 8x (For single-ended and differential operation) 110: 16x (For differential operation only) 111: Reserved
821	PGA Power-On Signal Note: in ADC Wake Sleep/dynamic On/Off Mode, it should Set to 0	0: Power-Down 1: Power-On
822	ADC Pseudo-Differential Mode Enable	0: Disable 1: Enable
830:823	DAC1 8 Bit register Control	00: DAC1 Output is ADC Vref bottom Voltage FF: DAC1's Output is ADC Vref top Voltage
831	ACMP 1 Input 100u Current Source Enable	0: Disable 1: Enable
832	ACMP 0 Input 100u Current Source Enable	0: Disable 1: Enable
833	Reserved	
834	DAC1 Power-On Signal	0: Power-down 1: Power-On When DAC0 Used Only, need set this bit
835	Reserved	
837:836	ACMP Buffer Bandwidth Selection	00: 1 K 01: 5 K 10: 20 K 11: 50 K
839:838	ADC Speed Selection	00: Reserved 01: Reserved 10: 100 kHz 11: Reserved

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
840	DAC0 Power-On Signal	0: Power-down 1: Power-On When DAC0 Used Only, need set this bit
842:841	ADC Vref Source Select	00: ADC Vref 01: Reserved 10: 1/4 V_{DD} 11: None
843	DAC0 Input Selection	0: From Register 1: From DCMP1's Negative Input
851:844	DAC0 8 Bit Register Control	00: DAC0 Output is 0 FF: DAC0 Output is 1 V
852	Reserved	
854:853	ACMP 0 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
856:855	ACMP 0 Input Selection	00: PIN 6 Input 01: With Buffer 10: V_{DD} 11: None
858:857	ACMP 1 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
860:859	ACMP 1 Input Selection	00: PIN 12 Input 01: ADC PGA OUT 10: ACMP 0 Input (before Gain) 11: None
861	Reserved	
862	Reserved	
863	ACMP 2 Input Selection	0: PIN 13 Input 1: ACMP 0 Input (before Gain)
865:864	ACMP 2 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
866	Reserved	
868:867	ACMP 3 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
870:869	ACMP 3 Input Selection	00: PIN 15 Input 01: PIN 13 Input 10: ACMP 0 Input (before Gain) 11: None
872:871	ACMP 4 Positive Input Gain Control	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
874:873	ACMP 4 Input Selection	00: PIN 3 Input 01: PIN 15 Input 10: ACMP 0 Input (before Gain) 11: None
875	Reserved	
877:876	Output Buffer1 Source Selection	00: Buffer Power-down 01: ACMP 2' Input 10: ACMP 3's Input 11: DAC1's Output
879:878	Output Buffer0 Source Selection	00: Buffer Power-down 01: ACMP 0' Input 10: ACMP 1's Input 11: DAC0's Output
880	Reserved	
881	Reserved	
882	ADC Wake Sleep Enable	0: Disable 1: Enable
883	DAC1 Input Selection	0: From DCMP1's Negative input 1: From Register
884	ADC Wake Sleep Enable	0: Disable 1: Enable
885	Force ADC Analog Circuit On	0: Disable 1: Enable
886	PGA Output Enable	0: Disable 1: Enable
BG, ACMP and Vref		
891:887	Reserved	
896:892	ACMP0 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP0 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP0 / 2 11110: DAC1_OUT 11111: DAC0_OUT

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
901:897	ACMP1 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 11.5 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP0 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP0 / 2 11110: DAC1_OUT 11111: DAC0_OUT
906:902	ACMP2 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_OUT 11111: DAC0_OUT
911:907	ACMP3 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_OUT 11111: DAC0_OUT

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
916:912	ACMP4 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}3 11001: V_{DD}/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP2 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP2 / 2 11110: DAC1_OUT 11111: DAC0_OUT
921:917	ACMP5 Vref Value Selection	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: Vref_Ext_ACMP1 11011: Vref_Ext_ACMP5 11100: Vref_Ext_ACMP1 / 2 11101: Vref_Ext_ACMP5 / 2 11110: DAC1_OUT 11111: DAC0_OUT
922	Reserved	
923	Bangap OK for ADC, ACMP Output Delay Time Select, the start Time is porb_core go to High	0: 550 µs 1: 100 µs
925:924	ACMP5 Hysteresis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
927:926	ACMP4 Hysteresis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
929:928	ACMP3 Hysteresis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
931:930	ACMP2 Hysteresis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
933:932	ACMP1 Hysteresis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
935:934	ACMP0 Hysteresis Control	00: 0 01: 25 mV 10: 50 mV 11: 200 mV
936	Bandgap Turn On by Register	0: Turn Off 1: Turn On (if chip is Power-down, the Bandgap will Power-down even if it is set to 1)
937	Reserved	
938	Reserved	
939	Reserved	
IO Pad		
940	IO pre-Charge Enable Bit	0: Disable 1: Enable
PIN 2		
942:941	PIN2 Input Mode Control	00: Digital in without Schmitt trigger 01: Digital in with Schmitt trigger 10: Low Voltage Digital IN 11: Reserved
944:943	PIN2 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
945	PIN2 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 3		
947:946	PIN 3 Input Mode Control	00: Digital in without Schmitt trigger 01: Digital in with Schmitt trigger 10: Low Voltage Digital IN 11: Analog IO
949:948	PIN 3 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
951:950	PIN 3 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
952	PIN 3 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
PIN 4		
955:953	PIN 4 Mode Control	000: Digital in without Schmitt trigger 001: Digital in with Schmitt trigger 010: Low Voltage Digital IN 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
957:956	PIN 4 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
958	PIN 4 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
959	PIN 4 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 5		
961:960	PIN 5 Input Mode Control	00: Digital in without Schmitt trigger 01: Digital in with Schmitt trigger 10: Low Voltage Digital IN 11: Analog IO
963:962	PIN 5 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
965:964	PIN 5 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
966	PIN 5 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 6		
969:967	PIN 6 Mode Control	000: Digital in without Schmitt trigger 001: Digital in with Schmitt trigger 010: Low Voltage Digital IN 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
971:970	PIN 6 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
972	PIN 6 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
973	PIN 6 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 7		

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
975:974	PIN 7 Input Mode Control	00: Digital in without Schmitt trigger 01: Digital in with Schmitt trigger 10: Low Voltage Digital IN 11: Analog IO
977:976	PIN 7 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
979:978	PIN 7 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
980	PIN 7 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 8		
983:981	PIN 8 Mode Control	000: Digital in without Schmitt trigger 001: Digital in with Schmitt trigger 010: Low Voltage Digital IN 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
985:984	PIN 8 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
986	PIN 8 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
987	PIN 8 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 9		
989:988	PIN 9 Input Mode Control	00: Digital in without Schmitt trigger 01: Digital in with Schmitt trigger 10: Low Voltage Digital IN 11: Analog IO
991:990	PIN 9 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
993:992	PIN 9 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
994	PIN 9 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 10		
996:995	PIN 10 Input Mode Control	00: Digital in without Schmitt trigger 01: Digital in with Schmitt trigger 10: Low Voltage Digital IN 11: Analog IO

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
998:997	PIN 10 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
1000:999	PIN 10 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1001	PIN 10 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
1002	PIN 10 4x Drive Enable	0: Disable 1: Enable
1015:1003	Reserved	
1023:1016	Die ID: Power up Sequence Bits	Data Hex: 5A
Matrix 1 Output Selection		
1029:1024	Matrix 1 OUT:In0 of 2-bit LUT4	
1035:1030	Matrix 1 OUT:In1 of 2-bit LUT4	
1041:1036	Matrix 1 OUT:In0 of 2-bit LUT5	
1047:1042	Matrix 1 OUT:In1 of 2-bit LUT5	
1053:1048	Matrix 1 OUT:In0 of 2-bit LUT6	
1059:1054	Matrix 1 OUT:In1 of 2-bit LUT6	
1065:1060	Matrix 1 OUT:In0 of 2-bit LUT7	
1071:1066	Matrix 1 OUT:In1 of 2-bit LUT7	
1077:1072	Matrix 1 OUT:In0 of 3-bit LUT8	
1083:1078	Matrix 1 OUT:In1 of 3-bit LUT8	
1089:1084	Matrix 1 OUT:In2 of 3-bit LUT8	
1095:1090	Matrix 1 OUT:In0 of 3-bit LUT9	
1101:1096	Matrix 1 OUT:In1 of 3-bit LUT9	
1107:1102	Matrix 1 OUT:In2 of 3-bit LUT9	
1113:1108	Matrix 1 OUT:In0 of 3-bit LUT10	
1119:1114	Matrix 1 OUT:In1 of 3-bit LUT10	
1125:1120	Matrix 1 OUT:In2 of 3-bit LUT10	
1131:1126	Matrix 1 OUT:In0 of 3-bit LUT11	
1137:1132	Matrix 1 OUT:In1 of 3-bit LUT11	
1143:1138	Matrix 1 OUT:In2 of 3-bit LUT11	
1149:1144	Matrix 1 OUT:In0 of 3-bit LUT12	
1155:1150	Matrix 1 OUT:In1 of 3-bit LUT12	
1161:1156	Matrix 1 OUT:In2 of 3-bit LUT12	
1167:1162	Matrix 1 OUT:In0 of 3-bit LUT13	
1173:1168	Matrix 1 OUT:In1 of 3-bit LUT13	
1179:1174	Matrix 1 OUT:In2 of 3-bit LUT13	
1185:1180	Matrix 1 OUT:In0 of 3-bit LUT14	
1191:1186	Matrix 1 OUT:In1 of 3-bit LUT14	

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1197:1192	Matrix 1 OUT:In2 of 3-bit LUT14	
1203:1198	Matrix 1 OUT:In0 of 3-bit LUT15	
1209:1204	Matrix 1 OUT:In1 of 3-bit LUT15	
1215:1210	Matrix 1 OUT:In2 of 3-bit LUT15	
1221:1216	Matrix 1 OUT:In0 of 4-bit LUT1	
1227:1222	Matrix 1 OUT:In1 of 4-bit LUT1	
1233:1228	Matrix 1 OUT:In2 of 4-bit LUT1	
1239:1234	Matrix 1 OUT:In3 of 4-bit LUT1	
1245:1240	Matrix 1 OUT: Set or nRST of DFF6/Latch6	
1251:1246	Matrix 1 OUT: Data of DFF6/Latch6	
1257:1252	Matrix 1 OUT: Clock of DFF6/Latch6	
1263:1258	Matrix 1 OUT: Set or nRST of DFF7/Latch7	
1269:1264	Matrix 1 OUT: Data of DFF7/Latch7	
1275:1270	Matrix 1 OUT: Clock of DFF7/Latch7	
1281:1276	Matrix 1 OUT: Set or nRST of DFF8/Latch8	
1287:1282	Matrix 1 OUT: Data of DFF8/Latch8	
1293:1288	Matrix 1 OUT: Clock of DFF8/Latch8	
1299:1294	Matrix 1 OUT: Data of DFF9/Latch9	
1305:1300	Matrix 1 OUT: Clock of DFF9/Latch9	
1311:1306	Matrix 1 OUT: Data of DFF10/Latch10	
1317:1312	Matrix 1 OUT: Clock of DFF10/Latch10	
1323:1318	Matrix 1 OUT: Data of DFF11/Latch11	
1329:1324	Matrix 1 OUT: Clock of DFF11/Latch11	
1335:1330	Matrix 1 OUT: Clock of Pipe Delay 1	
1341:1336	Matrix 1 OUT: Input Data of Pipe Delay 1	
1347:1342	Matrix 1 OUT: Reset of Pipe Delay 1	
1353:1348	Matrix 1 OUT: Input of Edge Detector and Programmable Delay 1	
1359:1354	Matrix 1 OUT: Input of Inverter 1	
1365:1360	Matrix 1 OUT: Digital Output of PIN 12	
1371:1366	Matrix 1 OUT: Digital Output of PIN 13	
1377:1372	Matrix 1 OUT: OE of PIN 13	
1383:1378	Matrix 1 OUT: Digital Output of PIN 14	
1389:1384	Matrix 1 OUT: OE of PIN 14	
1395:1390	Matrix 1 OUT: Digital Output of PIN 15	
1401:1396	Matrix 1 OUT: Digital Output of PIN 16	
1407:1402	Matrix 1 OUT: OE of PIN 16	
1413:1408	Matrix 1 OUT: Digital Output of PIN 17	
1419:1414	Matrix 1 OUT: Digital Output of PIN 18	
1425:1420	Matrix 1 OUT: OE of PIN 18	
1431:1426	Matrix 1 OUT: Digital Output of PIN 19	
1437:1432	Matrix 1 OUT: OE of PIN 19	

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1443:1438	Matrix 1 OUT: Digital Output of PIN 20	
1449:1444	Matrix 1 OUT: PDB(Power-down) for ACMP1	
1455:1450	Matrix 1 OUT: PDB(Power-down) for ACMP2	
1461:1456	Matrix 1 OUT: PDB(Power-down) for ACMP3	
1467:1462	Matrix 1 OUT:CNT7/CNT8/PWM/ADC External Clock (CLK_Matrix2)	
1473:1468	Matrix 1 OUT:CNT1/CNT3/CNT4 External Clock (CLK_Matrix3)	
1479:1474	Matrix 1 OUT: Input of DLY/CNT1	
1485:1480	Matrix 1 OUT: Input of DLY/CNT3	
1491:1486	Matrix 1 OUT: Input of DLY/CNT4	
1497:1492	Matrix 1 OUT: Keep of DLY/CNT4	
1503:1498	Matrix 1 OUT: Up of DLY/CNT4	
1509:1504	Matrix 1 OUT: Input of DLY/CNT7	
1515:1510	Matrix 1 OUT: Input of DLY/CNT8	
1521:1516	Matrix 1 OUT: PWM Power-down	
1527:1522	Matrix 1 OUT: PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 0	
1533:1528	Matrix 1 OUT: PWM/DCMP0 Positive Input and PWM/DCMP1 Negative Input Register Selection Bit 1	
1539:1534	Matrix 1 OUT: Cross Connection Output to Matrix 0 [0]	
1545:1540	Matrix 1 OUT: Cross Connection Output to Matrix 0 [1]	
1551:1546	Matrix 1 OUT: Cross Connection Output to Matrix 0 [2]	
1557:1552	Matrix 1 OUT: Cross Connection Output to Matrix 0 [3]	
1563:1558	Matrix 1 OUT: Cross Connection Output to Matrix 0 [4]	
1569:1564	Matrix 1 OUT: Cross Connection Output to Matrix 0 [5]	
1575:1570	Matrix 1 OUT: Cross Connection Output to Matrix 0 [6]	
1581:1576	Matrix 1 OUT: Cross Connection Output to Matrix 0 [7]	
1587:1582	Matrix 1 OUT: Cross Connection Output to Matrix 0 [8]	
1593:1588	Matrix 1 OUT: Cross Connection Output to Matrix 0 [9]	
1599:1594	Reserved	
Programmable Delay with Edge Detector 0		
1601:1600	Mode Selection	00: Rising Edge Detect 01: Falling Edge Detect 10: Both Edge Detect 11: Both Edge Delay
1603:1602	Delay Time Selection	00: 110 ns Delay 01: 220 ns Delay 10: 330 ns Delay 11: 440 ns Delay
1604	Output Delay Control	0: Output no Delay 1: Output Delay

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
Programmable Delay with Edge Detector 1		
1606:1605	Mode Selection	00: Rising Edge Detect 01: Falling Edge Detect 10: Both Edge Detect 11: Both Edge Delay
1608:1607	Delay Time Selection	00: 110 ns Delay 01: 220 ns Delay 10: 330 ns Delay 11: 440 ns Delay
1609	Output Delay Control	0: Output No Delay 1: Output Delay
Pipe Delay 0		
1613:1610	OUT0 Selection Bits	Register Bits From 0 to 15, Data Delay From 1 to 16 pipes
1617:1614	OUT1 Selection Bits	Register Bits From 0 to 15, Data Delay From 1 to 16 pipes
1618	OUT1 Output polarity Control	0: non-inverted 1: inverted
Pipe Delay 1		
1622:1619	OUT0 Selection Bits	Register Bits From 0 to 15, Data Delay From 1 to 16 pipes
1626:1623	OUT1 Selection Bits	Register Bits From 0 to 15, Data Delay From 1 to 16 pipes
1627	OUT1 Output polarity Control	0: non-inverted 1: inverted
Oscillator		
1629:1628	PWM and ADC Clock Source Select	00: RING OSC 01: Matrix(Matrix1_OUT73) 10: RC OSC 11: SPI_SCLK(Matrix0_OUT83)
1632:1630	Clock divide Ratio Control for ring OSC to Matrix	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
1633	PWM Data synchronized with SPI Clock Enable	0: Disable 1: Enable
1634	FSM Data synchronized with SPI Clock Enable	0: Disable 1: Enable
1636:1635	Clock divide Ratio Control for RING OSC	00: /1 01: /4 10: /8 11: /16
1637	Ring OSC Clock to Matrix Input Enable	0: Disable 1: Enable
1638	Matrix Power-down (Matrix0_OUT84) enable for ring Oscillator	0: Disable 1: Enable

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1639	ADC Clock divide by 16 Bypass	0: Non-Bypass 1: Bypass
1640	Ring OSC Turn On by Register Note: if chip is Powered Down, the Ring OSC will Power-down even if this bit is set to 1	0: Turn Off 1: Turn On
1641	ADC Data synchronized with SPI Clock Enable	0: Disable 1: Enable
1642	RC OSC Clock to Matrix Input Enable	0: Disable 1: Enable
1644:1643	Clock divide Ratio Control for RC OSC	00: /1 01: /2 10: /4 11: /8
1647:1645	Clock divide Ratio Control for RC OSC to Matrix	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
1648	Matrix Power-down (Matrix0_OUT84) enable for RC Oscillator	0: Disable 1: Enable
1649	RC OSC Turn On by Register Note: if chip is Powered Down, the Ring OSC will Power-down even if this Bit is Set to 1	0: Turn Off 1: Turn On
1650	RC OSC frequency Select	0: 25 kHz 1: 2 MHz
1651	bypass RC oscillator with external clock(matrix-_OUT1_73)	0: RC OSC 1: external clock
1652	matrix power-down (matrix0_OUT84) enable for LF oscillator	0: Disable 1: Enable
1653	Low Frequency OSC turn on by register	0: Turn Off 1: Turn On (if chip is Power-down, the LF OSC will Power-down even if it is Set to 1)
1655:1654	Clock divide Ratio Control for LF OSC	00: /1 01: /2 10: /4 11: /16
SPI		
1656	SPI Used as ADC Buffer Enable (1 Clock Delayed)	
1657	SPI Parallel Input Data Source Selection	0: FSM0[7:0], FSM1[7:0] 1: ADC
1658	SPI Clock phase (CPHA)	
1659	SPI Clock polarity (CPOL)	
1660	byte Selection	0: 16 bits 1: 8-bits (least significant 8 Bits)
1661	SPI Input/Output Mode Selection	0: Serial IN Parallel OUT 1: Parallel IN Serial OUT
PWM0		

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1669:1662	Register 3, 8 Bits NVM Data to PWM/DCMP or DAC Input	Data
1672:1670	PWM0 Dead Band zone Control	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
1673	PWM/DCMP0 Mode Selection	0: PWM Output duty cycle Down to 0 % and DCMP OUT = 1 if IN+ > IN- 1: PWM Output duty cycle up to 100 % and DCMP OUT = 1 if IN+ >= IN-
1674	PWM/DCMP0 Function Selection	0: PWM 1: DCMP When in PWM Mode, OUTN0 is pwm1's Negative output When in DCMP Mode, OUTN0 is DCMP1's match Output
1675	PWM/DCMP0 Clock Source Selection	0: Clock From MUX State by registers [1629:1628] 1: Matrix1_73
1676	PWM/DCMP0 Clock Inversion	0: Disable 1: Enable
1677	power-down sync to clock and output state control in power-down mode	0: power-down is not synchronized with clock, and output reset to 0 when PWM/DCMP is power-down, 1: power-down is synchronized with clock, when PD = 0, the clock is enabled after 2 clock cycles, while when PD = 1, the clock is gated immediately. and the output is kept at current state when PD = 1.
1678	PWM/DCMP0 Turn On by Register	0: Disable 1: Enable
1680:1679	PWM/DCMP0 Positive Input Source Selection	00: ADC 01: 8MSBs SPI 10: FSM0_Q[7:0] 11: From MUX State by Matrix1_OUT[84:83]
1682:1681	PWM/DCMP0 Negative Input Source Selection	00: CNT8_Q[7:0] 01: Register 0 10: 8LSBs SPI 11: FSM1_Q[7:0]
1690:1683	Register 2, 8 Bits NVM Data to PWM/DCMP or DAC Input	Data
PWM1		
1693:1691	PWM1 Dead Band zone Control	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
1694	PWM/DCMP1 Mode Selection	0: PWM Output duty cycle Down to 0 % and DCMP OUT = 1 if IN+ > IN- 1: PWM Output duty cycle up to 100 % and DCMP OUT = 1 if IN+ >= IN-

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1695	PWM/DCMP1 Function Selection	0: PWM 1: DCMP When in PWM Mode, OUTN1 is pwm1's Negative output When in DCMP Mode, OUTN0 is DCMP1's match Output
1696	PWM/DCMP1 Clock Source Selection	0: Clock From MUX State by registers [1629:1628] 1: Matrix1_73
1697	PWM/DCMP1 Clock Inversion	0: Disable 1: Enable
1698	PWM/DCMP1 Turn On by Register	0: Disable 1: Enable
1700:1699	PWM/DCMP1 Positive Input Source Selection	00: ADC 01: 8LSBs SPI 10: FSM1[7: 0] 11: Register 1
1702:1701	PWM/DCMP1 Negative Input and DAC Input Source Selection	00: CNT11_Q[7:0] 01: From MUX State by Matrix1_OUT[84:83] 10: 8MSBs SPI 11: FSM0_Q[7:0]
1710:1703	Register 1, 8 Bits NVM Data to PWM/DCMP or DAC Input	Data
PWM2		
1713:1711	PWM2 Dead Band zone Control	000: 10 ns 001: 20 ns 010: 30 ns 011: 40 ns 100: 50 ns 101: 60 ns 110: 70 ns 111: 80 ns
1714	PWM/DCMP2 Mode Selection	0: PWM Output duty cycle Down to 0 % and DCMP OUT = 1 if IN+ > IN- 1: PWM Output duty cycle up to 100 % and DCMP OUT = 1 if IN+ >= IN-
1715	PWM/DCMP2 Function Selection	0: PWM 1: DCMP When in PWM Mode, OUTN2 is pwm2's Negative output When in DCMP Mode, OUTN2 is DCMP1's match Output
1716	PWM/DCMP2 Clock Source Selection	0: Clock From MUX State by registers [1629: 1628] 1: Matrix1_73
1717	PWM/DCMP2 Clock Inversion	0: Disable 1: Enable
1718	PWM/DCMP2 Turn On by Register	0: Disable 1: Enable
1720:1719	PWM/DCMP2 Positive Input Source Selection	00: ADC 01: 8MSBs SPI 10: FSM1[7: 0] 11: Register 3
1722:1721	PWM/DCMP2 Negative Input and DAC Input Source Selection	00: CNT8_Q[7: 0] 01: Register 2 10: 8LSBs SPI 11: FSM0_Q[7: 0]

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1730:1723	Register 0, 8 Bits NVM Data to PWM/DCMP or DAC Input	Data
DLY/CNT 0		
1744:1731	CNT0 14bits Data From Register	Data
1747:1745	DLY/CNT0 Clock Source Select	000: RC OSC 001: RC OSC_DIV4 010: RC OSC_DIV24 011: RC OSC_DIV64 100: LFOSC 101: DLY_OUT9 110: RING OSC 111: Matrix0_OUT72
1749:1748	DLY0 Edge Mode Select or CNT0 Reset Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1751:1750	DLY/CNT0 Macrocell Function Select	00: DLY 01: CNT 10: Edge Detect 11: Wake Sleep Ratio Control
1752	Wake Sleep Output State When WS Oscillator is Power-down	0: in Power-down Mode 1: in Normal Operation State
DLY/CNT 1		
1766:1753	CNT1 14-bits Data from Register	Data
1769:1767	DLY/CNT1 Clock Source Select	000: RC OSC 001: RC OSC_DIV4 010: RC OSC_DIV24 011: RC OSC_DIV64 100: LF OSC 101: DLY_OUT0 110: RING OSC 111: Matrix1_OUT74
1771:1770	DLY1 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1773:1772	DLY/CNT1 Macrocell Function Select	00: DLY 01: CNT 10: Edge Detect 11: Reserved

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
DLY/CNT 2/FSM0		
1787:1774	CNT2 14-bits Data from Register	Data
1791:1788	DLY2/CNT2/FSM0 Clock Source Select	0000: RC OSC 0001: RC OSC_DIV4 0010: RC OSC_DIV12 0011: RC OSC_DIV24 0100: RC OSC_DIV64 0101: DLY_OUT1 0110: Matrix0_OUT72 0111: Matrix0_OUT72 divide by 8 1000: RING OSC 1001: Matrix0_OUT83(SPI_SCLK) 1010: LF OSC 1011: CLK of FSM_DIV256 1100: CLK PWM 1101: Reserved 1110: Reserved 1111: Reserved
1793:1792	DLY2 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1795:1794	DLY/CNT2 Macrocell Function Select	00: DLY 01: CNT/FSM 10: Edge Detect 11: None
1797:1796	FSM0 Input Data Source Select	00: 14 Bits NVM Data 01: 8-bits ADC Data 10: 0 11: 8LSBs SPI Parallel Data
1798	CNT2 Value Control	0: Reset (CNT value = 0) 1: Set (CNT value = FSM Data)
DLY/CNT 3		
1812:1799	CNT3 14-bits Data from Register	Data
1815:1813	DLY/CNT3 Clock Source Select	000: RC OSC 001: RC OSC_DIV4 010: RC OSC_DIV24 011: RC OSC_DIV64 100: LF OSC 101: DLY_OUT2 110: RING OSC 111: Matrix1_OUT74

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1817:1816	DLY3 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1819:1818	DLY/CNT3 Macrocell Function Select	00: DLY 01: CNT 10: Edge Detect 11: CNT (the Reset From Matrix not Control the Oscillator)
DLY/CNT 4/FSM1		
1827:1820	CNT4 8-bits Data From Register	Data
1831:1828	DLY4/CNT4/FSM1 Clock Source Select	0000: RC OSC 0001: RC OSC_DIV4 0010: RC OSC_DIV12 0011: RC OSC_DIV24 0100: RC OSC_DIV64 0101: DLY_OUT3 0110: Matrix1_OUT74 0111: Matrix0_OUT72 divide by 8 1000: RING OSC 1001: Matrix0_OUT83(SPI_SCLK) 1010: LF OSC 1011: CLK FSM_DIV256 1100: CLK PWM 1101: Reserved 1110: Reserved 1111: Reserved
1833:1832	DLY4 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1834	DLY4/CNT4/FSM1 Macrocell Function Select	0: DLY 1: CNT/FSM
1836:1835	FSM1 Input Data Source Select	00: 8-bits NVM Data 01: 8-bits ADC Data 10: 8MSBs SPI Parallel Data 11: 0
1837	CNT4 Value Control	0: Reset (CNT value = 0) 1: Set (CNT value = FSM Data)
DLY/CNT 5		

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1845:1838	CNT5 8-bits Data From Register	Data
1848:1846	DLY/CNT5 Clock Source Select	000: RC OSC 001: RC OSC_DIV4 010: RC OSC_DIV24 011: RC OSC_DIV64 100: LF OSC 101: DLY_OUT4 110: RING OSC 111: Matrix0_OUT73
1850:1849	DLY5 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1851	DLY/CNT5 Macrocell Function Select	0: DLY 1: CNT
DLY/CNT 6		
1859:1852	CNT6 8-bits Data from Register	Data
1862:1860	DLY/CNT6 Clock Source Select	000: RC OSC 001: RC OSC_DIV4 010: RC OSC_DIV24 011: RC OSC_DIV64 100: LF OSC 101: DLY_OUT5 110: RING OSC 111: Matrix0_OUT73
1864:1863	DLY6 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1865	DLY/CNT6 Macrocell Function Select	0: DLY 1: CNT
DLY/CNT 7		
1873:1866	CNT7 8-bits Data from Register	Data

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1876:1874	DLY/CNT7 Clock Source Select	000: RC OSC 001: RC OSC_DIV4 010: RC OSC_DIV24 011: RC OSC_DIV64 100: LF OSC 101: DLY_OUT6 110: RING OSC 111: Matrix1_OUT73
1878:1877	DLY7 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1879	DLY/CNT7 Macrocell Function Select	0: DLY 1: CNT
DLY/CNT 8		
1887:1880	CNT8 8-bits Data from Register	Data
1891:1888	DLY/CNT8 Clock Source Select	0000: RC OSC 0001: RC OSC_DIV4 0010: RC OSC_DIV12 0011: RC OSC_DIV24 0100: RC OSC_DIV64 0101: DLY_OUT7 0110: Matrix1_OUT73 0111: Matrix0_OUT72 divide by 8 1000: RING OSC 1001: Matrix0_OUT83(SPI_SCLK) 1010: LF OSC 1011: CLK FSM_DIV256 1100: CLK PWM 1101: Reserved 1110: Reserved 1111: Reserved
1893:1892	DLY8 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1894	DLY/CNT8 Macrocell Function Select	0: DLY 1: CNT/PWM_RAMP
DLY/CNT 9		
1902:1895	CNT9 8-bits Data from Register	Data

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1906:1903	DLY/CNT9 Clock Source Select	0000: RC OSC 0001: RC OSC_DIV4 0010: RC OSC_DIV12 0011: RC OSC_DIV24 0100: RC OSC_DIV64 0101: DLY_OUT8 0110: Matrix0_OUT72 0111: Matrix0_OUT72 divide by 8 1000: RING OSC 1001: Matrix0_OUT83(SPI_SCLK) 1010: LF OSC 1011: CLK FSM_DIV256 1100: CLK PWM 1101: Reserved 1110: Reserved 1111: Reserved
1908:1907	DLY9 Edge Mode Select	If DLY Mode; 00: Both Edge 01: Falling Edge 10: Rising Edge 11: None If CNT Reset Mode; 00: Both Edge Reset 01: Falling Edge Reset 10: Rising Edge Reset 11: High level Reset
1909	DLY/CNT9 Macrocell Function Select	0: DLY 1: CNT/PWM_RAMP
1910	Reserved	
PIN 12		
1913:1911	PIN 12 Mode Control	000: Digital in without Schmitt trigger 001: Digital in with Schmitt trigger 010: Low Voltage Digital in 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
1915:1914	PIN 12 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1916	PIN 12 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
1917	PIN 12 Output Driver Current double	0: 1x drive 1: 2x drive
1918	PIN 12 4x Drive Enable	0: Disable 1: Enable
PIN 13		
1920:1919	PIN 13 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog IO

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1922:1921	PIN 13 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
1924:1923	PIN 13 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1925	PIN 13 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 14		
1927:1926	PIN 14 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog IO
1929:1928	PIN 14 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
1931:1930	PIN 14 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1932	PIN 14 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 15		
1935:1933	PIN 15 Mode Control	000: Digital in without Schmitt trigger 001: Digital in with Schmitt trigger 010: Low Voltage Digital IN 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
1937:1936	PIN 15 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1938	PIN 15 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
1939	PIN 15 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 16		
1941:1940	PIN 16 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog IO
1943:1942	PIN 16 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
1945:1944	PIN 16 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1946	PIN 16 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 17		
1949:1947	PIN 17 Mode Control	000: Digital in without Schmitt trigger 001: Digital in with Schmitt trigger 010: Low Voltage Digital IN 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
1951:1950	PIN 17 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1952	PIN 17 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
1953	PIN 17 Output Driver Current double	0: 1x drive 1: 2x drive
PIN 18		
1955:1954	PIN 18 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog IO
1957:1956	PIN 18 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
1959:1958	PIN 18 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1960	PIN 18 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 19		
1962:1961	PIN 19 Input Mode Control	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low Voltage Digital Input 11: Analog IO
1964:1963	PIN 10 Output Mode Control	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-DRAIN 11: 2x Open-DRAIN
1966:1965	PIN 19 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M

Table 63: Register Map (Continued)

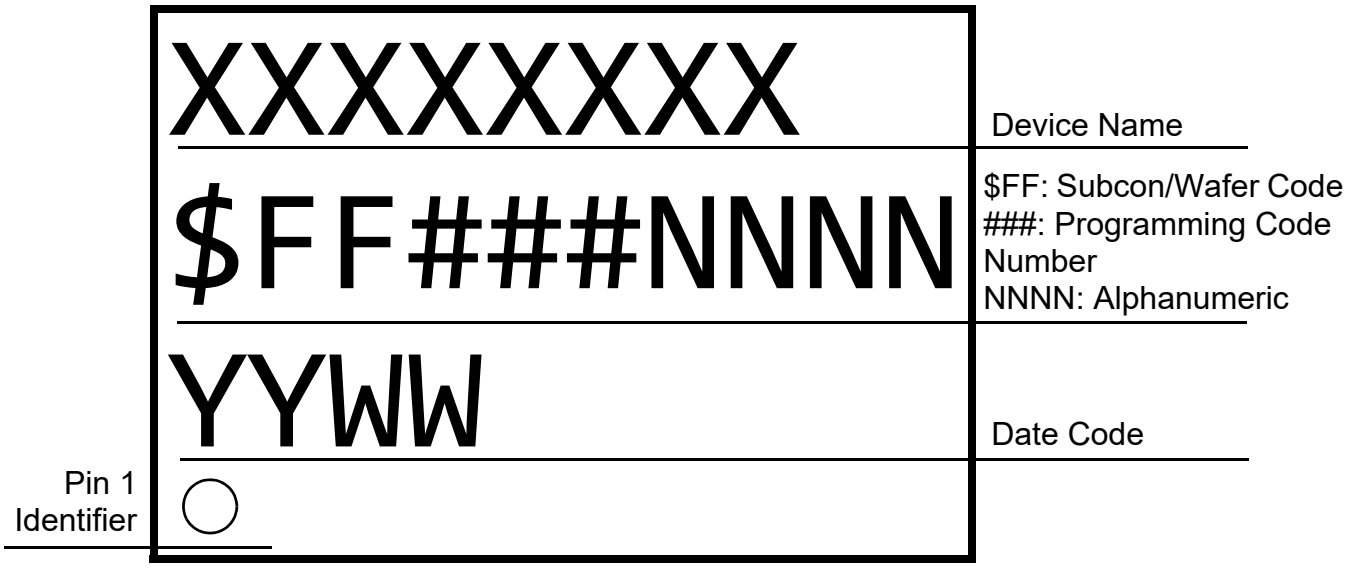
Register Bit Address	Signal Function	Register Bit Definition
1967	PIN 19 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
PIN 20		
1970:1968	PIN 20 Mode Control	000: Digital IN without Schmitt trigger 001: Digital IN with Schmitt trigger 010: Low Voltage Digital IN 011: Analog IO 100: Push-Pull 101: NMOS Open-DRAIN 110: PMOS Open-DRAIN 111: Analog IO & NMOS Open-DRAIN
1972:1971	PIN 20 Pull-Up/Down Resistor Selection	00: Floating 01: 10 k 10: 100 k 11: 1 M
1973	PIN 20 Pull-Up Resistor Enable	0: Pull-Down 1: Pull-Up
1974	PIN 20 Output Driver Current double	0: 1x drive 1: 2x drive
1981:1975	Reserved	
1987:1982	Reserved	
1995:1988	Reserved	
2001:1996	Reserved	
2007:2002	Reserved	
2008	Bypass V_{DD} to 1.8 V Device Only When Power is 1.8 V	0: 1.8 V Use Regulator 1: Bypass V_{DD} as 1.8 V Device Power
2009	Input pad Enable to Core nRST Delay 500 µs Enable	0: Delay 4 µs 1: Delay 500 µs
2010	Power Auto Detector Function for Charge Pump	0: Enable 1: Disable
2012:2011	Reserved	
2014:2013	Reserved	
SPI top Control		
2015	SPI Parallel Output Selection for Matrix 1 (IN[44] → IN[51])	0: Matrix 1 Input From DCMP 1: Matrix 1 Input From SPI Parallel Output [7: 0]
2017:2016	SPI SDIO Output Control	0X: PIN 10 digital OUT From Matrix 0 (OUT67) 10: From SPI (SDO) 11: From ADC serial Output
PIN 2 Reset Control		
2018	Bypass the PIN 2	0: PIN 2 Edge Active 1: PIN 2 High Active
2019	PIN2 Edge Detect Mode	0: Rising Edge 1: Falling Edge
2020	PIN2 Reset Enable	0: Enable 1: Disable
2027:2021	Reserved	
NVM		
2029:2028	Reserved	

Table 63: Register Map (Continued)

Register Bit Address	Signal Function	Register Bit Definition
2030	Reserved	
2038:2031	Pattern ID	Data Note: assigned to track code revision
2039	Read Protection	0: Protection Disable 1: Protection Enable
2047:2040	Die ID: Power up Sequence Bits	Data Hex: A5

24 Package Top Marking Definitions

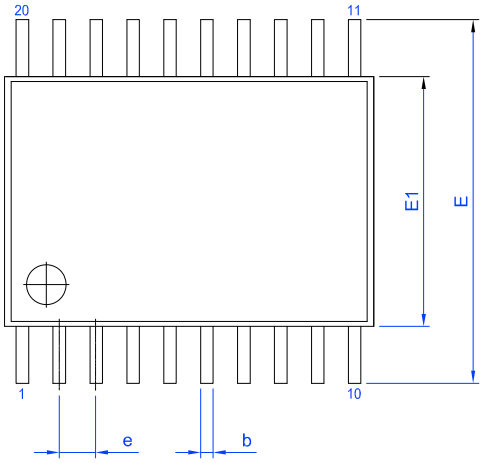
24.1 TSSOP-20



25 Package Information

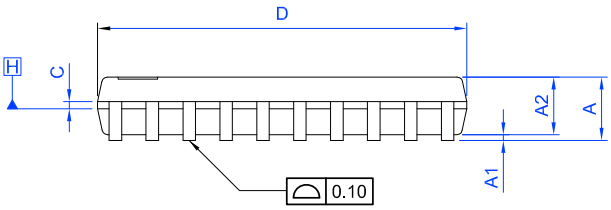
25.1 PACKAGE OUTLINES FOR TSSOP 20L 173 MIL GREEN PACKAGE

JEDEC MO-220
IC Net Weight: 0.083 g

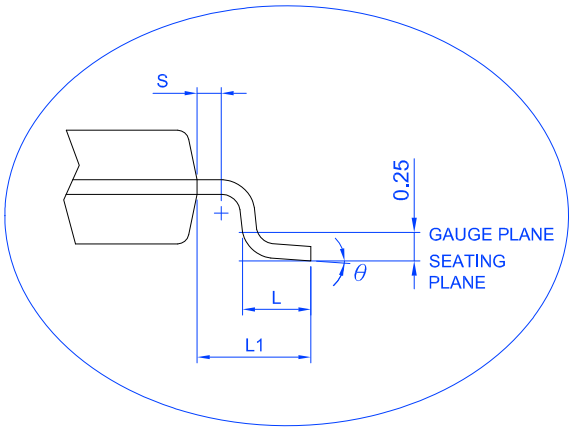


Marking View

Side View



Side View



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	-	-	1.20	D	6.40	6.50	6.60
A1	0.05	-	0.15	E1	4.30	4.40	4.50
A2	0.80	0.90	1.05	E	6.40 BSC		
b	0.19	-	0.30	L	0.50	0.60	0.75
C	0.09	-	0.20	L1	1.00 REF		
e	0.65 BSC			S	0.20	-	-
				Θ	0°	-	8°

NOTES:

1.JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F

2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.

5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H

25.2 TSSOP HANDLING

Be sure to handle TSSOP package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle TSSOP package with fingers as this can contaminate the package pins and interface with solder reflow.

25.3 SOLDERING INFORMATION

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 25.74 mm3 (nominal) for TSSOP-20. More information can be found at www.jedec.org.

26 Ordering Information

Part Number	Type
SLG46620-AG	20-pin TSSOP
SLG46620-AGTR	20-pin TSSOP Tape and Reel (4k units)

Note 1 Use SLG46620-AG to order. Shipments are automatically in Tape and Reel.
Note 2 "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

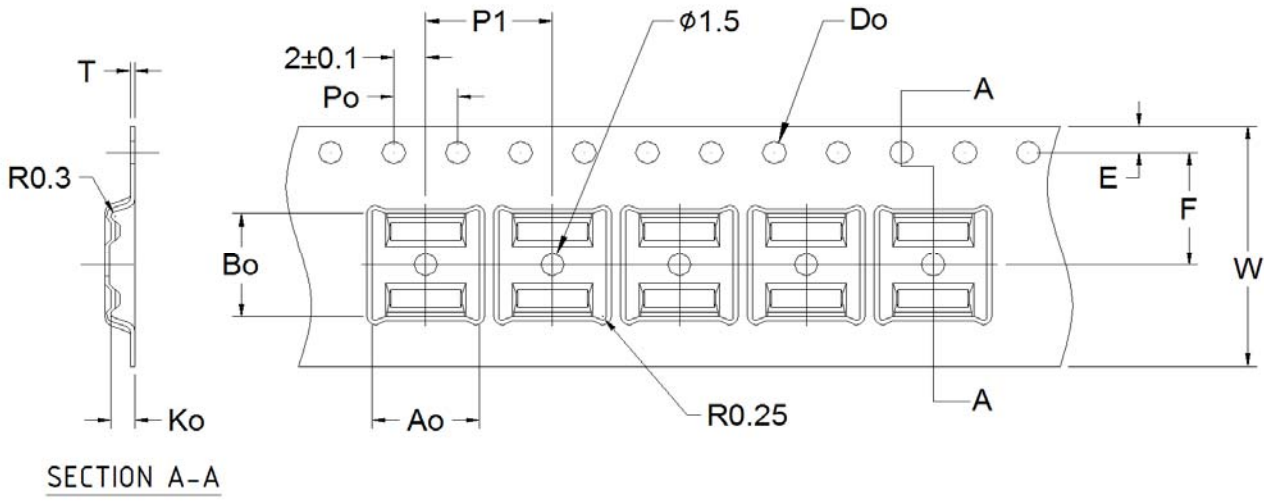
26.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
TSSOP 20L 173 MIL Green Package	20	6.5 x 6.4	4,000	4,000	330/100	42	336	42	336	16	8

26.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
TSSOP 20L 173 MIL Green Package	6.8	6.9	1.6	4	8	1.5	1.75	7.5	16	0.3

26.3 TSSOP- 20

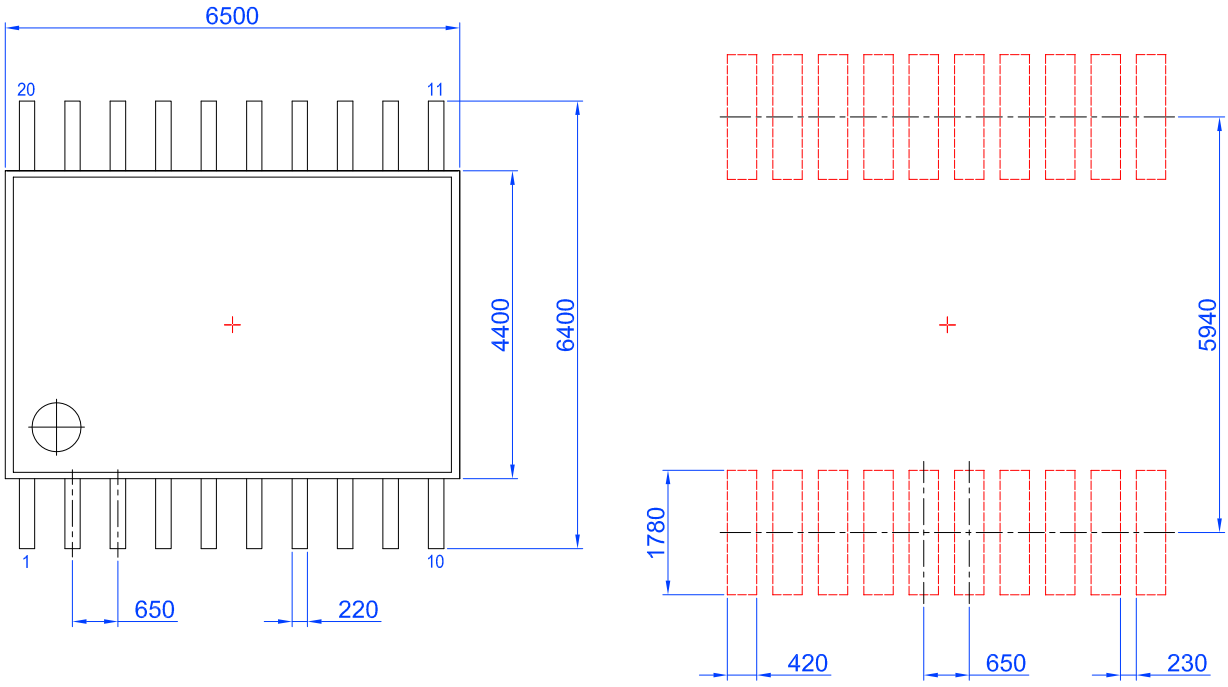


Refer to EIA-481 specification

Note: 1.Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

27 Layout Guidelines

27.1 TSSOP-20



Unit: µm

Glossary

A

ACMP	Analog Comparator
ADC	Analog-to-Digital Converter

B

BG	Bandgap
BW	Bandwidth

C

CH	Channel Selection
CLK	Clock
CNT	Counter
CSB	Chip Select

D

DAC	Digital to Analog Converter
DCMP	Digital Comparator
DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic discharge

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

H

HTOL	High Temperature Operating Life

I

IN	Input
IO	Input/Output

L

LSB	Least Significant Bit
LUT	Look-Up Table

M

MISO, SDO	Master Input Slave Output
MOSI, SDI	Master Output Slave Input

MSB	Most Significant Bit
MUX	Multiplexer

N

nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	One-Time-Programmable
OUT	Output

P

PD	Power-Down
PGA	Programmable Gain Amplifier
PGEN	Pattern Generator
POR	Power-On Reset
PWR	Power
P DLY	Programmable Delay
PWM	Pulse-Width Modulator

R

RTI	Referred to input
RTO	Referred to output

S

SCLK	Serial Clock
SMT	With Schmitt Trigger

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
3.15	7-Apr-2025	Changed the SPI terminology from Controller/Peripheral back to Master/Slave, POCI/PICO back to MISO/MOSI
3.14	20-Mar-2025	Updated figures in sections: Counters/Delay Generators, Delay Mode (Counter Data: 3) CNT/DLY0...CNT/DLY9, Counter Mode (Counter Data: 3) CNT/DLY0...CNT/DLY9, CNT/FSM Mode CNT/DLY2, CNT/DLY4 Fixed typos Updated table heading of table Oscillators Frequency Limits - Temperature Range changed to Ambient Temperature Range Updated table titles of tables EC, Input Leakage Current, ACMP Specifications, Vref OUT Specifications, Delay Estimated for Each ACMP, Single-Ended PGA Operation, Differential PGA Operation, Pseudo-Differential PGA Operation, Differential/Pseudo-Differential PGA Mode - added information about “Typical Values are at T_A = 25 °C” Removed Note from sections Electrical Characteristics, OSC Power-On Delay, ACMP Characteristics, Vref OUT Characteristics, PGA Specifications Updated the terms Master/Slave to Controller/Peripheral, MISO/MOSI to POCI/PICO to comply with the latest SPI standard specification
3.13	11-Dec-2024	Fixed typos Added Note to sections Electrical Characteristics, OSC Power-On Delay, ACMP Characteristics, Vref OUT Characteristics, PGA Specifications Updated Ambient Operating Temperature symbol, T was changed to T_A
3.12	20-Nov-2024	Updated LUT block names to match with Go Configure™ Software Hub Fixed typos Fixed typos in header in table Functional Pin Description Corrected description in subsection Pull-Up/Down Resistors
3.11	25-May-2023	Updated IC Net Weight in section Package Information
3.10	6-Mar-2023	Added notes to section Ordering Information
3.9	15-Feb-2023	Updated ACMP0 Block Diagram
3.8	3-Feb-2023	Updated Package Marking for TSSOP package
3.7	6-Jan-2023	Updated ADC Characteristics Including PGA
3.6	13-Dec-2022	Added additional information about AEC-Q100 Updated table Oscillators Power-On Delay Updated table Vref OUT Specifications Updated data for RC OSC (2 MHz) in table Oscillators Frequency Limits
3.5	28-Jun-2022	Updated tables Vref Range, Vref OUT Specifications, section Analog Comparators
3.4	7-Mar-2022	Updated R_{PUP} and R_{PDWN} in section Electrical Characteristics Corrected table Delay Estimated for Each ACMP Renesas rebranding Corrected POR Initialization and Power Down sections Fixed typos Corrected 4-bit LUTs names
3.3	16-Mar-2020	Corrected Table Electrical Characteristics (V_{IH}, V_{IL}) Added note for CNTs Added Note 3 in Register OE 4x Drive Structure Diagram Fixed typos
3.2	7-Oct-2019	Updated Digital Comparator/Pulse Width Modulator section Updated Block Diagram Fixed typos
3.1	30-Sept-2019	Updated Electrostatic Discharge Ratings

Revision	Date	Description
3.0	27-Sept-2019	Updated ACMP Input Voltage Offset Added Vref OUT Specification Table Updated Oscillator Frequency Limits Updated PGA Typical Performance Section Updated ACMP Maximum Power-On Delay Figures Added IO Typical Performance Section Updated Input Leakage Current Updated PIN Block Diagrams Updated PGA Offset and Gain error for all mode Updated ADC Characteristics (including PGA) Updated graph for ACMP Input Current Source Updated Programmable Delay Expected Delays and Widths Updated Typical Current Consumption Estimated for Each Macrocell table Updated Delay Estimated for Each ACMP table Updated Typical Delay Estimated for Each Macrocell Updated Vref Output Error Updated ACMP Buffer Input Voltage Offset Updated ACMP Gain Error Updated ACMP Startup Time Updated Table EC at T_A = -40 °C to +105 °C, V_{DD} = 1.71 V to 3.6 V, Unless Otherwise Noted Updated Table Oscillators Frequency Limits Updated Figures OSC Power-on Delay Added Figures Oscillators Frequency vs. V_{DD} Updated Table OSC Power-On Corrected Programmable Delay / Edge Detector description and timing diagrams Corrected Oscillator Block Diagram Final version

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
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4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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