RRA70181

Bidirectional, Low-Side and High-Side Voltage Output, Current-Sense Amplifier

Description

The RRA70181 is a single-channel, bidirectional current-sense amplifier optimized for high-side or low-side measurement in space- and power-constrained systems. It maintains accurate operation across -0.2V to +26V common-mode range-independent of supply-and runs from 2.7V to 5.5V. A dedicated REF pin sets the output zero (mid-scale for ±current or a user-defined offset), enabling seamless charge/discharge or source/sink monitoring. A precision matched internal network delivers fixed gains of 20/50/100/200V/V with ≤±1% gain error, while input-referred offset of ≤±150µV at VCM = 0V (≤±500µV at 12V) and ≤1µV/°C drift support small shunt resistors and tight accuracy. Low power draw (≤260µA max IQ), -40°C to +125°C operation, and compact SOT-23-6 package make the RRA70181 ideal for always-on current monitoring in 12V/24V power rails.

Part	Package	Body Size (Nominal)
RRA70181	SOT-23-6	2.90mm×1.60mm

Features

- Wide common-mode range: -0.2V to +26V (supports high-side and low-side sensing)
- High bandwidth: 350kHz small signal (20V/V devices)
- Low offset: ≤±150µV (VCM = 0V), ≤±500µV (VCM = 12V)
- Fast response: 2V/µs output slew rate
- High accuracy: ≤±1% gain error (max); ≤1µV/°C offset drift (max)
- Fixed-gain options: 20/50/100/200V/V
- Low power: ≤260µA quiescent current (per channel)
- Bidirectional current-sensing capability

Applications

- Battery packs and BMS monitoring
- USB C and power delivery power paths
- DC/DC and point-of-load rails
- Hot swap, eFuse, and ORing controllers
- Motor and BLDC drives
- LED lighting drivers
- Solar PV systems and chargers

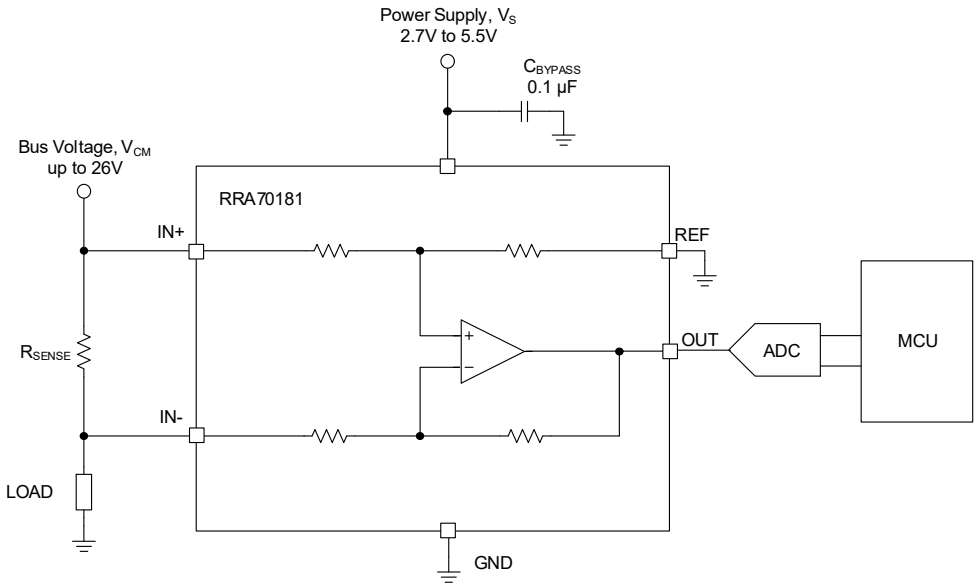

Figure 1. Typical Application Circuit

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1. Overview

1.1 Functional Block Diagram

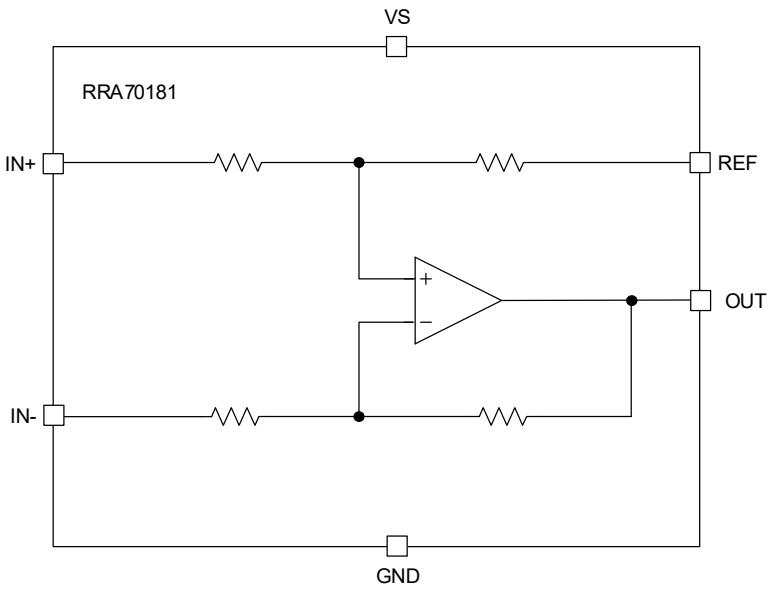


Figure 2. Block Diagram

2. Pin Information

2.1 SOT-23

2.1.1 Pin Assignments

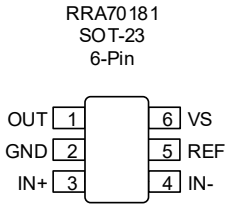


Figure 3. Pin Assignments – Top View

2.1.2 Pin Descriptions

Pin Number	Pin Name	Function
1	OUT	Signal Output
2	GND	Ground
3	IN+	Non-inverting Signal Input
4	IN-	Inverting Signal Input
5	REF	Reference Input
6	VS	Supply Voltage

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by the warranty.

Parameter	Minimum	Maximum	Unit
Supply Voltage, VS	-	6.0	V
Input Voltage, IN to GND (Differential (V_{IN+}) – (V_{IN-}))	-28	28	V
Input Voltage, IN+ to IN- (Common Mode)	(GND) – 0.3	28	V
Output Voltage	(GND) – 0.3	(Vs) + 0.3	V
Output Current	-	±8	mA
Output Short-Circuit	Continuous		mA
Ambient Temperature, T_A	-55	150	°C
Junction Temperature, T_J	-	150	°C
Storage Temperature, T_{stg}	-65	150	°C
Human Body Model (Tested per JS-001)	-	6	kV
Charged Device Model (Tested per JS-002)	-	1.5	kV
Latch-Up (Tested per JESD78; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage, V_S	2.7	5	5.5	V
Common-mode Input Voltage (IN+ and IN-), V_{CM}	-0.2	12	26	V
Ambient Temperature, T_A	-40	-	125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	SOT-23-6	θ_{JA}[1]	Junction to ambient	175	°C/W
		θ_{JC}[2]	Junction to case	120	°C/W

1. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

V_S = 5V, V_{REF} = V_S/2, V_{IN+} = 12V, and V_{SENSE} = V_{IN+} – V_{IN-} at T_A = 25°C, (unless otherwise noted)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Input						
Common-Mode Rejection Ratio	CMRR	V_{IN+} = 0V to 26V, V_{SENSE} = 0mV, T_A = -40°C to 125°C	90	100	-	dB
Input Offset Voltage	V_{OS}	V_{SENSE} = 0mV, VIN+ = 0V	-	±25	±150	µV
		V_{SENSE} = 0mV	-	±100	±500	µV

V_S = 5V, V_{REF} = V_S/2, V_{IN+} = 12V, and V_{SENSE} = V_{IN+} – V_{IN-} at T_A = 25°C, (unless otherwise noted) (Cont.)

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Input Offset Voltage Temperature Coefficient	TCV_{OS}	V_{SENSE} = 0mV, T_A = -40°C to 125°C	-	±0.2	1	µV/°C
Power Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V, VIN+ = 12V, V_{SENSE} = 0mV	-	±8	±40	µV/V
Input Bias Current	I_B	V_{IN+} = 0V, V_{SENSE} = 0mV	-	-6	-	µA
		V_{SENSE} = 0mV	-	75	-	µA
Input Offset Current	I_{OS}	V_{SENSE} = 0mV	-	±0.05	-	µA
Quiescent Current	I_Q	V_{SENSE} = 0mV	-	197	260	µA
		V_{SENSE} = 0mV, T_A = -40°C to 125°C	-	-	300	µA
Output						
Gain	G	RRA70181-2xx	-	20	-	V/V
		RRA70181-5xx	-	50	-	V/V
		RRA70181-8xx	-	100	-	V/V
		RRA70181-9xx	-	200	-	V/V
Gain Error	E_G	V_{OUT} = 0.5V to V_S – 0.5V, T_A = -40°C to 125°C	-	±0.1	±1	%
Gain Error vs Temperature	-	T_A = -40°C to 125°C	-	1.5	20	ppm/°C
Nonlinearity Error	-	V_{OUT} = 0.5V to V_S – 0.5V	-	±0.01	-	%
Maximum Capacitive Load	-	No sustained oscillation	-	1	-	nF
Output Voltage Swing	V_{SP}	Swing to V_S, R_L = 10kΩ to GND, T_A = -40°C to 125°C	-	V_S – 0.02	V_S – 0.03	V
	V_{SN}	Swing to GND, R_L = 10kΩ to GND, T_A = -40°C to 125°C	-	V_{GND} + 0.0005	V_{GND} + 0.005	V
AC Parameters						
Bandwidth	BW	RRA70181-2xx, C_L = 10pF	-	350	-	kHz
		RRA70181-5xx, C_L = 10pF	-	210	-	kHz
		RRA70181-8xx, C_L = 10pF	-	150	-	kHz
		RRA70181-9xx, C_L = 10pF	-	105	-	kHz
Slew Rate	SR	-	-	2	-	V/µs
Noise						
Voltage Noise Density, RTI	e_n	-	-	40	-	nV/√Hz

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Typical Performance Graphs

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V, add V_{REF} = V_S/2(unless otherwise specified)

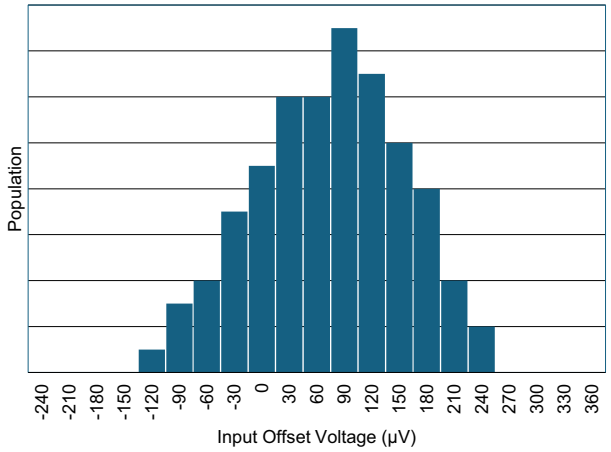


Figure 4. VOS Production Distribution Gain = 20

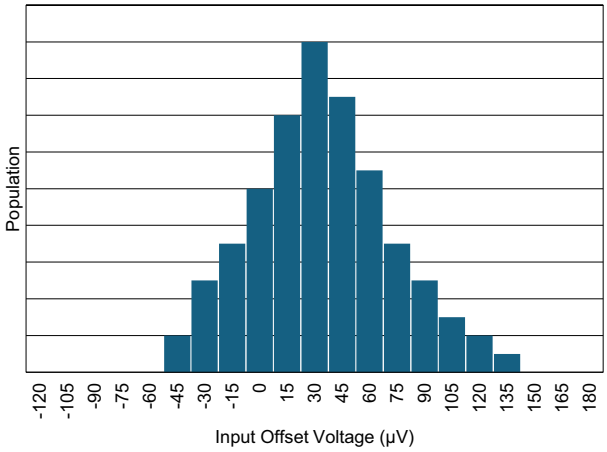


Figure 5. VOS Production Distribution Gain = 50

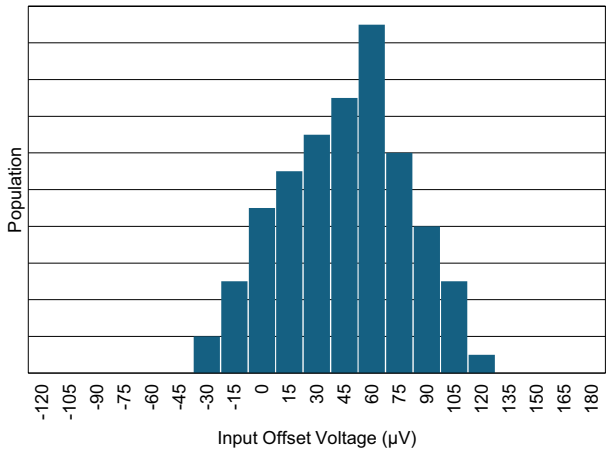


Figure 6. VOS Production Distribution Gain = 100

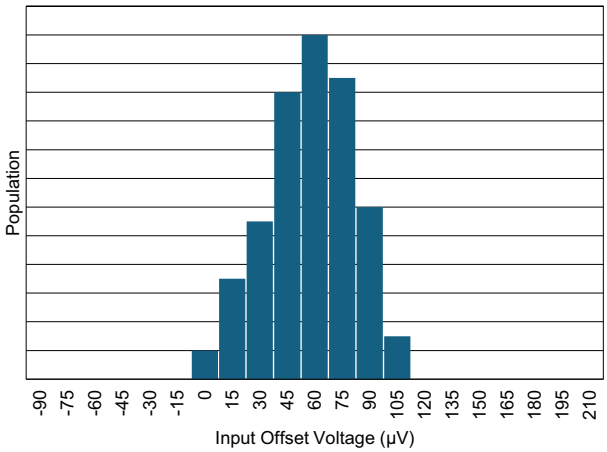


Figure 7. VOS Production Distribution Gain = 200

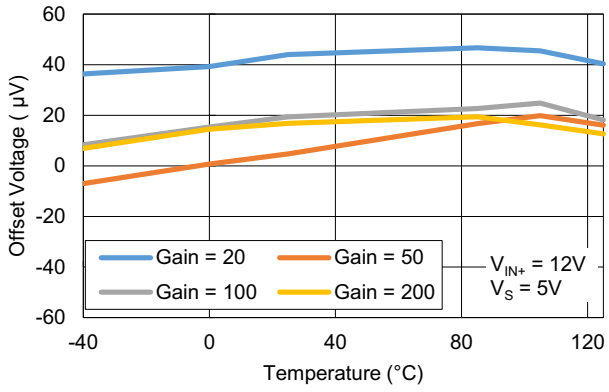


Figure 8. Offset Voltage vs Temperature

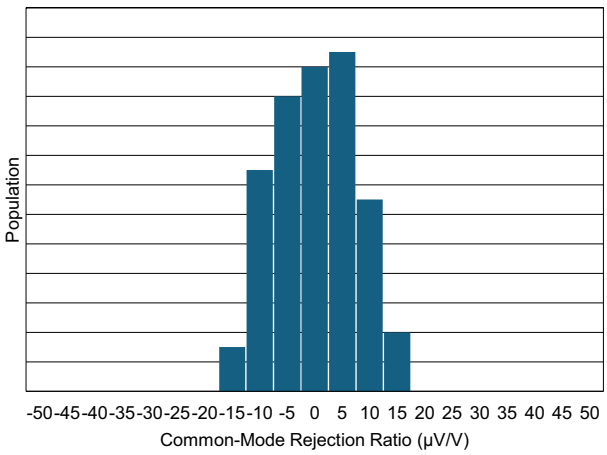


Figure 9. CMRR Production Distribution Gain = 20

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V, add V_{REF} = V_S/2(unless otherwise specified) (Cont.)

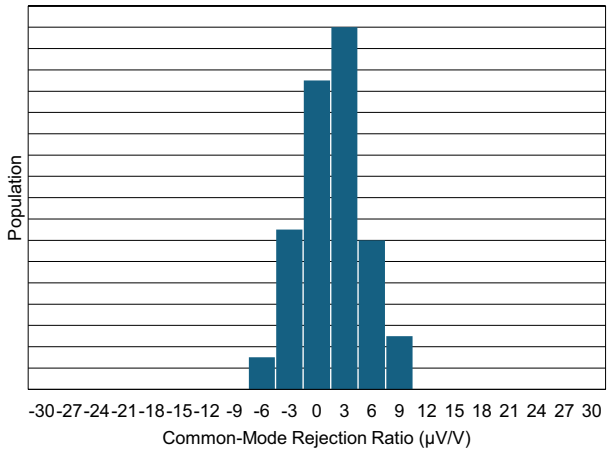


Figure 10. CMRR Production Distribution Gain = 50

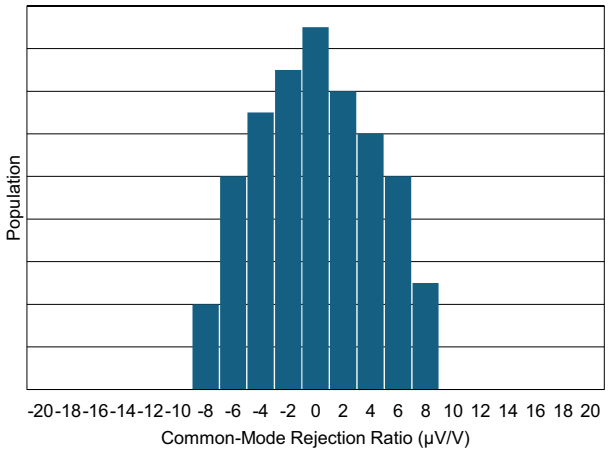


Figure 11. CMRR Production Distribution Gain = 100

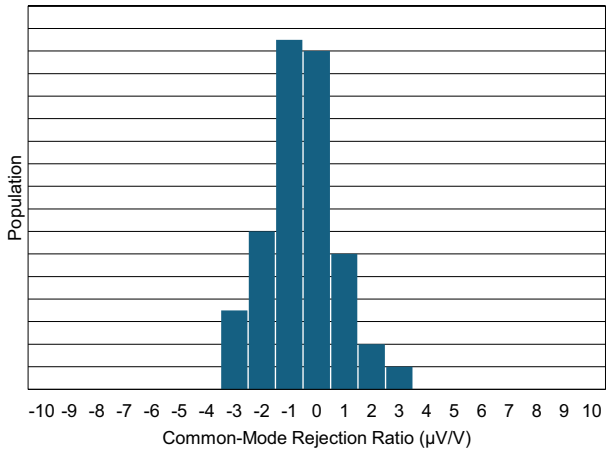


Figure 12. CMRR Production Distribution Gain = 200

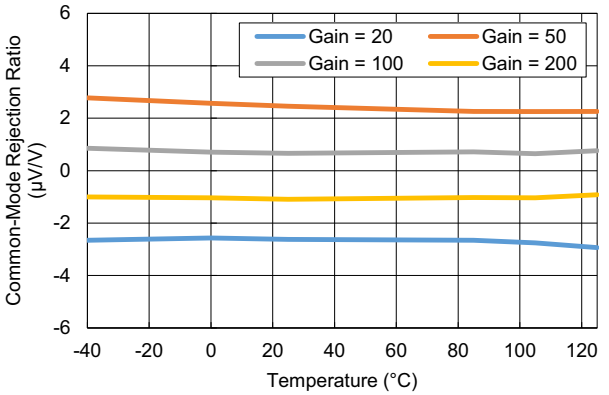


Figure 13. CMRR vs Temperature

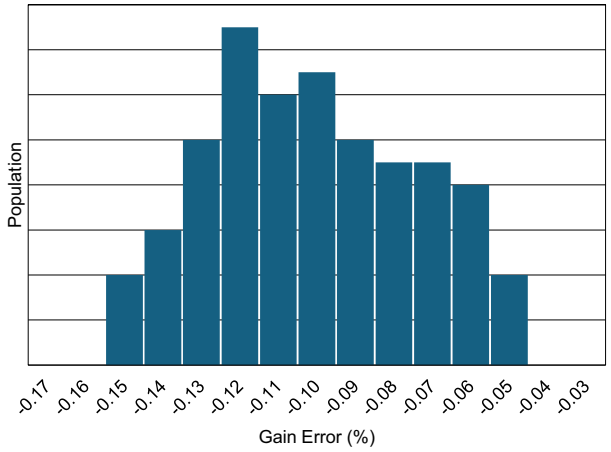


Figure 14. Gain Error Production Distribution Gain = 20

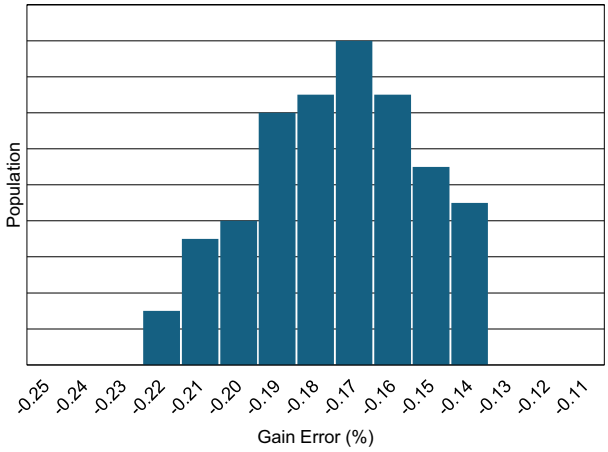


Figure 15. Gain Error Production Distribution Gain = 50

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V, add V_{REF} = V_S/2(unless otherwise specified) (Cont.)

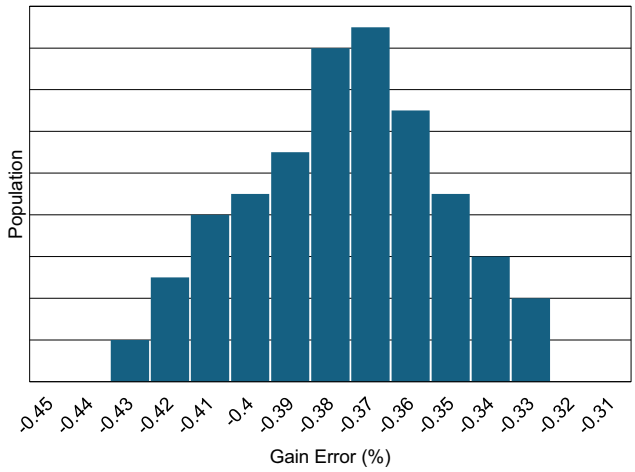


Figure 16. Gain Error Production Distribution Gain = 100

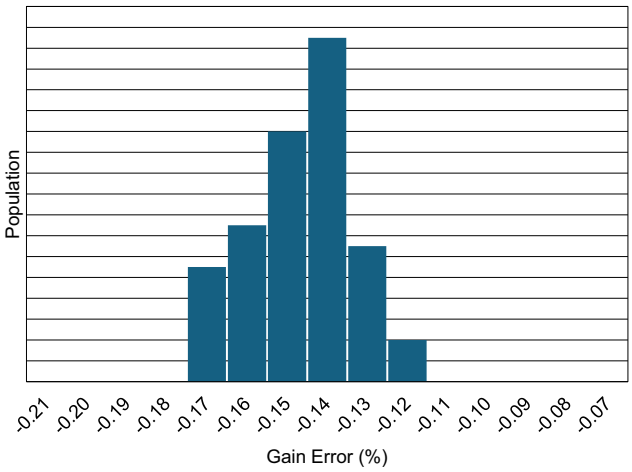


Figure 17. Gain Error Production Distribution Gain = 200

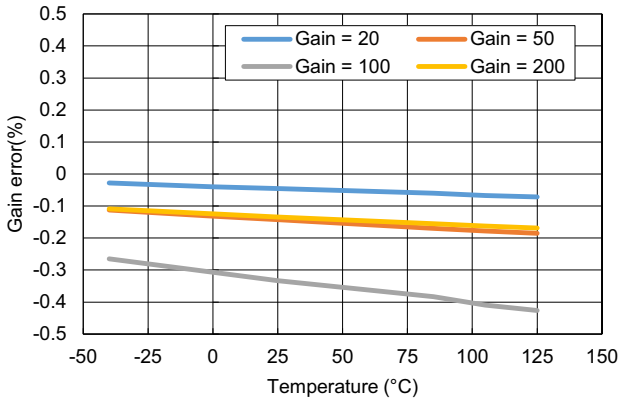


Figure 18. Gain Error vs Temperature

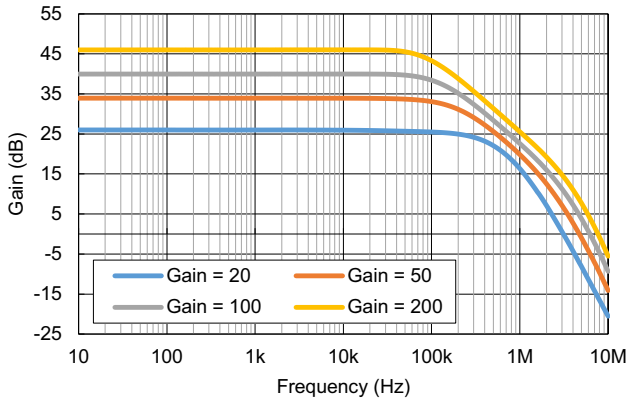


Figure 19. Gain vs Frequency

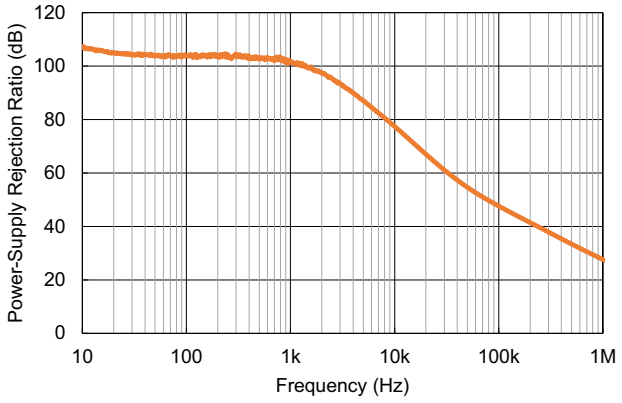


Figure 20. PSRR vs Frequency

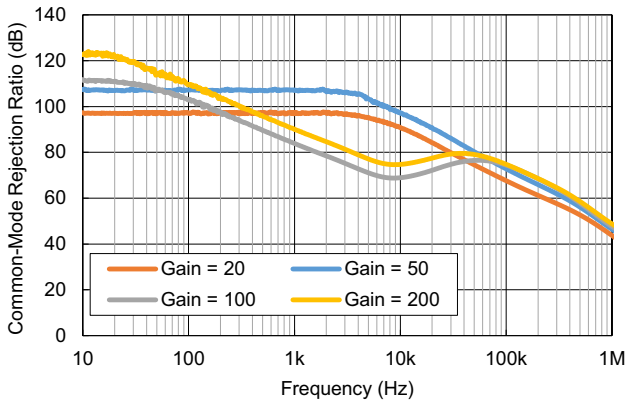


Figure 21. CMRR vs Frequency

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V, add V_{REF} = V_S/2(unless otherwise specified) (Cont.)

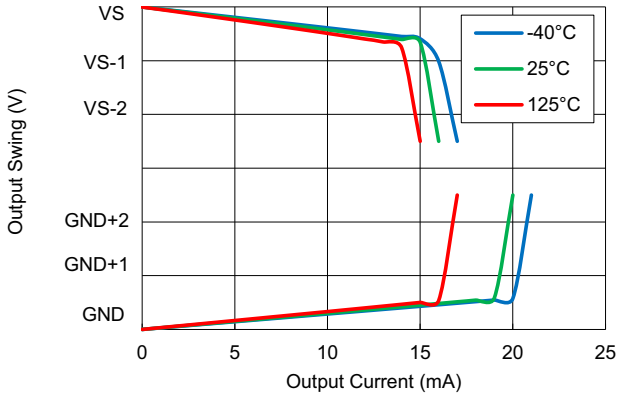


Figure 22. Output Voltage Swing vs Output Current

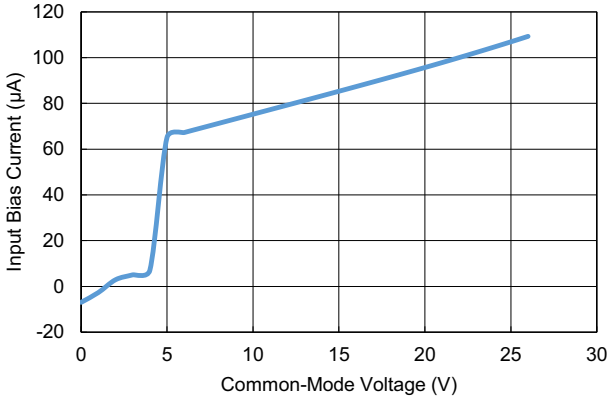


Figure 23. Input Bias Current vs Common-Mode Voltage

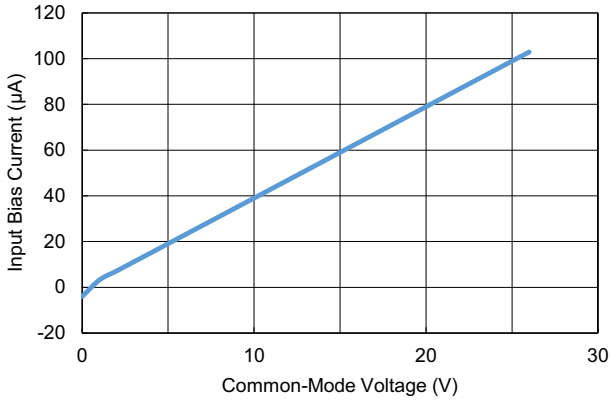


Figure 24. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

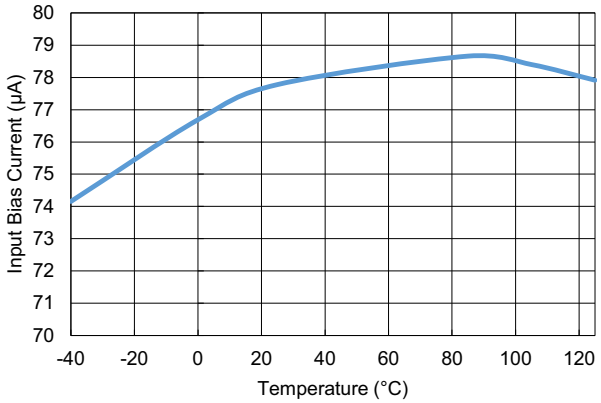


Figure 25. Input Bias Current vs Temperature

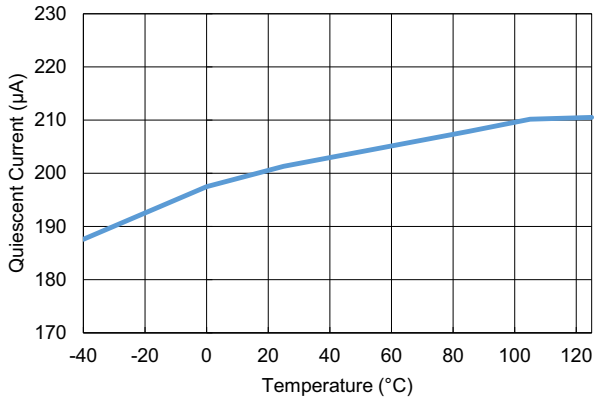


Figure 26. Quiescent Current vs Temperature

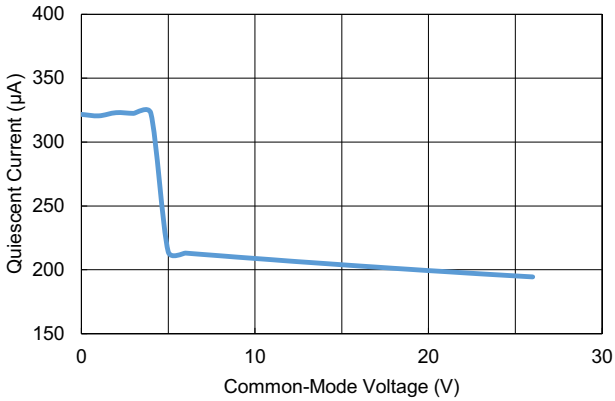


Figure 27. Quiescent Current vs Common-Mode Voltage

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V, add V_{REF} = V_S/2(unless otherwise specified) (Cont.)

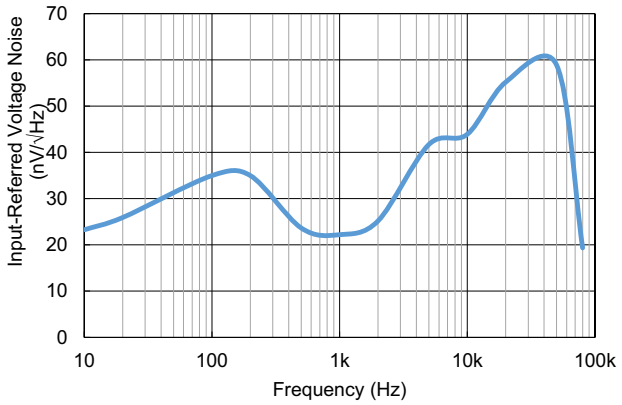


Figure 28. Input Refereed Voltage Noise vs Frequency (G = 100)

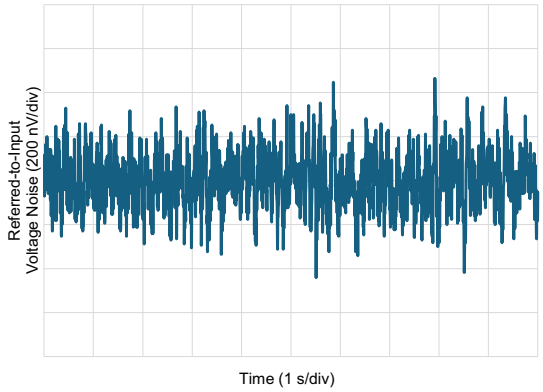


Figure 29. 0.1Hz to 10Hz Voltage Noise (Referred-to-Input)

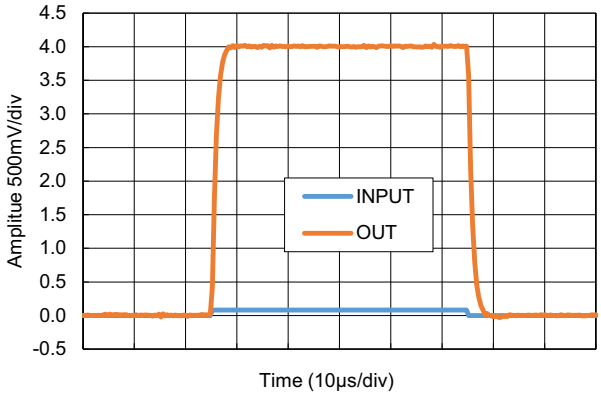


Figure 30. Step Response

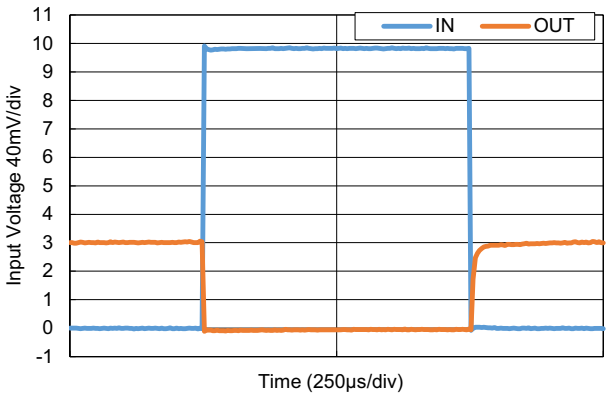


Figure 31. Inverting Differential Input Overload

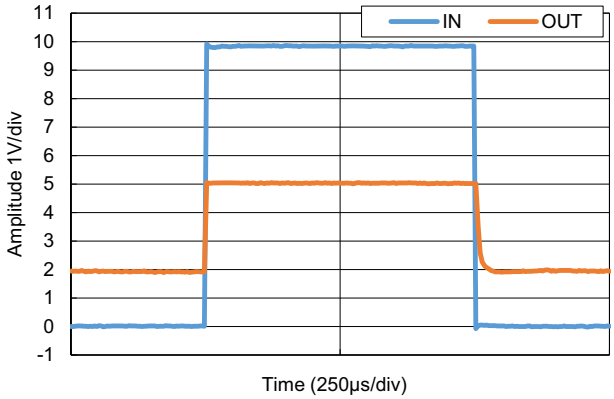


Figure 32. Non-inverting Differential Input Overload

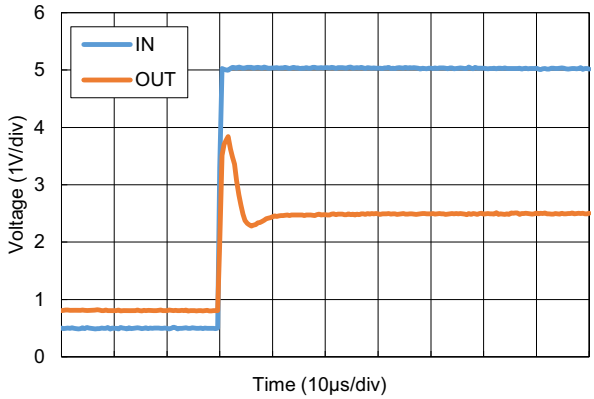


Figure 33. Startup Response

At T_A = 25°C, V_S = 5V, and V_{IN+} = 12V, add V_{REF} = V_S/2(unless otherwise specified) (Cont.)

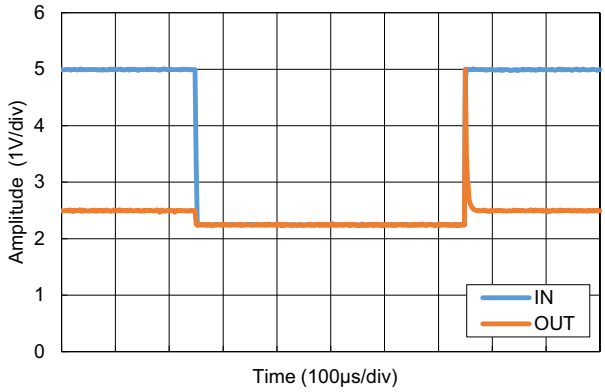


Figure 34. Brownout Recovery

5. Functional Description

5.1 Overview

The RRA70181 is a current-sense amplifier that measures load current indirectly, by amplifying the small differential voltage that develops across an external shunt resistor as current flows through it. The RRA70181's deliberate separation between input common-mode range and supply voltage sets it apart from a general-purpose op amp wired as a difference amplifier. The input stage tolerates common-mode voltages well outside V_S, letting a device powered from a modest low-voltage supply accurately sense current on a bus operating at a significantly higher voltage. This is the foundation for both primary use cases: high-side sensing, with the shunt between the supply and the load, and low-side sensing, with the shunt between the load and ground.

5.2 Common-Mode Range Independent of V_S

Because the input network attenuates the common-mode signal before it reaches the gain stage, V_{CM} can lie above, below, or straddle V_S. This is what makes a single device topology usable for both:

- High-side sensing — Shunt placed between the supply and the load, IN+ on the supply side. V_{CM} tracks the bus voltage and can include transients or ripple riding on that bus.
- Low-side sensing — Shunt placed between the load and ground, IN+ on the load side. V_{CM} stays near ground, isolating the amplifier from bus-voltage transients but inserting a small ground disturbance into the return path.

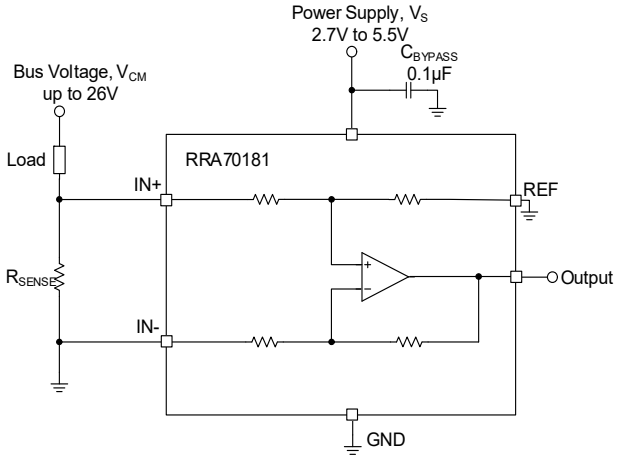


Figure 35. Low-Side Sensing

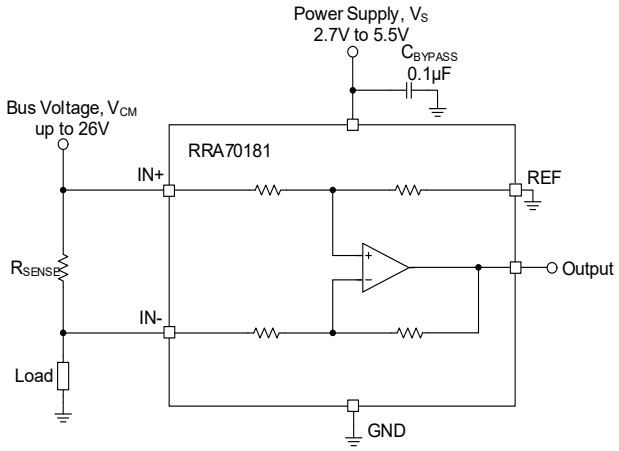


Figure 36. High-Side Sensing

The choice between the two is not just a wiring preference; it is a system-level trade-off between measurement fidelity at the sensed rail and disturbance to the load's ground reference, and it should be made based on what the downstream ADC or control loop can tolerate.

5.3 Bidirectional Sensing Using V_{REF}

The REF pin serves two roles simultaneously: it sets the output's zero-current operating point and determines whether the device is configured for unidirectional or bidirectional current sensing.

Table 1. REF Configuration and Output Behavior

REF Configuration	Output Behavior	Typical Use
Tied to GND	Output rests near 0V at zero current, rises with current in one direction only	Simple overcurrent detection, unidirectional load monitoring
Biased to VS/2	Output centers mid-scale, swings above for one current direction and below for the other	Battery charge/discharge monitoring, bidirectional motor drive
Biased to an intermediate value	Output centers off mid-scale, giving asymmetric headroom	Applications where one current direction is expected to dominate and needs more output range than the other

The governing transfer function is:

(EQ. 1) $$V_{OUT} = I_{LOAD} \times R_{SENSE} \times GAIN + V_{REF}$$

Because REF is buffered internally, it can be driven from a resistor divider or DAC output without loading concerns, though noise on REF appears directly at the output and should be filtered if the reference source is not clean.

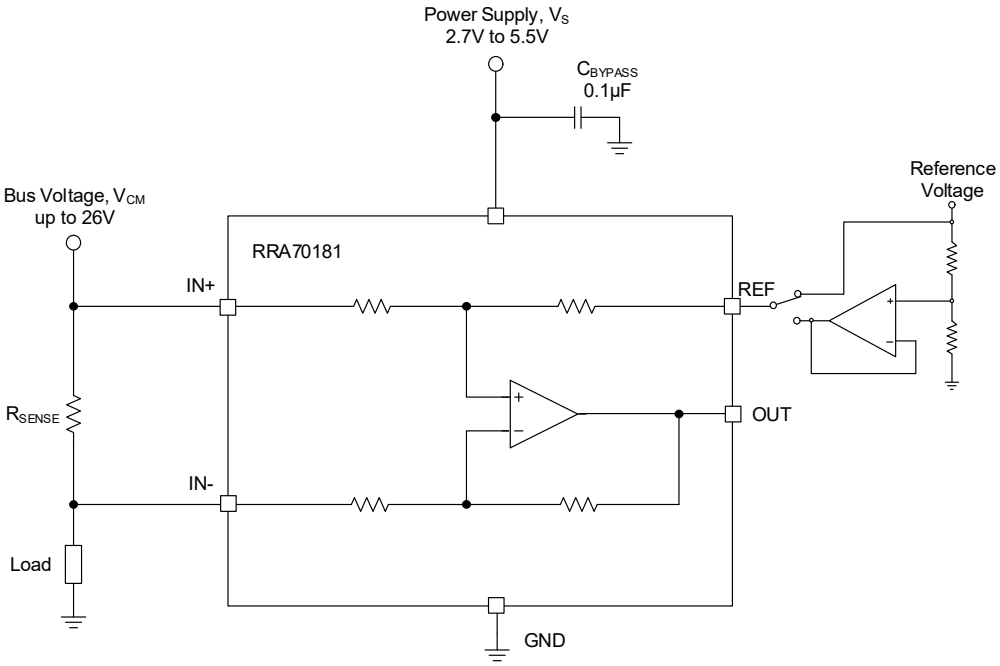


Figure 37. Bidirectional Application

5.4 Bandwidth, Slew Rate, and Transient Response

In continuous monitoring or closed-loop control, bandwidth requires margin above the control loop's own bandwidth so the sense path does not become the limiting element. In fault detection, bandwidth and slew rate together determine how quickly a genuine overcurrent event is flagged to an external comparator; this matters far more for catching brief current pulses than for tracking a slowly varying average.

5.5 Offset Voltage, Gain Accuracy, and Output Swing

Offset voltage, gain accuracy, and output swing interact directly in shunt selection. Offset voltage sets a floor on resolvable current, becoming dominant near the bottom of the range. Gain error scales with signal size, becoming dominant near full scale. Swing limits near the rails constrain how close to either current extreme the output stays linear. A well-chosen R_{SENSE} balances all three: larger improves low-current accuracy but costs power and risks swing limiting at high current; smaller does the reverse.

5.6 Device Functional Modes

Under normal operation, the output is a linear representation of sensed current, provided V_S and V_{CM} stay within their specified ranges and the gained differential signal plus V_{REF} stays within the output's swing limits. Unidirectional and bidirectional behavior are not separate hardware modes; they are the same transfer function, with REF bias determining whether the usable output range covers one current direction or both.

The remaining condition worth understanding is input differential overload: when the differential input times gain would require an output beyond the supply rails, the device saturates the output near the relevant rail rather than producing a corrupted reading. No damage results as long as absolute maximum ratings are not exceeded, and the output resumes tracking accurately within a short recovery interval once the overload clears. Confirm the specific recovery time against the Electrical Specifications if fast-fault response matters to your application.

6. Application Information

The RRA70181 amplifies the voltage across a current-sense resistor as current flows through the load. Because REF can be biased anywhere between GND and V_S, the same basic topology supports unidirectional or bidirectional sensing and high-side or low-side placement. The main design task is selecting R_{SENSE}, gain, and REF bias to fit the target current range and downstream ADC.

6.1 Basic Connection

Connect IN+ and IN– directly across the shunt, keeping the trace length between shunt and inputs as short as practical. Any added resistance in that path shows up directly as gain error. Place a power-supply bypass capacitor as close as possible to VS and GND. If the output feeds an ADC, tie REF to the ADC's reference input (or to GND for the simplest unidirectional case) rather than an unrelated reference, to avoid introducing a ground-offset error between the two devices.

6.2 RSENSE and Gain Selection

Sense resistor selection is a trade-off between accuracy, power dissipation, and output headroom. A practical sequence:

1. Start from the maximum allowable shunt power dissipation to set an upper bound on R_{SENSE}.
2. Confirm $R_{SENSE} \times GAIN \times I_{MAX}$ (plus V_{REF}) does not exceed the positive swing limit.
3. Confirm $R_{SENSE} \times GAIN \times I_{MIN}$ does not undershoot the negative swing limit.
4. If step 1 conflicts with steps 2–3, drop to a lower-gain device grade if available, or accept reduced accuracy at light load.

6.3 Signal Filtering

If the RRA70181 output feeds a high-impedance load such as an ADC, the best place to filter is at the output using a simple RC network, connected from OUT to ground. Filtering here reduces high-frequency noise coming from three sources simultaneously (the common-mode voltage, the sensed differential signal, and the device's own power supply) without disturbing the sense path itself.

If filtering ahead of the amplifier is required instead (for example, to reject switching noise before it reaches the device), the series resistors R_P shown at IN+ and IN– must be kept small, typically under 10Ω. This limit exists because the device's internal input resistance and its input bias currents are not perfectly matched when a differential signal is present. Adding external series resistance at the inputs causes a slightly different voltage drop on each side, which the amplifier reads as a small additional signal showing up as gain error rather than as filtered noise. The larger the added resistance, the larger this error becomes, and the effect is more pronounced on higher-gain versions of the device, since they typically have lower internal input resistance to begin with.

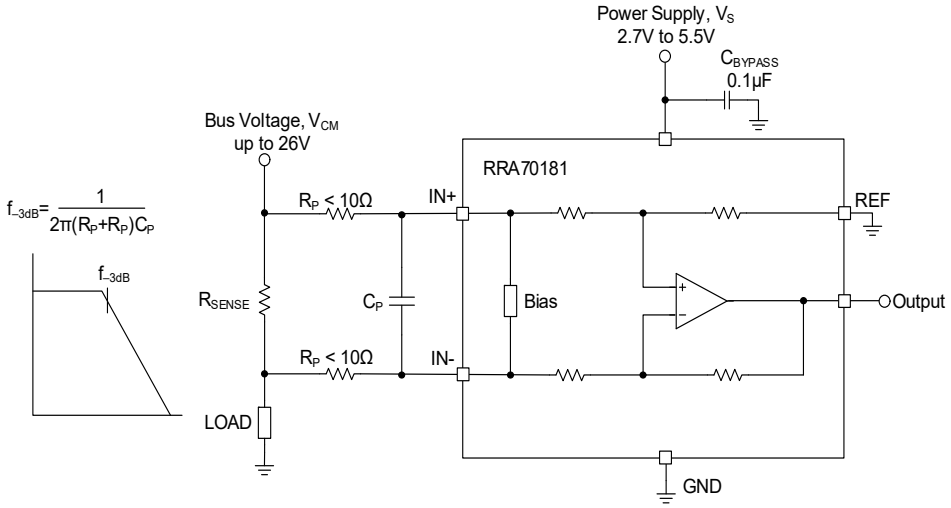


Figure 38. Input Filtering

Quick tip: Filter at the output whenever possible. If input-side filtering is unavoidable, keep the series resistance minimal and treat any value above roughly 10Ω as a deliberate accuracy trade-off rather than a free choice.

6.4 Power Supply Recommendations

The RRA70181's input circuitry is designed to sense voltage differences at common-mode voltages well beyond its own supply rail, the bus being measured can sit as high as 26V while the device itself runs from a supply as low as 2.7V. This is possible because the input stage and the supply pin are functionally independent: the inputs measure relative to the bus, not relative to VS.

The output stage does not share this independence. OUT can only swing within the range set by VS, so no matter how high the sensed bus voltage is, the measurement is always compressed into an output window bounded by the supply. This is why gain and shunt resistor selection matter as much as they do the design task is really about fitting a wide-range input measurement into a supply-limited output window without losing accuracy or headroom.

A power-supply bypass capacitor (0.1µF) should be placed close to the VS and GND pins to keep the local supply clean, especially in applications where the supply itself may be noisy or shared with switching circuitry.

6.5 Transient Protection

In applications where the sensed bus can experience transients beyond the device's normal common-mode range: automotive load dump, hot-plug events, or inductive switching spikes, additional protection ahead of the inputs is required. Two configurations, shown in the reference schematics, cover the two most common cases:

6.5.1 Dual-Zener Diodes

In this configuration, IN+ and IN– each have their own diode running independently to ground. This is the simplest and most board-space-efficient option, and it's sufficient whenever the expected transient energy is within what a low-power Zener (or Zener-type transient absorber) can safely dissipate. Only Zener-type diodes should be used, general-purpose TVS protection devices introduce a response delay that is too slow to protect a fast, low-level analog input (see Figure 39).

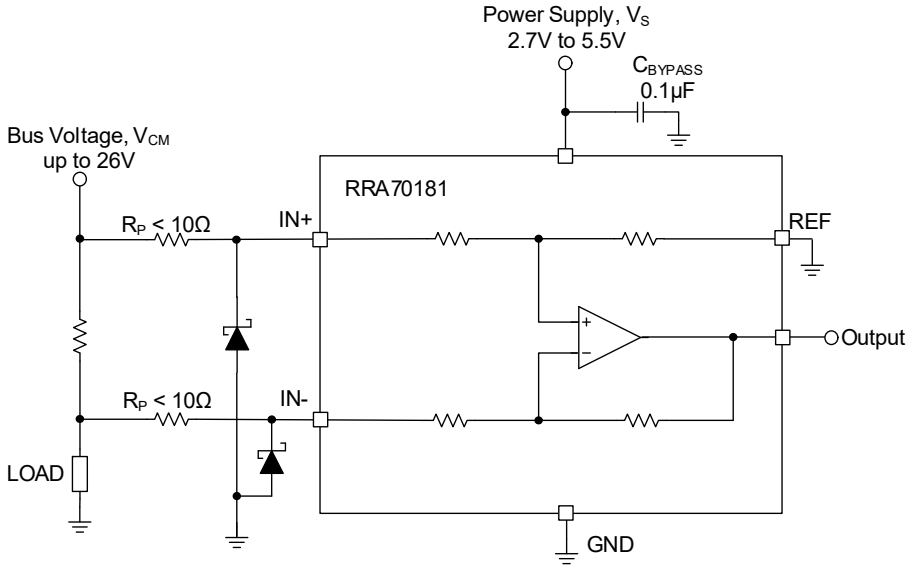


Figure 39. Transient Protection Using Dual-Zener Diodes

6.5.2 Transorb with Back-to-Back Input Clamps

When the expected transient energy exceeds what a low-power Zener diode can absorb, a higher-power transient absorber (transorb) is used instead, combined with a pair of back-to-back diodes connected directly between IN+ and IN–. The back-to-back pair clamps the differential voltage between the two inputs to each other, while the transorb clamps the shared node to ground. This configuration handles larger transient events at the cost of slightly more board space than the dual-Zener option (see Figure 40).

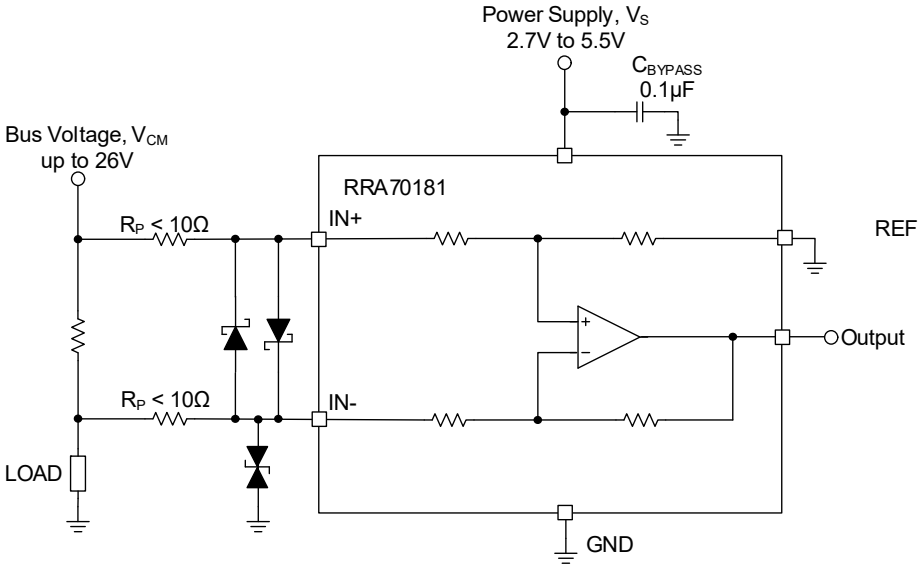


Figure 40. Transient Protection Using a Single Transorb (TVS Diode) and Input Clamps

In both configurations, the series resistors R_P (< 10Ω) ahead of each input serve two purposes: they limit the current flowing into the clamping diode(s) during a transient, and they provide the working impedance the diode needs in order to clamp effectively in the first place. R_P needs to stay small enough to avoid adding measurable gain error, while still being present to do its protective job.

Renesas recommends starting with the dual-Zener option for board-space-constrained designs where the transient profile is well-characterized and modest in energy. Move to the transorb-with-back-to-back-clamps option when transient energy exceeds Zener capability, or when the application (automotive, industrial) demands a higher margin of protection.

6.6 Layout Guidelines

- Use a Kelvin (4-wire) connection from the shunt to IN+/IN– so only the shunt's own resistance appears in the sensed signal; shared trace or via resistance adds directly to measurement error, which matters most given typical sub-ohm shunt values.
- Place the bypass capacitor as close as possible to VS and GND.
- Keep shunt-to-input traces short and symmetric to avoid an impedance mismatch between IN+ and IN–.
- If REF is grounded rather than actively driven, tie it to the same local ground node as GND, not a separate ground plane region, to avoid a ground-offset error at the output.

7. Package Outline Drawings

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1][2]	Part Marking	Gain	# Channels	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RRA70181-2PF	1812[5]	20	1	6 Ld SOT-23	P6.064	Reel, 3k units	-40 to 125°C
RRA70181-5PF	1815[5]	50					
RRA70181-8PF	1818[5]	100					
RRA70181-9PF	1819[5]	200					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 1. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.
5. The part marking is located on the bottom of the part.

9. Revision History

Revision	Date	Description
1.01	Nov 5, 2026	Updated typo on Figures 35, 36, and 38.
1.00	Aug 3, 2026	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRA70181-2PF	6	SOT-23	P6.064/KA0006AA
RRA70181-5PF	6	SOT-23	P6.064/KA0006AA
RRA70181-8PF	6	SOT-23	P6.064/KA0006AA
RRA70181-9PF	6	SOT-23	P6.064/KA0006AA

A.2 Symbol Pin Information

A.2.1 6-SOT-23

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	OUT	Output	-
2	GND	Power	-
3	IN+	Input	-
4	IN-	Input	-
5	REF	Input	-
6	VS	Power	-

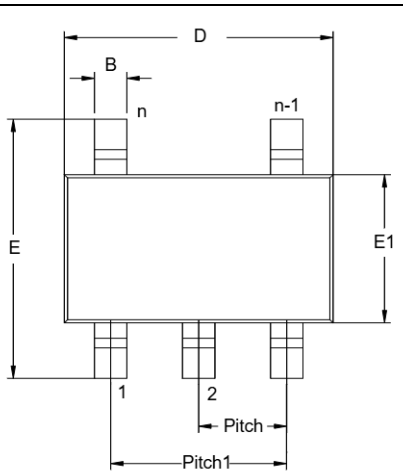
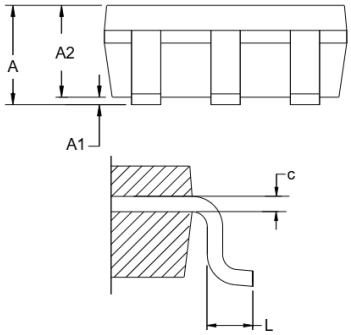
A.3 Symbol Parameters

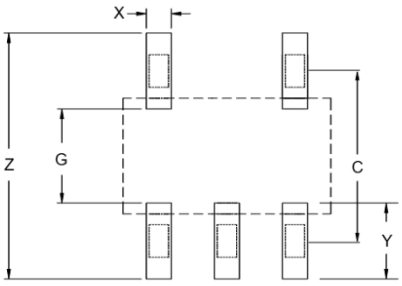
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Slew Rate
RRA70181-2PF	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs
RRA70181-5PF	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs
RRA70181-8PF	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs
RRA70181-9PF	Commercial	SMD	Compliant	-40 °C	125 °C	2.7 V	5.5 V	2 V/µs

A.4 Footprint Design Information

A.4.1 6-SOT-23

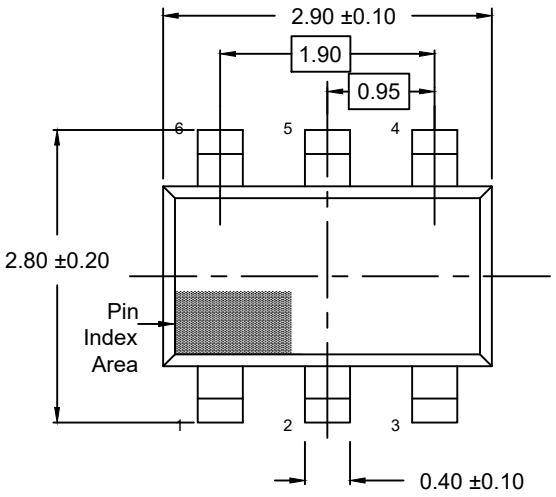
IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOT23	P6.064/KA0006AA	6

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.80	 Bottom View  Side View
Maximum body span (vertical side)	Dmax	3.00	
Minimum lead span (horizontal side)	Emin	2.60	
Maximum lead span (horizontal side)	Emax	3.00	
Minimum lead width	Bmin	0.30	
Maximum lead width	Bmax	0.50	
Minimum body width (horizontal side)	E1min	1.50	
Maximum body width (horizontal side)	E1max	1.70	
Number of leads: 3, 4, 5 or 6	PinCount	6	
Comma separated list showing pin sequence (Na,Nb,...). Example: 1,2,3 or 1,2,3,4,5,6 or 5,4,1,3,2	PinOrder	1,2,3,4,5,6	
Distance between the center of any two adjacent pins	Pitch	0.95	
Overall pitch (e1)	Pitch1	1.90	
Maximum Height	Amax	1.45	
Minimum standoff height	A1min	0.00	
Maximum body height	A2max	1.30	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.22	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.55	

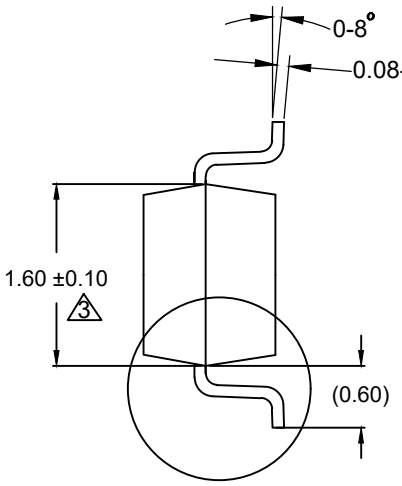
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between pads. Measured from outside edges	Z	3.60	 PCB Top View
Distance between pads. Measured from inside edges	G	1.20	
Pad width	X	0.60	
Pad length	Y	1.20	
Row spacing. Distance between pad centers	C	2.40	

Package Outline Drawing

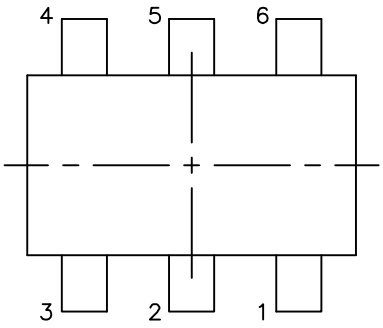
P6.064
KA0006AB
6L-SOT 2.90 x 1.60 x 1.45 mm Body, 0.95 mm Pitch, 6 Lead Small Outline Transistor Plastic Package
Rev. 06, Jul 22, 2026



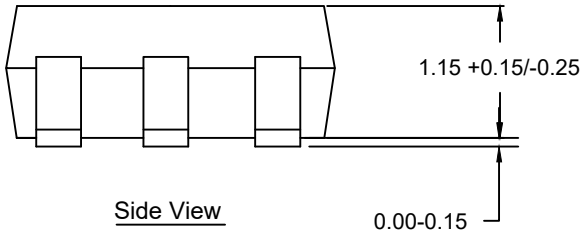
Top View



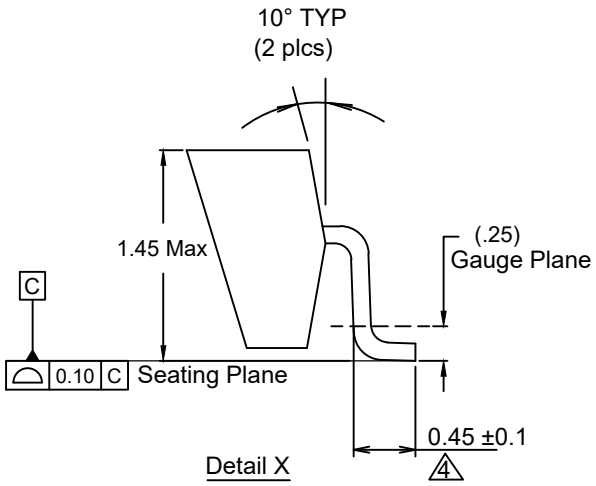
See Detail X
End View



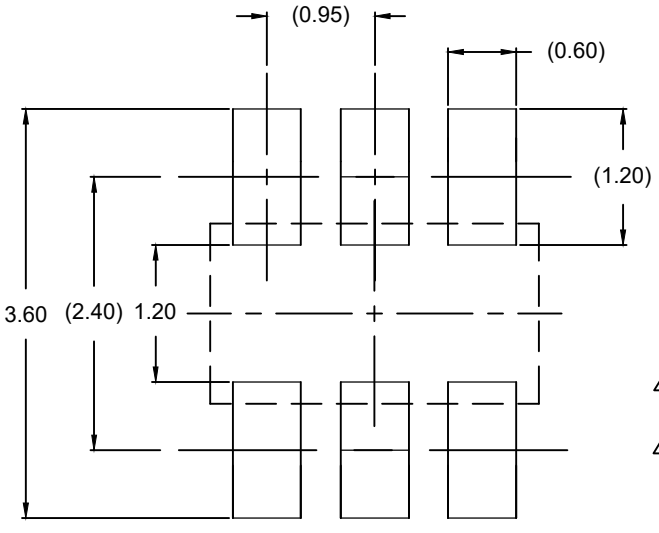
Bottom View



Side View



Detail X



Typical Recommended Land Pattern

Note:

1. Dimensions and tolerances are as per ASME Y14.5M-1994.
2. Dimensions are in mm.
   Dimensions in ( ) are for reference only.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. Package conforms to JEDEC MO-178AB.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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